

TPS79501-Q1 Automotive, Ultra-Low Noise, High-PSRR, Fast, RF, 500mA Low-Dropout Linear Regulator

1 Features

- Qualified for Automotive Applications
- 500mA Low-Dropout Regulator With Enable
- High PSRR (50dB at 10kHz)
- Stable With a 1 μ F Ceramic Capacitor
- Excellent Load/Line Transient Response
- Low Dropout Voltage (110mV at Full Load)
- For a more updated portfolio device, see the [TPS745-Q1](#)

2 Applications

- Short/medium range radar
- Automotive camera
- Automotive display
- Head unit & digital cockpit

3 Description

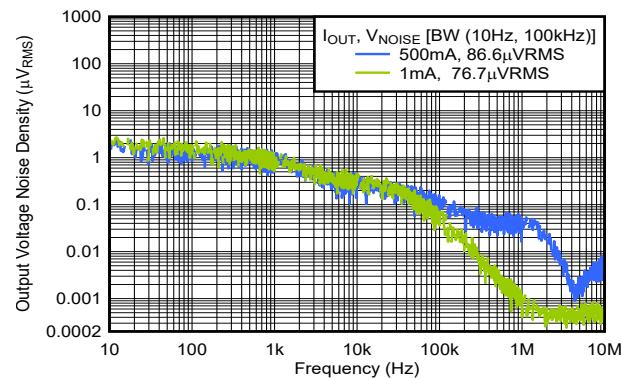
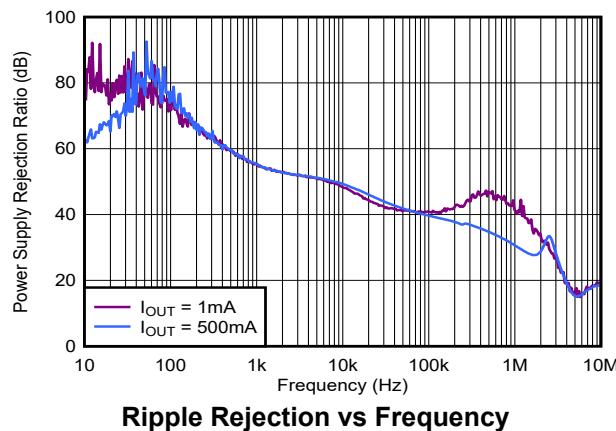
The TPS79501-Q1 low-dropout (LDO), low-power linear voltage regulator features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline SON package. The device is stable with a small 1 μ F ceramic capacitor on the output. The TPS79501-Q1 offers low dropout voltages (for example, 110mV at 500mA). Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high-PSRR and low-noise features, as well as from the fast response time.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TPS79501-Q1	DRB (VSON, 8)	3.00mm × 3.00mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

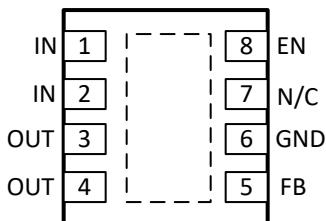


Figure 4-1. DRB Package 8-Pin VSON With Exposed Thermal Pad Top View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	VSON		
EN	8	Input	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	Input	Feedback input voltage.
GND	6	—	Regulator ground
IN	1, 2	Input	Input to the device.
N/C	7	—	No internal connection
OUT	3, 4	Output	Regulator output
Thermal Pad	Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, V_{IN} (New chip)	-0.3	6.5	V
	Supply, V_{IN} (Legacy chip)	-0.3	6	
	Enable, V_{EN}	-0.3	$V_{IN} + 0.3$	
	Output, V_{OUT}	-0.3	6	
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J	-40	150	°C
	Storage, T_{stg}	-65	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{IN}	Input supply voltage (legacy chip)		2.7	5.5	6.0	V
	Input supply voltage (new chip)		2.7	5.5		
C _{IN}	Input capacitor		2.2			μF
C _{OUT}	Output capacitor		1 ⁽¹⁾	200		
C _{FF}	Feed-forward capacitor (new chip)		0	10	100	nF
I _{OUT}	Output current		0	500		mA
V _{EN}	Enable voltage (legacy chip)		0	5.5	6.0	V
	Enable voltage (new chip)		0	5.5		
F _{EN}	Enable toggle frequency (new chip)				10	kHz
T _j	Junction Temperature		–40	125		°C

(1) The minimum effective capacitance is 0.47 μF.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS795-Q1		UNIT	
		DRB (VSON)			
		8 PINS ⁽²⁾	8 PINS ⁽³⁾		
R _{θJA}	Junction-to-ambient thermal resistance	47.8	54.7	°C/W	
R _{θJC(top)}	Junction-to-case (top) thermal resistance	83	76.1	°C/W	
R _{θJB}	Junction-to-board thermal resistance	N/A	30.1	°C/W	
Ψ _{JT}	Junction-to-top characterization parameter	2.1	6.6	°C/W	
Ψ _{JB}	Junction-to-board characterization parameter	17.8	30.2	°C/W	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	12.1	16.7	°C/W	

- (1) For more information about traditional and new thermal metrics, see the "Semiconductor and IC Package Thermal Metrics" application note.
 (2) Legacy chip.
 (3) New chip.

5.5 Electrical Characteristics

at operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{\text{EN}} = V_{\text{IN}}$, $V_{\text{IN}} = V_{\text{OUT}(\text{nom})} + 1\text{V}$ (1), $I_{\text{OUT}} = 1\text{mA}$, and $C_{\text{OUT}} = 10\mu\text{F}$ and $C_{\text{NR}} = 0.01\mu\text{F}$ (Legacy Chip only), unless otherwise noted. All typical values at $T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	Legacy chip		2.7	5.5		V
		New chip		2.7	6.0		
I_{OUT}	Continuous output current			0	500	mA	
V_{FB}	Internal reference			1.2	1.225	1.25	V
V_{OUT}	Output voltage range			1.225		5.5 V_{DO}	V
V_{OUT}	Output accuracy	$0\mu\text{A} \leq I_{\text{OUT}} \leq 500\text{mA}$, $V_{\text{OUT}(\text{nom})} + 1\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$ (1) (legacy chip)		0.98 $V_{\text{OUT}(\text{nom})}$	1.02 $V_{\text{OUT}(\text{nom})}$		%
		$0\mu\text{A} \leq I_{\text{OUT}} \leq 500\text{mA}$, $V_{\text{OUT}(\text{nom})} + 1\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$ (1) (new chip)		0.975 $V_{\text{OUT}(\text{nom})}$	1.02 $V_{\text{OUT}(\text{nom})}$		
$\Delta V_{\text{OUT}}/\Delta V_{\text{IN}}$	Line regulation	$V_{\text{OUT}} + 1\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$			0.05	0.12	%/V
$\Delta V_{\text{OUT}}/\Delta I_{\text{OUT}}$	Load regulation	$0\mu\text{A} \leq I_{\text{OUT}} \leq 500\text{mA}$			3		mV
V_{DO}	Dropout voltage	$V_{\text{IN}} = V_{\text{OUT}} - 0.1\text{V}$	$I_{\text{OUT}} = 500\text{mA}$		110	170	mV
I_{CL}	Output current limit	$V_{\text{OUT}} = 0$ (legacy chip)		2.4	2.8	4.2	A
I_{CL}	Output current limit	$V_{\text{IN}} = V_{\text{OUT}(\text{nom})} + 1.25\text{V}$ or 2.0V (whichever is greater), $V_{\text{OUT}} = 0.9xV_{\text{OUT}(\text{nom})}$ (new chip only)		1.04		1.65	A
I_{SC}	Short-circuit current limit	$V_{\text{OUT}} = 0$ (new chip only)			550		mA
I_{GND}	Ground current	$0\mu\text{A} \leq I_{\text{OUT}} \leq 500\text{mA}$ (legacy chip)			265	385	μA
I_{GND}	Ground current	$0\mu\text{A} \leq I_{\text{OUT}} \leq 500\text{mA}$ (new chip)			500	900	μA
I_{SHDN}	Shutdown current	$V_{\text{EN}} = 0\text{V}$, $2.7\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$			0.07	1	μA
I_{FB}	Feedback pin current	$V_{\text{FB}} = 1.225\text{V}$				1	μA
PSRR	Power-supply rejection ratio	$f = 100\text{Hz}$, $I_{\text{OUT}} = 10\text{mA}$ (legacy chip)		59			dB
		$f = 100\text{Hz}$, $I_{\text{OUT}} = 10\text{mA}$ (new chip)		64			
		$f = 100\text{Hz}$, $I_{\text{OUT}} = 500\text{mA}$ (legacy chip)		58			
		$f = 100\text{Hz}$, $I_{\text{OUT}} = 500\text{mA}$ (new chip)		50			
		$f = 10\text{kHz}$, $I_{\text{OUT}} = 500\text{mA}$ (legacy chip)			39		
		$f = 10\text{kHz}$, $I_{\text{OUT}} = 500\text{mA}$ (new chip)					
		$f = 100\text{kHz}$, $I_{\text{OUT}} = 500\text{mA}$ (legacy chip)					
		$f = 100\text{kHz}$, $I_{\text{OUT}} = 500\text{mA}$ (new chip)					
V_n	Output noise voltage	$BW = 100\text{Hz}$ to 100kHz , $I_{\text{OUT}} = 500\text{mA}$	$C_{\text{NR}} = 0.001\mu\text{F}$	46			μV_{RMS}
			$C_{\text{NR}} = 0.0047\mu\text{F}$	41			
			$C_{\text{NR}} = 0.01\mu\text{F}$	35			
			$C_{\text{NR}} = 0.1\mu\text{F}$	33			
		$BW = 10\text{Hz}$ to 100kHz , $I_{\text{OUT}} = 500\text{mA}$	New Chip	78			
t_{str}	Time, start-up	$R_L = 6\Omega$, $C_{\text{OUT}} = 1\mu\text{F}$	$C_{\text{NR}} = 0.001\mu\text{F}$	50			μs
			$C_{\text{NR}} = 0.0047\mu\text{F}$	75			
			$C_{\text{NR}} = 0.01\mu\text{F}$	110			
			new chip	550			
I_{EN}	Enable pin current	$V_{\text{EN}} = 0\text{V}$		-1	1	μA	
R_{PULLDOWN}	Pulldown resistance	$V_{\text{IN}} = 3.3\text{V}$ (new chip only)			100		Ω
V_{UVLO}	UVLO threshold	V_{IN} rising (legacy chip)		2.25	2.65		V
		V_{IN} rising (new chip)		1.28	1.62		
$V_{\text{UVLO(HYST)}}$	UVLO hysteresis	V_{IN} hysteresis (legacy chip)			100		mV
		V_{IN} hysteresis (new Chip)			130		

5.5 Electrical Characteristics (continued)

at operating temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), $V_{\text{EN}} = V_{\text{IN}}$, $V_{\text{IN}} = V_{\text{OUT}(\text{nom})} + 1\text{V}$ ⁽¹⁾, $I_{\text{OUT}} = 1\text{mA}$, and $C_{\text{OUT}} = 10\mu\text{F}$ and $C_{\text{NR}} = 0.01\mu\text{F}$ (Legacy Chip only), unless otherwise noted. All typical values at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{EN(HI)}}$	High-level enable input voltage	$2.7V^{(1)} \leq V_{\text{IN}} \leq 5.5\text{V}$ (legacy chip)	1.7			V_{IN}
		$2.7V^{(1)} \leq V_{\text{IN}} \leq 5.5\text{V}$ (new chip)	0.85			
$V_{\text{EN(LOW)}}$	Low-level enable input voltage	$2.7V^{(1)} \leq V_{\text{IN}} \leq 5.5\text{V}$ (legacy chip)			0.7	V
		$2.7V^{(1)} \leq V_{\text{IN}} \leq 5.5\text{V}$ (new chip)			0.425	

(1) Minimum $V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$ or 2.7V , whichever is greater.

5.6 Typical Characteristics

at $V_{\text{EN}} = V_{\text{IN}}$, $V_{\text{IN}} = V_{\text{OUT}(\text{nom})} + 1\text{V}$, $I_{\text{OUT}} = 1\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{NR}} = 0.01\mu\text{F}$, $C_{\text{IN}} = 2.2\mu\text{F}$, and $T_J = 25^\circ\text{C}$ (unless otherwise noted)

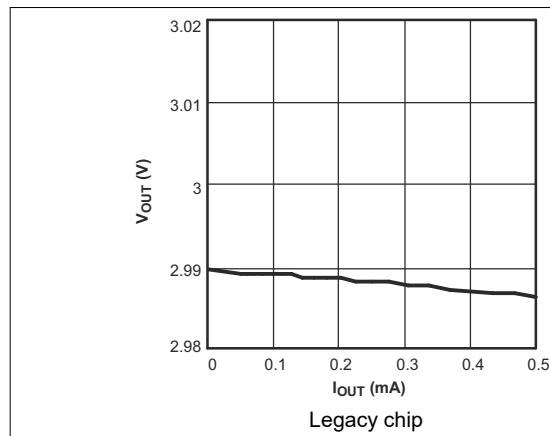


Figure 5-1. TPS795-Q1 Output Voltage vs Output Current

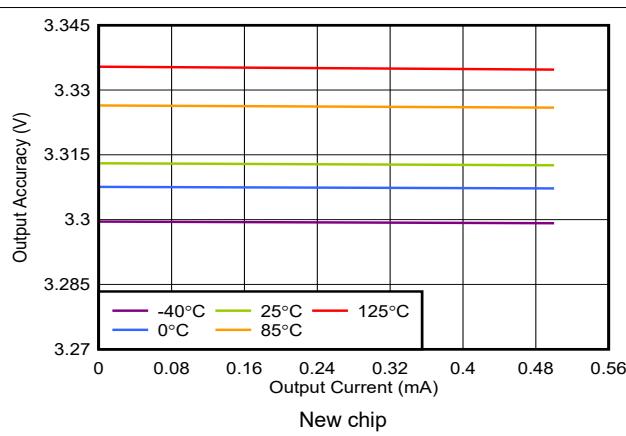


Figure 5-2. TPS795-Q1 Output Voltage vs Output Current

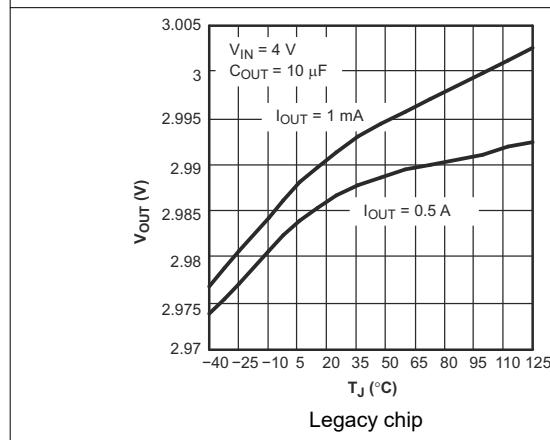


Figure 5-3. TPS795-Q1 Output Voltage vs Junction Temperature

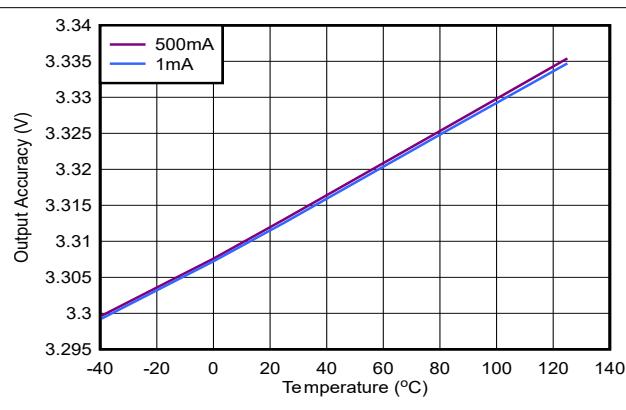


Figure 5-4. TPS795-Q1 Output Voltage vs Junction Temperature

5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25^{\circ}C$ (unless otherwise noted)

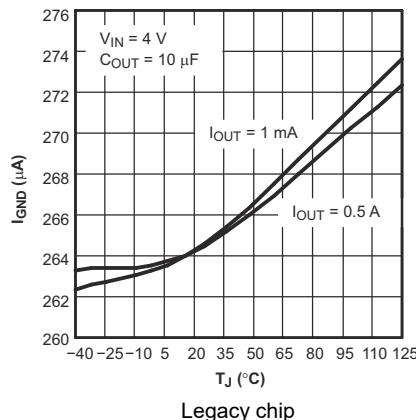


Figure 5-5. TPS795-Q1 Ground Current vs Junction Temperature

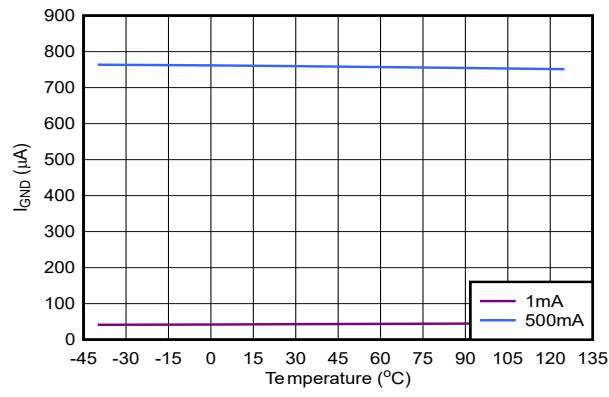


Figure 5-6. TPS795-Q1 Ground Current vs Junction Temperature

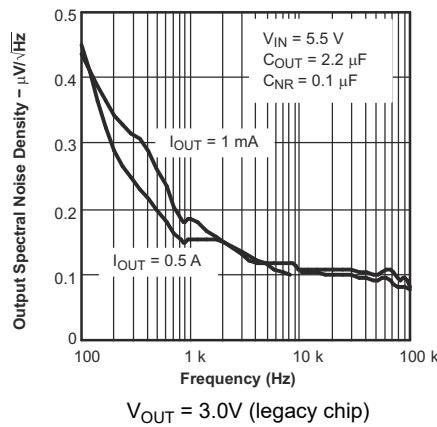


Figure 5-7. TPS795-Q1 Output Spectral Noise Density vs Frequency

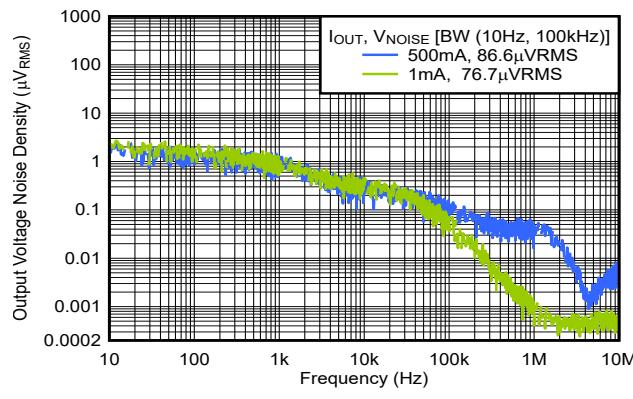


Figure 5-8. TPS795-Q1 Output Spectral Noise Density vs Frequency

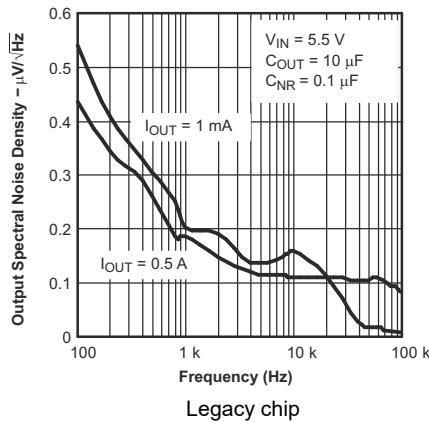


Figure 5-9. TPS795-Q1 Output Spectral Noise Density vs Frequency

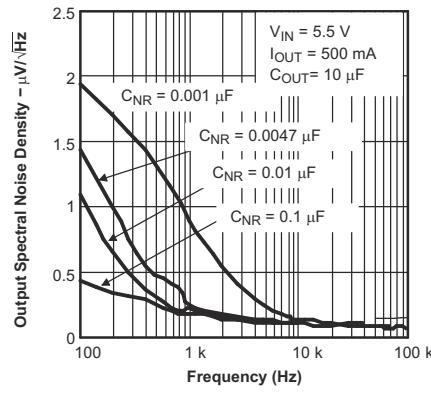


Figure 5-10. TPS795-Q1 Output Spectral Noise Density vs Frequency

5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25^{\circ}C$ (unless otherwise noted)

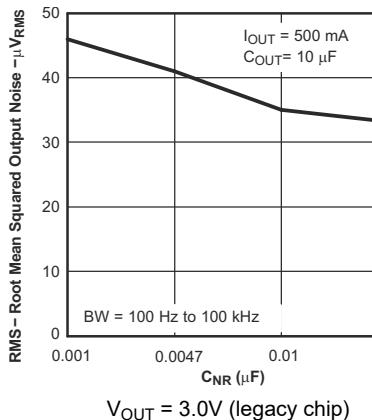


Figure 5-11. TPS795-Q1 Root Mean Squared Output Noise vs C_{NR}

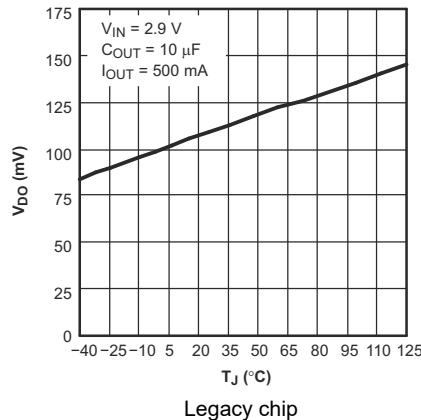


Figure 5-12. TPS795-Q1 Dropout Voltage vs Junction Temperature

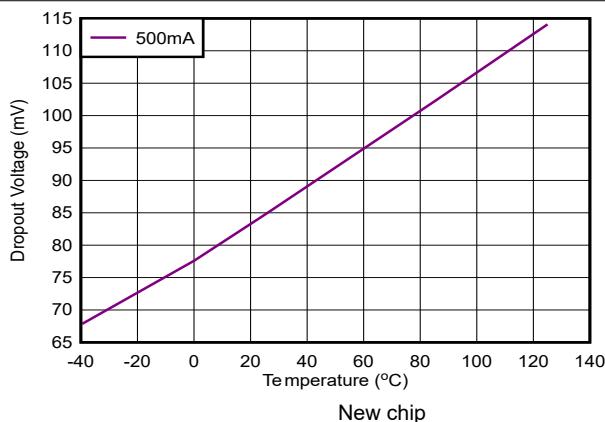


Figure 5-13. TPS795-Q1 Dropout Voltage vs Junction Temperature

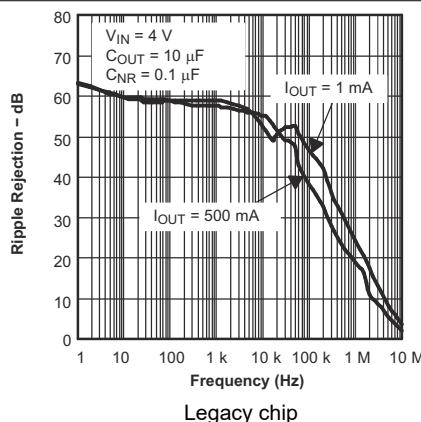


Figure 5-14. TPS795-Q1 Ripple Rejection vs Frequency

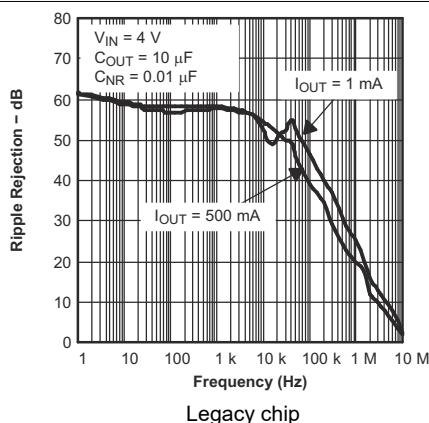


Figure 5-15. TPS795-Q1 Ripple Rejection vs Frequency

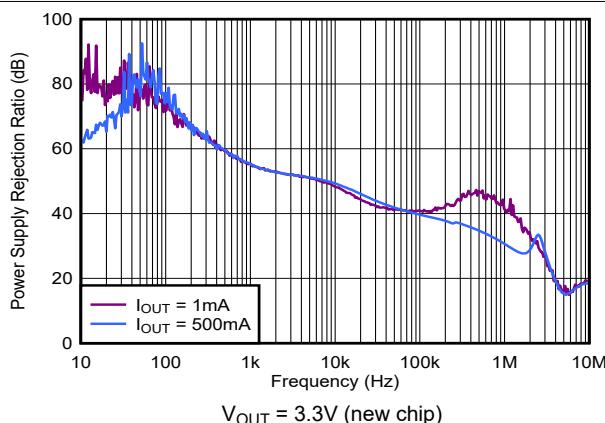


Figure 5-16. TPS795-Q1 Ripple Rejection vs Frequency

5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25^{\circ}C$ (unless otherwise noted)

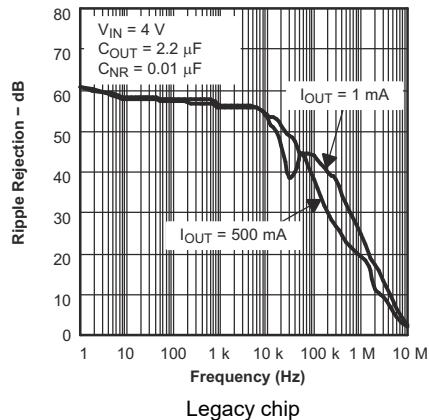


Figure 5-17. TPS795-Q1 Ripple Rejection vs Frequency

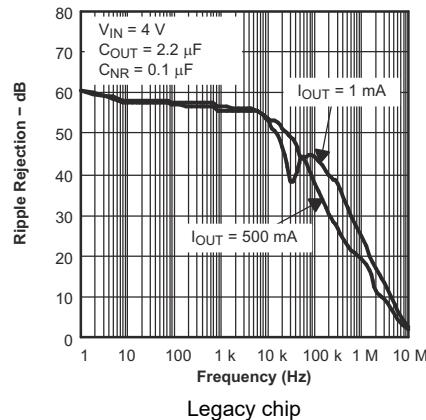


Figure 5-18. TPS795-Q1 Ripple Rejection vs Frequency

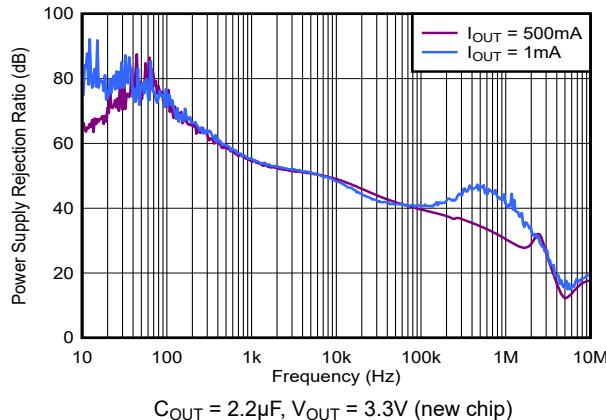


Figure 5-19. TPS795-Q1 Ripple Rejection vs Frequency

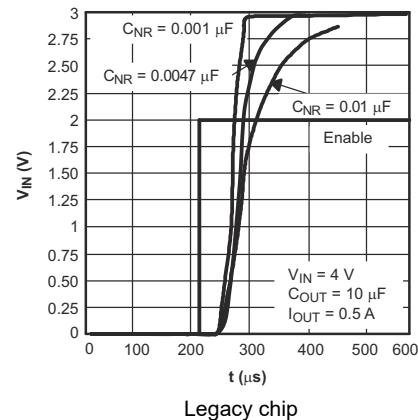


Figure 5-20. TPS795-Q1 Start-Up Time

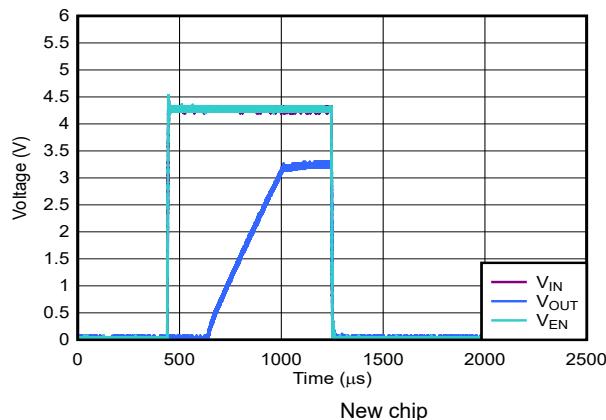


Figure 5-21. TPS795-Q1 Start-Up Time

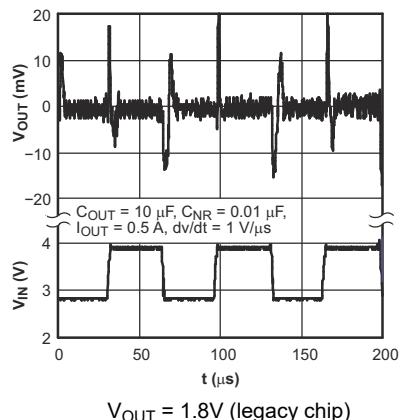


Figure 5-22. TPS795-Q1 Line Transient Response

5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25^{\circ}C$ (unless otherwise noted)

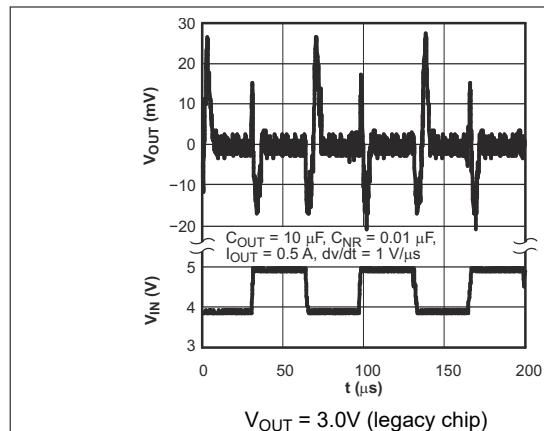


Figure 5-23. TPS795-Q1 Line Transient Response

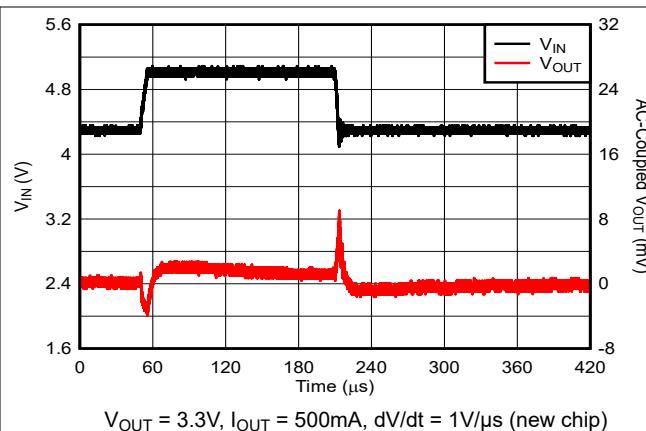


Figure 5-24. TPS795-Q1 Line Transient Response

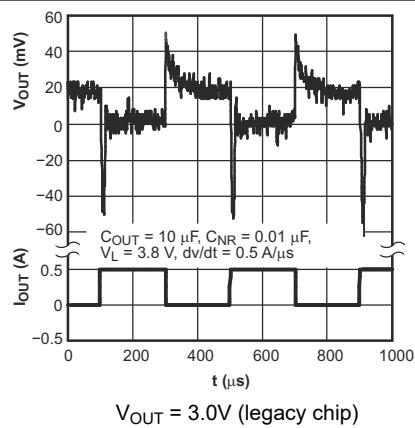


Figure 5-25. TPS795-Q1 Load Transient Response

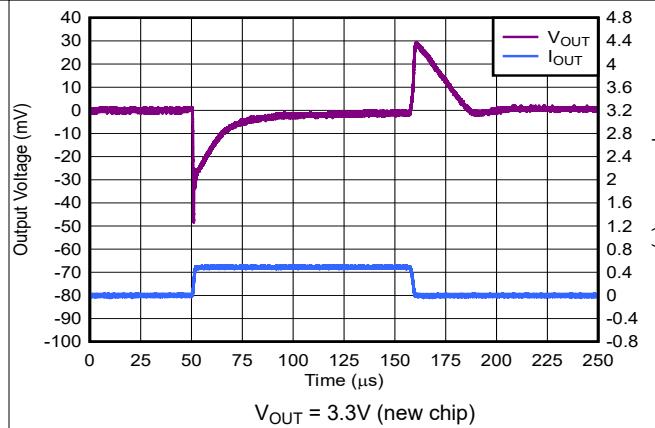


Figure 5-26. TPS795-Q1 Load Transient Response

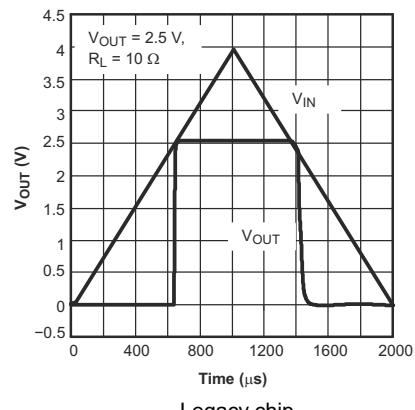


Figure 5-27. TPS795-Q1 Power Up and Power Down

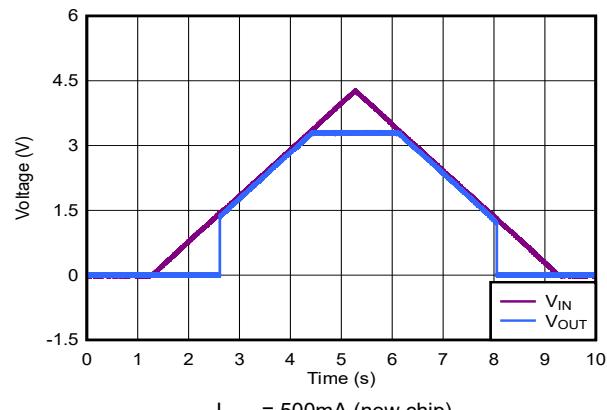


Figure 5-28. TPS795-Q1 Power-Up and Power-Down

5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25^{\circ}C$ (unless otherwise noted)

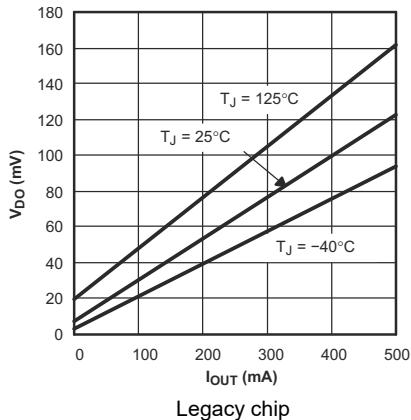


Figure 5-29. TPS795-Q1 Dropout Voltage vs Output Current

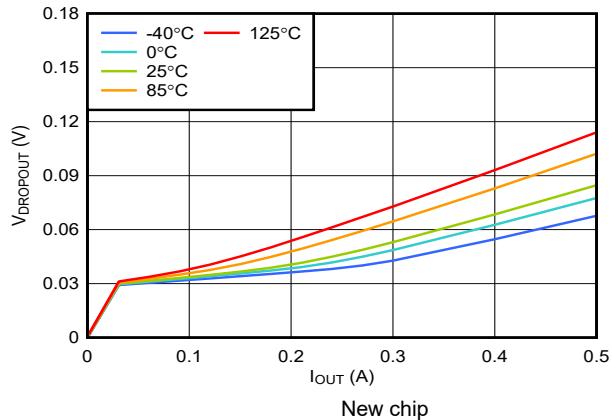


Figure 5-30. TPS795-Q1 Dropout Voltage vs Output Current

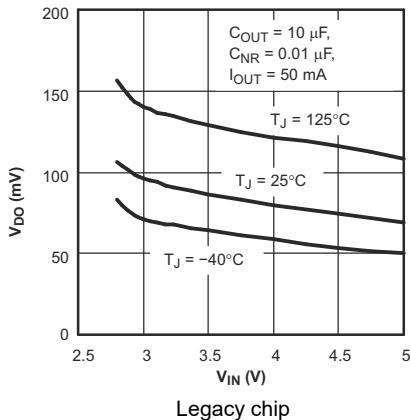


Figure 5-31. TPS795-Q1 Dropout Voltage vs Input Voltage

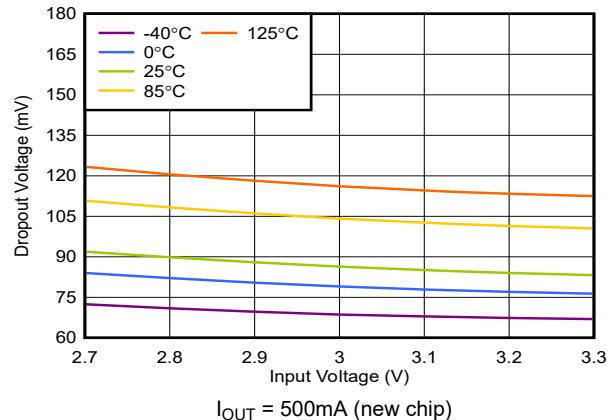


Figure 5-32. TPS795-Q1 Dropout Voltage vs Input Voltage

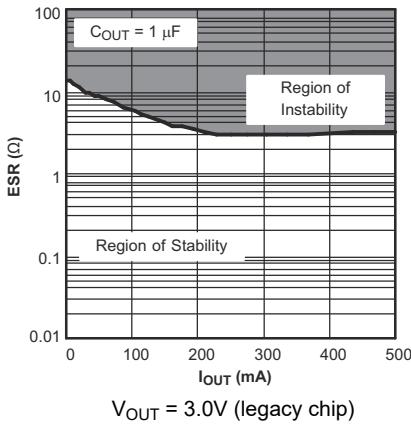


Figure 5-33. TPS795-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

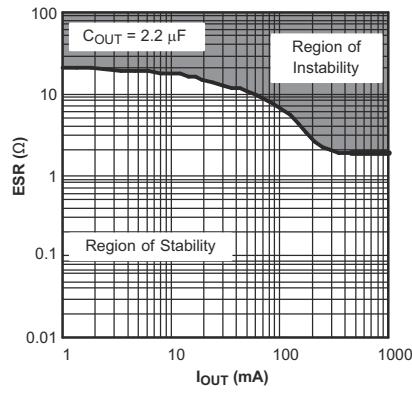


Figure 5-34. TPS795-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25^{\circ}C$ (unless otherwise noted)

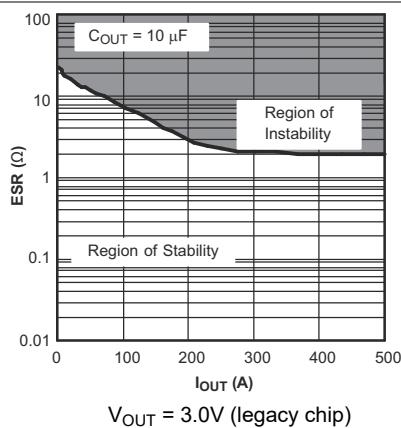


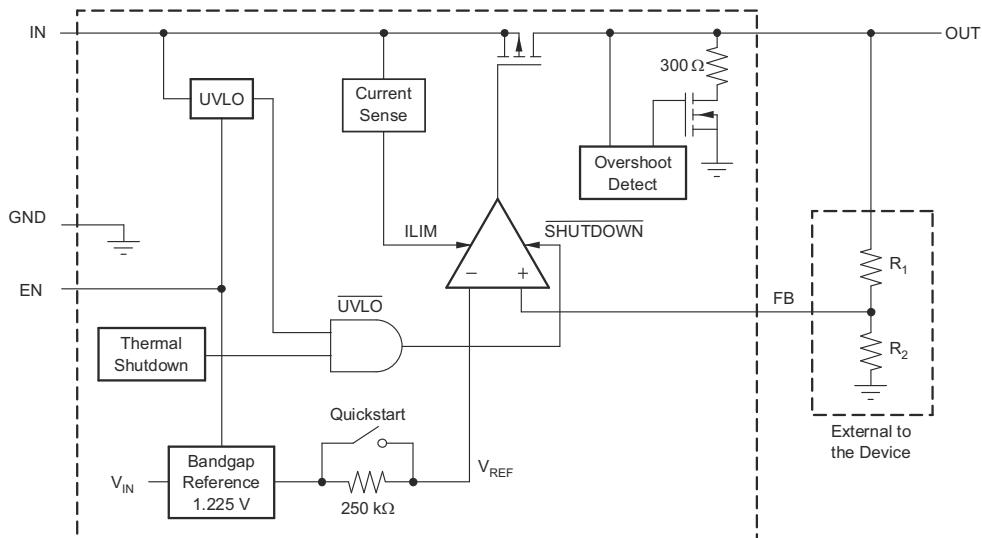
Figure 5-35. TPS795-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

6 Detailed Description

6.1 Overview

The TPS79501-Q1 low-dropout (LDO) regulator has been optimized for use in noise-sensitive equipment. This regulator offers current limit protection, output enable, active discharge, undervoltage lockout (UVLO), and thermal protection.

6.2 Functional Block Diagram



Adjustable version

Figure 6-1. Functional Block Diagram (Legacy Chip)

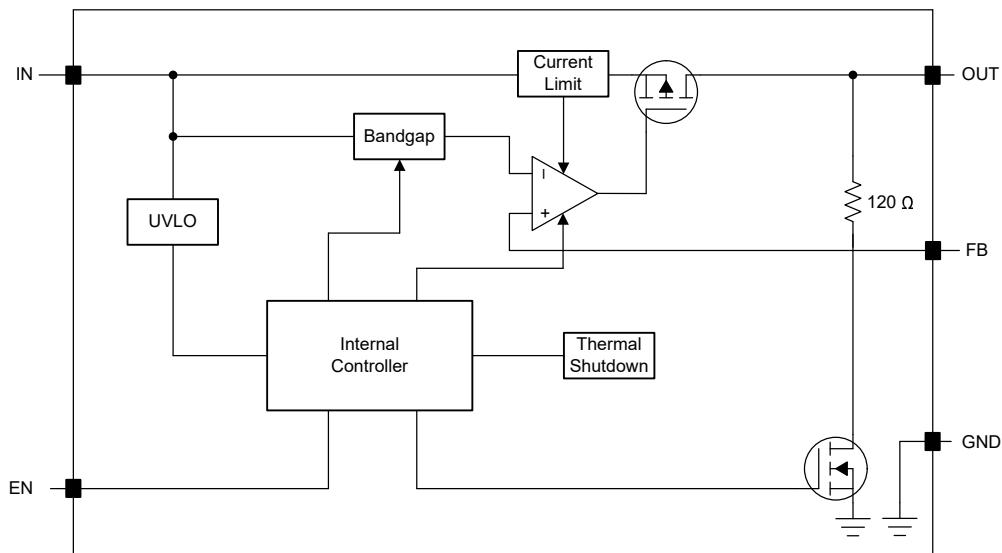


Figure 6-2. Functional Block Diagram (New Chip)

6.3 Feature Description

6.3.1 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

6.3.2 Undervoltage Lockout (UVLO)

The TPS79501-Q1 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has approximately 100mV of hysteresis to help reject input voltage drops when the regulator first turns on.

6.3.3 Regulator Protection

The TPS79501-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting is sometimes appropriate.

During normal operation, the TPS79501-Q1 (legacy chip) limits output current to approximately 2.8A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package.

For the new chip, the device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application note](#).

Figure 6-3 shows a diagram of the foldback current limit.

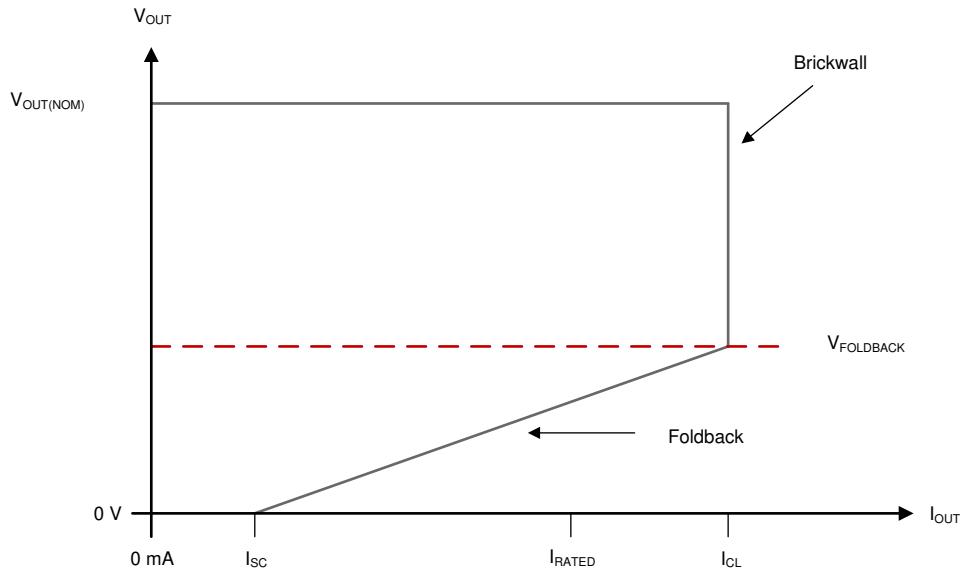


Figure 6-3. Foldback Current Limit

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

[Device Functional Mode Comparison](#) provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{sd}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{sd}$).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS79501-Q1 LDO is optimized for use in noise-sensitive applications. The device features low dropout voltages, high PSRR, low output noise, low quiescent current, and an enable input to reduce supply currents when the regulator is turned off.

7.2 Typical Application

A typical application circuit is shown in [Figure 7-1](#).

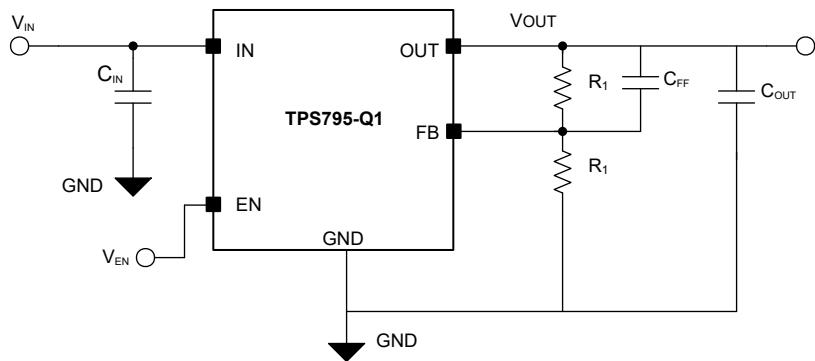


Figure 7-1. Typical Application Circuit

Note

Feed-forward capacitor (C_{FF}) is optional

7.2.1 Design Requirements

[Design Parameters](#) lists the design requirements.

Table 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3V
Output voltage	2.5V
Maximum output current	500mA

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although the legacy chip of TPS79501-Q1 does not require an input capacitor, good analog design practise is to place a $0.1\mu\text{F}$ to $2.2\mu\text{F}$ capacitor near the input of the regulator to counteract reactive input sources. A higher-value input capacitor can be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS79501-Q1 device requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is $1\mu\text{F}$. Any $1\mu\text{F}$ or larger ceramic capacitor is suitable.

7.2.2.2 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in [Load Transient Waveform](#) are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

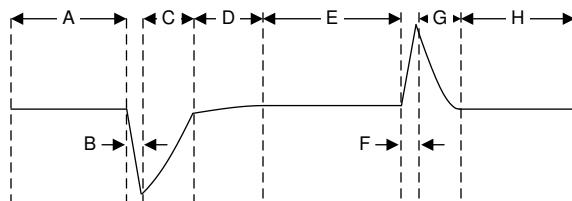


Figure 7-2. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)
- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.2.2.3 Programming the TPS79501-Q1 Adjustable LDO Regulator

The output voltage of the TPS79501-Q1 adjustable regulator is programmed using an external resistor divider. The output voltage is calculated using [Equation 1](#):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2} \right) \quad (1)$$

where

- $V_{REF} = 1.2246V$ typ (the internal reference voltage)

Resistors R_1 and R_2 must be selected for approximately $40\mu A$ divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values must be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to select the following values using [Equation 2](#):

$R_2 = 30.1\text{k}\Omega$ to set the divider current at $40\mu A$

$C_1 = 15\text{pF}$ for stability, and then calculate R_1

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_2 \quad (2)$$

To improve the stability of the adjustable version, place a small compensation capacitor between OUT and FB.

The approximate value of this capacitor can be calculated as [Equation 3](#):

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 μ F instead of 1 μ F.

7.2.3 Application Curves

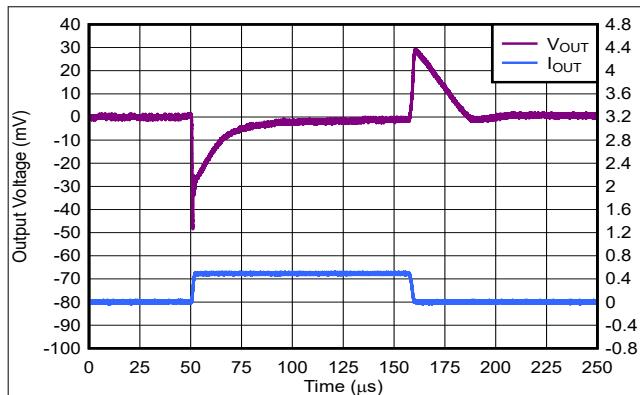


Figure 7-3. TPS795 Load Transient

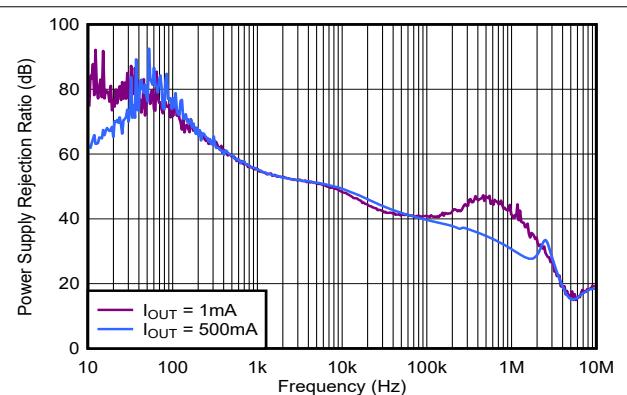


Figure 7-4. TPS795 Ripple Rejection vs Frequency

7.3 Power Supply Recommendations

The TPS79501-Q1 is designed to operate from an input voltage supply range from 2.7V to 5.5V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, design with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the ground pin of the device.

7.4.1.2 Thermal Information

7.4.1.2.1 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and providing reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using [Equation 4](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VSON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, the pad must be attached

to an appropriate amount of copper PCB area to verify that the device does not overheat. The tab must be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using [Equation 5](#):

$$R_{\theta JA} = \frac{(+125^\circ\text{C} - T_A)}{P_D} \quad (5)$$

Note

When the device is mounted on an application PCB, use Ψ_{JT} and Ψ_{JB} , as explained in the [Section 7.4.1.2.2](#) section.

7.4.1.2.2 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB} , as shown in the [Thermal Information](#) table, the junction temperature can be estimated with corresponding formulas (given in [Equation 6](#)). For backwards compatibility, an older $\theta_{JC, Top}$ parameter is also listed.

$$\begin{aligned} \Psi_{JT}: \quad T_J &= T_T + \Psi_{JT} \cdot P_D \\ \Psi_{JB}: \quad T_J &= T_B + \Psi_{JB} \cdot P_D \end{aligned} \quad (6)$$

Where P_D is the power dissipation shown by [Equation 5](#), T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as [Figure 7-6](#) shows).

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B , see the application note [SBVA025, Using New Thermal Metrics](#), available for download at www.ti.com.

By looking at [Figure 7-5](#), the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with [Equation 6](#) is a good way to estimate T_J by simply measuring T_T or T_B , regardless of the application board size.

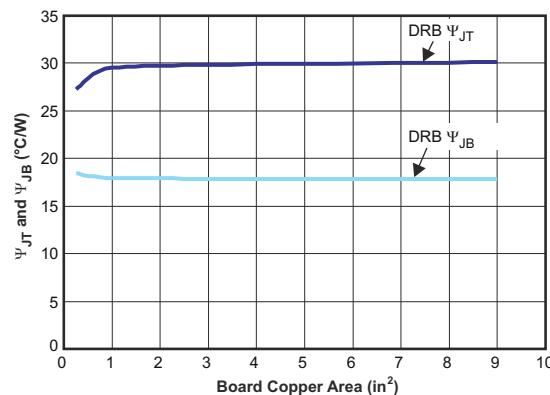


Figure 7-5. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(\text{top})}$ to determine thermal characteristics, see the [Using New Thermal Metrics](#) application note, available for download at www.ti.com.

For further information, see the [Semiconductor and IC Package Thermal Metrics](#) application note , also available on the TI website.

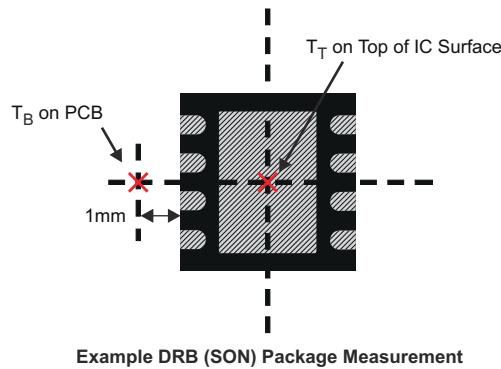


Figure 7-6. Measuring Point for T_T and T_B

7.4.2 Layout Example

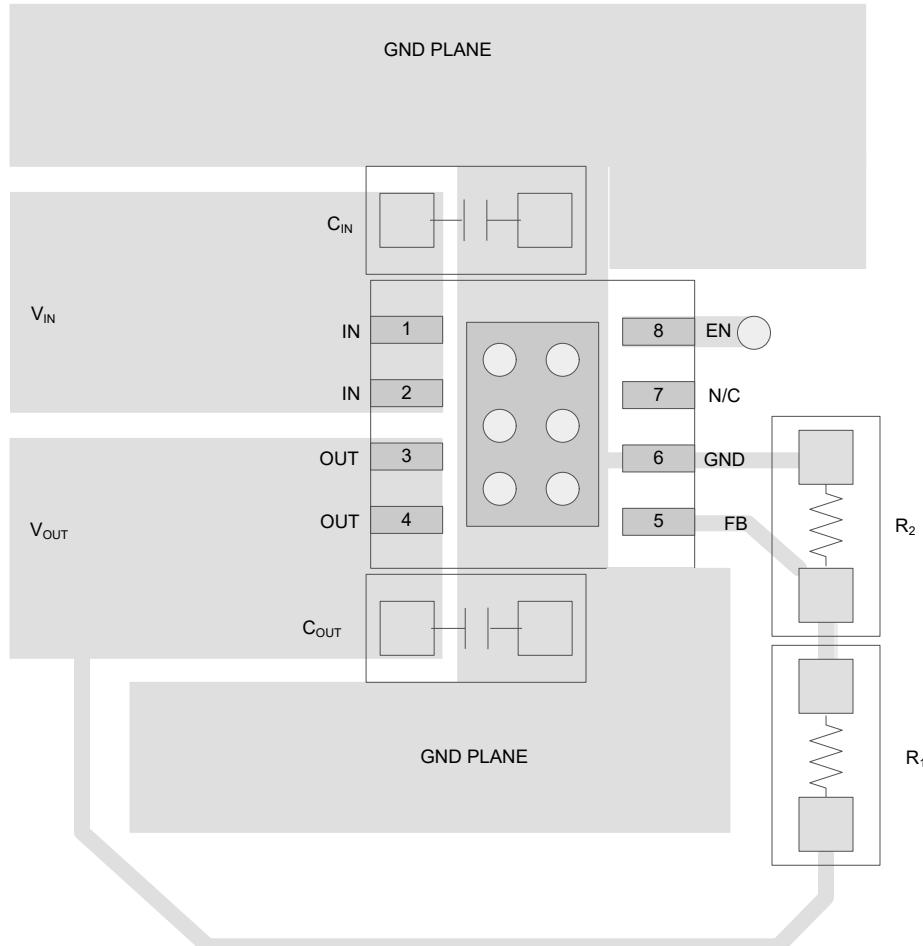


Figure 7-7. TPS79501-Q1 DRB Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For the TI PCB Thermal Calculator, go to <http://www.ti.com/pcbthermalcalc>.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *Using New Thermal Metrics*, [SBVA025](#)
- *Solder Pad Recommendations for Surface-Mount Devices*, [SBFA015](#)

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2010) to Revision A (February 2026)	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 PACKAGE OPTION ADDENDUM

PACKAGE INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
TPS79501GQDRBRQ1	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-1 68 HR	-40 to 125	QVE

- (1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OSOLETE: TI has discontinued the production of the device.

- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

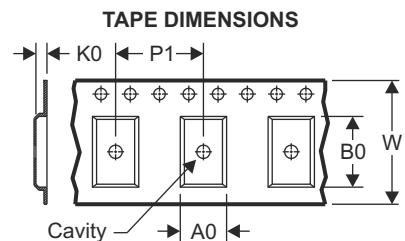
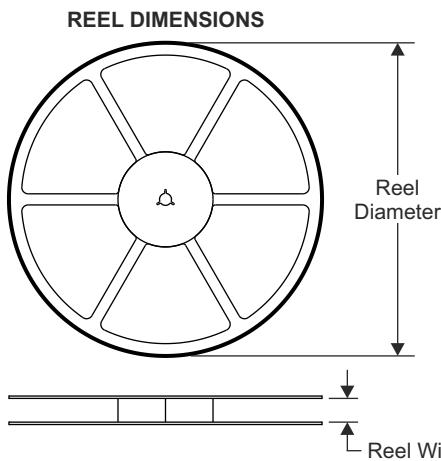
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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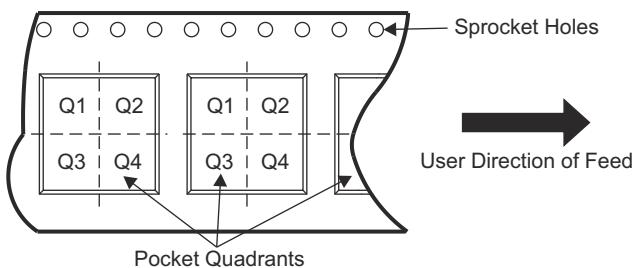
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

10.2 Tape and Reel Information



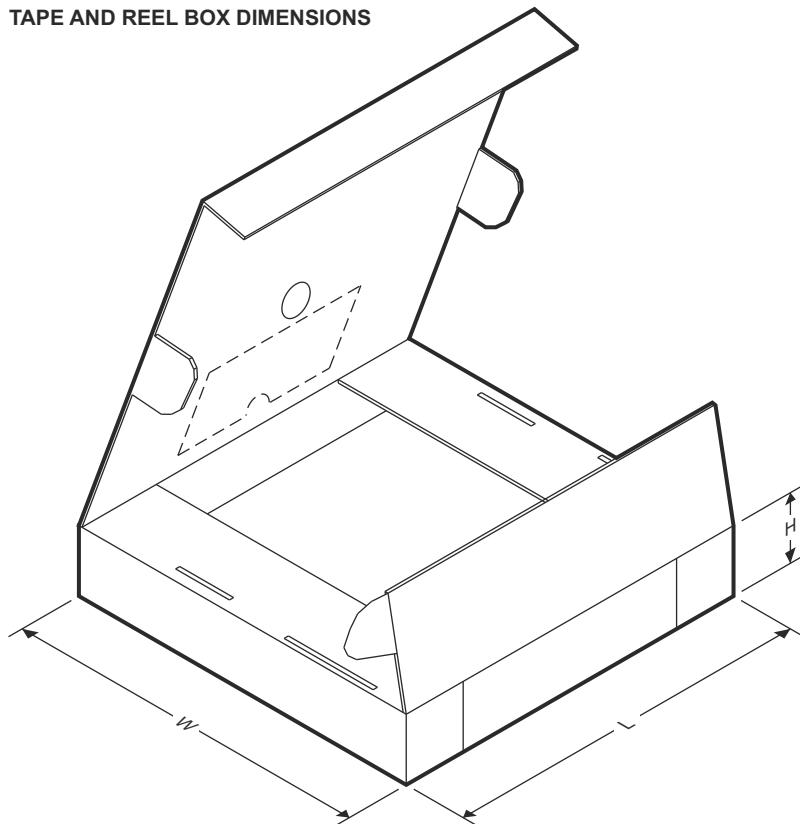
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79501GQDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79501GQDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79501QDRBRM3Q1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVE
TPS79501QDRBRQ1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	QVE
TPS79501QDRBRQ1.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	QVE

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

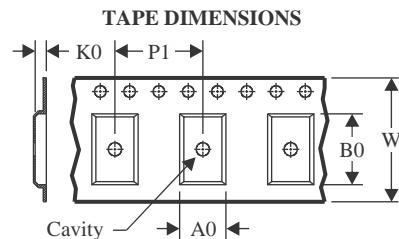
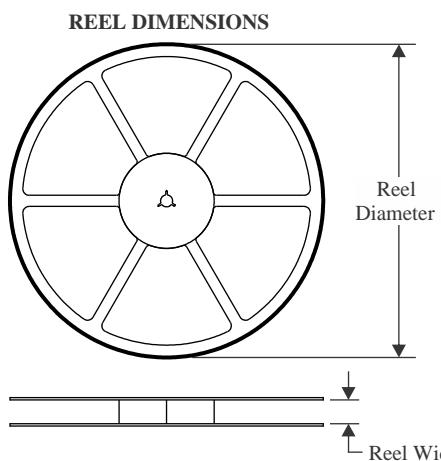
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

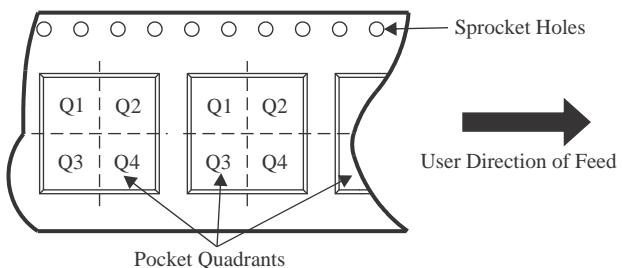
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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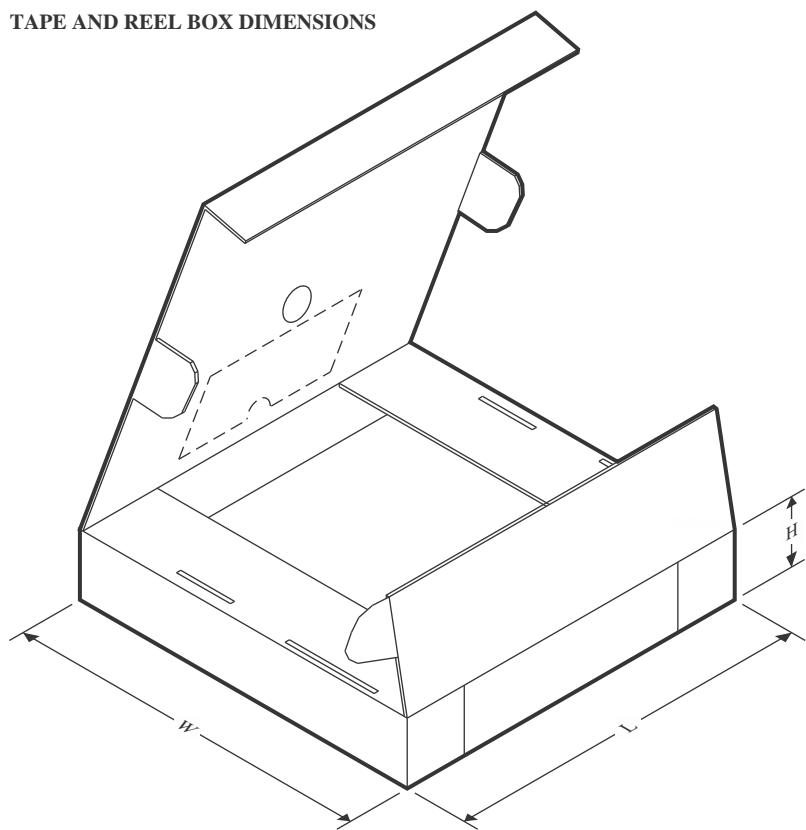
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79501QDRBRM3Q1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79501QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79501QDRBRM3Q1	SON	DRB	8	3000	367.0	367.0	35.0
TPS79501QDRBRQ1	SON	DRB	8	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

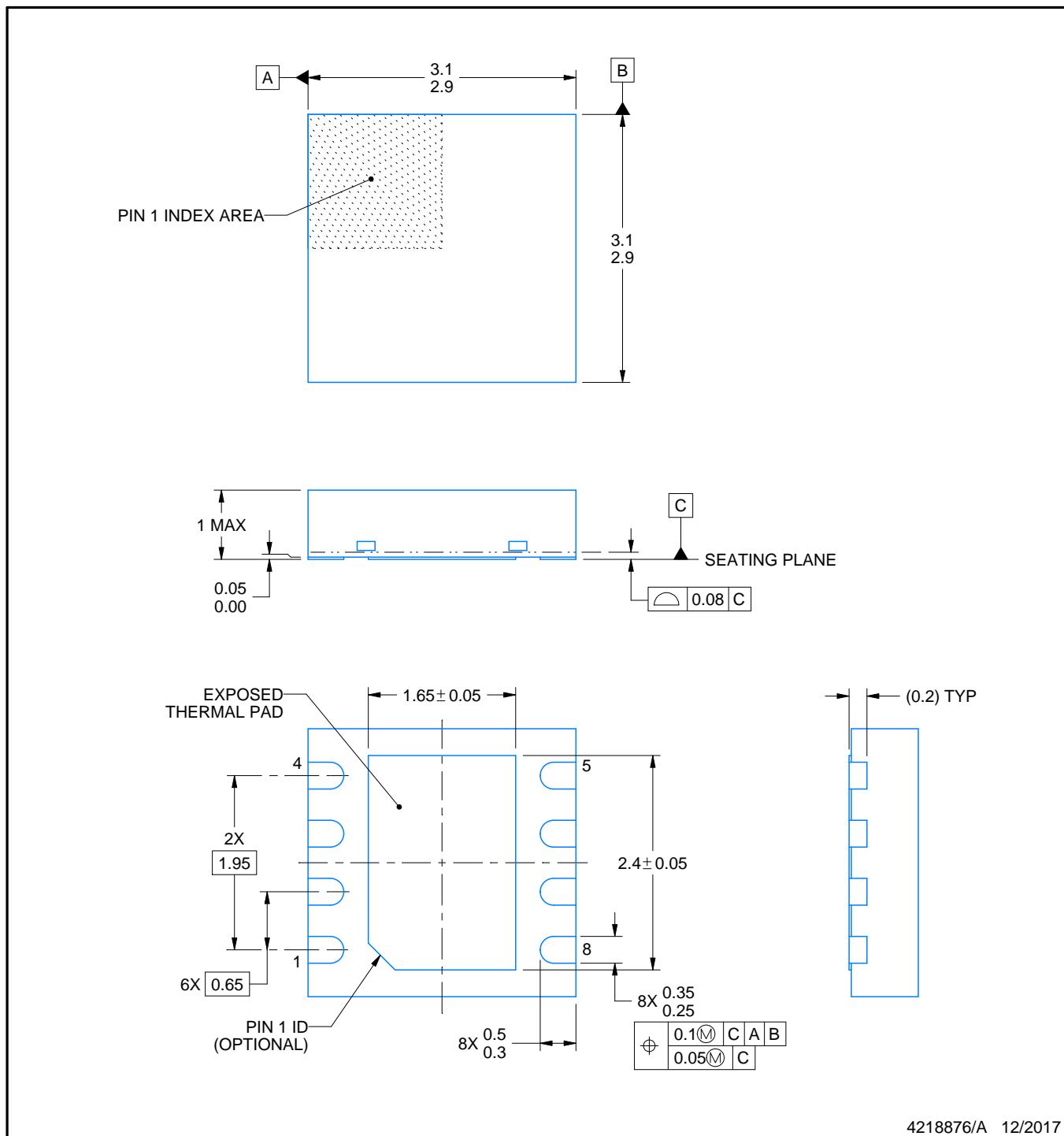


PACKAGE OUTLINE

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

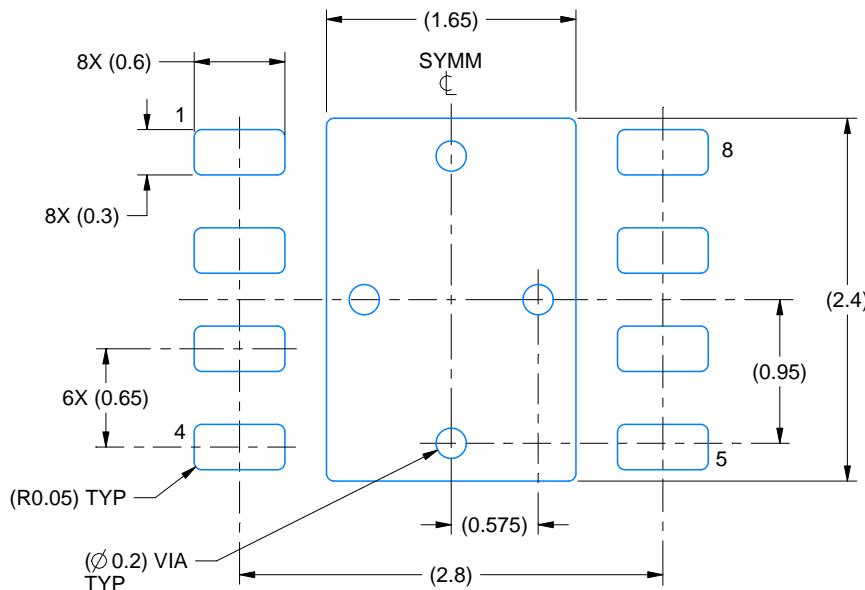
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DRB0008B

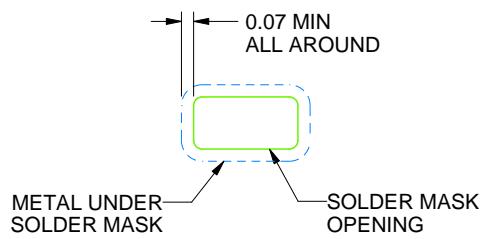
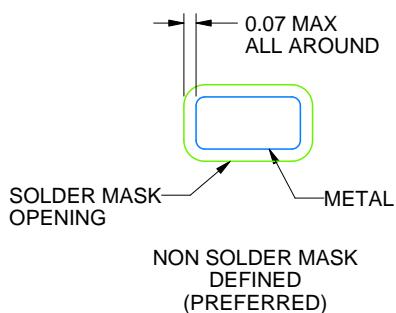
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE

SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

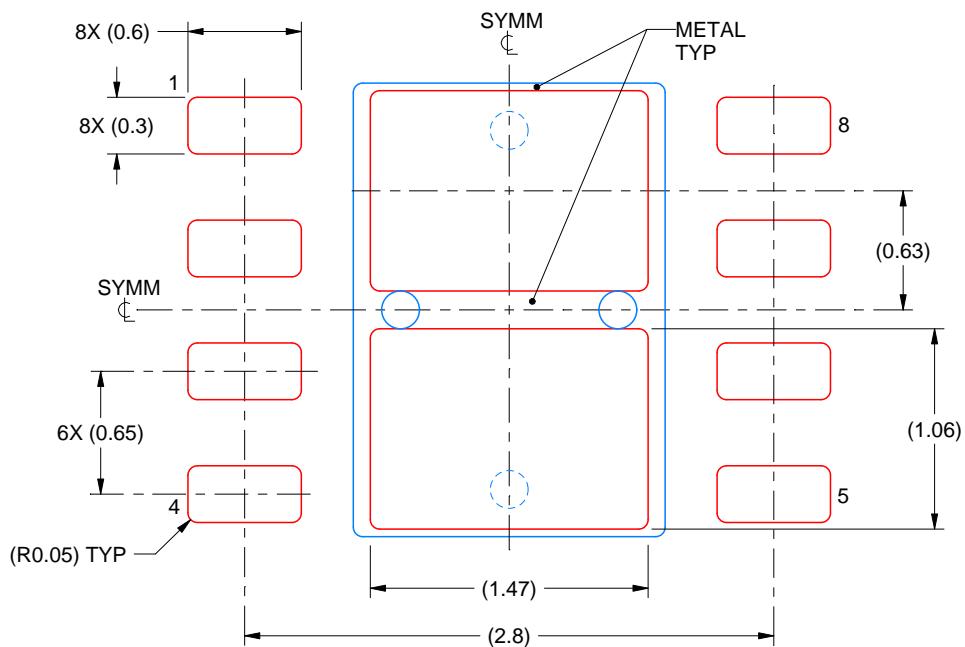
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025