TPS77401-EP
250-mA LDO VOLTAGE REGULATOR WITH POWER-GOOD OUTPUT

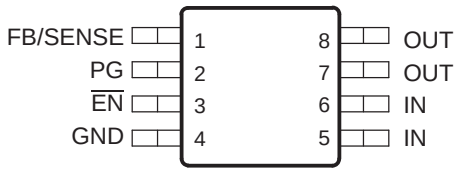
SLVS702 – OCTOBER 2006

FEATURES

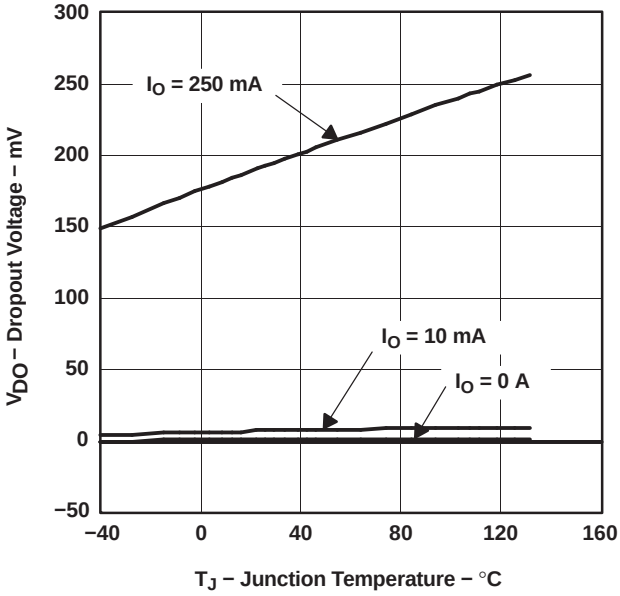
- **Controlled Baseline**
  - **One Assembly**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Open-Drain Power-Good (PG) Status Output**
- **Available in 1.5-V, 1.8-V, 2.7-V, 2.8-V, 3.3-V, 5-V Fixed-Output and Adjustable Versions**
- **Dropout Voltage Typically 200 mV at 250 mA**
- **Ultralow 92-μA Quiescent Current (Typ)**
- **8-Pin MSOP (DGK) Package**
- **Low Noise (55 μV_{rms}) Without an External Filter (Bypass) Capacitor**
- **2% Tolerance Over Specified Conditions For Fixed-Output Versions**
- **Fast Transient Response**
- **Thermal Shutdown Protection**
- **See the TPS779xx Family of Devices for Active-High Enable**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DGK PACKAGE
(TOP VIEW)



DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE



DESCRIPTION

The TPS77401 is a low-dropout (LDO) regulator with power good (PG) function. This device is capable of supplying 250 mA of output current with a dropout of 200 mV. Quiescent current is 92 μA at full load dropping down to 1 μA when device is disabled. This device is optimized to be stable with a wide range of output capacitors including low-ESR ceramic (10-μF) or low-capacitance (1 μF) tantalum capacitors. This device has extremely low noise output performance (55 μV_{rms}) without using any added filter capacitors. The TPS77401 is designed to have fast transient response for larger load current changes.

The TPS77401 is offered in 1.5-V, 1.8-V, 2.7-V, 2.8-V, 3.3-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is 2% over line, load, and temperature ranges. The TPS77401 device is available in an 8-pin mini small-outline package (MSOP) (DGK).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DESCRIPTION (CONTINUED)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 200 mV at an output current of 250 mA for 3.3-V option) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 92 μA over the full range of output current, 0 mA to 250 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when the enable ($\overline{EN}$) pin is connected to a low-level input voltage. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ shuts down the regulator, reducing the quiescent current to less than 1 μA at T_J = 25°C.

For the TPS77401, the power good (PG) terminal is an active-high output, which can be used to implement a power-on reset or a low-battery indicator. An internal comparator in the TPS77401 monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT falls below 82% of its regulated voltage, PG goes to a low-impedance state. PG goes to a high-impedance state when OUT is above 82% of its regulated voltage.

AVAILABLE OPTIONS(1)

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICE MSOP (DGK)	
	TYP	ORDERABLE PART NUMBER	SYMBOL
–55°C to 125°C	Adjustable 1.5 V to 5.5 V	TPS77401MDGKREP	BYQ

(1) The TPS77401 is programmable using an external resistor divider (see application information). The DGK package is available taped and reeled.

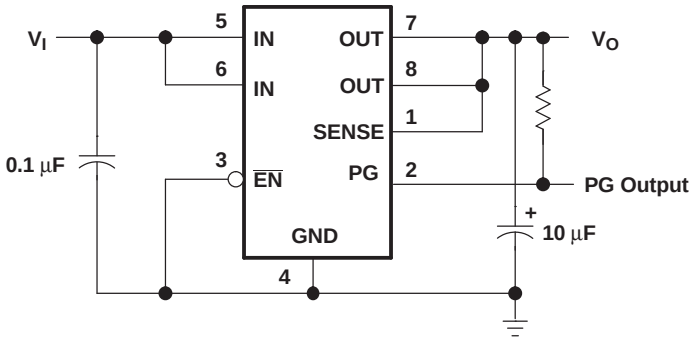
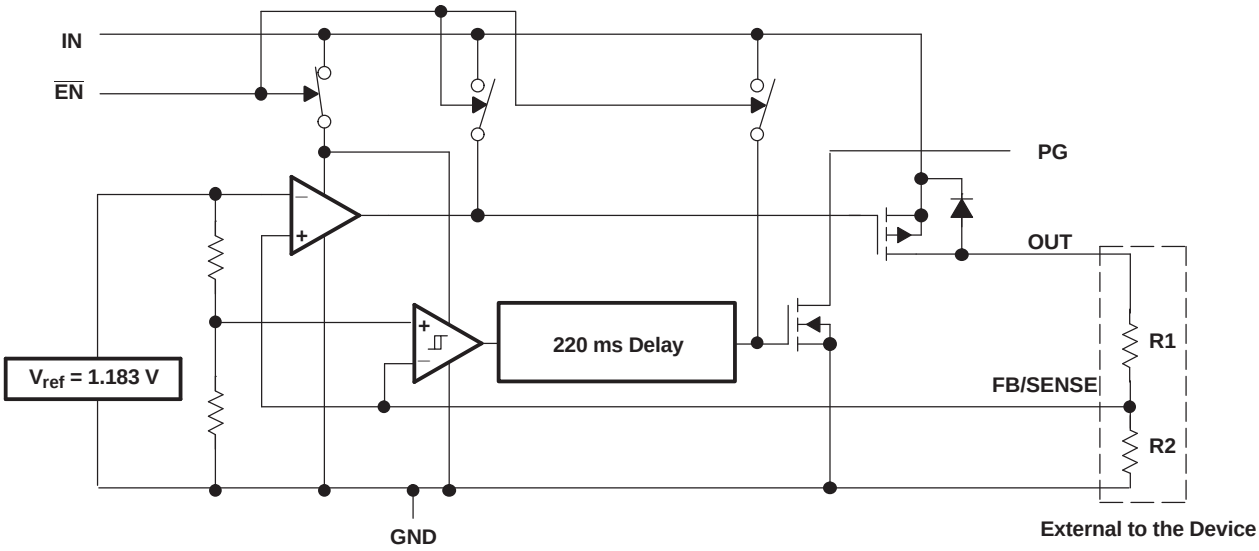


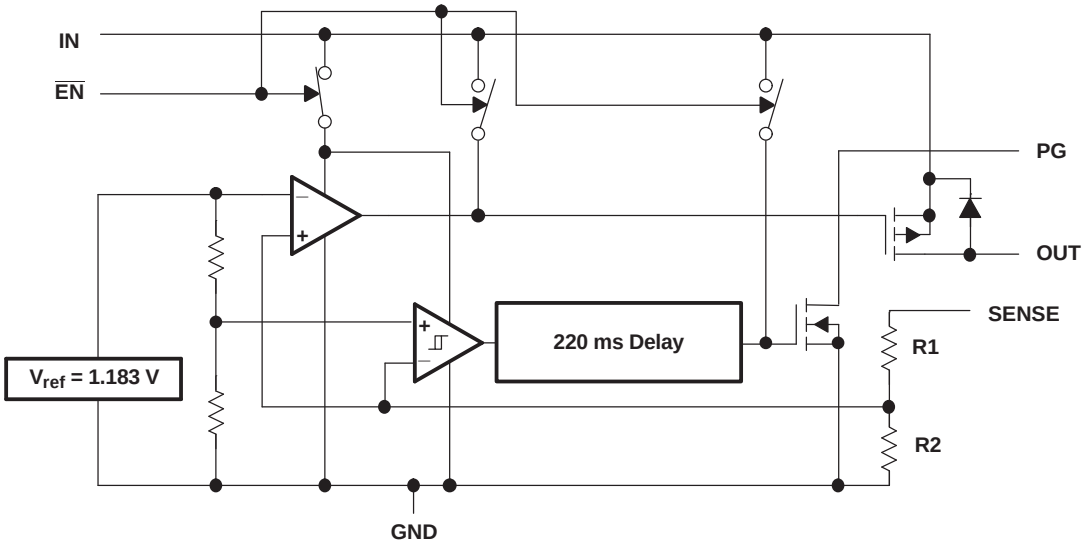
Figure 1. Typical Application Configuration (for Fixed-Output Options)

FUNCTIONAL BLOCK DIAGRAMS

ADJUSTABLE VERSION



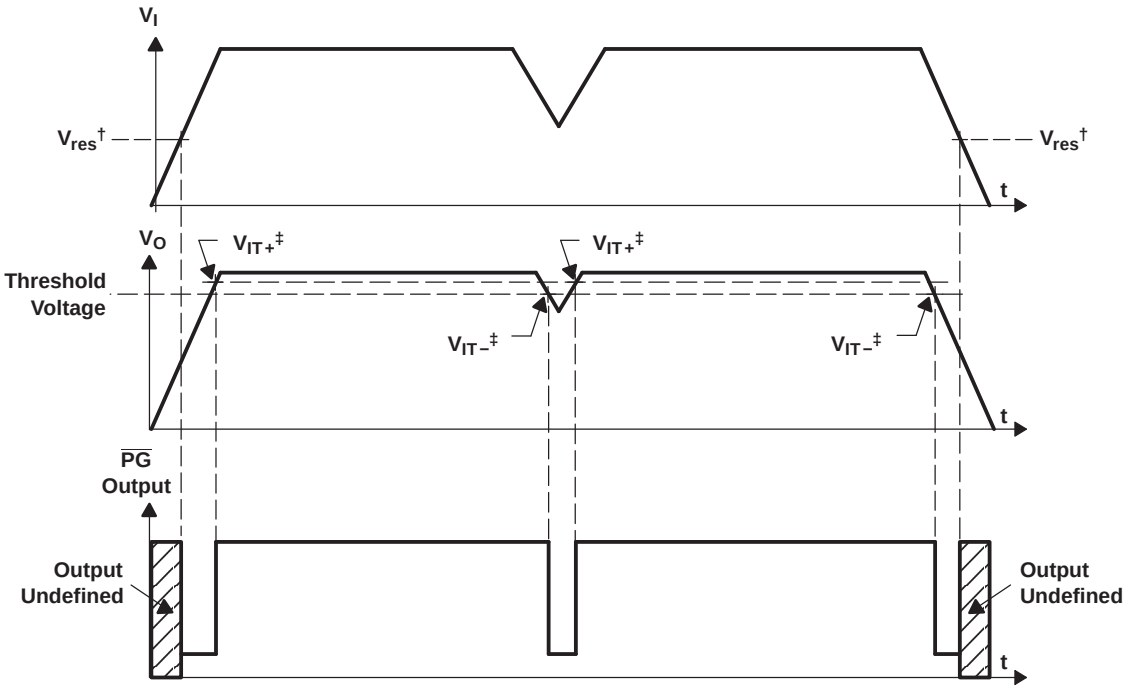
FIXED-VOLTAGE VERSION



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
FB/SENSE	1	I	Feedback input voltage for adjustable device (sense input for fixed options)
PG	2	O	Power good
$\overline{EN}$	3	I	Enable
GND	4		Regulator ground
IN	5, 6	I	Input voltage
OUT	7, 8	O	Regulated output voltage

PG TIMING DIAGRAM



† V_{res} is the minimum input voltage for a valid PG. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ V_{IT} − Trip voltage is typically 18% lower than the output voltage (82%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage range(2)	–0.3	13.5	V
	Voltage range at $\overline{EN}$	–0.3	16.5	V
	Maximum PG voltage		16.5	V
	Peak output current		Internally limited	
	Continuous total power dissipation		See Dissipation Rating Table	
V_O	Output voltage (OUT, FB)		5.5	V
T_j	Operating virtual junction temperature range(3)	–55	125	°C
T_{stg}	Storage temperature range	–65	150	°C
	ESD rating, Human-Body Model (HBM)		2	kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.
(3) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional infomation on enhanced plastic packaging

Dissipation Ratings – Free-Air Temperatures

PACKAGE	AIR FLOW (CFM)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGK	0	266.2	3.84	376 mW	3.76 mW/°C	207 mW	150 mW
	150	255.2	3.92	392 mW	3.92 mW/°C	216 mW	157 mW
	250	242.8	4.21	412 mW	4.12 mW/°C	227 mW	165 mW

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage(1)	2.7	10	V
V_O	Output voltage range	1.5	5.5	V
I_O	Output current(2)	0	250	mA
T_J	Operating virtual junction temperature(2)	–55	125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
(2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

Electrical Characteristics

over recommended operating junction temperature range (T_J = –55°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 10 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage[1][2]	Adjustable voltage	1.5 V ≤ V_O ≤ 5.5 V	T_J = 125°C	0.98V_O		1.02V_O	V
			T_J = Full range	0.977V_O		1.023V_O	
	1.5-V output	T_J = 25°C,	2.7 V < V_{IN} < 10 V		1.5		V
		2.7 V < V_{IN} < 10 V		1.470		1.530	
	1.8-V output	T_J = 25°C,	2.8 V < V_{IN} < 10 V		1.8		V
		2.8 V < V_{IN} < 10 V		1.764		1.836	
	2.7-V output	T_J = 25°C,	3.7 V < V_{IN} < 10 V		2.7		
		3.7 V < V_{IN} < 10 V		2.646		2.754	
	2.8-V output	T_J = 25°C,	3.8 V < V_{IN} < 10 V		2.8		
		3.8 V < V_{IN} < 10 V		2.744		2.856	
	3.3-V output	T_J = 25°C,	4.3 V < V_{IN} < 10 V		3.3		
		4.3 V < V_{IN} < 10 V		3.234		3.366	
	5-V output	T_J = 25°C,	6 V < V_{IN} < 10 V		5.0		V
		6.0 V < V_{IN} < 10 V		4.9		5.1	
Quiescent current (GND current)[1][2]		T_J = 25°C			92		µA
		T_J = Full range				135	
Output voltage line regulation ($\Delta V_O/V_O$)[3]		V_O + 1 V < V_I ≤ 10 V,	T_J = 25°C		0.005		%/V
		V_O + 1 V < V_I ≤ 10 V				0.05	%/V
Load regulation		T_J = 25°C			1		mV
Output noise voltage		BW = 300 Hz to 100 kHz,	T_J = 25°C		55		µVrms
Output current limit		V_O = 0 V			0.9	1.3	A
Peak output current		2 ms pulse width,	50% duty cycle		400		mA
Thermal shutdown junction temperature					144		°C
Standby current		$\overline{EN}$ = V_I	T_J = 25°C			1	µA
			T_J = Full range			3	
FB input current	Adjustable voltage	FB = 1.5 V				1	µA
High-level enable input voltage				2			V
Low-level enable input voltage						0.7	V
Enable input current				–1		1	µA
PSRR Power-supply rejection ratio		f = 1 kHz,	T_J = 25°C		55		dB
PG	Minimum input voltage for valid PG	$I_{(PG)}$ = 300 µA,	$V_{(PG)}$ ≤ 0.8 V		1.1		V
	Trip threshold voltage	V_O decreasing		79		85	%V_O
	Hysteresis voltage	Measured at V_O			0.5		
	Output low voltage	V_I = 2.7 V,	$I_{(PG)}$ = 1 mA		0.15	0.4	V
	Leakage current	$V_{(PG)}$ = 5 V				1	µA

(1) Minimum input operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum input voltage = 10 V, minimum output current 1 mA.
(2) I_O = 1 mA to 250 mA
(3) If V_O < 1.8 V, then $V_{I(max)}$ = 10 V, $V_{I(min)}$ = 2.7 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{I(max)} - 2.7\ V\right)}{100} \times 1000$$

If V_O > 2.5 V, then $V_{I(max)}$ = 10 V, $V_{I(min)} = V_O$ + 1 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{I(max)} - \left(V_O + 1\right)\right)}{100} \times 1000$$

Electrical Characteristics (continued)

over recommended operating junction temperature range (T_J = –55°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 10 μF (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage(4)	2.8-V output	I_O = 250 mA,	T_J = 25°C		270		mV
			I_O = 250 mA				475	
		3.3-V output	I_O = 250 mA	T_J = 25°C		200		
				T_J = Full Range			350	
		5-V output	I_O = 250 mA,	T_J = 25°C		125		
			I_O = 250 mA				190	

(4) IN voltage equals $V_{O(typ)}$ – 100 mV; 1.5-V, 1.8-V, and 2.7-V dropout voltage limited by input voltage range limitations (i.e., 3.3-V input voltage needs to drop to 3.2-V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage	vs Output current	2, 3
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Output impedance	vs Frequency	9
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	vs Junction temperature	11
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Output voltage and enable pulse	vs Time	16
Equivalent series resistance	vs Output current	18–21

TPS77x33

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

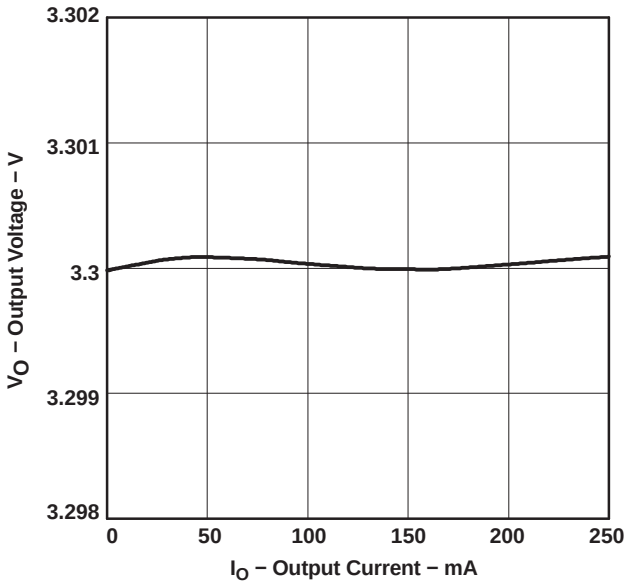


Figure 2.

TPS77x18

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

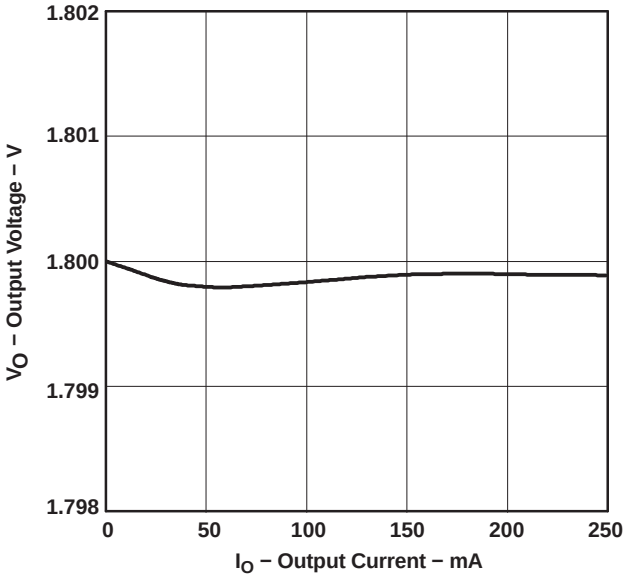


Figure 3.

TPS77x33
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

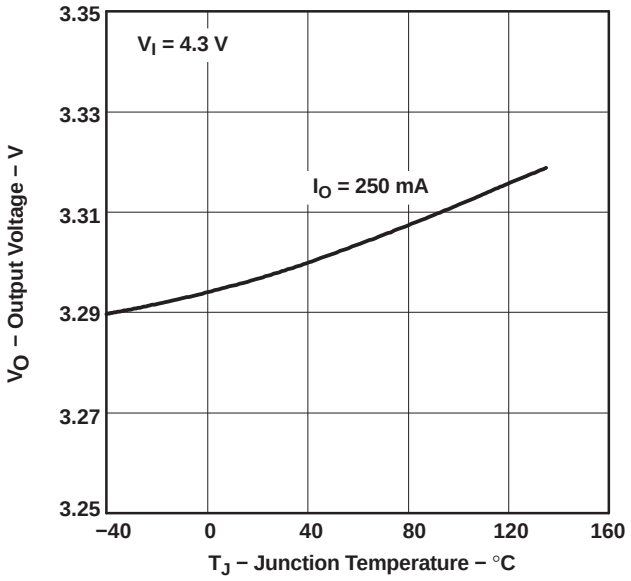


Figure 4.

TPS77x18
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

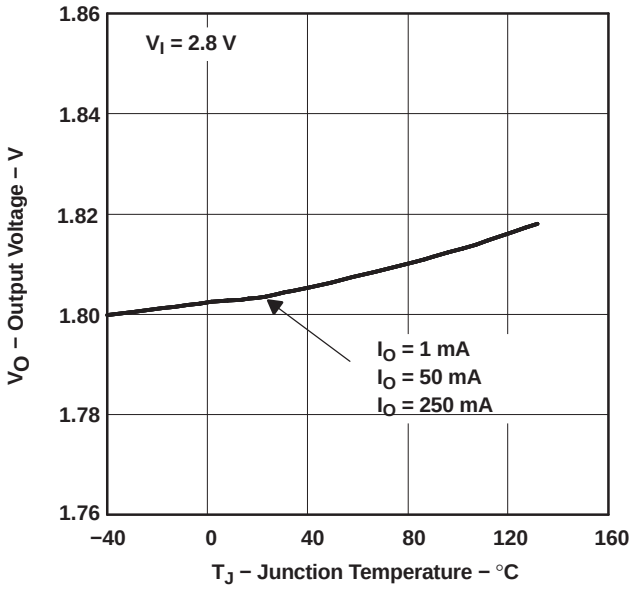


Figure 5.

TPS77xxx
GROUND CURRENT
vs
JUNCTION TEMPERATURE

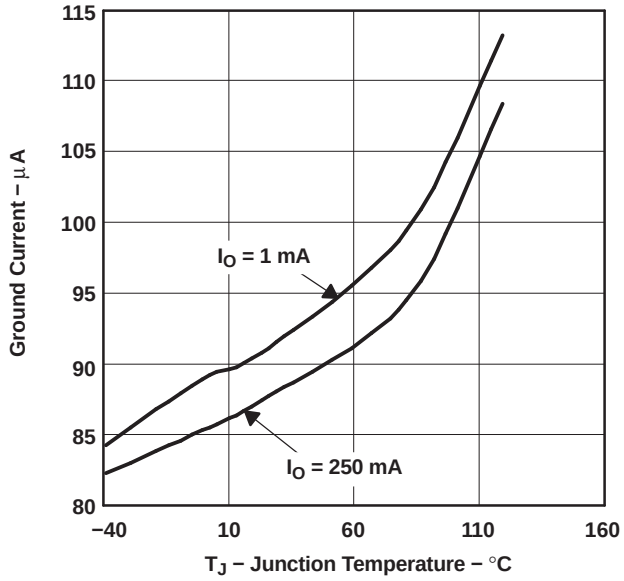


Figure 6.

TPS77x33
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

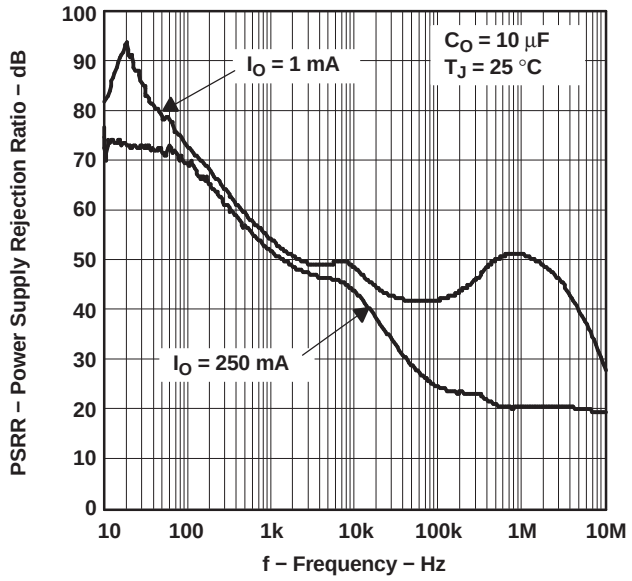


Figure 7.

TPS77x33
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

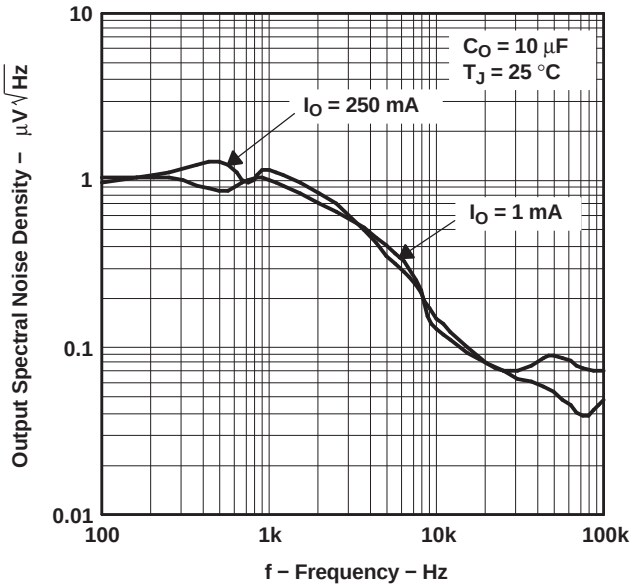


Figure 8.

TPS77x33
OUTPUT IMPEDANCE
vs
FREQUENCY

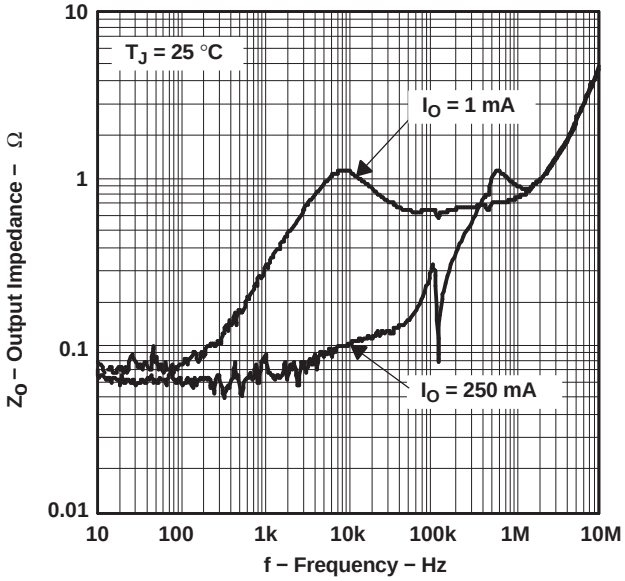


Figure 9.

TPS77x01
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

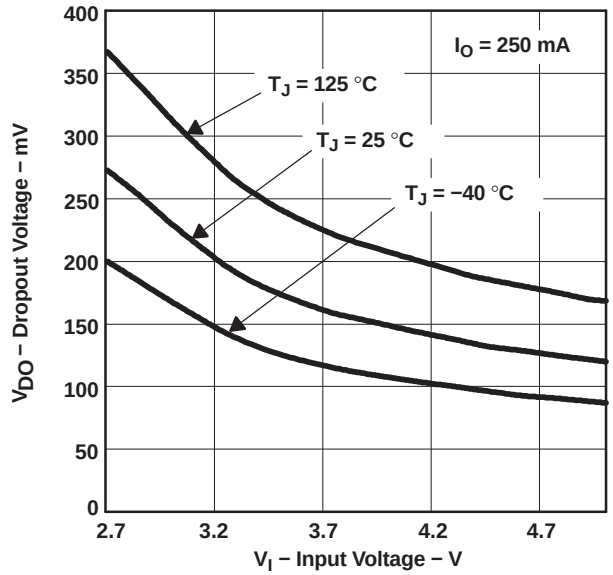


Figure 10.

TPS77x33
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

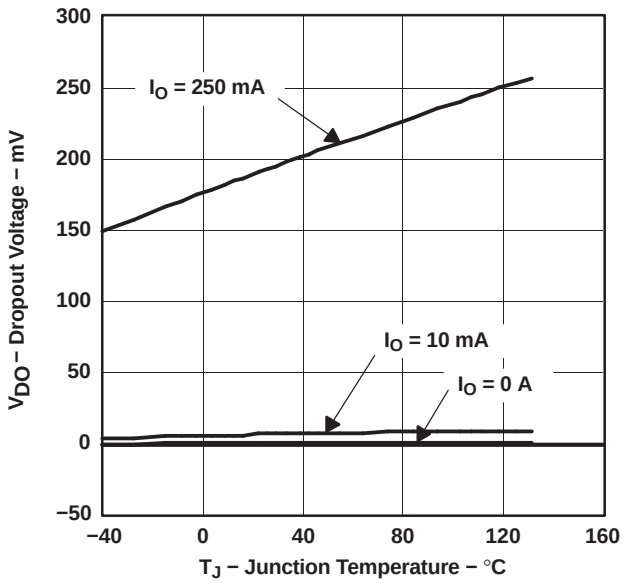


Figure 11.

TPS77x18
LINE TRANSIENT RESPONSE

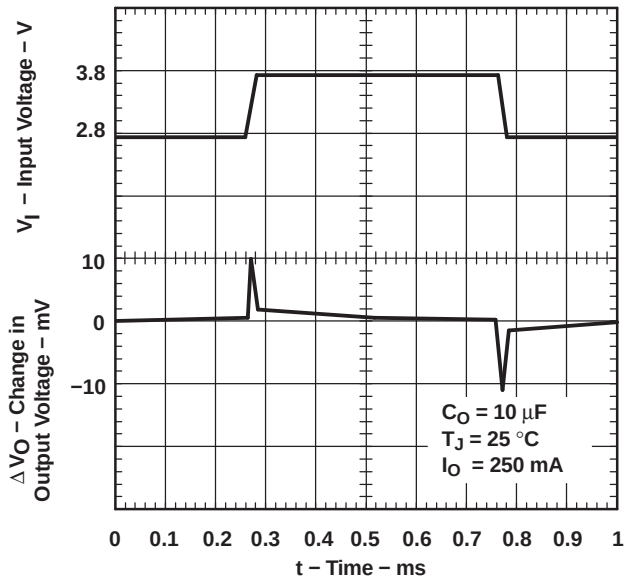


Figure 12.

TPS77x18
LOAD TRANSIENT RESPONSE

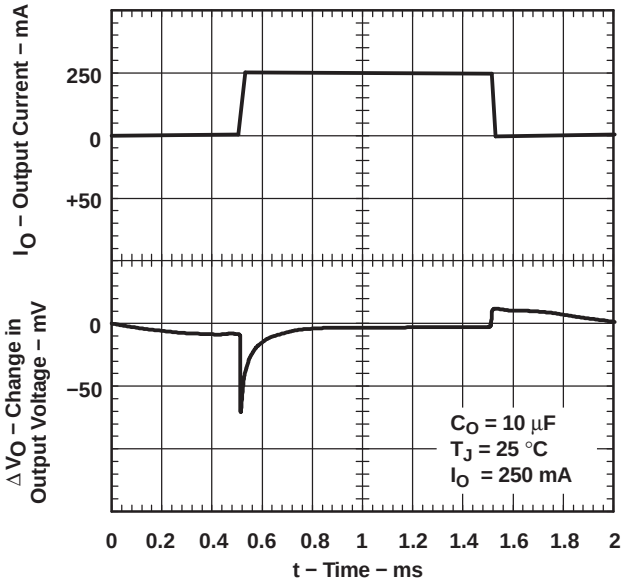


Figure 13.

TPS77x33
LINE TRANSIENT RESPONSE

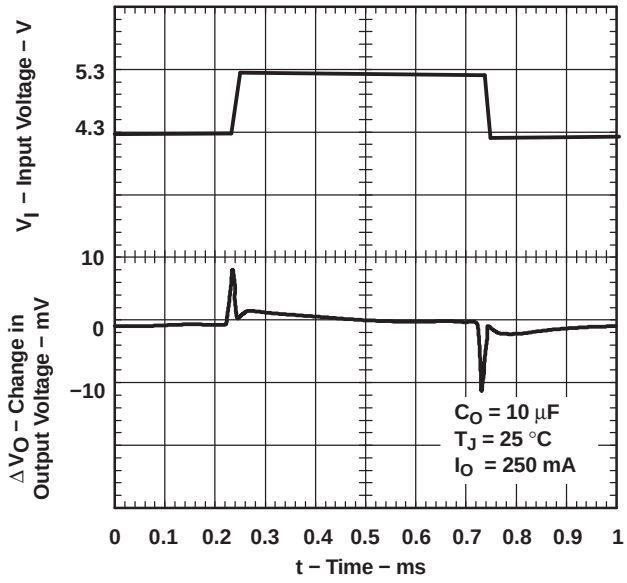


Figure 14.

TPS77x33
LOAD TRANSIENT RESPONSE

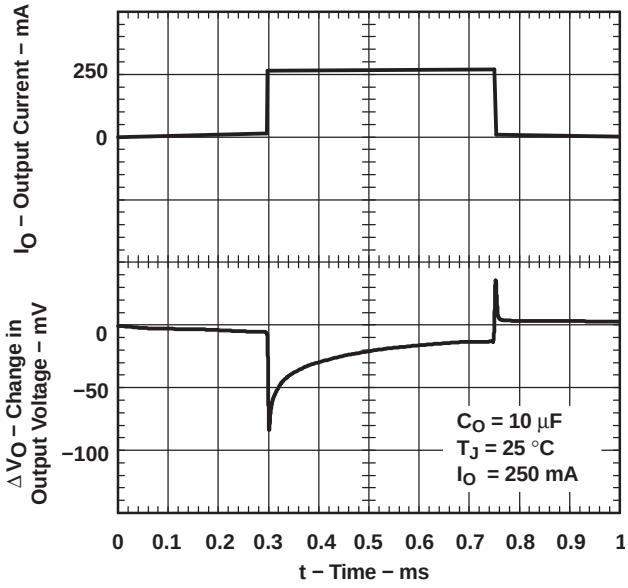


Figure 15.

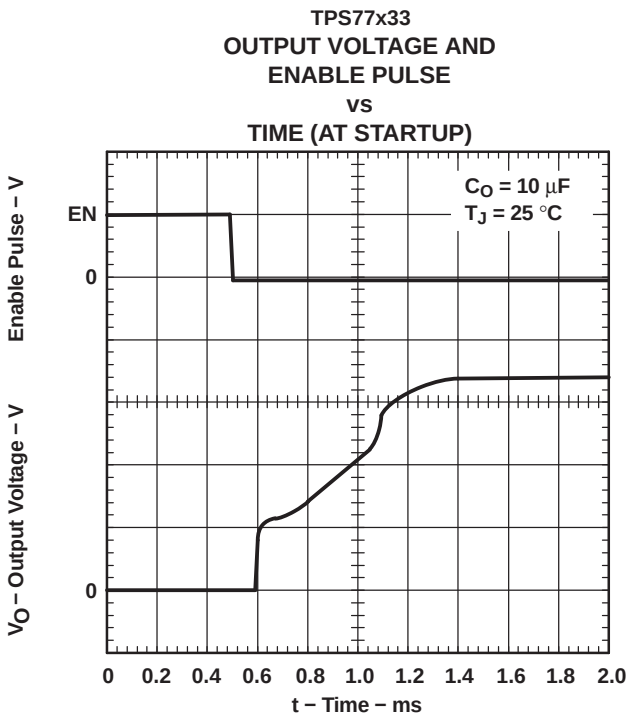


Figure 16.

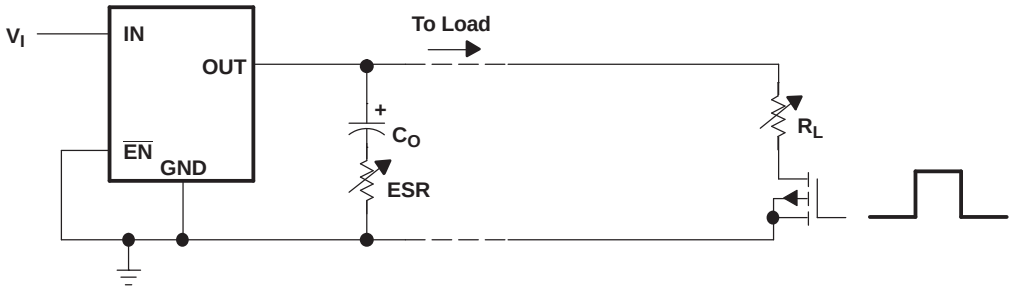


Figure 17. Test Circuit for Typical Regions of Stability (Figure 18 through Figure 21) (Fixed-Output Options)

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

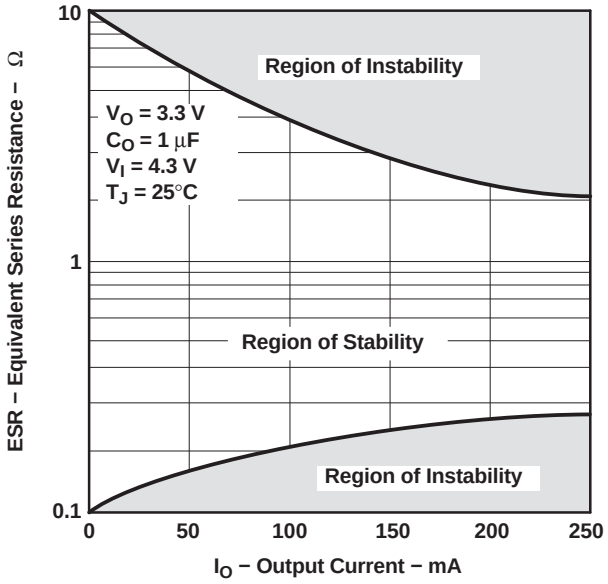


Figure 18.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

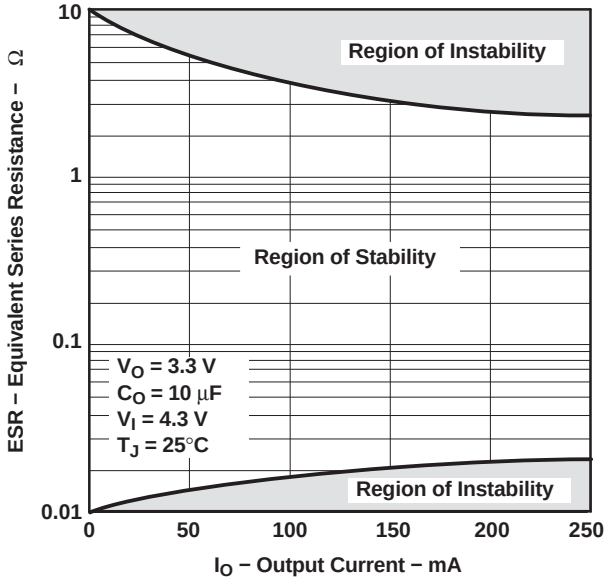


Figure 19.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

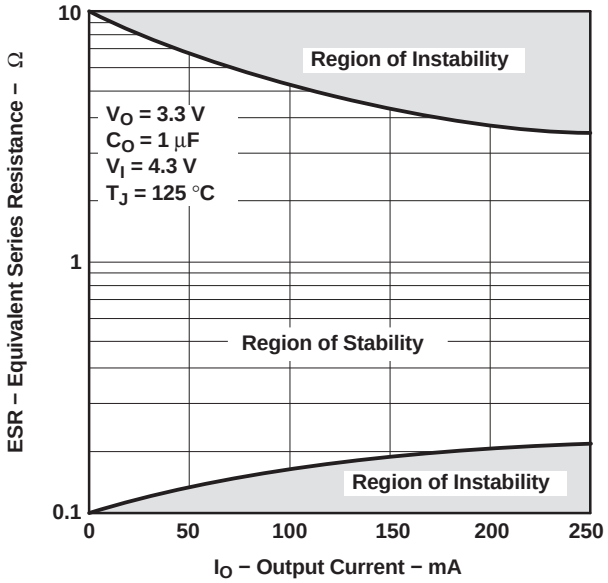


Figure 20.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

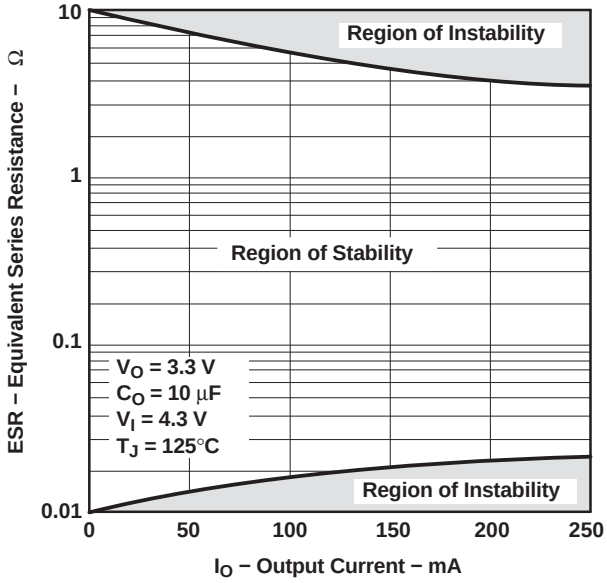


Figure 21.

APPLICATION INFORMATION

Pin Functions

Enable ($\overline{EN}$)

The $\overline{EN}$ terminal is an input that enables or shuts down the device. If $\overline{EN}$ is a logic high, the device is in shutdown mode. When $\overline{EN}$ goes to logic low, the device is enabled.

Power Good (PG)

The PG terminal is an open-drain, active-high output that indicates the status of V_{out} (output of the LDO). When V_{out} reaches 82% of the regulated voltage, PG goes to a high-impedance state. It goes to a low-impedance state when V_{out} falls below 82% (i.e., overload condition) of the regulated voltage. The open-drain output of the PG terminal requires a pullup resistor.

Sense (SENSE)

The SENSE terminal of the fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and V_{out} to filter noise is not recommended because it may cause the regulator to oscillate.

Feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_{out} to filter noise is not recommended because it may cause the regulator to oscillate.

External Capacitor Requirements

An input capacitor is not usually required; however, a bypass capacitor (0.047 µF or larger) improves load transient response and noise rejection if the device is located more than a few inches from the power supply. A higher-capacitance capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Most low-noise LDOs require an external capacitor to further reduce noise. This will impact the cost and board space. The TPS77401 have very low noise specification requirements without using any external components.

Like all LDO regulators, the TPS77401 requires an output capacitor connected between OUT (output of the LDO) and GND (signal ground) to stabilize the internal control loop. The minimum recommended capacitance value is 1 µF, provided the ESR meets the requirement in Figure 19 and Figure 21. In addition, a low-ESR capacitor can be used if the capacitance is at least 10 µF and the ESR meets the requirements in Figure 18 and Figure 20. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements previously described.

Ceramic capacitors have different types of dielectric material with each exhibiting different temperature and voltage variation. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO type ceramic type capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are, therefore, acceptable to use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature; therefore, the Y5U and Z5U are not generally recommended for use on this LDO. Independent of which type of capacitor is used, one must make certain that at the worst-case condition, the capacitance/ESR meets the requirements specified in Figure 18 through Figure 21.

Figure 22 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

APPLICATION INFORMATION (continued)

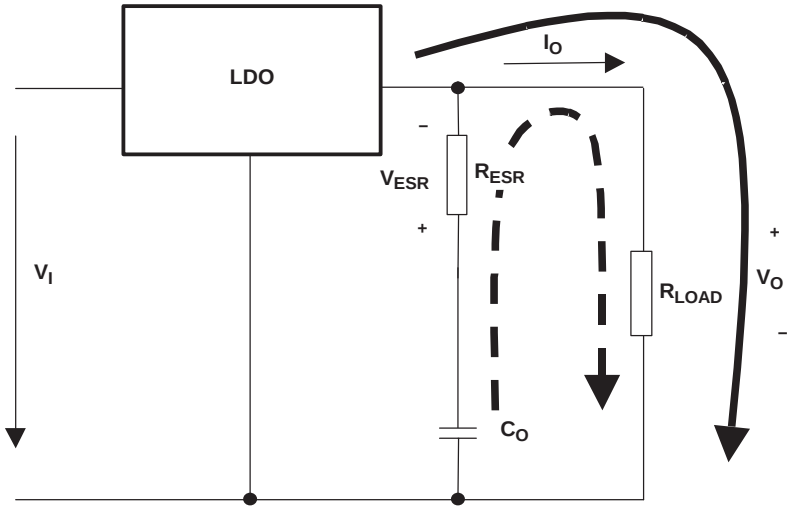


Figure 22. LDO Output Stage With Parasitic Resistances ESR

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V_{Cout} = V_{out}$). This means no current is flowing into the C_{out} branch. If I_{out} suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 23). Therefore, capacitor C_{out} provides the current for the new load condition (dashed arrow). C_{out} now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at R_{ESR}. This voltage is shown as V_{ESR} in Figure 22.
- When C_{out} is conducting current to the load, initial voltage at the load is $V_{out} = V_{Cout} – V_{ESR}$. Due to the discharge of C_{out}, the output voltage V_{out} drops continuously until the response time t_1 of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 23.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs, where number 1 displays the lowest ESR and number 3 displays the highest ESR.

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

APPLICATION INFORMATION (continued)

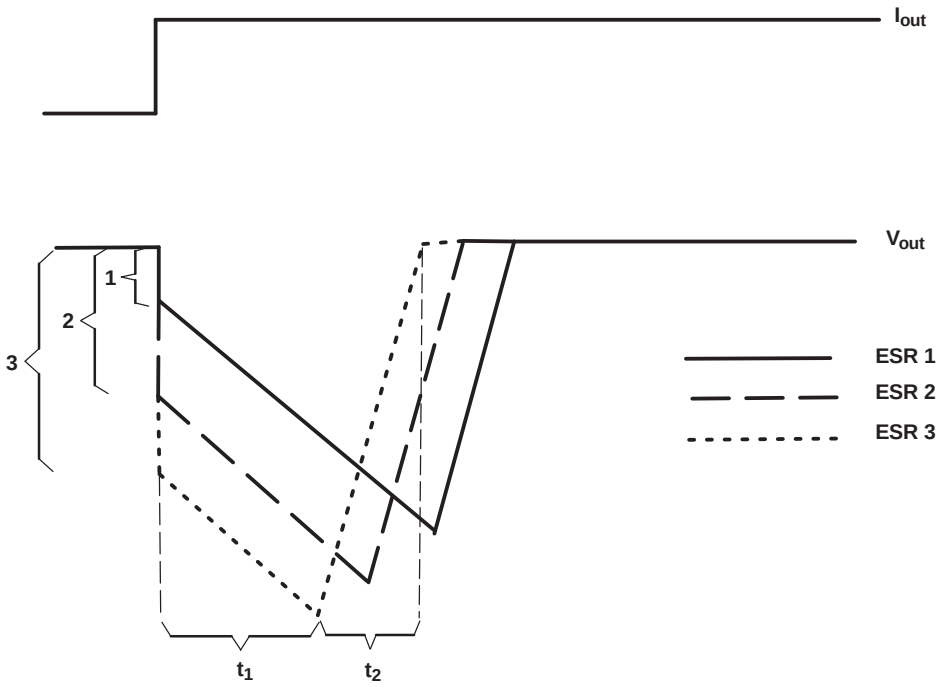


Figure 23. Correlation of Different ESRs and Their Influence to the Regulation of V_{out} at a Load Step From Low-to-High Output Current

APPLICATION INFORMATION (continued)

Programming the TPS77401 Adjustable LDO Regulator

The output voltage of the TPS77401 adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using:

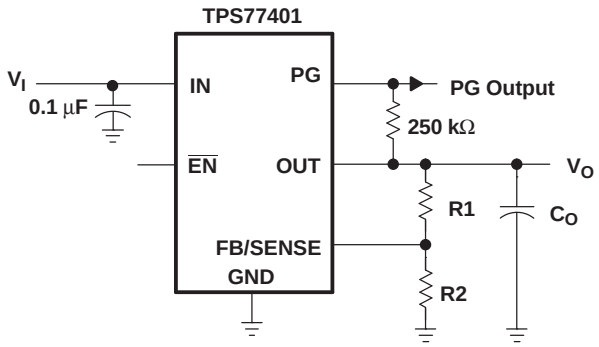
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower-value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided, as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.5	30.1	kΩ
3.3 V	53.8	30.1	kΩ
3.6 V	61.5	30.1	kΩ

NOTE: To reduce noise and prevent oscillation, R1 and R2 need to be as close as possible to the FB/SENSE terminal.

Figure 24. TPS77401 Adjustable LDO Regulator Programming

Regulator Protection

The TPS77401 PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The device also features internal current limiting and thermal protection. During normal operation, the TPS77401 limits output current to approximately 0.9 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

APPLICATION INFORMATION (continued)

Power Dissipation and Junction Temperature

Specified regulator operation is ensured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ = Maximum allowable junction temperature
$R_{\theta JA}$ = Thermal resistance, junction to ambient, for the package, i.e., 266.2°C/W for the 8-terminal MSOP with no airflow
T_A = Ambient temperature

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS77401MDGKREP	Obsolete	Production	VSSOP (DGK) | 8	-	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BYQ
TPS77401MDGKREP.A	Obsolete	Production	VSSOP (DGK) | 8	-	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BYQ
V62/06663-01XE	Obsolete	Production	VSSOP (DGK) | 8	-	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BYQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

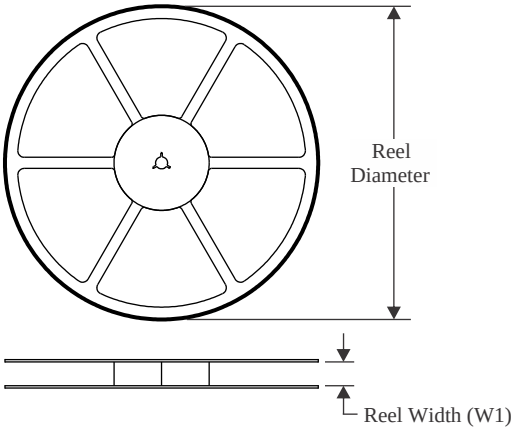
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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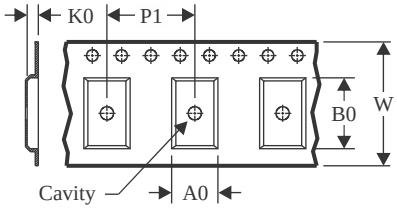
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

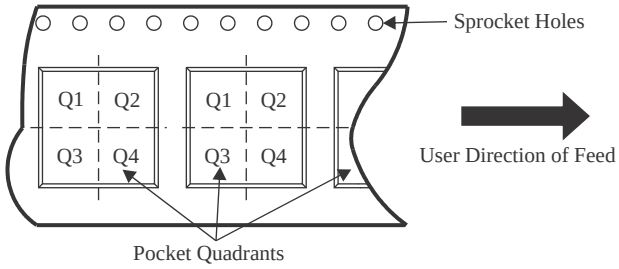


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

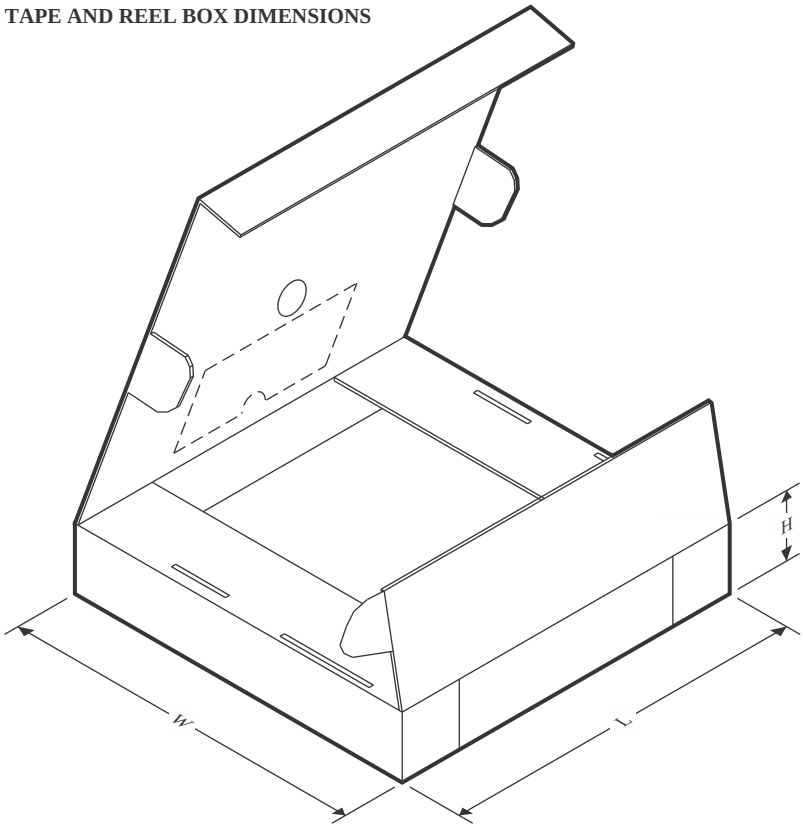
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77401MDGKREP	VSSOP	DGK	8	0	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

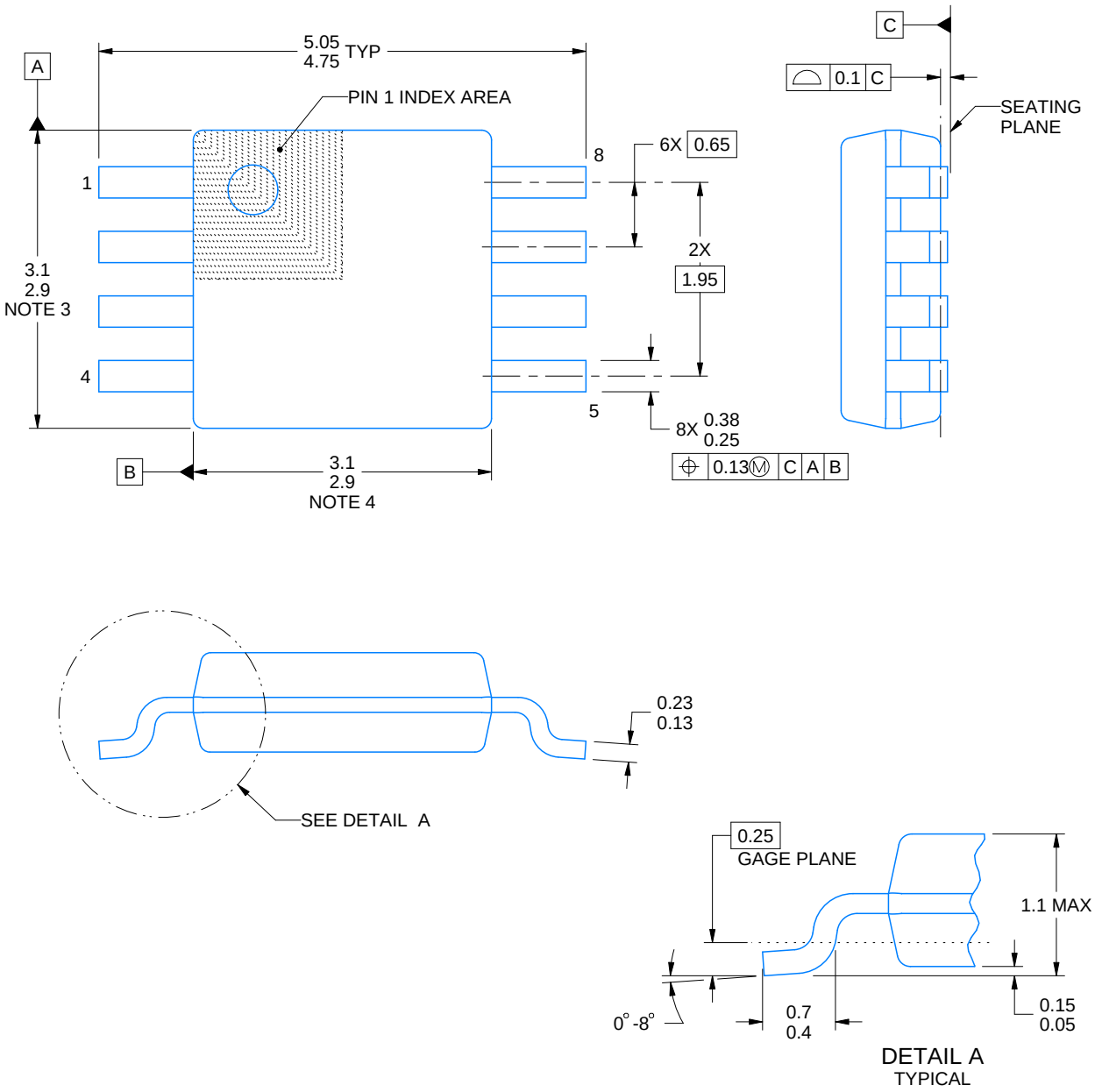
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77401MDGKREP	VSSOP	DGK	8	0	358.0	335.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

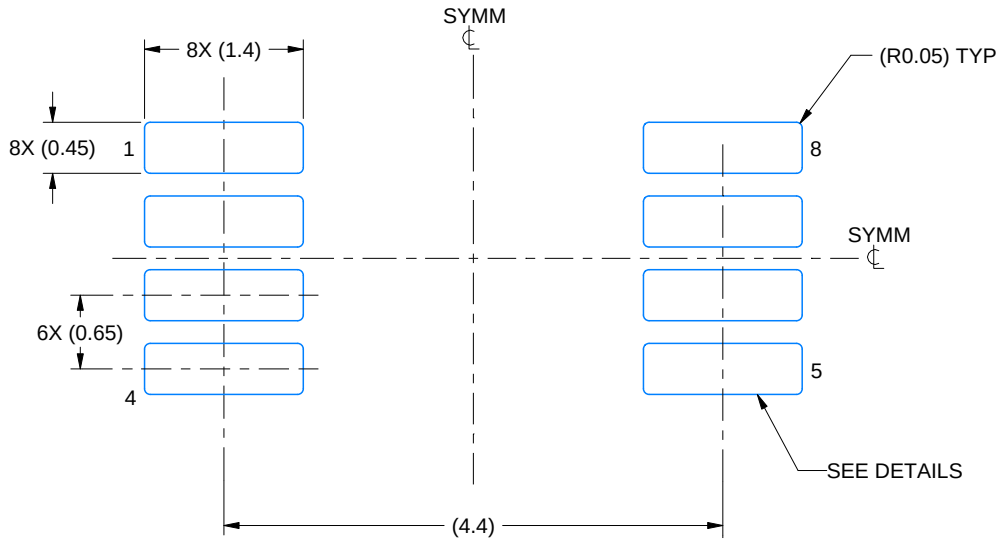
SMALL OUTLINE PACKAGE



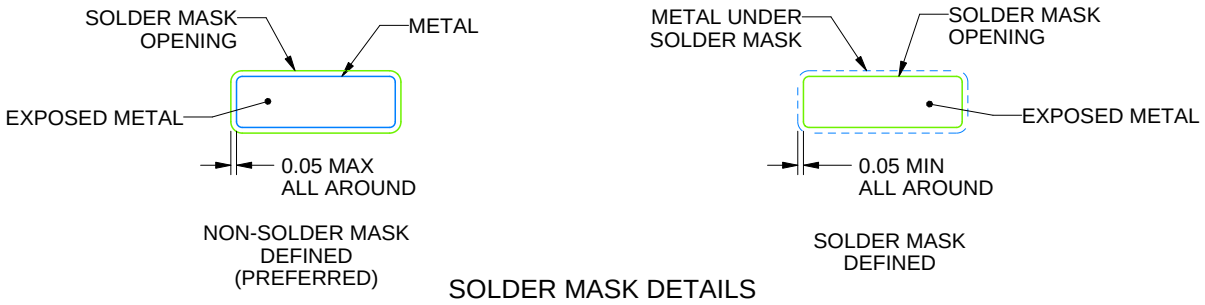
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

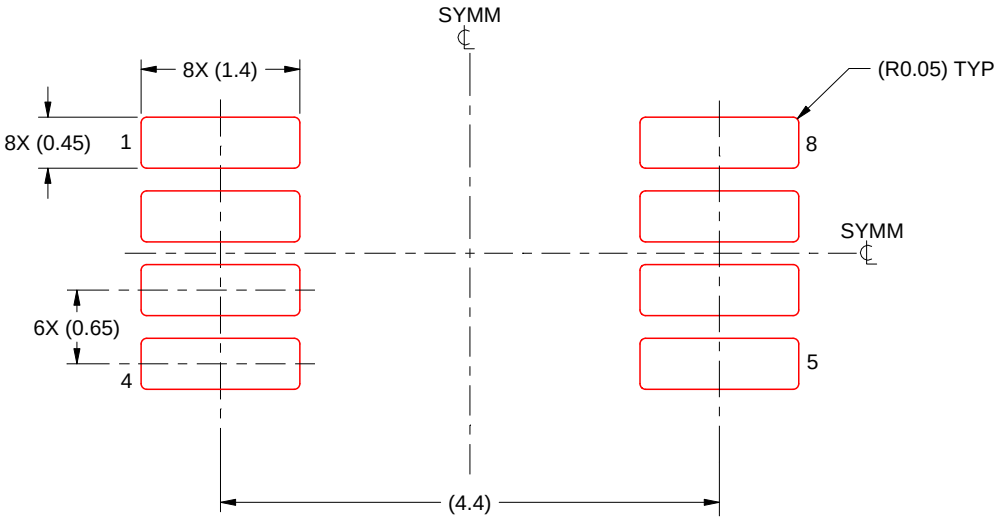


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025