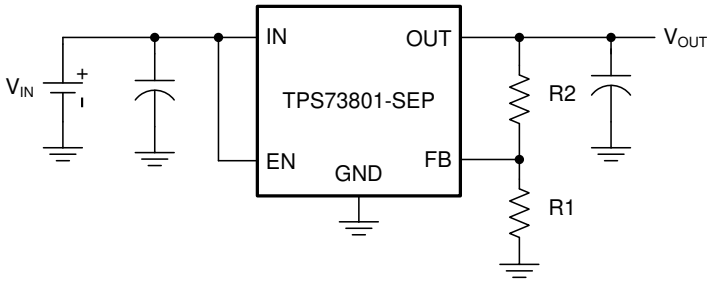
TPS73801-SEP 1-A Radiation Tolerant Low Dropout (LDO) Voltage Regulator

1 Features

- Vendor Item Drawing (VID) V62/18616
- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) availability of 50 krad(Si)
- Single-Event Effects (SEE) characterized
  - SEL, SEB, and SEGR immune up to LET = 43 MeV-cm^2/mg
  - SET and SEFI characterized up to LET = 43 MeV-cm^2/mg
- Space enhanced plastic
  - Au bondwire and NiPdAu-Ag lead finish
  - Enhanced mold compound for low outgassing
  - One fabrication, assembly, and test site
  - Extended product life cycle
  - Extended product change notification
  - Product traceability
- Optimized for fast transient response
- Output current: 1 A
- Dropout voltage: 300 mV
- Low noise: 45 μV_{RMS} (10 Hz to 100 kHz)
- 1-mA quiescent current
- No protection diodes needed
- Controlled quiescent current in dropout
- Adjustable output voltage: 1.21 V to 20 V
- Less than 1-µA quiescent current in shutdown
- Stable with 10-µF output capacitor
- Stable with ceramic capacitors
- Reverse-battery protection
- No reverse current
- Thermal limiting
- Military temperature range (–55°C to 125°C)



Simplified Schematic

2 Applications

- Supports low Earth orbit (LEO) space applications
- Space satellite payloads
- Command and data handling (C&DH)
- Optical imaging payload
- Radar imaging payload
- Satellite electrical power system (EPS)

3 Description

The TPS73801-SEP is a low-dropout (LDO) regulator optimized for fast transient response. The device can supply 1 A of output current with a dropout voltage of 300 mV. Operating quiescent current is 1 mA and drops to less than 1 µA in shutdown. In addition to fast transient response, a very low output noise makes the TPS73801-SEP regulator ideal for sensitive RF supply applications.

Output voltage range is from 1.21 to 20 V, capable of utilizing output capacitors as low as 10 µF, including ceramic. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection.

Device Information

PART NUMBER(1)	GRADE	PACKAGE
TPS73801MDCQTPSEP	50 krad(Si) RLAT	SOT-223 (6) 6.55 mm × 7.26 mm Mass = 119.8 mg(2)
TPS73801MDCQPSEP		

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Dimension and mass values are nominal.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....5
5.5 Electrical Characteristics....5
5.6 Typical Characteristics....7
6 Detailed Description....12
6.1 Overview....12
6.2 Functional Block Diagram....12
6.3 Feature Description....12
6.4 Device Functional Modes....14
7 Application and Implementation....15
7.1 Application Information....15
7.2 Typical Application....16
7.3 Power Supply Recommendations....17
7.4 Layout....17
8 Device and Documentation Support....20
8.1 Receiving Notification of Documentation Updates....20
8.2 Support Resources....20
8.3 Trademarks....20
8.4 Electrostatic Discharge Caution....20
8.5 Glossary....20
9 Revision History....20
10 Mechanical, Packaging, and Orderable Information....21

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4 Pin Configuration and Functions

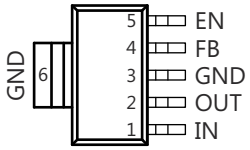

Figure 4-1. DCQ Package
SOT-223
Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	—	Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 µF to 10 µF is sufficient. The TPS73801-SEP regulators are designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
2	OUT	—	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10 µF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients.
3	GND	—	Ground.
4	FB	I	Feedback. This is the input to the error amplifier. This pin is internally clamped to ±7 V. It has a bias current of 3 µA that flows into the pin. The FB pin voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 V to 20 V.
5	EN	I	Enable. The EN pin is used to put the TPS73801-SEP regulators into a low-power shutdown state. The output is off when the EN pin is pulled low. The EN pin can be driven either by 5-V logic or open-collector gate, normally several microamperes, and the EN pin current, typically 3 µA. If unused, the EN pin must be connected to the IN pin. The device is in the low-power shutdown state if the EN pin is not connected.
6	GND	—	Ground.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{IN}	Input voltage	IN	–20	20	V
		OUT	–20	20	
		Input-to-output differential(2)	–20	20	
		FB	–7	7	
		EN	–20	20	
t_{short}	Output short-circuit duration			Indefinite	
T_J	Operating virtual-junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT cannot exceed ±20 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	V_{OUT} + VDO	20	V
V_{IH}	EN high-level input voltage	2	20	V
V_{IL}	EN low-level input voltage		0.25	V
T_J	Recommended operating junction temperature	–55	125	°C

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5.4 Thermal Information

THERMAL METRIC[1]		TPS73801-SEP DCQ (SOT-223) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	31.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

Over operating temperature range T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP[10]	MAX	UNIT
V_{IN}	Input voltage[1] [2] [12]		25°C	2.21		20	V
V_{FB}	FB pin voltage[1] [3]	V_{IN} = 2.21 V, I_{LOAD} = 1 mA	25°C	1.192	1.21	1.228	V
		V_{IN} = 2.5 V to 20 V, I_{LOAD} = 1 mA to 1 A	Full range	1.174	1.21	1.246	
	Line regulation[1]	ΔV_{IN} = 2.21 V to 20 V, I_{LOAD} = 1 mA	Full range		1.5	5	mV
	Load regulation[1]	V_{IN} = 2.5 V, ΔI_{LOAD} = 1 mA to 1 A	25°C		2	8	mV
			Full range			18	
V_{DO}	Dropout voltage[2] [5] [4] V_{IN} = $V_{OUT(NOMINAL)}$	I_{LOAD} = 1 mA	25°C		0.02	0.06	V
			Full range			0.10	
		I_{LOAD} = 100 mA	25°C		0.1	0.17	
			Full range			0.22	
		I_{LOAD} = 500 mA	25°C		0.19	0.27	
			Full range			0.35	
		I_{LOAD} = 1 A	25°C		0.24	0.30	
			Full range			0.40	
I_{GND}	GND pin current[4] [6] V_{IN} = $V_{OUT(NOMINAL)}$ + 1	I_{LOAD} = 0 mA	Full range		1	1.5	mA
		I_{LOAD} = 1 mA	Full range		1.1	1.6	
		I_{LOAD} = 100 mA	Full range		3.8	5.5	
		I_{LOAD} = 500 mA	Full range		15	25	
		I_{LOAD} = 1 A	Full range		35	80	
V_N	Output voltage noise	C_{OUT} = 10 µF, I_{LOAD} = 1 A, B_W = 10 Hz to 100 kHz	25°C		45		μV_{RMS}
I_{FB}	FB pin bias current[1] [7]		25°C		3	10	µA
V_{EN}	Shutdown threshold	V_{OUT} = OFF to ON	Full range		0.9	2	V
		V_{OUT} = ON to OFF	Full range	0.25	0.75		
I_{EN}	$\overline{EN}$ pin current [8]	V_{EN} = 0 V	25°C		0.01	1	µA
		V_{EN} = 20 V	25°C		3	30	
	Quiescent current in shutdown	V_{IN} = 6 V, V_{EN} = 0 V	25°C		0.01	1	µA
PSRR	Ripple rejection[11]	V_{IN} – V_{OUT} = 1.5 V (avg), V_{RIPPLE} = 0.5 V_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 0.75 A	25°C	55	63		dB

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5.5 Electrical Characteristics (continued)

Over operating temperature range T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP(10)	MAX	UNIT
I_{CL}	Current limit	V_{IN} = 7 V, V_{OUT} = 0 V	25°C		2		A
		V_{IN} = $V_{OUT(NOMINAL)}$ + 1	Full range	1.6			
I_{REV}	Input reverse leakage current	V_{IN} = –20 V, V_{OUT} = 0 V	Full range			1	mA
I_{RO}	Reverse output current(9)	V_{OUT} = 1.21 V, V_{IN} < 1.21 V	25°C		300	600	µA

(1) The TPS73801-SEP is tested and specified for these conditions with the FB pin connected to the OUT pin.
(2) Dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
(3) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
(4) To satisfy requirements for minimum input voltage, the TPS73801-SEP is tested and specified for these conditions with an external resistor divider (two 4.12-kΩ resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-mA DC load on the output.
(5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to $V_{IN} – V_{DROPOUT}$.
(6) GND pin current is tested with V_{IN} = ($V_{OUT(NOMINAL)}$ + 1 V) and a current source load. The GND pin current decreases at higher input voltages.
(7) FB pin bias current flows into the FB pin.
(8) EN pin current flows into the EN pin.
(9) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.
(10) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(11) Parameter is specified by characterization and is not tested in production.
(12) This is the input voltage range the device is specifed to operate under. Operation at a lower VIN that respects dropout requirements may be possible, but is not characterized or tested.

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5.6 Typical Characteristics

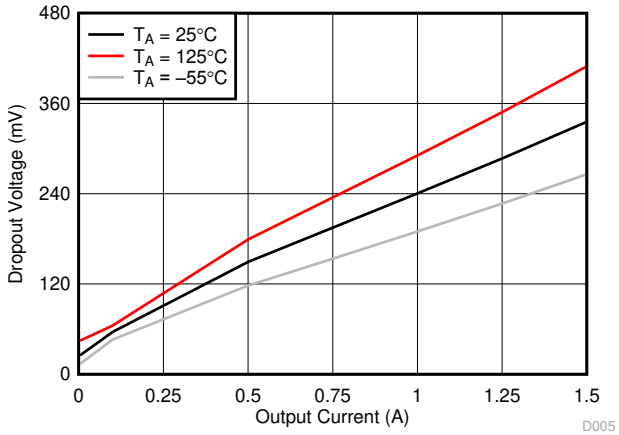


Figure 5-1. Dropout Voltage vs Output Current

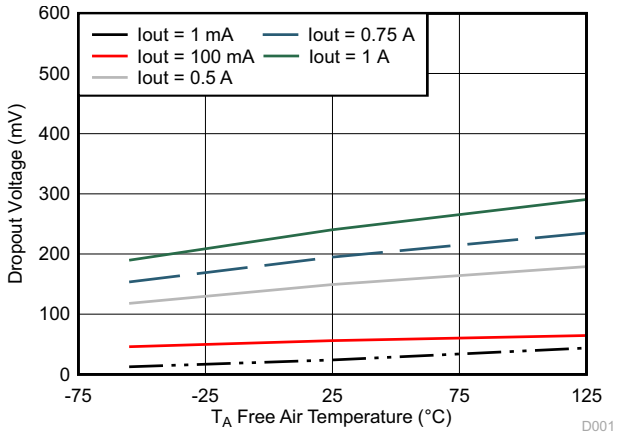
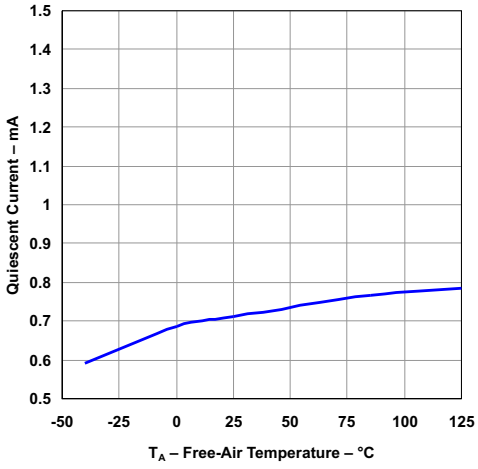
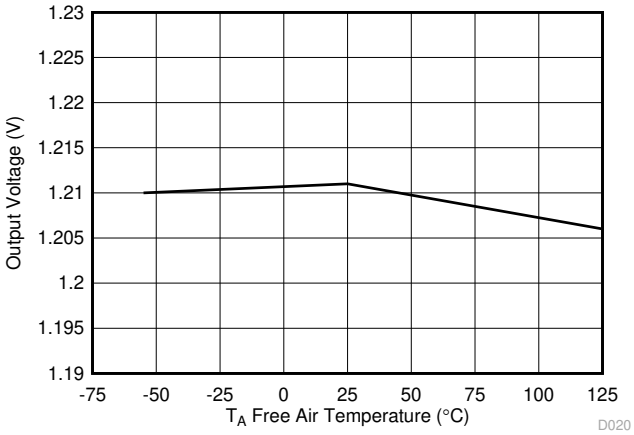


Figure 5-2. Dropout Voltage vs Temperature



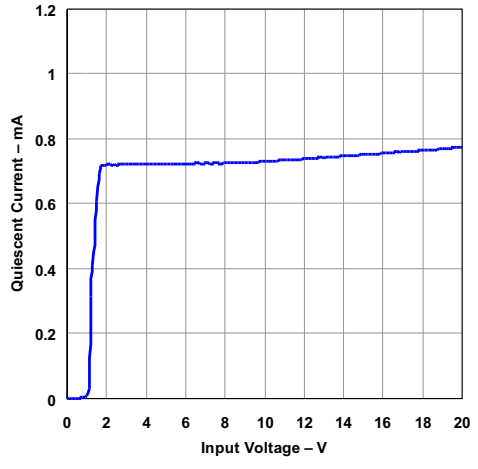
V_{IN} = 6 V I_{OUT} = 0 A $V_{EN} = V_{IN}$

Figure 5-3. Quiescent Current vs Temperature



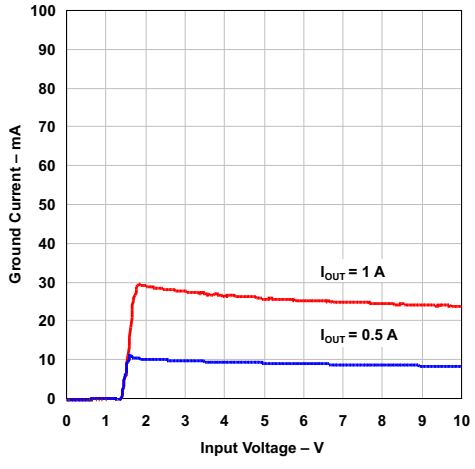
V_{IN} = 2.9 V I_{OUT} = 1 mA

Figure 5-4. Output Voltage vs Temperature



T_J = 25°C R_{OUT} = 4.3 kΩ $V_{EN} = V_{IN}$

Figure 5-5. Quiescent Current vs Input Voltage



T_J = 25°C V_{OUT} = 1.21 V $V_{EN} = V_{IN}$

Figure 5-6. Ground Current vs Input Voltage

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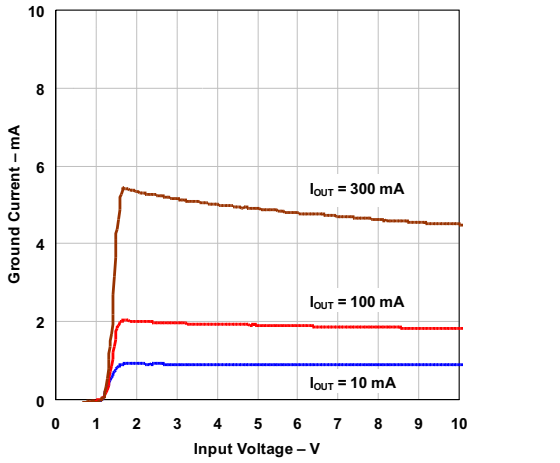
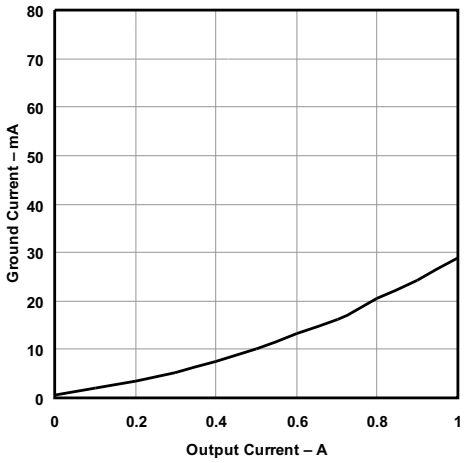
5.6 Typical Characteristics (continued)



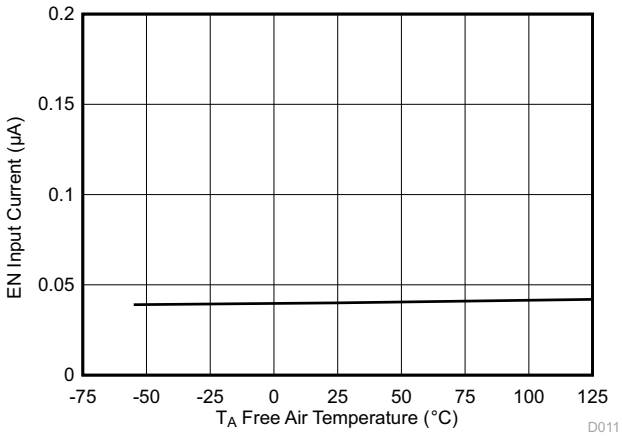
T_J = 25°C V_{OUT} = 1.21 V V_{EN} = V_{IN}

Figure 5-7. Ground Current vs Input Voltage



V_{IN} = V_{OUT}(nom) + 1

Figure 5-8. Ground Current vs Output Current



V_{EN} = 0 V

Figure 5-9. EN Input Current vs Temperature

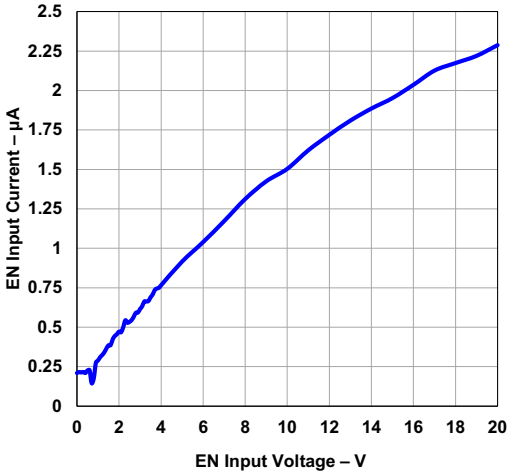
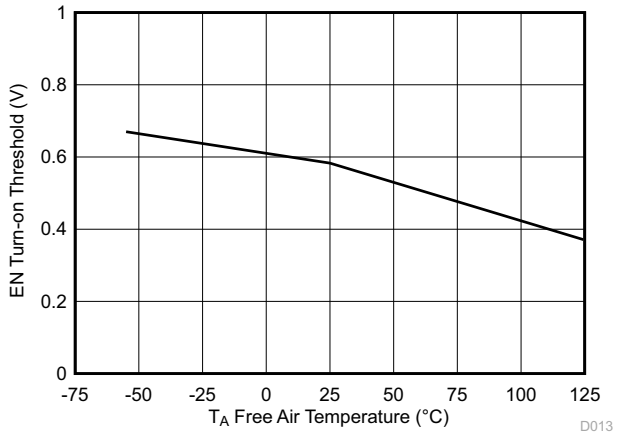
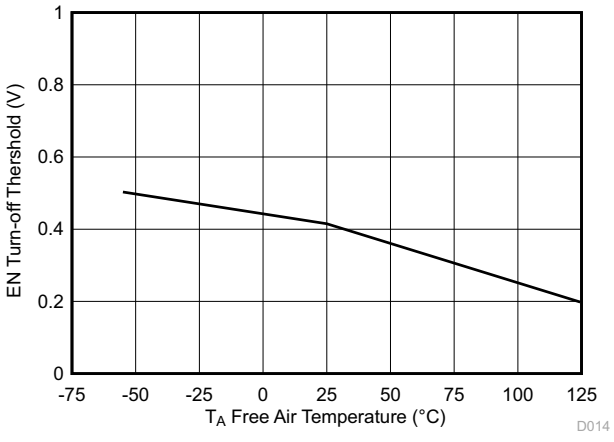


Figure 5-10. EN Input Current vs EN Input Voltage



I_{OUT} = 1 mA

Figure 5-11. EN Threshold (Off to On) vs Temperature



I_{OUT} = 1 mA

Figure 5-12. EN Threshold (On to Off) vs Temperature

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5.6 Typical Characteristics (continued)

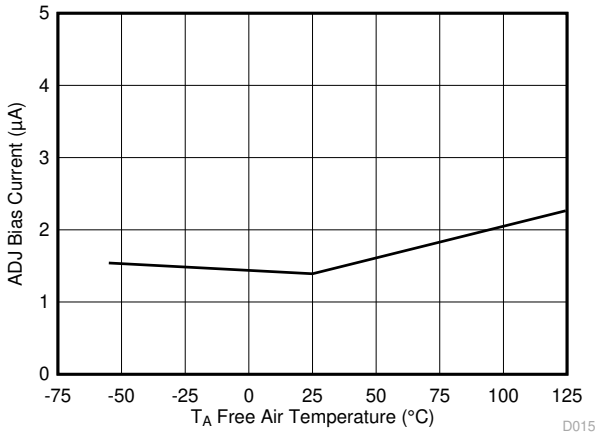
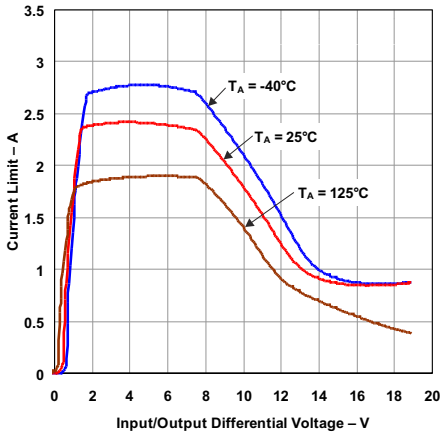
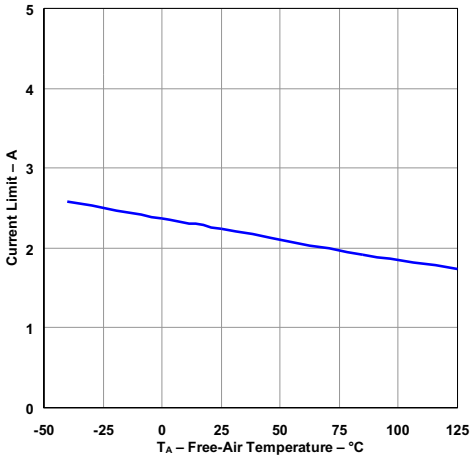


Figure 5-13. FB Bias Current vs Temperature



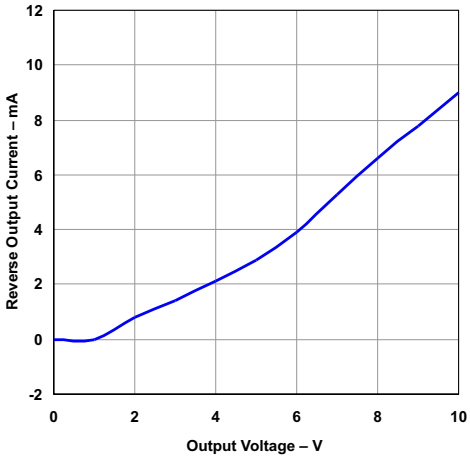
ΔV_{OUT} = 100 mV

Figure 5-14. Current Limit vs Input/Output Differential Voltage



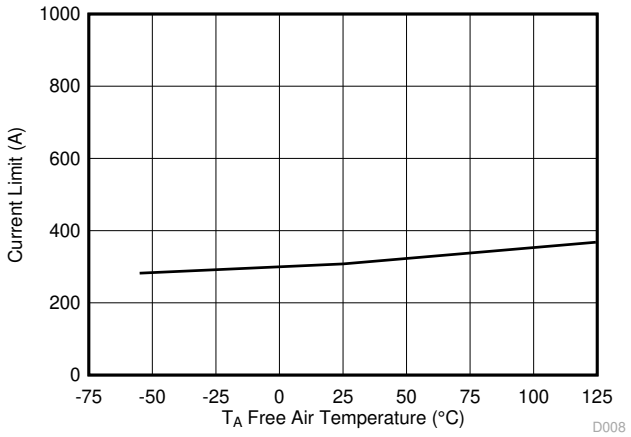
V_{IN} = 7 V V_{OUT} = 0 V

Figure 5-15. Current Limit vs Temperature



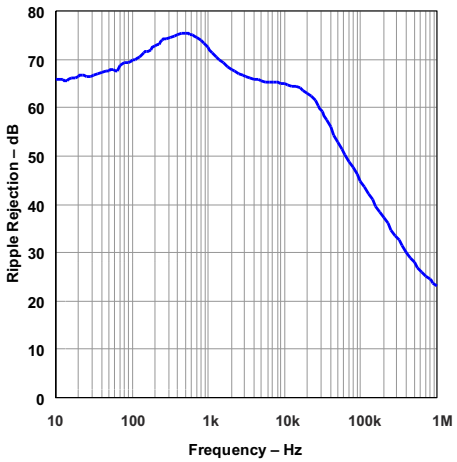
T_J = 25°C V_{IN} = 0 V Current flows into OUT pin

Figure 5-16. Reverse Output Current vs Output Voltage



V_{IN} = 0 V

Figure 5-17. Reverse Output Current vs Temperature



V_{IN} = 2.7 V V_{RIPPLE} = 0.05 V_{PP} I_{OUT} = 750 mA
C_{IN} = 0 C_{OUT} = 10 µF (ceramic) T_A = 25°C

Figure 5-18. Ripple Rejection vs Frequency

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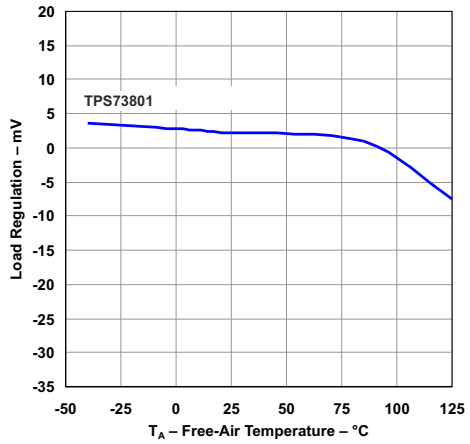
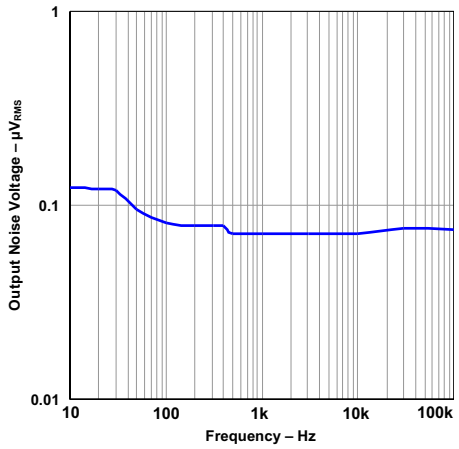
5.6 Typical Characteristics (continued)



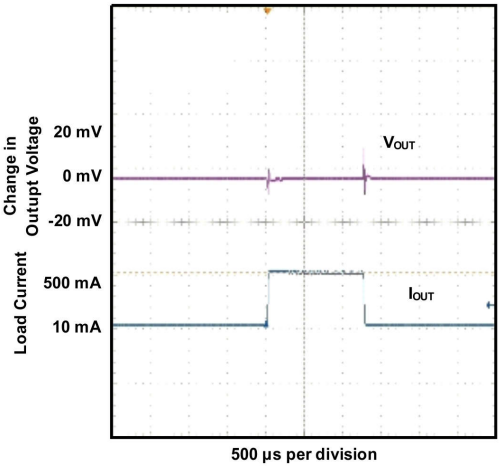
I_{OUT} = 1 A

Figure 5-19. Load Regulation vs Temperature



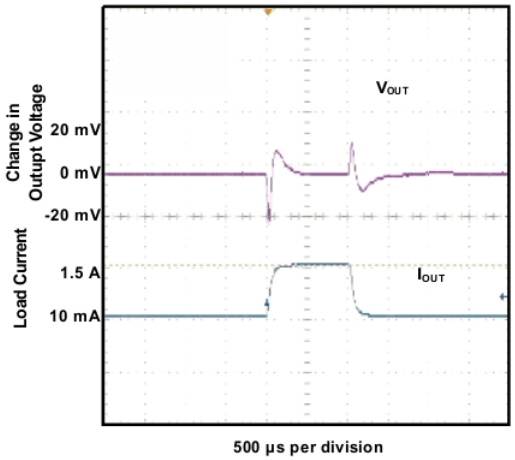
C_{OUT} = 10 µF (ceramic) I_{OUT} = 1 A

Figure 5-20. Output Noise Voltage vs Frequency



V_{IN} = 4.3 V C_{IN} = 10 µF C_{OUT} = 10 µF (ceramic)

Figure 5-21. Load Transient Response



V_{IN} = 4.3 V C_{IN} = 10 µF C_{OUT} = 10 µF (ceramic)

Figure 5-22. Max Load Transient Response

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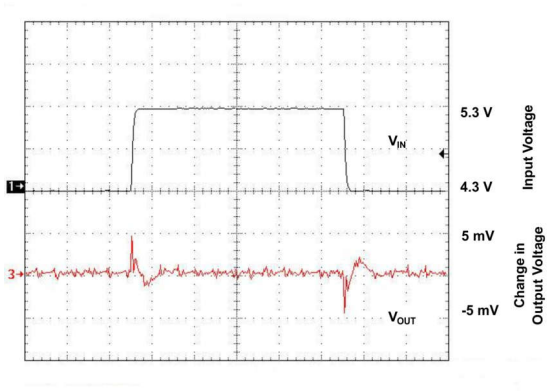
5.6 Typical Characteristics (continued)



I_{OUT} = 1.5 A C_{IN} = 10 µF C_{OUT} = 10 µF (ceramic)

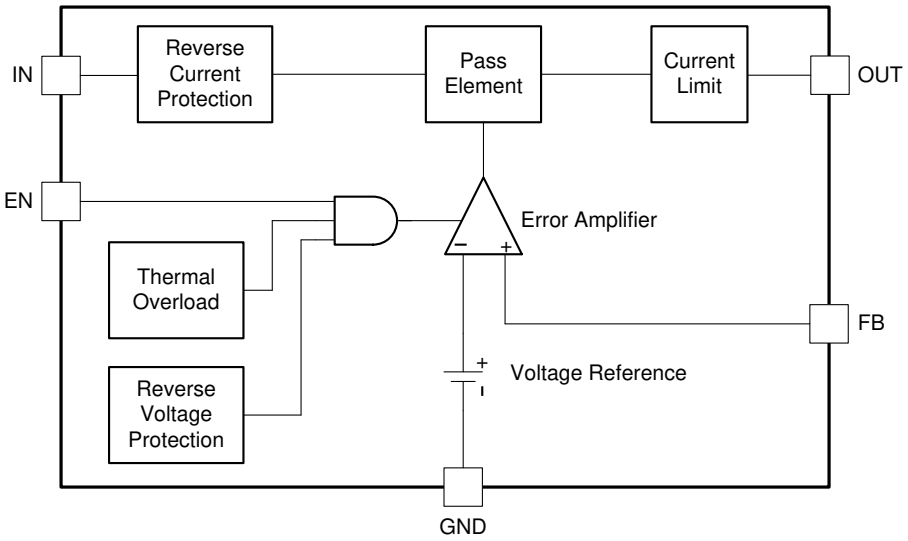
Figure 5-23. Line Transient Response

6 Detailed Description

6.1 Overview

The TPS73801-SEP is a 1-A LDO regulator optimized for fast transient response. The devices are capable of supplying 1 A at a dropout voltage of 300 mV. The low operating quiescent current (1 mA) drops to less than 1 µA in shutdown. In addition to the low quiescent current, the TPS73801-SEP regulators incorporate several protection features which make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the input is pulled to ground, the TPS73801-SEP acts as if it has a diode in series with its output and prevents reverse current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20 V and still allow the device to start and operate.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Adjustable Operation

The TPS73801-SEP has an adjustable output voltage range of 1.21 V to 20 V. The output voltage is set by the ratio of two external resistors as shown in Figure 6-1. The device maintains the voltage at the FB pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V / R1), and the current in R2 is the current in R1 plus the FB pin bias current. The FB pin bias current, 3 µA at 25°C, flows through R2 into the FB pin. The output voltage can be calculated using the formula shown in Equation 1. The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown the output is turned off, and the divider current is zero.

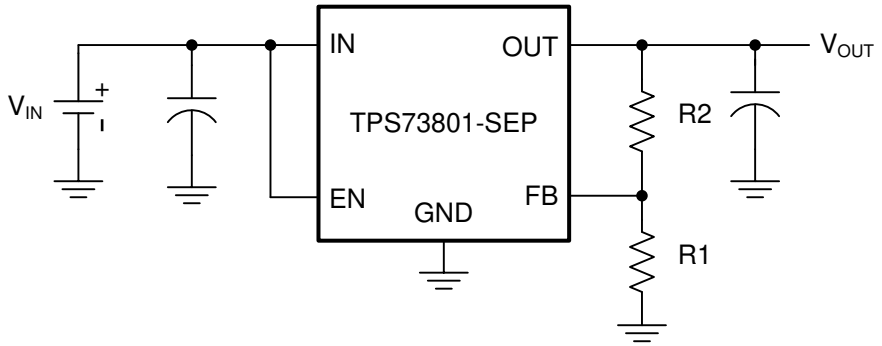


Figure 6-1. Adjustable Operation

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The output voltage can be set using the following equations:

$$V_{OUT} = 1.21\ V\left(1 + \frac{R2}{R1}\right) + I_{FB} \times R2 \quad (1)$$

$$V_{FB} = 1.21\ V \quad (2)$$

$$I_{FB} = 3\ \mu A \text{ at } 25°C \quad (3)$$

Output Range = 1.21 to 20 V (4)

6.3.2 Fixed Operation

The TPS73801-SEP can be used in a fixed voltage configuration. By connecting the FB pin to OUT, the TPS73801-SEP will regulate the output to 1.21 V. During fixed voltage operation, the FB pin can be used for a Kelvin connection if routed separately to the load. This allows the regulator to compensate for voltage drop across parasitic resistances (R_P) between the output and the load. This becomes more crucial with higher load currents.

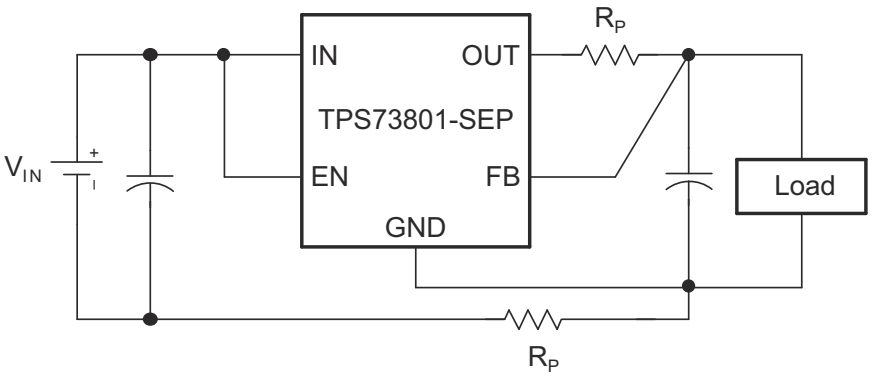

Figure 6-2. Kelvin Sense Connection

6.3.3 Overload Recovery

Like many IC power regulators, the TPS73801-SEP has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown. See Figure 5-14.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TPS73801-SEP.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

6.3.4 Output Voltage Noise

The TPS73801-SEP regulators have been designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically 40 nV/$\sqrt{Hz}$ over this frequency bandwidth for the TPS73801-SEP. For higher output voltages (generated by using a resistor divider), the output

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voltage noise is gained up accordingly. This results in RMS noise over the 10-Hz to 100-kHz bandwidth of 14 μVRMS for the TPS73801-SEP.

Higher values of output voltage noise may be measured when care is not exercised with regards to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TPS73801-SEP. Power supply ripple rejection must also be considered; the TPS73801-SEP regulators do not have unlimited power-supply rejection and pass a small portion of the input noise through to the output.

6.3.5 Protection Features

The TPS73801-SEP regulators incorporate several protection features that make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 μA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TPS73801-SEP can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. The output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the EN pin turns off the device and stops the output from sourcing the short-circuit current.

The FB pin can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the FB pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the FB pin is connected to a resistor divider that would pull the FB pin above its 7-V clamp voltage if the output is pulled high, the FB pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the FB pin to less than 5 mA when the FB pin is at 7 V. The 13-V difference between OUT and FB pins divided by the 5-mA maximum current into the FB pin yields a minimum top resistor value of 2.6 kΩ.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. When the IN pin of the TPS73801-SEP is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 μA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin has no effect on the reverse output current when the output is pulled above the input.

6.4 Device Functional Modes

See the device modes in Table 6-1.

Table 6-1. Device Modes

EN	DEVICE STATE
H	Regulated voltage
L	Shutdown

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Output Capacitance and Transient Response

The TPS73801-SEP regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10uF with an ESR of 3 Ohms or less is recommended as a starting point for stable operation. Adding footprints for components such as a feedforward capacitor is recommended practice to allow tuning of stability if needed based on hardware results. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS73801-SEP, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10-µF Y5V capacitor can exhibit an effective value as low as 1 µF to 2 µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

7.1.2 Startup Considerations

The TPS73801-SEP does not have a built-in soft start feature to control the rise of the output during startup. Consideration should be given to the inrush current and the manner in which the device is enabled.

If the slew rate of the input supply is controlled, one of the simplest methods to control the rise of the output is to tie EN to IN. This allows the output voltage to follow the rising input voltage (minus the dropout voltage) after the EN turn-on threshold has been crossed until the output tops out at its programmed set voltage.

If the LDO is enabled after the input voltage is already high, there are additional startup considerations. Designs with larger output capacitance may see the inrush current hit the current limit, limiting the slew rate of the rising output but potentially coming with thermal or part stress drawbacks. Designs with both minimal output capacitance and low loads may experience a temporary overshoot at startup due to the combination of fast output slew rate and slow discharge rate from the load. A feed-forward capacitor, added bleeder load, or external soft start circuitry are a few methods for overshoot mitigation.

If integrated soft-start is desired, consider the TPS7H1121-SEP. This 2.25V to 14V input, 0.6V minimum output, 2A load LDO features programmable current limit, power good output, and external compensation in addition to the programmable soft-start.

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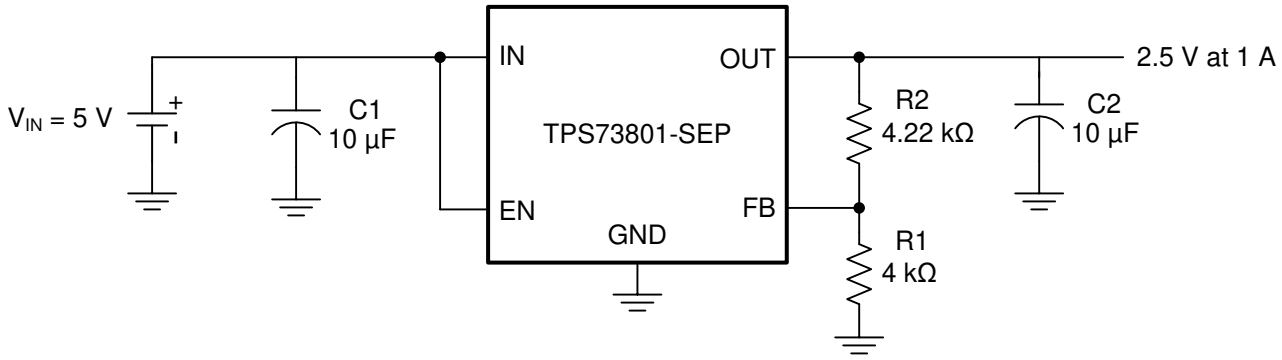
7.2 Typical Application

This section will highlight some of the design considerations when implementing this device in various applications.



All capacitors are ceramic.

Figure 7-1. Adjustable Output Voltage Operation

7.2.1 Design Requirements

Table 7-1 shows the design parameters for this application.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	5 V
Output voltage (V_{OUT})	2.5 V
Output current (I_{OUT})	0 to 1 A
Load regulation	1%

7.2.2 Detailed Design Procedure

The TPS73801-SEP has an adjustable output voltage range of 1.21 to 20 V. The output voltage is set by the ratio of two external resistors R1 and R2 as shown in Figure 7-1. The device maintains the voltage at the FB pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V / R1), and the current in R2 is the current in R1 plus the FB pin bias current. The FB pin bias current, 3 µA at 25°C, flows through R2 into the FB pin. The output voltage can be calculated using Equation 5.

$$V_{OUT} = 1.21\,V\left(1+\frac{R2}{R1}\right)+I_{FB}\times R2 \tag{5}$$

The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown the output is turned off, and the divider current is zero. For an output voltage of 2.50 V, R1 will be set to 4.0 kΩ. R2 is then found to be 4.22 kΩ using the equation above.

$$V_{OUT} = 1.21V\left(1+\frac{4.22k\Omega}{4.0k\Omega}\right)+3\mu A\times 4.22k\Omega \tag{6}$$

$$V_{OUT} = 2.50\ V \tag{7}$$

The adjustable device is tested and specified with the FB pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: V_{OUT} / 1.21 V. For example, load regulation for an output current change of 1 mA to 1.5 A is –2 mV (typ) at V_{OUT} = 1.21 V. At V_{OUT} = 2.50 V, the typical load regulation is:

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(2.50 V / 1.21 V)(–2 mV) = –4.13 mV (8)

Figure 7-2 shows the actual change in output is approximately 3 mV for a 1-A load step. The maximum load regulation at 25°C is –8 mV. At V_{OUT} = 2.50 V, the maximum load regulation is:

(2.50 V / 1.21 V)(–8 mV) = –16.53 mV (9)

Since 16.53 mV is 0.7% of the 2.5-V output voltage, the load regulation will meet the design requirements.

7.2.3 Application Curve

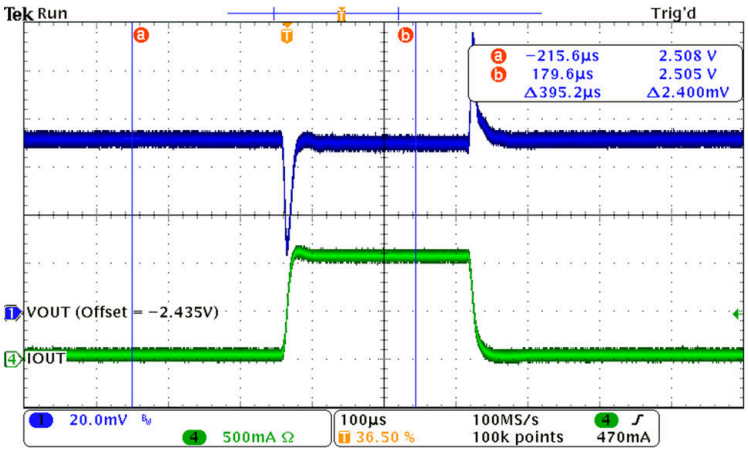

Figure 7-2. 1-A Load Transient Response

7.3 Power Supply Recommendations

The device is designed to operate with an input voltage supply up to 20 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

1. For best performance, all traces should be as short as possible.
2. Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
3. A minimum output capacitor of 10 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. X5R and X7R dielectrics are preferred.
4. Place the output capacitor as close as possible to the OUT pin of the device.
5. The tab of the DCQ package should be connected to ground.

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7.4.2 Layout Example

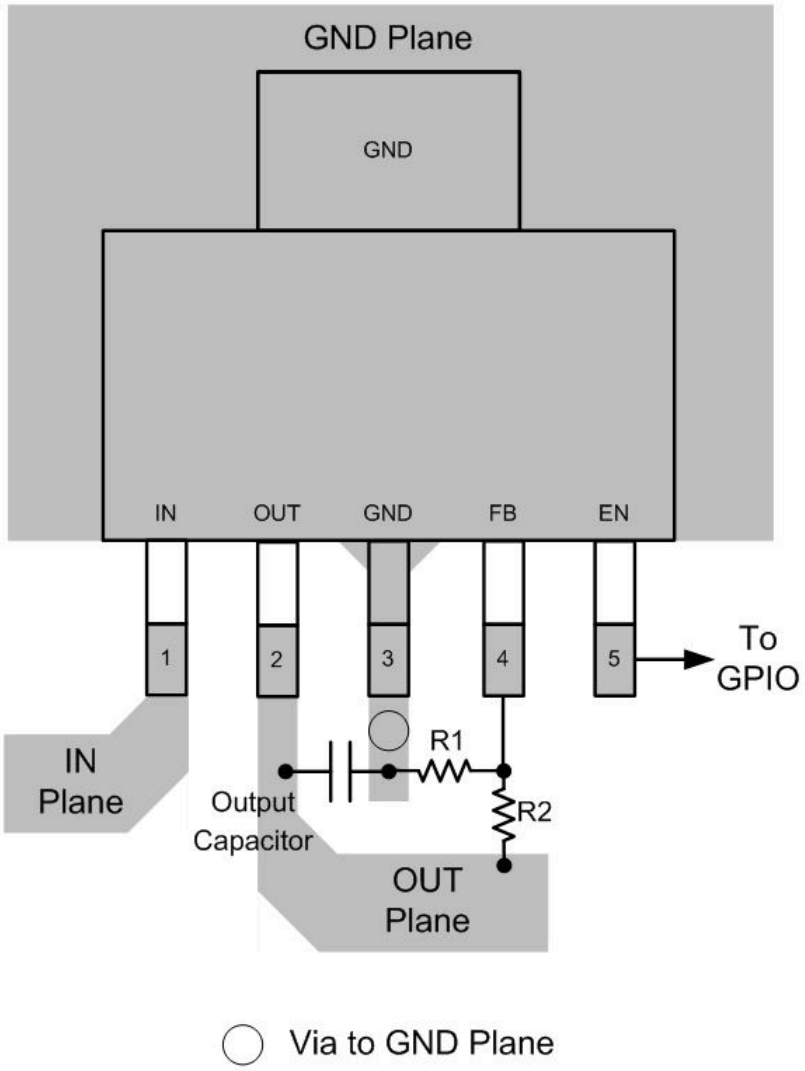

Figure 7-3. SOT-223 Layout Example (DCQ)

7.4.3 Thermal Considerations

The power handling capability of the device is limited by the recommended maximum operating junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: I_{OUT} (V_{IN} – V_{OUT})
2. GND pin current multiplied by the input voltage: I_{GND} × V_{IN}

The GND pin current can be found using the GND Pin Current graphs in Section 5.6 . Power dissipation is equal to the sum of the two components listed above.

The TPS73801-SEP series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the recommended maximum operating junction temperature is 125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

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7.4.3.1 Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 V to 6 V, an output current range of 0 mA to 500 mA, and a maximum ambient temperature of 50°C, what is the operating junction temperature?

The power dissipated by the device is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)}) \quad (10)$$

where

- $I_{OUT(MAX)}$ = 500 mA
- $V_{IN(MAX)}$ = 6 V
- I_{GND} at (I_{OUT} = 500 mA, V_{IN} = 6 V) = 10 mA

So,

$$P = 500\ mA \times (6\ V - 3.3\ V) + 10\ mA \times 6\ V = 1.41\ W \quad (11)$$

The thermal resistance of the DCQ package is 50.5°C/W. So the junction temperature rise above ambient is approximately equal to:

$$1.41\ W \times 50.5°C/W = 71.2°C \quad (12)$$

The junction temperature rise can then be added to the maximum ambient temperature to find the operating junction temperature (T_J):

$$T_J = 50°C + 71.2°C = 121.2°C \quad (13)$$

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8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2021) to Revision B (July 2026)	Page
• Changed rated TID from 20krad(Si) to 50krad(Si) and updated formatting	1
• Added temperature range	1
• Added links to the VID and radiation reports	1
• Added RthetaJC(bot) information	5
• Updated VIN min and VEN min. Added footnote to clarify VIN spec	5
• Added section to give guidance on the startup behavior of the device	15

Changes from Revision * (December 2018) to Revision A (May 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated radiation hardened and space enhanced plastic bullets in the *Features* section	1
• Updated *Applications* section	1
• Added device mass and dimensions to Device Information table	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73801MDCQPSEP	Active	Production	SOT-223 (DCQ) | 6	78 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
TPS73801MDCQPSEP.A	Active	Production	SOT-223 (DCQ) | 6	78 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
TPS73801MDCQTPSEP	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
TPS73801MDCQTPSEP.A	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
V62/18616-01XE	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
V62/18616-01XE-T	Active	Production	SOT-223 (DCQ) | 6	78 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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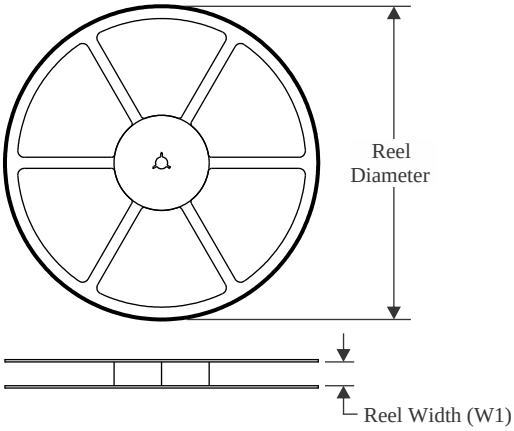
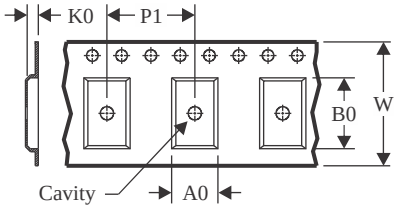
TAPE AND REEL INFORMATION

REEL DIMENSIONS

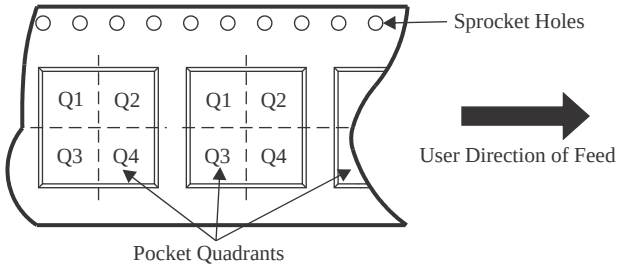


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

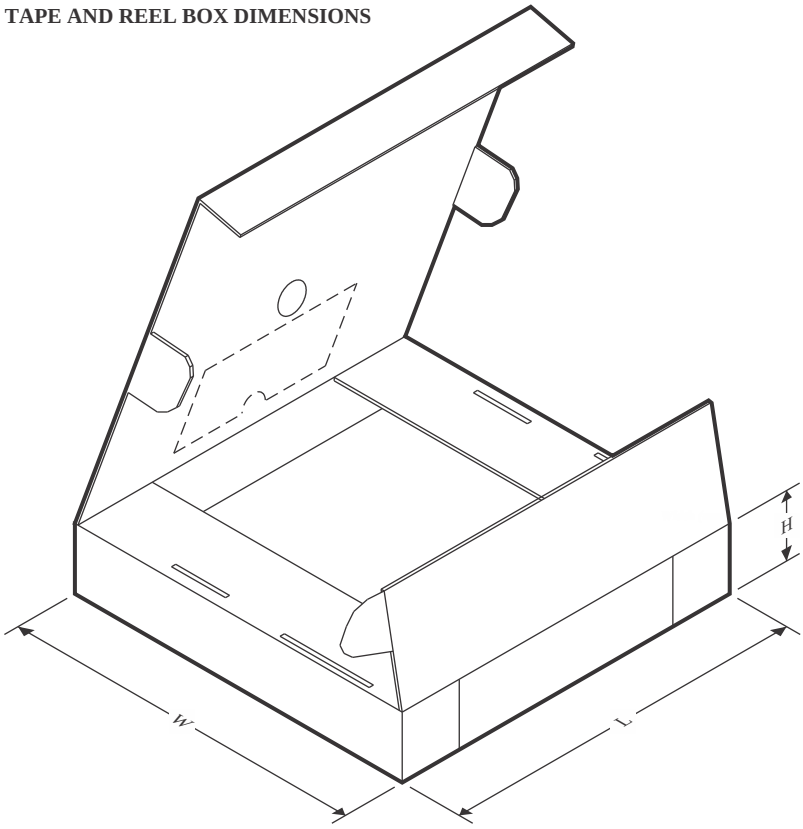
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73801MDCQTPSEP	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3

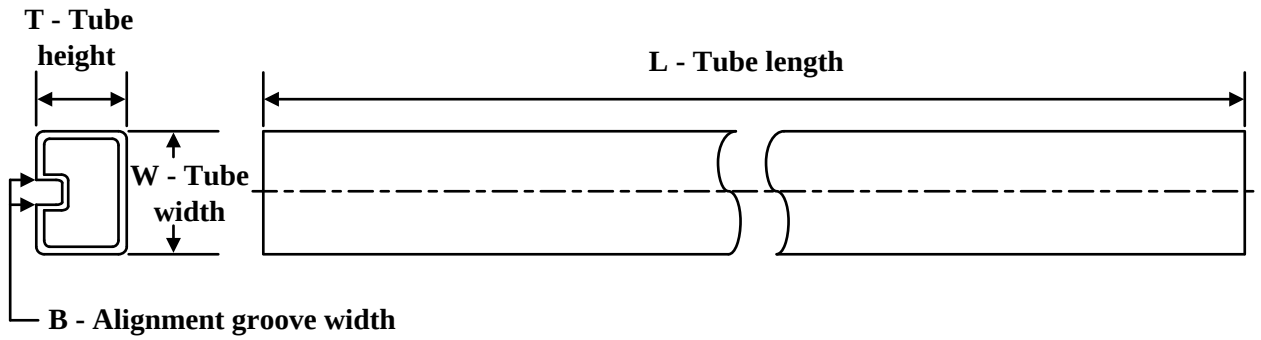
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73801MDCQTPSEP	SOT-223	DCQ	6	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

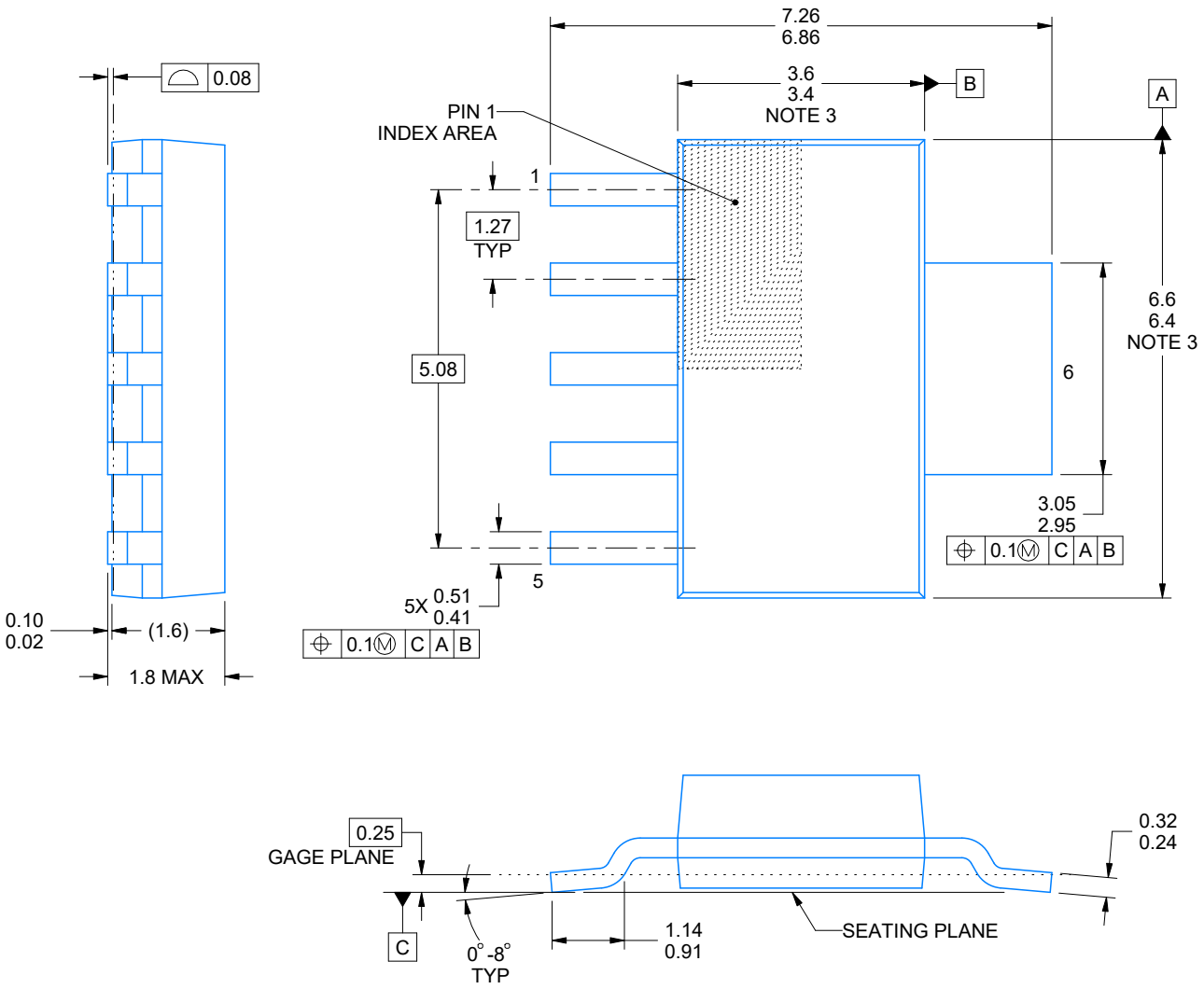
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS73801MDCQPSEP	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73801MDCQPSEP.A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
V62/18616-01XE-T	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



4214845/C 11/2021

NOTES:

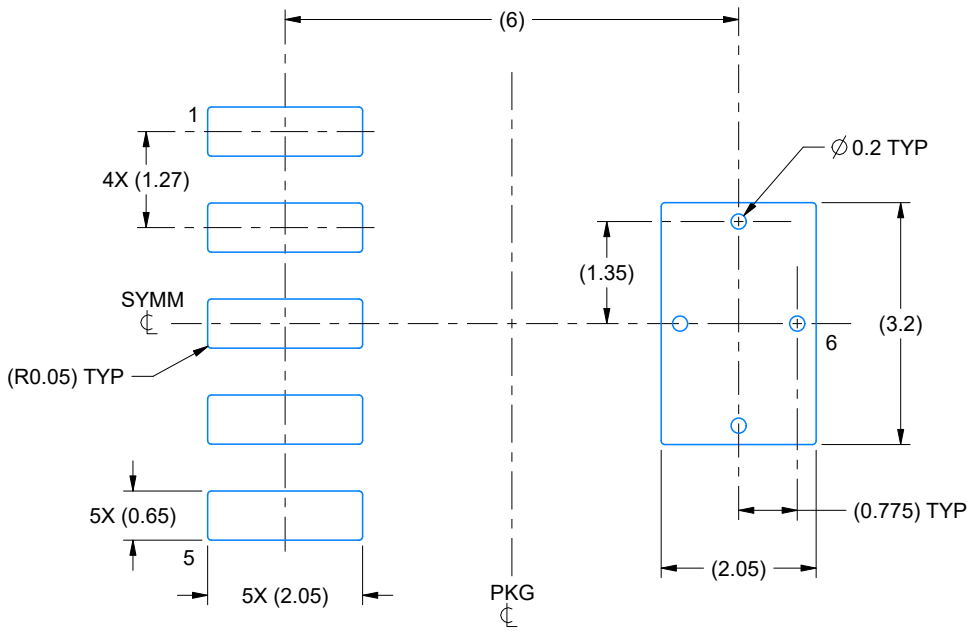
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

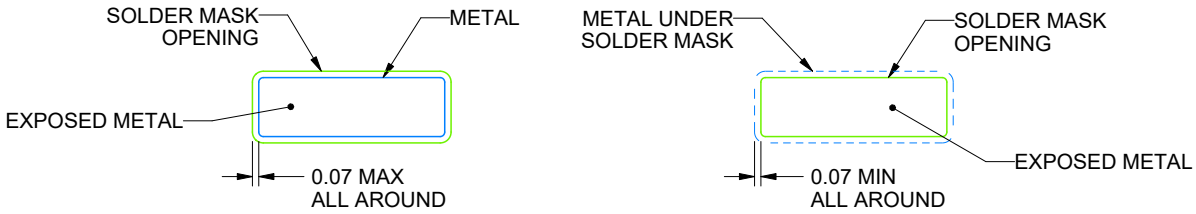
DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

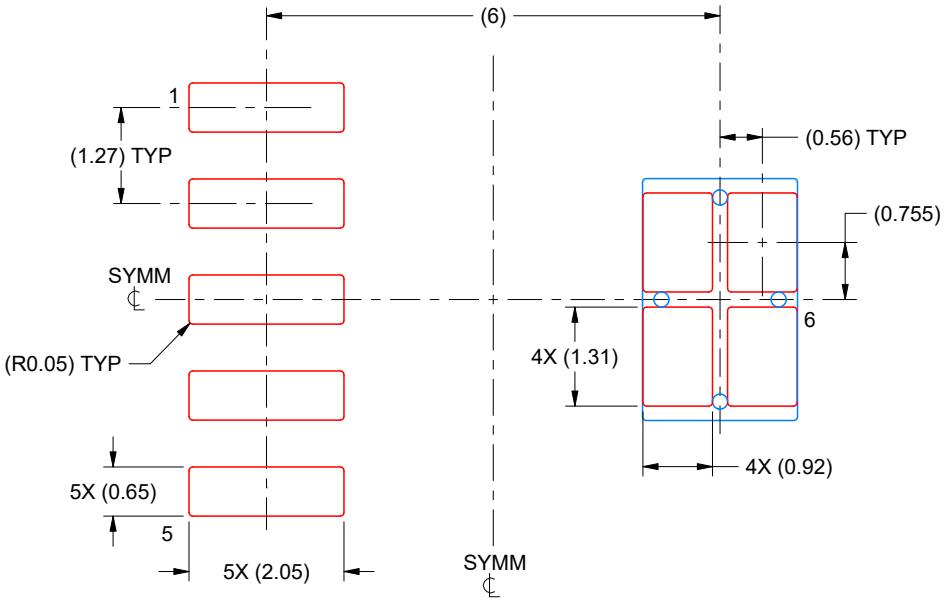


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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