TPS723 200-mA, Low-Noise, High-PSRR, Negative Output Low-Dropout Linear Regulators

1 Features

- Input voltage range: –2.7V to –10V (–11V abs. max)
- Available in –2.5V (fixed) and –1.186V to –10V (adjustable) versions
- V_{OUT} accuracy (across line, load and temperature):
  - ±1.6% for new chip
  - ±3.0% for legacy chip
- Output current: Up to 200mA
- Ultra-low noise: 60μV_{RMS} (typ) with 10nF NR cap
- Low I_Q (new chip): 30μA at I_{LOAD} = 0mA
- High PSRR: 65dB (typ) at 1kHz, 40dB (typ) at 100kHz
- Low dropout voltage:
  - 140mV (typ) at 200mA, –2.5V (new chip)
  - 280mV (typ) at 200mA, –2.5V (legacy chip)
- Stable with a 2.2μF ceramic output capacitor
- Less than 2μA (max) quiescent current in shutdown mode
- Thermal and overcurrent protection
- Operating junction temperature: –40°C to +125°C
- Packages:
  - New chip:
    - 5-pin SOT-23 (DBV) [$R_{\theta JA}$: 153.7°C/W]
  - Legacy chip:
    - 5-pin SOT-23 (DBV) [$R_{\theta JA}$: 206.9°C/W]
    - 5-pin SOT-23-THIN (DDC) [$R_{\theta JA}$: 194.8°C/W]
    - 6-pin WSON (DRV) [$R_{\theta JA}$: 85.6°C/W]

2 Applications

- Optical modules
- Semiconductor manufacturing
- Medical accessories
- Oscilloscopes
- Active antenna system mMIMO (AAS)

3 Description

The TPS723 low-dropout (LDO) negative voltage regulator offers an ideal combination of features to support low noise analog and mixed-signal applications. The TPS723 supports input voltages from –10V to –2.7V, and outputs from –10V to –1.186V (in adjustable config). This regulator is stable with small, low-cost ceramic capacitors (up-to 2.2μF), and includes enable (EN) and noise reduction (NR) functions.

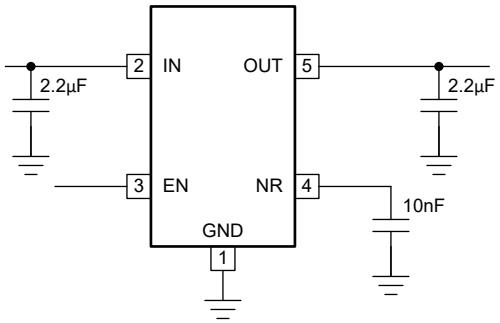
The TPS723 supports very tight DC accuracy of ±1.6% (new chip) over line, load and temperature range. The device responds quickly to line and load transients. The TPS723 supports a low dropout of typically 140mV (typ , new chip) at 200mA of load current. The device has built-in protection mechanism for over-current and overtemperature for reliable operation of the LDO.

The TPS723 supports low noise on output (60μV_{RMS} with NR cap of 10nF) and available in a small 5-pin SOT-23 package,with performance fully specified over a temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1) (2)	PACKAGE SIZE(3)
TPS723	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DDC (SOT-23-THIN, 5)	2.9mm × 2.8mm
	DRV (WSON, 6)	2mm × 2mm

(1) For more information, see Section 10.
(2) The two SOT-23 packages are identical in size, but the SOT-23-THIN package is thinner.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

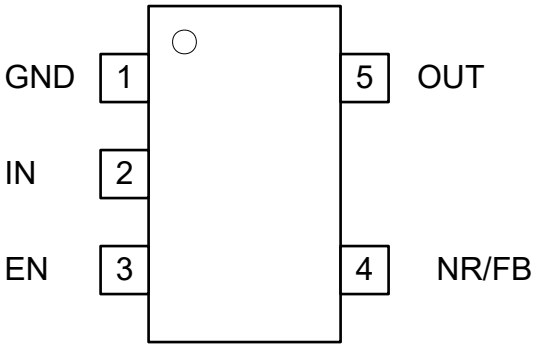


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

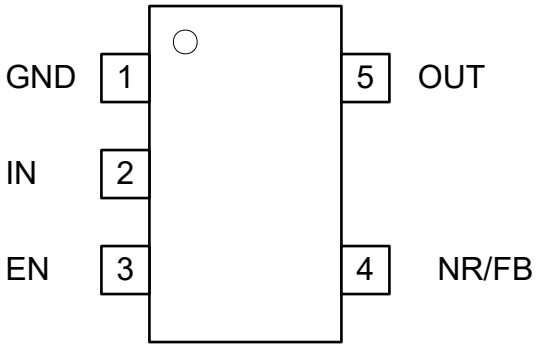


Figure 4-2. DDC Package, 5-Pin SOT-23-THIN (Top View)

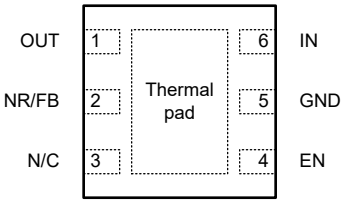


Figure 4-3. DRV Package, 6-Pin WSON (Top View)

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DBV, DDC	DRV		
GND	1	5	—	Ground pin.
IN	2	6	I	Input supply pin. See the Section 5.3 table and the Section 7.1.3 section for more information.
EN	3	4	I	Bipolar enable pin. Driving this pin above the positive enable threshold or below the negative enable threshold turns on the regulator. Driving this pin below the positive disable threshold and above the negative disable threshold puts the regulator into shutdown mode. High and low thresholds are listed in the Section 5.5 table. This pin has a weak internal pulldown and can be left floating to enable. Refer to the Section 6.3.2 (EN) section for more details.
NR	4	2	—	Fixed voltage versions only. Connecting an external capacitor between this pin and ground, bypasses noise generated by the internal band gap. This configuration allows output noise to be reduced to very low levels. The capacitor on NR pin also helps in controlling the inrush current by introducing RC delay during start-up. Refer to the Section 6.3.7 section for more details.
FB	4	2	I	When using the adjustable device, this pin sets the output voltage with the help of a feedback divider. This functionality is only available in the adjustable configuration, and the pin must be connected through a resistor divider to the output for the device to function.
OUT	5	1	O	Output of the regulator. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the Section 5.3 table and the Section 7.1.3 section. Place the output capacitor as close to output of the device as possible.
N/C	—	3	—	Not internally connected. Leave this pin open or connected to any potential. Tie this pin to ground for improved thermal performance.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	IN	Input supply voltage range	–11	0.3	V
	EN	Enable voltage range	$-V_{IN}$	5.5	
	OUT	Output voltage range	–11	0.3	
	NR	NR voltage range (legacy chip)	–11	5.5	
		NR voltage range (new chip)	–6	0.3	
Current		OUT	Internally limited		A
Output short-circuit duration			Indefinite		
Continuous total power dissipation			See Thermal Information table		
T_J		Operating junction temperature	–65	150	°C
T_{stg}		Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE (New chip)	VALUE (Legacy chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	–10		–2.7	V
V_{OUT}	Output voltage range	–10		–1.186	
V_{EN}	Enable voltage range	–10		5.0	
I_{OUT}	Output current	0		200	mA
C_{IN} (1)	Input capacitor (legacy chip)	0.1		2.2	µF
	Input capacitor (new chip)		0.47		
C_{OUT} (2)	Output capacitor	2.2		100	
C_{NR}	NR capacitor		0.01		
C_{FF} (3)	Feed-forward capacitor (for adjustable, new chip only)		0.01		
C_{OUT} ESR	Output capacitor ESR (for new chip)			0.5	Ω
T_J	Operating junction temperature	–40		125	°C

(1) An input capacitor is not required for LDO stability. However, an input capacitance with an effective value of 0.1µF minimum is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(2) All capacitor values listed are the nominal value and the effective capacitance is assumed to derate to 50% of the nominal capacitor value.

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(3) The C_{FF} capacitor improves transient, noise, and PSRR performance, but is not required for regulator stability. Using a higher capacitance CFF is permissible but start-up time increases.

5.4 Thermal Information

THERMAL METRIC(1)		TPS723				UNIT
		DBV (SOT23) [Legacy chip]	DBV (SOT23) [New chip]	DDC (SOT23–THIN) [Legacy chip]	DRV (WSON) [Legacy chip]	
		5 PINS	5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.9	153.7	194.8	85.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.5	73.4	41.4	83.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.9	34.8	35.9	47.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.3	7.6	1.0	3.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	35.0	34.5	35.7	47.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	31.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = – 2.7V or V_{IN} = $V_{OUT(nom)}$ – 0.5V (whichever is lower), I_{OUT} = 1mA, V_{EN} = +1.5V, C_{OUT} = 1µF, and C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range			–10		–2.7	V
V_{FB}	Feedback reference voltage (TPS72301)	Legacy chip	T_J = 25°C	–1.210	–1.186	–1.162	V
	Feedback reference voltage (TPS72301)	New chip		–1.1883	–1.186	–1.1836	
V_O	Output voltage range (TPS72301)			–10 + V_{DO}		V_{FB}	V
V_O	Nominal	Legacy chip (TPS723)	T_J = 25°C	–1		1	%
	Accuracy (fixed output)		–10V ≤ V_I ≤ V_O – 0.5V, 10µA ≤ I_O ≤ 200mA	–2	±1	2	
	Accuracy (adjustable output)			–3	±1	3	
	Accuracy (both fixed , adjustable)	New chip (TPS723)	–10V ≤ V_I ≤ V_O – 0.5V, 10µA ≤ I_O ≤ 200mA	–1.6	±0.04	1.6	
$\Delta V_O(\Delta V_I)$	Line regulation	Legacy chip	–10V ≤ V_I ≤ $V_{O(nom)}$ – 0.5V		0.04		%/V
		New chip			–0.003		
$\Delta V_O(\Delta I_O)$	Load regulation	Legacy chip	0mA ≤ I_O ≤ 200mA		0.002		%/mA
		New chip			0.0001		
V_{DO}	Dropout voltage	Legacy chip	I_O = 200mA, V_O = 0.96 × $V_{O(NOM)}$		280	500	mV
		New chip			140	245	
V_{UVLO+}	Rising input supply UVLO	New chip		–2.4	–2.1		V
V_{UVLO-}	Falling input supply UVLO	New chip			–1.9	–1.4	V
I_{LIM}	Output current limit	Legacy chip	V_O = 0.85 × $V_{O(NOM)}$	300	550	800	mA
		New chip	V_O = 0.85 × $V_{O(NOM)}$	300	385	485	

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5.5 Electrical Characteristics (continued)

Over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = – 2.7V or V_{IN} = $V_{OUT(nom)}$ – 0.5V (whichever is lower), I_{OUT} = 1mA, V_{EN} = +1.5V, C_{OUT} = 1µF, and C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GND}	Ground pin current	Legacy chip	I_O = 0 mA (I_Q), –10V ≤ V_I ≤ V_O – 0.5V		130	200	µA
			I_O = 200 mA, –10V ≤ V_I ≤ V_O – 0.5V		350	500	
		New chip	I_O = 0 mA (I_Q), –10V ≤ V_I ≤ V_O – 0.5V		30.0	55	
			I_O = 200 mA , –10V ≤ V_I ≤ V_O – 0.5V		290	450	
I_{SHDN}	Shutdown ground pin current	Legacy chip	– 0.4V ≤ V_{EN} ≤ 0.4V, –10V ≤ V_I ≤ V_O – 0.5V		0.1	2.0	µA
		New chip	– 0.4V ≤ V_{EN} ≤ 0.4V, –10V ≤ V_I ≤ V_O – 0.5V		0.7	2.0	
I_{FB}	Feedback pin current	Legacy chip	–10V ≤ V_I ≤ V_O – 0.5V		0.05	1.0	µA
		New chip			0.001	0.1	
I_{EN}	EN pin current	Legacy chip	–10V ≤ V_I ≤ V_O – 0.5V, –10V ≤ V_{EN} ≤ ±3.5V		0.1	2.0	
		New chip			0.6	2.0	
$V_{EN(HI)}$	Enable threshold (positive)	Legacy chip		1.5			V
$V_{EN(LO)}$	Enable threshold (negative)					– 1.5	V
$V_{DIS(HI)}$	Disable threshold (positive)					0.4	V
$V_{DIS(LO)}$	Disable threshold (negative)			– 0.4			V
$V_{EN(HI)}$	Enable threshold (positive)	New chip		1.5			V
$V_{EN(LO)}$	Enable threshold (negative)					– 1.5	V
$V_{DIS(HI)}$	Disable threshold (positive)					0.4	V
$V_{DIS(LO)}$	Disable threshold (negative)			– 0.4			V
T_{sd+}	Thermal shutdown temperature	Legacy chip	Shutdown, temperature increasing		165		°C
T_{sd-}			Reset, temperature decreasing		145		°C
T_{sd+}		New chip	Shutdown, temperature increasing		175		°C
T_{sd-}			Reset, temperature decreasing		155		°C
PSRR	Power-supply ripple rejection		I_O = 200mA, 1kHz, C_I = C_O = 10µF		65		dB
			I_O = 200mA, 10kHz, C_I = C_O = 10µF		48		
V_n	Output noise voltage		Bandwidth = 10Hz to 100kHz, V_O = 2.5V, I_O = 200mA, $C_{NR/SS}$ = 0.01µF, C_O = 1µF		60		μ_{VRMS}
t_{STR}	Start-up time	Legacy chip	V_O = –2.5V, C_O = 1µF, R_L = 25Ω		1		ms
t_{STR}	Start-up time	New chip	V_O = –2.5V, C_O = 1µF, R_L = 25Ω		8		ms

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5.6 Typical Characteristics

at $V_{IN} = V_{OUT(NOM)} – 0.5V$, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

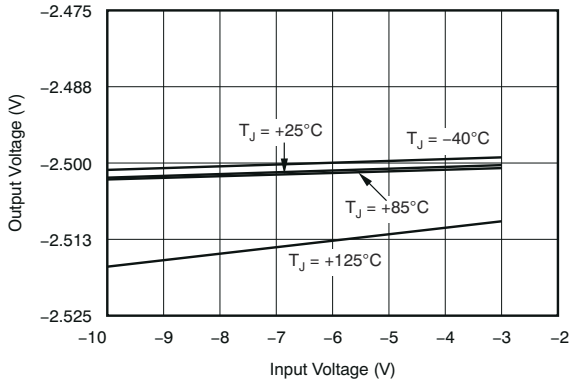


Figure 5-1. Output Voltage vs Input Voltage (legacy chip)

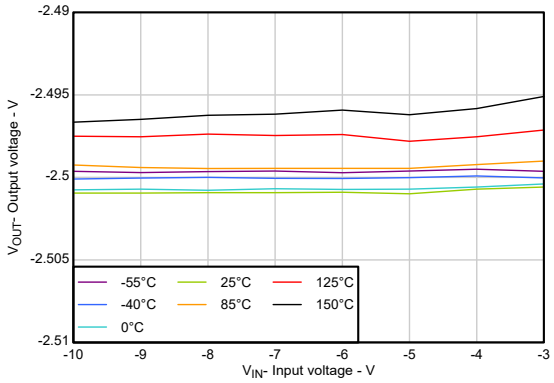


Figure 5-2. Output Voltage vs Input Voltage (new chip)

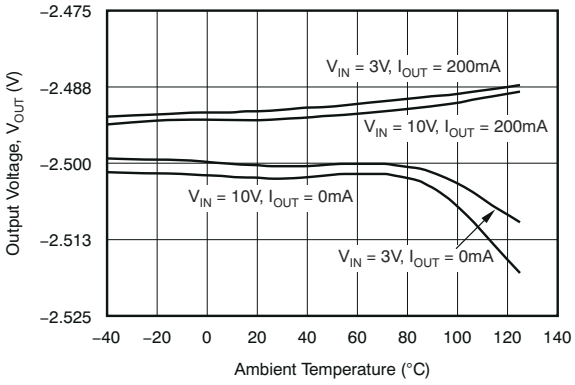


Figure 5-3. Output Voltage vs Ambient Temperature (legacy chip)

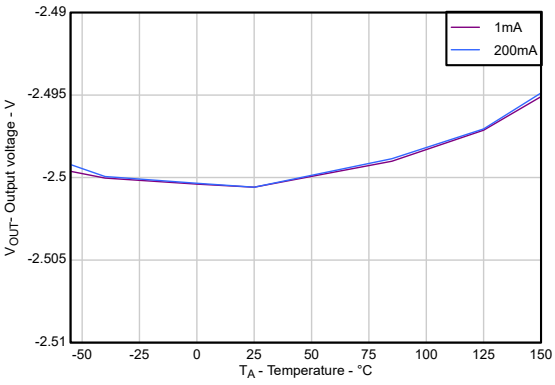


Figure 5-4. Output Voltage vs Ambient Temperature (new chip)

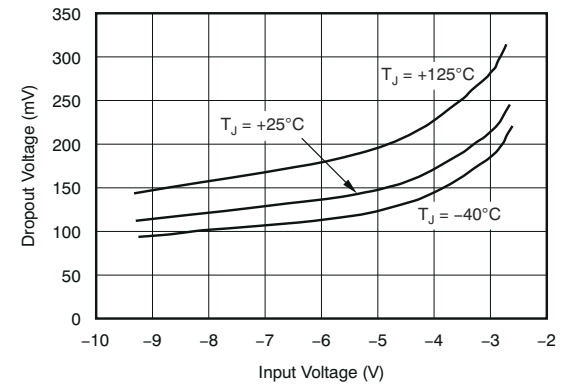


Figure 5-5. TPS72301 Dropout Voltage vs Input Voltage (legacy chip)

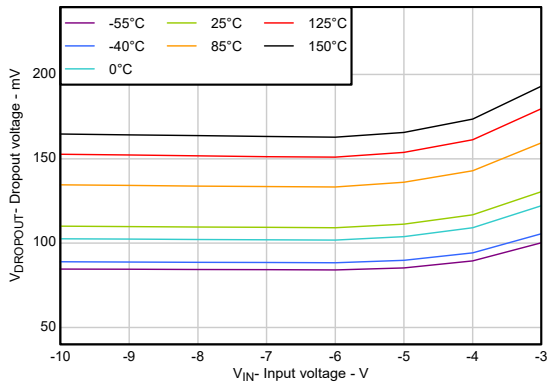


Figure 5-6. TPS72301 Dropout Voltage vs Input Voltage (new chip)

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5.6 Typical Characteristics (continued)

at $V_{IN} = V_{OUT(NOM)} – 0.5V$, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

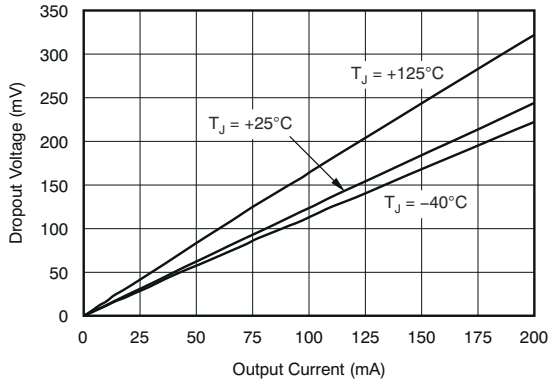


Figure 5-7. Dropout Voltage vs Output Current (legacy chip)

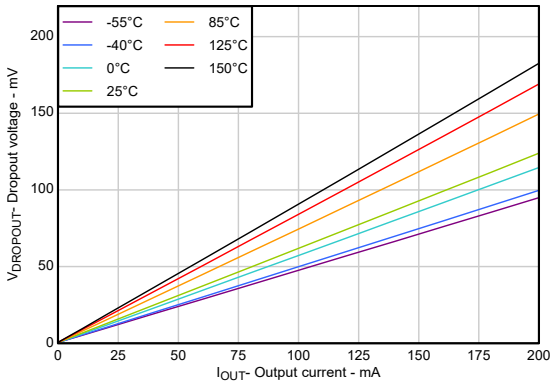


Figure 5-8. Dropout Voltage vs Output Current (new chip)

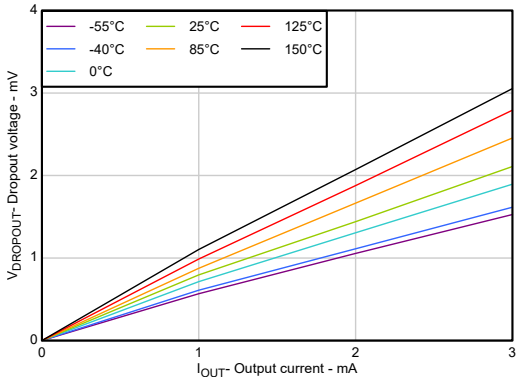


Figure 5-9. Dropout Voltage vs Output Current (light loads, new chip)

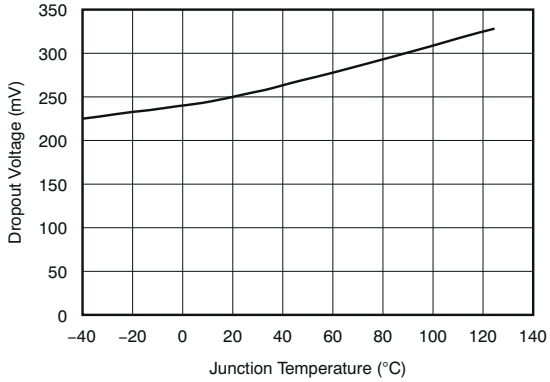


Figure 5-10. TPS72325 Dropout Voltage vs Junction Temperature (legacy chip)

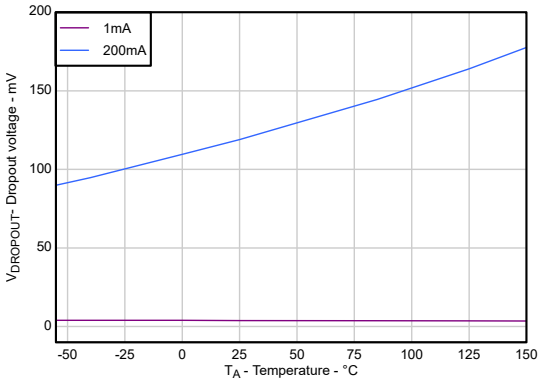


Figure 5-11. TPS72325 Dropout Voltage vs Junction Temperature (new chip)

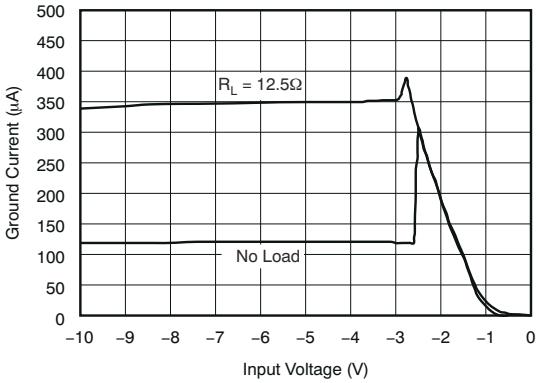


Figure 5-12. Ground Current vs Input Voltage (legacy chip)

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5.6 Typical Characteristics (continued)

at $V_{IN} = V_{OUT(NOM)} – 0.5V$, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

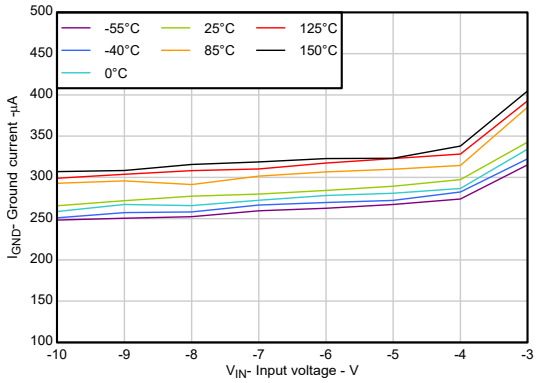


Figure 5-13. Ground Current vs Input Voltage (new chip)

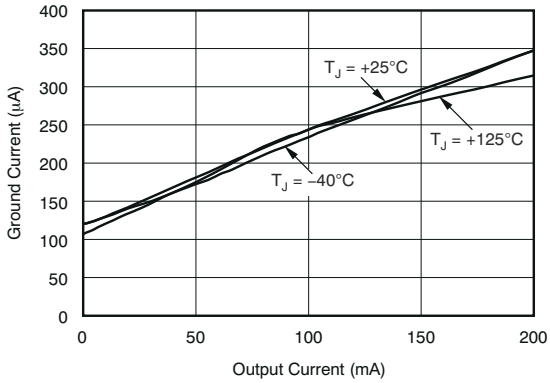


Figure 5-14. Ground Current vs Output Current (legacy chip)

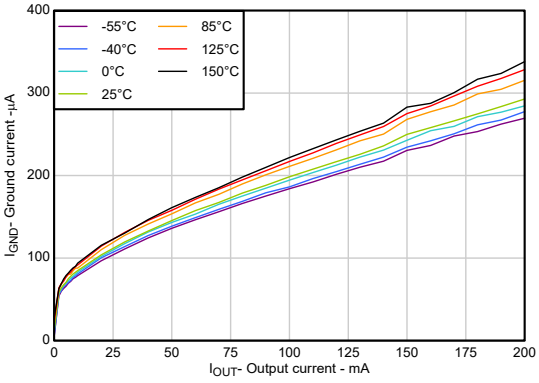


Figure 5-15. Ground Current vs Output Current (new chip)

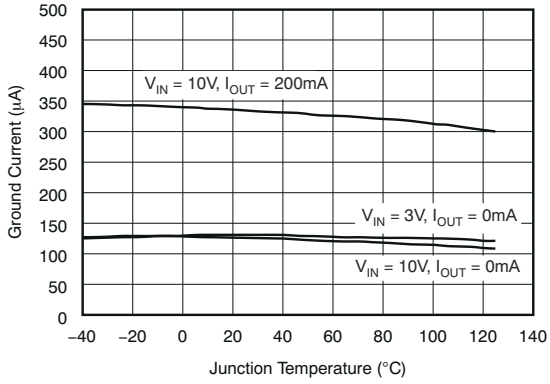


Figure 5-16. Ground Current vs Junction Temperature (legacy chip)

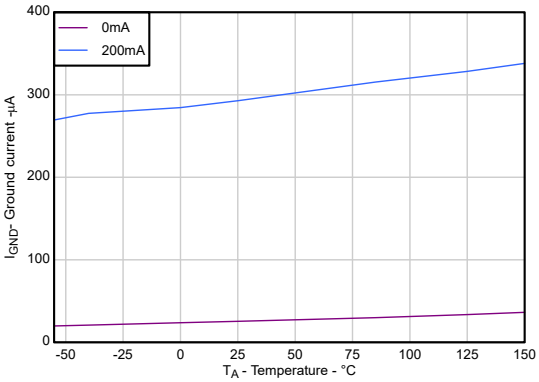


Figure 5-17. Ground Current vs Junction Temperature (new chip)

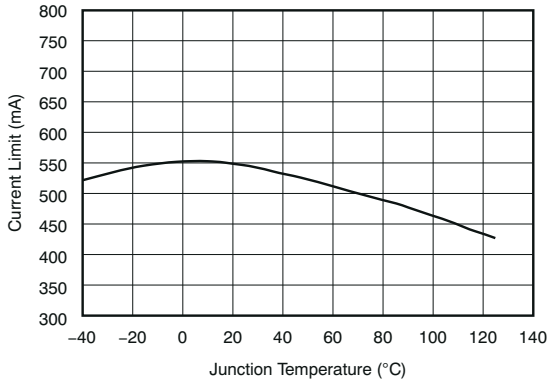


Figure 5-18. TPS72325 Current Limit vs Junction Temperature (legacy chip)

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5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

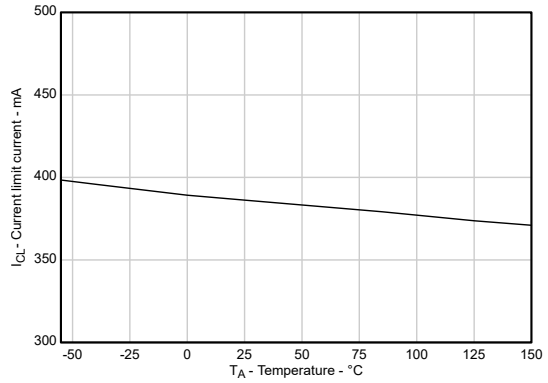


Figure 5-19. TPS72325 Current Limit vs Junction Temperature (new chip)

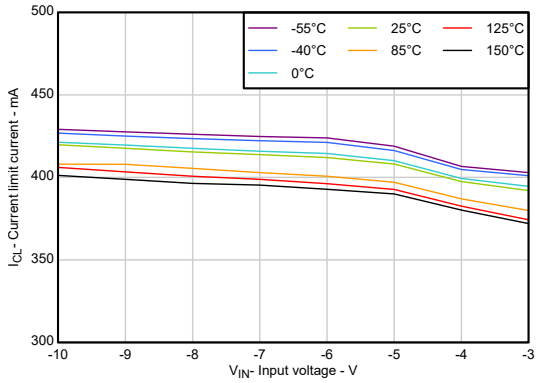


Figure 5-20. TPS72325 Current Limit vs V_{IN} (new chip)

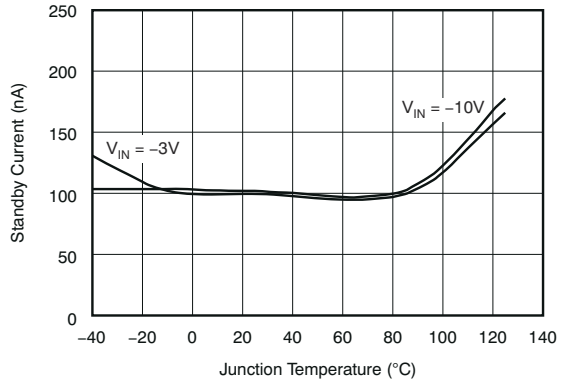


Figure 5-21. Standby Current vs Junction Temperature (legacy chip)

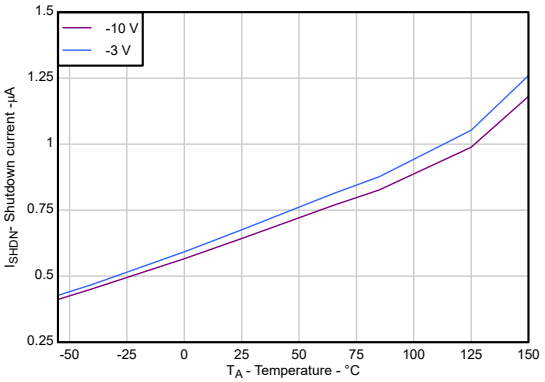


Figure 5-22. Standby Current vs Junction Temperature (new chip)

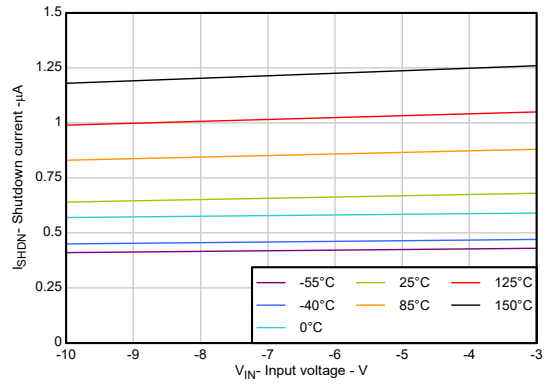


Figure 5-23. Standby Current vs V_{IN} (new chip)

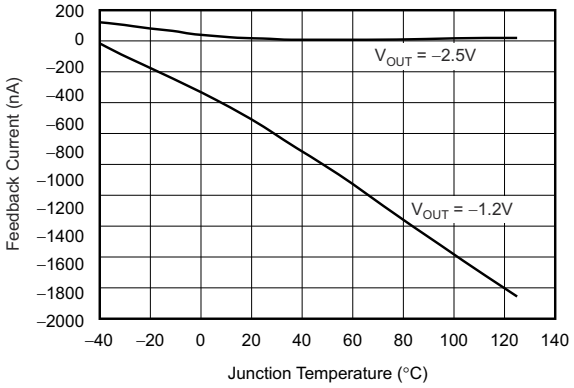


Figure 5-24. TPS72301 Feedback Pin Current vs Junction Temperature (legacy chip)

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5.6 Typical Characteristics (continued)

at $V_{IN} = V_{OUT(NOM)} – 0.5V$, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

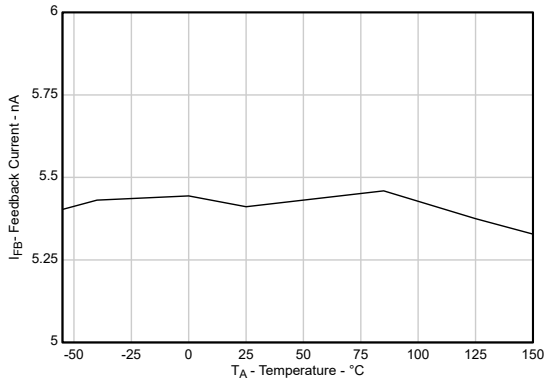


Figure 5-25. TPS72301 Feedback Pin Current vs Junction Temperature (new chip)

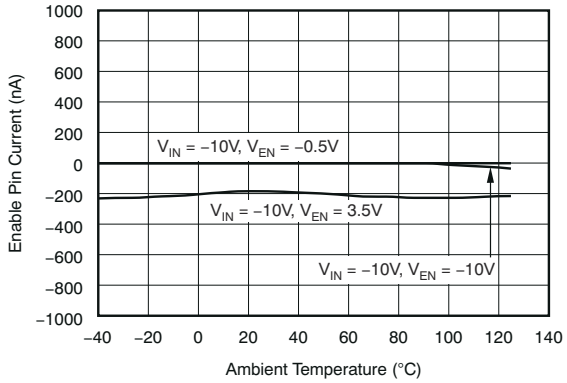


Figure 5-26. Enable Pin Current vs Junction Temperature (legacy chip)

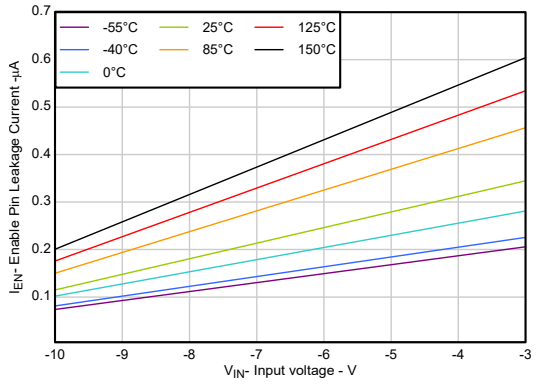


Figure 5-27. Enable Pin Current vs Junction Temperature (new chip)

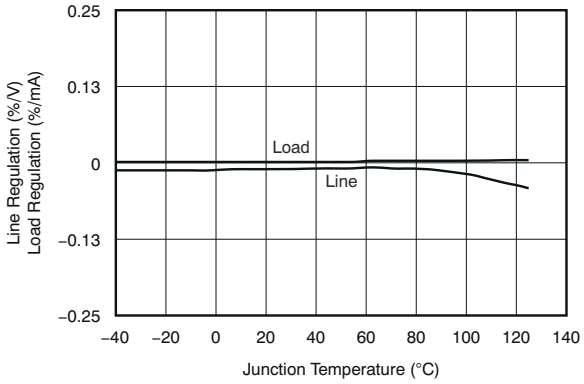


Figure 5-28. Line And Load Regulation vs Junction Temperature (legacy chip)

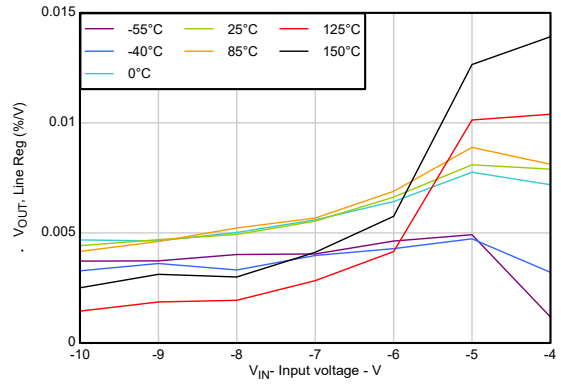


Figure 5-29. Line Regulation vs Junction Temperature (new chip)

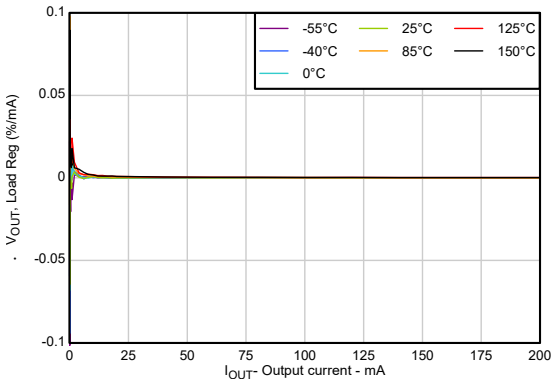


Figure 5-30. Load Regulation vs Junction Temperature (new chip)

5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

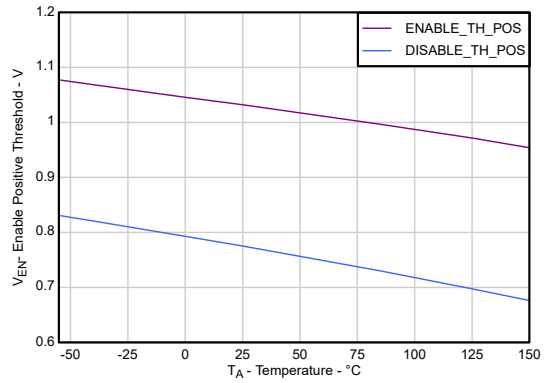


Figure 5-31. EN Thresholds (Positive) vs Junction Temperature (new chip)

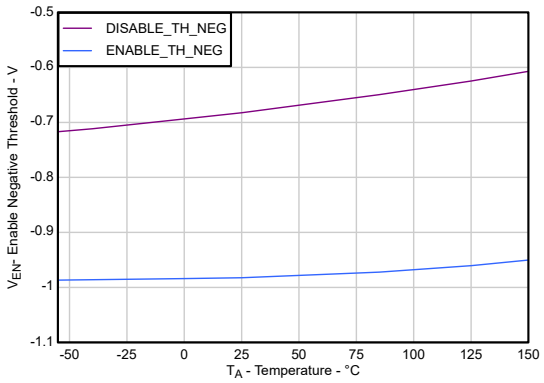


Figure 5-32. EN Thresholds (Negative) vs Junction Temperature (new chip)

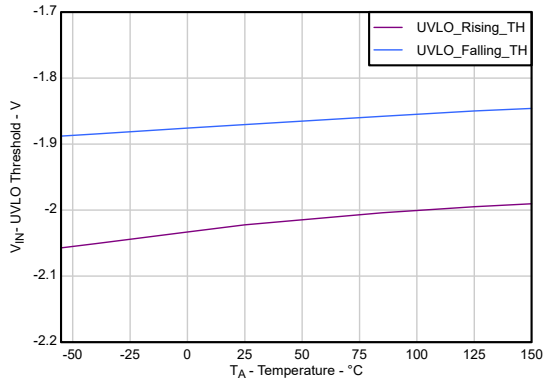


Figure 5-33. UVLO vs Junction Temperature (new chip)

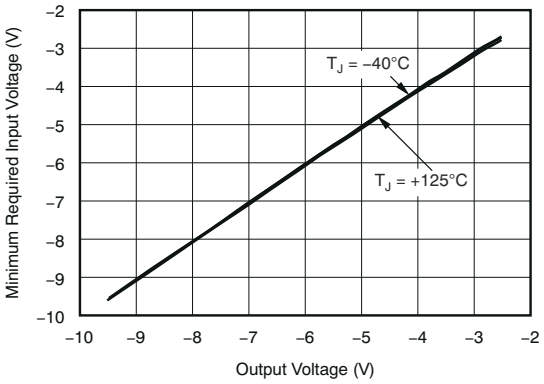


Figure 5-34. TPS72301 Minimum Required Input Voltage vs Output Voltage (legacy chip)

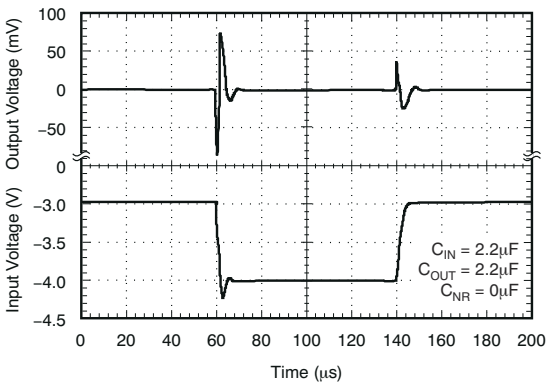
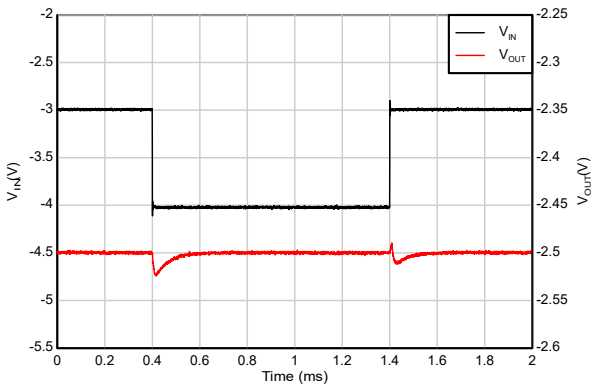


Figure 5-35. TPS72325 Line Transient Response (legacy chip)



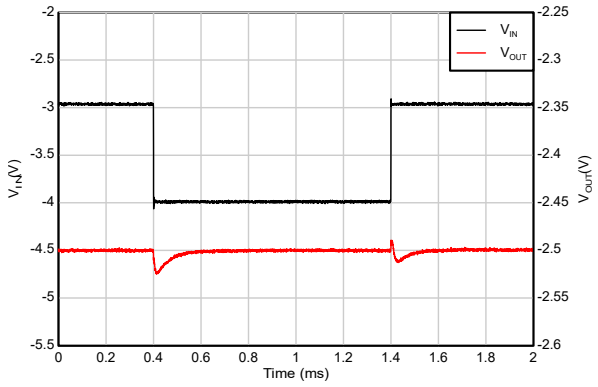
V_{IN} = -3V to -4V with dV_{IN}/dt = 1V/µs, I_{OUT} = 1mA

Figure 5-36. TPS72325 Line Transient Response (new chip)

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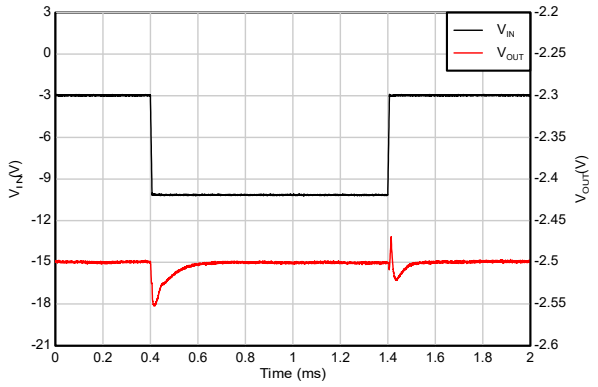
5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)



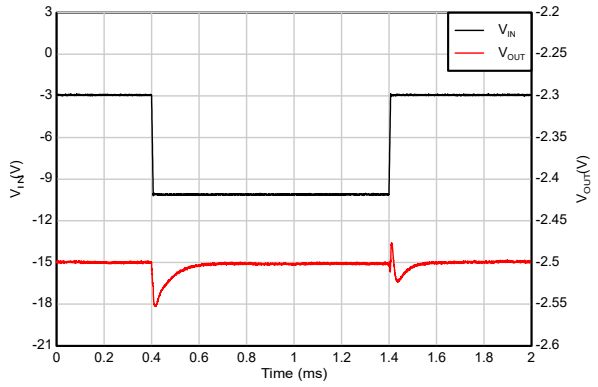
V_{IN} = -3V to -4V with dV_{IN}/dt = 1V/µs, I_{OUT} = 200mA

Figure 5-37. TPS72325 Line Transient Response (new chip)



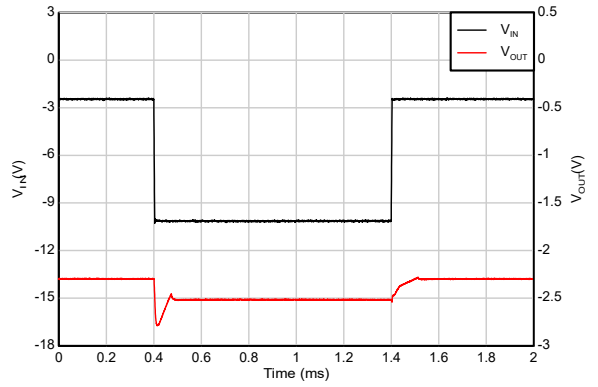
V_{IN} = -3V to -10V with dV_{IN}/dt = 1V/µs, I_{OUT} = 1mA

Figure 5-38. TPS72325 Line Transient Response (new chip)



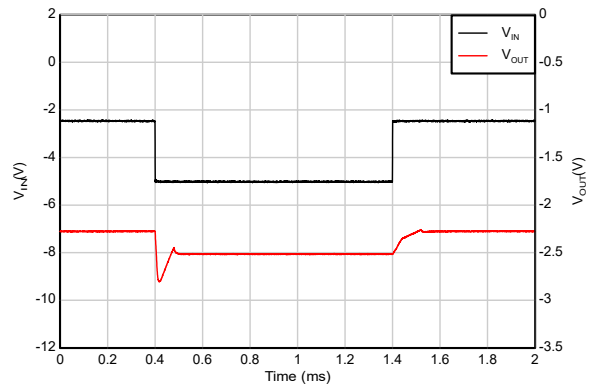
V_{IN} = -3V to -10V with dV_{IN}/dt = 1V/µs, I_{OUT} = 200mA

Figure 5-39. TPS72325 Line Transient Response (new chip)



V_{IN} = -2.5V to -10V with dV_{IN}/dt = 2V/µs, I_{OUT} = 1mA

Figure 5-40. TPS72325 Dropout exit Response (new chip)



V_{IN} = -2.5V to -5.0V with dV_{IN}/dt = 2V/µs, I_{OUT} = 1mA

Figure 5-41. TPS72325 Dropout exit Response (new chip)

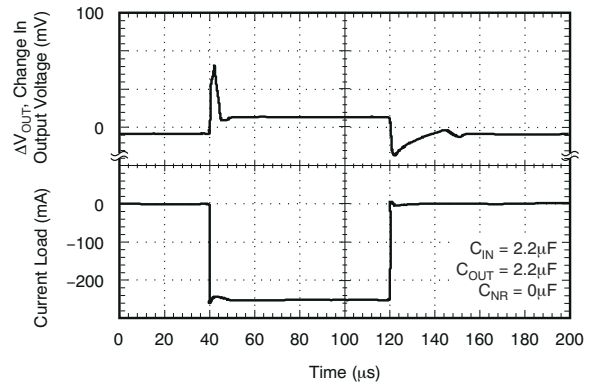


Figure 5-42. TPS72325 Load Transient Response (legacy chip)

5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

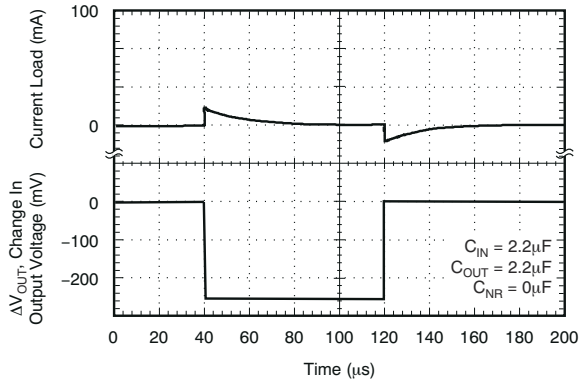
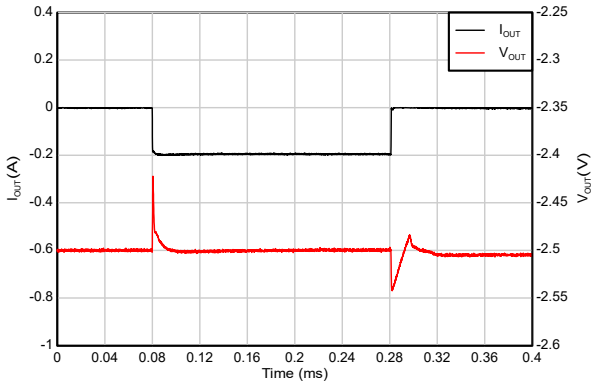
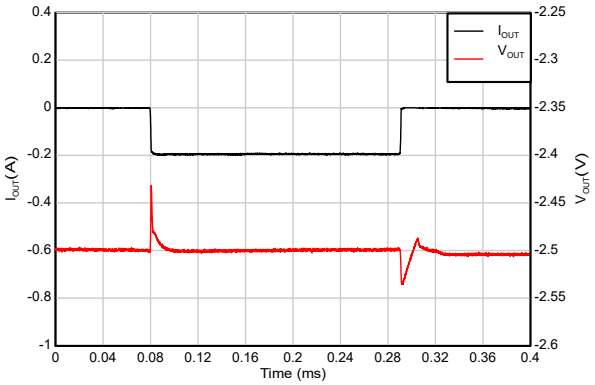


Figure 5-43. TPS72325 Load Transient Response (legacy chip)



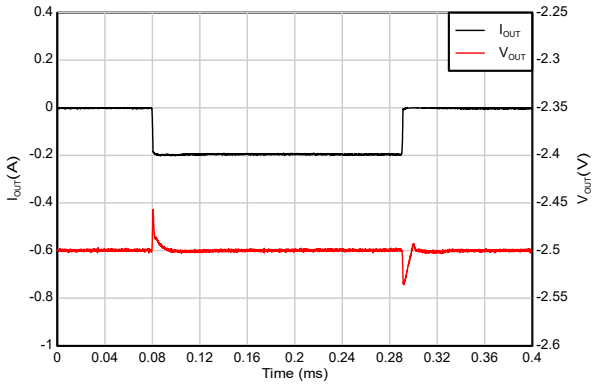
I_{OUT} = 1µA to 200mA with dI_{OUT}/dt = 1A/µs

Figure 5-44. TPS72325 Load Transient Response (new chip)



I_{OUT} = 1µA to 200mA with dI_{OUT}/dt = 0.2A/µs

Figure 5-45. TPS72325 Load Transient Response (new chip)



I_{OUT} = 1mA to 200mA with dI_{OUT}/dt = 0.2A/µs

Figure 5-46. TPS72325 Load Transient Response (new chip)

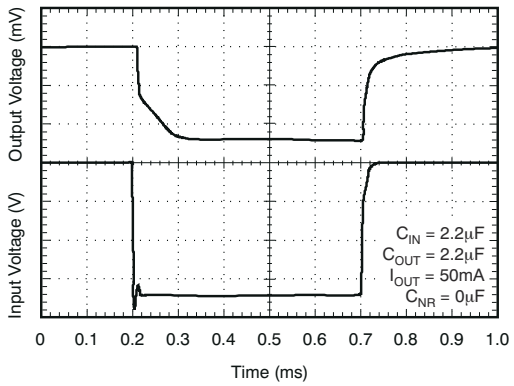


Figure 5-47. TPS72325 Start-Up Response (legacy chip)

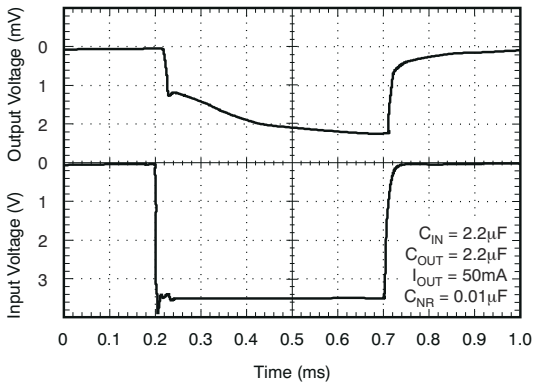


Figure 5-48. TPS72325 Start-Up Response (legacy chip)

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5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

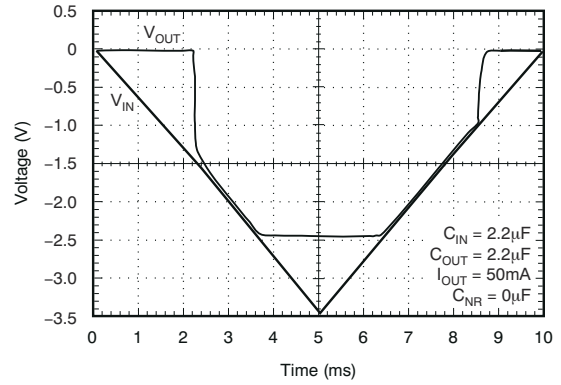
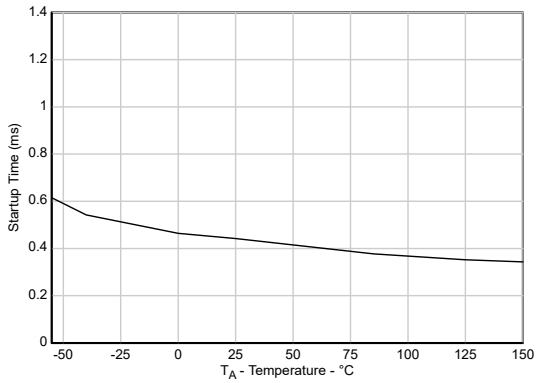
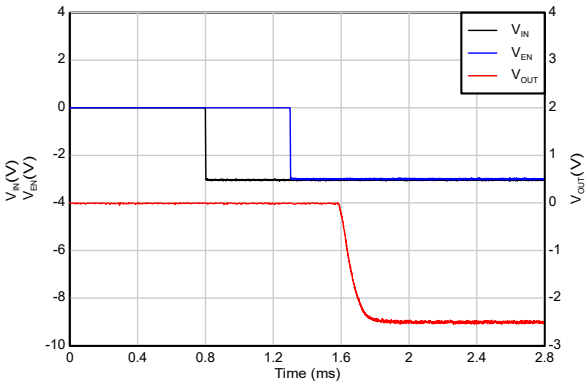


Figure 5-49. TPS72325 Power-Up/Power-Down (legacy chip)



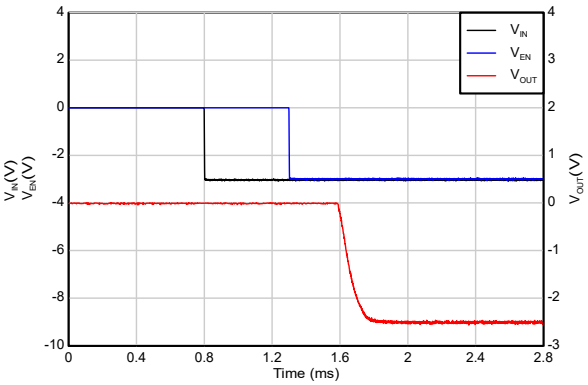
I_{OUT} = 0mA, C_{NR} not conneted.

Figure 5-50. TPS72325 Start-up time vs Temp (new chip)



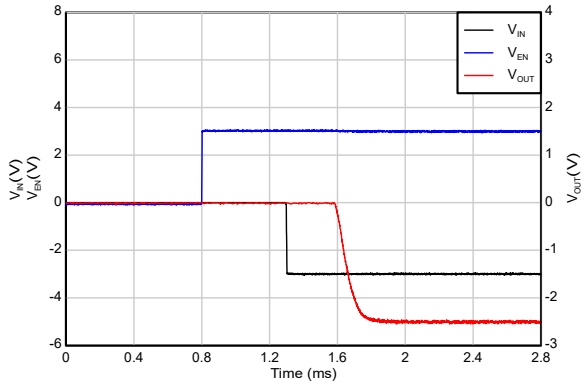
I_{OUT} = 1mA

Figure 5-51. TPS72325 Start-up Response (V_{IN} ramping before EN) (New chip)



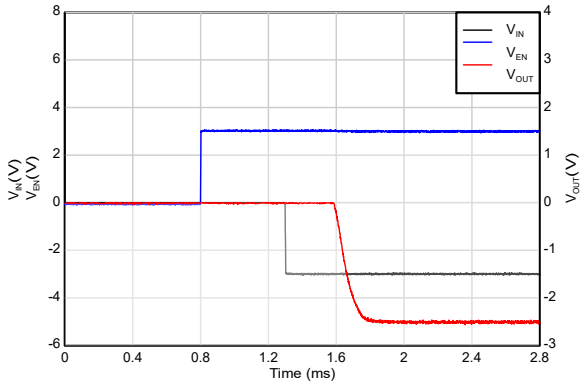
I_{OUT} = 200mA

Figure 5-52. TPS72325 Start-up Response (V_{IN} ramping before EN) (New chip)



I_{OUT} = 1mA

Figure 5-53. TPS72325 Start-up Response (V_{IN} ramping after EN) (New chip)



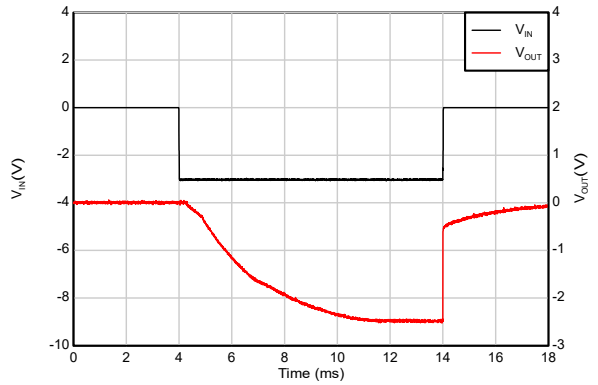
I_{OUT} = 200mA

Figure 5-54. TPS72325 Start-up Response (V_{IN} ramping after EN) (New chip)

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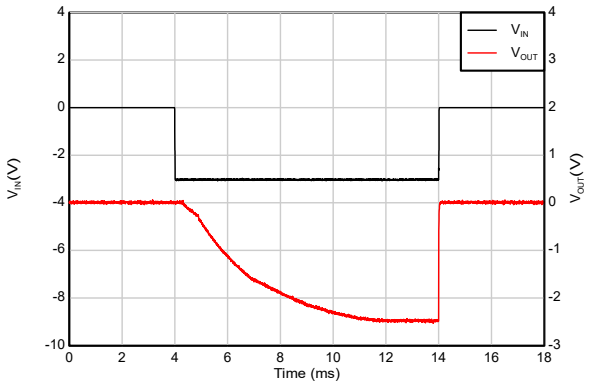
5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)



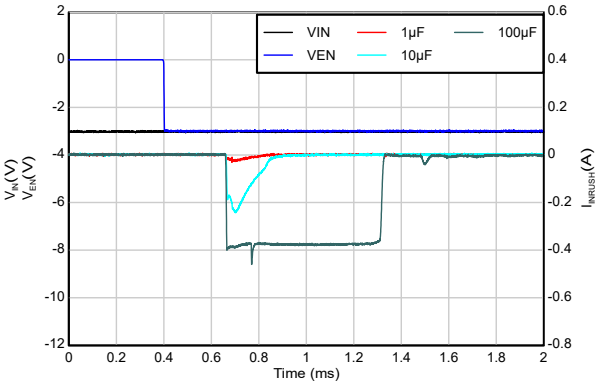
I_{OUT} = 1mA, C_{NR} = 10nF

Figure 5-55. TPS72325 Start-up Response (V_{IN} & EN tied together) (New chip)



I_{OUT} = 200mA, C_{NR} = 10nF

Figure 5-56. TPS72325 Start-up Response (V_{IN} & EN tied together) (New chip)



I_{OUT} = 0mA

Figure 5-57. Start-up inrush current vs C_{OUT} (New chip)

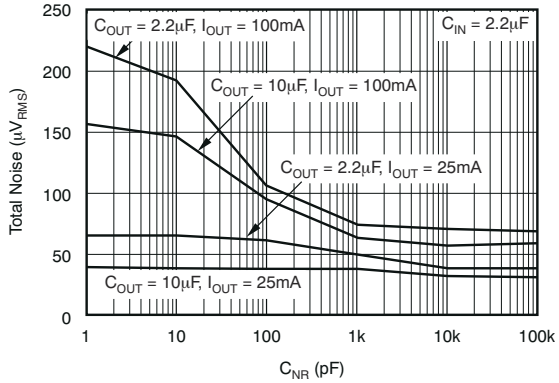
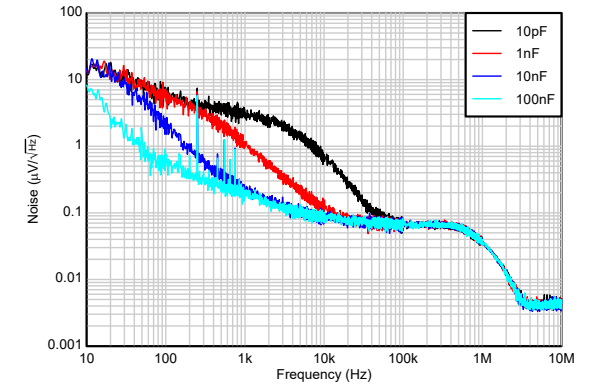
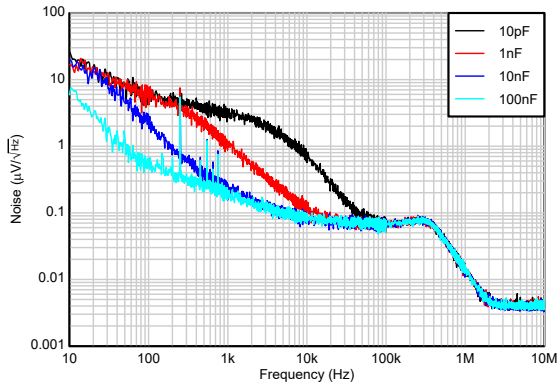


Figure 5-58. TPS72325 Total Noise vs C_{NR} (10Hz to 100kHz) (legacy chip)



I_{OUT} = 200mA

Figure 5-59. TPS72325 Total Noise vs C_{NR} (10Hz to 10MHz) (New chip)



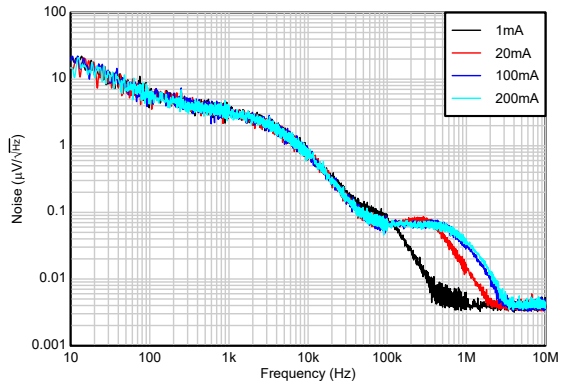
I_{OUT} = 20mA

Figure 5-60. TPS72325 Total Noise vs C_{NR} (10Hz to 10MHz) (New chip)

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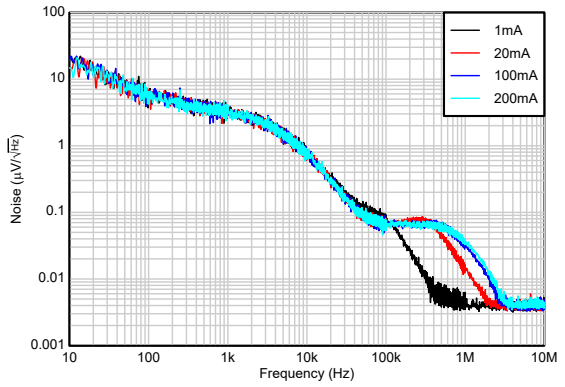
5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)



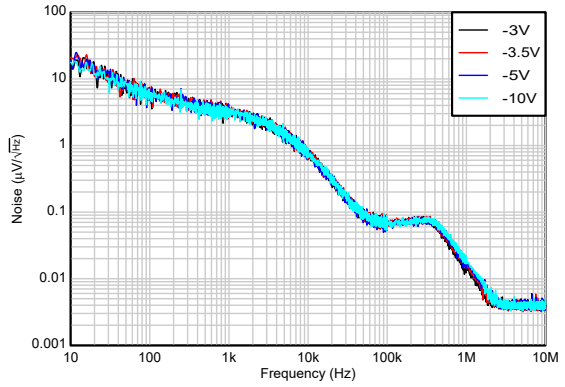
V_{IN} = –3.0V

Figure 5-61. TPS72325 Total Noise vs I_{OUT} (10Hz to 10MHz) (New chip)



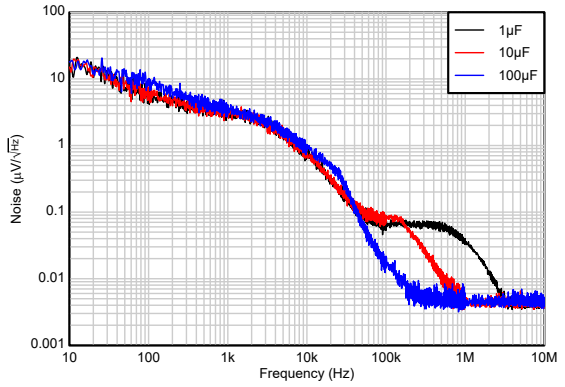
I_{OUT} = 200mA

Figure 5-62. TPS72325 Total Noise vs V_{IN} (10Hz to 10MHz) (New chip)



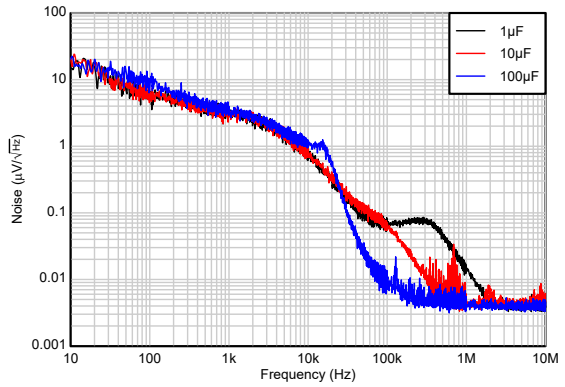
I_{OUT} = 20mA

Figure 5-63. TPS72325 Total Noise vs V_{IN} (10Hz to 10MHz) (New chip)



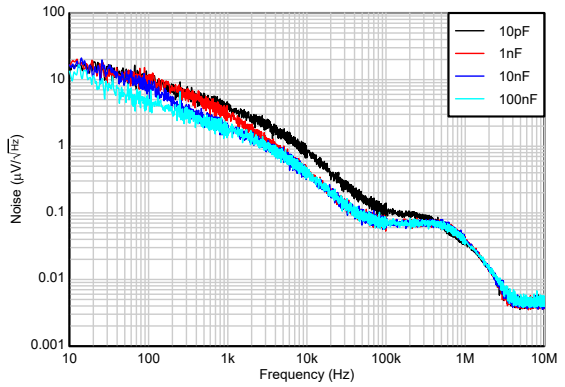
I_{OUT} = 200mA

Figure 5-64. TPS72325 Total Noise vs C_{OUT} (10Hz to 10MHz) (New chip)



I_{OUT} = 20mA

Figure 5-65. TPS72325 Total Noise vs C_{OUT} (10Hz to 10MHz) (New chip)



I_{OUT} = 200mA

Figure 5-66. TPS72301 Total Noise vs C_{FF} (10Hz to 10MHz) (New chip)

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5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)

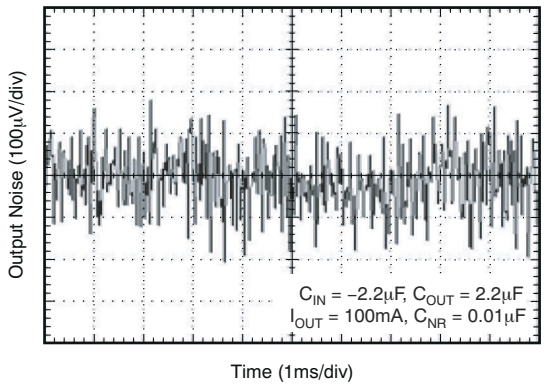


Figure 5-67. TPS72325 Output Noise vs Time (legacy chip)

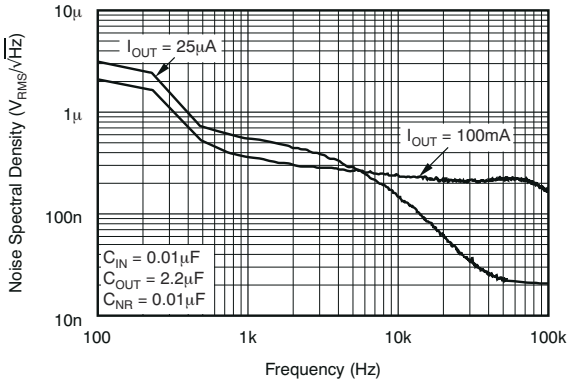


Figure 5-68. TPS72325 Noise Spectral Density vs Frequency (legacy chip)

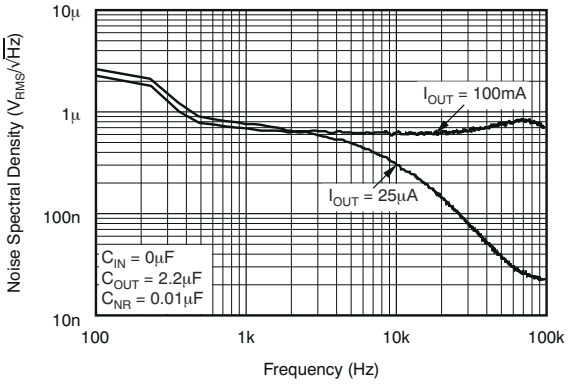


Figure 5-69. TPS72325 Noise Spectral Density vs Frequency (legacy chip)

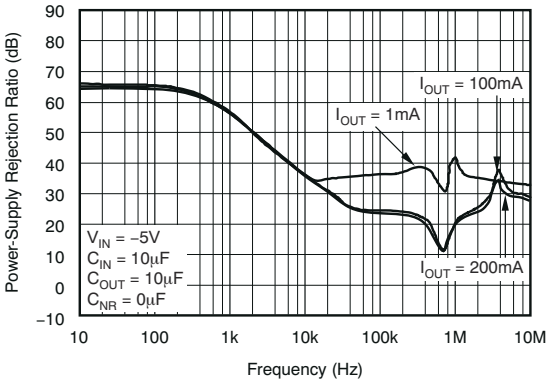


Figure 5-70. PSRR vs Frequency (legacy chip)

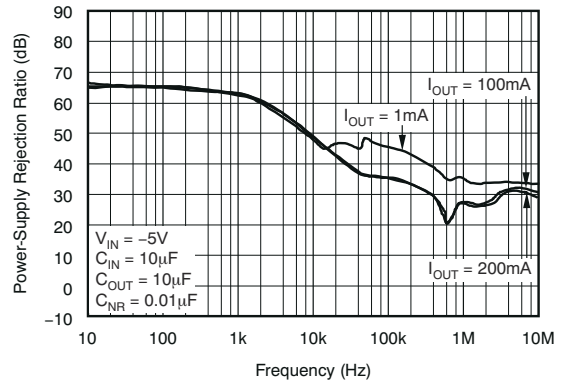


Figure 5-71. PSRR vs Frequency (legacy chip)

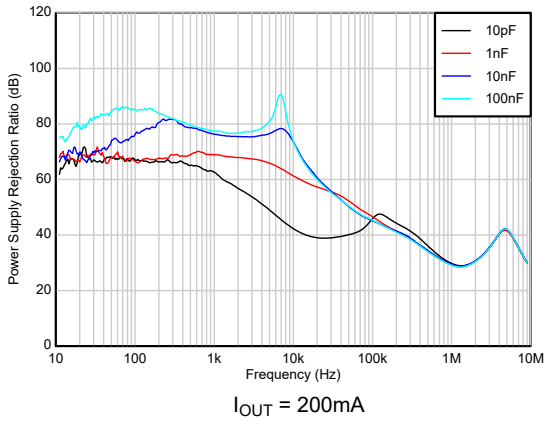
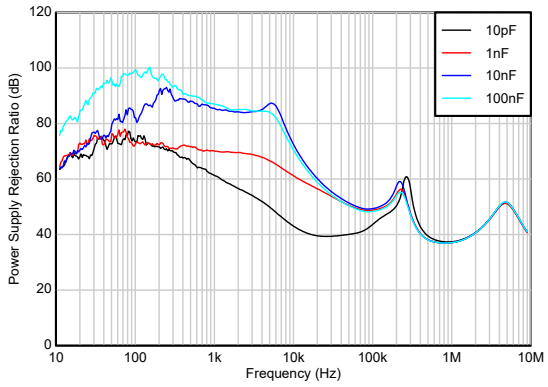


Figure 5-72. PSRR vs C_{NR} (New chip)

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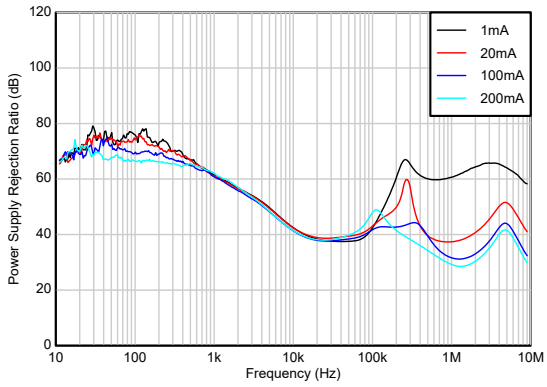
5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)



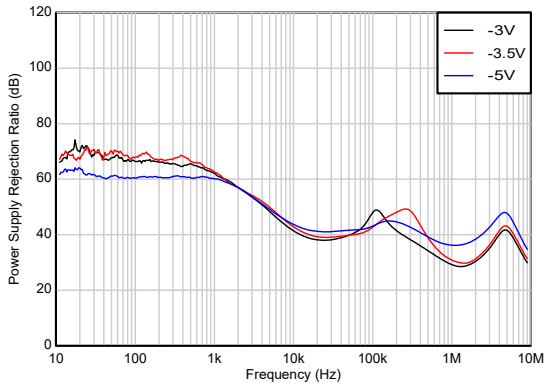
I_{OUT} = 20mA

Figure 5-73. PSRR vs C_{NR} (New chip)



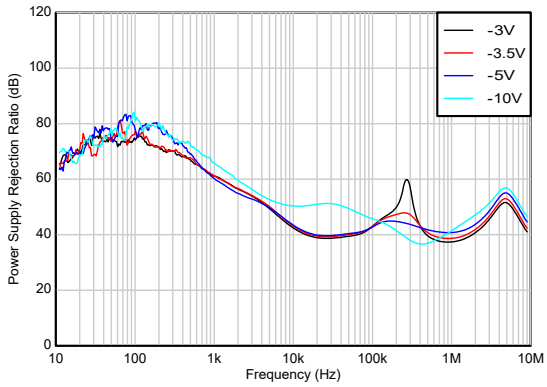
V_{IN} = –3.0V

Figure 5-74. PSRR vs I_{OUT} (New chip)



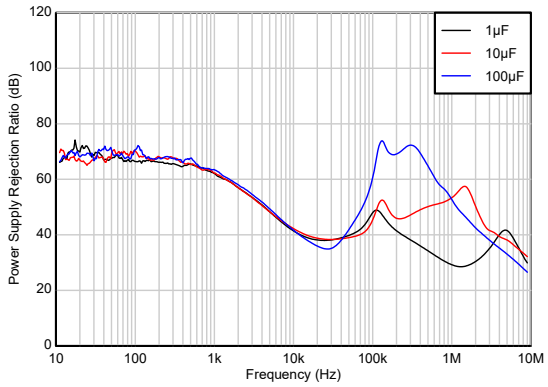
I_{OUT} = 200mA

Figure 5-75. PSRR vs V_{IN} (New chip)



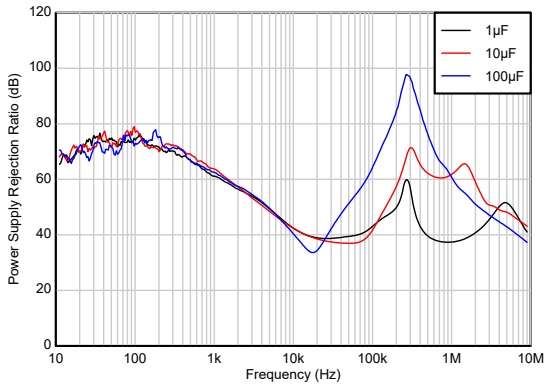
I_{OUT} = 20mA

Figure 5-76. PSRR vs V_{IN} (New chip)



I_{OUT} = 200mA

Figure 5-77. PSRR vs C_{OUT} (New chip)



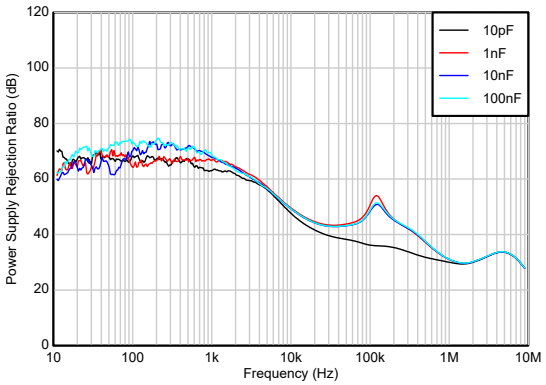
I_{OUT} = 20mA

Figure 5-78. PSRR vs C_{OUT} (New chip)

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5.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ – 0.5V, V_{OUT} = -2.5V, = I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF (unless otherwise noted)



I_{OUT} = 200mA

Figure 5-79. PSRR vs C_{FF} (adjustable only) (New chip)

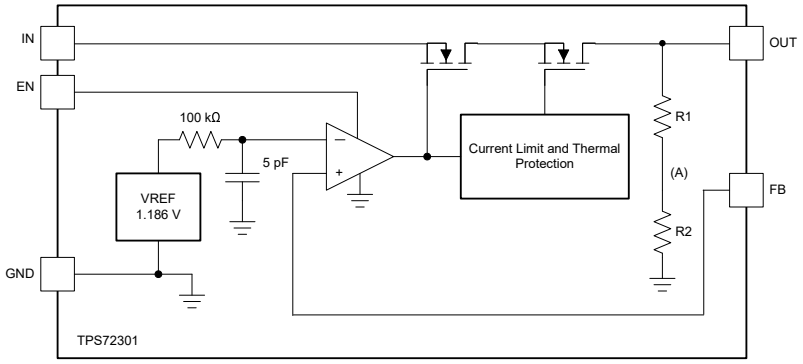
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6 Detailed Description

6.1 Overview

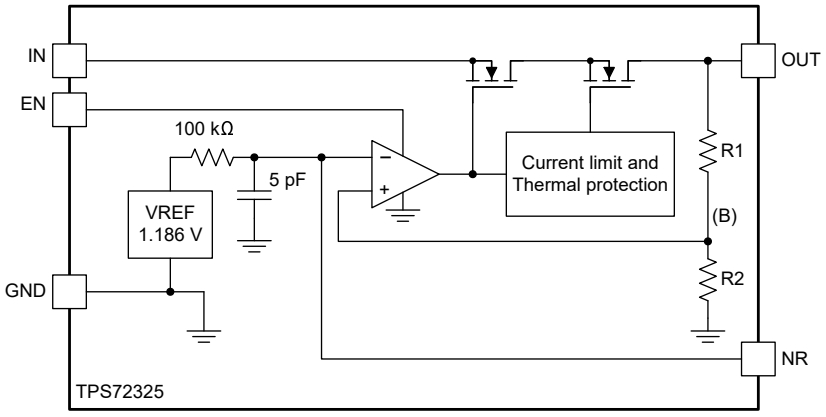
The TPS723 is a low-dropout, negative linear voltage regulator with an output tolerance of ±1.6% across load, and temperature variation (for the new chip) and a rated load current of 200mA. The device is offered in trimmed output voltages between –1.5V and –5.2V and as an adjustable regulator from –1.186V to –10V. The device features very low noise (60 μV_{RMS} with NR cap of 10nF) and high power-supply rejection ratio (40dB typical at 100kHz) , making the TPS723 designed for high-sensitivity analog and RF applications. A shutdown mode is available, reducing ground current to 2-μA maximum over temperature and process.

6.2 Functional Block Diagrams



R1 + R2 = 100kΩ

Figure 6-1. Functional Block Diagram (Adjustable, Legacy Chip)



R1 + R2 = 97kΩ

Figure 6-2. Functional Block Diagram (Fixed, Legacy Chip)

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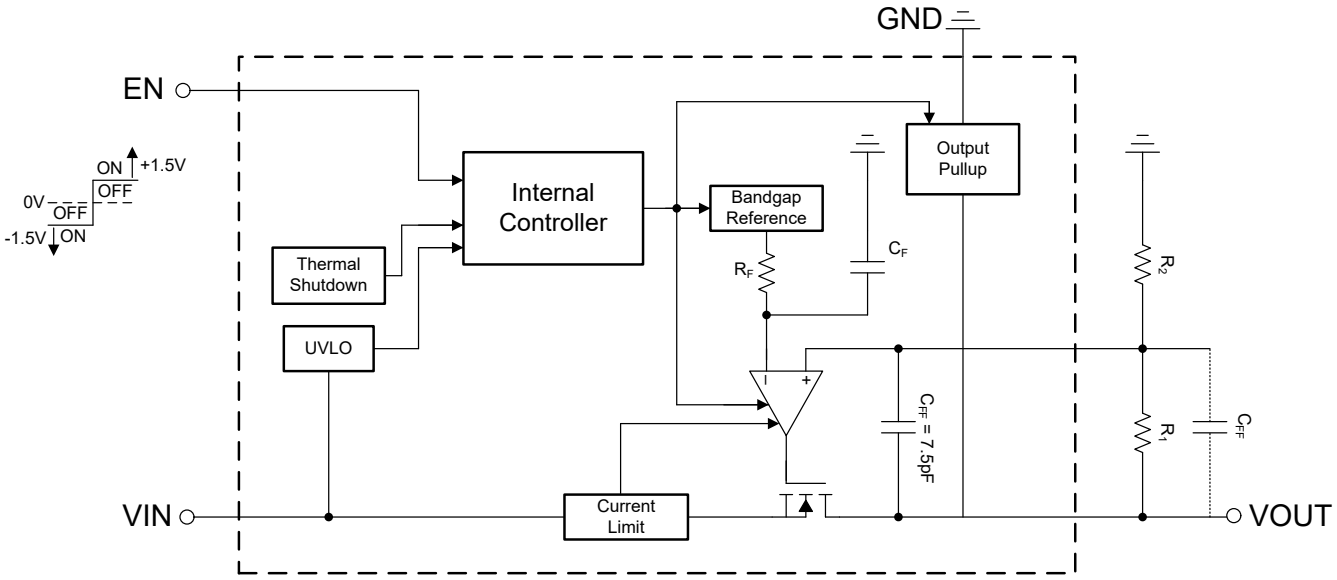


Figure 6-3. Functional Block Diagram (Adjustable, New Chip)

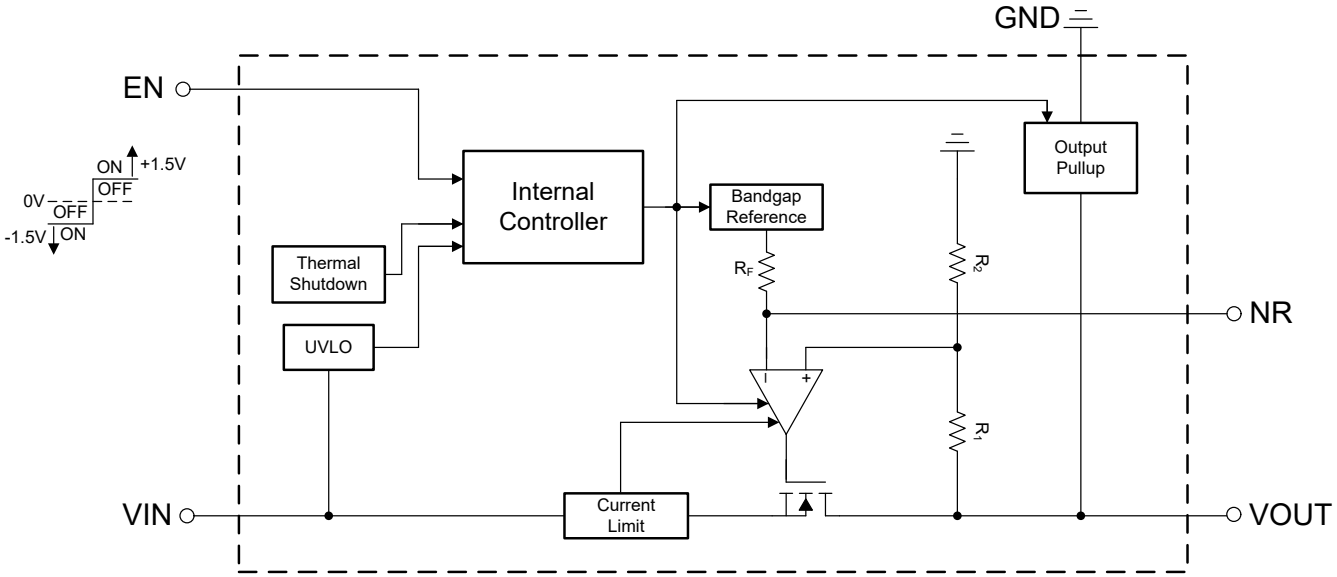


Figure 6-4. Functional Block Diagram (Fixed, New Chip)

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6.3 Feature Description

6.3.1 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table. Also see, Figure 5-18 in the *Typical Characteristics* section.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-5 shows a diagram of the current limit.

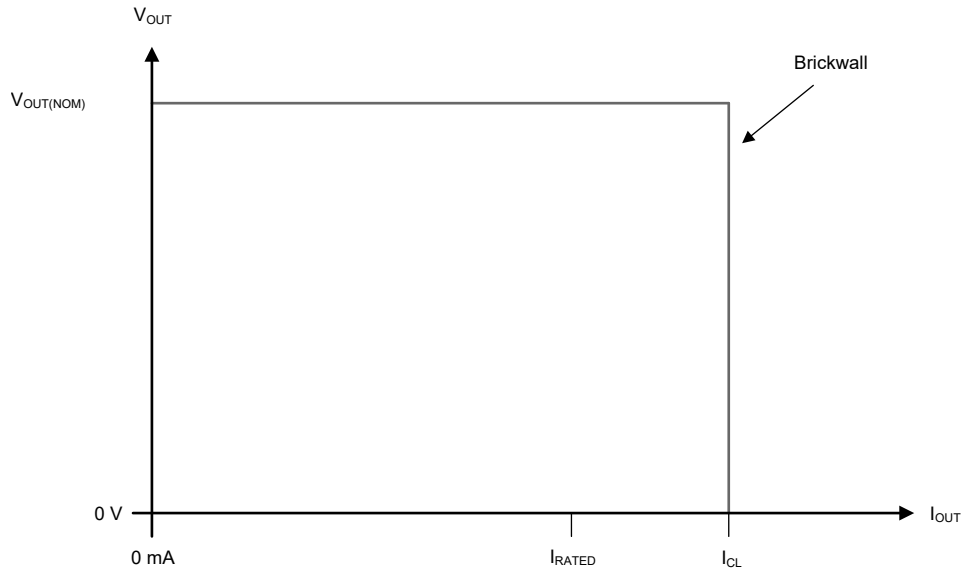


Figure 6-5. Current Limit

Do not drive the output less than 0.3V below the input. An output voltage less than 0.3V below the input voltage biases the body diode in the pass transistor, and allows current to flow from the input to the output. This current is not limited by the device. If this condition is expected, make sure to externally limit the reverse current. See the Reverse Current section for more details.

6.3.2 Enable

For TPS723, The enable pin (EN) is an active-high pin and supports a bipolar logic. The output is enabled when the voltage applied to EN is greater than $V_{EN(HI)}$ (≥ +1.5V) or is lower than $V_{EN(LO)}$ (≤ -1.5V). The device is disabled when EN is lower than $V_{DIS(HI)}$ (≤ 0.4V) and higher than $V_{DIS(LO)}$ (≥ -0.4V). If external control of the output voltage is not needed, connect EN to IN. When devices is disabled, most internal circuitry is turned off, putting the TPS723 into shutdown mode, drawing 2µA maximum ground current. See the Section 5.5 table for details on the values of $V_{EN(HI)}$, $V_{EN(LO)}$, $V_{DIS(HI)}$, and $V_{DIS(LO)}$.

In new chip only, the EN pin also has a weak internal pulldown functionality toward input supply and the EN pin can be left floating to enable the device. The internal pulldown current on the EN pin is captured in the Section 5.5 table as Enable current. However, care must be taken to verify that when EN is tied toward positive logic, the external logic driver must be able to provide the required pull-down current. The new chip also has an internal pullup circuit that activates when the device is disabled and actively charges the output voltage toward ground.

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6.3.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the output voltage minus the input voltage ($V_{OUT} – V_{IN}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Section 5.3* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a maximum input voltage lower than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage rises to more than the nominal output regulation, then the output voltage rises as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.4 Output Pullup

The new chip has an output pullup circuit. The output pullup activates in the following conditions:

- When the device is disabled ($V_{EN} > V_{DIS(LO)}$ or $V_{EN} < V_{EN(LO)}$)
- If $V_{UVLO} < V_{IN} < -1.0V$

Do not rely on the output pullup circuit for charging a large amount of output capacitance toward ground after the input supply has collapsed because reverse current can flow from the input to the output. This reverse current flow can cause damage to the device. See also *Section 7.1.4*.

6.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{OUT} – V_{IN}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Section 5.3* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.6 Undervoltage Lockout (UVLO)

The new chip has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the Section 5.5 table.

6.3.7 NR and Programmable Soft Start

For TPS723, the NR (noise reduction) capacitor in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and the cutoff frequency can be calculated with Equation 2. The typical value of R_F is 400kΩ (typical). Increasing the C_{NR} capacitor has a greater affect because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, a 10nF (typical) C_{NR} is recommended.

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$$f_{cutoff} = 1/(2 \times \pi \times R_F \times C_{NR}) \quad (2)$$

In a new chip version, this NR capacitor (C_{NR}) also helps in controlling the inrush current by introducing RC delay during start-up on the internal reference (V_{NR}). For any external C_{NR}, approximate start-up time, when the internal reference (V_{NR}) charges to the 90% of the typical value can be calculated with Equation 3.

$$T_{start-up} \approx 2.2 \times \tau = 2.2 \times R_F \times C_{NR} \quad (3)$$

For more information on current limits, see the *How a Noise-reduction Pin Improves System Performance* application note.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Section 5.5* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} < V_{OUT(nom)} - V_{DO}$ and $V_{IN} < V_{IN(max)}$	$V_{EN} > V_{EN(HI)}$ or $V_{EN} < V_{EN(LO)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{OUT(nom)} - V_{DO} < V_{IN} < V_{IN(max)}$	$V_{EN} > V_{EN(HI)}$ or $V_{EN} < V_{EN(LO)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} > V_{UVLO-}$	$V_{EN} < V_{DIS(HI)}$ or $V_{EN} > V_{DIS(LO)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is lower than the nominal output voltage minus the dropout voltage ($V_{OUT(nom)} – V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The EN voltage has previously crossing the $V_{EN(HI)}$ or $V_{EN(LO)}$ threshold voltage and has not yet crossed the disable thresholds ($V_{DIS(HI)}$ or $V_{DIS(LO)}$)

6.4.3 Dropout Operation

If the input voltage is more positive (higher) than the nominal output voltage minus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} > V_{OUT(NOM)} – V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value lower than or equal to the nominal output voltage minus the dropout voltage ($V_{OUT(NOM)} - V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the EN pin either higher than the maximum $V_{DIS(LO)}$ or lower than the minimum $V_{DIS(HI)}$ pin input voltage (see the *Section 5.5* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively charged to ground by an internal discharge circuit from the output to ground.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Adjustable Device Feedback Resistor Selection

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (4)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current (I_{FB}) listed in the *Section 5.5* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (5)$$

7.1.2 Recommended Capacitor Types

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a general rule, expect the effective capacitance to decrease by as much as 50%. For new chip, the input and output capacitors recommended in the *Section 5.3* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.3 Input and Output Capacitor Selection

For new chip: The TPS723 (new chip) requires an output capacitor of 2.2µF or larger (1.0µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.0Ω and 0.5Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor.

For new chip: Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

For legacy chip: Appropriate input and output capacitors should be used for the intended application. The TPS723 (legacy chip) only requires a 2.2-µF ceramic output capacitor to be used for stable operation. Both the capacitor value and equivalent series resistance (ESR) affect stability, output noise, PSRR, and transient response. For typical applications, a 2.2-µF ceramic output capacitor located close to the regulator is sufficient.

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7.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \geq V_{IN}$ - 0.3 V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased below the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-1 shows one approach for protecting the device.

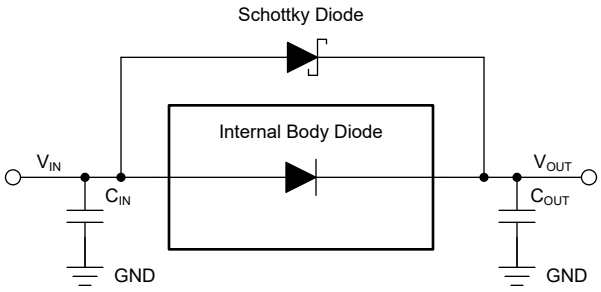


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values (for new chip) are listed in the *Section 5.3* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (6)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (7)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 10µA. Equation 8 calculates the feedback divider current.

$$I_{FB_Divider} = V_{OUT} / (R_1 + R_2) \quad (8)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$µs.

7.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

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$$P_D = (V_{OUT} – V_{IN}) \times I_{OUT} \quad (9)$$

Note

For negative voltage rails, the headroom across the LDO is calculated as V_{OUT} - V_{IN}. Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (10)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the Section 5.4 table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The Section 5.4 table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (11)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (12)$$

where

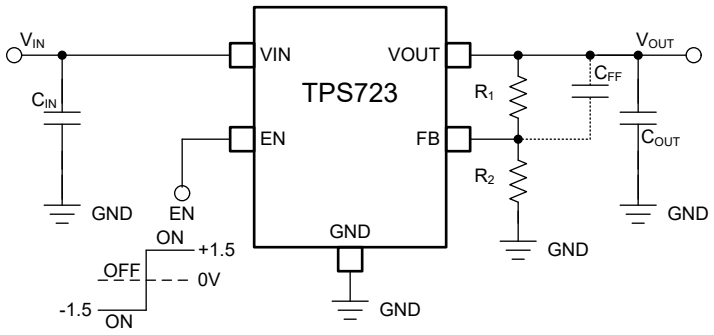
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.2 Typical Application

The TPS72301 allows designers to specify any output voltage from –10V to –1.2V. As shown in the application circuit in Figure 7-2, an external resistor divider is used to scale the output voltage (V_O) to the reference voltage. For best accuracy, use precision resistors for R_1 and R_2. Use the equations in Figure 7-2 to determine the values for the resistor divider.



V_{OUT} = –1.186 × (1 + R_1 / R_2), where R_1 + R_2 ≅ 100kΩ (for legacy chip) and R_2 ≤ 118.6kΩ (for new chip)

Figure 7-2. TPS72301 Adjustable LDO Regulator Programming

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	–10V to –2.7V
Output voltage	–2.5V
Output current	200mA
Output capacitor	2.2µF

7.2.1.1 Capacitor Selection for Stability

Appropriate input and output capacitors must be used for the intended application. The TPS723 only requires a 2.2-µF ceramic output capacitor to be used for stable operation. Both the capacitor value and equivalent series resistance (ESR) affect stability, output noise, PSRR, and transient response. For typical applications, a 2.2-µF ceramic output capacitor located close to the regulator is sufficient.

7.2.1.2 Output Noise

Without external bypassing, output noise of the TPS723 from 10 Hz to 100 kHz is 200 μV_{RMS} typical. The dominant contributor to output noise is the internal band-gap reference. Adding an external 0.01-µF capacitor to ground reduces noise to 60 μV_{RMS}. Best noise performance is achieved using appropriate low ESR capacitors for bypassing noise at the NR and OUT pins. See Figure 5-58 in the *Typical Characteristics* section.

7.2.1.3 Power-Supply Rejection

The TPS723 offers a very high PSRR for applications with noisy input sources or highly sensitive output supply lines. For best PSRR, use high-quality input and output capacitors.

7.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND pin current, and power the load.

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7.2.3 Application Curves

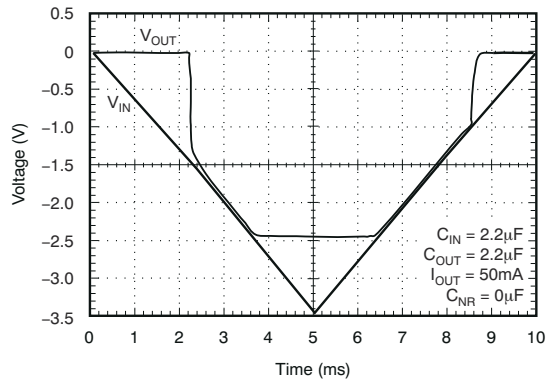


Figure 7-3. TPS72325 Power-Up, Power-Down (legacy chip)

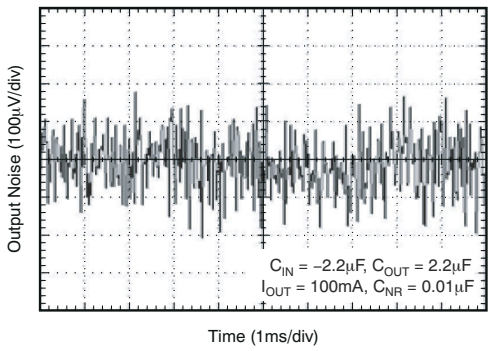


Figure 7-4. TPS72325 Output Noise vs Time (legacy chip)

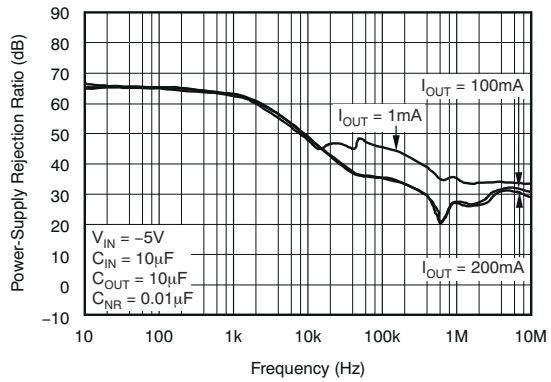
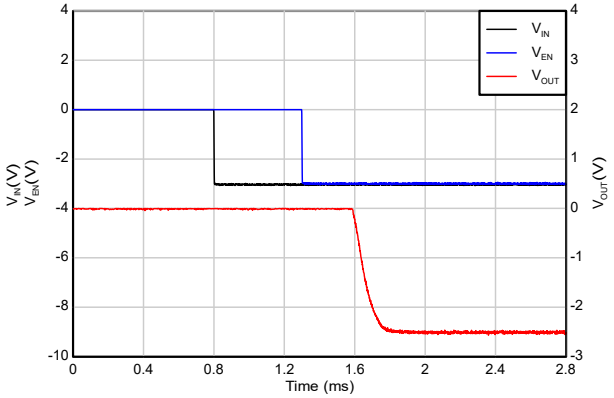
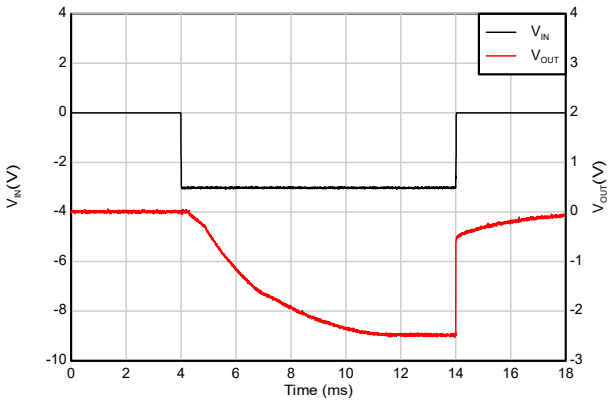


Figure 7-5. PSRR vs Frequency (legacy chip)



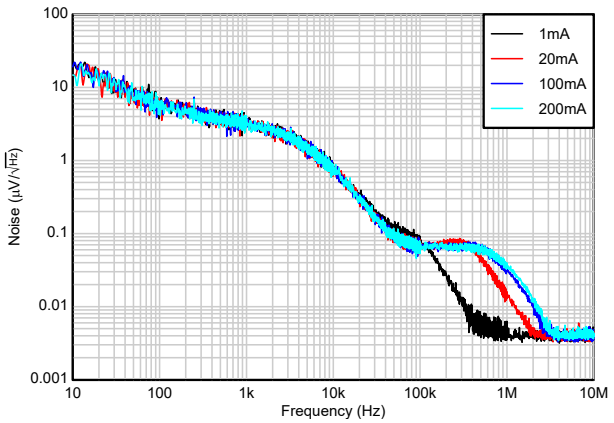
I_{OUT} = 200mA

Figure 7-6. TPS72325 Start-up Response (V_{IN} ramping before EN) (New chip)



I_{OUT} = 200mA, C_{NR} = 10nF

Figure 7-7. TPS72325 Start-up Response (V_{IN} & EN tied together) (New chip)



V_{IN} = –3.0V

Figure 7-8. TPS72325 Total Noise vs I_{OUT} (10 Hz to 100 kHz) (New chip)

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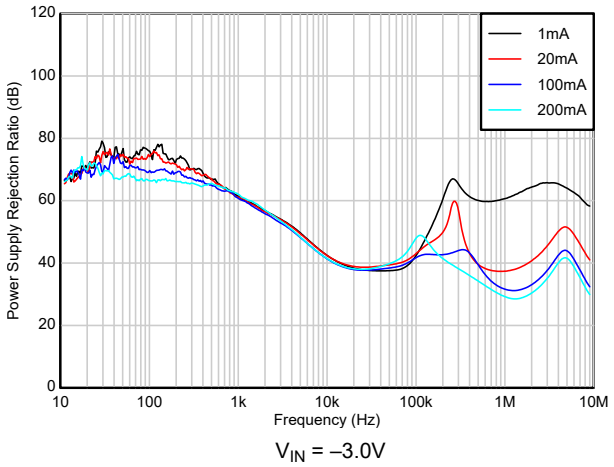


Figure 7-9. PSRR vs I_{OUT} (New chip)

7.3 Best Design Practices

Do place at least one 2.2-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1-µF to 2.2-µF low ESR capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

7.4 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between –10V and –2.7V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_I and V_O, with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

7.5.2 Layout Example

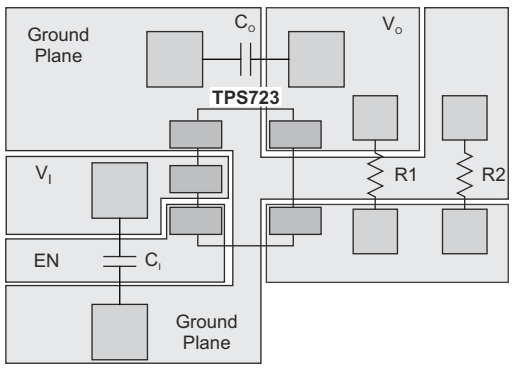


Figure 7-10. Example Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS723 is available through the product folders under *Simulation Models*.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature (1)

PRODUCT	V_{OUT}
TPS723**xxyyyz M3**	**xx** is nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable). **yyy** is package designator. **z** is package quantity. This device either ships with the legacy chip (CSO: DLN) or the new chip (CSO: DM6), which uses the latest manufacturing flow. The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the document. M3 is a suffix designator only significant for the new chip with CSO:DM6, which uses the latest manufacturing flow.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2019) to Revision E (March 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Features* section to add information about the new chip	1
• Updated the *Description* section to highlight key device performance parameters for both new and legacy chip	1
• Updated the *Pin Configuration and Functions* section to add detailed functionality about each pin	3
• Updated the *Absolute Maximum Ratings, ESD Ratings, Recommended Operating Conditions and Electrical Characteristics* to add performance details about the new chip and comparison with the legacy chip	4
• Updated *Typical Characteristics* section to show performance comparison between legacy and new chip	7
• Updated *Overview* section to provide information about the new chip	21
• Added functional block diagrams for the new chip and updated functional block diagrams for the fixed and adjustable devices	21
• Updated *Current Limit* section to show detailed information about device functionality	23
• Updated *Enable* section to show detailed information about device functionality	23
• Added *Dropout voltage* section to show detailed information about device functionality	24
• Added *Output Pullup* section to show detailed information about device functionality	24
• Added *Thermal Shutdown* section to show detailed information about device functionality	24
• Added *Undervoltage Lockout (UVLO)* section to show detailed information about device functionality	24
• Added *NR and Programmable Soft Start* section to show detailed information about device functionality	24
• Updated the *Device Functional Modes* section to show functionality of the device	25
• Added *Adjustable Device Feedback Resistor Selection* section to show detailed application information of the device	26
• Added *Recommended Capacitor Types* section to show detailed application information of the device	26
• Added *Input and Output Capacitor Selection* section to show detailed application information of the device	26
• Added *Reverse Current* section to show detailed application information of the device	27
• Added *Feed-Forward Capacitor (C_{FF})* section to show detailed application information of the device	27
• Added *Power Dissipation (P_D)* section to show detailed application information of the device	27
• Added *Estimating Junction Temperature* section to show detailed application information of the device	28
• Updated Figure 7-2 and added note comparing the legacy and new chip	29
• Added Table 7-1	29
• Added new curves to *Application Curves*	30
• Deleted the *Power Dissipation* and *Thermal Protection* sections	31
• Updated *Device Nomenclature* to provide further details about the device	32

Changes from Revision C (September 2014) to Revision D (December 2019)	Page
• Added DRV package to document	1
• Changed *Applications* section to link to end equipment	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS72301DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	T08I
TPS72301DDCR	NRND	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DDCR.A	NRND	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DRVR	NRND	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72301DRVR.A	NRND	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72301DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72301DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72325DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T02I
TPS72325DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02I
TPS72325DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T02I
TPS72325DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T02I
TPS72325DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS723 :

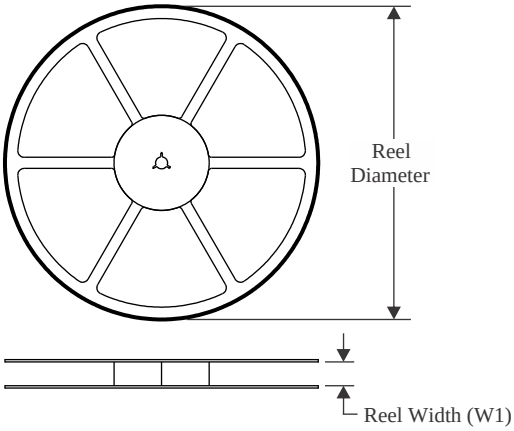
- Automotive : TPS723-Q1

NOTE: Qualified Version Definitions:

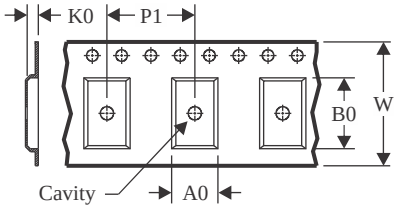
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

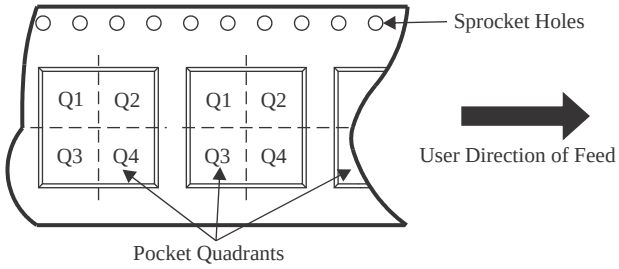


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

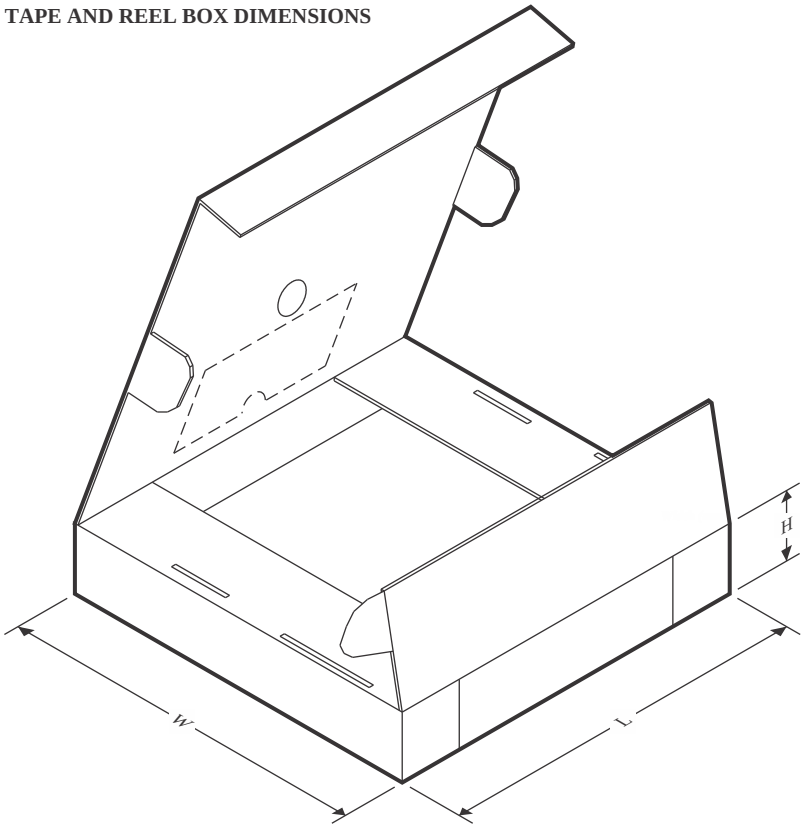
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72301DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS72301DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS72325DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325DBVRG4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

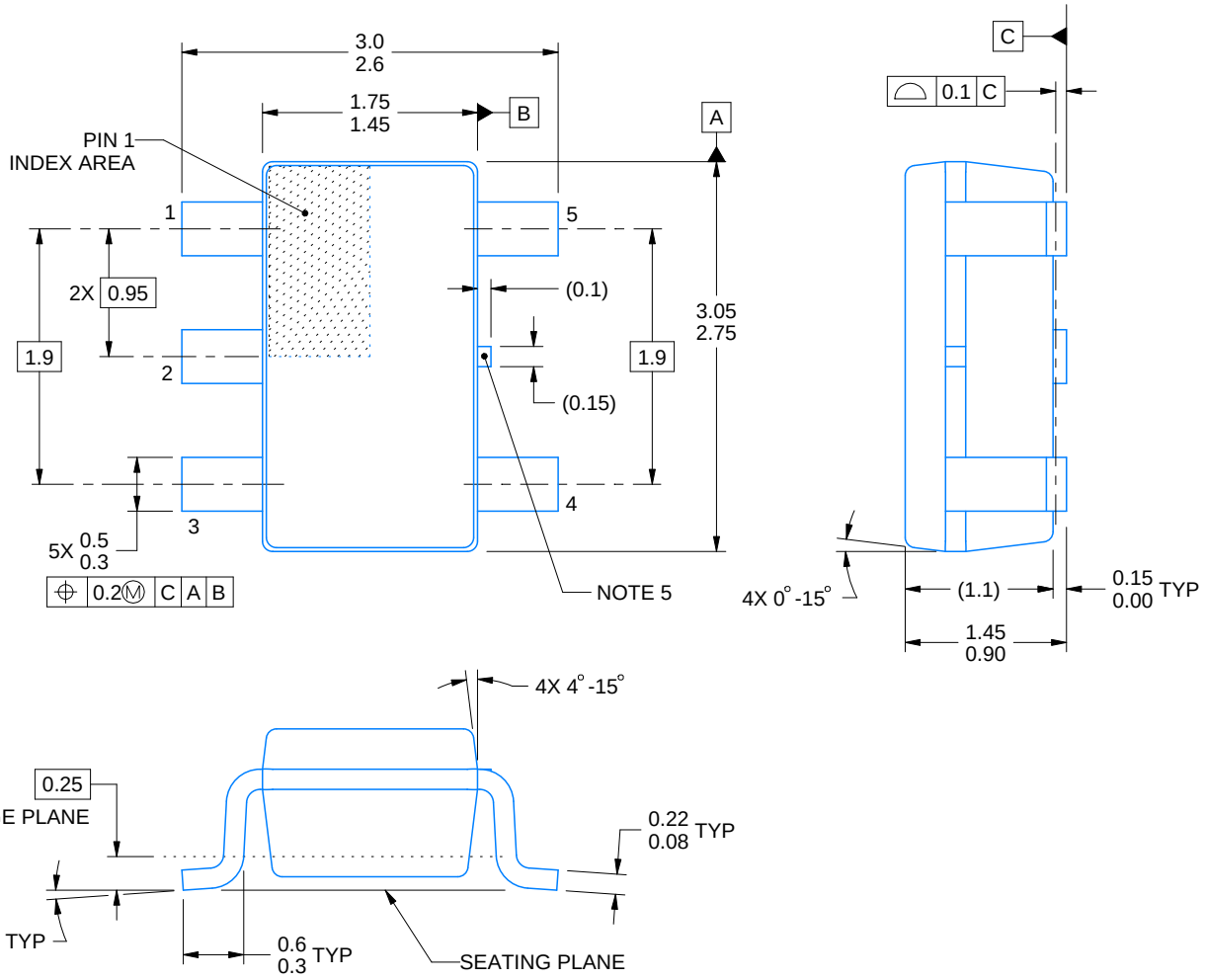
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72301DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS72301DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS72301DBVRG4	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS72301DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS72301DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS72301DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS72301DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS72301DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS72325DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS72325DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS72325DBVRG4	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS72325DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

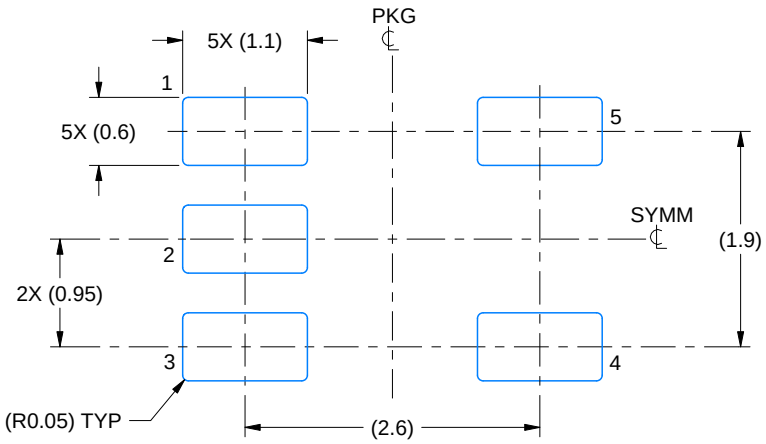
SMALL OUTLINE TRANSISTOR



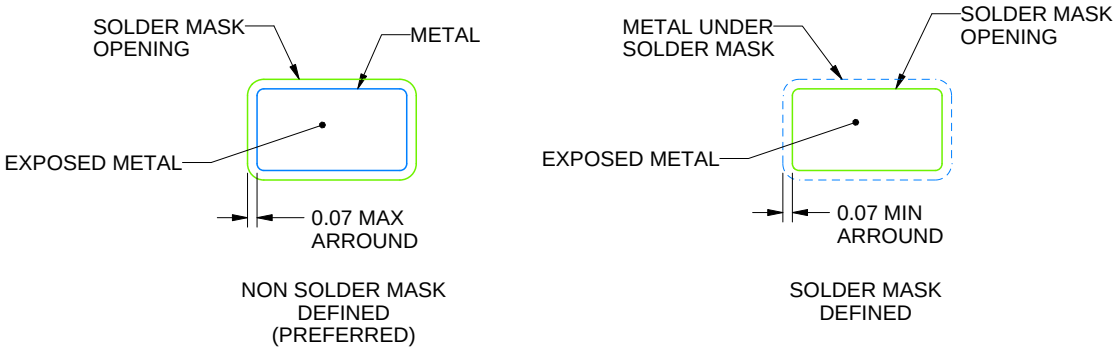
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

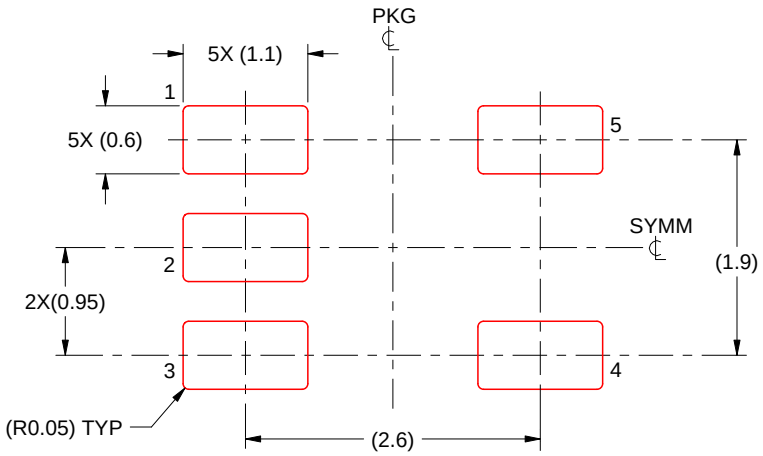


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

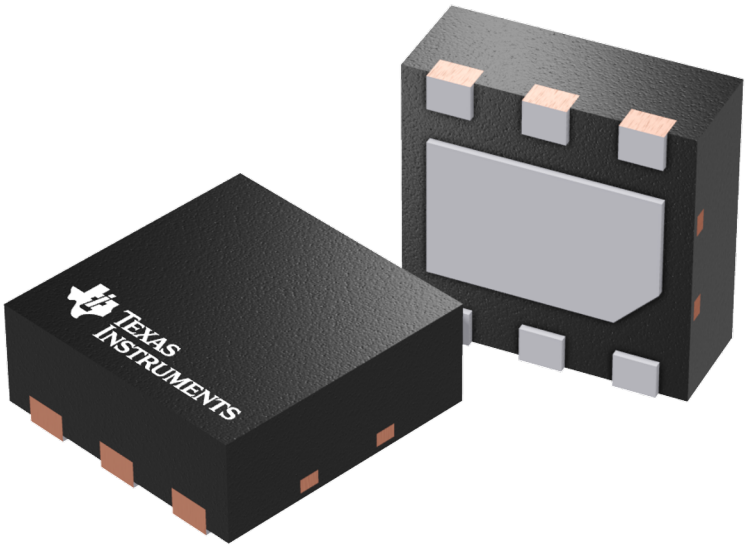
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

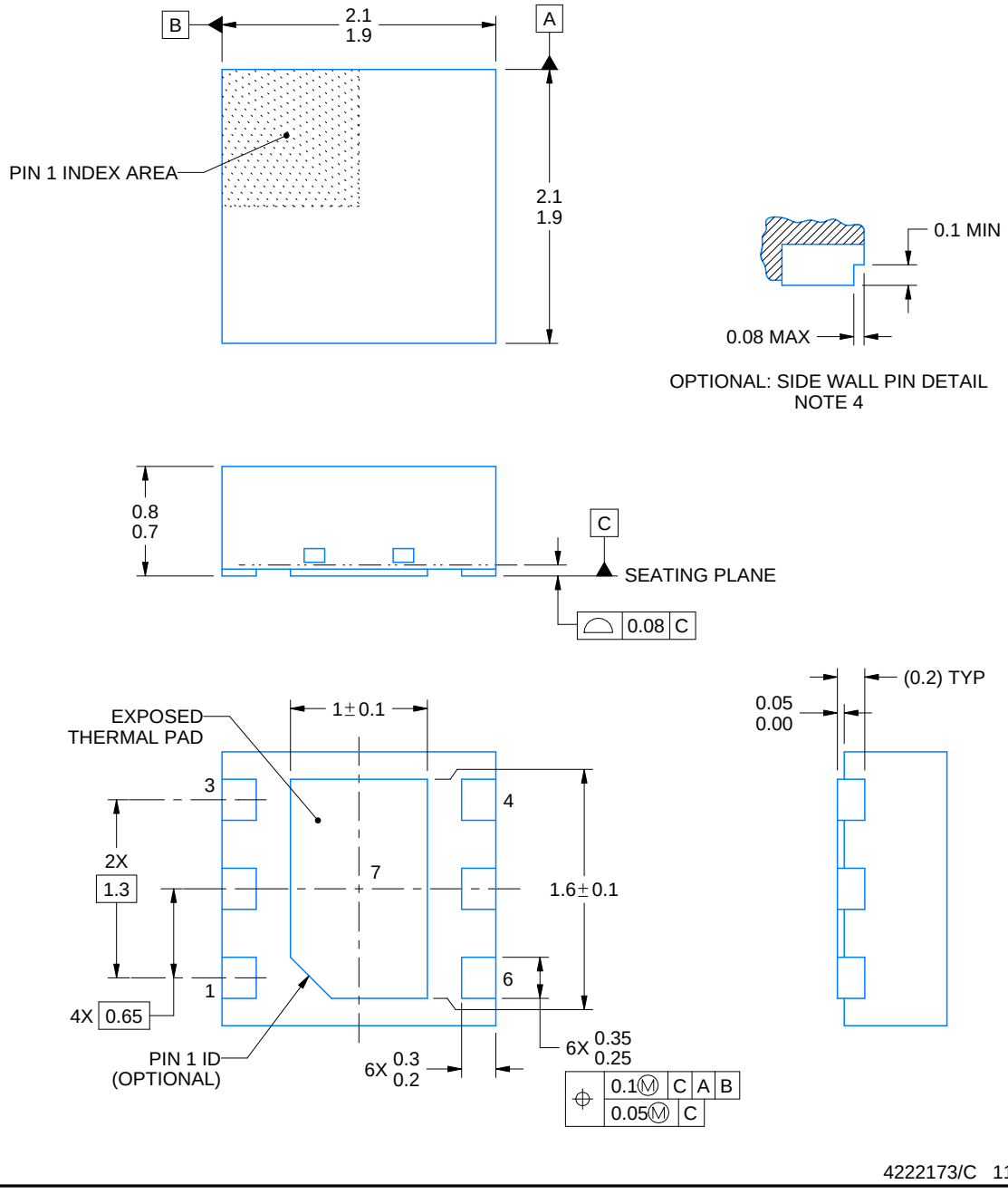
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



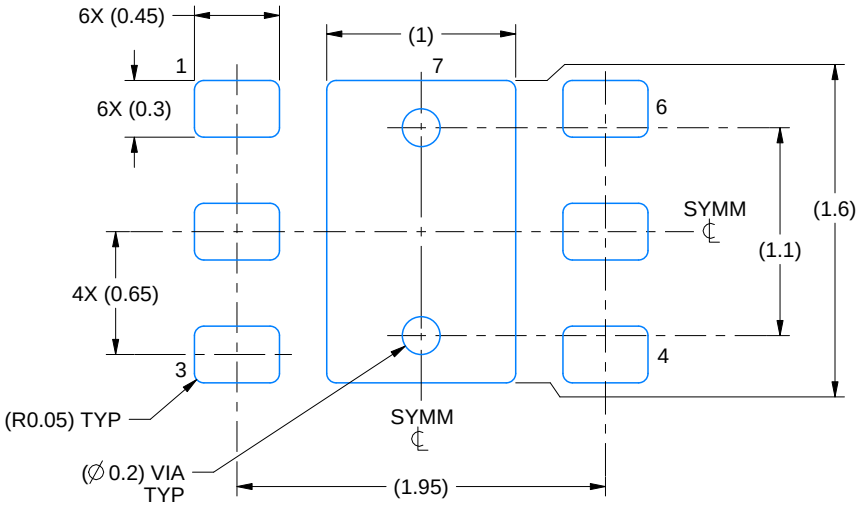
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

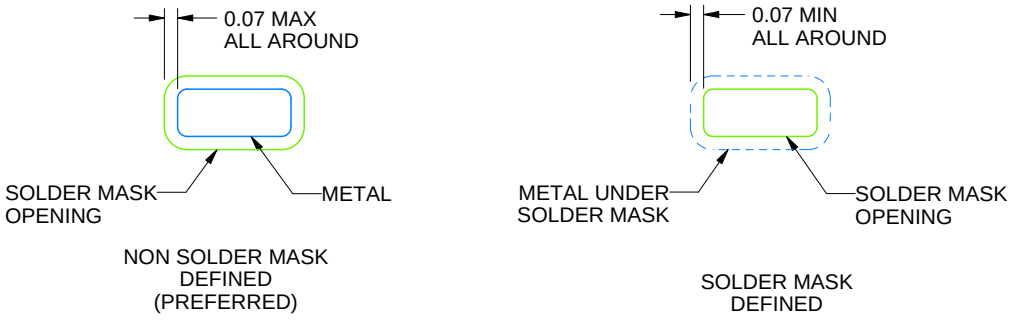


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

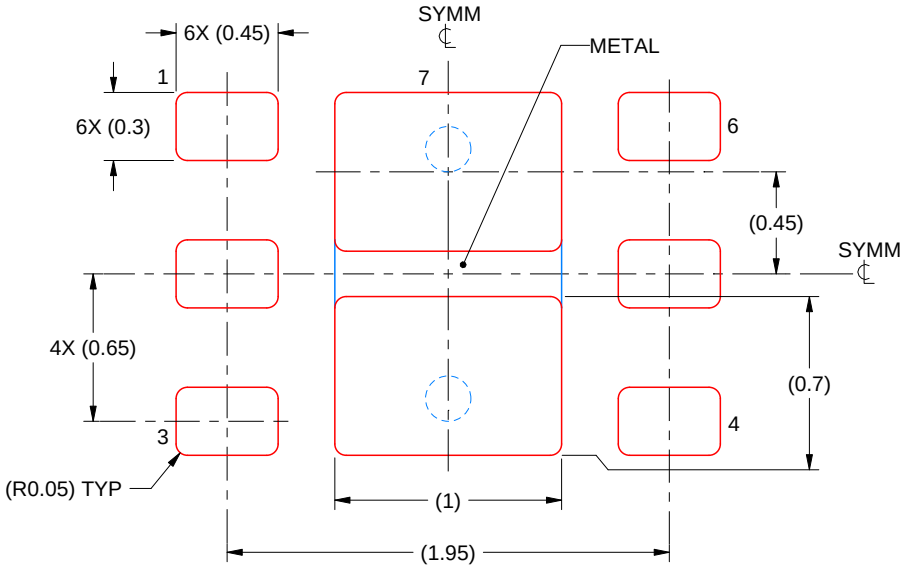


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

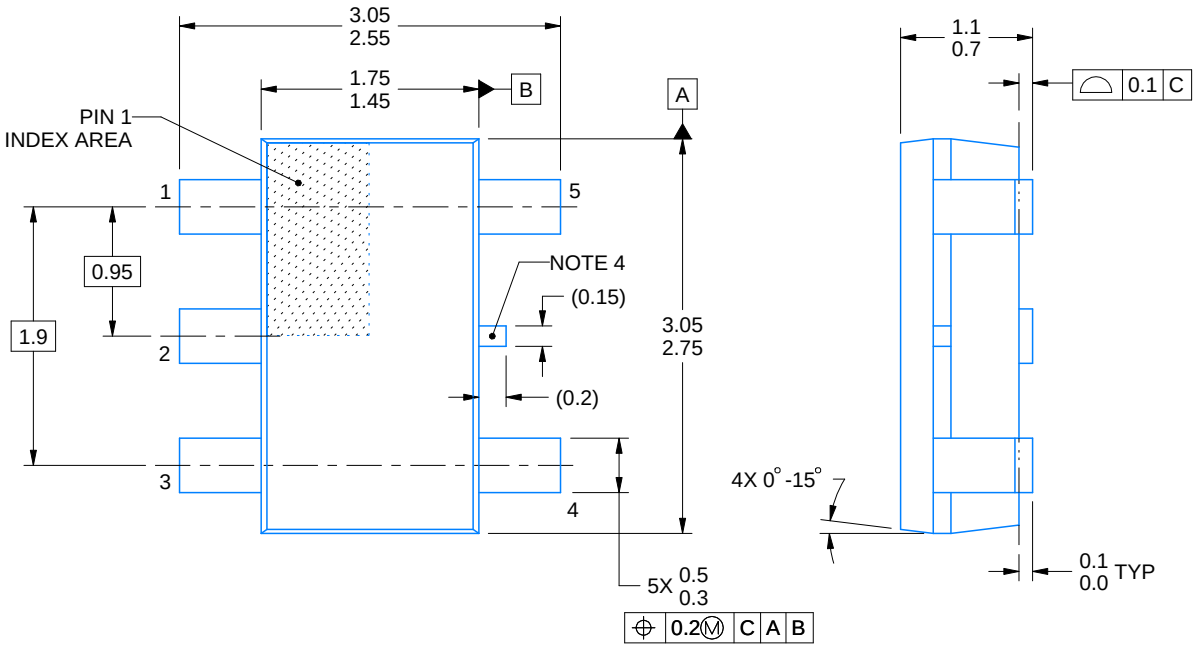
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

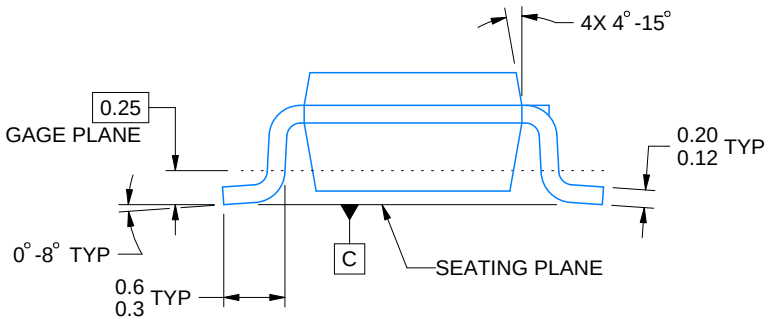
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

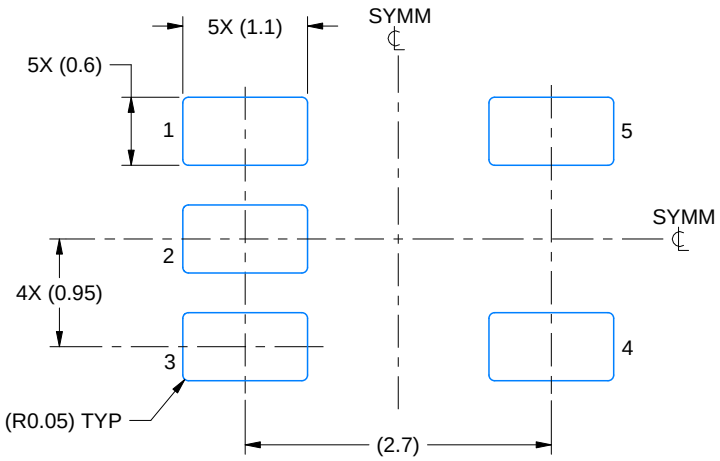




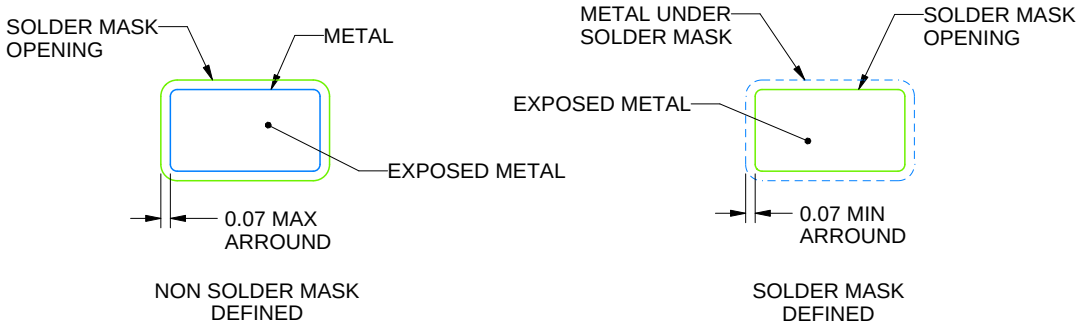
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

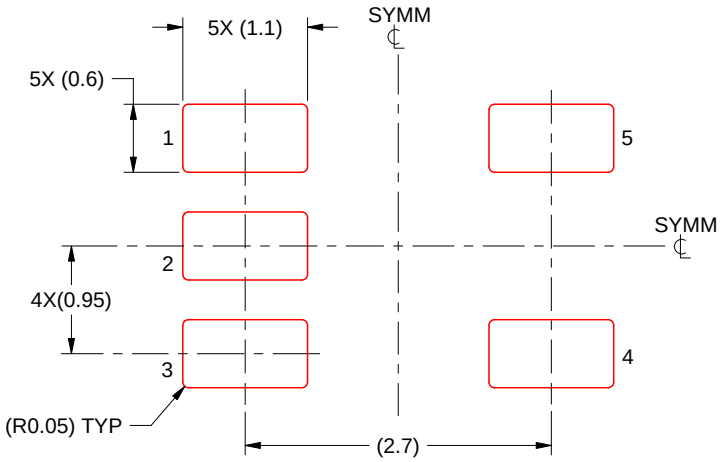


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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