

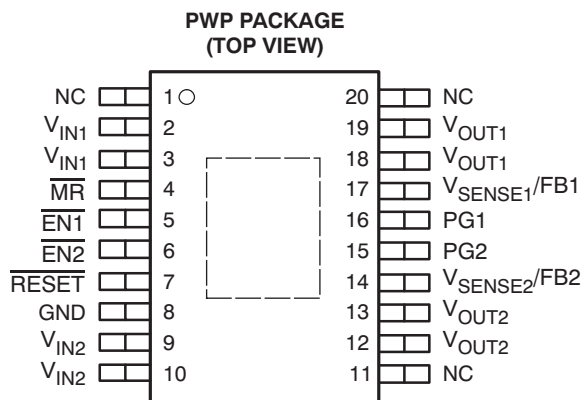
## DUAL-OUTPUT, LOW DROPOUT VOLTAGE REGULATORS WITH INTEGRATED SVS FOR SPLIT VOLTAGE SYSTEMS

### FEATURES

- Dual Output Voltages for Split-Supply Applications
- Independent Enable Functions (See Part Number [TPS707xx](#) for Sequenced Outputs)
- Output Current Range of 250 mA on Regulator 1 and 125 mA on Regulator 2
- Voltage Options: 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and Dual Adjustable Outputs
- Open Drain Power-On Reset with 120-ms Delay
- Open Drain Power Good for Regulator 1 and Regulator 2
- Ultralow 190- $\mu$ A (typ) Quiescent Current
- 1- $\mu$ A Input Current During Standby
- Low Noise: 65  $\mu$ V<sub>RMS</sub> Without Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- One Manual Reset Input
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 20-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection

### DESCRIPTION

The TPS708xx is a low dropout voltage regulator with integrated SVS ( $\overline{\text{RESET}}$ , POR, or power on reset) and power good (PG) functions. These devices are capable of supplying 250 mA and 125 mA by regulator 1 and regulator 2 respectively. Quiescent current is typically 190  $\mu$ A at full load. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset input, and independent enable functions provide a complete system solution.



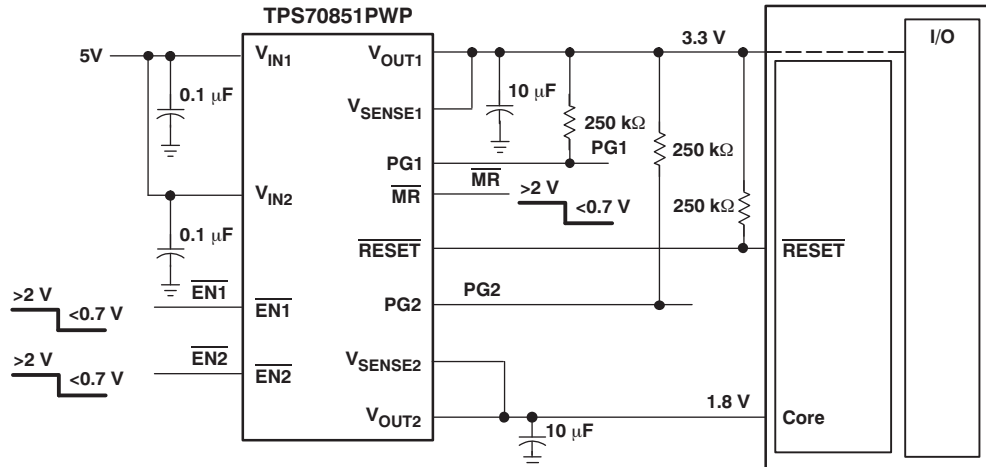
NC: No internal connection



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## DESCRIPTION (CONTINUED)

The TPS708xx family of voltage regulators offers very low dropout voltage and dual outputs. These devices have extremely low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 10-µF low ESR capacitors.

These devices have fixed 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and adjustable voltage options. Regulator 1 can support up to 250 mA, and regulator 2 can support up to 125 mA. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 170 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 230 µA over the full range of output current and full range of temperature). This LDO family also features a sleep mode; applying a high signal to  $\overline{\text{EN1}}$  or  $\overline{\text{EN2}}$  (enable) shuts down regulator 1 or regulator 2, respectively. When a high signal is applied to both  $\overline{\text{EN1}}$  and  $\overline{\text{EN2}}$ , both regulators enter sleep mode, thereby reducing the input current to 2 µA at  $T_J = +25^\circ\text{C}$ .

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage condition at  $V_{\text{OUT1}}$ . The PG1 pin can be used to implement a SVS ( $\overline{\text{RESET}}$ , POR, or power on reset) for the circuitry supplied by regulator 1. The PG2 pin reports the voltage conditions at  $V_{\text{OUT2}}$ . The PG2 pin can be used to implement a SVS (power on reset) for the circuitry supplied by regulator 2.

The TPS708xx features a  $\overline{\text{RESET}}$  (SVS, POR, or power on reset).  $\overline{\text{RESET}}$  output initiates a reset in the event of an undervoltage condition.  $\overline{\text{RESET}}$  also indicates the status of the manual reset pin ( $\overline{\text{MR}}$ ). When  $\overline{\text{MR}}$  is in the logic high state,  $\overline{\text{RESET}}$  goes to a high impedance state after a 120-ms delay. To monitor  $V_{\text{OUT1}}$ , the PG1 output pin can be connected to  $\overline{\text{MR}}$ . To monitor  $V_{\text{OUT2}}$ , the PG2 output pin can be connected to  $\overline{\text{MR}}$ .

The device has an undervoltage lockout UVLO circuit that prevents the internal regulators from turning on until  $V_{\text{IN1}}$  reaches 2.5V.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION<sup>(1)</sup>

| PRODUCT  | VOLTAGE (V) <sup>(2)</sup> |                   | PACKAGE-<br>LEAD<br>(DESIGNATOR) | SPECIFIED<br>TEMPERATURE<br>RANGE (T <sub>J</sub> ) | ORDERING<br>NUMBER | TRANSPORT<br>MEDIA, QUANTITY |
|----------|----------------------------|-------------------|----------------------------------|-----------------------------------------------------|--------------------|------------------------------|
|          | V <sub>OUT1</sub>          | V <sub>OUT2</sub> |                                  |                                                     |                    |                              |
| TPS70802 | Adjustable                 | Adjustable        | HTSSOP-20 (PWP)                  | –40°C to +125°C                                     | TPS70802PWP        | Tube, 70                     |
|          |                            |                   |                                  |                                                     | TPS70802PWPR       | Tape and Reel, 2000          |
| TPS70845 | 3.3 V                      | 1.2 V             | HTSSOP-20 (PWP)                  | –40°C to +125°C                                     | TPS70845PWP        | Tube, 70                     |
|          |                            |                   |                                  |                                                     | TPS70845PWPR       | Tape and Reel, 2000          |
| TPS70848 | 3.3 V                      | 1.5 V             | HTSSOP-20 (PWP)                  | –40°C to +125°C                                     | TPS70848PWP        | Tube, 70                     |
|          |                            |                   |                                  |                                                     | TPS70848PWPR       | Tape and Reel, 2000          |
| TPS70851 | 3.3 V                      | 1.8 V             | HTSSOP-20 (PWP)                  | –40°C to +125°C                                     | TPS70851PWP        | Tube, 70                     |
|          |                            |                   |                                  |                                                     | TPS70851PWPR       | Tape and Reel, 2000          |
| TPS70858 | 3.3 V                      | 2.5 V             | HTSSOP-20 (PWP)                  | –40°C to +125°C                                     | TPS70858PWP        | Tube, 70                     |
|          |                            |                   |                                  |                                                     | TPS70858PWPR       | Tape and Reel, 2000          |

(1) For the most current package and ordering information see the Package Option Addendum located at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) For fixed 1.20 V operation, tie FB to OUT.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

|                                                                         | TPS708xx                                      | UNIT |
|-------------------------------------------------------------------------|-----------------------------------------------|------|
| Input voltage range: V <sub>IN1</sub> , V <sub>IN2</sub> <sup>(2)</sup> | –0.3 to +7                                    | V    |
| Voltage range at $\overline{\text{EN1}}$ , $\overline{\text{EN2}}$      | –0.3 to +7                                    | V    |
| Output voltage range (V <sub>OUT1</sub> , V <sub>SENSE1</sub> )         | 5.5                                           | V    |
| Output voltage range (V <sub>OUT2</sub> , V <sub>SENSE2</sub> )         | 5.5                                           | V    |
| Maximum $\overline{\text{RESET}}$ , PG1, PG2 voltage                    | 7                                             | V    |
| Maximum $\overline{\text{MR}}$ voltage                                  | V <sub>IN1</sub>                              | V    |
| Peak output current                                                     | Internally limited                            | —    |
| Continuous total power dissipation                                      | See <a href="#">Dissipation Ratings Table</a> | —    |
| Operating virtual junction temperature range, T <sub>J</sub>            | –40 to +150                                   | °C   |
| Storage temperature range, T <sub>stg</sub>                             | –65 to +150                                   | °C   |
| ESD rating, HBM                                                         | 2                                             | kV   |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are tied to network ground.

## DISSIPATION RATINGS

| PACKAGE            | AIR FLOW (CFM) | $T_A \leq +25^\circ\text{C}$ | DERATING<br>FACTOR | $T_A = +70^\circ\text{C}$ | $T_A = +85^\circ\text{C}$ |
|--------------------|----------------|------------------------------|--------------------|---------------------------|---------------------------|
| PWP <sup>(1)</sup> | 0              | 3.067 W                      | 30.67 mW/°C        | 1.687 W                   | 1.227 W                   |
|                    | 250            | 4.115 W                      | 41.15 mW/°C        | 2.265 W                   | 1.646 W                   |

- (1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on a 4-in by 4-in ground layer. Simultaneous and continuous operation of both regulator outputs at full load may exceed the power dissipation rating of the PWP package. For more information, refer to TI technical brief [SLMA002](#).

## RECOMMENDED OPERATING CONDITIONS

Over operating temperature range (unless otherwise noted).

|                                                         | MIN  | MAX  | UNIT |
|---------------------------------------------------------|------|------|------|
| Input voltage, $V_I$ <sup>(1)</sup> (regulator 1 and 2) | 2.7  | 6    | V    |
| Output current, $I_O$ (regulator 1)                     | 0    | 500  | mA   |
| Output current, $I_O$ (regulator 2)                     | 0    | 250  | mA   |
| Output voltage range (for adjustable option)            | 1.22 | 5.5  | V    |
| Operating virtual junction temperature, $T_J$           | –40  | +125 | °C   |

- (1) To calculate the minimum input voltage for maximum output current, use the following equation:  $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$ .

## ELECTRICAL CHARACTERISTICS

Over recommended operating junction temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN1}$  or  $V_{IN2} = V_{OUT(nom)} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{\text{EN}} = 0\text{ V}$ , and  $C_{OUT} = 33\text{ }\mu\text{F}$  (unless otherwise noted).

| PARAMETER                                                                                                                           |                                                          |                   | TEST CONDITIONS                                                                        |                                       | MIN   | TYP   | MAX   | UNIT              |     |
|-------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-------------------|----------------------------------------------------------------------------------------|---------------------------------------|-------|-------|-------|-------------------|-----|
| V <sub>O</sub>                                                                                                                      | Output voltage <sup>(1),(2)</sup>                        | Reference voltage | 2.7 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               | FB connected to V <sub>O</sub>        |       | 1.22  |       | V                 |     |
|                                                                                                                                     |                                                          |                   | 2.7 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               | FB connected to V <sub>O</sub>        | 1.196 |       | 1.244 |                   |     |
|                                                                                                                                     |                                                          | 1.2 V Output      | 2.7 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       |       | 1.2   |       |                   |     |
|                                                                                                                                     |                                                          |                   | 2.7 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       | 1.176 |       | 1.224 |                   |     |
|                                                                                                                                     |                                                          | 1.5 V Output      | 2.7 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       |       | 1.5   |       |                   |     |
|                                                                                                                                     |                                                          |                   | 2.7 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       | 1.47  |       | 1.53  |                   |     |
|                                                                                                                                     |                                                          | 1.8 V Output      | 2.8 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       |       | 1.8   |       |                   |     |
|                                                                                                                                     |                                                          |                   | 2.8 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       | 1.764 |       | 1.836 |                   |     |
|                                                                                                                                     |                                                          | 2.5 V Output      | 3.5 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       |       | 2.5   |       |                   |     |
|                                                                                                                                     |                                                          |                   | 3.5 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C                               |                                       | 2.45  |       | 2.55  |                   |     |
| 3.3 V Output                                                                                                                        | 4.3 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C |                   |                                                                                        | 3.3                                   |       |       |       |                   |     |
|                                                                                                                                     | 4.3 V < V <sub>IN</sub> < 6 V,<br>T <sub>J</sub> = +25°C |                   | 3.234                                                                                  |                                       | 3.366 |       |       |                   |     |
| Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{\text{EN}}1 = \overline{\text{EN}}2 = 0\text{ V}^{(1)}$ |                                                          |                   | See <sup>(2)</sup>                                                                     | T <sub>J</sub> = +25°C                |       | 190   |       | μA                |     |
|                                                                                                                                     |                                                          |                   | See <sup>(2)</sup>                                                                     |                                       |       |       |       |                   | 230 |
| Output voltage line regulation ( $\Delta V_O/V_O$ ) for regulator 1 and regulator 2 <sup>(3)</sup>                                  |                                                          |                   | V <sub>O</sub> + 1 V < V <sub>IN</sub> ≤ 6 V,<br>T <sub>J</sub> = +25°C <sup>(1)</sup> |                                       |       | 0.01  |       | %V                |     |
|                                                                                                                                     |                                                          |                   | V <sub>O</sub> + 1 V < V <sub>IN</sub> ≤ 6 V<br>T <sub>J</sub> = +25°C <sup>(1)</sup>  |                                       |       |       |       |                   | 0.1 |
| Load regulation for V <sub>OUT1</sub> and V <sub>OUT2</sub>                                                                         |                                                          |                   | T <sub>J</sub> = +25°C                                                                 |                                       |       | 1     |       | mV                |     |
| V <sub>n</sub>                                                                                                                      | Output noise voltage                                     | Regulator 1       | BW = 300 Hz to 50 kHz,<br>C <sub>O</sub> = 33 μF, T <sub>J</sub> = +25°C               |                                       |       | 65    |       | μV <sub>RMS</sub> |     |
|                                                                                                                                     |                                                          | Regulator 2       |                                                                                        |                                       |       | 65    |       |                   |     |
| Output current limit                                                                                                                |                                                          | Regulator 1       | V <sub>OUT</sub> = 0 V                                                                 |                                       |       | 1.6   | 1.9   | A                 |     |
|                                                                                                                                     |                                                          | Regulator 2       |                                                                                        |                                       |       | 0.750 | 1     |                   |     |
| Thermal shutdown junction temperature                                                                                               |                                                          |                   |                                                                                        |                                       |       | +150  |       | °C                |     |
| I <sub>I</sub> (standby)                                                                                                            | Standby current                                          | Regulator 1       | $\overline{\text{EN}}1 = V_{\text{IN}}$ , $\overline{\text{EN}}2 = V_{\text{IN}}$      | T <sub>J</sub> = +25°C                |       |       | 2     | μA                |     |
|                                                                                                                                     |                                                          | Regulator 2       | $\overline{\text{EN}}1 = V_{\text{IN}}$ , $\overline{\text{EN}}2 = V_{\text{IN}}$      |                                       |       |       | 6     |                   |     |
| PSRR                                                                                                                                | Power-supply ripple rejection                            | Regulator 1       | f = 1 kHz, C <sub>OUT</sub> = 33 μF, I <sub>OUT1</sub> = 250 mA                        | T <sub>J</sub> = +25°C <sup>(1)</sup> |       | 60    |       | dB                |     |
|                                                                                                                                     |                                                          | Regulator 2       | f = 1 kHz, C <sub>OUT</sub> = 33 μF, I <sub>OUT2</sub> = 125 mA                        | T <sub>J</sub> = +25°C <sup>(1)</sup> |       | 50    |       |                   |     |
| UVLO threshold                                                                                                                      |                                                          |                   |                                                                                        |                                       |       | 2.4   | 2.65  | V                 |     |
| RESET Terminal                                                                                                                      |                                                          |                   |                                                                                        |                                       |       |       |       |                   |     |
| Minimum input voltage for valid $\overline{\text{RESET}}$                                                                           |                                                          |                   | I <sub>(RESET)</sub> = 300 μA, V <sub>(RESET)</sub> ≤ 0.8 V                            |                                       |       | 1.0   | 1.3   | V                 |     |
| $t_{\text{(RESET)}}$                                                                                                                |                                                          |                   | $\overline{\text{RESET}}$ pulse duration                                               |                                       |       | 80    | 120   | 160               | ms  |
| Output low voltage                                                                                                                  |                                                          |                   | V <sub>IN</sub> = 3.5 V, I <sub>(RESET)</sub> = 1 mA                                   |                                       |       | 0.15  | 0.4   | V                 |     |
| Leakage current                                                                                                                     |                                                          |                   | V <sub>(RESET)</sub> = 6 V                                                             |                                       |       |       | 1     | μA                |     |

(1) Minimum input operating voltage is  $2.7\text{ V}$  or  $V_{O(\text{typ})} + 1\text{ V}$ , whichever is greater. Maximum input voltage =  $6\text{ V}$ , minimum output current =  $1\text{ mA}$ .

(2)  $I_O = 1\text{ mA}$  to  $250\text{ mA}$  for Regulator 1 and  $1\text{ mA}$  to  $125\text{ mA}$  for Regulator 2.

(3) If  $V_O < 1.8\text{ V}$  then  $V_{\text{Imax}} = 6\text{ V}$ ,  $V_{\text{Imin}} = 2.7\text{ V}$ :  

$$\text{Line regulation (mV)} = (\%/\text{V}) \times V_O \times \frac{(V_{\text{Imax}} - 2.7)}{100} \times 1000$$
If  $V_O > 2.5\text{ V}$  then  $V_{\text{Imax}} = 6\text{ V}$ ,  $V_{\text{Imin}} = V_O + 1\text{ V}$ :  

$$\text{Line regulation (mV)} = (\%/\text{V}) \times V_O \times \frac{[V_{\text{Imax}} - (V_O + 1)]}{100} \times 1000$$

## ELECTRICAL CHARACTERISTICS (continued)

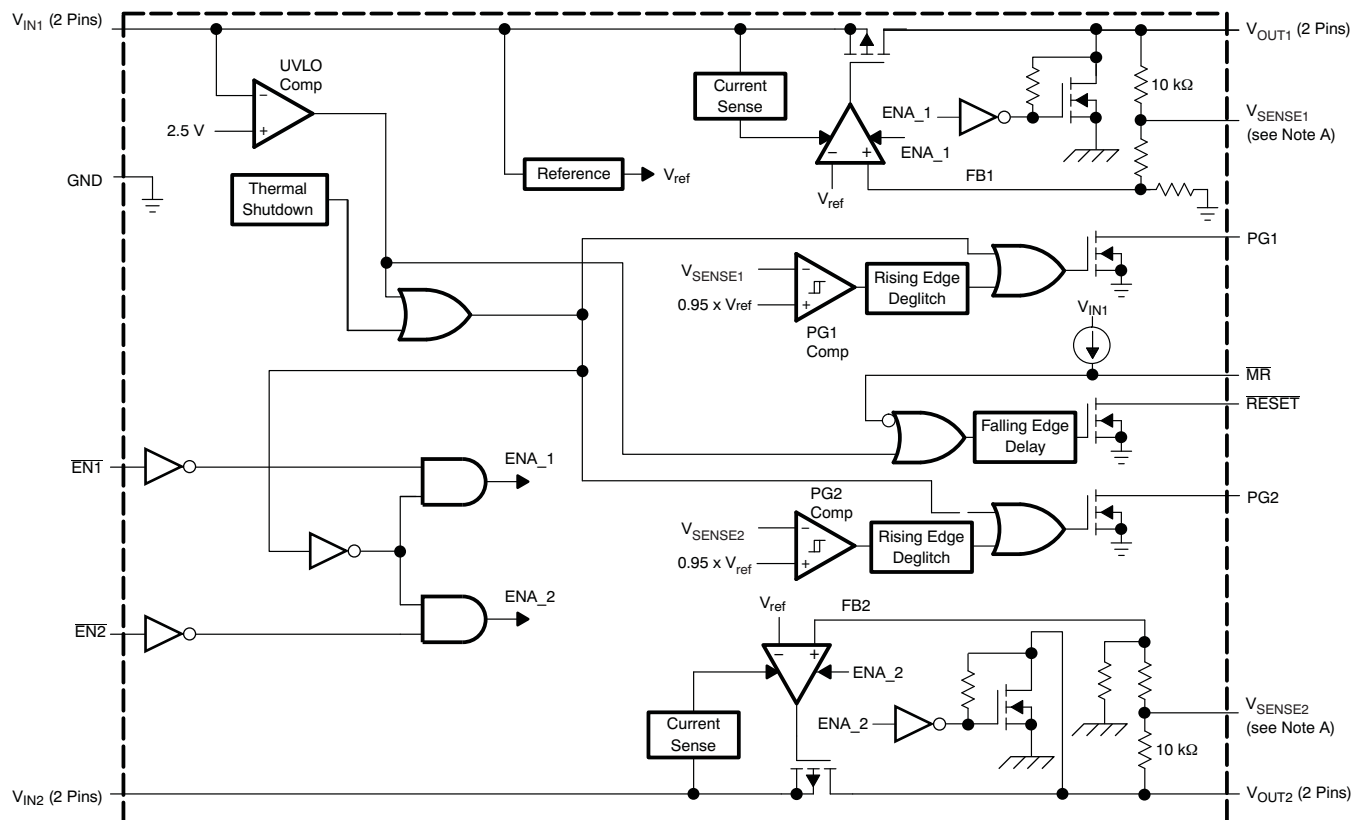
Over recommended operating junction temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN1}$  or  $V_{IN2} = V_{OUT(nom)} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{\text{EN}} = 0\text{ V}$ , and  $C_{OUT} = 33\text{ }\mu\text{F}$  (unless otherwise noted).

| PARAMETER                                        | TEST CONDITIONS                                                              | MIN | TYP  | MAX | UNIT          |
|--------------------------------------------------|------------------------------------------------------------------------------|-----|------|-----|---------------|
| <b>PG1/PG2 Terminal</b>                          |                                                                              |     |      |     |               |
| Minimum input voltage for valid PGx              | $I_{(PGx)} = 300\text{ }\mu\text{A}$ , $V_{(PGx)} \leq 0.8\text{ V}$         |     | 1.0  | 1.3 | V             |
| Trip threshold voltage                           | $V_O$ decreasing                                                             | 92  | 95   | 98  | % $V_{OUT}$   |
| Hysteresis voltage                               | Measured at $V_O$                                                            |     | 0.5  |     | % $V_{OUT}$   |
| $t_{r(PGX)}$                                     | Rising edge deglitch                                                         |     | 30   |     | $\mu\text{s}$ |
| Output low voltage                               | $V_{IN} = 2.7\text{ V}$ , $I_{(PGx)} = 1\text{ mA}$                          |     | 0.15 | 0.4 | V             |
| Leakage current                                  | $V_{(PGx)} = 6\text{ V}$                                                     |     |      | 1   | $\mu\text{A}$ |
| <b>EN1/EN2 Terminal</b>                          |                                                                              |     |      |     |               |
| High-level $\overline{\text{ENx}}$ input voltage |                                                                              | 2   |      |     | V             |
| Low-level $\overline{\text{ENx}}$ input voltage  |                                                                              |     |      | 0.7 | V             |
| Input current ( $\overline{\text{ENx}}$ )        |                                                                              | -1  |      | 1   | $\mu\text{A}$ |
| <b>MR Terminal</b>                               |                                                                              |     |      |     |               |
| High-level input voltage                         |                                                                              | 2   |      |     | V             |
| Low-level input voltage                          |                                                                              |     |      | 0.7 | V             |
| Falling edge delay                               | Measured at $V_O$                                                            |     | 140  |     | $\mu\text{s}$ |
| Pull-up current source                           |                                                                              |     | 6    |     | $\mu\text{A}$ |
| <b>V<sub>OUT1</sub> Terminal</b>                 |                                                                              |     |      |     |               |
| Dropout voltage <sup>(4)</sup>                   | $I_O = 250\text{ mA}$ , $V_{IN1} = 3.2\text{ V}$ $T_J = +25^{\circ}\text{C}$ |     | 83   |     | mV            |
|                                                  | $I_O = 250\text{ mA}$ , $V_{IN1} = 3.2\text{ V}$                             |     |      | 140 |               |
| Peak output current                              | 2 ms pulse width                                                             |     | 750  |     | mA            |
| Discharge transistor current                     | $V_{OUT1} = 1.5\text{ V}$                                                    |     | 7.5  |     | mA            |
| <b>V<sub>OUT2</sub> Terminal</b>                 |                                                                              |     |      |     |               |
| Peak output current                              | 2 ms pulse width                                                             |     | 375  |     | mA            |
| Discharge transistor current                     | $V_{OUT2} = 1.5\text{ V}$                                                    |     | 7.5  |     | mA            |
| <b>FB Terminal</b>                               |                                                                              |     |      |     |               |
| Input current: TPS70802                          | FB = 1.8 V                                                                   |     | 1    |     | $\mu\text{A}$ |

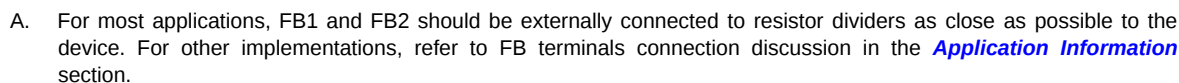
(4) Input voltage ( $V_{IN1}$  or  $V_{IN2}$ ) =  $V_{O(typ)} - 100\text{ mV}$ . For 1.5-V, 1.8-V, and 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3-V regulator input is set to 3.2 V to perform this test.

## DEVICE INFORMATION

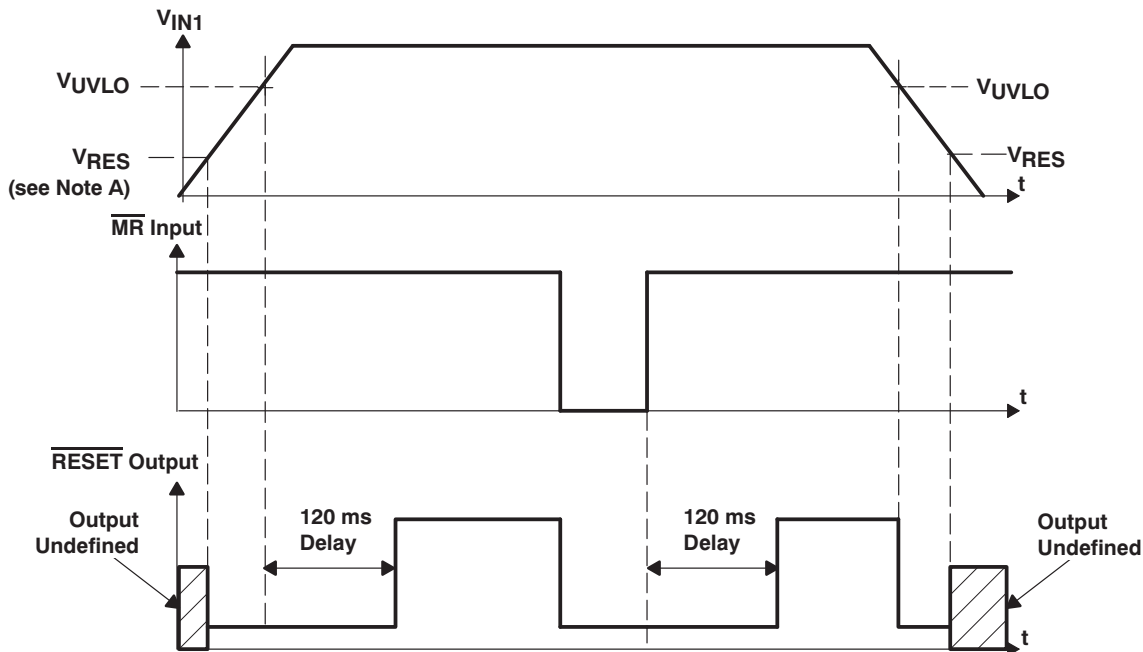
### Fixed Voltage Version



- A. For most applications,  $V_{SENSE1}$  and  $V_{SENSE2}$  should be externally connected to  $V_{OUT1}$  and  $V_{OUT2}$ , respectively, as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the [Application Information](#) section.

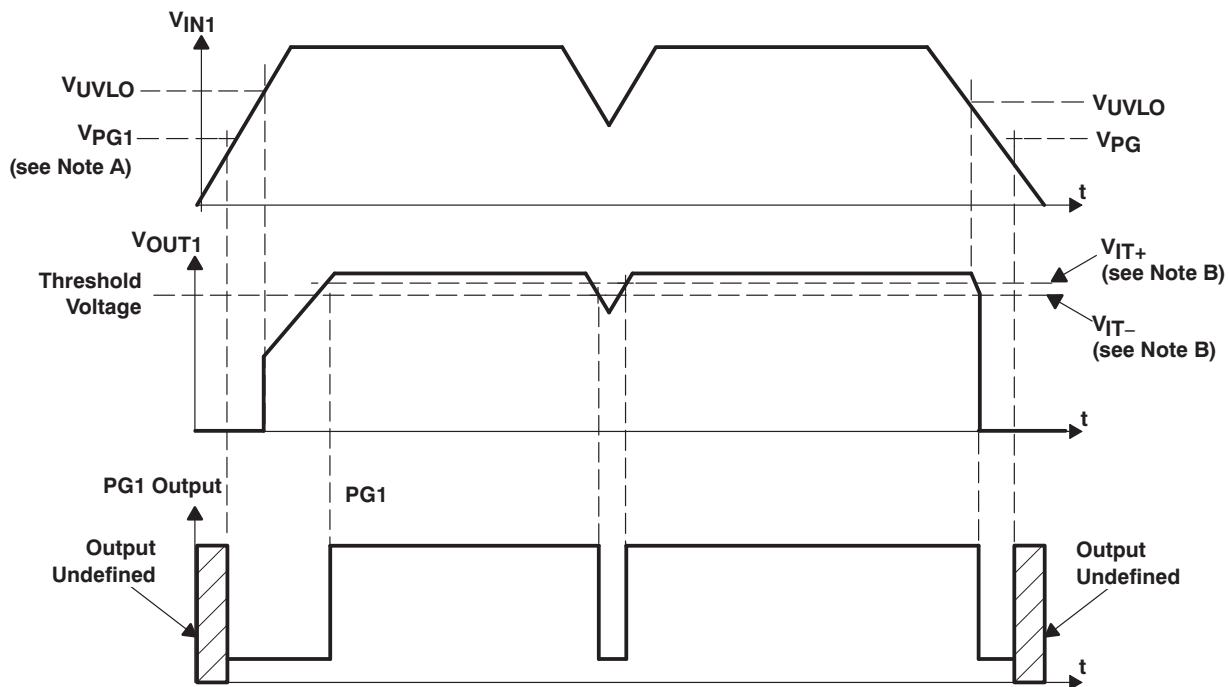


### RESET Timing Diagram



NOTE A:  $V_{RES}$  is the minimum input voltage for a valid  $\overline{RESET}$ . The symbol  $V_{RES}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.

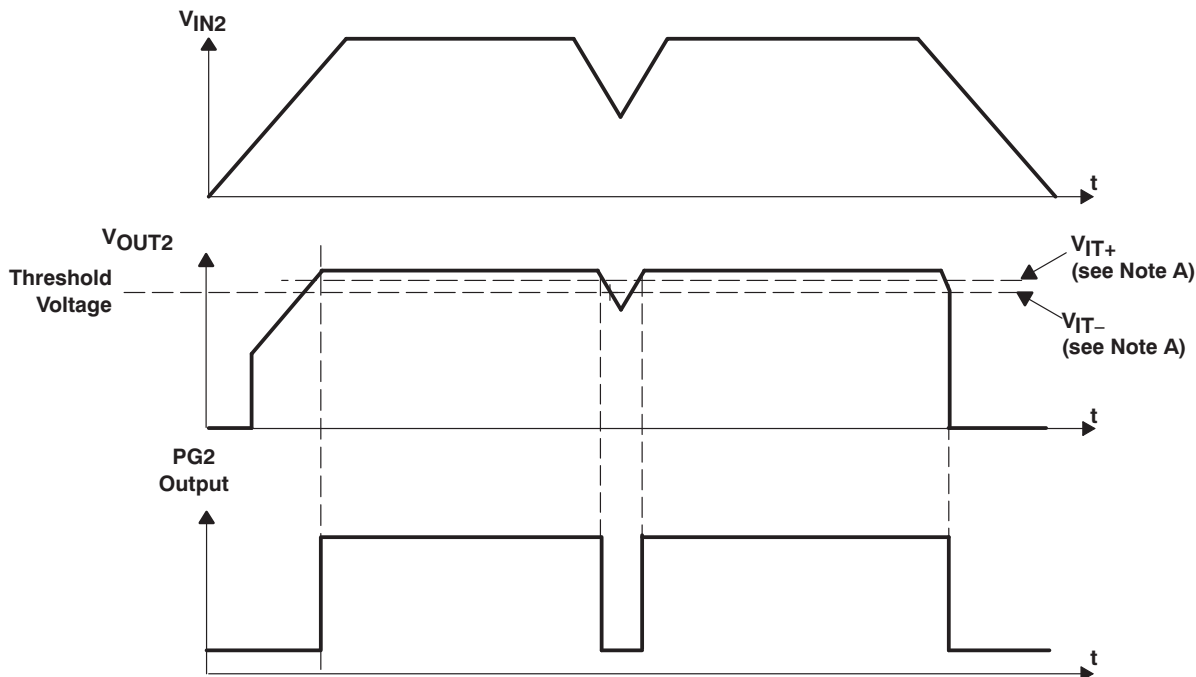
### PG1 Timing Diagram



NOTES A:  $V_{PG1}$  is the minimum input voltage for a valid PG. The symbol  $V_{PG1}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B:  $V_{IT-}$  trip voltage is typically 5% lower than the output voltage ( $95\%V_O$ ).  $V_{IT-}$  to  $V_{IT+}$  is the hysteresis voltage.

PG2 Timing Diagram (assuming  $V_{IN1}$  already powered up)



NOTE A:  $V_{IT-}$  trip voltage is typically 5% lower than the output voltage ( $95\%V_O$ ).  $V_{IT-}$  to  $V_{IT+}$  is the hysteresis voltage.

## TERMINAL FUNCTIONS

| TERMINAL           |           | I/O | DESCRIPTION                                                                                      |
|--------------------|-----------|-----|--------------------------------------------------------------------------------------------------|
| NAME               | NO.       |     |                                                                                                  |
| $\overline{EN1}$   | 5         | I   | Active low enable for $V_{OUT1}$                                                                 |
| $\overline{EN2}$   | 6         | I   | Active low enable for $V_{OUT2}$                                                                 |
| GND                | 8         | —   | Ground                                                                                           |
| $\overline{MR}$    | 4         | I   | Manual reset input, active low, pulled up internally                                             |
| NC                 | 1, 11, 20 | —   | No connection                                                                                    |
| PG1                | 16        | O   | Open drain output, low when $V_{OUT1}$ voltage is less than 95% of the nominal regulated voltage |
| PG2                | 15        | O   | Open drain output, low when $V_{OUT2}$ voltage is less than 95% of the nominal regulated voltage |
| $\overline{RESET}$ | 7         | I   | Open drain output, SVS (power-on reset) signal, active low                                       |
| $V_{IN1}$          | 2, 3      | I   | Input voltage of regulator 1                                                                     |
| $V_{IN2}$          | 9, 10     | I   | Input voltage of regulator 2                                                                     |
| $V_{OUT1}$         | 18, 19    | O   | Output voltage of regulator 1                                                                    |
| $V_{OUT2}$         | 12, 13    | O   | Output voltage of regulator 2                                                                    |
| $V_{SENSE2}/FB2$   | 14        | I   | Regulator 2 output voltage sense/regulator 2 feedback for adjustable                             |
| $V_{SENSE1}/FB1$   | 17        | I   | Regulator 1 output voltage sense/regulator 1 feedback for adjustable                             |

## Detailed Description

The TPS708xx low dropout regulator family provides dual regulated output voltages with independent enable functions. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Other features are integrated SVS (power-on reset,  $\overline{\text{RESET}}$ ) and power good (PG1, PG2) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete power solution.

The TPS708xx, unlike many other LDOs, features very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ( $I_B = I_C/\beta$ ). The TPS708xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage-driven, operating current is low and stable over the full load range.

## Pin Functions

### Enable ( $\overline{\text{EN1}}$ , $\overline{\text{EN2}}$ )

The  $\overline{\text{EN}}$  terminals are inputs that enable or shut down each respective regulator. If  $\overline{\text{EN}}$  is at a voltage high signal, the respective regulator is in shutdown mode. When  $\overline{\text{EN}}$  goes to voltage low, the respective regulator is enabled.

### Power-Good (PG1, PG2)

The PG terminals are open drain, active high output terminals that indicate the status of each respective regulator. When  $V_{\text{OUT1}}$  reaches 95% of its regulated voltage, PG1 goes to a high impedance state. When  $V_{\text{OUT2}}$  reaches 95% of its regulated voltage, PG2 goes to a high impedance state. Each PG goes to a low impedance state when its respective output voltage is pulled below 95% (that is, goes to an overload condition) of its regulated voltage. The open drain outputs of the PG terminals require a pull-up resistor.

### Manual Reset Pin

$\overline{\text{MR}}$  is an active low input terminal used to trigger a reset condition. When  $\overline{\text{MR}}$  is pulled to logic low, a POR ( $\overline{\text{RESET}}$ ) occurs. The terminal has a 6- $\mu\text{A}$  pull-up current to  $V_{\text{IN1}}$ .

### Sense ( $V_{\text{SENSE1}}$ , $V_{\text{SENSE2}}$ )

The sense terminals of fixed-output options must be connected to the regulator outputs, and the connection should be as short as possible. Internally, the sense terminal connects to high-impedance, wide-bandwidth amplifiers through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way as to minimize or avoid noise pickup. Adding RC networks between sense terminals and  $V_{\text{OUT}}$  terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

## FB1 and FB2

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize or avoid noise pickup. Adding RC networks between FB terminals and  $V_{OUT}$  terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

## $\overline{RESET}$ Indicator

The TPS708xx features a  $\overline{RESET}$  (SVS, POR, or power on reset).  $\overline{RESET}$  can be used to drive power on reset circuitry or a low-battery indicator.  $\overline{RESET}$  is an active low, open drain output that indicates the status of the manual reset pin ( $\overline{MR}$ ). When  $\overline{MR}$  is in a high-impedance state,  $\overline{RESET}$  goes to a high impedance state after a 120-ms delay. To monitor  $V_{OUT1}$ , the PG1 output pin can be connected to  $\overline{MR}$ . To monitor  $V_{OUT2}$ , the PG2 output pin can be connected to  $\overline{MR}$ . The open drain output of the  $\overline{RESET}$  terminal requires a pull-up resistor. If  $\overline{RESET}$  is not used, it can be left floating.

## $V_{IN1}$ and $V_{IN2}$

$V_{IN1}$  and  $V_{IN2}$  are inputs to each regulator. **Internal bias voltages are powered by  $V_{IN1}$ .**

## $V_{OUT1}$ and $V_{OUT2}$

$V_{OUT1}$  and  $V_{OUT2}$  are output terminals of each regulator.

## TYPICAL CHARACTERISTICS

Table of Graphs

|       |                                        |                         | FIGURE                  |
|-------|----------------------------------------|-------------------------|-------------------------|
| $V_O$ | Output voltage                         | vs Output current       | Figure 1 to Figure 3    |
|       |                                        | vs Junction temperature | Figure 4 to Figure 5    |
|       | Ground current                         | vs Junction temperature | Figure 6                |
| PSRR  | Power-supply rejection ratio           | vs Frequency            | Figure 7 to Figure 10   |
|       | Output spectral noise density          | vs Frequency            | Figure 11 to Figure 14  |
| $Z_O$ | Output impedance                       | vs Frequency            | Figure 15 to Figure 18  |
|       | Dropout voltage                        | vs Temperature          | Figure 19 and Figure 20 |
|       |                                        | vs Input voltage        | Figure 21 and Figure 22 |
|       | Load transient response                |                         | Figure 23 and Figure 24 |
|       | Line transient response ( $V_{OUT1}$ ) |                         | Figure 25               |
|       | Line transient response ( $V_{OUT2}$ ) |                         | Figure 26               |
| $V_O$ | Output voltage                         | vs Time (start-up)      | Figure 27 and Figure 28 |
|       | Equivalent series resistance (ESR)     | vs Output current       | Figure 30 to Figure 33  |

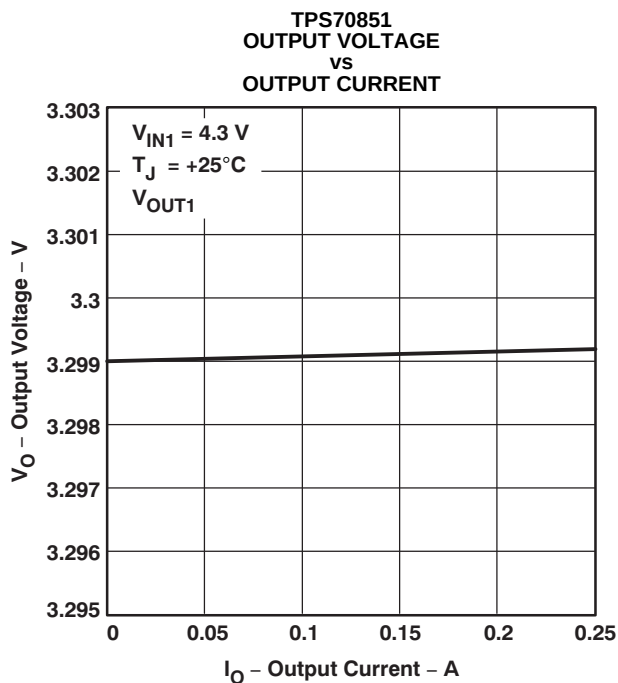


Figure 1.

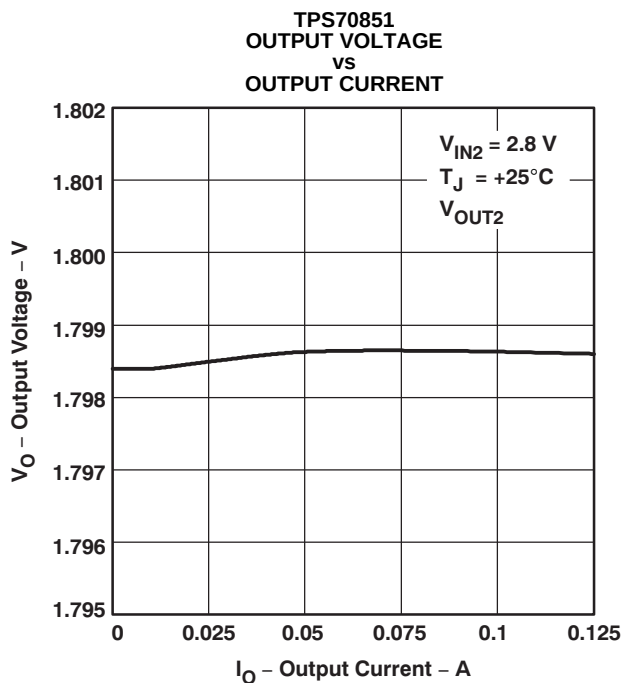
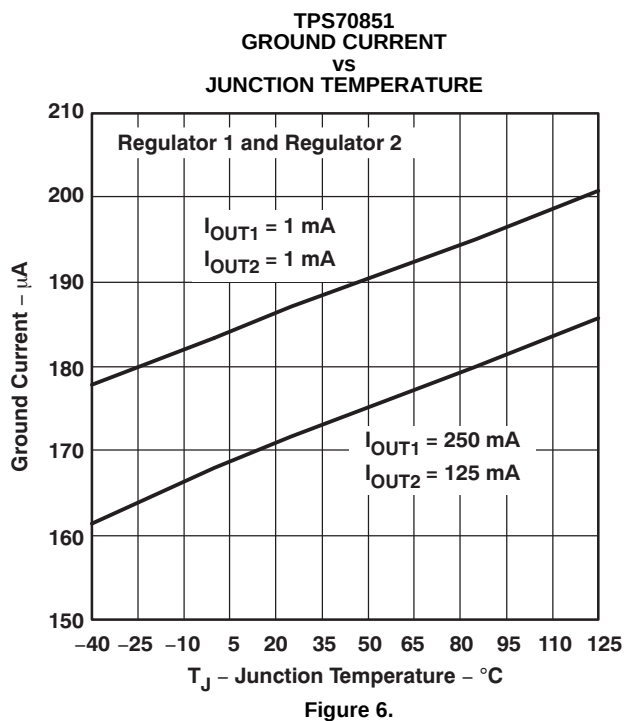
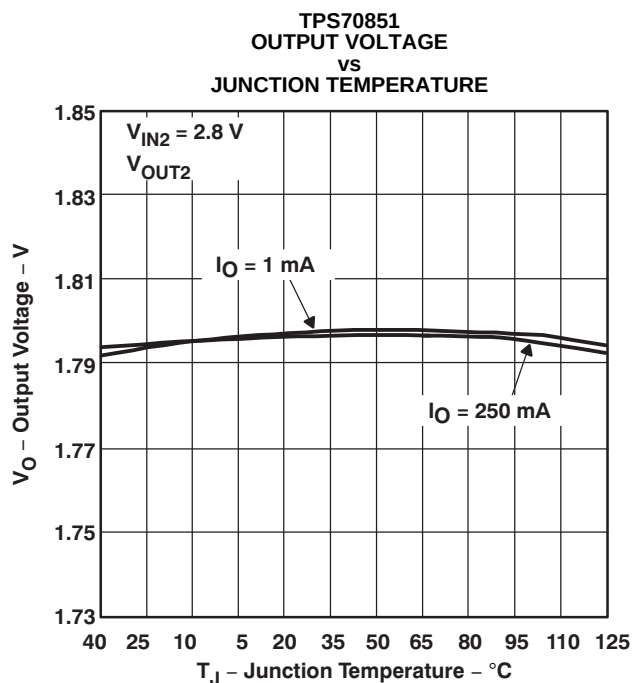
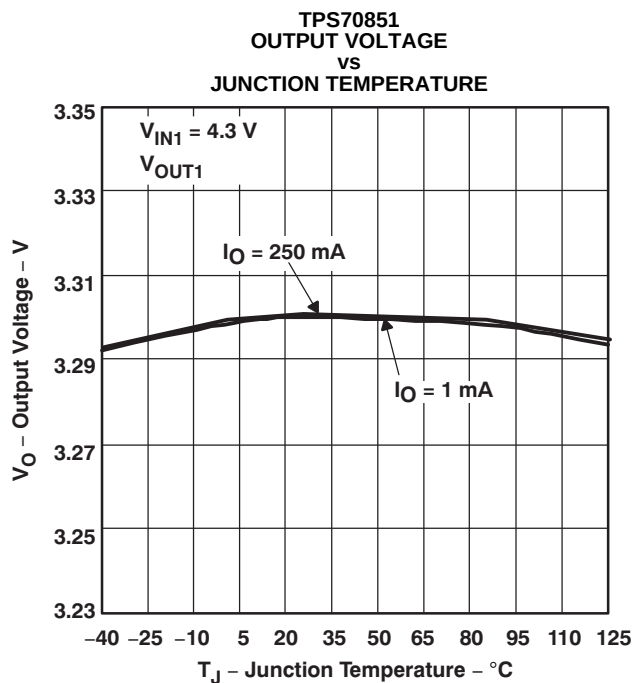
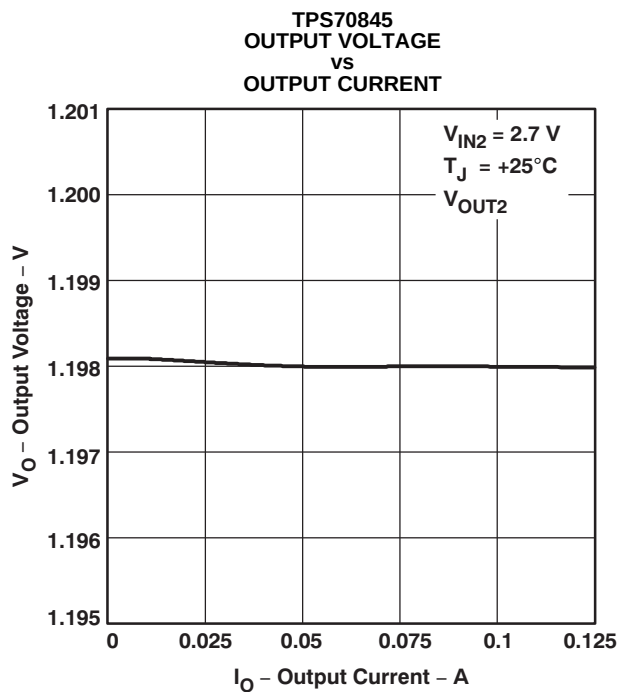


Figure 2.



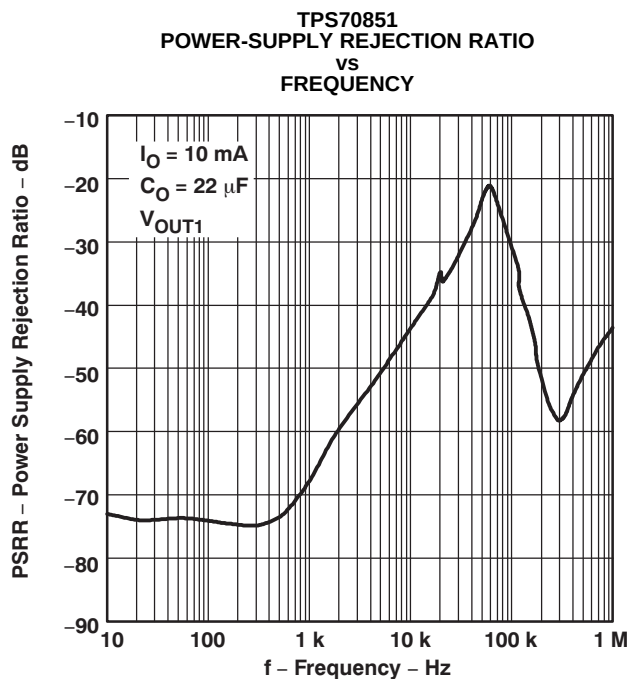


Figure 7.

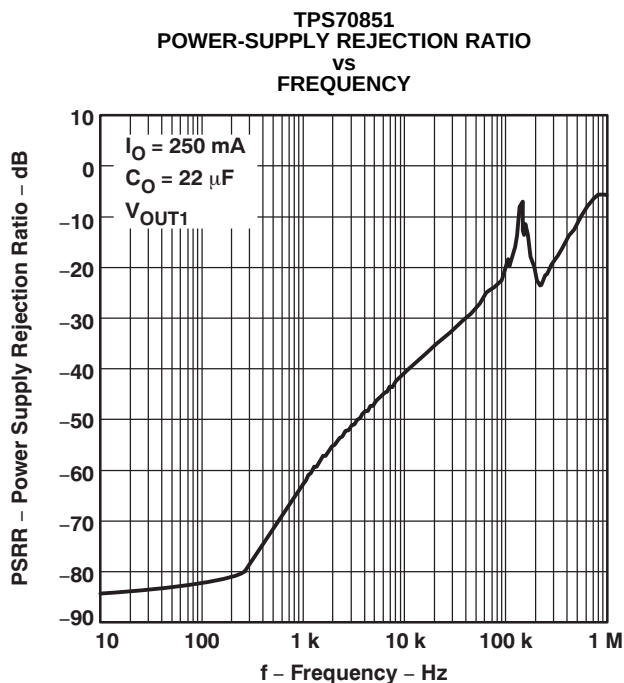


Figure 8.

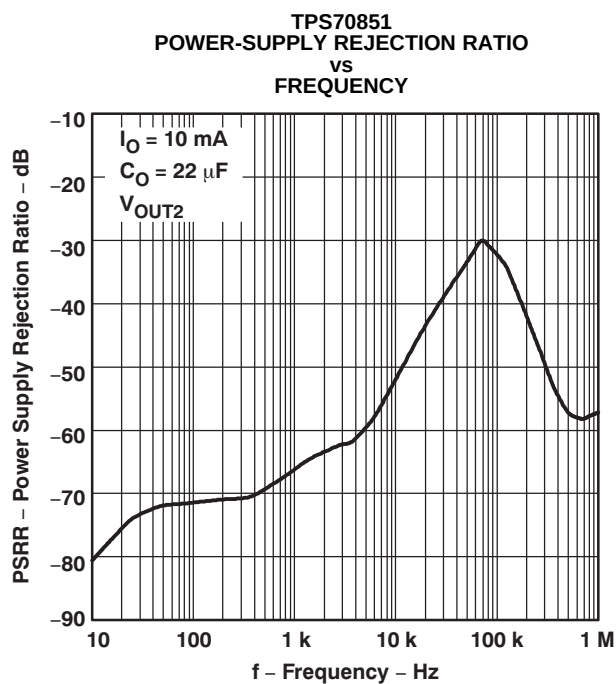


Figure 9.

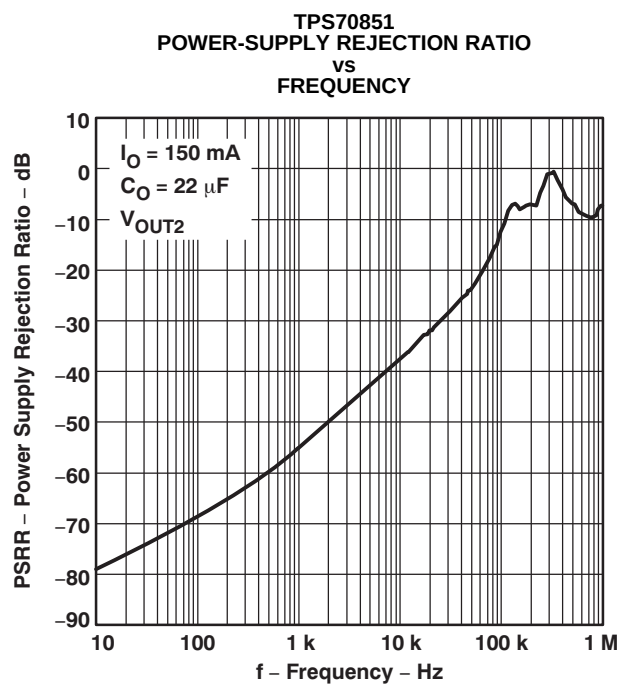


Figure 10.

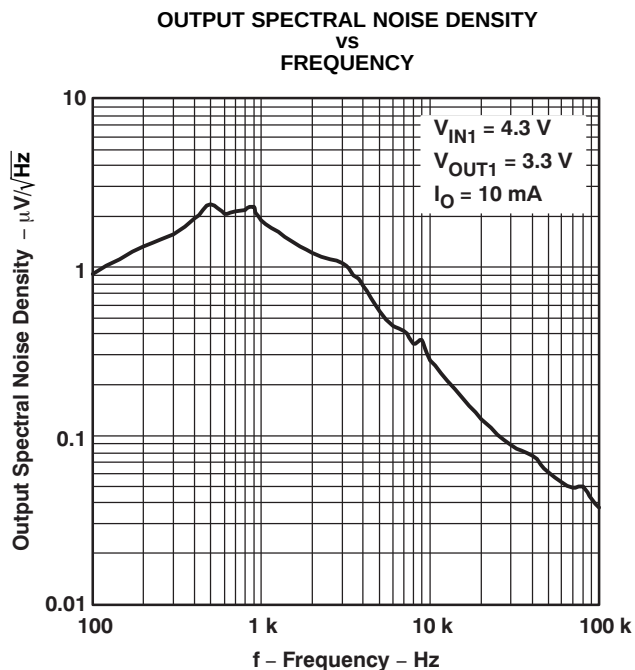


Figure 11.

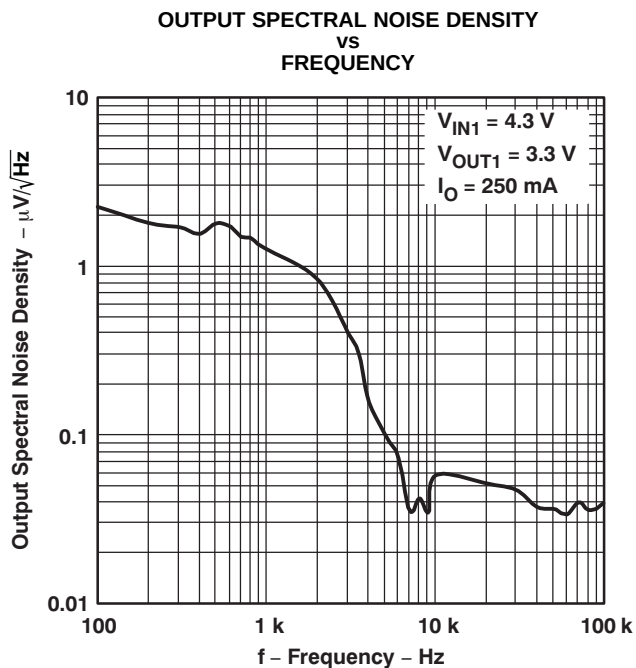


Figure 12.

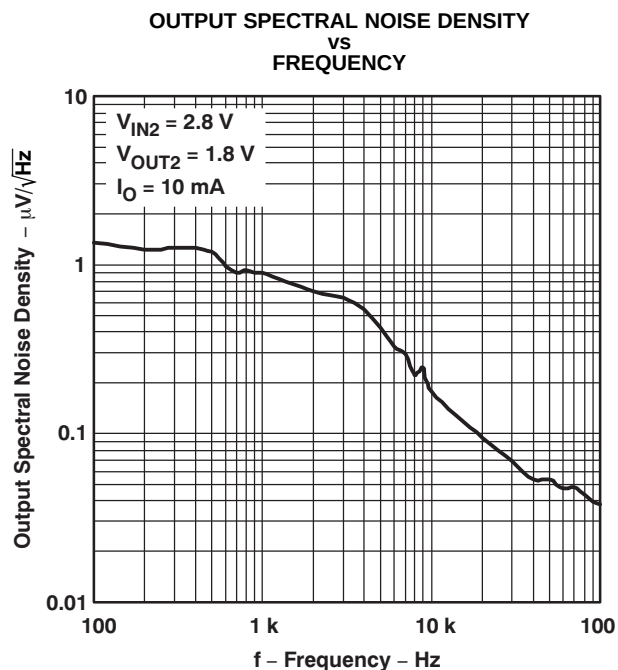


Figure 13.

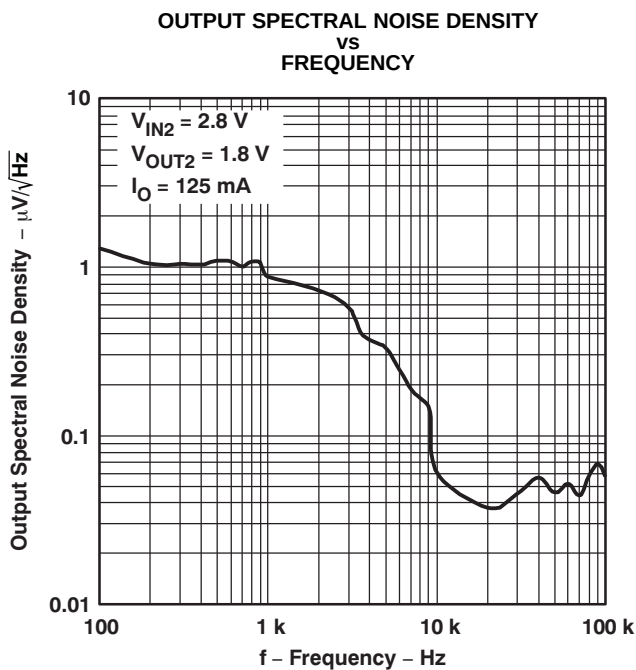


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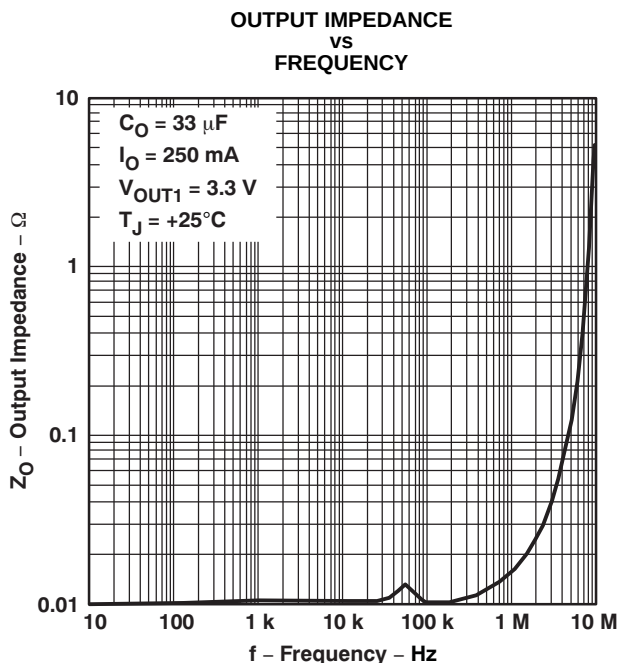


Figure 15.

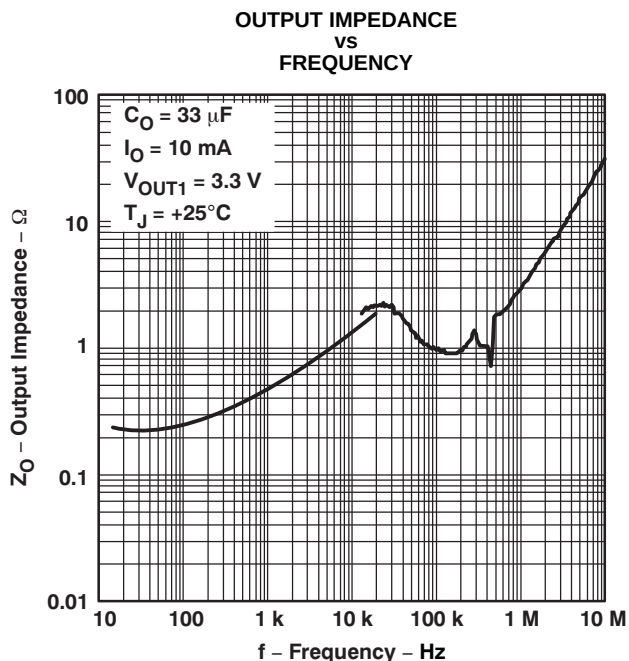


Figure 16.

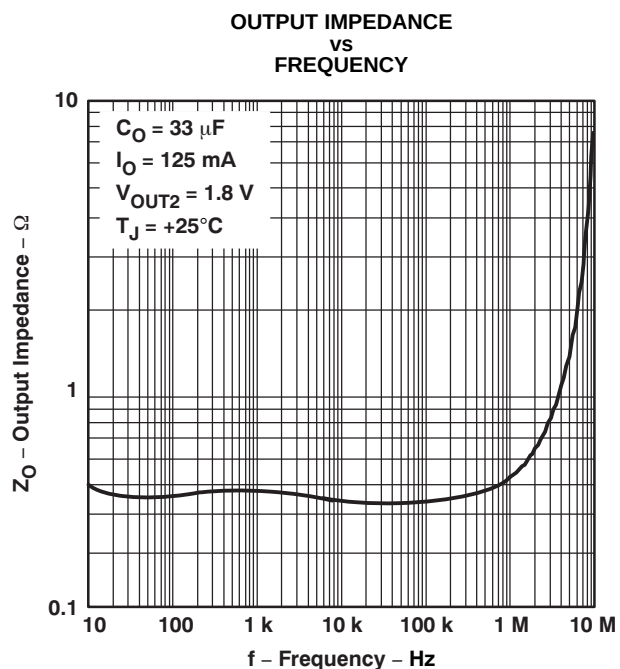


Figure 17.

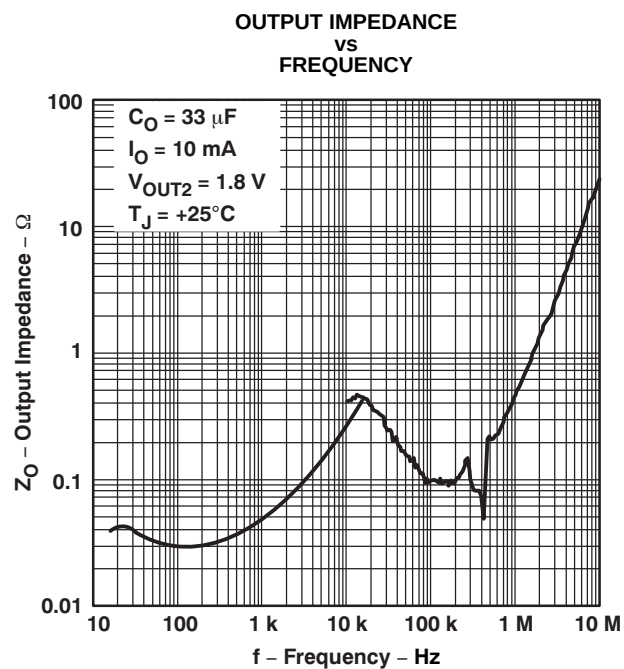


Figure 18.

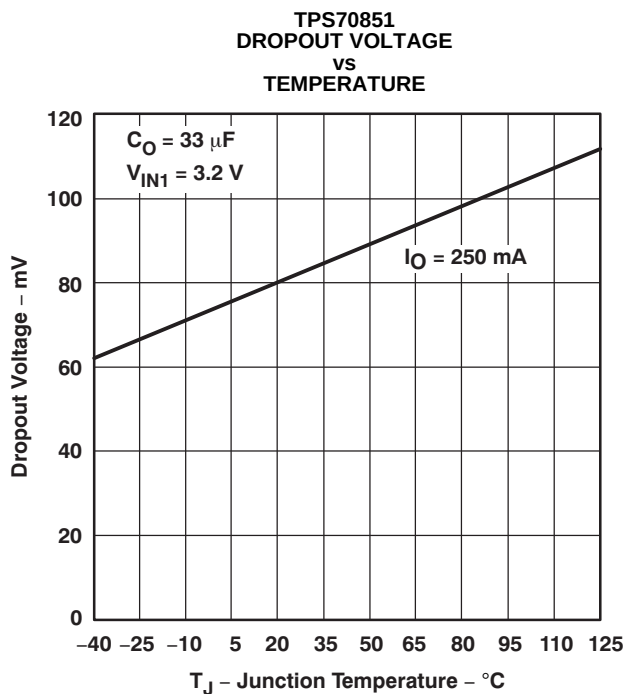


Figure 19.

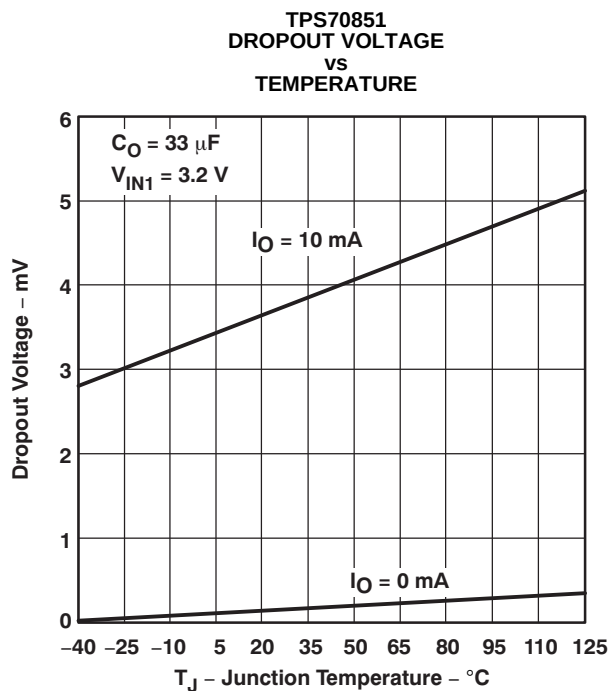


Figure 20.

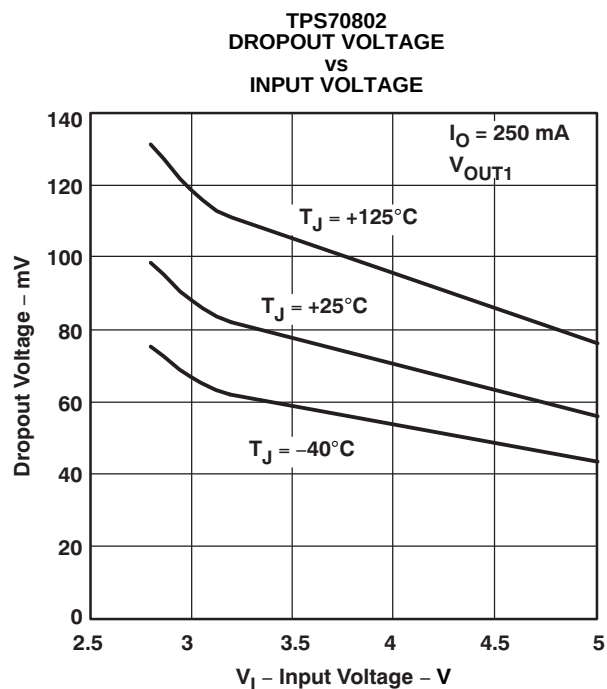


Figure 21.

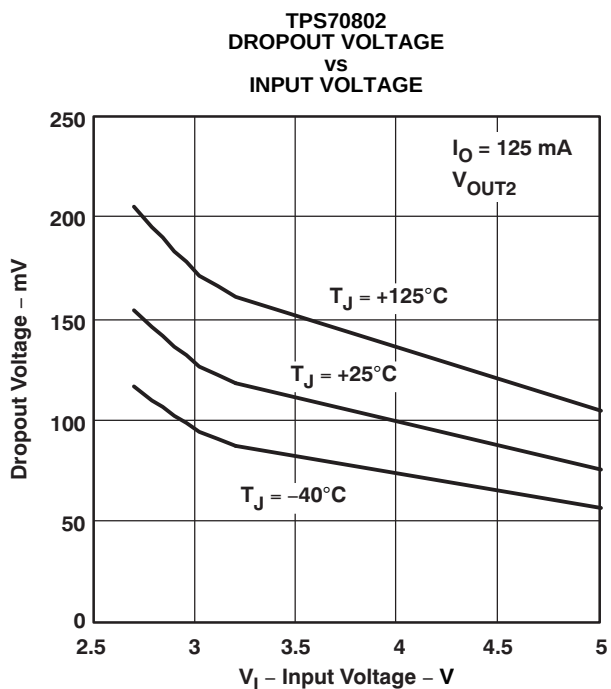


Figure 22.

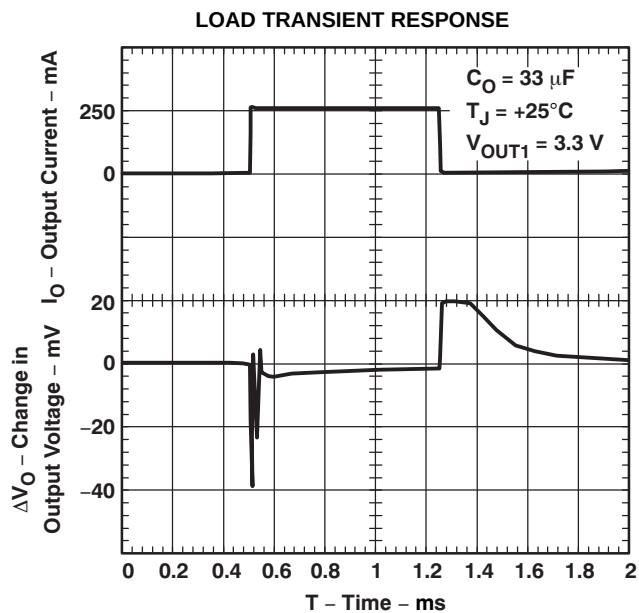


Figure 23.

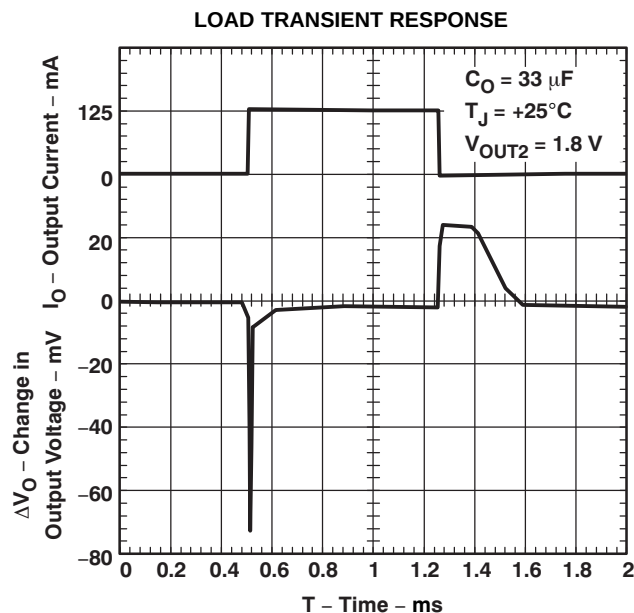


Figure 24.

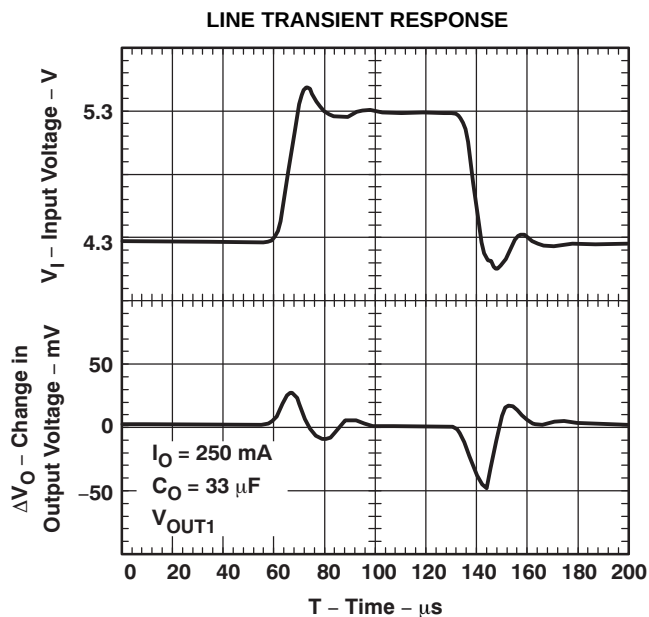


Figure 25.

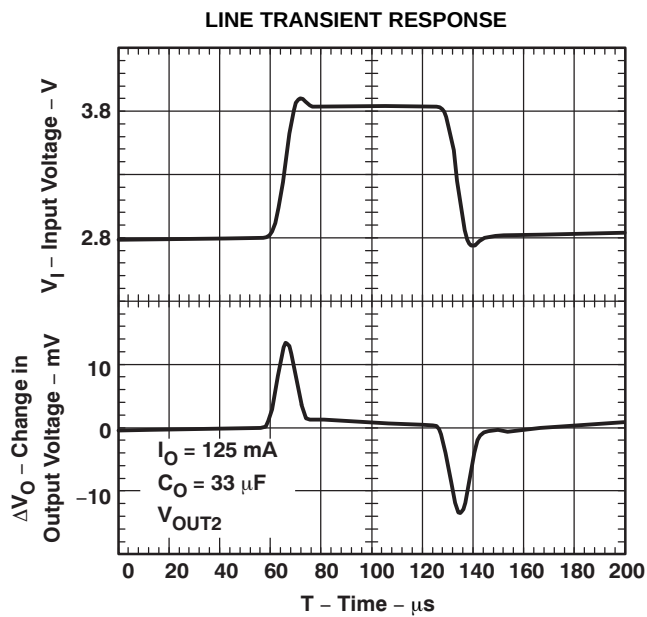


Figure 26.

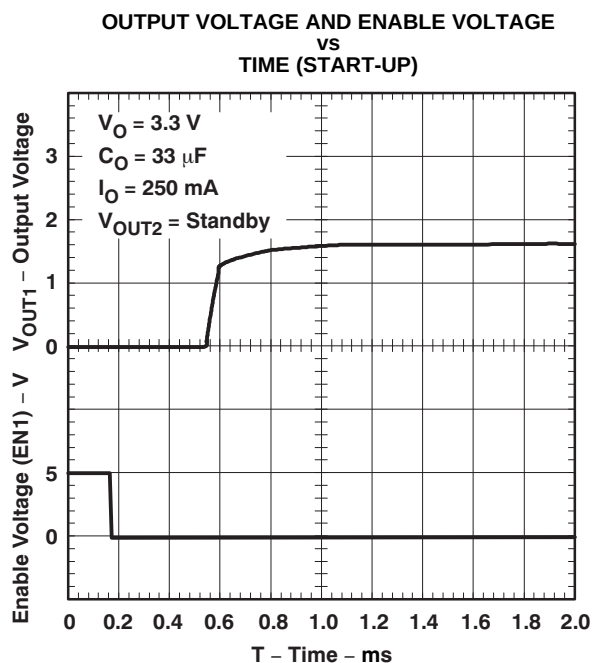


Figure 27.

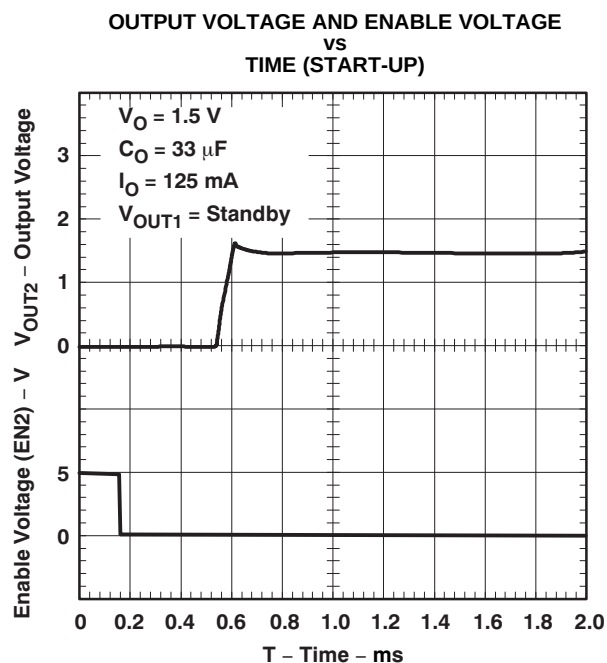


Figure 28.

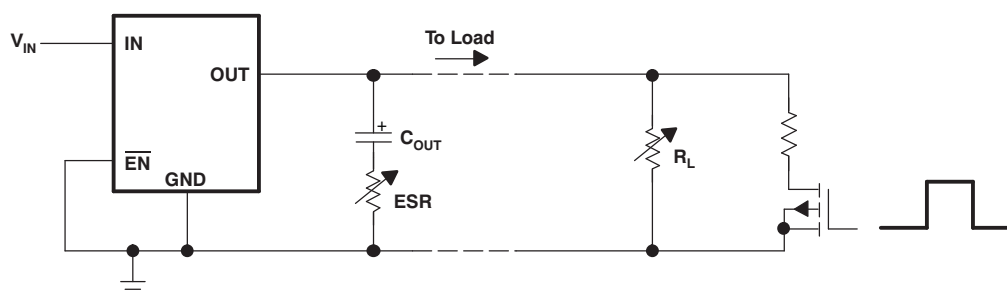


Figure 29. Test Circuit for Typical Regions of Stability

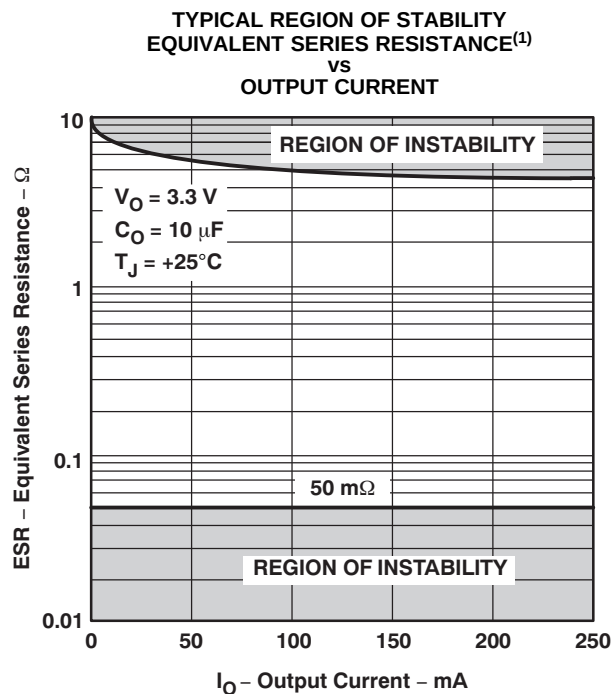


Figure 30.

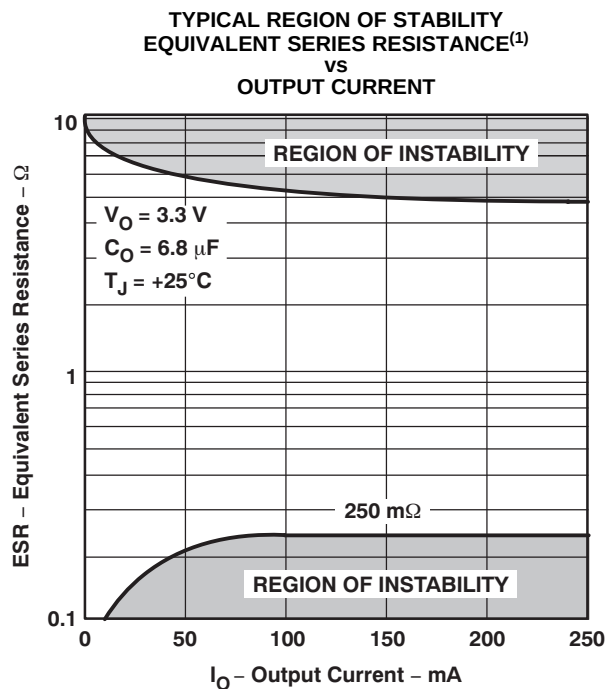


Figure 31.

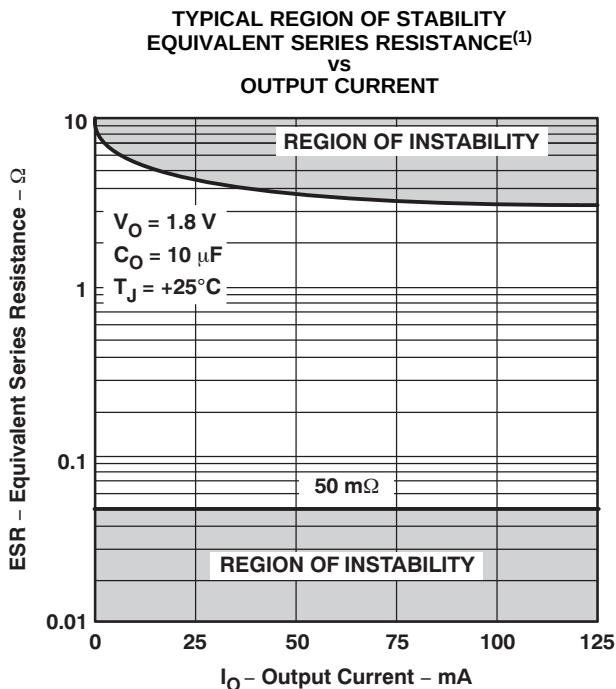


Figure 32.

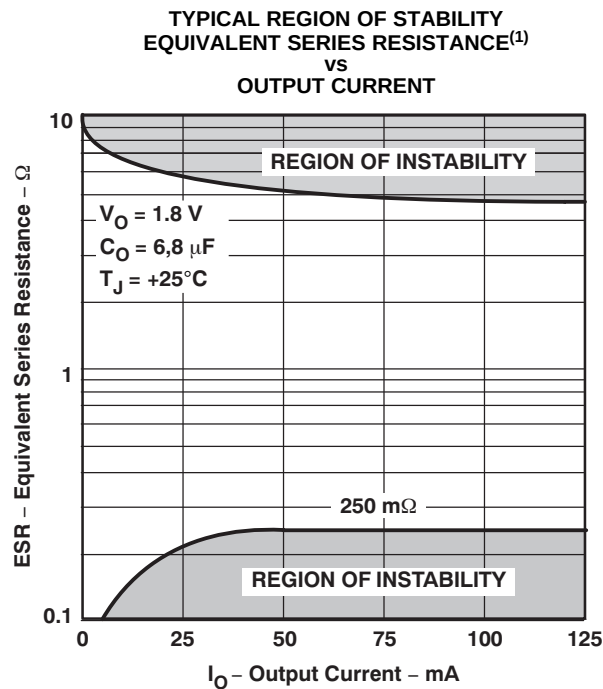


Figure 33.

<sup>(1)</sup> Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

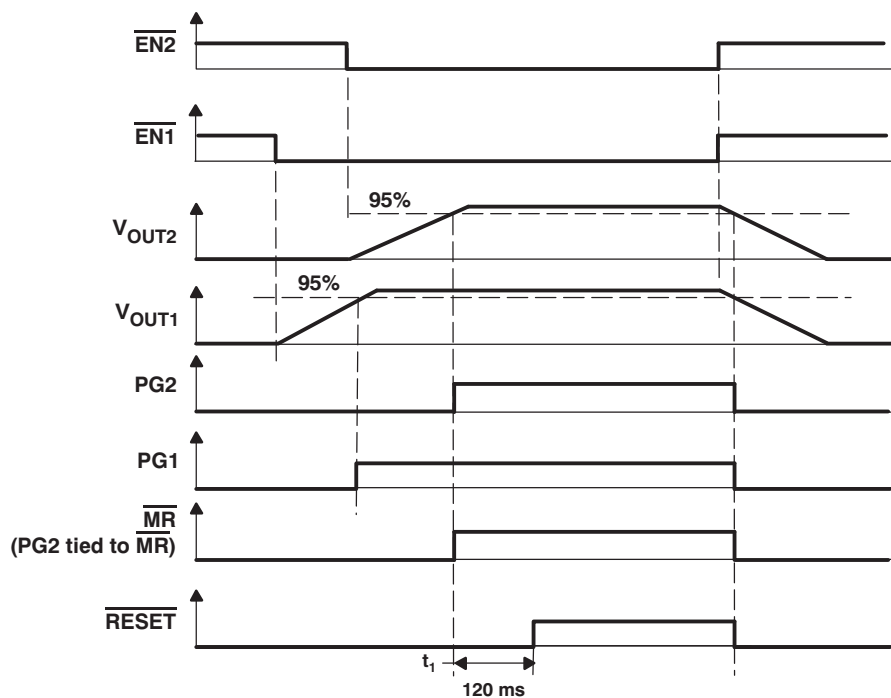
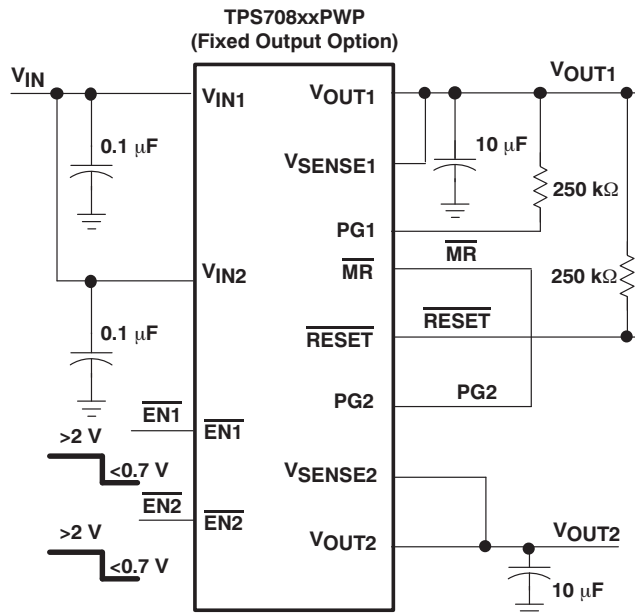
## APPLICATION INFORMATION

### Sequencing Timing Diagrams

This section provides a number of timing diagrams showing how this device functions in different configurations.

**Application condition:**  $V_{IN1}$  and  $V_{IN2}$  are tied to the same fixed input voltage greater than  $V_{UVLO}$ . PG2 is tied to  $\overline{MR}$ .

$\overline{EN1}$  and  $\overline{EN2}$  are initially high; therefore, both regulators are off, and PG1 and PG2 (tied to  $\overline{MR}$ ) are at logic low. Since  $\overline{MR}$  is at logic low,  $\overline{RESET}$  is also at logic low. When  $\overline{EN1}$  is taken to logic low,  $V_{OUT1}$  turns on. Later, when  $\overline{EN2}$  is taken to logic low,  $V_{OUT2}$  turns on. When  $V_{OUT1}$  reaches 95% of its regulated output voltage, PG1 goes to logic high. When  $V_{OUT2}$  reaches 95% of its regulated output voltage, PG2 (tied to  $\overline{MR}$ ) goes to logic high. When  $V_{IN1}$  is greater than  $V_{UVLO}$  and  $\overline{MR}$  (tied to PG2) is at logic high,  $\overline{RESET}$  is pulled to logic high after a 120-ms delay. When  $\overline{EN1}$  and  $\overline{EN2}$  return to logic high, both devices power down and both PG1, PG2 (tied to  $\overline{MR}$ ), and  $\overline{RESET}$  return to logic low.

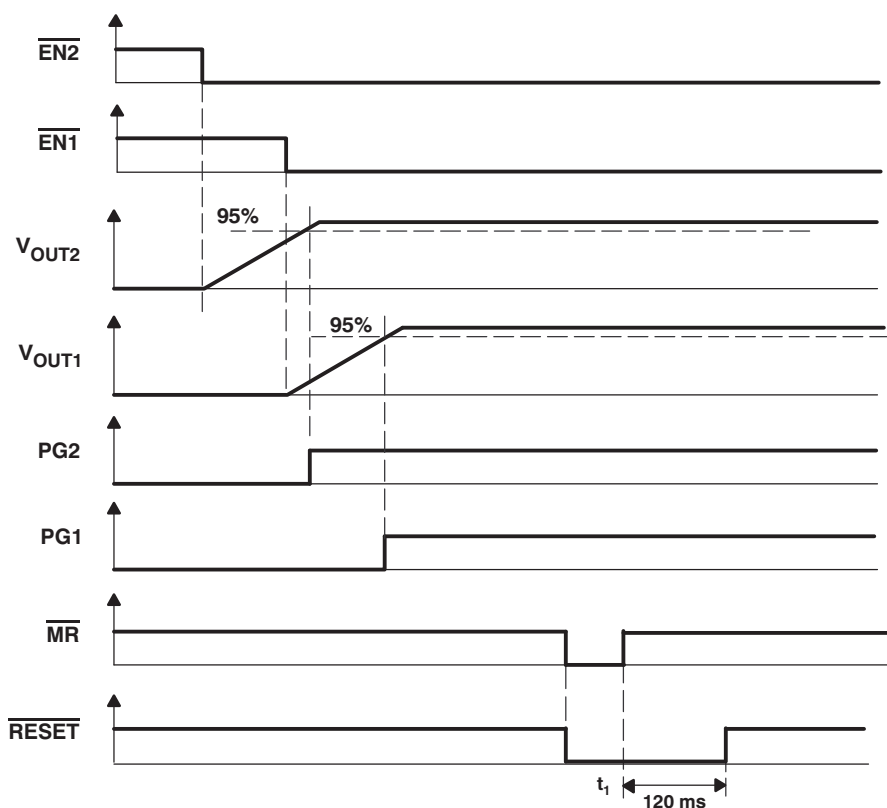
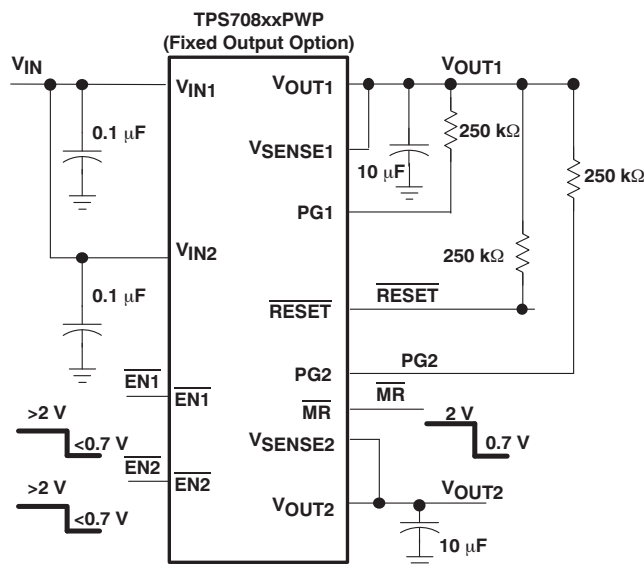


NOTES: A.  $t_1$ : Time at which  $V_{IN}$  is greater than  $V_{UVLO}$  and  $\overline{MR}$  is logic high.  
B. The timing diagram is not drawn to scale.

Figure 34. Timing When  $V_{OUT1}$  Is Enabled Before  $V_{OUT2}$

**Application condition:**  $V_{IN1}$  and  $V_{IN2}$  are tied to the same fixed input voltage greater than  $V_{UVLO}$ .  $\overline{MR}$  is initially logic high but is eventually toggled.

$\overline{EN1}$  and  $\overline{EN2}$  are initially high; therefore, both regulators are off, and PG1 and PG2 are at logic low. Since  $V_{IN1}$  is greater than  $V_{UVLO}$  and  $\overline{MR}$  is at logic high,  $\overline{RESET}$  is also at logic high. When  $\overline{EN2}$  is taken to logic low,  $V_{OUT2}$  turns on. Later, when  $\overline{EN1}$  is taken to logic low,  $V_{OUT1}$  turns on. When  $V_{OUT2}$  reaches 95% of its regulated output voltage, PG2 goes to logic high. When  $V_{OUT1}$  reaches 95% of its regulated output voltage, PG1 goes to logic high. When  $\overline{MR}$  is taken to logic low,  $\overline{RESET}$  is taken low. When  $\overline{MR}$  returns to logic high,  $\overline{RESET}$  returns to logic high after a 120-ms delay.

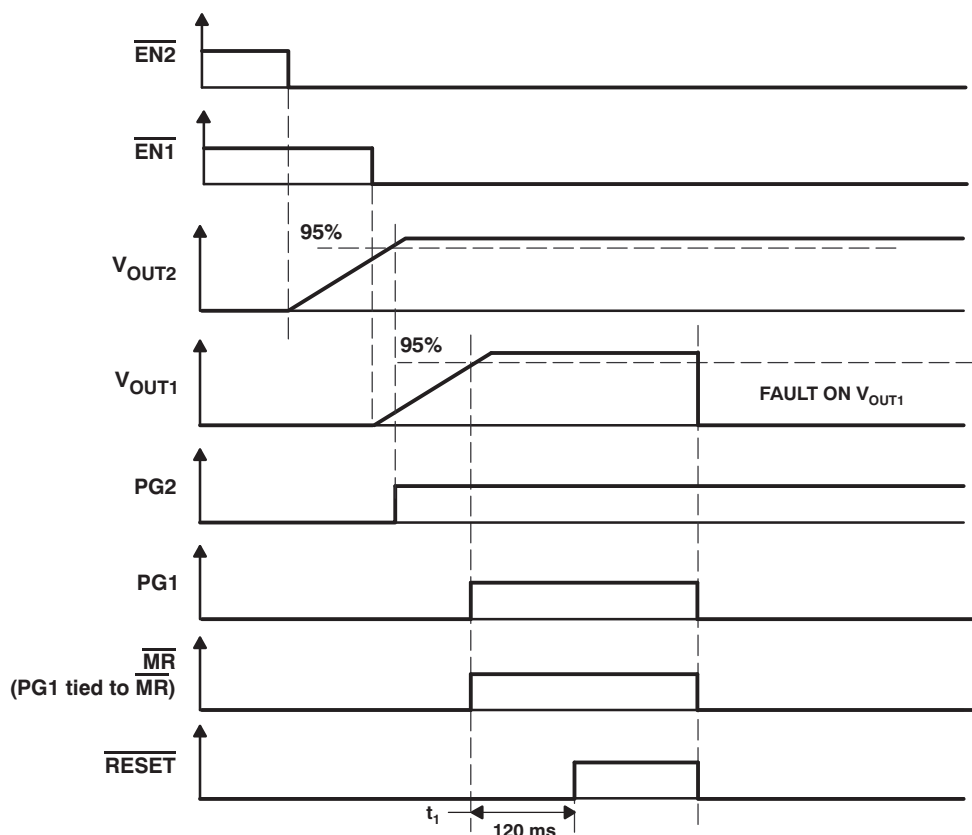
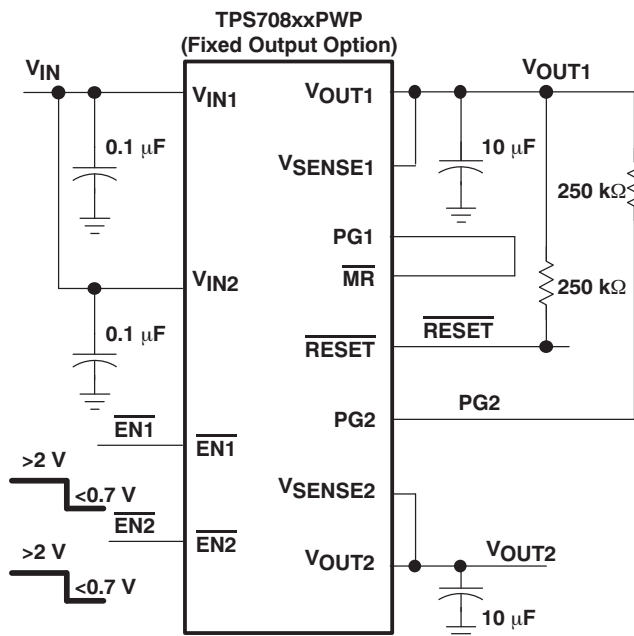


NOTES: A.  $t_1$ : Time at which  $V_{IN}$  is greater than  $V_{UVLO}$  and  $\overline{MR}$  is logic high.  
B. The timing diagram is not drawn to scale.

**Figure 35. Timing When  $\overline{MR}$  is Toggled**

**Application condition:**  $V_{IN1}$  and  $V_{IN2}$  are tied to same fixed input voltage greater than  $V_{UVLO}$ . PG1 is tied to  $\overline{MR}$ .

$\overline{EN1}$  and  $\overline{EN2}$  are initially high; therefore, both regulators are off, and PG1 (tied to  $\overline{MR}$ ) and PG2 are at logic low. Since  $\overline{MR}$  is at logic low,  $\overline{RESET}$  is also at logic low. When  $\overline{EN2}$  is taken to logic low,  $V_{OUT2}$  turns on. Later, when  $\overline{EN1}$  is taken to logic low,  $V_{OUT1}$  turns on. When  $V_{OUT2}$  reaches 95% of its regulated output voltage, PG2 goes to logic high. When  $V_{OUT1}$  reaches 95% of its regulated output voltage, PG1 goes to logic high. When  $V_{IN1}$  is greater than  $V_{UVLO}$  and  $\overline{MR}$  (tied to PG2) is at logic high,  $\overline{RESET}$  is pulled to logic high after a 120-ms delay. When a fault on  $V_{OUT1}$  causes it to fall below 95% of its regulated output voltage, PG1 (tied to  $\overline{MR}$ ) goes to logic low. Since  $\overline{MR}$  is logic low,  $\overline{RESET}$  goes to logic low.  $V_{OUT2}$  is unaffected.



NOTES: A.  $t_1$ : Time at which  $V_{IN}$  is greater than  $V_{UVLO}$  and  $\overline{MR}$  is logic high.  
B. The timing diagram is not drawn to scale.

**Figure 36. Timing When There is a Fault on  $V_{OUT1}$**

## APPLICATION INFORMATION

### Input Capacitor

For a typical application, an input bypass capacitor (0.1  $\mu\text{F}$  to 1  $\mu\text{F}$ ) is recommended. This capacitor will filter any high frequency noise generated in the line. For fast transient conditions where droop at the input of the LDO may occur because of high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor depends on the output current and response time of the main power supply, as well as the distance to the  $V_I$  pins of the LDO.

### Output Capacitor

As with most LDO regulators, the TPS708xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance values are 10- $\mu\text{F}$  ceramic capacitors with an ESR (equivalent series resistance) between 50-m $\Omega$  and 2.5- $\Omega$  or 6.8- $\mu\text{F}$  tantalum capacitors with ESR between 250 m $\Omega$  and 4  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors with capacitance values greater than 10  $\mu\text{F}$  are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. [Table 1](#) gives a partial listing of surface-mount capacitors suitable for use with the TPS708xx for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for user applications. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

**Table 1. Partial Listing of TPS708xx-Compatible Surface-Mount Capacitors**

| VALUE            | MANUFACTURER | MAX ESR        | MFR PART NO.    |
|------------------|--------------|----------------|-----------------|
| 22 $\mu\text{F}$ | Kemet        | 345 m $\Omega$ | 7495C226K0010AS |
| 33 $\mu\text{F}$ | Sanyo        | 100 m $\Omega$ | 10TPA33M        |
| 47 $\mu\text{F}$ | Sanyo        | 100 m $\Omega$ | 6TPA47M         |
| 68 $\mu\text{F}$ | Sanyo        | 45 m $\Omega$  | 10TPC68M        |

## ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called *equivalent series resistance* (ESR), and the inductive impedance is called *equivalent series inductance* (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 37.



Figure 37. ESR and ESL

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

Figure 38 shows the output capacitor and its parasitic resistances in a typical LDO output stage.

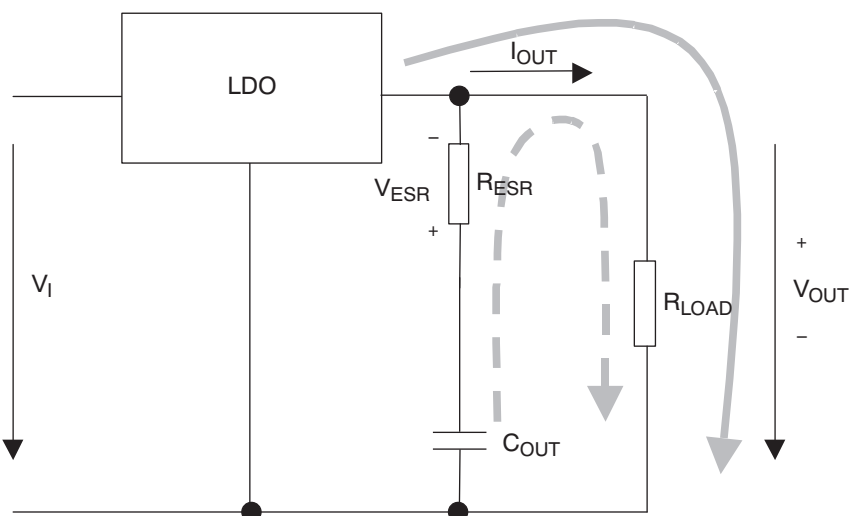
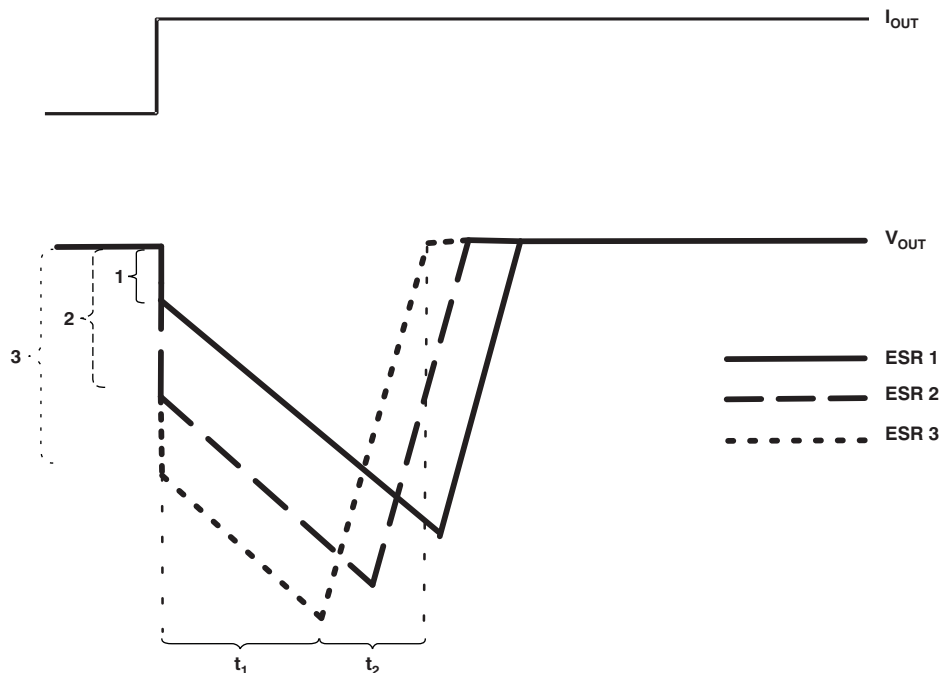


Figure 38. LDO Output Stage with Parasitic Resistances ESR

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ( $V_{(CO)} = V_{OUT}$ ). This condition means no current is flowing into the  $C_O$  branch. If  $I_{OUT}$  suddenly increases (a transient condition), the following results occur:

- The LDO is not able to supply the sudden current need because of its response time. Therefore, capacitor  $C_O$  provides the current for the new load condition (dashed arrow).  $C_O$  now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop occurs at  $R_{ESR}$ . This voltage is shown as  $V_{ESR}$  in Figure 38.
- When  $C_O$  is conducting current to the load, initial voltage at the load will be  $V_O = V_{(CO)} - V_{ESR}$ . As a result of the discharge of  $C_O$ , the output voltage  $V_O$  drops continuously until the response time  $t_1$  of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as  $t_2$  in Figure 39.



**Figure 39. Correlation of Different ESRs and Their Influence on the Regulation of  $V_O$  at a Load Step from Low-to-High Output Current**

Figure 39 also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the greater the voltage droop during the LDO response period.

## Programming the TPS70802 Adjustable LDO Regulator

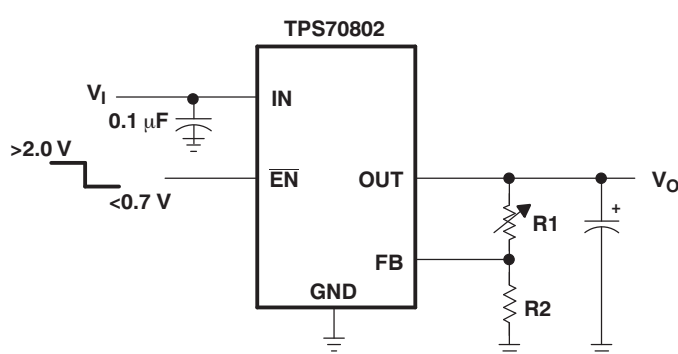
The output voltage of the TPS70802 adjustable regulators is programmed using external resistor dividers as shown in [Figure 40](#).

Resistors R1 and R2 should be chosen for approximately a 50-μA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at the sense terminal increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at approximately 50 μA, and then calculate R1 using [Equation 1](#):

$$R1 = \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (1)$$

where:

- $V_{REF} = 1.224 \text{ V typ}$  (the internal reference voltage)



OUTPUT VOLTAGE  
PROGRAMMING GUIDE

| OUTPUT VOLTAGE | R1   | R2   | UNIT |
|----------------|------|------|------|
| 2.5 V          | 31.6 | 30.1 | kΩ   |
| 3.3 V          | 51.1 | 30.1 | kΩ   |
| 3.6 V          | 59.0 | 30.1 | kΩ   |

Figure 40. TPS70802 Adjustable LDO Regulator Programming

## Regulator Protection

Both TPS708xx PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS708xx also features internal current limiting and thermal protection. During normal operation, the TPS708xx regulator 1 limits output current to approximately 1.6 A (typ) and regulator 2 limits output current to approximately 750 mA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

## Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (2)$$

where:

- $T_{Jmax}$  is the maximum allowable junction temperature
- $R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, that is, 32.6°C/W for the 20-terminal PWP with no airflow.
- $T_A$  is the ambient temperature

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (3)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS70802PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70802             |
| TPS70802PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70802             |
| TPS70802PWPG4                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70802             |
| <a href="#">TPS70845PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70845             |
| TPS70845PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70845             |
| <a href="#">TPS70848PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70848             |
| TPS70848PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70848             |
| <a href="#">TPS70851PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70851             |
| TPS70851PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70851             |
| <a href="#">TPS70851PWPR</a> | Active        | Production           | HTSSOP (PWP)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70851             |
| TPS70851PWPR.A               | Active        | Production           | HTSSOP (PWP)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70851             |
| <a href="#">TPS70858PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70858             |
| TPS70858PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | PT70858             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS70851PWPR | HTSSOP       | PWP             | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS70851PWPR | HTSSOP       | PWP             | 20   | 2000 | 350.0       | 350.0      | 43.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS70802PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70802PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70802PWPG4 | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70845PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70845PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70848PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70848PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70851PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70851PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70858PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| TPS70858PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |

## GENERIC PACKAGE VIEW

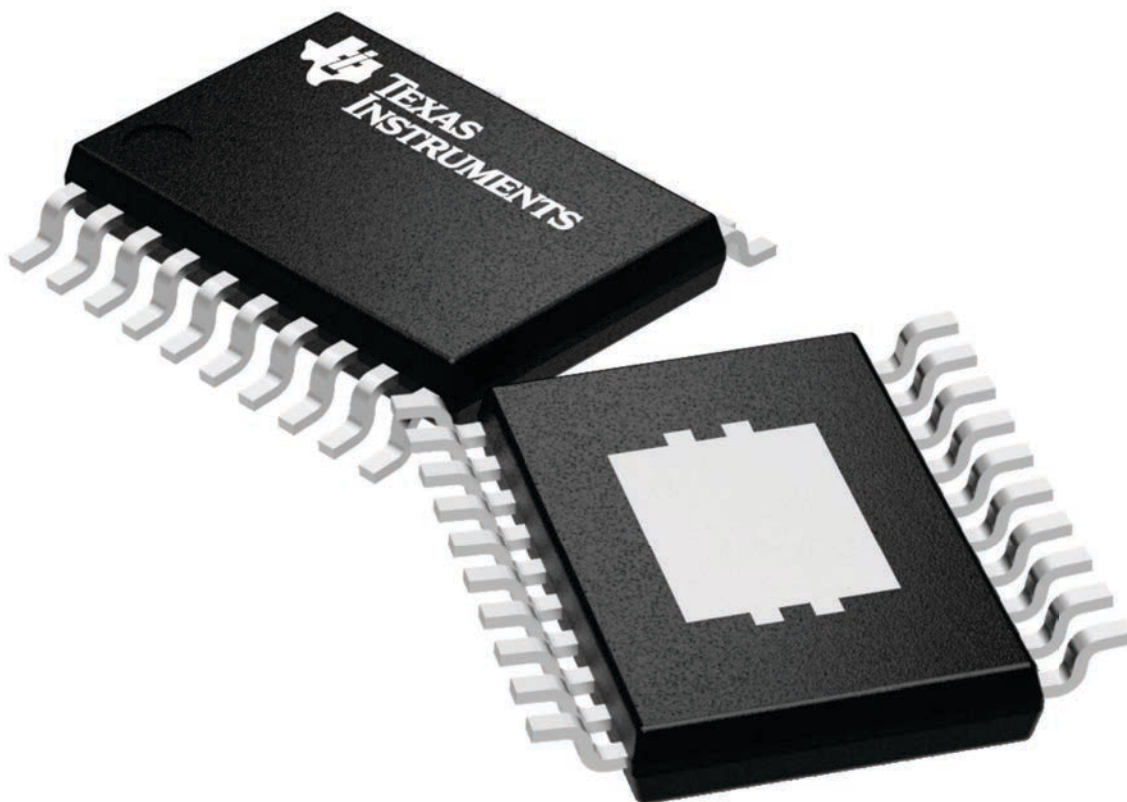
**PWP 20**

**HTSSOP - 1.2 mm max height**

6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224669/A



## PowerPAD™ TSSOP - 1.2 mm max height

Technical drawing of a 20-pin connector. The drawing includes a top view, a side view, and a detail view (Detail A).

**Top View Dimensions:**

- Overall width: 6.6 TYP, 6.2
- Pin pitch: 6.6, 6.4
- Pin 1 Index Area: 4.5, 4.3
- Pin 11 to Pin 20 distance: 11
- Pin 1 to Pin 10 distance: 10
- Pin 11 to Pin 20 distance: 20
- Pin 11 to Pin 20 distance: 18X 0.65
- Pin 11 to Pin 20 distance: 2X 5.85
- Pin 11 to Pin 20 distance: 20X 0.30, 0.17
- Pin 11 to Pin 20 distance: 0.1 (M) C A B

**Side View Dimensions:**

- Seating Plane: 0.1 C
- Pin 11 to Pin 20 distance: 4X (0°-12°)

**Detail A Dimensions:**

- SEE DETAIL A
- (0.15) TYP
- 2X 0.7 MAX NOTE 5
- 2X 0.27 MAX NOTE 5
- Thermal Pad: 2.79, 2.24
- Pin 11 to Pin 20 distance: 1.2 MAX
- Pin 11 to Pin 20 distance: 0.15, 0.05
- Pin 11 to Pin 20 distance: 0.75, 0.50
- Pin 11 to Pin 20 distance: 0.25
- GAGE PLANE
- Pin 11 to Pin 20 distance: 0°-8°

PowerPAD is a trademark of Texas Instruments.

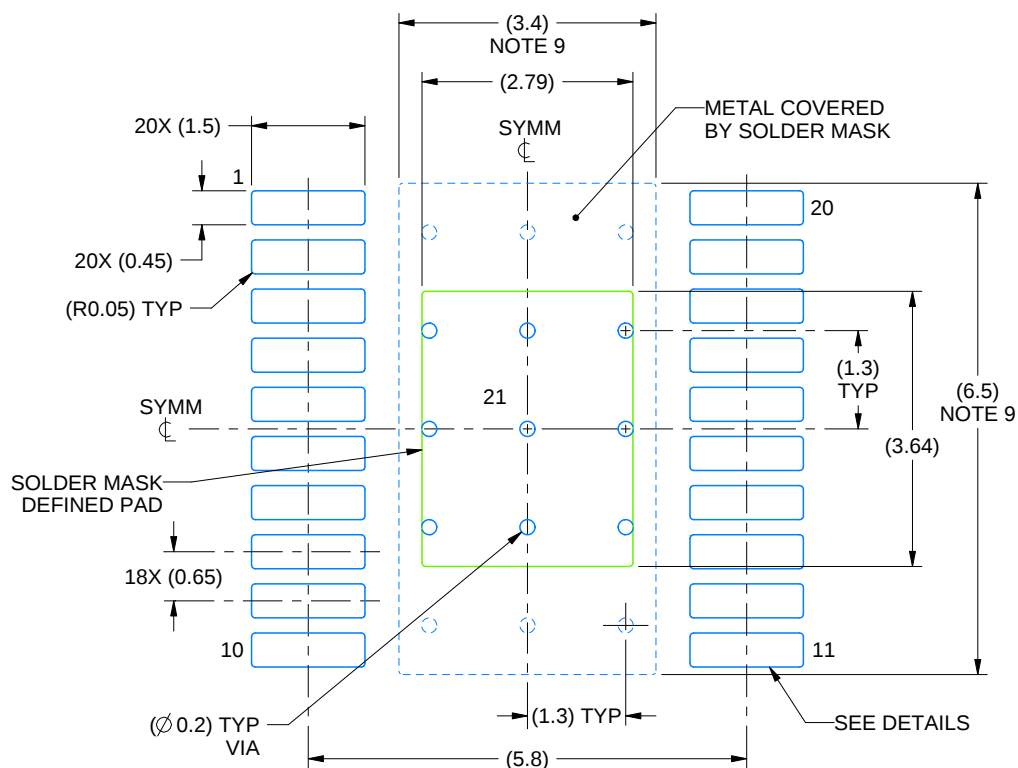
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

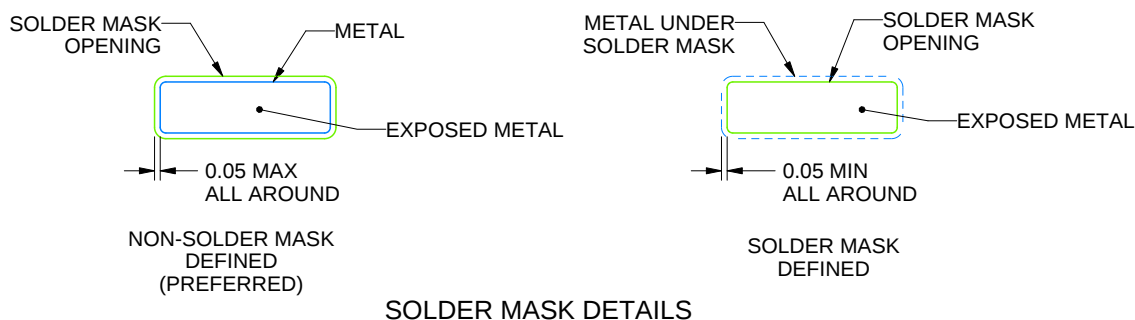
PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4231145/A 08/2024

NOTES: (continued)

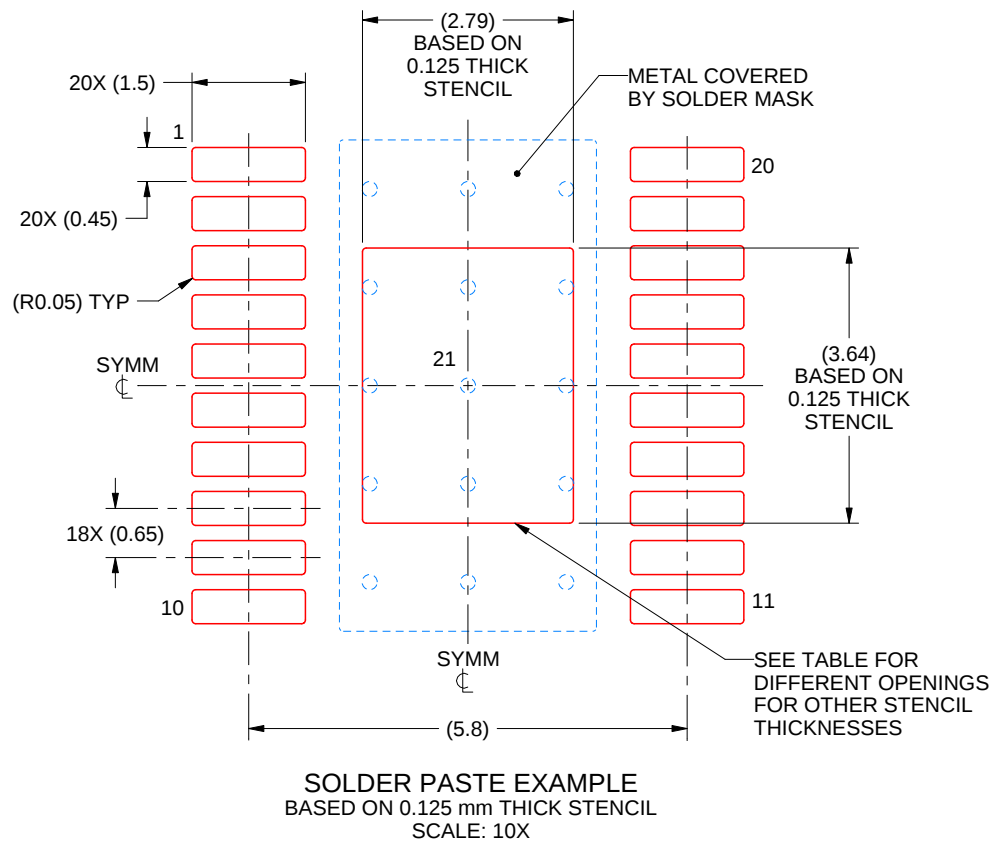
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.12 X 4.07            |
| 0.125             | 2.79 X 3.64 (SHOWN)    |
| 0.15              | 2.55 X 3.32            |
| 0.175             | 2.36 X 3.08            |

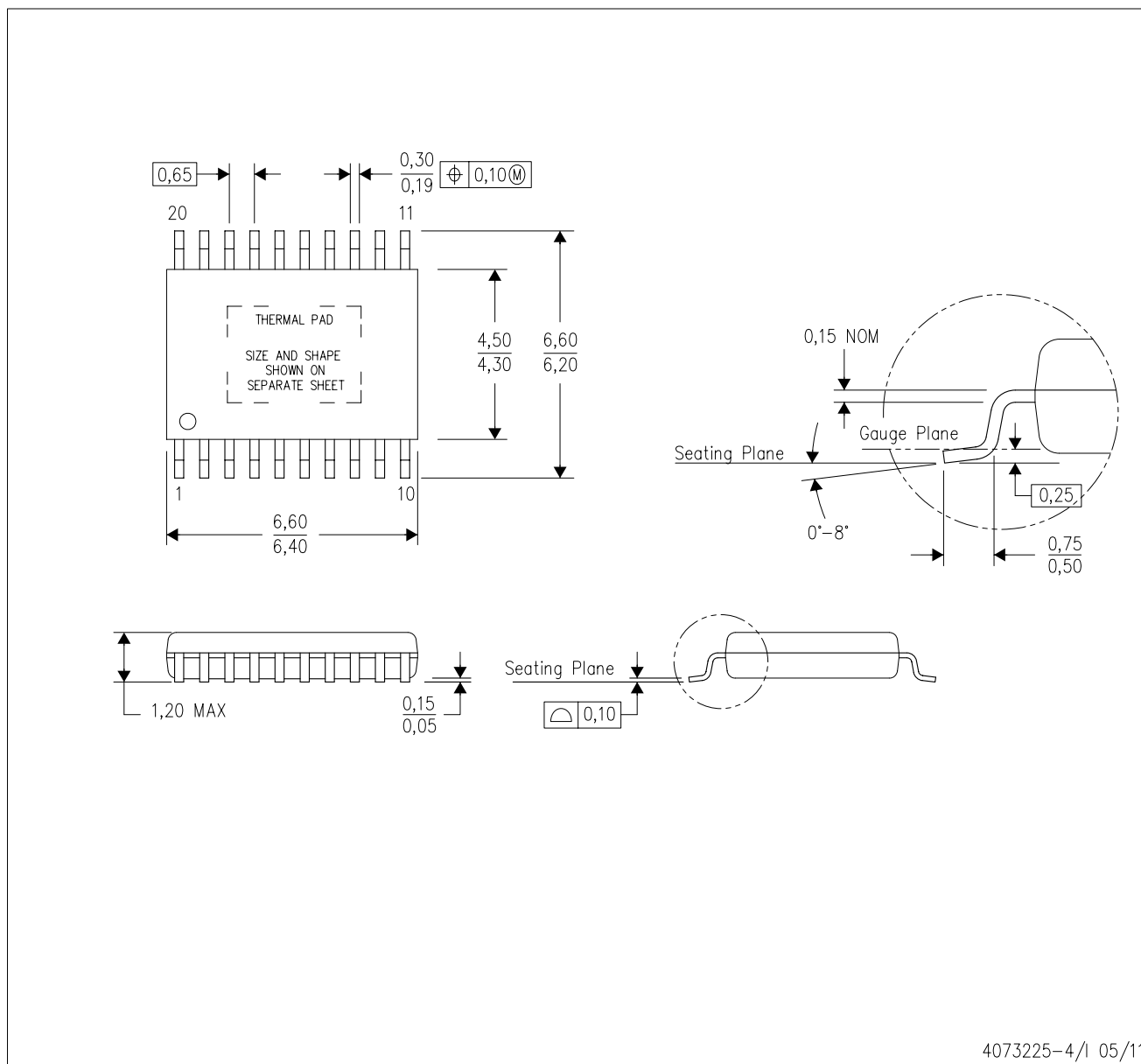
4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

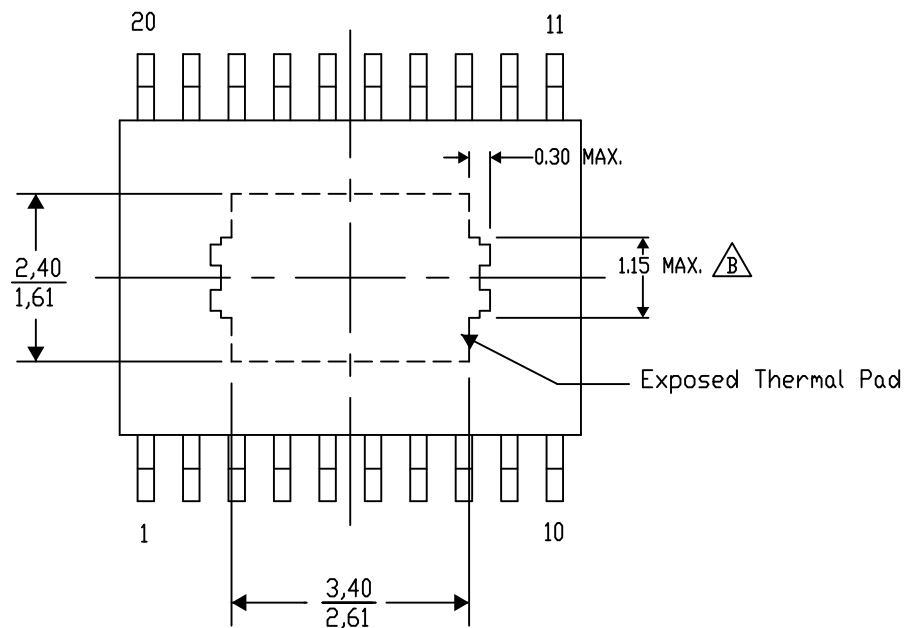
## PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-15/AO 01/16

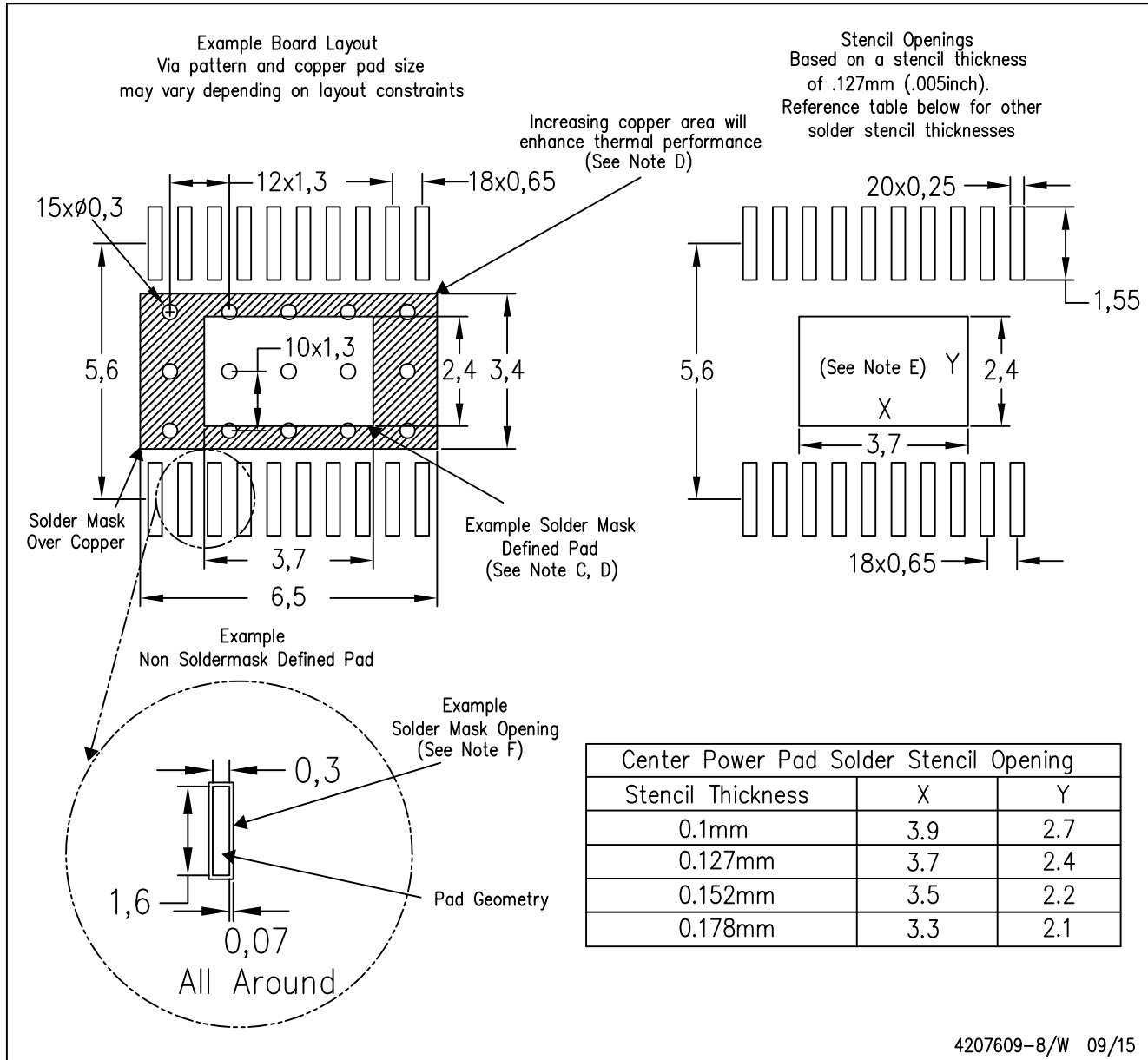
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R-PDSO-G20)

## PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Last updated 10/2025