4.5-V TO 18-V INPUT, HIGH CURRENT, SYNCHRONOUS STEP DOWN THREE BUCK CONVERTER WITH INTEGRATED FET AND DYING GASP STORAGE AND RELEASE CIRCUIT

Check for Samples: TPS65250

FEATURES

- **Wide Input Supply Voltage Range (4.5 V - 18 V)**
- **0.8 V, 1% Accuracy Reference**
- **Continuous Loading: 3 A (Buck 1), 2 A (Buck 2 and 3)**
- **Maximum Current: 3.5 A (Buck 1), 2.5 A (Buck 2 and 3)**
- **Adjustable Switching Frequency 300 kHz - 2.2 MHz Set By External Resistor**
- **External Synchronization Pin for Oscillator**
- **External Enable/Sequencing and Soft Start Pins**
- **Adjustable Current Limit Set By External Resistor**
- **Soft Start Pins**
- **Current-Mode Control With Simple Compensation Circuit**
- **Power Good and Reset Generator**
- **Storage and Release Circuit Optimized for Reduction of Storage Capacitance in Dying Gasp Mode (Option)**
- **Low Power Mode Set By External Signal**
- **QFN Package, 40-Pin 6 mm x 6 mm RHA**

APPLICATIONS

- **xDSL/xPON Modems**
- **Cable Modems**
- **Power Line Modem**
- **Home Gateway and Access Point Networks**
- **Wireless Routers**
- **Set Top Box**

DESCRIPTION/ORDERING INFORMATION

The TPS65250 features three synchronous wide input range high efficiency buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9-, 12- and 15-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and the input supply minus 1 V. Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The COMP pin allows optimizing transient versus dc accuracy response with a simple RC compensation.

The switching frequency of the converters can either be set with an external resistor connected to ROSC pin or can be synchronized to an external clock connected to SYNC pin if needed. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. Both Bucks 2 and Buck 3 run in-phase and 180° out of phase with Buck 1 to minimize input filter requirements.

TPS65250 features a unique storage and release circuitry for dying gasp mode. The storage capacitor is separated from input capacitor during normal operation. The storage and release circuit will charge the storage capacitor with a controlled circuit to reduce the inrush current from the adaptor supply to a storage voltage of 20 V to accumulate as much energy as possible taking advantage of the ½ CV^2 feature.

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TPS65250 continuously monitors the input voltage. Once the input voltage drops below a release voltage of 10.5 V, the circuit tries to transfer charge from storage capacitor to the input capacitor keeping the input voltage closer to release value for as long as possible. The release voltage should be set lower than the processor dying gasp detect voltage. This feature greatly reduces the capacitance required to support the dying gasp operation. The storage and release circuitry is completely on chip except for the charge and storage capacitors. The control circuit makes sure that the current charging the storage capacitor is limited during power up and the storage capacitor is fully charged to its target value before the end of reset (PGOOD pin) flag to the processor is released. The circuit also features a flag signal issued to the host circuit to indicate that the 'dump' stage is in process (GASP pin). This signal can be used to initiate the dying gasp process and reduce the system complexity. During the release process Buck 3 must stay enabled, but Buck 1 and Buck 2 can be disabled to maximize the release time.

TPS65250 features a supervisor circuit that monitors Buck 1 and Buck 3 output voltage and generates an internal power good (PG) signal. The PGOOD pin is asserted once sequencing is done, all PG signals are reported and a selectable end of reset time lapses. The polarity of the PGOOD signal is active high.

TPS65250 also features a low power mode enabled by an external signal, which allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

TPS65250 is packaged in a small, thermally efficient QFN RHA40 package.

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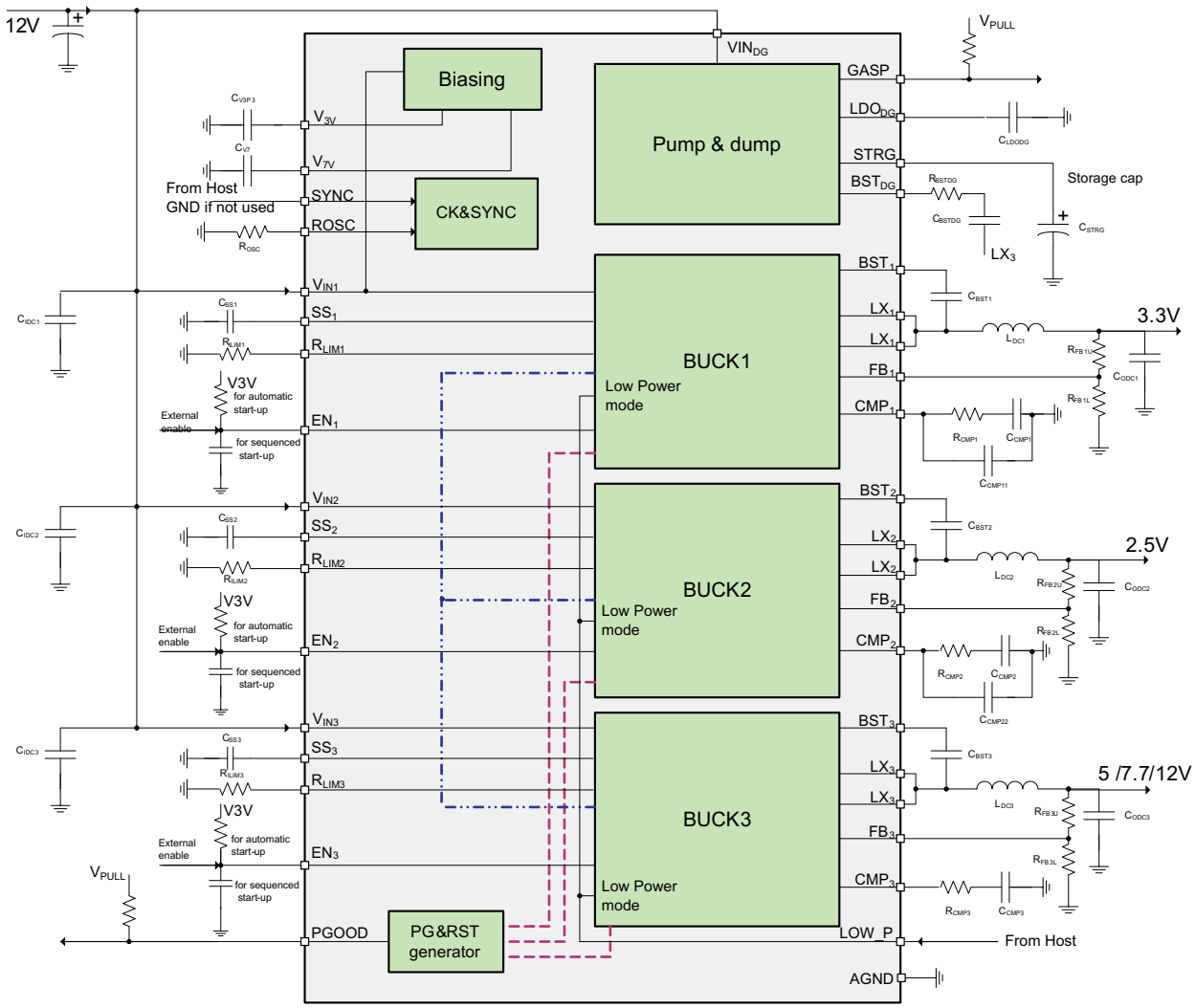
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

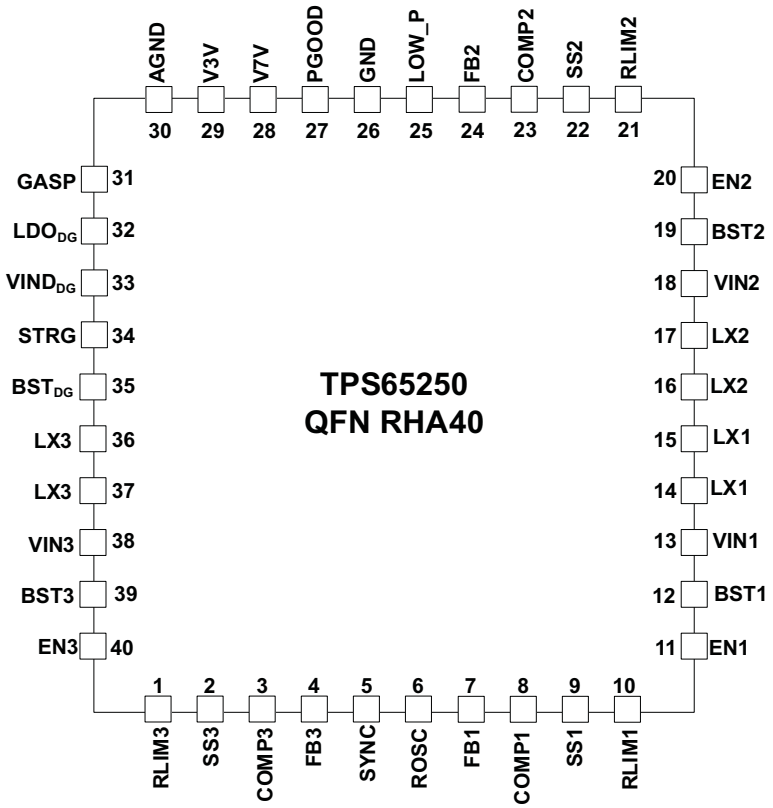


ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	40-pin (QFN) - RHA	Reel of 2500	TPS65250RHAR	TPS65250
		Reel of 250	TPS65250RHAT	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN OUT



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TERMINAL FUNCTIONS (DCA)

NAME	NO.	I/O	DESCRIPTION
RLIM3	1	I	Current limit setting for Buck 3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft start pin for Buck 3. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP3	3	O	Compensation for Buck 3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback input for Buck 3. Connect a divider set to 0.8V from the output of the converter to ground.
SYNC	5	I	Synchronous clock input. If there is a sync clock in the system, connect to the pin. When not used connect to GND.
ROSC	6	I	Oscillator set. This resistor sets the frequency of internal autonomous clock. If there is no synchronous clock, the operating frequency of the regulators is set to the internal autonomous clock. If external synchronization is used resistor should be fitted and set to ~70% of external clock frequency.
FB1	7	I	Feedback pin for Buck 1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft start pin for Buck 1. Fit a small ceramic capacitor to this pin to set the converter soft start time.
RLIM1	10	I	Current limit setting pin for Buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck 1. A low level signal on this pin disables it. If pin is left open a weak internal pull-up to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	12	I	Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck 1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	14, 15	O	Switching node for Buck 1
LX2	16, 17	O	Switching node for Buck 2
VIN2	18	I	Input supply for Buck 2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	19	I	Bootstrap capacitor for Buck 2. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	20	I	Enable pin for Buck 2. A low level signal on this pin disables it. If pin is left open a weak internal pull-up to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting for Buck 2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft start pin for Buck 2. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP2	23	O	Compensation pin for Buck 2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter
FB2	24	I	Feedback input for Buck 2. Connect a divider set to 0.8 V from the output of the converter to ground.
LOW_P	25	I	Low power operation mode(active high) input for TPS65250
GND	26		Ground pin
PGOOD	27	O	Power good. Open drain output asserted after all converters are sequenced and within regulation. Polarity is factory selectable (active high default).
V7V	28	O	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
AGND	30		Analog ground. Connect all GND pins and the power pad together.

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TERMINAL FUNCTIONS (DCA) (continued)

NAME	NO.	I/O	DESCRIPTION
GASP	31	O	Open drain output to signal dying gasp operation to host (active low).
LDO_{DG}	32	O	Dying gaps 18-V supply output. Decouple with a 10-µF, 25-V ceramic capacitor.
VIN_{DG}	33	I	Dying gasp circuit connection to input supply. Fit a 10-µF ceramic capacitor close to this pin.
STRG	34	O	Reservoir capacitor for dying gasps "storage and release" operation.
BST_{DG}	35	I	Bootstrap capacitor for dying gasp circuit. Fit a ceramic capacitor from this pin to the switching node of Buck 3.
LX3	36, 37	O	Switching node for Buck 3
VIN3	38		Input supply for Buck 3. Fit a 10-µF ceramic capacitor close to this pin.
BST3	39	I	Bootstrap capacitor for Buck 3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck 3. A low level signal on this pin disables it. If pin is left open a weak internal pull-up to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
PAD			Power pad. Connect to ground.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

	Voltage range at STRG	–0.3 to 30	V
	Voltage range at VIN1,VIN2, VIN3, VINDG, LDODG, LX1, LX2, LX3	–0.3 to 18	V
	Voltage range at LX1, LX2, LX3 (maximum withstand voltage transient < 10 ns)	–1 to 18	V
	Voltage at BST1, BST2, BST3, BSTDG, referenced to Lx pin	–0.3 to 7	V
	Voltage at V7V, COMP1, COMP2, COMP3	–0.3 to 7	V
	Voltage at V3V, RLIM1, RLIM2, RLIM3, EN1,EN2,EN3, SS1, SS2,SS3, FB1, FB2, FB3, PGOOD, GASP, SYNC, ROSC, LOW_P	–0.3 to 3.6	V
	Voltage at AGND, GND	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_J	Junction temperature	–40		125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM) all pins but LDO_{DG}	2000		V
Human body model, LDO_{DG}	1000		V
Charge device model (CDM), VIN_{DG}	500		V

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 55°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
RHA	30	3.33	2.30	1.33

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x .6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, T_J = –40°C to 125°C, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		18	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		1.3		mA
IDD_Q	Quiescent, low power disabled (Lo)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		20		mA
$IDD_{Q_LOW_P}$	Quiescent, low power enabled (Hi)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		1.5		mA
$UVLO_{VIN}$	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V3V	Internal biasing supply			3.3		V
V7V	Internal biasing supply			6.25		V
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT START, SWITCHING FREQUENCY AND SYNC CIRCUIT, LOW POWER MODE)						
VIH	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENX} rising	1.55			V
	Enable high level	V3p3 = 3.2 V - 3.4 V	0.66 x V_{3p3}			
VIL	Enable threshold Low	V3p3 = 3.2 V - 3.4 V, V_{ENX} falling			1.24	V
	Enable low level	V3p3 = 3.2 V - 3.4 V			0.33 x V_{3p3}	
ICH_{EN}	Pull up current enable pin			1.1		µA
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft start pin current source			5		µA

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ELECTRICAL CHARACTERISTICS (continued)

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, T_J = –40°C to 125°C, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
R_{FSW}	Frequency setting resistor	Depending on set frequency	50		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	-10		10	%
V_{SYNCH}	External clock threshold high	V3p3 = 3.3 V	1.55			V
V_{SYNCL}	External clock threshold low	V3p3 = 3.3 V			1.24	V
$SYNC_{RANGE}$	Synchronization range		0.2		2.2	MHz
$SYNC_{CLK_MIN}$	Sync signal minimum duty cycle		40			%
$SYNC_{CLK_MAX}$	Sync signal maximum duty cycle				60	%
VIH_{LOW_P}	Low power mode threshold high	V3p3 = 3.3 V, V_{ENX} rising	1.55			V
VIL_{LOW_P}	Low power mode threshold Low	V3p3 = 3.3 V, V_{ENX} falling			1.24	V
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12 V , T_J = 25°C	-1%	0.8	1%	V
		V_{IN} = 4.5 to 18V	-2%	0.8	2%	
t_{ON_MIN}	Minimum on time (current sense blanking)			80	120	ns
D	Duty cycle range		5		95	%
$V_{LINEREG}$	Line regulation - DC $\Delta V_{OUT}/\Delta V_{INB}$	V_{INB} = 4.5 V to 18 V, I_{OUT} = 1000 mA		0.5		%/V
$V_{LOADREG}$	Load regulation - DC $\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 % - 90% $I_{OUT,MAX}$		0.5		%/A
C_{OUT}	Output capacitance	Recommended f_{SW} = 1.14 MHz	10	22		µF
L	Nominal Inductance	Recommended f_{SW} = 1.14 MHz		4.7		µH
$R_{DS_ON_HI_BUCK1}$	Turn-On resistance high side Buck 1	V_{IN} = 12 V, T_J = 25°C		95		mΩ
$R_{DS_ON_LO_BUCK1}$	Turn-On resistance low side Buck 1	V_{IN} = 12 V, T_J = 25°C		50		mΩ
$R_{DS_ON_HI_BUCK23}$	Turn-On resistance high side Buck 2 and 3	V_{IN} = 12 V, T_J = 25°C		120		mΩ
$R_{DS_ON_LO_BUCK23}$	Turn-On resistance low side Buck 2 and 3	V_{IN} = 12 V, T_J = 25°C		80		mΩ
$V_{UTTOLTRAN\ 1}$	Transient V_{OUT} variation during load transient measured at feedback point	ΔI = 1 A in Δt =1 µs, C_{LOAD} = 22 µF, ceramic		1.5		%
$V_{UTTOLTRAN\ 2}$	Transient V_{OUT} variation during load transient measured at feedback point	I = 0.75 A in Δt = 1 µs, C_{LOAD} = 22 µF, ceramic		1.5		%
$V_{UTTOLTRAN\ 3}$	Transient V_{OUT} variation during load transient measured at feedback point	I = 0.75 A in Δt = 1 µs, C_{LOAD} = 22 µF, ceramic		1.5		%
I_{LIMIT1}	Peak inductor current limit range		1		4	A
I_{LIMIT2}	Peak inductor current limit range		1		3	A
I_{LIMIT3}	Peak inductor current limit range		1		3	A
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling (device will be disabled after t_{ON_HICCUP})		85		%
		Output rising (PG will be asserted)		90		
$t_{UV_deglitch}$	Deglitch time (both edges)	Each buck		11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		12		ms
t_{OFF_HICCUP}	Hiccup mode OFF time	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		20		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high side fet will be forced off)		109		%
		Output falling (high side fet will be allowed to switch)		107		
t_{RP}	minimum reset period	Measured after the later of Buck1 or Buck 3 power-up successfully		1000		ms
DYING GASP STORAGE AND RELEASE CIRCUIT						
$I_{PRECHARGE_LIMIT}$	Inrush current storage	V_{IN} = 12 V, storage charging from 0 V to V_{IN}		0.1	0.15	A
$I_{STORAGE_LIMIT}$	Current limit for current dumped from storage to VIN	Dump mode. Current flowing from V_{STRG} to V_{IN}		2	3	A

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ELECTRICAL CHARACTERISTICS (continued)

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, T_J = –40°C to 125°C, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LDO_LIMIT}	Pump and dump LDO current limit	V_{IN} = 12 V, maximum charge current supplied by V_{IN}	0.2		0.4	A
$t_{PRECHARGE}$	Time to charge storage capacitor to VIN with IPRECHARGE_LIMIT	V_{IN} = 12 V, $V_{STORAGE}$ = 18 V. R_{BST} = 10 Ω, C_{BST} = 20 nF, $C_{STORAGE}$ = 1000 µF		100		ms
t_{CHARGE}	Time to charge storage capacitor from VIN to final charge value	V_{IN} = 12 V, $V_{STORAGE}$ = 18 V. R_{BST} = 10 Ω, C_{BST} = 20 nF, $C_{STORAGE}$ = 1000 µF		100		ms
$V_{STORAGE}$	Storage Voltage range				30	V
V_{BST_PD}	Bootstrap pin range				30	V
V_{LDOPD}	Pump and dump LDO pin range		0		20	V
V_{LDOPD}	Dying gasp Release voltage	V_{IN} = 9 V to 15 V range	-5%	10.5	5%	V
$V_{STORAGE}$	Dying gasp Storage voltage	Storage voltage must be smaller than ~2V_{IN} - 1.5 V.	-5%	20.1	5%	V
THERMAL SHUTDOWN						
T_{TRIP_OTS}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis	Device re-starts when T_J < (T_{TRIP_OTS} - T_{HYST})		20		°C
$T_{TRIP_DEGLITCH}$	Thermal shut down deglitch			110		µs
CURRENT LIMIT PROTECTION						
$RLIM_1$	Limit resistance range Buck 1		75		300	kΩ
$RLIM_{2\&3}$	Limit resistance range Bucks 2 and 3		100		300	kΩ
$ILIM_1$	Buck 1 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 33	1.2		5.5	A
$ILIM_2$	Buck 2 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 34	1		4.1	A
$ILIM_3$	Buck 3 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 35	1.3		4.4	A

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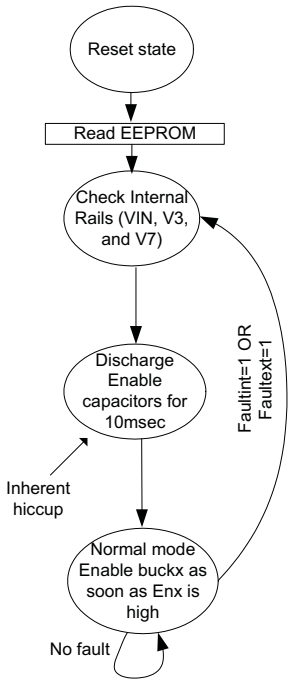
STATE MACHINE



Faultint: Overtemperature, $UVLO_{VIN}$, $V7V_{UVLO}$
Faultext: UV on any buck for more than 10 ms

Figure 1. Normal Operation

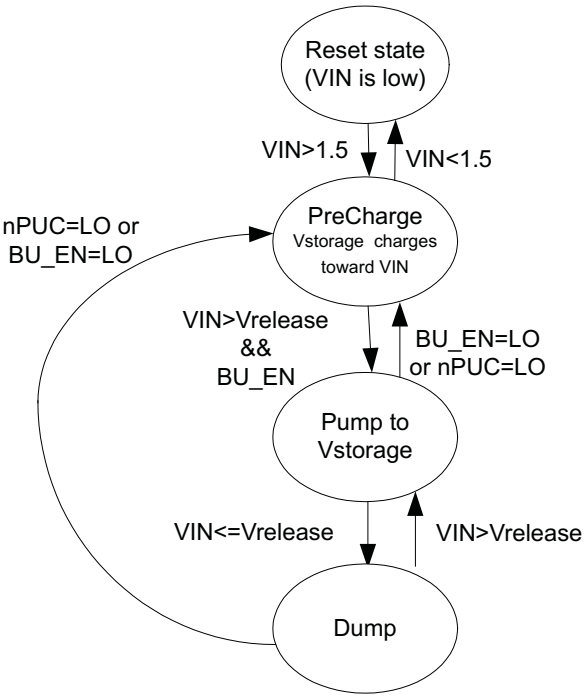


Figure 2. Pump and Dump Mode

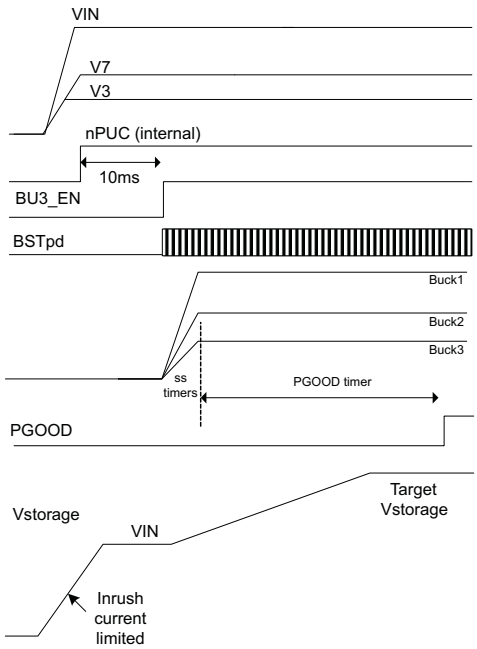


Figure 3. Power-Up Timing (Showing Automatic Start-Up) nPUC Occurs at 3 V

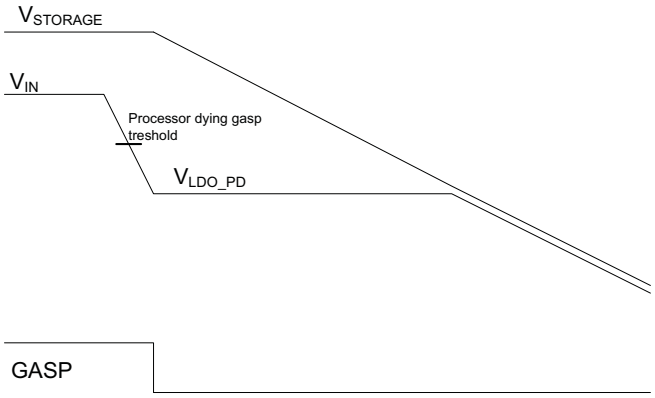


Figure 4. Pump and Dump Timing

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TYPICAL CHARACTERISTICS

Buck 1

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.1 MHz (unless otherwise noted)

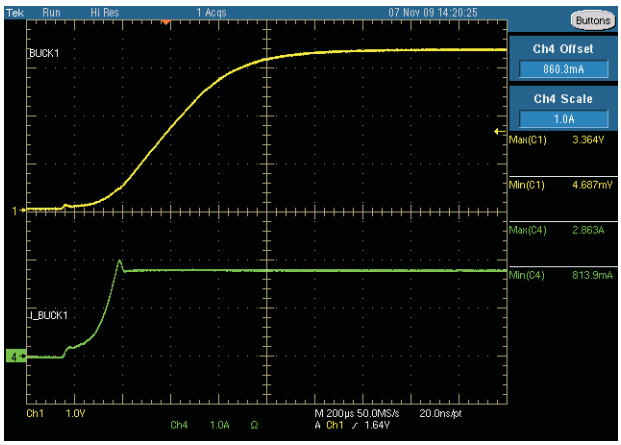

Figure 5. Start-Up
V_{OUT} = 3.3 V, 2 A

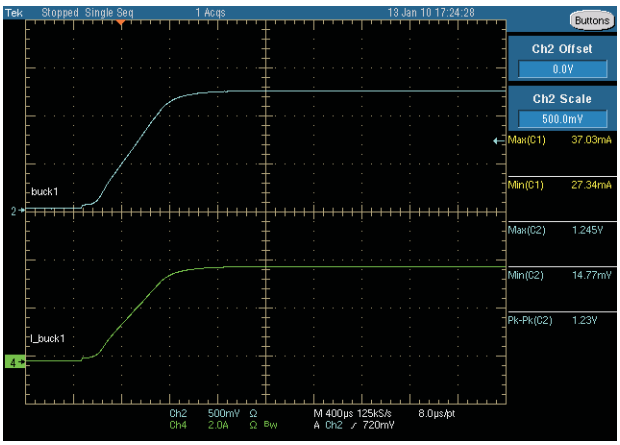

Figure 6. Start-Up
V_{OUT} = 1.2 V, 3.5 A

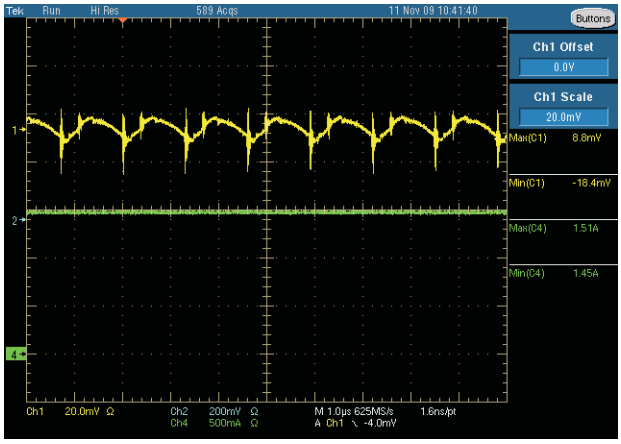

Figure 7. Ripple
V_{OUT} = 3.3 V, 1.5 A, f_{SW} = 1.1 MHz, 20 mV/div

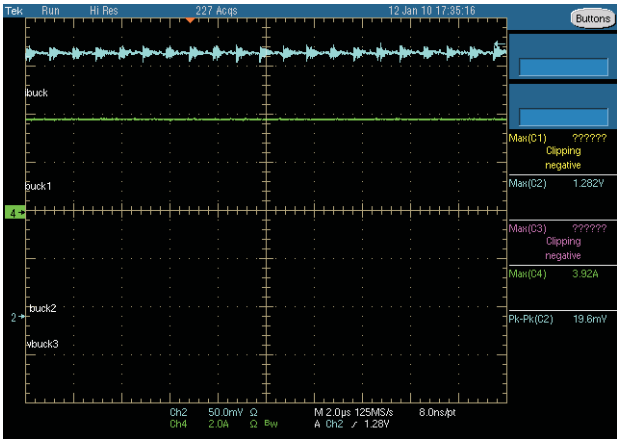

Figure 8. Ripple
V_{OUT} = 1.2 V, 4 A, f_{SW} = 1.1 MHz, 50 mV/div

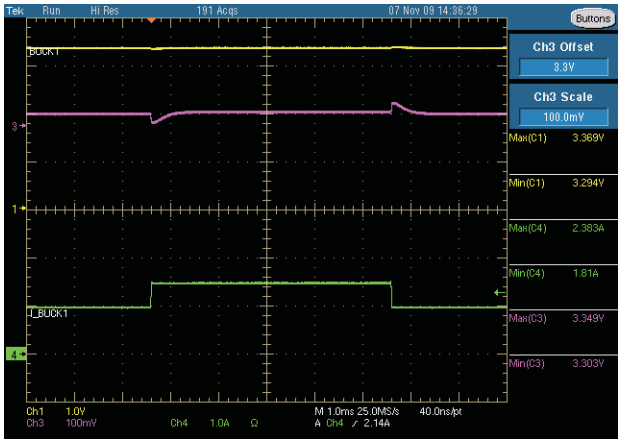

Figure 9. Transient Load Response
V_{OUT} = 3.3 V, ΔI = 1 A to 1.5 A, 100 mV/div

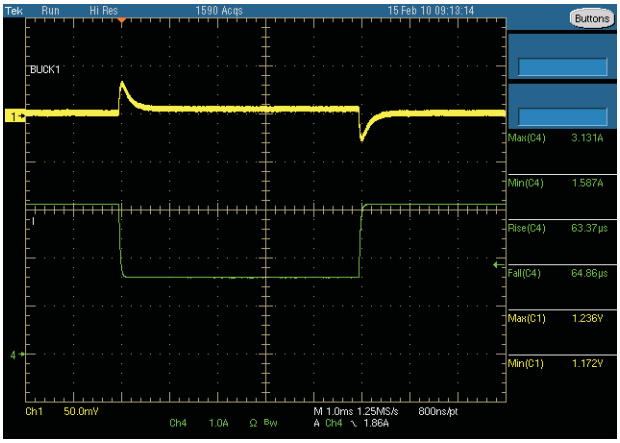

Figure 10. Transient Load Response
V_{OUT} = 1.2 V, ΔI = 1.3 A to 3 A, 50 mV/div

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TYPICAL CHARACTERISTICS (continued)

Buck 1

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.1 MHz (unless otherwise noted)

Figure 11. Transient Supply Response
V_{OUT} = 3.3 V, ΔV = 8 V to 16.5 V, 20 mV/div

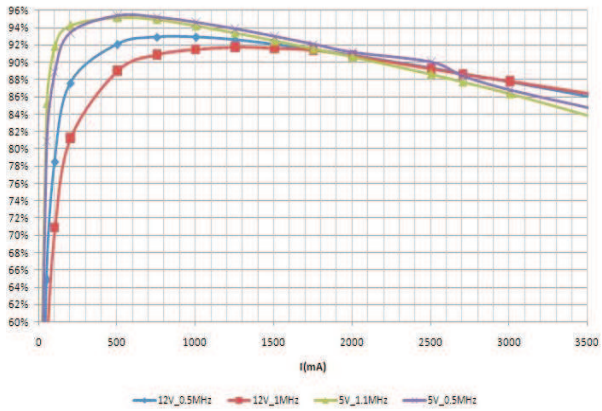

Figure 12. Efficiency
V_{OUT} = 3.3 V, L= 4.7 µH, DCR = 28 mΩ

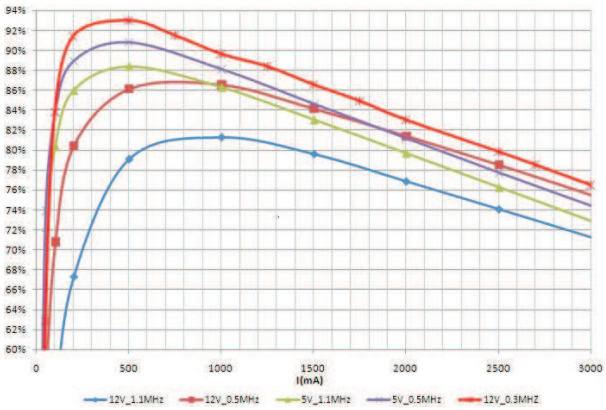

Figure 13. Efficiency
V_{OUT} = 1.2 V, L = 4.7 µH, DCR = 28 mΩ

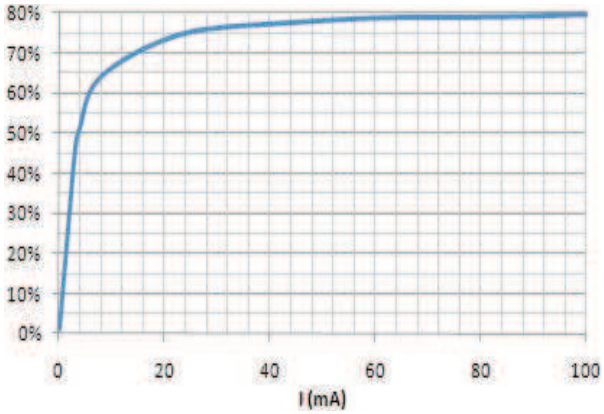

Figure 14. Efficiency Low Power Enabled
V_{OUT} = 3.3 V, L = 4.7 µH

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TYPICAL CHARACTERISTICS

Buck 2

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.14 MHz (unless otherwise noted)

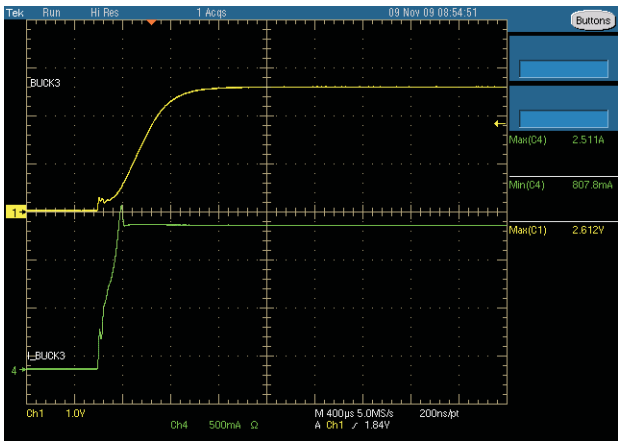

Figure 15. Start-Up
V_{OUT} = 2.5 V, 1.5 A

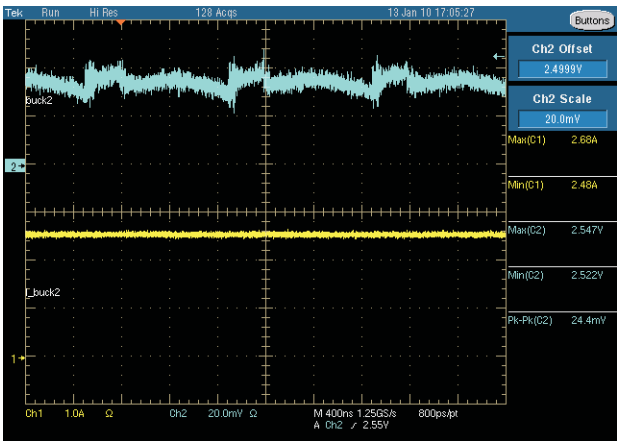

Figure 16. Ripple
V_{OUT} = 2.5 V, 2.5 A, f_{SW} = 0.8 MHz 20 mV/div

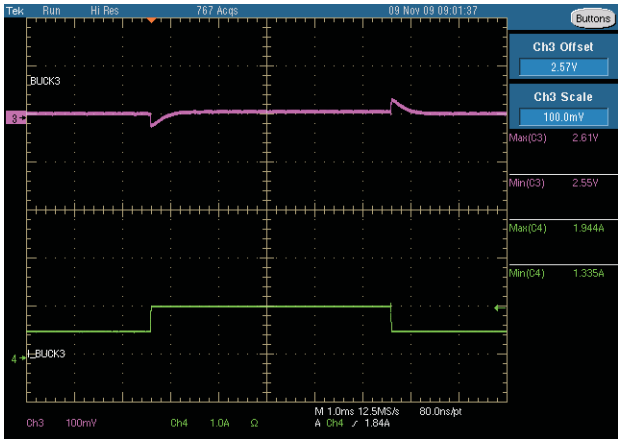

Figure 17. Transient Load Response
V_{OUT} = 2.5 V, ΔI = 1 A to 1.5 A

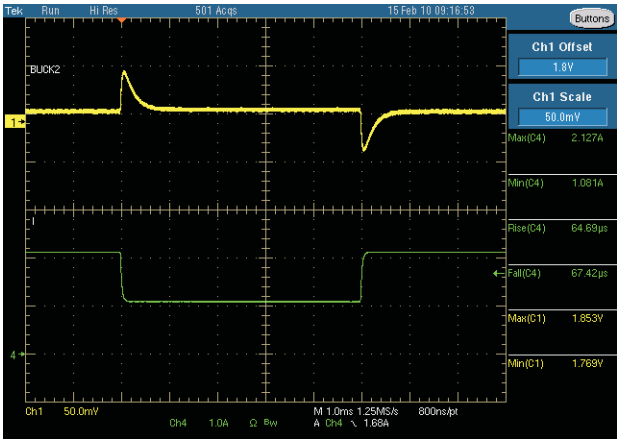

Figure 18. Transient Load Response
V_{OUT} = 1.8 V, ΔI = 1 A to 2 A

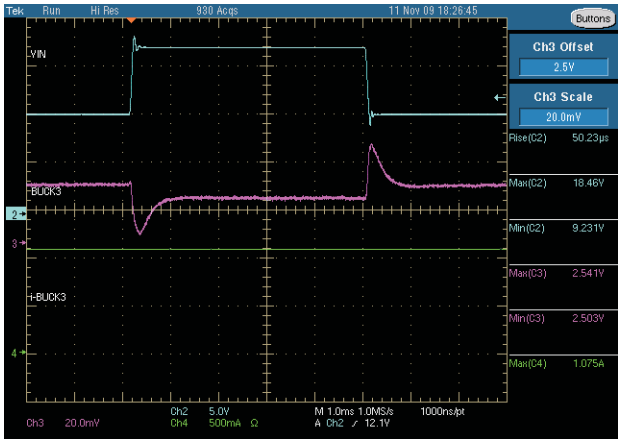

Figure 19. Transient Supply Response
V_{OUT} = 2.5 V, ΔV = 9 V to 8 V

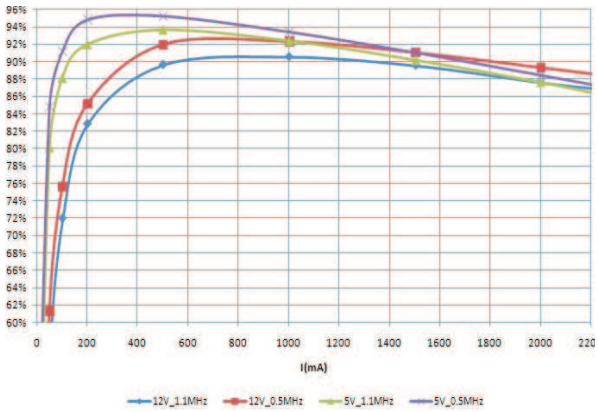

Figure 20. Efficiency
V_{OUT} = 3.3 V, L = 4.7 µH, DCR = 28 mΩ (Also Applies to Buck3)

TYPICAL CHARACTERISTICS (continued)

Buck 2

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.14 MHz (unless otherwise noted)

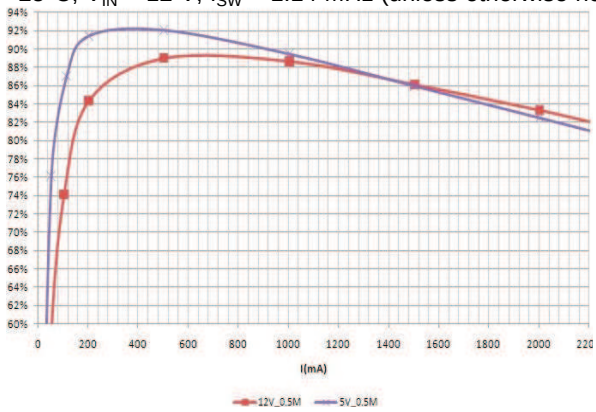

Figure 21. Efficiency
V_{OUT} = 1.8 V, L = 4.7 µH, DCR = 28 mΩ (Also Applies to Buck3)

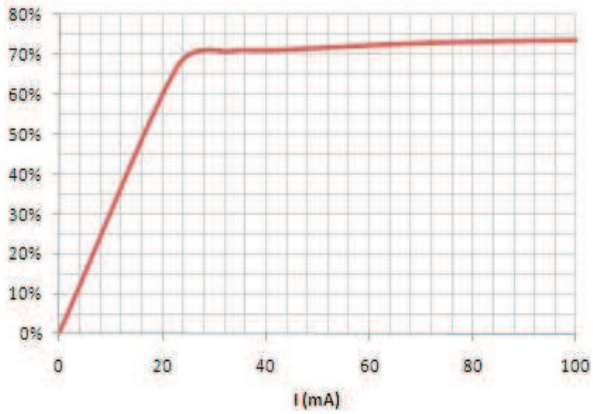

Figure 22. Efficiency Low Power Enabled
V_{OUT} = 2.5 V, L = 4.7 µF

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TYPICAL CHARACTERISTICS

Buck 3

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.14 MHz (unless otherwise noted)

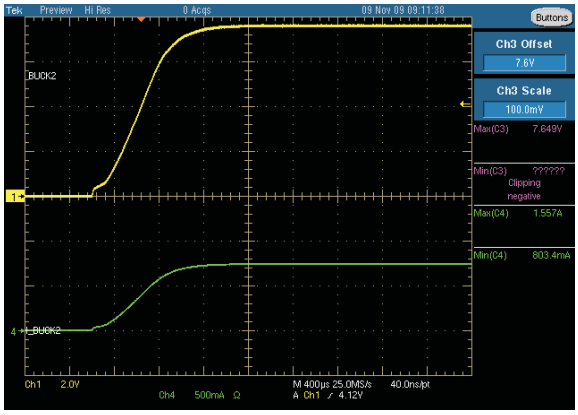

Figure 23. Start-Up
V_{OUT} = 7.5 V, 0.7 A

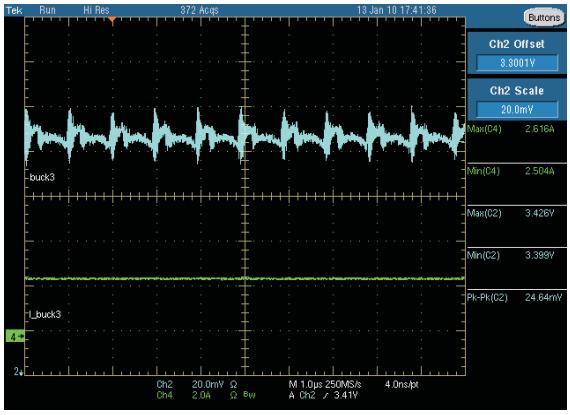

Figure 24. Ripple
V_{OUT} = 7.5 V, 2.5 A, f_{SW} = 800 kHz 20 mV/div

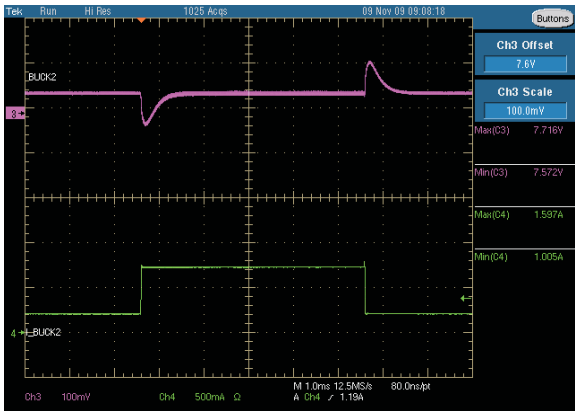

Figure 25. Transient Load Response
V_{OUT} = 7.5 V, ΔI = 1 A to 1.5 A

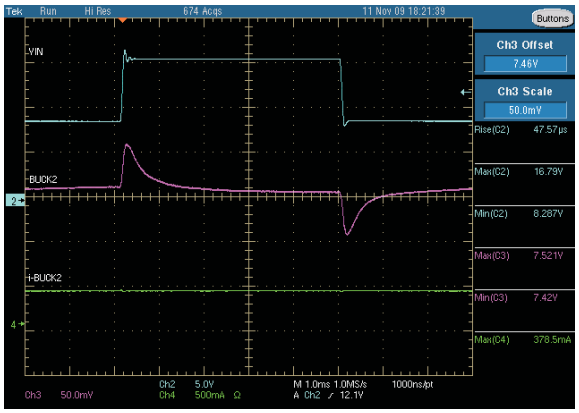

Figure 26. Transient Supply Response
V_{OUT} = 2.5 V, ΔV = 9 V to 8 V

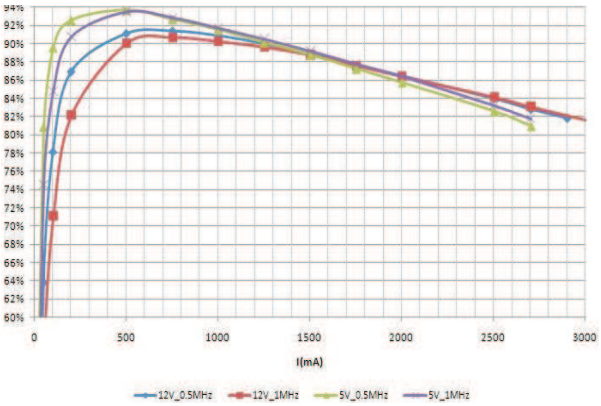

Figure 27. Efficiency
V_{OUT} = 2.5 V, L = 4.7 µH, DCR = 28 mΩ (Also Applies to Buck2)

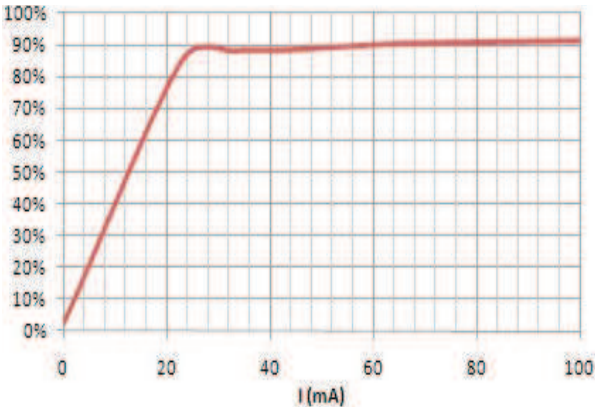

Figure 28. Efficiency Low Power Enabled
V_{OUT} = 7.5 V, L = 4.7 µF

TYPICAL APPLICATION CIRCUIT FOR ADSL SYSTEM AND COMPONENT SELECTION

The TPS65250 has been devised to optimize the power train of xDSL applications. Figure 29 shows a simplified block diagram.

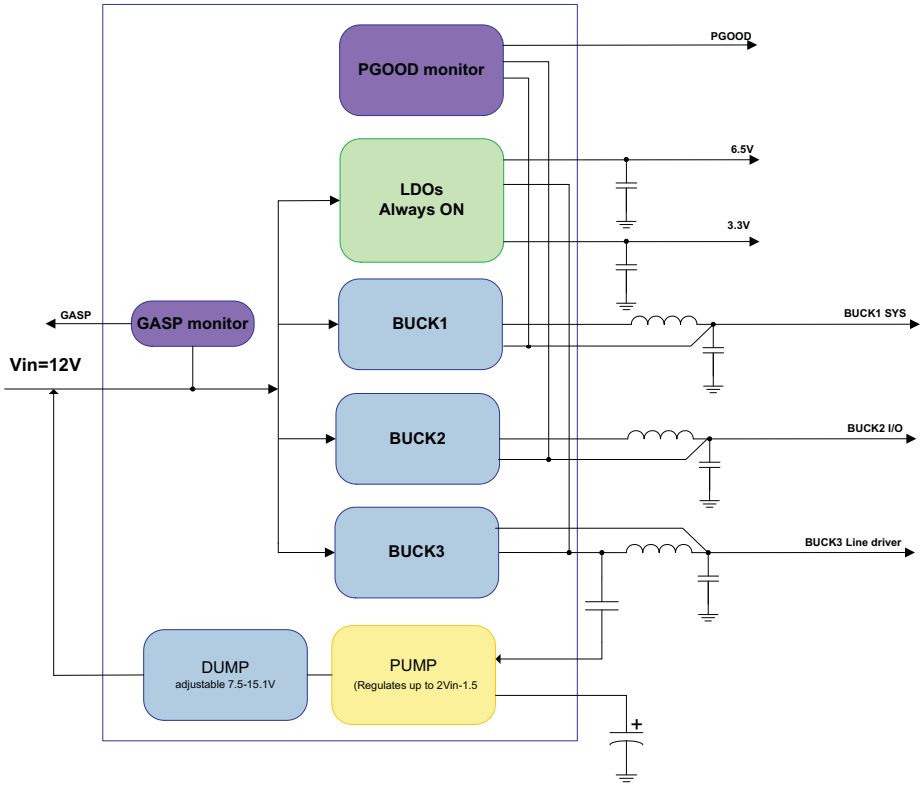

Figure 29. TPS65250 Main Blocks

TPS65250 has several features that improve and simplify the power stage design including a unique storage and release circuit optimized for reduction of storage capacitance needed in dying gasp mode, as well as a low power mode. Table 1 shows the advantages of its usage.

Table 1. Storage and Release Circuit Advantages

FEATURE	ADVANTAGE
System can operate with a 12-V adapter keeping the storage features of a higher storage voltage.	System can run with a12-V adapter instead of bulky and expensive 22 V.
Storage capacitors are separated from the input supply minimizing stresses during normal operation.	Converters run from 12 V allowing for improved efficiency and performance compared to converters operating from 22 V.
Storage capacitors are charged with a controlled inrush free circuit from the adaptor supply to a selected storage voltage as high as [$2V_{IN}$ - 1.5 V].	Reduced stresses on AC adapter, reduced inrush current
Controlled voltage release during dump operation	If the input voltage drops below a selected release voltage, charge from the storage capacitors is transferred to the input stage keeping the input voltage closer to release value for as long as possible.
Reduced number of parts	Storage and release circuitry is completely on chip except for the charge and storage capacitors.
Self-contained pump and dump signaling	Circuit features a flag signal issued to indicate that the dump stage is in process. Can be used to signal the host processor to start a load reduction process.
Enable input pins for start-up and sequencing	Enable pins allow for immediate start-up, for accurate sequencing add a capacitor to the enable pins.

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Table 1. Storage and Release Circuit Advantages (continued)

FEATURE	ADVANTAGE
Adjustable current limit	Using a resistor to set the peak current limit allows to choose the smallest possible inductor for a given load condition by setting the current limit to match the saturation current of the inductor.
Adjustable frequency and sync pin	TPS65250 can be synchronized to a 1.1-MHz or 2.2-MHz external clock. The Sync pin is blanked time equal to the PGOOD delay plus 0.5 s to allow for external low clock setting.
Low power mode	In low power mode device takes less than 20 mW with a 12-V input. If an step load > 100 mA is applied to any of the converters, its output will switch to PWM mode.
Always on LDOs	Two LDOS rated 3.3 V, 10 mA and 6.5 V, 10 mA are available as long as input supply is higher than UVLO threshold.
Reduced footprint	Integrated fets in all converters plus integrated driver circuits for storage and release, minimize the real state required by power stage. Selectable frequency allow to reduce size of inductor plus input/output capacitors.
Voltage supervisor and reset generator	All rails are monitored and a Power Good signal is issued after an adjustable time-out elapses.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency connect a resistor from ROSC to ground. Figure 30 shows the required resistance for a given switching frequency.

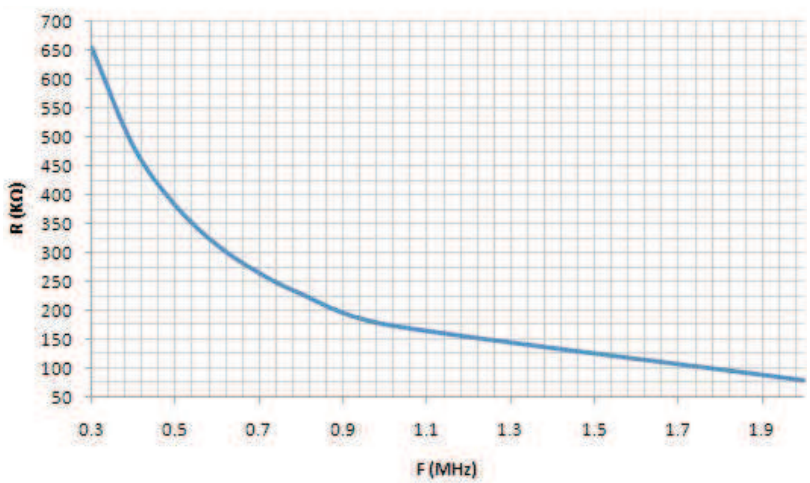

Figure 30. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 174 \bullet f^{-1.122} \tag{1}$$

For operation at 800 kHz a 230-kΩ resistor is required.

Synchronization

The status of the SYNC pin will be ignored during start-up and the TPS65250's control will only synchronize to an external signal after the PGOOD signal is asserted. The status of the SYNC pin will be ignored during start-up and the TPS65250 will only synchronize to an external clock if the PGOOD signal is asserted. When synchronization is applied, the PWM oscillator frequency must be lower than the sync pulse frequency to allow the external signal trumping the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to ground.

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Out-of-Phase Operation

Buck 1 has a low conduction resistance compared to Buck 2 and 3. Normally buck 1 is used to drive higher system loads. Buck 2 and 3 are used to drive some peripheral loads like I/O and line drivers . The combination of buck 2 and 3's loads may be on par with Buck 1's. In order to reduce input ripple current, buck 2 operates in phase with buck 3; buck 1 and buck 2 operate 180 degrees out-of-phase. This enables the system, having less input ripple, to lower component cost, save board space and reduce EMI.

Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1-MΩ pull-up to the 3V3 rail.

Soft Start Time

The device has an internal pull-up current source of 5 µA that charges an external slow start capacitor to implement a slow start time. Equation 2 shows how to select a slow start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the slow start charge current (I_{SS}) is 5 µA. The soft start circuit requires 1 nF per 200 µS to be connected at the SS pin. A 1-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant pins.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \tag{2}$$

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with 40.2 kΩ for the R1 resistor and use the Equation 3 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \tag{3}$$

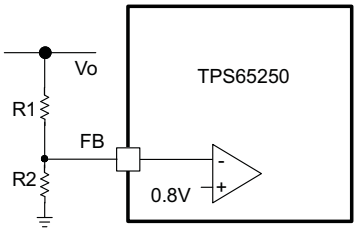

Figure 31. Voltage Divider Circuit

Error Amplifier

The device has a transconductance error amplifier. The transconductance of the error amplifier is 130 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

Loop Compensation

TPS65250 is a current mode control dc/dc converter. The error amplifier is a 130-µA/V transconductance amplifier. A type-II compensation circuit is adequate for the converter to have a phase margin between 60 and 90 degrees.

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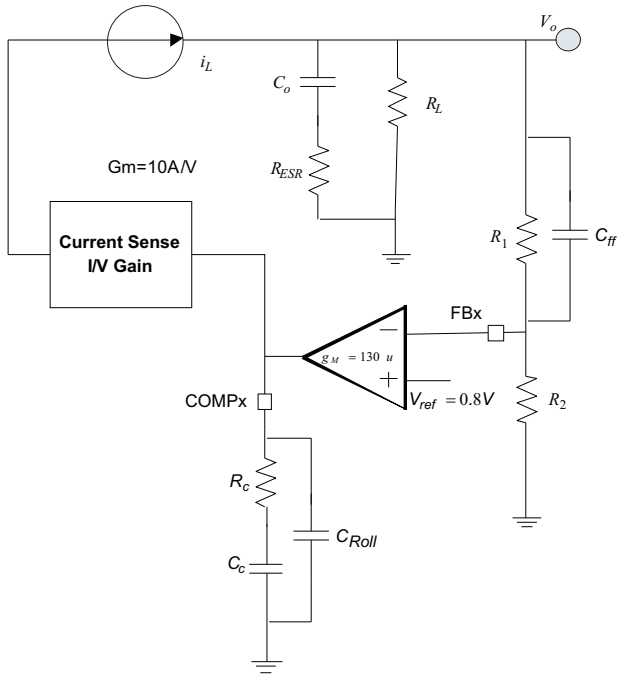

Figure 32. Loop Compensation

The design guidelines for TPS65250 loop compensation are as follows:

1. Set up cross over frequency fc.
2. R_C can be determined by:

$$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}} \tag{4}$$

   Where is the G_M amplifier gain (130 µA/V), is the power stage gain (10 A/V).

3. Place a compensation zero at the dominant pole,

$$fp = \frac{1}{C_O \cdot R_L \cdot 2\pi} \tag{5}$$

   C_C can be determined by:

$$C_C = \frac{R_L \cdot Co}{R3} \tag{6}$$

4. C2 is optional. It can be used to cancel the zero from Co's ESR.

$$C2 = \frac{\mathrm{Re}sr \cdot Co}{R3} \tag{7}$$

In some applications the transient response performance is the primary goal, a type-III compensation circuit allows the system having one more zero. The additional zero provides extra phase margin and the system can achieve an extra high crossover frequency. C3 can be added at the upper leg of the output divider to form a zero with R1.

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies between 500 kHz and 1 MHz give best trade off between performance and cost. When using smaller L and Cs, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Use type III circuit for switching frequencies higher than 500 kHz.
Select cross over frequency (fc) to be less than 1/5 to 1/10 of switching frequency.	Suggested fc = fs/10	Suggested fc = fs/10
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Co}{g_M \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance COMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff} is smaller than soft start equivalent frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when Buck 1 and 3 converters' outputs are more than 90% of its nominal output voltage. The default reset time is 1000 ms. The polarity of the PGOOD is active high.

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Current Limit Protection

Figure 33 shows the (peak) inductor current limit for Buck 1. The typical limit can be approximated with the following graph.

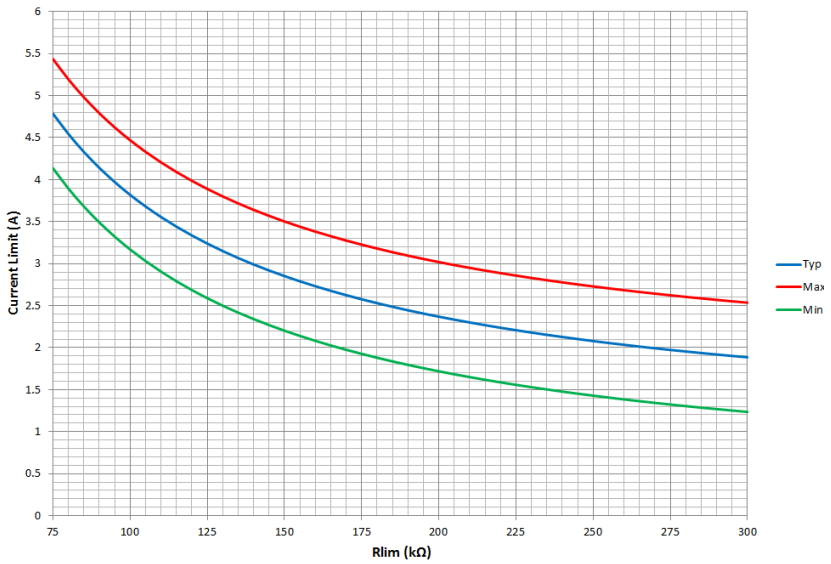

Figure 33. Buck 1

Figure 34 shows the (peak) inductor current limit for Buck 2. The typical limit can be approximated with the following graph.

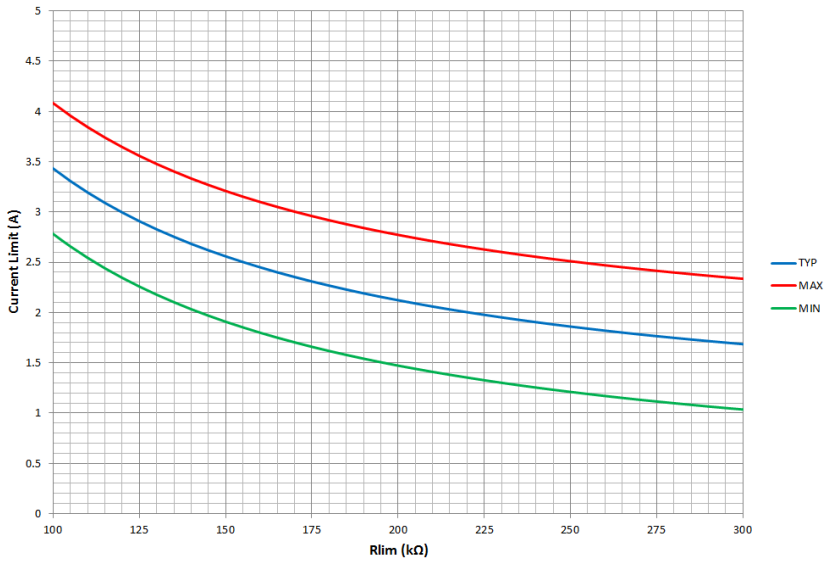

Figure 34. Buck 2

Figure 35 shows the (peak) inductor current limit for Buck 3. The typical limit can be approximated with the following graph.

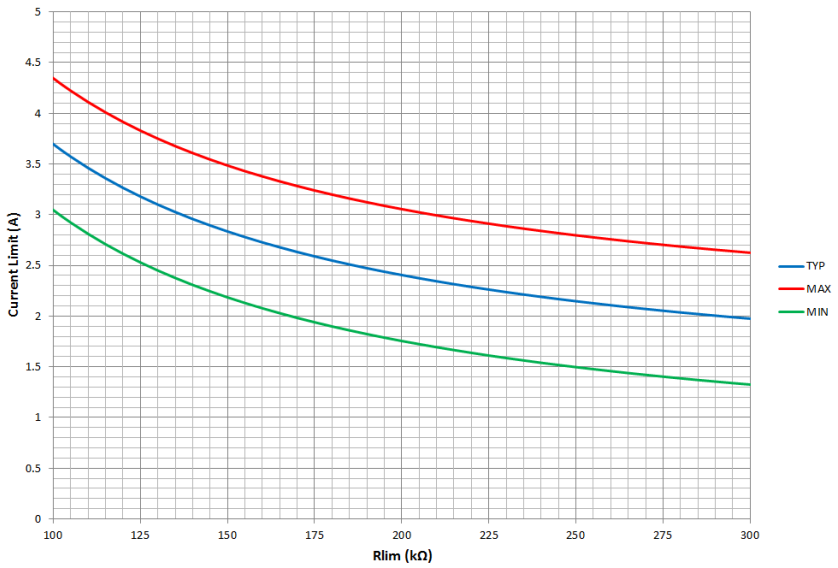

Figure 35. Buck 3

All converters operate in hiccup mode: Once an over-current lasting more than 10 ms is sensed in any of the converters, they will shuts down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 10 ms, only the relevant converter affected will go into and out of under-voltage and no global hiccup mode will occur. The converter will be protected by the cycle-by-cycle current limit during that time.

Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

Power Dissipation

The total power dissipation inside TPS65250 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (R_{JA}) and ambient temperature.

To calculate the temperature inside the device under continuous loading use the following procedure.

1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading.
3. Determine from the graphs below the expected losses in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.
4. To calculate the maximum temperature inside the IC use the following formula:

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$$T_{HOT_SPOT} = T_A + P_{DIS} \bullet \theta_{JA} \tag{8}$$

Where:

T_A is the ambient temperature

P_{DIS} is the sum of losses in all converters

θ_{JA} is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout

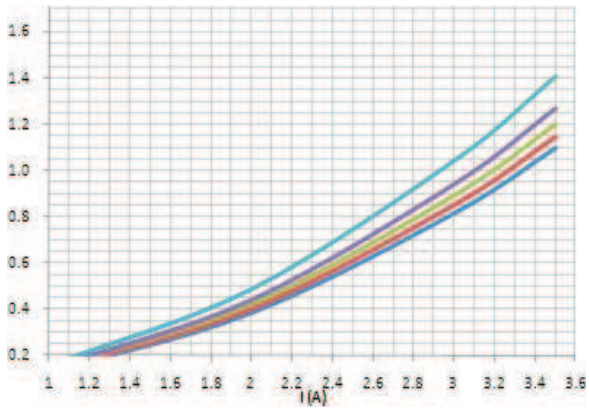

Figure 36. Buck 1
V_{IN} = 12 V, f_{SW} = 500 kHz

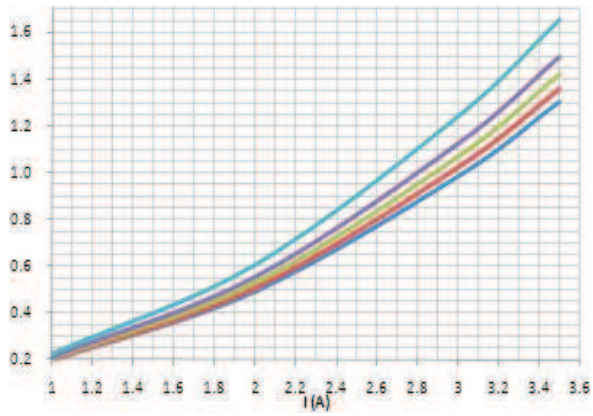

Figure 37. Buck 1
V_{IN} = 12 V, f_{SW} = 1.1 MHz

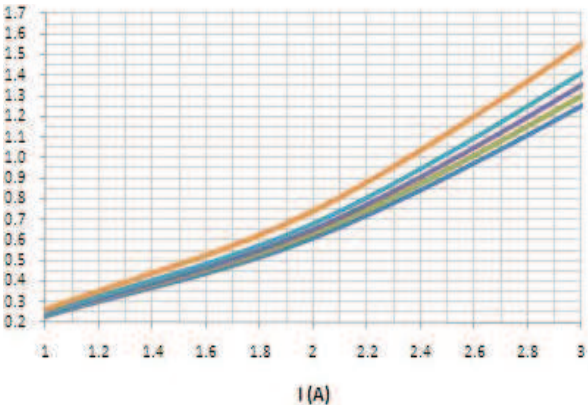

Figure 38. Buck 2 and 3
V_{IN} = 12 V, f_{SW} = 500 kHz

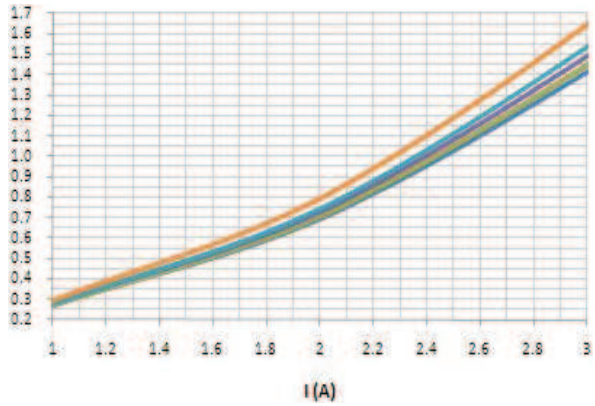

Figure 39. Buck 2 and 3
V_{IN} = 12 V, f_{SW} = 1.1 MHz

Low Power Mode Operation

By pulling the Low_p pin high all converters will operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. Although each buck converter has a skip comparator that makes sure regulation is not lost when a heavy load is applied and low power mode is enabled, system design needs to make sure that the LP pin is pulled low for continuous loading in excess of 100 mA.

When low power is implemented, the peak inductor current used to charge the output capacitor is:

$$I_{LIMIT} = 0.25 \bullet T_{SLEEP_CLK} \bullet \frac{V_{IN} - V_{OUT}}{L} \tag{9}$$

Where T_{SLEEP_CLK} is half of the converter switching period, $2/f_{SW}$.

The size of the additional ripple added to the output is:

$$\Delta V_{OUT} = \frac{1}{C} \bullet \left(\frac{L \bullet I_{LIMIT}^{2}}{2} \bullet \frac{V_{IN}}{V_{OUT} \bullet (V_{IN} - V_{OUT})} - \frac{I_{LOAD}}{f_{SLEEP_CLK}} \right) \tag{10}$$

And the peak output voltage during low power operation is:

$$V_{OUT_PK} = V_{OUT} + \frac{\Delta V_{OUT}}{2} \tag{11}$$

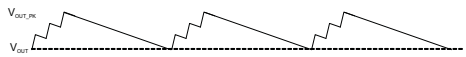

Figure 40. Peak Output Voltage During Low Power Operation

APPLICATION INFORMATION

Design Guide - Step-By-Step Design Procedure

The following example illustrates the design procedure for selecting external components for the three buck converters. For this example the following schematic will be used.

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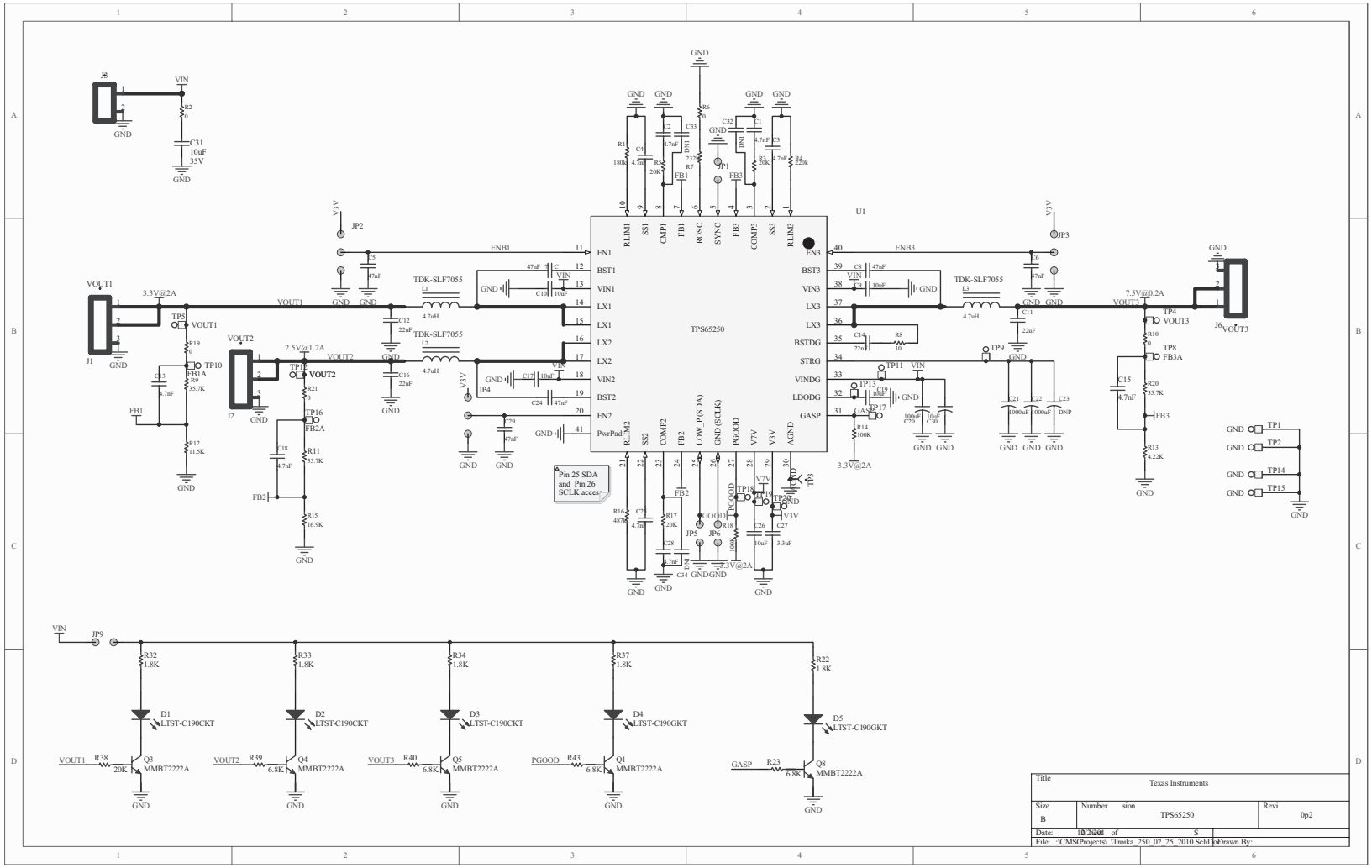

Figure 41. TPS65250 Reference Design

The control and power signals used in the design are shown in Table 2.

Table 2. Control and Power Signals

SIGNAL	TYPE	STATUS	FUNCTION
POWER			
VIN	I		12-V DC main supply to TPS65250
GND			System ground. All ground pins and power pad should be connected together.
3.3V	O		Output of Buck 1
2.5V	O		Output of Buck 2
7.5V	O		Output of Buck 3
VPULL	O		Voltage used to connect the pull-up resistors of the Open Drain outputs (PGOOD, GASP).
CONTROL			
EN1, EN2	I	Active high	Enable signals for Buck 1 and Buck 2. Left open they will start automatically once power is applied. If capacitors are fitted to their enable pins, start-up will be delayed.
EN3	I	Active high	Enable signal for Buck 3. Externally enabled by host processor. During the release stage (GASP) Buck 3 must stay enabled.
LOW_P	I	Active high	External processor signal to force buck converters in low power mode and reduce input power.
SYNC	I		External 1.14-MHz clock. Device will start with an internal frequency set to 0.8 MHz.
PGOOD	O	Active low	PGOOD (end of reset signal) to processor. Buck 1 and Buck 3 are monitored.
GASP	O	Active low	Release stage of the pump and dump procedure. Input supply collapsed and energy stored in CSTG capacitor is released in a controlled way to the input supply.

The following example illustrates the design procedure for selecting external components for the three buck converters. The example focuses on BUCK 1, but the procedure can be directly applied to BUCK 2 and 3 as well. The design goal parameters are given in Table 3.

Table 3. Design Parameters

Output voltage	3.3 V
Transient response 0.5-A to 2-A load step	165 mV
Maximum output current	2 A
Input voltage	12 V nom, 9.6 V to 14.4 V
Output voltage ripple	< 30 mV p-p
Switching frequency	500 kHz

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, you will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 300 kHz to 2.2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and a high efficiency operation. Note however that for xDSL applications is desirable to synchronize the converter to the system clock running at either 1.1 MHz or 2.2 MHz. If 1.1 MHz is to be used, set the external resistor to 232 kΩ for PMIC switching at 800 KHz (~70% of clock frequency).

Output Inductor Selection

To calculate the value of the output inductor, use Equation 12. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, KIND is normally from 0.1 to 0.3 for the majority of applications.

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For this design example, use KIND = 0.2 and the inductor value is calculated to be 5.4 µH. For this design, a nearest standard value was chosen: 4.7 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 13 and Equation 14.

$$Lo = \frac{Vin - Vout}{Io \cdot K_{ind}} \cdot \frac{Vout}{Vin \cdot fsw} \tag{12}$$

$$Iripple = \frac{Vin - Vout}{Lo} \cdot \frac{Vout}{Vin \cdot fsw} \tag{13}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \cdot \left(\frac{Vo \cdot (Vin\max - Vo)}{Vin\max \cdot Lo \cdot fsw} \right)^2} \tag{14}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{15}$$

Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

Equation 16 gives the minimum output capacitance to meet the transient specification. For this example, L_O = 4.7 µH, ΔI_{OUT} = 2 A – 0.5 A = 1.5 A and ΔV_{OUT} = 165 mV. Using these numbers gives a minimum capacitance of 19.4 µF. A standard 22-µF ceramic capacitor is chose in the design.

$$Co > \frac{\Delta I_{OUT}{}^2 \cdot L_o}{V_{out} \cdot \Delta Vout} \tag{16}$$

Equation 17 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. From Equation 13, the output current ripple is 0.46 A. From Equation 17, the minimum output capacitance meeting the output voltage ripple requirement is 1.74 µF.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{Vripple}{Iripple}} \tag{17}$$

After considering both requirements, for this example, one 22-µF, 6.3-V X7R ceramic capacitor with 3 mΩ of ESR will be used.

Input Capacitor

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in Equation 18. For this example, I_{OUT} = 2 A, V_{OUT} = 3.3 V, V_{INmin} = 9.6 V, from Equation 18, the input capacitors must support a ripple current of 1.81 A RMS.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vin\min} \cdot \frac{(Vin\min - Vout)}{Vin\min}} \tag{18}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 19. Using the design example values, I_{OUTmax} = 2 A, C_{IN} = 10 µF, f_{SW} = 1100 kHz, yields an input voltage ripple of 45 mV.

$$\Delta Vin = \frac{Iout\max \cdot 0.25}{Cin \cdot fsw} \tag{19}$$

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Bootstrap Capacitor Selection

A 0.047-µF ceramic capacitor must be connected between the BST to LX pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

Adjustable Current Limiting Resistor Selection

The converter uses the voltage drop on the high-side MOSFET to measure the inductor current. The over current protection threshold can be optimized by changing the trip resistor. Figure 33 governs the threshold of over current protection for Buck 1. When selecting a resistor, do not exceed the graph limits. In this example, the over current threshold is 3.2 A. In order to prevent a premature limit trip, the minimum line is used and the resistor is 100 kΩ.

When setting high-side current limit to large current values, ensure that the additional load immediately prior to an overcurrent condition will not cause the switching node voltage to exceed 20 V. Additionally, ensure during worst case operation, with all bucks loaded immediately prior to current limit, the maximum virtual junction temperature of the device does not exceed 125°C.

Bootstrap Capacitors

The device has three integrated boot regulators and requires a small ceramic capacitor between the BST and LX pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 µF. For the pump circuit use 0.022 nF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Output Voltage and Feedback Resistors Selection

For the example design, 35.7 kΩ was selected for R10. V_{OUT} is 3.3 V, V_{REF} = 0.8 V. Using Equation 3, R7 is calculated as 11.5 kΩ. A standard 80.6-kΩ resistor is chose in this design.

Compensation

TPS65250 is a current mode control dc/dc converter. It uses a transconductance error amplifier. A type-II compensation circuit is adequate for the converter to have a phase margin between 60 and 90 degrees. The following equations show the procedure of designing a peak current mode control dc/dc converter.

The compensation design takes the following steps:

1. Set up the anticipated cross-over frequency. Use Equation 4 to calculate the compensation network's resistor value. In this example, the anticipated cross-over frequency (fc) is 65 kHz. The power stage gain ( ) is 10A/V and the GM amplifier gain (gm_{ps}) is 130 µA/V.
2. Place compensation zero at low frequency to boost the phase margin at the crossover frequency. From the procedures above, the compensation network includes a 20-kΩ resistor (R12) and a 4700-pF capacitor (C1).
3. An additional pole can be added to attenuate high frequency noise.

In some applications the transient response performance is the primary goal, a type-III compensation circuit allows the system having one more zero. The additional zero provides extra phase margin and the system can achieve an extra high crossover frequency. In this example, a 4.7-nF capacitor can be added at the upper leg of the output divider. C15 and R10 form a zero, which boost the phase margin and lift the gain so that the converter has a high crossover frequency at 100 kHz.

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3.3-V and 6.5 LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 10 µF for V7V pin 28
- 3.3 µF for V3V pin 29

Choice of Converter for Pump Operation And Sequencing Requirement

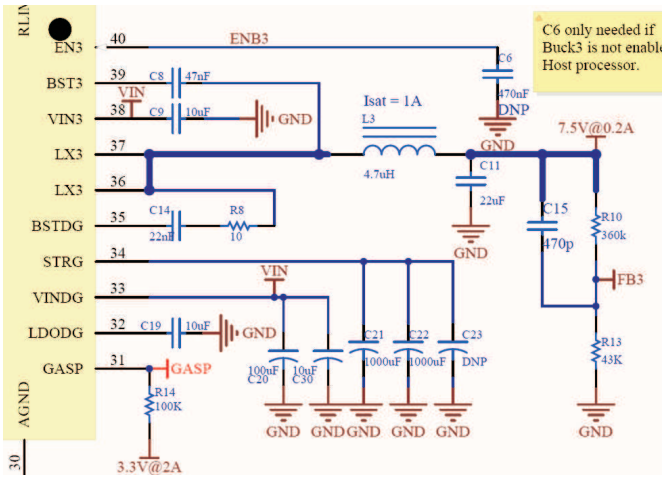

Figure 42. Pump and Dump Pins

Although any converter can be used to feed the pump circuit buck 3 is the best option that allows for an easy layout as the input of the pump circuit (BSTG pin 35) is next to its switching node and allows for a short connection for a trace associated to a high frequency switching node. Connect a 22-nF capacitor in series with a 10-Ω resistor from the LX3 node to the BSTDG pin.

The storage capacitor charges in two stages:

1. When V_{IN} is applied the capacitor charges in a controlled way to a voltage close to V_{IN} at a rate of 0.1 ms/µF.
2. Once the capacitor is charged Buck 3 is enabled and its switching node provides the energy to charge the capacitor to the final storage voltage. Once this voltage is achieved the pump circuit will only provide current to compensate the self-discharge of the storage capacitor.

Note that it is important that these two charge stages do not overlap. In other words buck 3 must be enabled only after the first stage of charging is achieved.

Based on these considerations the following sequencing requirement is required:

Table 4. Sequencing

CONVERTER	V	FUNCTION	SEQUENCING	SOFT START
Buck 1	3.3	System, SoC	1st supply to start, no delay. EN1 tied to V3P3.	Use 4.7 nF to achieve SS ~0.5 ms.
Buck 2	2.5	MEM, I/O, SoC	Simultaneous start with buck 1. EN2 tied to v3P3.	Use 3.9 nF to achieve rationometric start-up with respect to Buck 1.
Buck 3	7.5	Line drivers	Enabled by SoC. Must start after storage capacitor settles t_I ~V_{IN}.	Use 4.7 nF.

If a 2000-µF capacitor is used for storage, Buck 3 must start at least 200 ms after Buck 1 and Buck 3 are enabled. There are two possible options to cover the sequencing requirement on Buck 3:

- Use a GPIO from the SoC connected To EN3. There will be a delay of hundreds of ms to a few seconds before the line drivers are enabled. By then the storage capacitor will be charged to ~V_{IN}.
- Fit a capacitor at the EN pin. With a delay of 1.67 ms/nF, a 470-nF capacitor will provide a delay of ~784 ms from the time when Buck 1 and Buck 2 are enabled to the time when Buck 3 is enabled. This will provide ample time for the storage capacitor to settle at ~V_{IN} and also for addition of more storage capacitance if required.

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Capacitance Reduction With TPS65250 Pump and Dump Circuit

Table 6 shows the capacitance reduction achieved compared to the typical application where the storage capacitor is connected to the adapter supply the following formula applies.

$$\Delta t = \frac{1}{2} C_{IN}(V_{DET}^{2} - V_{LOW}^{2}) \tag{20}$$

Where:

P = Gasp power

Δt = Gasp time, 60 ms

V_{DET} = Detection voltage (at this point is assumed input supply has disappeared), 11 V

V_{LOW} = Minimum gasp voltage, 8.5 V

Size of Storage Capacitor

On choosing the capacitor for storage the following considerations should be taken into account:

- Capacitor type: Given the relatively high values required for gasp applications electrolytic are typically the choice of capacitor due to their low cost.
- Capacitor voltage rating and derating: The electrolytic capacitors of interest for a 12-V application are rated at 25 V. Assuming an 80% derating factor, this will match the storage voltage. Bear in mind that the accuracy of this voltage is 5%, therefore calculations should include the worst case number. For a 20-V setting the storage voltage will be in the 19 V - 21 V range.
- Capacitor dimension: For this particular example a 25-mm height restriction is in place.
- Capacitor tolerance and life: As electrolytic capacitors degrade with time the choice of capacitor will dictate the overall system life expectancy. It is recommended to add the following adjustment factors to the chosen capacitor value.
- Capacitor package: Surface mount devices are considerably more expensive than through hole devices.

Based on these considerations the series M of Panasonic through hole capacitors is chosen.

http://industrial.panasonic.com/www-data/pdf/ABA0000/ABA0000CE12.pdf

Good savings and real estate reductions can be obtained if 25-V capacitors are used. As Table 5 shows only the 1000-µF part meets the height restriction of the design.

Table 5. 25-V Capacitors That Can Be Used in TPS65250 Pump and Dump Circuit to Support 2.85 W

C (µF)	HEIGHT (mm)
1000	20
2200	25 (too tall)
3300	25 (too tall)
4700	31 (too tall)

Table 6 shows the tabulated results for the TPS65250 P&D circuit with a gasp time of 60 ms, power levels of 1 W to 4 W, showing the capacitance (C_{STRG}) required for 20-V storage. The column C_{IN} shows the capacitance required using the typical approach of adding capacitance to the input supply. The data clearly shows that the pump and dump circuit allows for a major reduction in the storage capacitor.

Table 6. Storage Capacitance required with TPS65250 Pump and Dump Circuit

PV_{GASP} →	P = 1W		P = 2 W		P = 3 W		P = 4 W	
V_{STRG}↓	C_{IN} (µF)	C_{STRG} (µF)	C_{IN} (µF)	C_{STRG} (µF)	C_{IN} (µF)	C_{STRG} (µF)	C_{IN} (µF)	C_{STRG} (µF)
20	2,462	602	4,923	1,203	7,385	1,805	9,846	2,406

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Going through the iterative procedure, using only two 1000-µF, 25-V capacitors will allow for a gasp power in excess of 2.85 W, instead of the 6 required in the application without the pump and dump feature.

Table 7. 25-V Capacitors Used in TPS65250 Pump and Dump Circuit to Support 2.85 W

ECA1CM222B	C (µF)	P_GASP (W)	COMMENT
1	1000	1.63	Too little
2	2000	3.26	About right
3	3000	4.89	Too much

Note that the final capacitor value needs to be adjusted for the worst case of tolerance (typically -20%) and reduction of capacitor value at the end of tis life expectancy (typically 20%).

Pump and Dump Plots

Figure 43 shows the pump stage plots. Green trace is the input supply (12 V), yellow trace is the storage capacitor voltage, purple trace is the Buck 3 supply and blue trace is the PGOOD signal. The storage capacitor is 2000 µF and it takes ~200 ms to charge to the input supply. BUCK has a 470-nF capacitor connected to the EN pin provides a delay of ~800 ms from the time when the input voltage is applied and the storage capacitor charges to the 20-V target and the PGOOD signal has a 2-s delay before being asserted.

Figure 44 shows the dump stage plots. Yellow trace is the storage capacitor voltage, purple trace is the V_{IN} supply and blue trace is the 7.5-V Buck 3 signal green trace is Buck 3 current. The total gasp time is ~70 ms which is consistent with the calculations shown.

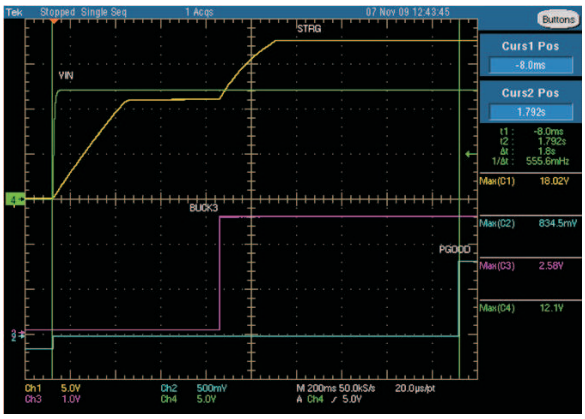

Figure 43. Pump Operation

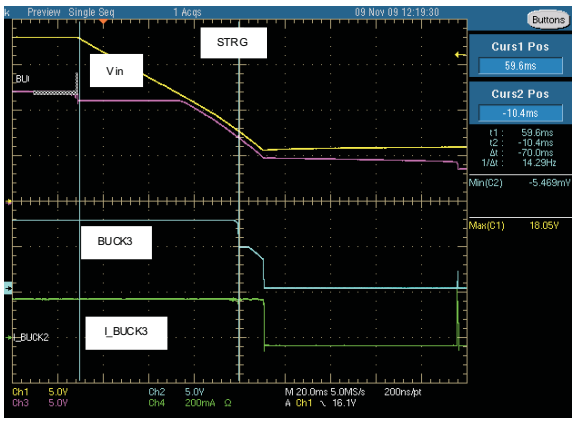

Figure 44. Dump Operation

Table 8 shows the loading on the rails plus rail efficiency to show the total power of ~3.18 W provided by the 12-V adapter supply.

Table 8. Rail Loading for TPS65250 Pump and Dump Circuit Verification

RAIL	V	I (A)	P_O (W)	EFFICIENCY	PIN (W)
Buck 1	3.3	0.22	0.73	85%	0.85
Buck 2	2.5	0.21	0.53	87%	0.6
Buck 3	7.5	0.2	1.5	87%	1.72
12 V	12	0.02			0.24
Total			2.75		3.42

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65250RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65250
TPS65250RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65250
TPS65250RHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65250
TPS65250RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65250
TPS65250RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65250
TPS65250RHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65250

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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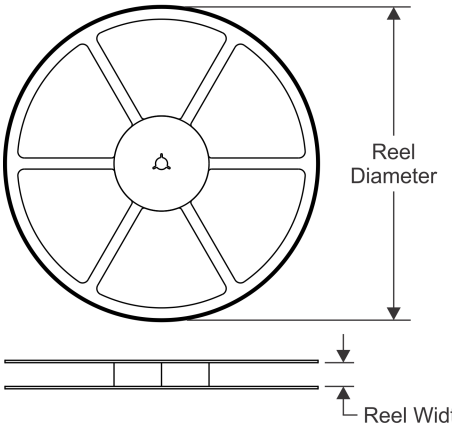
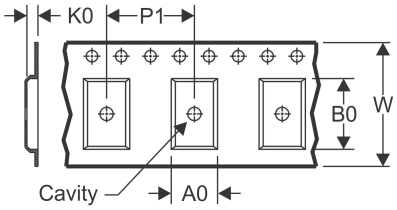
TAPE AND REEL INFORMATION

REEL DIMENSIONS

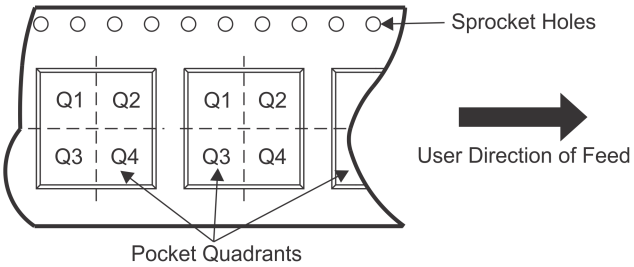


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

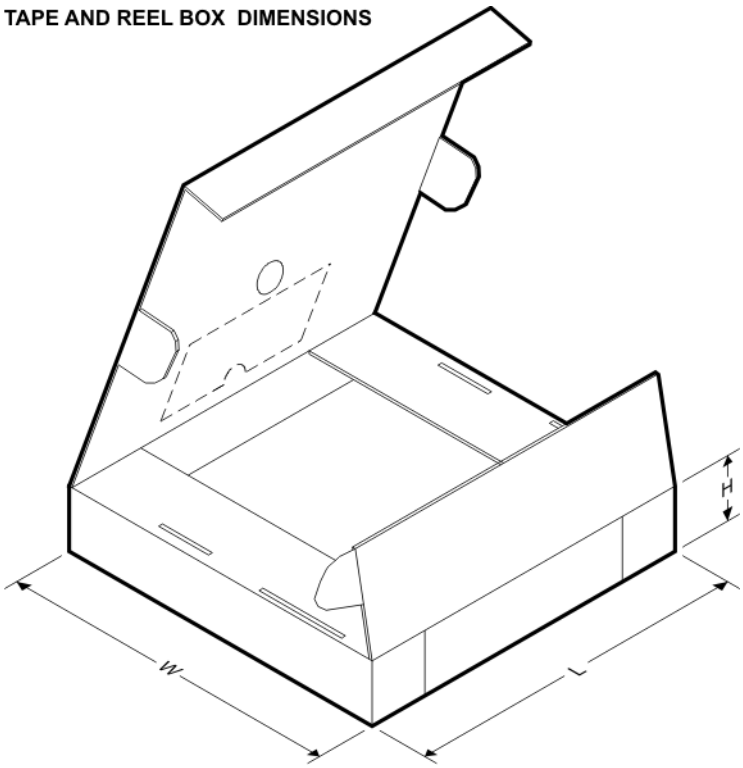
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65250RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65250RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65250RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65250RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

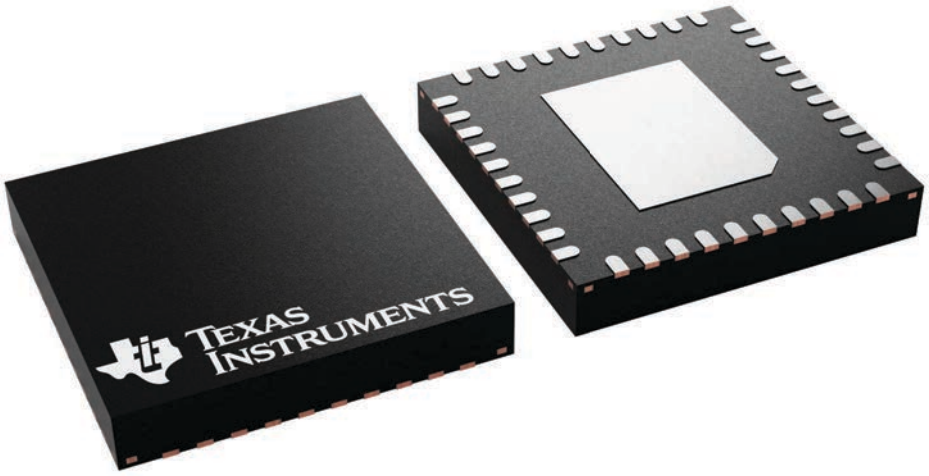
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



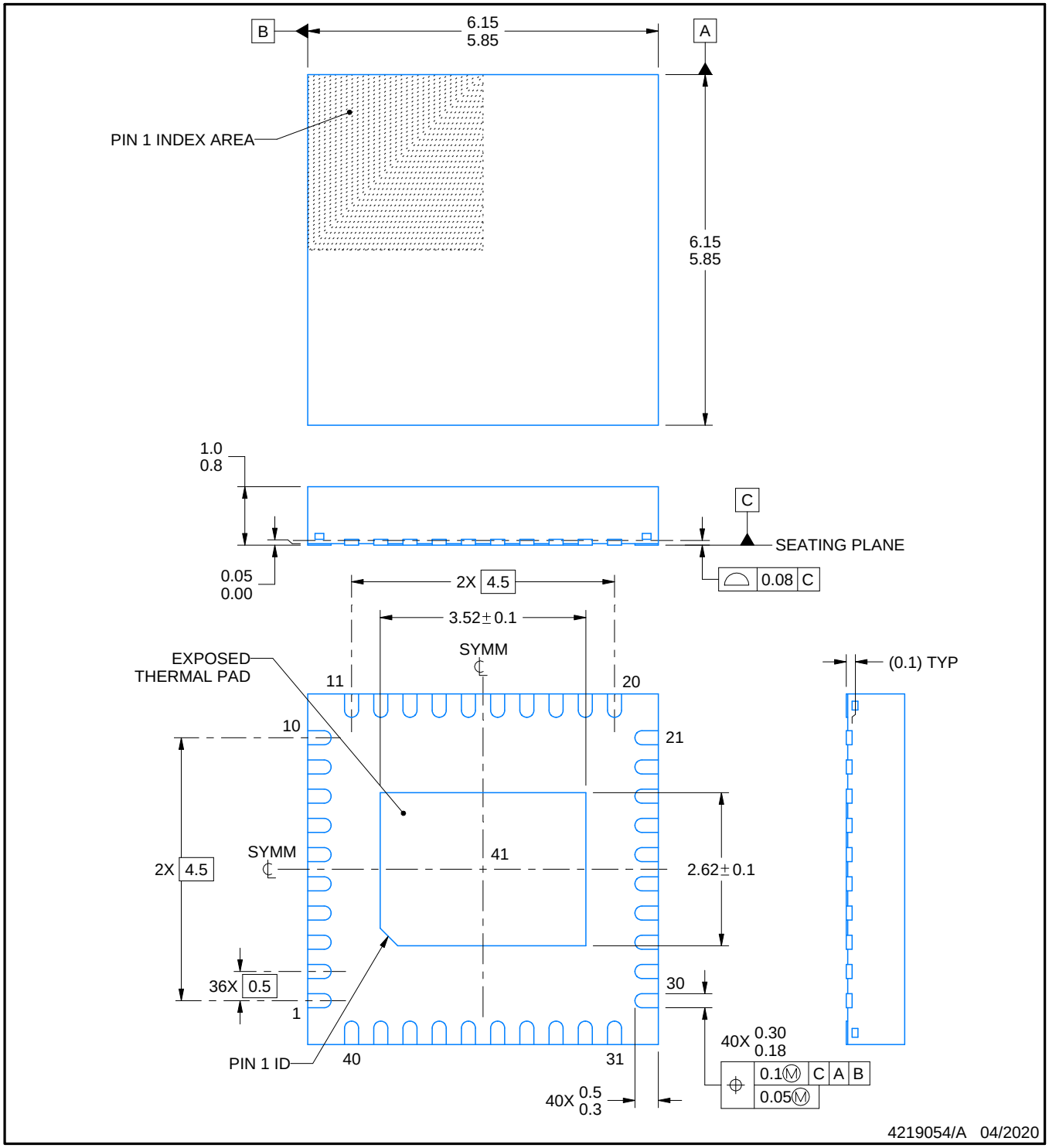
4225870/A

PACKAGE OUTLINE

RHA0040E

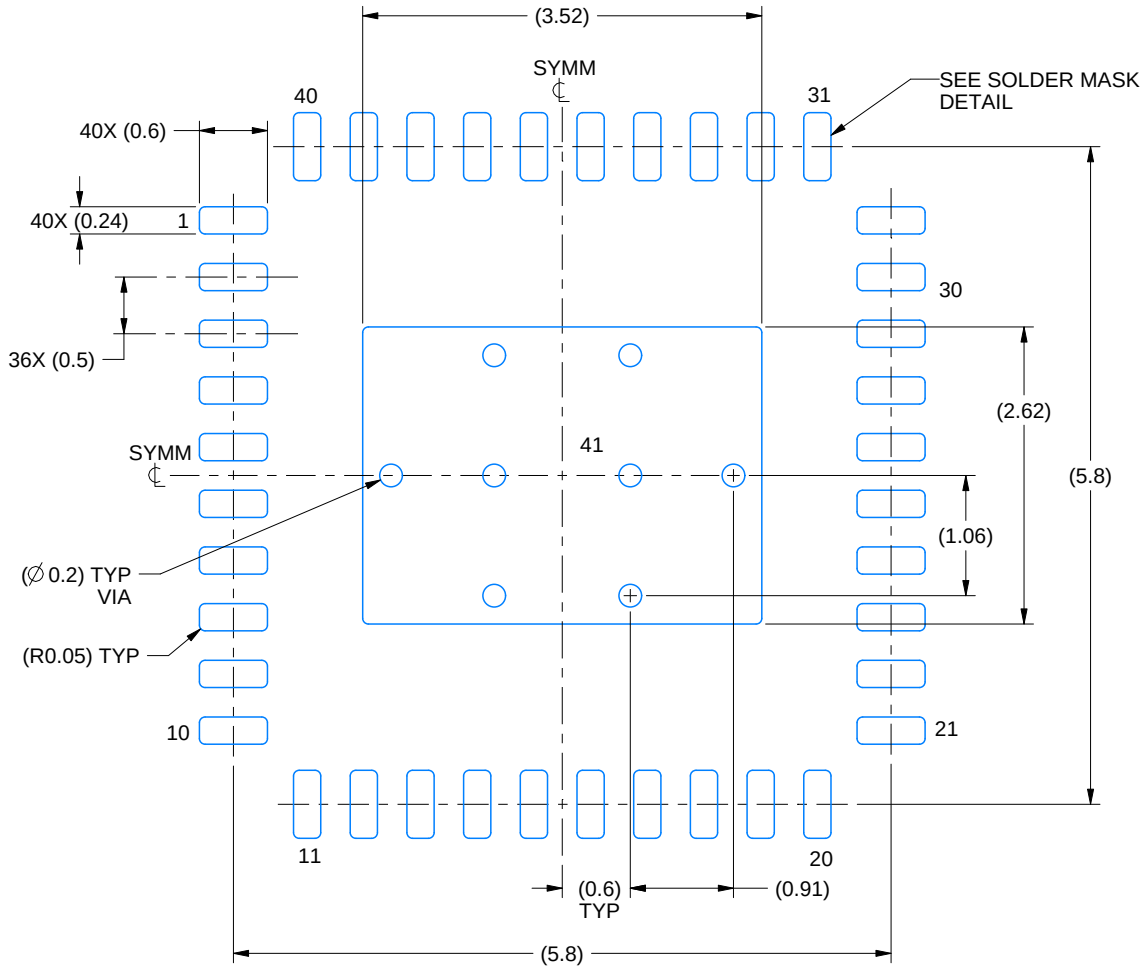
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

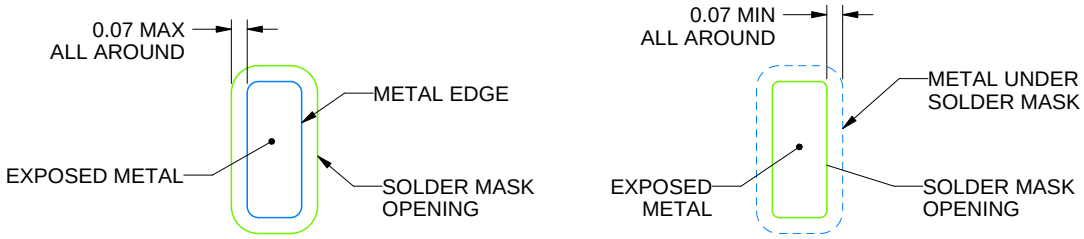


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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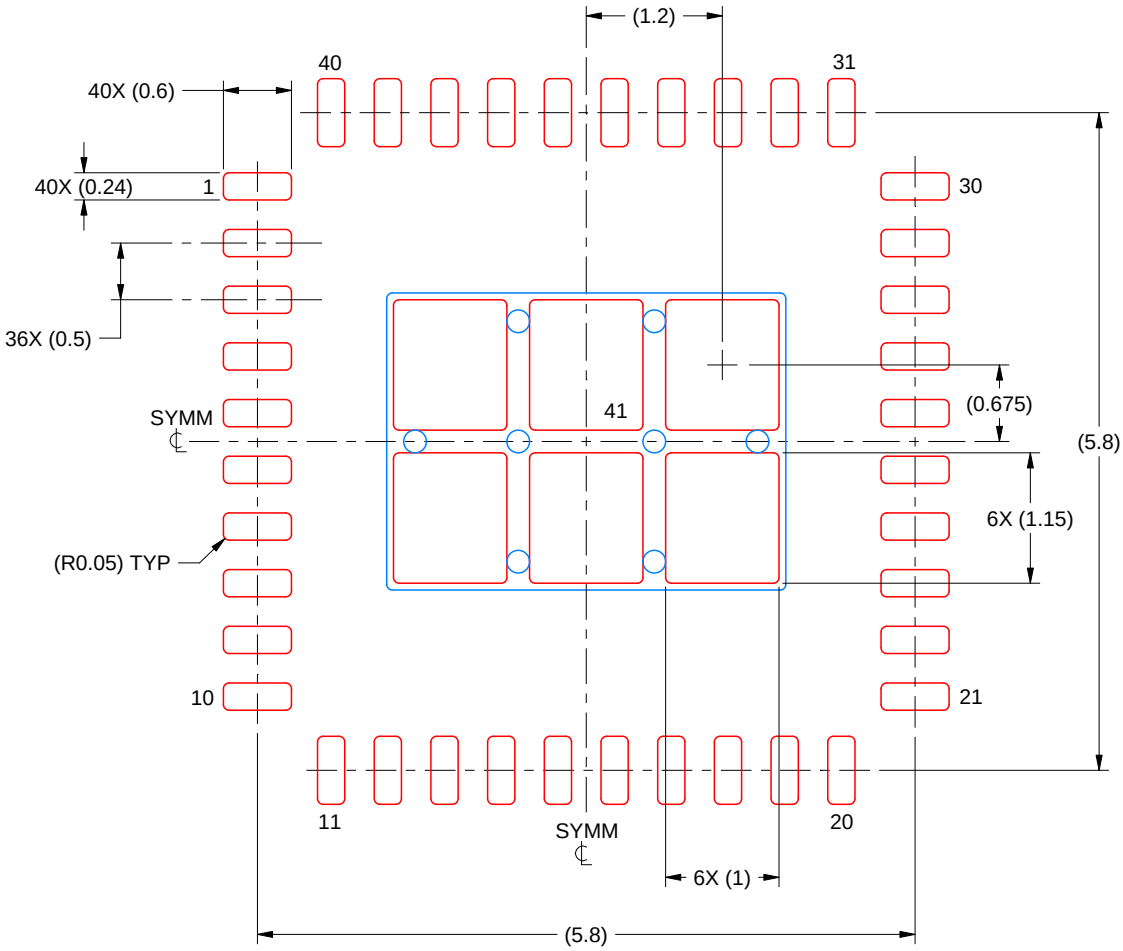
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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