TEXAS INSTRUMENTS

TPS62240, TPS62242, TPS62243

SLVS762C – JUNE 2007 – REVISED JULY 2015

TPS6224x 2.25-MHz 300-mA Step-Down Converter in 2 x 2 WSON and SOT Package

1 Features

- High Efficiency - Greater Than 94%
- Output Current up to 300 mA
- V_{IN} Range from 2 V to 6 V for Li-ion Batteries With Extended Voltage Range
- 2.25-MHz Fixed-Frequency Operation
- Power Save Mode at Light Load Currents
- Output Voltage Accuracy in PWM Mode ±1.5%
- Adjustable Output Voltage from 0.6 V to V_{IN}
- Typical 15-µA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Available in a SOT (5) and 2-mm × 2-mm × 0.8-mm WSON (6) Package
- Allows <1-mm Solution Height

2 Applications

- Bluetooth™ Headsets
- Mobile Phones, Smart Phones
- WLAN
- Low Power DSP Supplies
- Portable Media Players
- Digital Cameras

3 Description

The TPS6224x device is a highly efficient synchronous step-down DC-DC converter. The device provides up to 300-mA output current from a single Li-Ion cell and is ideal for battery powered portable applications like mobile phones and other portable equipment.

With an wide input voltage range of 2 V to 6 V, the device also supports two- and three-cell alkaline, 3.3-V and 5-V input voltage rails.

The TPS6224x operates at 2.25-MHz fixed switching frequency and enters power save mode operation at light load currents to maintain high efficiency over the entire load current range.

The power save mode is optimized for low output voltage ripple. For low-noise applications, the device can be forced into fixed-frequency pulse width modulation (PWM) mode by pulling the MODE pin high. In shutdown mode, the current consumption is reduced to less than 1 µA. The TPS6224x allows the use of small inductors and capacitors to achieve a small solution size.

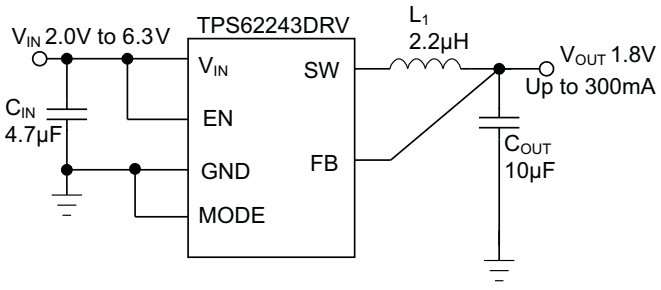
The TPS6224x operates over a free-air temperature range of –40°C to 85°C. The device is available in a 5-pin SOT and a 6-pin 2-mm × 2-mm WSON package.

Device Information(1)

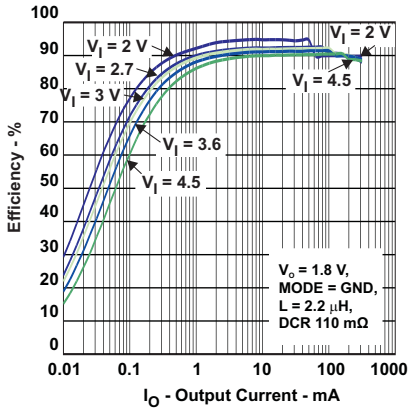
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6224x	WSON (6)	2.00 mm × 2.00 mm
	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2007) to Revision C	Page
• Changed editorial changes on bullets	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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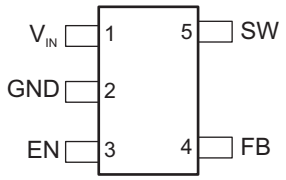
5 Device Options

PART NUMBER (1)	OUTPUT VOLTAGE (2)
TPS62240	adjustable
TPS62240	adjustable
TPS62242	1.2 V fixed output voltage
TPS62243	1.8 V fixed output voltage

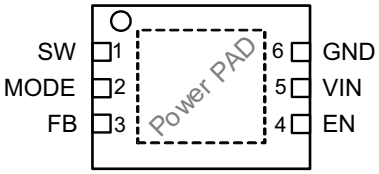
(1) The DDC (SOT 5 pin) and DRV (WSON 6 pin) packages are available in tape on reel. Add R suffix to order quantities of 3000 parts per reel.
(2) Contact TI for other fixed output voltage options.

6 Pin Configuration and Functions

DDC Package
5-Pin SOT
Top View



DRV Package
6-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	WSON	SOT		
EN	4	3	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
GND	6	2	PWR	GND supply pin.
FB	3	4	I	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor.
MODE	2	—	I	This pin is only available at WSON package option. MODE pin = High forces the device to operate in fixed-frequency PWM mode. MODE pin = Low enables the power save mode with automatic transition from PFM mode to fixed-frequency PWM mode.
SW	1	5	O	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.
VIN	5	1	PWR	V_{IN} power supply pin.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage (2)	–0.3	7	V
	Voltage at EN, MODE	–0.3	V_{IN} +0.3, ≤7	V
	Voltage on SW	–0.3	7	V
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3)	±1000	

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage, VIN	2		6	V
	Output voltage for adjustable voltage	0.6		V_{IN}	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6224x		UNIT
		DRV [WSON]	DDC [SOT]	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.8	226.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.5	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	48.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.6	48.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4,7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH, refer to parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2		6	V
I_{OUT}	Output current	2.3 V ≤ V_{IN} ≤ 6 V			300	mA
		2 V ≤ V_{IN} ≤ 2.3 V			150	
I_Q	Operating quiescent current	I_{OUT} = 0 mA. PFM mode enabled (MODE = GND) device not switching		15		µA
		I_{OUT} = 0 mA. PFM mode enabled (MODE = GND) device switching, V_{OUT} = 1.8 V, (1)		18.5		
		I_{OUT} = 0 mA, switching with no load (MODE = V_{IN}), PWM operation , V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.1	1	µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 6 V	1		V_{IN}	V
V_{IL}	Low level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET ON-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		240	480	mΩ
	Low-side MOSFET ON-resistance			180	380	
I_{LIMF}	Forward current-limit MOSFET high-side and low-side	V_{IN} = V_{GS} = 3.6 V	0.56	0.7	0.84	A
TSD	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN} ≤ 6 V	2	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Adjustable output voltage range		0.6		V_{IN}	V
V_{REF}	Reference voltage			600		mV
V_{FB}	Feedback voltage	MODE = V_{IN}, PWM operation, 2 V ≤ V_{IN} ≤ 6 V, in fixed output voltage versions V_{FB} = V_{OUT}, see (2)	–1.5%	0%	1.5%	
	Feedback voltage PFM mode	MODE = GND, device in PFM mode		0%		
	Load regulation	PWM mode		-0.5		%/A
$t_{Start\ Up}$	Start-up Time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW pin	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND, (3)		0.1	1	µA

(1) See the parameter measurement information.
(2) For V_{IN} = V_{OUT} + 0.6 .
(3) In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

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7.6 Typical Characteristics

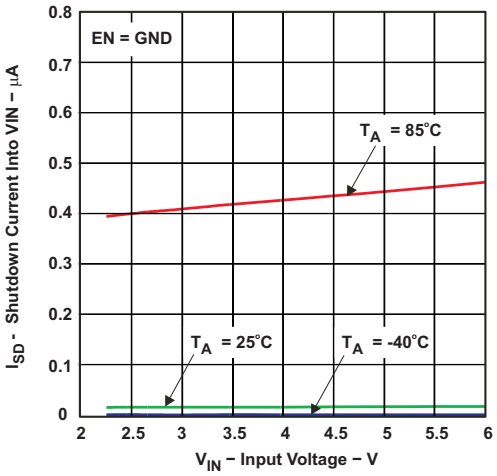


Figure 1. Shutdown Current Into VIN vs Input Voltage

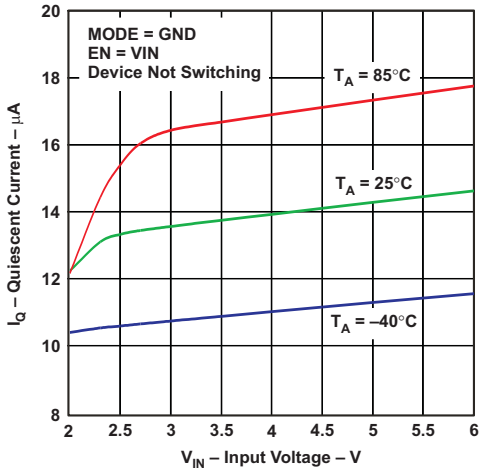


Figure 2. Quiescent Current vs Input Voltage

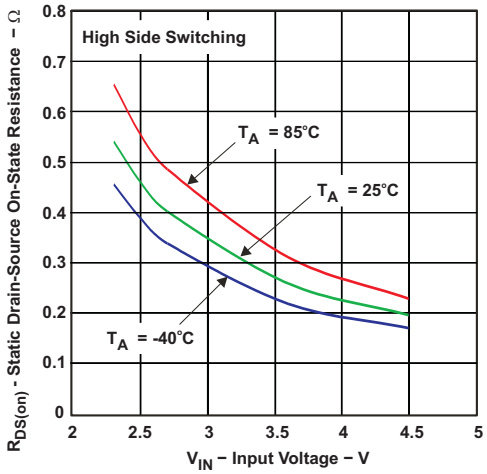


Figure 3. Static Drain-Source On-State Resistance vs Input Voltage

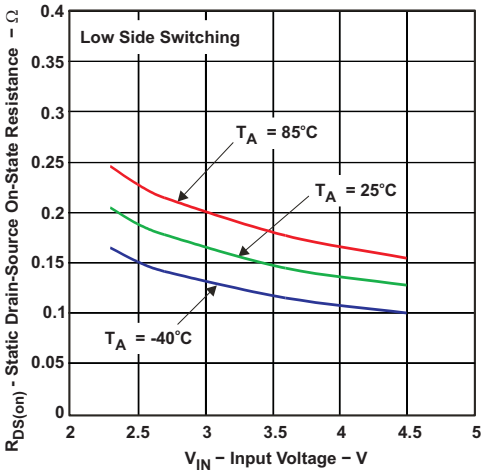


Figure 4. Static Drain-Source On-State Resistance vs Input Voltage

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8 Detailed Description

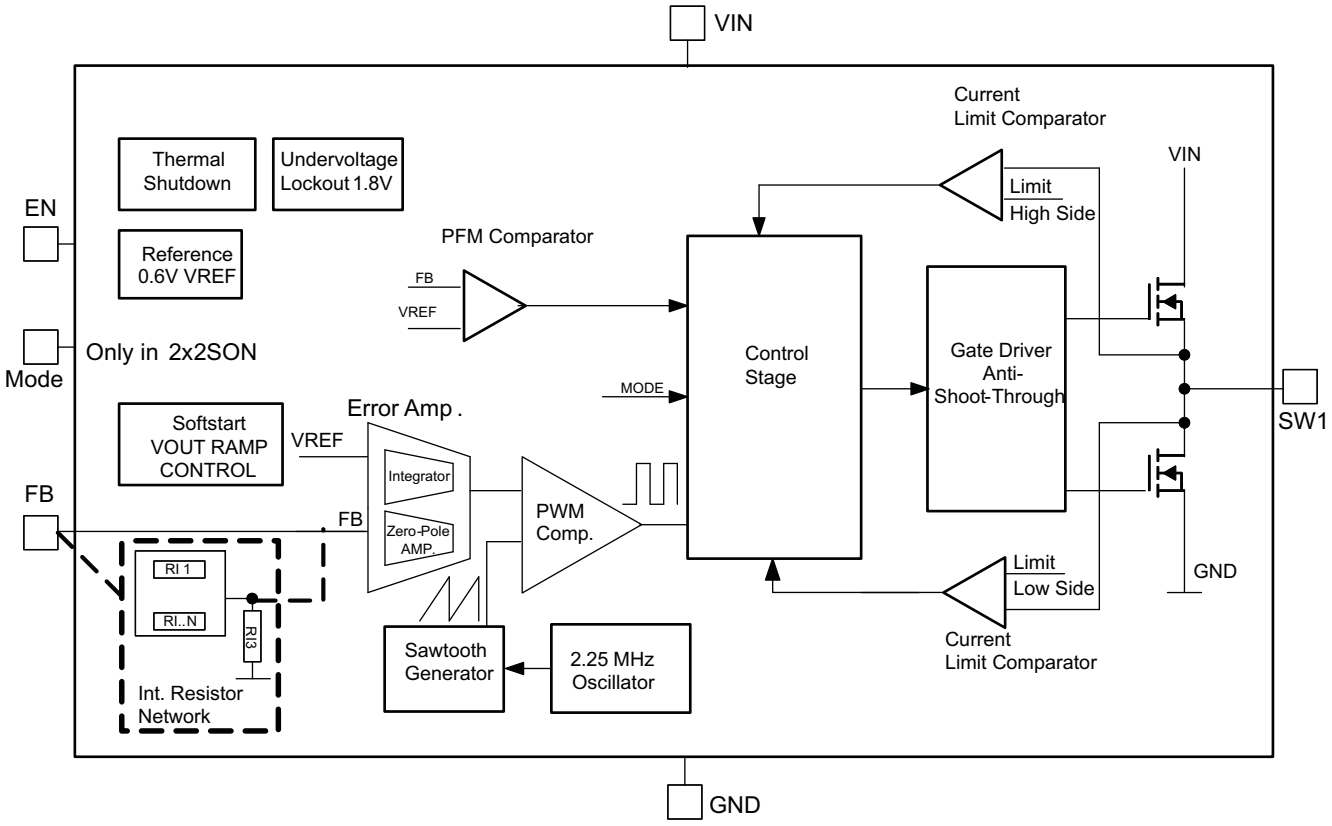
8.1 Overview

The TPS6224x step-down converter operates with typically 2.25-MHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power save mode and operates then in pulse frequency modulation (PFM) mode.

During PWM operation, the converter uses a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current then flows from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch if the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current then flows from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

Feature Description (continued)

8.3.2 Mode Selection

The MODE pin allows mode selection between forced PWM mode and power save mode.

Connecting this pin to GND enables the power save mode with an automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

8.3.3 Enable

The device is enabled by setting the EN pin to high. During the start up time $t_{Start\ Up}$, the internal circuits are settled and the soft start circuit is activated. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN pin = GND, the device enters shutdown mode in which all circuits are disabled. In fixed output voltage versions, the internal resistor divider network is then disconnected from FB pin.

8.3.4 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

8.4 Device Functional Modes

8.4.1 Soft Start

The TPS6224x has an internal soft-start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250 µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft-start circuit is enabled within the start-up time, $t_{Start\ up}$.

8.4.2 Power Save Mode

The power save mode is enabled with MODE pin set to low level. If the load current decreases, the converter will enter power save mode operation automatically. During power save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal, the device starts a PFM current pulse. The high-side MOSFET switch will turn on, and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal to or greater than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

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Device Functional Modes (continued)

With a fast single-threshold comparator, the output voltage ripple during PFM mode operation can be kept to a minimum. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency both depend on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

If the output current cannot be supported in PFM mode, the device exits PFM mode and enters PWM mode. The power save mode can be disabled through the MODE pin set to high. The converter will then operate in fixed-frequency PWM mode.

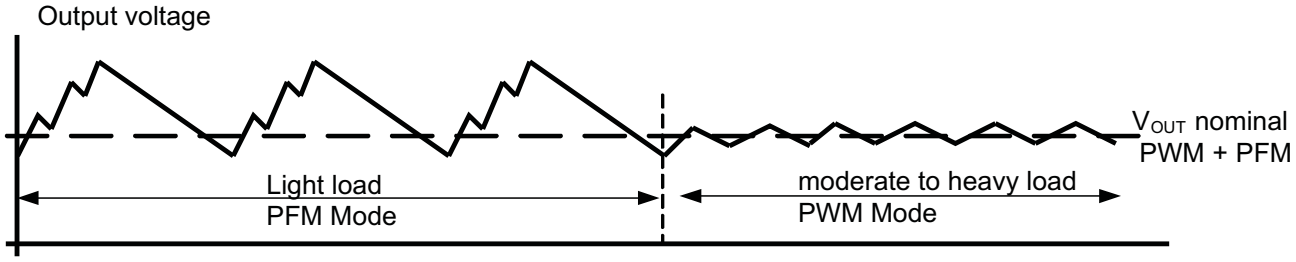


Figure 5. Power Save Mode

8.4.3 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the entire battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times R_{DS(on)}max + R_L \quad (1)$$

where

- $I_{OUT}max$ = Maximum output current plus inductor ripple current
- $R_{DS(on)}max$ = Maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_{OUT}max$ = Nominal output voltage plus maximum output voltage tolerance

8.4.4 Short-Circuit Protection

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current equal to I_{LIMF}. The current in the switches is monitored by current-limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of its current-limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again, once the current in the low-side MOSFET switch has decreased below the threshold of its current-limit comparator.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6224x device is a high-efficiency synchronous step-down DC-DC converter featuring power save mode or 2.25-MHz fixed-frequency operation.

9.2 Typical Application

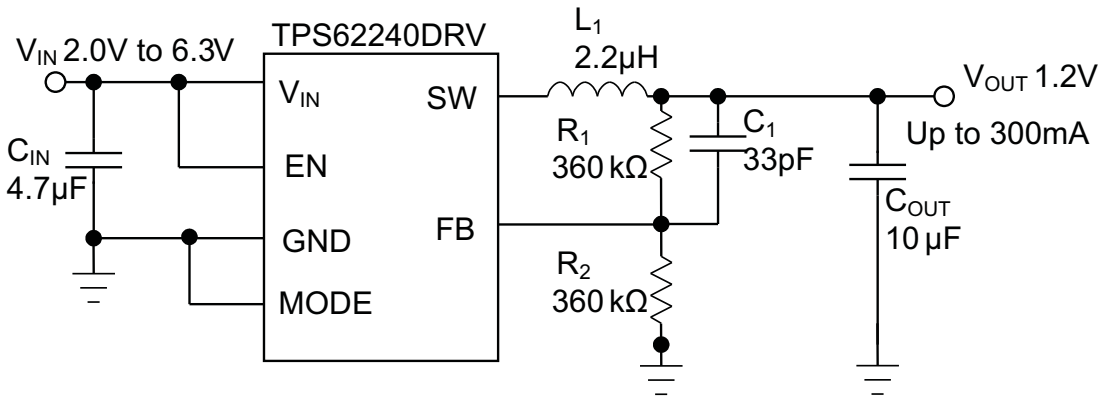


Figure 6. TPS62240DRV Adjustable 1.2 V

9.2.1 Design Requirements

The device operates over an input voltage range from 2 V to 6 V. The output voltage is adjustable using an external feedback divider.

9.2.2 Detailed Design Procedure

Table 1 shows the list of components for the *Application Curves*.

Table 1. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_{IN}	GRM188R60J475K	Murata	4.7 µF, 6.3 V. X5R Ceramic
C_{OUT}	GRM188R60J106M	Murata	10 µF, 6.3 V. X5R Ceramic
C_1		Murata	22 pF, COG Ceramic
L_1	LPS3015	Coilcraft	2.2 µH, 110 mΩ
R_1, R_2	Values depending on the programmed output voltage		

9.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$ with an internal reference voltage V_{REF} typical 0.6 V. (2)

To minimize the current through the feedback divider network, R_2 should be 180 kΩ or 360 kΩ. The sum of R_1 and R_2 should not exceed approximately 1 MΩ, to keep the network robust against noise.

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An external feedforward capacitor C_1 is required for optimum load transient response. The value of C_1 should be in the range from 22 pF to 33 pF.

Route the FB line away from noise sources, such as the inductor or the SW line.

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The TPS6224x is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The device is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1-µH effective inductance and 3.5-µF effective capacitance. Selecting larger capacitors is less critical because the corner frequency of the L-C filter moves to lower frequencies with fewer stability problems.

9.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

The inductor selection also has an impact on the output voltage ripple in the PFM mode. Higher inductor values will lead to lower output voltage ripple and higher PFM frequency, and lower inductor values will lead to a higher output voltage ripple but lower PFM frequency.

Equation 3 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transients the inductor current will rise above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{3}$$

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \tag{4}$$

where

- f = Switching frequency (2.25-MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the maximum switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC-DC conversion and consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

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Table 2. List of Inductors

DIMENSIONS (mm^3)	INDUCTANCE (µH)	INDUCTOR TYPE	SUPPLIER
2.5 × 2 × 1	2	MIPS2520D2R2	FDK
2.5 × 2 × 1.2	2	MIPSA2520D2R2	FDK
2.5 × 2 × 1	2.2	KSLI-252010AG2R2	Hitachi Metals
2.5 × 2 × 1.2	2.2	LQM2HPN2R2MJ0L	Murata
3 × 3 × 1.4	2.2	LPS3015	Coilcraft

9.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6224x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance overtemperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (6)$$

At light load currents, the converter operates in power save mode and the output voltage ripple depends on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

9.2.2.2.3 Input Capacitor Selection

The buck converter has a natural pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended. Because ceramic capacitors lose up to 80% of their initial capacitance at 5 V, it is recommended that a 10-µF input capacitor be used for input voltages greater than 4.5 V. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input, and the power is being supplied through long wires, such as from a wall adapter, a load step at the output, or V_{IN} step on the input, can induce ringing at the VIN pin. The ringing can couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE	SUPPLIER
4.7 µF	GRM188R60J475K	0603: 1.6 × 0.8 × 0.8 mm^3	Murata
10 µF	GRM188R60J106M69D	0603: 1.6 × 0.8 × 0.8 mm^3	Murata

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9.2.3 Application Curves

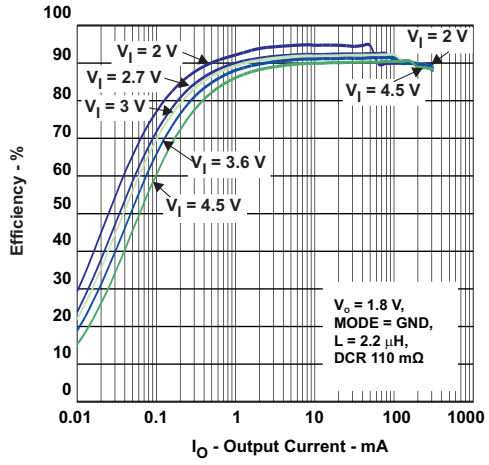


Figure 7. Efficiency (Power Save Mode) vs Output Current

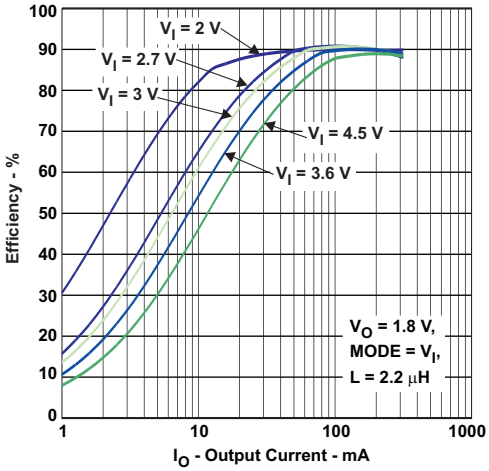


Figure 8. Efficiency (Forced PWM Mode) vs Output Current

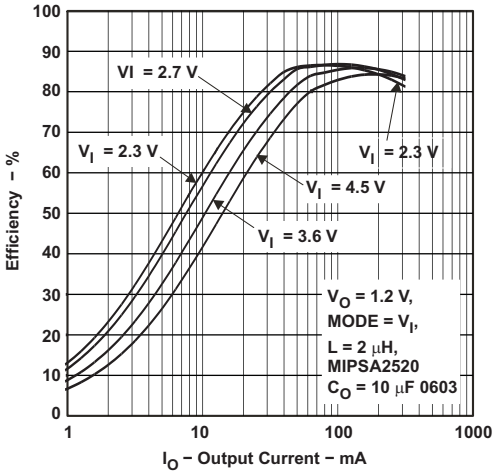


Figure 9. Efficiency vs Output Current

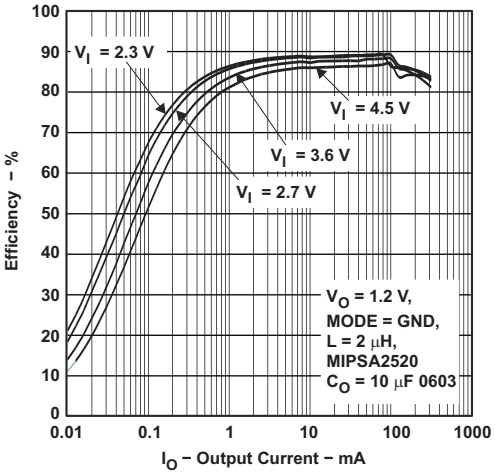


Figure 10. Efficiency vs Output Current

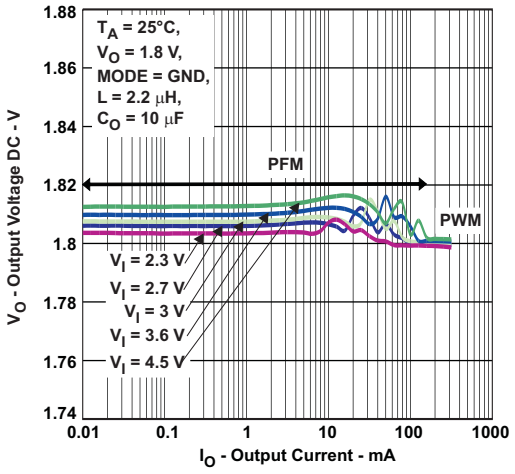


Figure 11. Output Voltage Accuracy vs Output Current

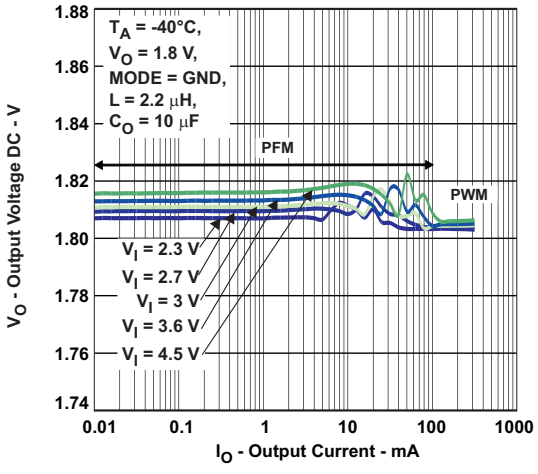


Figure 12. Output Voltage Accuracy vs Output Current

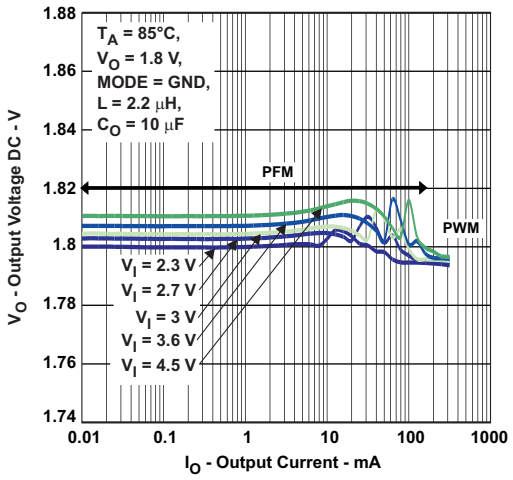


Figure 13. Output Voltage Accuracy vs Output Current

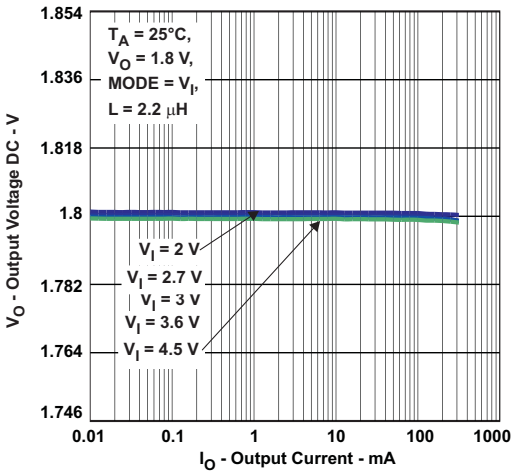


Figure 14. Output Voltage Accuracy vs Output Current

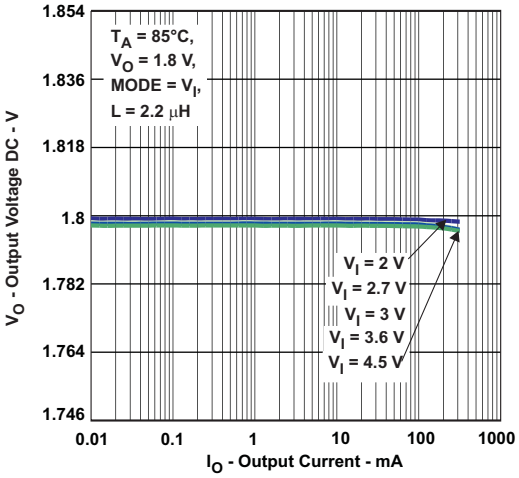


Figure 15. Output Voltage Accuracy vs Output Current

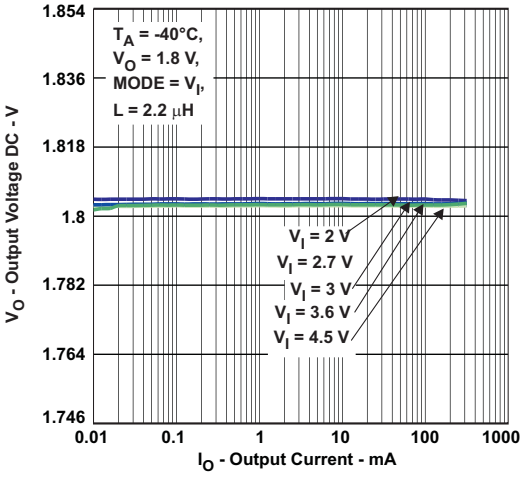


Figure 16. Output Voltage Accuracy vs Output Current

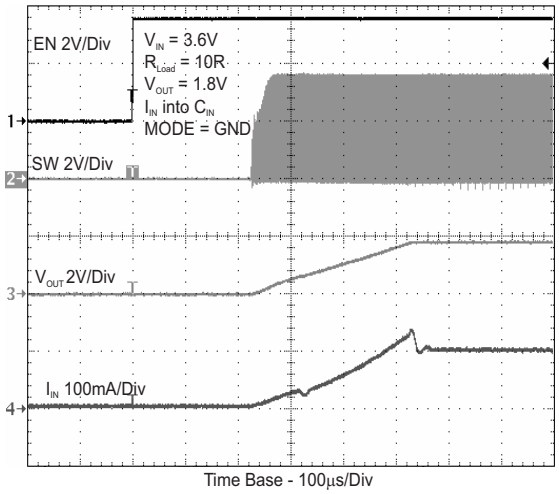


Figure 17. Start-Up Timing

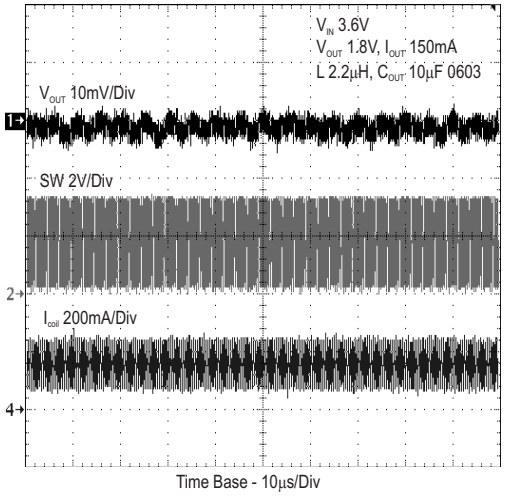


Figure 18. Typical Operation vs PWM Mode

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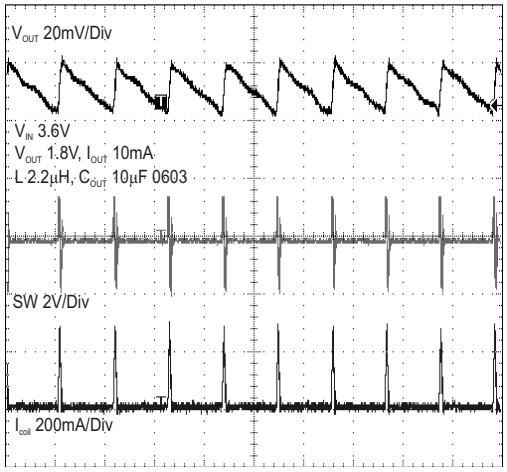


Figure 19. Typical Operation vs PFM Mode

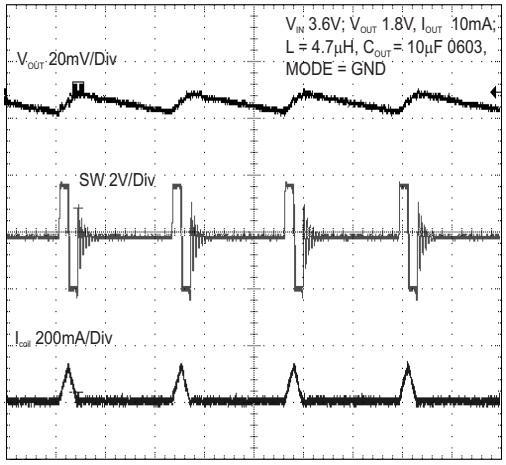


Figure 20. PFM Mode Ripple

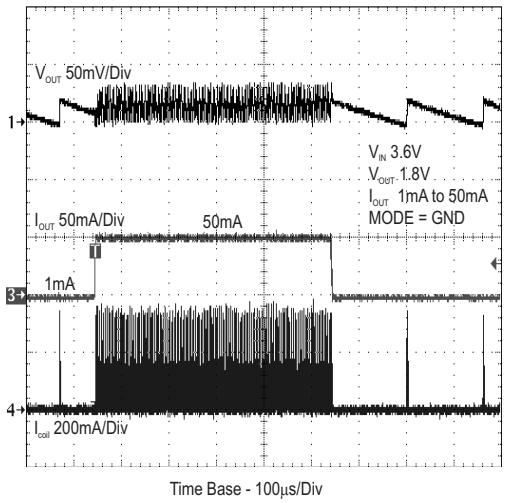


Figure 21. PFM Load Transient

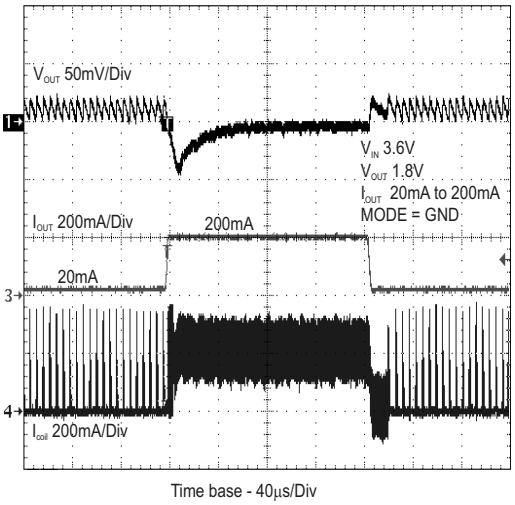


Figure 22. PFM Load Transient

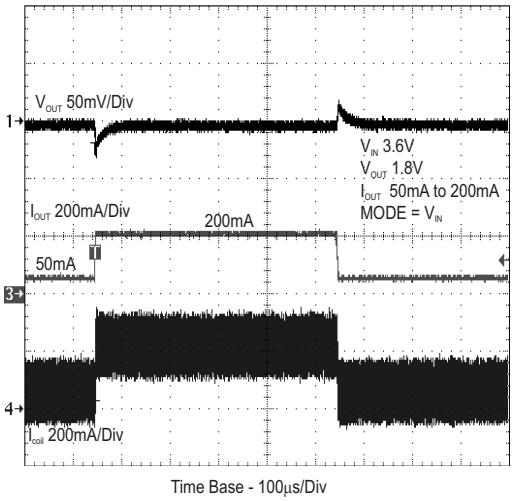


Figure 23. PFM Load Transient

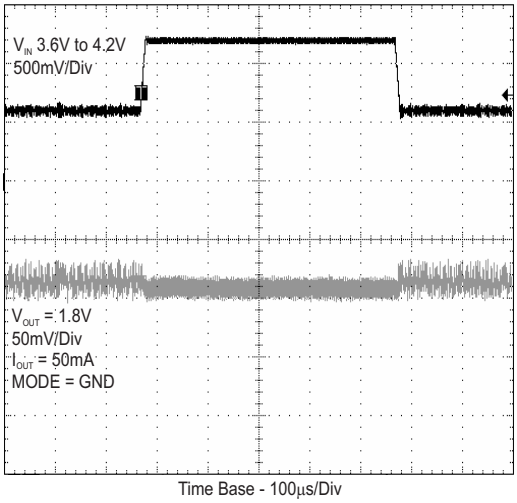


Figure 24. PFM Line Transient

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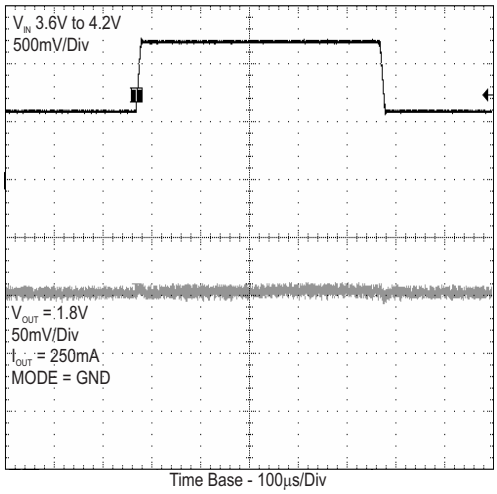


Figure 25. PFM Line Transient

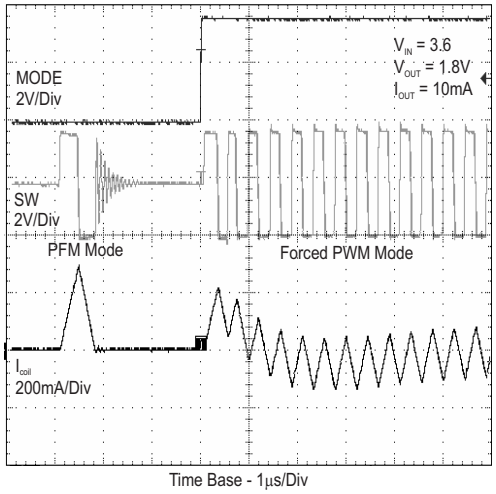


Figure 26. Mode Transition PFM to PWM

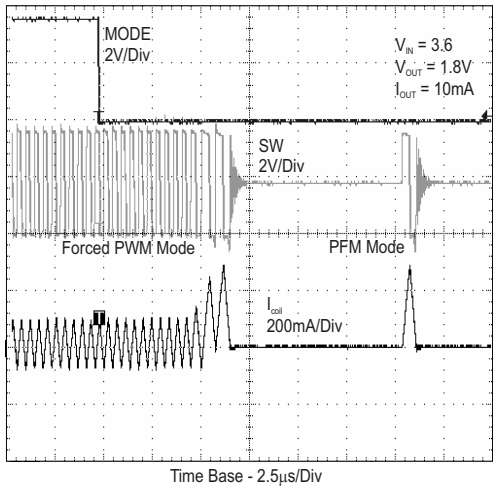


Figure 27. Mode Transition PWM to PFM

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9.3 System Examples

9.3.1 TPS62240, Adjustable Output Voltage 1.8 V

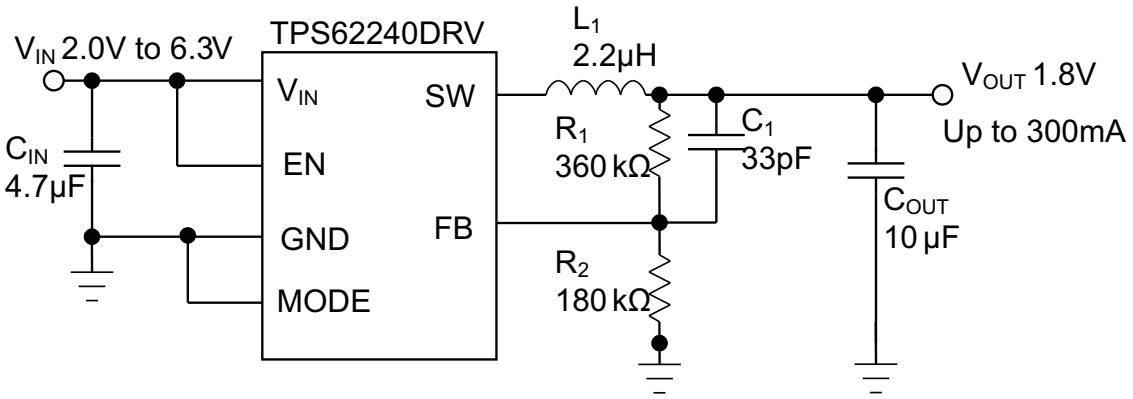


Figure 28. TPS62240DRV 1.8 V

9.3.2 TPS62243, Fixed Output Voltage 1.8 V

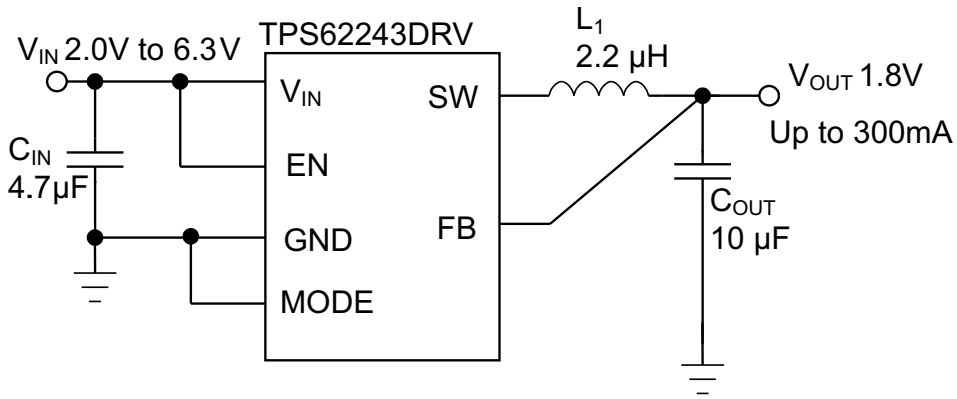


Figure 29. TPS62243 Fixed 1.8 V

10 Power Supply Recommendations

The TPS6224x device has no special requirements for its input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS6224x.

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11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, and additional stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD land (star point) underneath the IC. Keep the common path to the GND pin, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (for example, the SW line).

11.2 Layout Examples

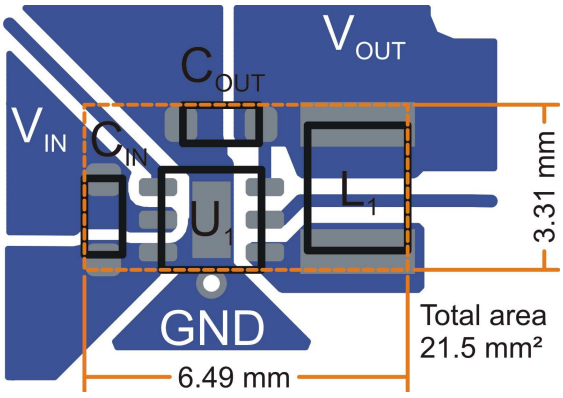


Figure 30. Suggested Layout for Fixed Output Voltage Options

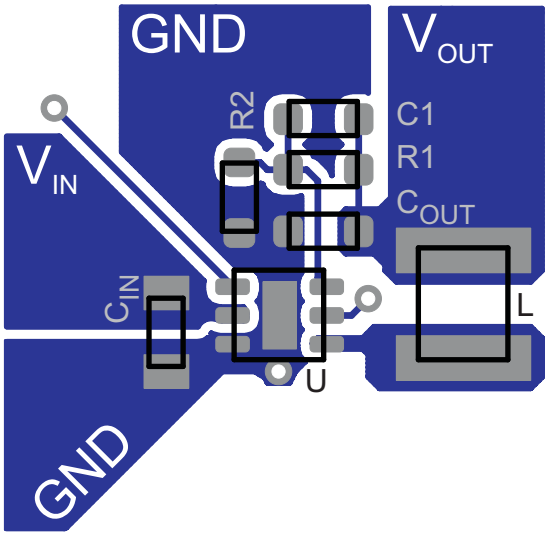


Figure 31. Suggested Layout for Adjustable Output Voltage Version

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62240	Click here	Click here	Click here	Click here	Click here
TPS62242	Click here	Click here	Click here	Click here	Click here
TPS62243	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62240DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BYO
TPS62240DDCR.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	BYO
TPS62240DDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	BYO
TPS62240DDCRG4	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	BYO
TPS62240DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYO
TPS62240DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYO
TPS62240DDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYO
TPS62240DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYJ
TPS62240DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYJ
TPS62240DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYJ
TPS62240DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYJ
TPS62240DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYJ
TPS62240DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYJ
TPS62240DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BYJ
TPS62242DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	CCY
TPS62242DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCY
TPS62242DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCY
TPS62242DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	CCY
TPS62242DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCY
TPS62242DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCY
TPS62243DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	CBQ
TPS62243DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBQ
TPS62243DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBQ
TPS62243DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	CBQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62243DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBQ
TPS62243DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBQ
TPS62243DRVTG4	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBQ
TPS62243DRVTG4.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBQ
TPS62243DRVTG4.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62242, TPS62243 :

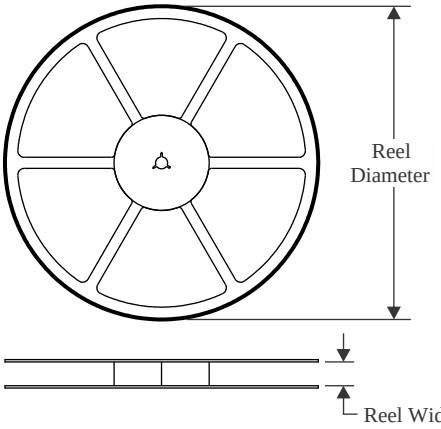
- Automotive : TPS62242-Q1, TPS62243-Q1

NOTE: Qualified Version Definitions:

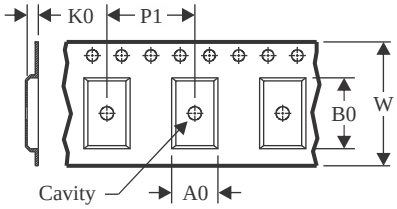
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

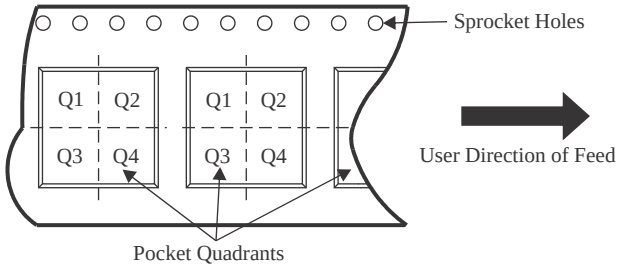


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

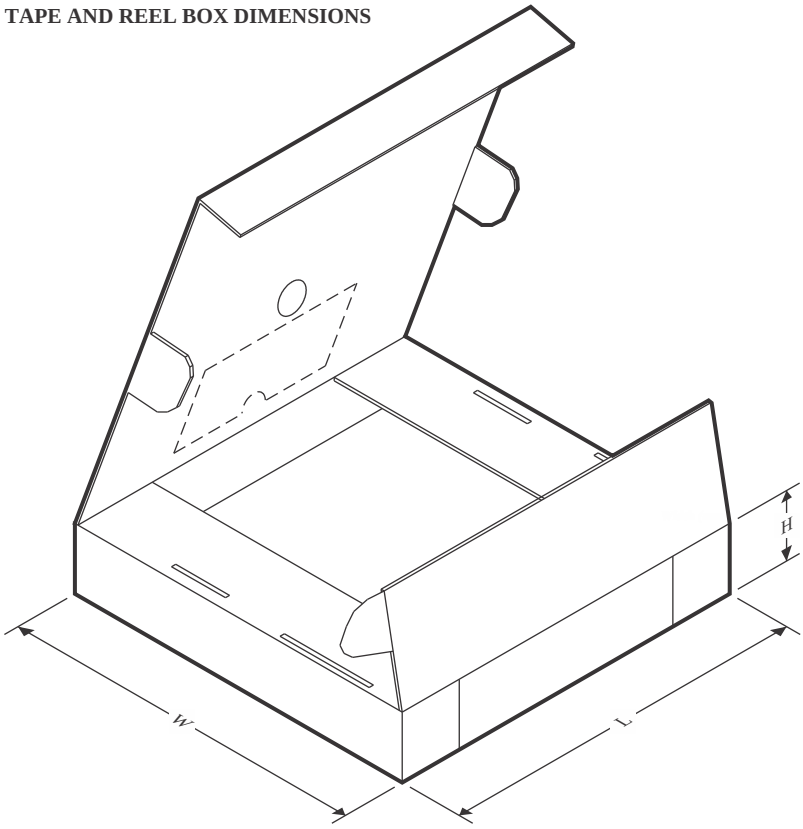
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62240DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62240DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62240DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62240DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62240DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62240DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62242DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62242DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62243DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62243DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62243DRVTG4	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

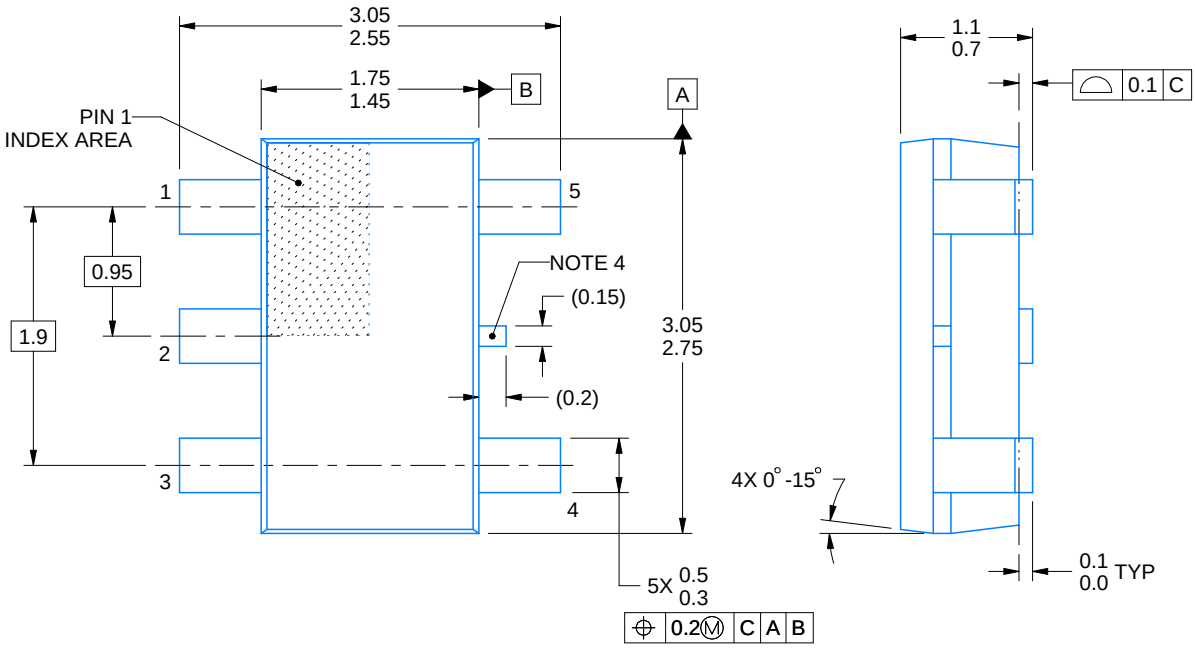
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62240DDCR	SOT-23-THIN	DDC	5	3000	210.0	185.0	35.0
TPS62240DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS62240DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS62240DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62240DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS62240DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS62242DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62242DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS62243DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62243DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS62243DRVTG4	WSON	DRV	6	250	210.0	185.0	35.0

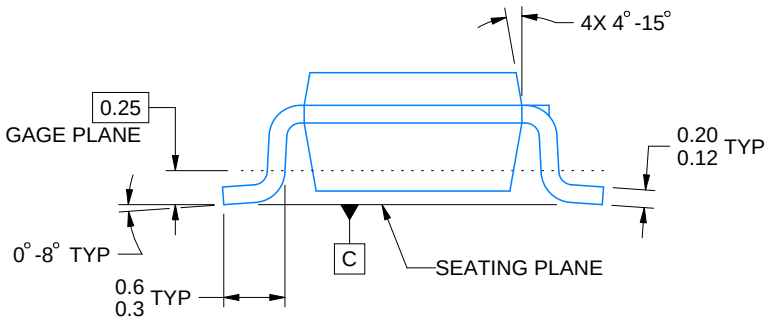
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

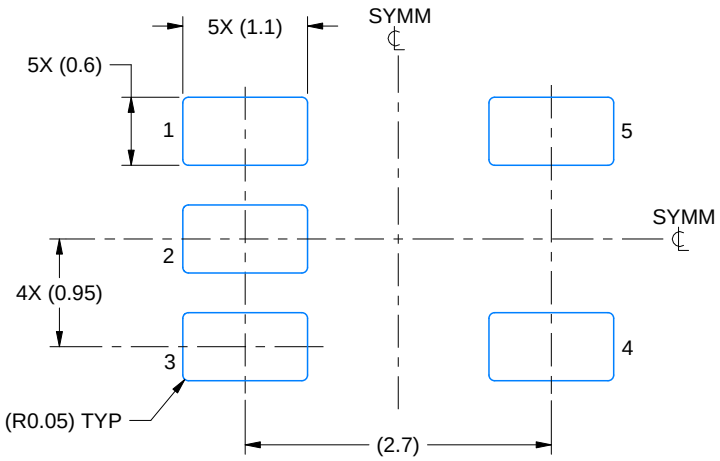




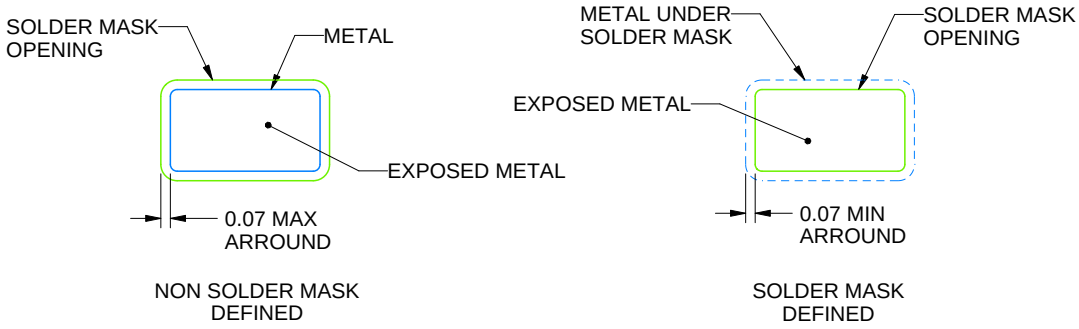
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

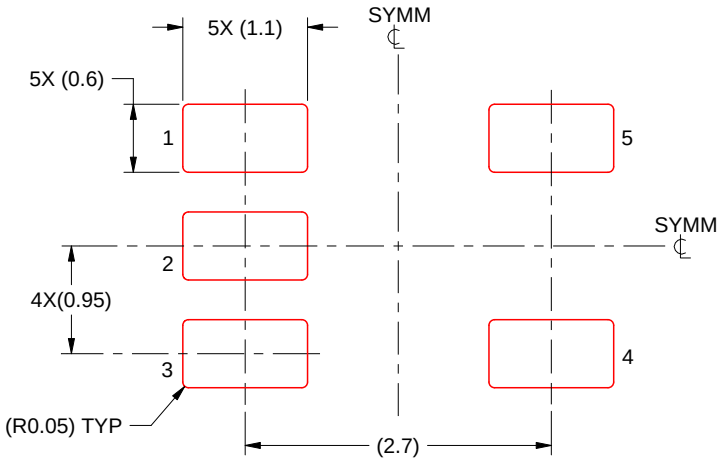


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

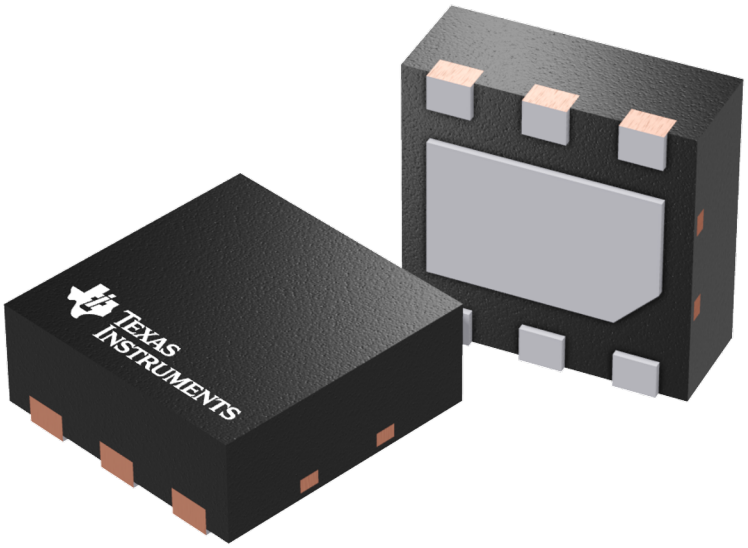
4220752/C 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



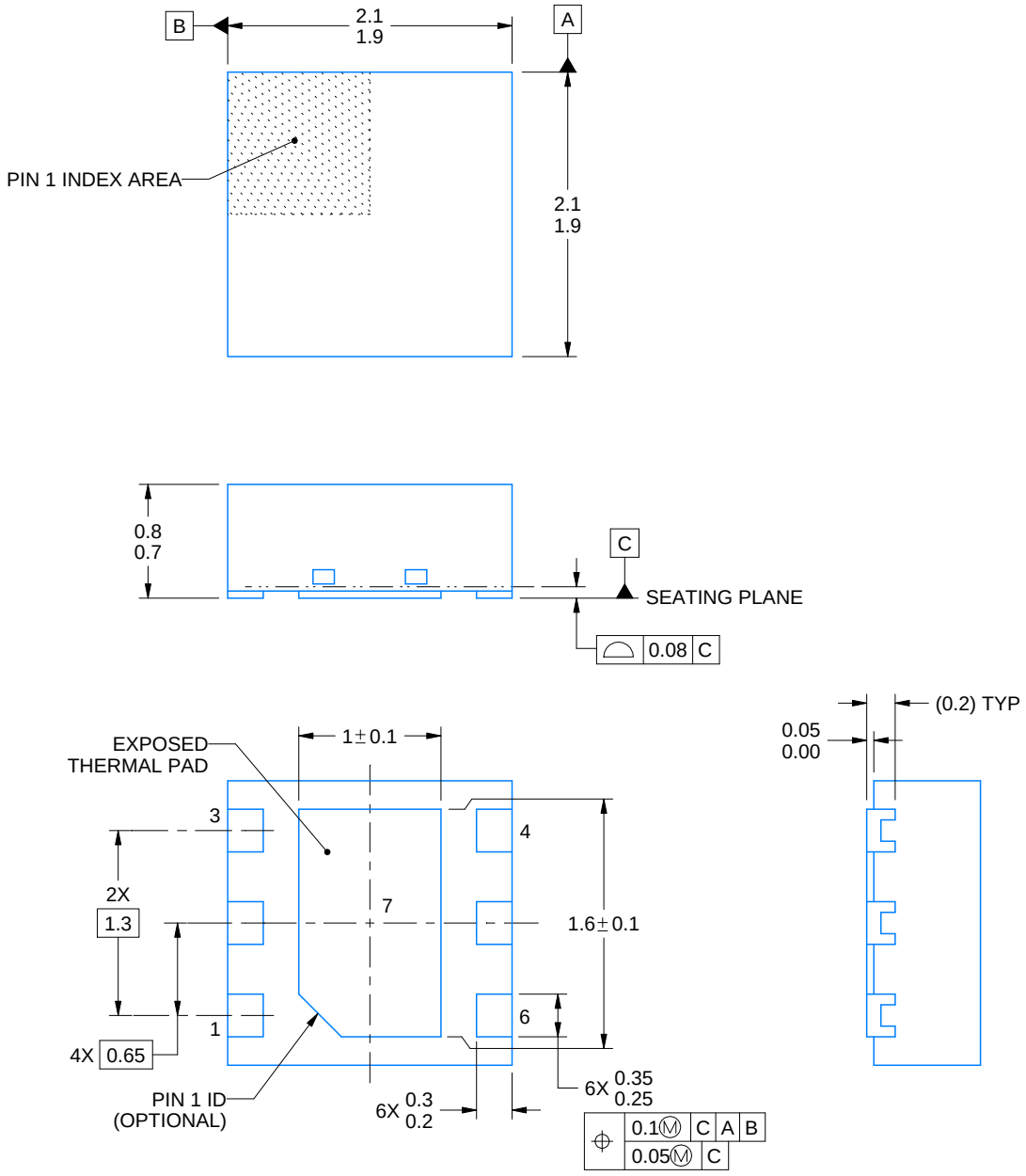
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

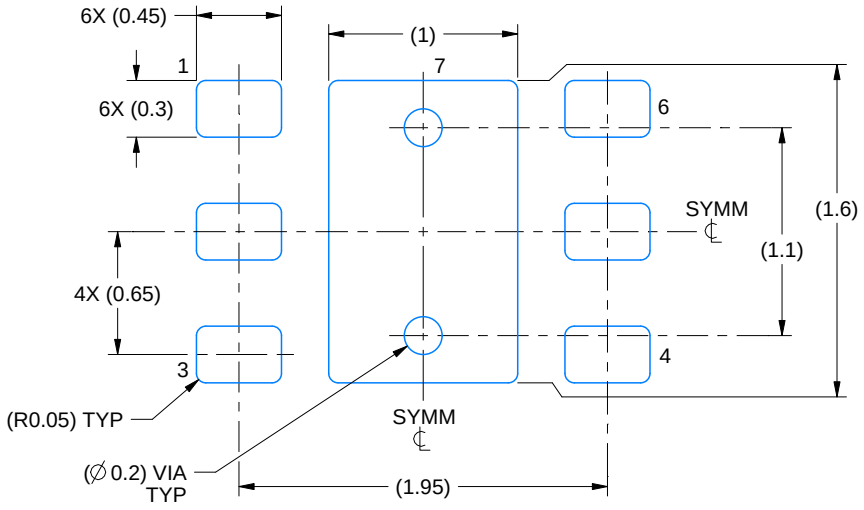
PLASTIC SMALL OUTLINE - NO LEAD



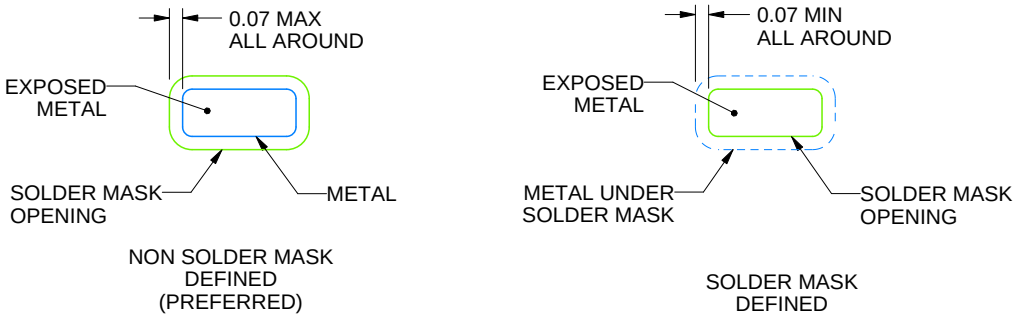
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

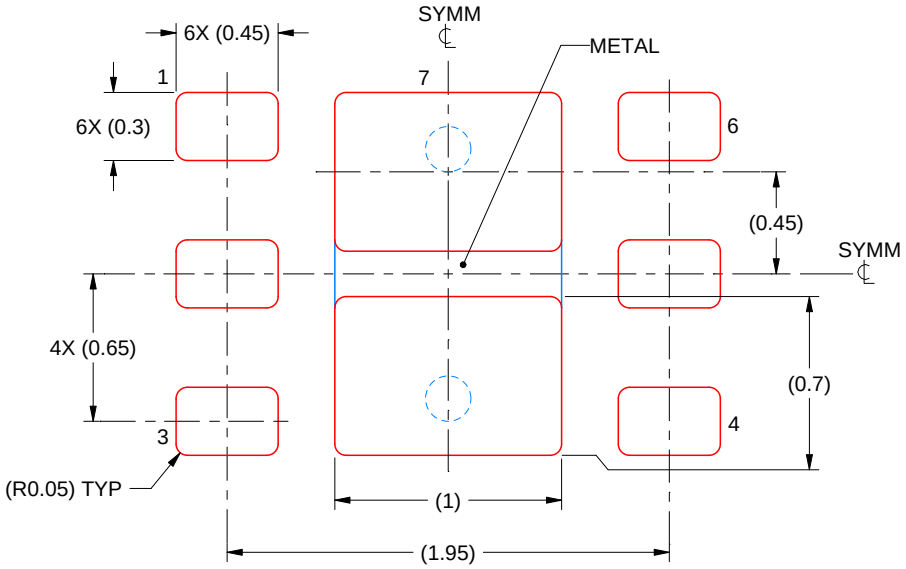


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



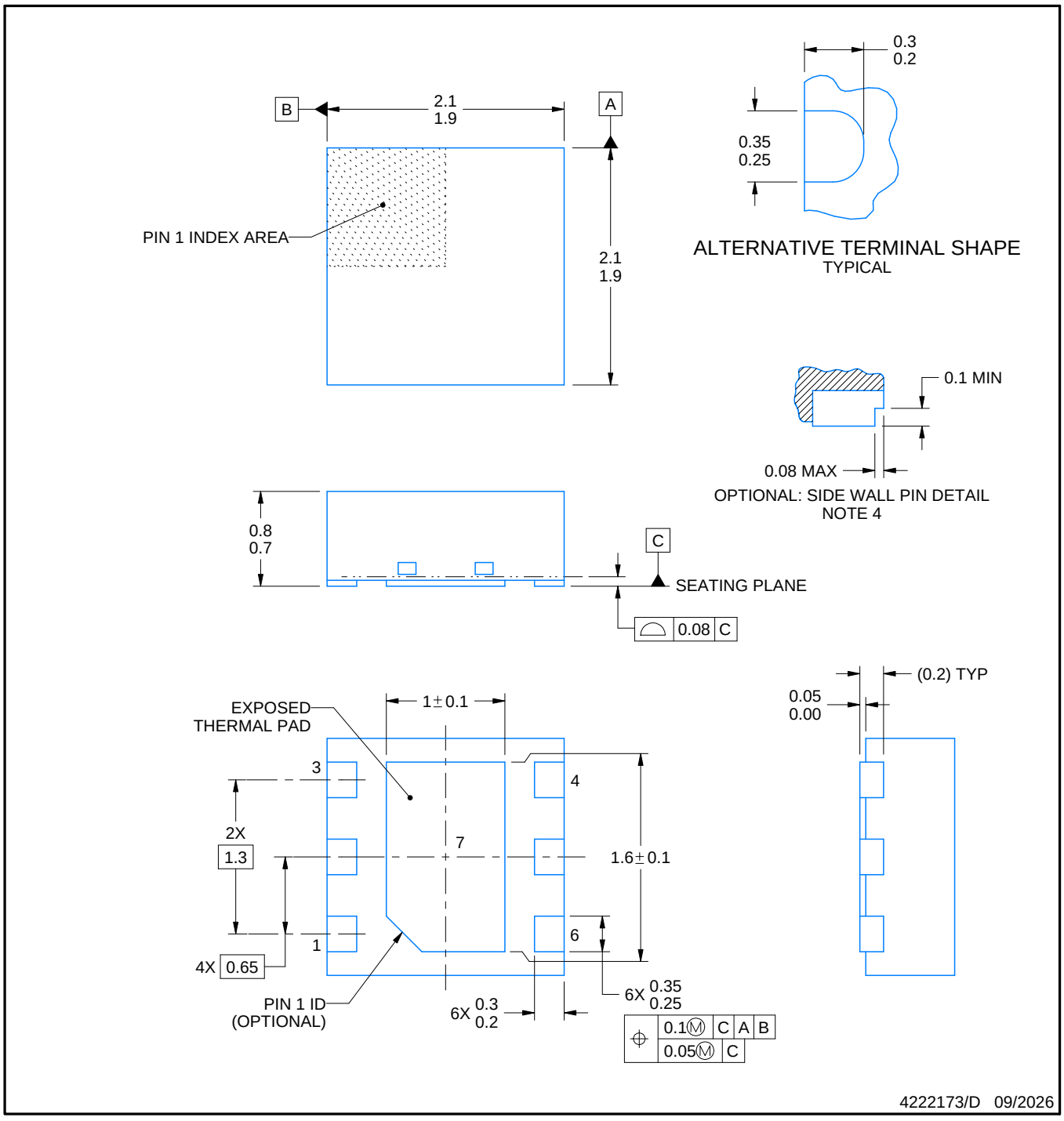
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

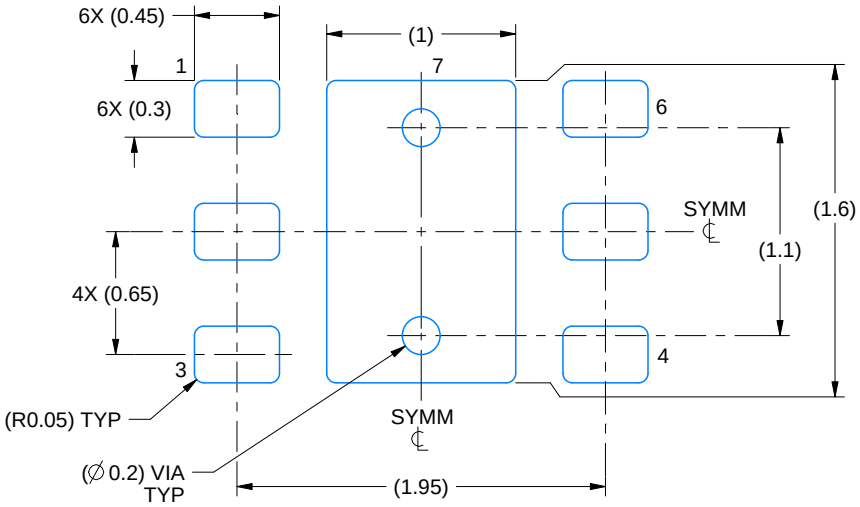
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

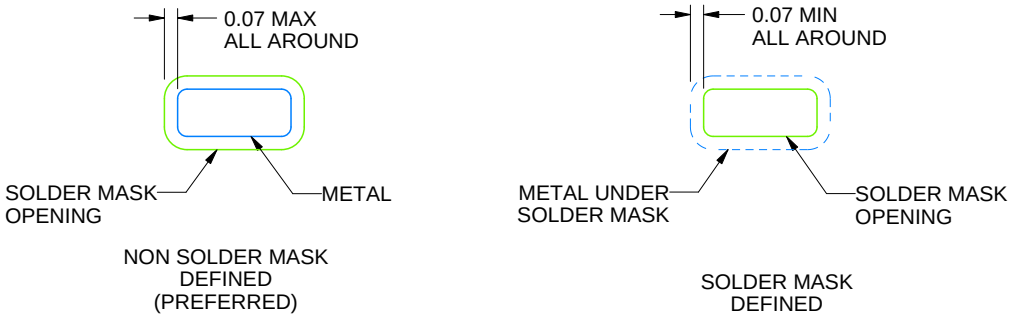


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

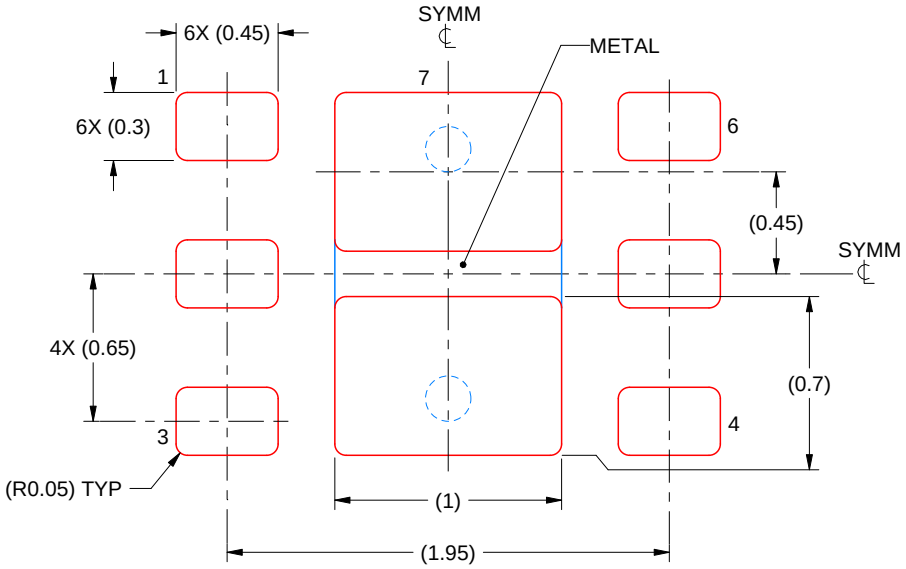


SOLDER MASK DETAILS

4222173/D 09/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/D 09/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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