TPS61388-Q1 36-VIN ,30-VOUT, Low-IQ, 8A ISW, Fully Integrated Synchronous Boost Converter with Pass-through

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1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Wide input voltage and output operation range
  - Input voltage range: 2V to 36V
  - 2.4V minimum for startup
  - Boost mode output voltage range : 5V to 30V
  - Pass-through mode output voltage up to 36V
  - Fixed output options: 10V, 8.5V, and 6.5V
- Pass-through operation when VIN>VOUT_SET
  - Typical 65µA quiescent current in Pass-through
  - Constant frequency when entering and exiting pass-through (TPS61388-Q1)
  - Frequency foldback when entering and exiting pass-through (TPS613881-Q1)
- Avoid AM band interference and crosstalk
  - Optional switching 400kHz or 2.2MHz by FSW pin
  - Optional clock synchronization
  - Spread spectrum frequency modulation
- High efficiency and power capability
  - Peak current limit: 8A
  - Low-side FET: 30mΩ, high-side FET: 25mΩ
- Minimized light load current consumption
  - Typical 30µA quiescent current into VIN pin
  - Typical 2µA quiescent current into VOUT pin
  - Maximum 1.25µA shutdown current into VIN pin
  - Selectable forced PWM mode, auto PFM mode
- Lead-less HotRod™ Lite package
- Integrated protection features
  - Cycle-by-cycle peak current limit
  - Output overvoltage protection
  - Power good indicator
  - Thermal shutdown protection at 170°C

2 Applications

- Pre-Boost for automotive Start-Stop/Cold crank
- Automotive infotainment and cluster
- Automotive camera ultrasonic cleaning system
- Land mobile

3 Description

The TPS61388-Q1 is a 36V, 8A automotive fully-integrated synchronous boost converter with pass-through feature. The converter supports absmax voltage up to 40V while the max boost output voltage covers up to 30V.

The TPS61388-Q1 employs peak current mode control scheme with frequency options of 400kHz and 2.2MHz, and is capable of synchronized to an external clock. There are two optional modes at light load through MODE/SYNC pin configuring: Auto PFM mode and Forced PWM mode to balance the efficiency and noise immunity.

The device features low shutdown current and low quiescent current Pass-through operation, eliminates the need for an external bypass switch when the supply voltage is greater than output target.

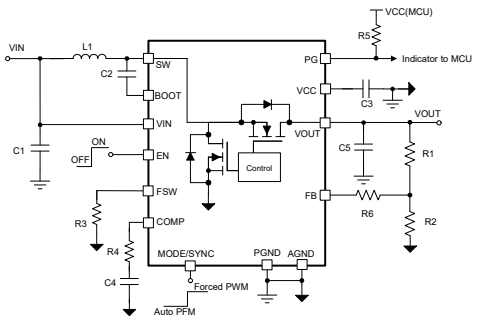
The TPS61388-Q1 has various fixed output voltage versions to save the external components. TPS61388-Q1 supports the external loop compensation so that the stability and transient response is optimized.

The device has built-in protection features like peak current limit, overvoltage protection, and thermal shutdown. External clock synchronization, spread spectrum modulation, and a lead-less package with minimal parasitic help to reduce EMI. The TPS61388-Q1 is available in a 3.0mm × 2.5mm HotRod™ Lite WQFN package with wettable flank.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)
TPS61388-Q1	WQFN-16	3.0mm × 2.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE (V)	OUTPUT VOLTAGE SELECTION RESISTOR (R_{FB})(1)	Frequency Foldback to 400kHz when entering &exiting Pass-through
TPS61388-Q1	10	$0\Omega \le R_{FB} \le 2.2k\Omega$	Disable
	8.5	$3.55k\Omega \le R_{FB} \le 9.25k\Omega$	
	6.5	$12k\Omega \le R_{FB} \le 21k\Omega$	
	Adjustable	$R_{FB} \ge 27k\Omega$	
TPS613881-Q1(2)	10	$0\Omega \le R_{FB} \le 2.2k\Omega$	Enable
	8.5	$3.55k\Omega \le R_{FB} \le 9.25k\Omega$	
	6.5	$12k\Omega \le R_{FB} \le 21k\Omega$	
	Adjustable	$R_{FB} \ge 27\Omega$	

(1) R_{SEL} is the sensed resistor from FB pin. Please refer to for details. Avoid using resistors other than the recommended values, otherwise the output voltage value is not guaranteed.
(2) Product Preview. Contact TI factory for more information.

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5 Pin Configuration and Functions

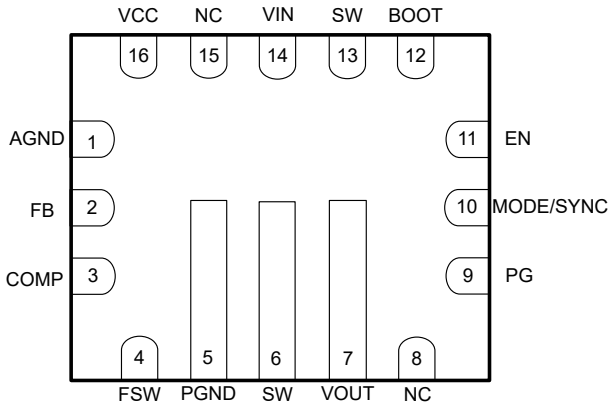

Figure 5-1. TPS61388-Q1 VAS Package, 16-Pin WQFN (Transparent Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	1	PWR	Analog ground of the IC.
FB	2	I	Feedback pin. Use a resistor divider to set the desired output voltage. Refer to Section 8.2.2.1 for more information.
COMP	3	O	Output of the internal transconductance error amplifier. An external RC network is connected to this pin to optimize the loop stability and response time.
FSW	4	I	Frequency setting pin. See Section 7.3.5 for more information.
PGND	5	PWR	Power ground of the IC. It is connected to the source of the low-side FET.
SW	6, 13	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side FET and the source of the high-side FET.
VOUT	7	PWR	Output of the drain of the HS FET.
NC	8,15	/	No connection. NC pin provides additional clearance spacing for FMEA consideration.
PG	9	O	Power good indicator and open drain output. If not used, leave the pin floating or connected to GND.
MODE/SYNC	10	I	Mode selection pin. This pin is not allowed to be floating. MODE/SYNC= high, Forced PWM mode MODE/SYNC = low, Auto PFM mode This pin is capable to be used to synchronize the external clock. Refer to Section 7.3.8 for details.
EN	11	I	Enable logic input.
BOOT	12	O	Power supply for high-side N-MOSFET gate drivers. A capacitor of 100nF is needed between this pin and the SW pin.
VIN	14	I	IC power supply input.
VCC	16	O	Output of internal regulator. A ceramic capacitor with more than 1µF is needed between this pin and GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, SW, VOUT	-0.3	40	V
Voltage range at terminals (2)	BOOT	–0.3	SW + 6.0	
Voltage range at terminals (2)	MODE/SYNC, FB, EN, FSW, VCC, COMP	–0.3	6.0	
Voltage range at terminals (2)	PG	–0.3	6.0	
T_J (3)	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 125°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(2)	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins(3)	±500	
$V_{(ESD)}$ (1)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, corner pins (3)	±750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		36	V
V_{OUT}	Outputvoltage, boost mode, switching	5		30	V
V_{OUT}	Outputvoltage, passthrough mode, not switching	VIN		36	V
T_J	Operating junction temperature(1)	–40		150	°C

(1) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE		UNIT
		VAS(JEDEC)	VAS(EVM)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.8	46.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.1	Not Applicable	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	Not Applicable	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	21.5	°C/W

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6.4 Thermal Information (continued)

THERMAL METRIC(1)		DEVICE		UNIT
		VAS(JEDEC)	VAS(EVM)	
		14 PINS	14 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	Not Applicable	Not Applicable	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = -40 to 150°C, L = 2.2µH, V_{IN} = 12V and V_{OUT} = 24V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2		36	V
V_{IN_UVLO}	VIN under voltage lockout threshold	V_{IN_UVLO} rising		2.35	2.4	V
		V_{IN_UVLO} falling		1.9	2.0	V
V_{CC}	VCC regulation	I_{VCC} = 10mA, V_{OUT} = 18V		5.1	5.5	V
V_{VCC_UVLO}	VCC UVLO threshold	V_{CC} rising		2.0		V
V_{VCC_UVLO}	VCC UVLO threshold	V_{CC} falling		1.9		V
I_{Q_VIN}	Quiescent current into V_{IN} pin	IC enabled, no load, no switching V_{IN} =2.4V to 5.6V, V_{FB} = V_{REF} + 0.1 V,T_J up to 125°C		2	3.5	µA
I_{Q_VIN}	Quiescent current into V_{IN} pin	IC enabled, no load, no switching V_{IN} = 5.9V to 20V, V_{FB} = V_{REF} + 0.1V,T_J up to 125°C		30	45	µA
I_{Q_VOUT}	Quiescent current into V_{OUT} pin	IC enabled, no load, no switching V_{IN} =2.4V to 5.6V, V_{OUT} = 6V to 30V, V_{FB} = V_{REF} + 0.1 V,T_J up to 125°C		28	45	µA
I_{Q_VOUT}	Quiescent current into V_{OUT} pin	IC enabled, no load, no switching V_{IN} = 5.9V to 20V, V_{OUT} = 6V to 30V, V_{FB} = V_{REF} + 0.1 V,T_J up to 125°C		2	8	µA
$I_{Q_PASSTHROUGH}$	Quiescent current in passthrough mode	V_{IN} =10.1V, V_{OUT} = 10V,T_J up to 125°C		65		µA
I_{SD}	Shutdown current into V_{IN} pin	IC disabled, V_{IN} = 2.4V to 20V,T_J up to 125°C		0.6	5	µA
I_{SW_LKG}	Leakage current into SW	IC disabled, VOUT = 0 V, SW = 2.4V to 20V, T_J up to 125°C			5	µA
$I_{REVERSE_SW}$	Reverse leakage current in SW	IC disabled, VOUT = 30V, SW = 0 V,T_J up to 125°C			5	µA
I_{FB_LKG}	Leakage current into FB	IC disabled, T_J up to 125°C			50	nA
I_{MODE_LKG}	Leakage current into MODE/SYN	IC disabled, T_J up to 125°C			50	nA
I_{PG_LKG}	Leakage current into PG/STATU	IC disabled, T_J up to 125°C			50	nA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage range	Boost mode	5		30	V
V_{OUT}	Output voltage range	Passthrough mode	VIN		36	V
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 5V, V_{OUT} rising, BOOST MODE	31	31.5	32.1	V
VOVP_HYS	Output over-voltage protection hysteresis	VIN = 5V, OVP threshold		1		V
VREF	Reference Voltage at FB pin	TJ = -40 to 125°C, RSEL ≥ 27K	0.985	1	1.015	V
VOUT_10V	TPS61388 Fixed Vout version	TJ = -40 to 125°C; 0Ω≤ RSEL ≤2.2K trim automotive	9.85	10	10.15	V
VOUT_8.5V	TPS61388 Fixed Vout version	TJ = -40 to 125°C; 3.55K ≤ RSEL≤9.25K trim automotive	8.3725	8.5	8.6275	V
VOUT_6.5V	TPS61388 Fixed Vout version	TJ = -40 to 125°C; 12K ≤ RSEL≤21K, trim automotive	6.4025	6.5	6.5975	V
VOLTAGE REFERENCE						
UVL_PT_f	UVL threshold in passthrough			969.5		mV

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6.5 Electrical Characteristics (continued)

T_J = -40 to 150°C, L = 2.2µH, V_{IN} = 12V and V_{OUT} = 24V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{CC} = 4.85 V		30		mΩ
$R_{DS(on)}$	High-side MOSFET on resistance	V_{CC} = 4.85 V		25		mΩ
CURRENT LIMIT						
I_{LIM_SW}	Peak switching current limit FPWM	Duty cycle = 65%	7	8	9	A
I_{LIM_SW}	Peak switching current limit Auto PFM	Duty cycle = 65%	7	8	9	A
I_{Zero}	HSD Zero current threshold at PFM			350		mA
I_{PK_PFM}	Peak current of PFM			1.35		A
SWITCHING FREQUENCY						
Fsw	Switching frequency	F_{SW} = VCC	2050	2200	2400	kHz
Fsw	Switching frequency	F_{SW} = GND	360	400	440	kHz
D_{max}	Maximum Duty Cycle	2.2MHz	78			%
t_{ON_min}	Minimal on time			70		ns
F_{DITHER}	Spread Spectrum Modulation Frequency range as Percentage of Fsw	2.2MHz and 400kHz		12%		Fsw
$F_{pattern}$		2.2MHz		9.0		kHz
$F_{pattern}$		400kHz		7		kHz
SOFT START						
t_{SS}	Soft start time			6		ms
LOGIC INTERFACE						
V_{EN_H}	EN Logic high threshold				1.2	V
V_{EN_L}	EN Logic low threshold		0.4			V
$V_{M/SYNC_H}$	MODE/SYNC pins Logic high threshold				1.2	V
$V_{M/SYNC_L}$	MODE/SYNC pins Logic Low threshold		0.4			V
R_{DOWN}	EN pin internal pull down resistor			800		kΩ
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	VFB = VREF + 0.4V, VCOMP = 1.5V, VCC=5V		20		µA
I_{SOURCE}	COMP pin source current	VFB = VREF -0.4V, VCOMP = 1.5V, VCC=5V		20		µA
G_{mEA}	Error amplifier trans conductance	V_{COMP} = 1.0 V		200		µA/V
V_{COMPH}	COMP pin high clamp voltage	VFB = VREF - 0.4V, ILIM = 8A		1.65		V
V_{COMPL}	COMP pin high low voltage	VFB = VREF + 0.4V		0.85		V
G_{PS}	Power stage trans-conductance (peak current ratio with comp voltage)	V_{IN} = 5.0V		11		A/V
POWER GOOD						
V_{PG_RISING}	Undervoltage threshold (PGOOD threshold)	PG rising	91.5	94	98	%
$V_{PG_FALLING}$	Undervoltage threshold (PGOOD threshold)	PG falling	89.5	92	95.5	%
I_{PG_SINK}	PG pin sink current capability	V_{PG} = 0.4 V		30		mA
t_{PG_DELAY}	PG delay time			1.6		ms
t_{PG_GLITCH}	Glitch filter time of PGOOD			40		µs
SYNC TIMING						
f_{SYNC}	Ext frequency range		-20%		+20%	FSW
T_{SYNC_MIN}	Minimum sync clock pulse width				50	ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown rising threshold	T_J rising		170		°C
T_{SD}	Thermal shutdown falling threshold	T_J falling		155		°C

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6.5 Electrical Characteristics (continued)

T_J = -40 to 150°C, L = 2.2µH, V_{IN} = 12V and V_{OUT} = 24V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_HYS}	Thermal shutdown hysteresis			15		°C

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7 Detailed Description

7.1 Overview

The TPS61388-Q1 is a fully-integrated 8A peak current capability synchronous boost converter with auto Pass-through feature that integrates a 30mΩ low-side power switch and a 25mΩ high-side rectifier switch to provide a high efficiency for small size application. The TPS61388-Q1 device is a wide input range automotive boost converter designed for automotive start-stop or other general boost purpose applications. The device maintains the output voltage from a vehicle battery during automotive clod crank with the input voltage down to 2V. The wide input range of the device covers automotive load dump transient up to absmax of 40V, while the maximum programmable working output voltage in boost mode covers up to 30V.

The TPS61388-Q1 employs peak current mode control with the switching frequency options of 400kHz and 2.2MHz. The device works in fixed frequency PWM operation in medium to heavy loads. There are two optional modes at light load by configuring the MODE pin: Auto PFM mode and Forced PWM to balance the efficiency and noise immunity at light load.

The device features a low shutdown current and a low quiescent current in standby mode, which minimizes battery drain at no and light load condition. The device also supports an ultra-low quiescent current Pass-through operation, which eliminates the need for an external bypass switch when the supply voltage is greater than the boost output regulation target.

The TPS61388-Q1 has various fixed output voltage versions to save the external components and reduce the quiescent current consumed by the external feedback resistor. TPS61388-Q1 supports the external loop compensation so that the stability and transient response is optimized at wider VOUT/VIN ranges.

The device has built-in protection features such as peak current limit, overvoltage protection, and thermal shutdown. External clock synchronization, spread spectrum modulation, and a lead-less package with minimal parasitic help to reduce EMI. The TPS61388-Q1 is available in a 3.0mm × 2.5mm HotRod™ Lite WQFN package with Wettable flank.

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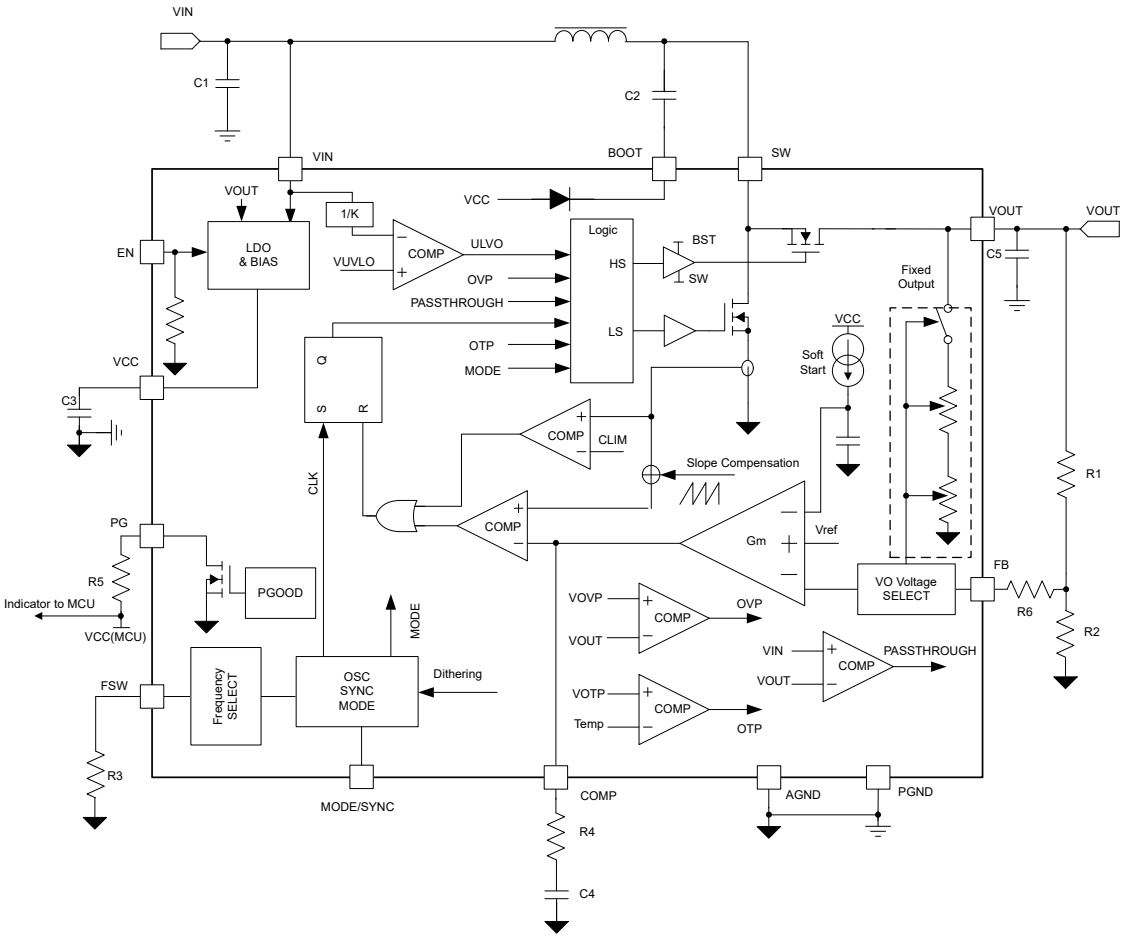
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCC Power Supply

The internal LDO in the TPS61388-Q1 outputs a regulated voltage of 5.1V with 10mA output current capability. A ceramic capacitor is connected between the VCC pin and GND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. Allow the effective capacitance of this ceramic capacitor to be above 1μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10V is recommended.

When the input voltage at the VIN pin is below 5.6V, the internal LDO is powered by the VOUT pin, when the input voltage at the VIN pin is above 5.9V, the internal LDO is powered by the VIN pin.

7.3.2 Input Undervoltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The TPS61388-Q1 has both VIN_UVLO and VCC_UVLO function. TPS61388-Q1 disables from switching when the falling voltage at the VIN pin trips the falling UVLO threshold VIN_UVLO, which is typically 1.9V. The device starts operating when the rising voltage at the VIN pin trips the rising UVLO threshold, which is typically 2.3V. TPS61388-Q1 also disables when the falling voltage at the VCC pin trips the UVLO threshold VCC_UVLO, which is typically 1.9V.

7.3.3 Enable and Soft Start

The TPS61388-Q1 has a 6ms soft start function to prevent high inrush current during start-up. When the EN pin is pulled high, the internal soft-start capacitor is charged with a constant current. During this time, the soft-start capacitor voltage is compared with the internal reference (1.0V). The lower one is fed into the internal positive

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input of the error amplifier. The output of the error amplifier (which determines the inductor peak current value) ramps up slowly as the soft-start capacitor voltage goes up. The soft-start phase is completed after the soft-start capacitor voltage exceeds the internal reference, which takes 6ms from 0V to 1.0V. When the EN pin is pulled low, the voltage of the soft-start capacitor is discharged to ground.

When system is always enabled, it is recommended to connecting EN pin to VCC pin.

7.3.4 Shut Down

When the input voltage is below the UVLO threshold or the EN pin is pulled low, The TPS61388-Q1 is in shutdown mode and all the functions are disabled.

The output voltage value is VIN voltage minus the voltage drop of high side body diode, typically VIN-0.7V.

7.3.5 Switching Frequency Setting

The TPS61388-Q1 uses a fixed-frequency control scheme. The switching frequency is selected as 400kHz or 2.2MHz depending on FSW configuration. Table 7-1 shows the detail.

Table 7-1. Frequency Configuration

Frequency	FSW connection
400kHz	Connect FSW directly to GND
400kHz	Connect FSW to GND through resistor, 0Ω≤ R_{FSW} ≤ 2.2kΩ
2.2MHz	Connect FSW to GND through resistor, R_{FSW} > 27kΩ
2.2MHz	Connect FSW directly to VCC

where

- R_{FSW} is the resistance between the FSW pin and the GND.

7.3.6 Spread Spectrum Frequency Modulation

The TPS61388-Q1 uses a triangle waveform to spread the switching frequency with ±6% of normal frequency. The frequency of the triangle waveform is 8.8KHz for 2.2MHz and 6.25kHz for 400kHz. For example, if the normal switching frequency of the TPS61388-Q1 is programmed to 2.2MHz, the spread spectrum function modulates the switching frequency in the range of 2.07MHz to 2.33MHz in a triangle of 8.8kHz.

The spread spectrum is disabled while in Auto PFM mode or an external clock is applied to the MODE/SYNC pin.

7.3.7 Bootstrap

The TPS61388-Q1 has an integrated bootstrap regulator circuit. To provide the gate drive supply voltage for high-side switches, a small ceramic capacitor is needed between the BST pin and SW pin. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 6.3V is recommended. A typical value of 0.1µF/6.3V is recommended.

7.3.8 MODE/SYNC Configuration

Table 7-2 summarizes the MODE/SYNC function and the entry condition.

This pin is not allowed to be left floating.

Table 7-2. MODE/SYNC Configuration

MODE/SYNC PIN CONFIGURATION	MODE
Logic Low	Auto PFM Mode
Logic High	Forced PWM Mode
External Synchronization	Forced PWM Mode

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The TPS61388-Q1 is capable of synchronizing to an external clock applied to the MODE/SYNC pin. The external clock needs to be within -+20% of the setting frequency for a reliable synchronization. The TPS61388-Q1 remains in Forced PWM mode if the oscillator is synchronized by an external clock. The spread spectrum feature is disabled when external synchronization is used.

7.3.9 Pass-through Operation

TPS61388-Q1 runs into pass-through operation when VIN is higher than VOUT-SET, high-side MOS is always on and quiescent current is optimized is to maximize the total efficiency.

Before entering pass-through, VIN rises to a voltage very close to VOUT-SET. In this condition the switching regulator operates at a very low duty cycles to keep VOUT in regulation. However, the minimum on-time limitation prevents the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency.

Table 7-3 summarizes the different features of the two part numbers when entering and exiting Pass-through operation with different configurations.

Table 7-3. Pass-through Behaviors with Part Number and Frequency Configuration

Part Number	Configuration		Entering and Exiting Pass-through Behavior
	Frequency	MODE	
TPS61388-Q1	2.2MHz	Forced PWM	Frequency keeps 2.2MHz
	400kHz	Forced PWM	Frequency keeps 400kHz
	2.2MHz or 400kHz	Auto PFM	Frequency spreads continuously
TPS613881-Q1	2.2MHz	Forced PWM	Frequency foldback to 400kHz
	400kHz	Forced PWM	Frequency keeps 400kHz
	2.2MHz or 400kHz	Auto PFM	Frequency spreads continuously

7.3.9.1 Auto PFM Behavior

For both TPS61388-Q1 and TPS613881-Q1, when the mode is selected to be Auto PFM mode, the frequency spreads automatically when VIN is close to VOUT- SET. Figure 7-1 shows the operation transformation.

This behavior provides very smooth output waveform when entering and exiting pass-through operation.

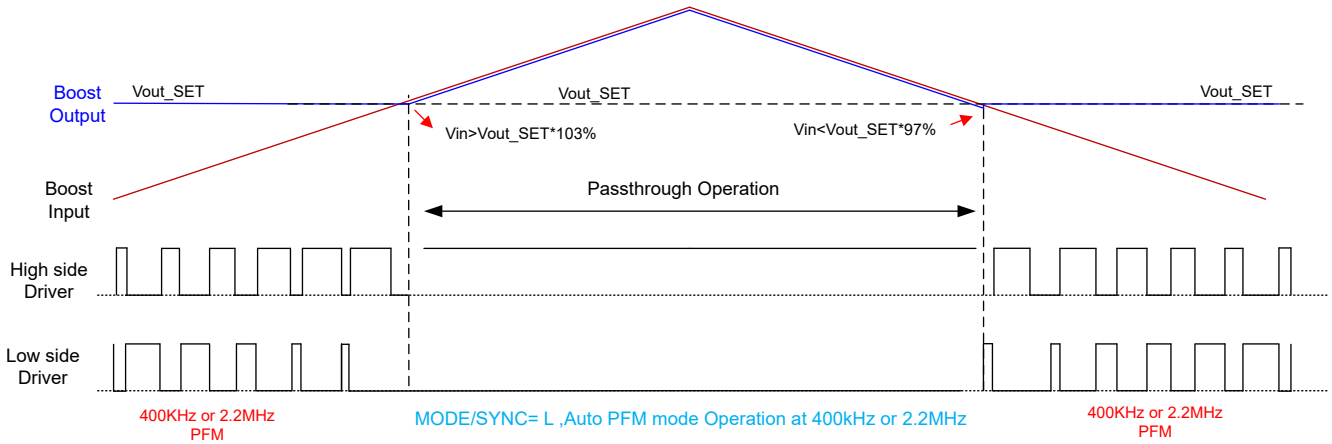

Figure 7-1. Entering and exiting Pass-through in Auto PFM mode 400kHz or 2.2MHz

7.3.9.2 400kHz Forced PWM Behavior

For both TPS61388-Q1 and TPS613881-Q1, when the mode is selected to be Forced PFM mode and the frequency is chosen to be 400kHz, Figure 7-2 shows the operation transformation.

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The minimum on time(70ns typical) limitation is enough to achieve small duty when VIN is close to VOUT for 400kHz. Vout reaches approximately 104% of Vout-SET before entering pass-through.

This behavior provide smooth waveform when entering and exiting pass-through operation.

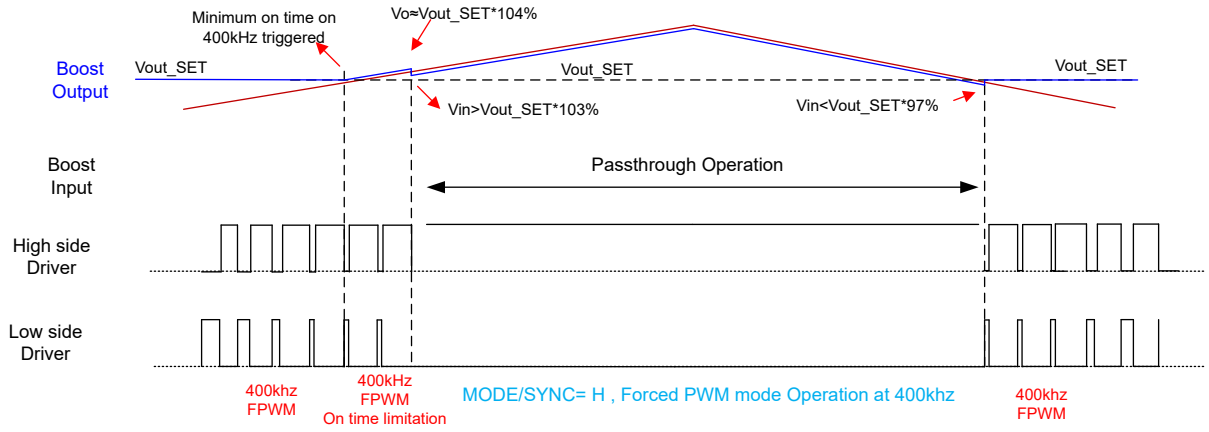

Figure 7-2. Entering and exiting Pass-through in Forced PWM mode 400kHz

7.3.9.3 2.2MHz Fixed Frequency Behavior with TPS61388-Q1

TPS61388-Q1 keeps frequency constant when entering and exiting Pass-through operation. When the mode is selected to be Forced PWM mode, and the frequency is chosen to be 2.2MHz, Figure 7-3 shows that switching frequency keeps 2.2Mhz when entering and exiting Pass-through operation.

Special care needs be taken when using 2.2Mhz with fixed frequency behavior. Refer to Section 7.3.9.4 for more details.

This behavior provides fixed 2.2MHz at all time and is benefit for EMC design and AM noise sensitive application.

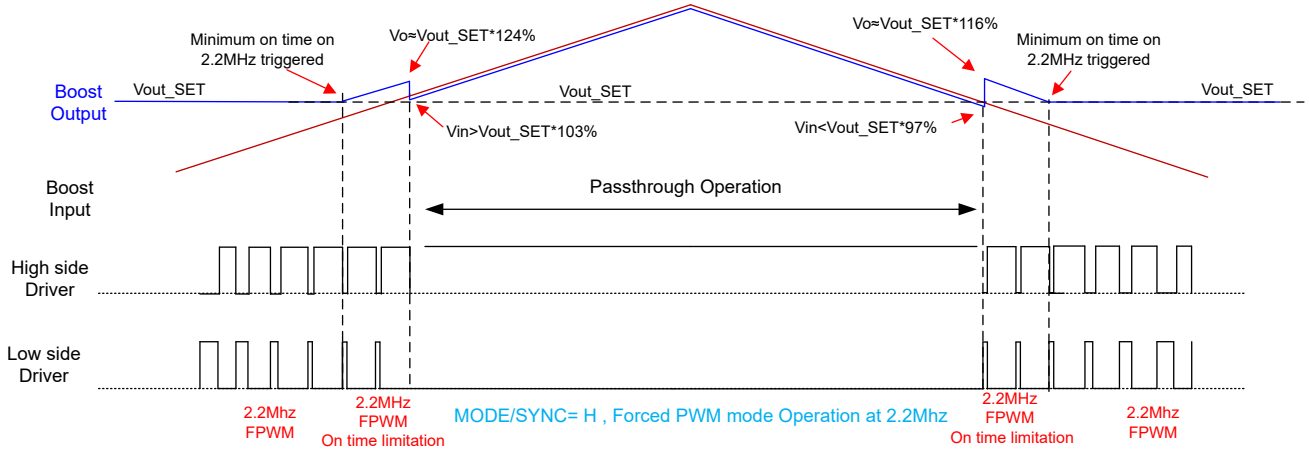

Figure 7-3. Entering and exiting Pass-through in Forced PWM mode in Fixed 2.2MHz

7.3.9.4 Special Limitation for FPWM 2.2MHz Fixed Frequency

As described in Section 7.3.9.3, for TPS61388-Q1 Forced PWM mode and 2.2MHz, the frequency keeps fixed entering and exiting pass-through operation. When exiting pass-through, the inductor current is uncontrollable and goes to a high level. The process can be seen in Figure 7-4.

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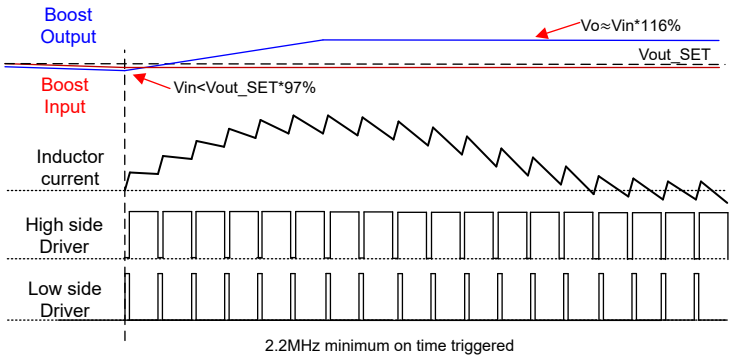

Figure 7-4. Inductor Current Inrush When Exiting Pass-through Fixed Frequency FPWM 2.2Mhz

The low side switch turns on with a minimum duty of approximately 20%, the inductor current increases with a slew rate related with input voltage; then the high side switch turns on with approximately 80% duty and inductor current tries to decrease. The inductor current fails to decrease to initial value until output voltage reaches 125% of input voltage. That is why we see inductor current keep increasing in the a few initial cycles.

Similarly, when TPS61388-Q1 working in this fixed frequency process, when Vin rises or drops rapidly, the switch current is also unctronolable.

Obviously, smaller inductor, larger output capacitor , higher voltage and heavier load current worsen the uncontrollable inrush current.

When using TPS61388-Q1 with fixed frequency FPWM and 2.2Mhz, inductance ,output capacitance, load current and output target voltage need comprehensive consideration to maintain a safe margin. In most case, a current of 20A within 100us is safe for TPS61388-Q1.Table 7-4 shows the recommended max output capacitance with typical Vout target and inductance.

Avoid using output target higher than 24V, the pass-through entering point is close to overvoltage protection.

Table 7-4. Recommended Maximum Output Capacitance With Typical Vout Target and Inductance

Vout target	L (μH)(1)	Load current/A	Cout_max(uF)(2)
10	0.68	2	200
10	1	2	250
18	1	2	100
18	2.2	2	120
24	2.2	1	50

(1) Choose the inductor with soft saturation to withstand high current like 15A or more
(2) The Cout is combination of ceramic and electrolytic ones, the value is the total effective capacitance.

7.3.9.5 2.2MHz Frequency Foldback Behavior with TPS613881-Q1

For TPS613881-Q1, when the mode is selected to be Forced PFM mode and the frequency is chosen to be 2.2MHz, Figure 7-5 shows the operation transformation.

TPS613881-Q1 foldbacks the switching frequency to decrease to 400kHz or lower when minimum on-time triggers, this provides a smooth transient between switching operation and Pass-through operation as well as avoid the working in AM band frequency.

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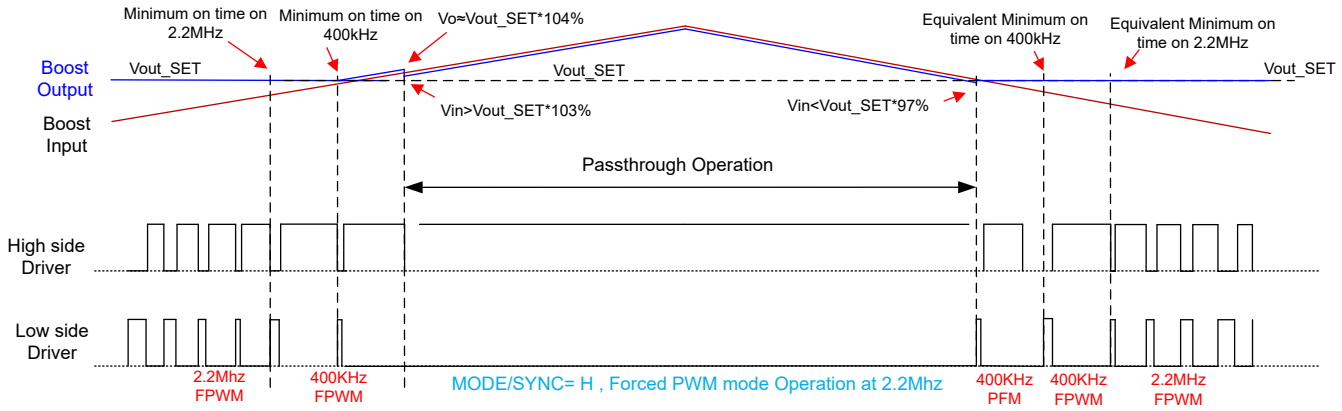

Figure 7-5. Entering and Exiting Pass-through in Forced PWM mode 2.2MHz with Frequency Foldback

7.3.10 Overvoltage Protection (OVP)

If the output voltage exceeds the OVP threshold (typically 31V), the TPS61388-Q1 immediately stops switching until the output voltage drops below the recovery threshold (typically 30V). This function protects the device against excessive voltage.

7.3.11 Power-Good Indicator

The TPS61388-Q1 integrates a power-good function to simplify sequencing and supervision. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor (between 5KΩ to 100KΩ) connect to a suitable voltage supply below 6V.

The PG pin goes high with a typical 1.5ms delay time after VOUT reaches typical 94% of the target output voltage. The PG pin immediately goes low with a 35µs deglitch filter delay when following occurs:

- Output voltage is lower than 92% of the target output voltage.
- EN logic low
- Thermal shutdown

The PG signal keeps high during Pass-through operation and overvoltage protection.

7.3.12 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown occurs at junction temperatures exceeding 170°C. When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 155°C (typical).

7.4 Device Functional Modes

7.4.1 Forced PWM Mode

The TPS61388-Q1 enters Forced PWM mode by pulling the MODE/SYNC pin to logic high for more than five switching cycles. In Forced PWM mode, the TPS61388-Q1 keeps the switching frequency constant at light load condition. When the load current decreases, the output of the internal error amplifier also decreases to keep the inductor peak current down. When the output current decreases further, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant.

7.4.2 Auto PFM Mode

The TPS61388-Q1 enters Auto PFM Mode by pulling the MODE/SYNC pin to logic low for more than five switching cycles. The TPS61388-Q1 improves the efficiency at light load when operating in Auto PFM mode. When the output current decreases to a certain level, the output voltage of the error amplifier is clamped by the internal circuit. If the output current reduces further, the inductor current through the high-side switch will be clamped but not lowered further. Pulses are skipped to improve the efficiency at light load.

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7.5 Pinout Design for Clearance and FMEA

The TPS61388-Q1 has a carefully designed pinout arrangement that provides additional clearance spacing between high-voltage pins (VIN, SW, and BOOT) and nearby low-voltage pins (such as VCC). Moreover, the TPS61388-Q1 pinout is designed for critical automotive applications requiring functional safety system design with stricter reliability and higher durability. In terms of pin FMEA (failure mode effects analysis), the typical failure scenarios include pin short to ground, pin short to input supply (VIN), pin short to a neighboring, and pin left open. These faults are considered as applied externally to the IC, therefore, are board-level failures rather than IC-level reliability failures. Example sources of such faults are stray conductive filaments causing pin-to-pin shorts or a board manufacturing defect causing an open-circuit track.

The TPS61388-Q1 fixed output voltage versions in particular are considered pin-FMEA compliant. The output voltage stays or below the regulation voltage in the event of a pin short circuit to a neighboring pin.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS61388-Q1 is designed for outputting voltage up to 30V with the 8A switch current capability. The TPS61388-Q1 works with different inductor and output capacitor combinations by external loop compensation. The following design procedure is used to select component values for the TPS61388-Q1.

8.2 Typical Application

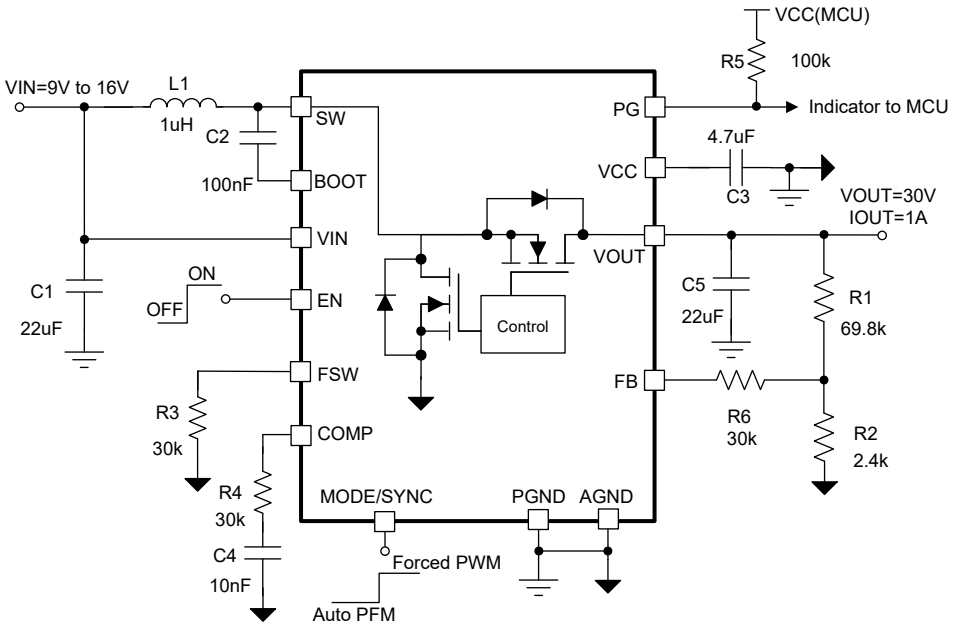

Figure 8-1. Typical Application

8.2.1 Design Requirements

A typical application example is ultrasonic lens cleaning powered through a car battery, which normally requires 30V output as its bias voltage and consumes less than 500mA current. 500mA load current is designed to provide margin. The following design procedure is used to select external component values for the TPS61388-Q1.

Table 8-1. Design Requirements

PARAMETERS	VALUES
Input Voltage	9V to 16V
Output Voltage	30V
Switching Frequency	2.2MHz
Output Current	500mA
Output Voltage Ripple	± 150 mV

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8.2.2 Detailed Design Procedure

8.2.2.1 Programming the Output Voltage

The output voltage is determined by the resistor sensed from FB pin before device is enabled. There are two ways to set the output voltage of the TPS61388-Q1, fixed output voltage and adjustable output voltage.

Figure 8-2 shows the typical circuit of the FB pin connection for fixed output voltage. The FB resistor R_{FB} is defined as Equation 1:

$$R_{FB} = R_{DOWN} \quad (1)$$

When designed for fixed output voltage, the TPS61388-Q1 uses the internal resistor divider and works with fixed output voltage. See Device Comparison Table for detailed information.

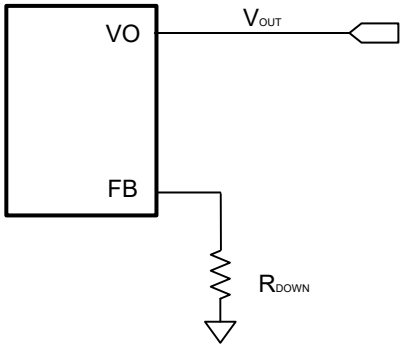

Figure 8-2. Typical Connection of FB Pin For Fixed Output Voltage

Figure 8-3 shows the typical circuit of the FB pin connection for adjustable output voltage. The FB resistor R_{FB} is defined as Equation 2:

$$R_{FB} = R_{INSERT} + \frac{R_{UP} \times R_{DOWN}}{R_{UP} + R_{DOWN}} \quad (2)$$

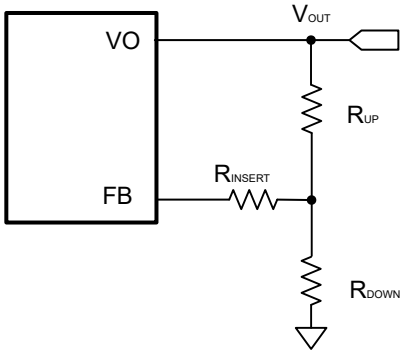

Figure 8-3. Typical Connection of FB Pin For Adjustable Output Voltage

The output voltage is programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to Equation 3.

$$V_{OUT} = V_{REF} \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} \quad (3)$$

Equation 3 shows that the output voltage setting is only influenced by R_{UP} and R_{DOWN}. In normal application, R_{INSERT} is 0Ω, that is, directly connect FB pin to middle point of feedback voltage divider. Also, keep R_{FB} larger than 27kΩ to avoid fixed output voltage mode.

For automotive application that do not prefer to use resistors more than 100kΩ, R_{INSERT} (>27kΩ) is used so that calculated R_{UP} and R_{DOWN} feedback resistor value is less than 100kΩ.

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When working with adjustable voltage, for the best accuracy, R_{DOWN} is recommended to be smaller than 200kΩ so that the current flowing through R_{DOWN} is at least 100 times larger than FB pin leakage current. Changing R_{DOWN} towards the lower value increases the robustness against noise injection. Changing R_{DOWN} to higher values reduces the quiescent current to achieve higher efficiency at light load.

8.2.2.2 Selecting the Inductor

A boost converter normally requires two main passive components for storing energy during power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency), transient behavior, and loop stability, which makes the inductor the most critical component in application.

When selecting the inductor and the inductance, the other important parameters are:

- The maximum current rating (consider RMS and peak current)
- The series resistance
- Operating temperature

The TPS61388-Q1 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 4A, the slope compensation is not adequate, and the loop is unstable. Therefore, it is recommended to make the peak-to-peak current ripple between 800mA to 4A when selecting the inductor.

The inductance is calculated by Equation 4, Equation 5, and Equation 6:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{4}$$

$$\Delta I_{L_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \tag{5}$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}} \tag{6}$$

where

- Δ_{IL} is the peak-peak inductor current ripple
- V_{IN} is the input voltage
- D is the duty cycle
- L is the inductor
- f_{SW} is the switching frequency
- Ripple % is the ripple ration versus the DC current
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- η is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current possiblely increase above the peak inductor current calculated.

Pay attention when using TPS613881-Q1 at Forced PWM mode 2.2MHz, the frequency decreases to 400kHz when Vin reaches approximately 80% of Vout target. Take special consideration when calculating the current ripple.

Inductor values can have ±20%, or even ±30%, tolerance with no current bias. When the inductor current approaches the saturation level, the inductance can decrease 20% to 35% from the value at 0A bias current, depending on how the inductor vendor defines saturation. When selecting an inductor, make sure the rated current, especially the saturation current, is larger than its peak current during the operation.

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The inductor peak current varies as a function of the load, switching frequency, and input and output voltages. The peak current is calculated with Equation 7 and Equation 8.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L \tag{7}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{IN} is the input average current
- Δ_{IL} is the ripple current of the inductor

The input DC current is determined by the output voltage. The output current is calculated by:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{8}$$

where

- I_{IN} is the input current of the inductor
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency

While the inductor ripple current depends on the inductance, the frequency, the input voltage, and duty cycle are calculated by Equation 4. Replace Equation 4 and Equation 8 into Equation 7 and get the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \tag{9}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- η is the efficiency
- V_{IN} is the input voltage
- L is the inductor
- f_{SW} is the switching frequency

The heat rating current (RMS) is calculated with Equation 10:

$$I_{L_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2} \tag{10}$$

where

- I_{L_RMS} is the RMS current of the inductor
- I_{IN} is the input current of the inductor
- Δ_{IL} is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature-related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency-dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)

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- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. Table 8-2 lists some recommended inductors.

Table 8-2. Recommended Inductors

PART NUMBER	FREQUENCY/ Hz	L (µH)	DCR TYP (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR(1)
XEL4030-102MEB	2.2M	1	8.9	9	4 × 4 × 3	Coilcraft
DFE322520FD-1R0M	2.2M	1	22	7.5	3.2 × 2.5 × 2	Murata
XGL6060-332MEC	400k	3.3	6.5	13.4	6.5 × 6.7 × 6.1	Coilcraft
XGL6060-472MEC	400k	4.7	9.1	10.2	6.5 × 6.7 × 6.1	Coilcraft

(1) See the *Third-party Products Disclaimer*.

8.2.2.3 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. The loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple is calculated by Equation 11:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (11)$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency

The additional output ripple component caused by ESR is calculated by Equation 12:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (12)$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple is usually neglected. However, for the tantalum or electrolytic capacitors, it has to be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement is estimated using Equation 13:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (13)$$

where

- ΔI_{STEP} is the transient load current step
- ΔV_{TRAN} is the allowed voltage dip for the load current step
- f_{BW} is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero)

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Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors derates by as much as 70% of the capacitance at the respective rated voltage. Therefore, leave enough margins on the voltage rating to maintain adequate capacitance at the required output voltage.

8.2.2.4 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter since ceramic capacitors have extremely low ESR and are available in small footprints. Input capacitors are recommended to be located as close as possible to the device. While a 22µF input capacitor or equivalent is sufficient for the most applications, larger values reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing possibly couple to the output and be mistaken as loop instability or even damage the device. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, needs to be placed between C_{IN} and the power source lead to reduce ringing that occurs between the inductance of the power source leads and C_{IN}.

8.2.2.5 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during the turnon of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1µF. C_{BST} oughts to be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1µF was selected for this design example.

8.2.2.6 V_{CC} Capacitor

The primary purpose of the V_{CC} capacitor is to supply the peak transient currents of the driver and bootstrap capacitor and provide stability for the V_{CC} regulator. The value of C_{VCC} oughts to be at least 10 times greater than the value of C_{BST}, and oughts to be a good quality, low-ESR ceramic capacitor. Place C_{VCC} close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7µF was selected for this design example.

8.2.2.7 Protect from Inrush Current

If the boost converter is plugged into a live supply, large current flew through inductor, the body diode of high side switch and Cout. With large Cout capacitance and steep slew rate of VIN, the inrush current could be extremely high and there is risk of damaging the body diode. Unfortunately, the current is uncontrollable.

To prevent device from damage, in these situations, a small schottky diode or silicon diode can be connected between VIN and VOUT to as shown in Figure 8-4.The diode provides a direct way to charge the output capacitor from VIN to VOUT. The diode also deactivate the resonant circuit and limit the VOUT over-shoot from LC resonance. Choose the diode rating of one half of the full load current or smaller since it only conducts current during VIN plug or fast transient conditions.

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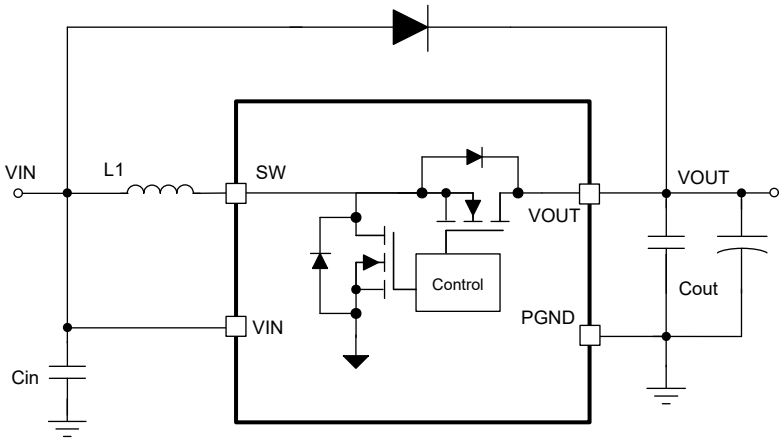

Figure 8-4. Inrush Current Protecting by Adding Diode between VIN and VOUT

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8.2.2.8 Loop Stability and Compensation

8.2.2.8.1 Small Signal Model

The TPS61388-Q1 uses the fixed frequency peak current mode control. There is an internal adaptive slope compensation to avoid subharmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with the loop compensation. Figure 8-5shows the equivalent small signal elements of a boost converter.

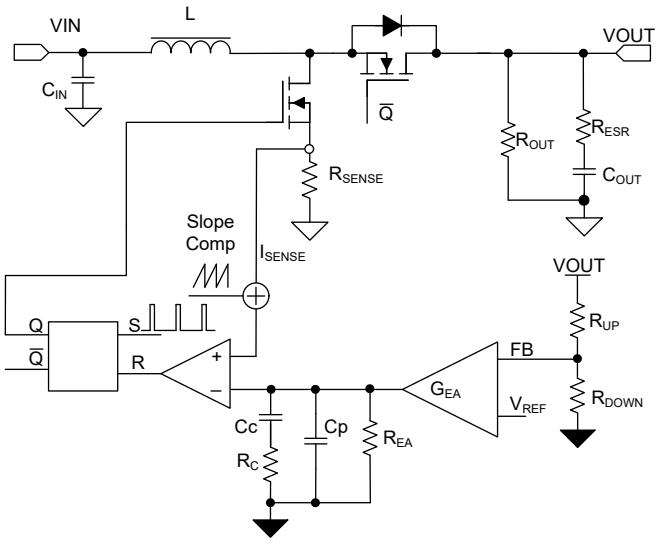

Figure 8-5. TPS61388-Q1 Control Equivalent Circuitry Model

The small signal of power stage is:

$$K_{PS}(S) = \frac{R_{OUT} \times (1-D)}{2 \times R_{SENSE}} \times \frac{(1+\frac{S}{2\pi \times f_{ESR}})(1-\frac{S}{2\pi \times f_{RHP}})}{(1+\frac{S}{2\pi \times f_P})} \quad (14)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor

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- R_{SENSE} is the equivalent internal current sense resistor, which is typically 91mΩ

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \quad (15)$$

where

- C_{OUT} is the output capacitance. For a boost converter having multiple identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (16)$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1-D)^2}{2\pi \times L} \quad (17)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- L is the inductance

Equation 18 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP}+R_{DOWN}} \times \frac{1+\frac{S}{2\times\pi\times f_Z}}{(1+\frac{S}{2\times\pi\times f_{P1}})\times(1+\frac{S}{2\times\pi\times f_{P2}})} \quad (18)$$

where

- R_{EA} is the output impedance of the error amplifier, typically R_{EA} = 500MΩ
- f_{P1}, f_{P2} is frequency of the pole in compensation network
- f_Z is frequency of zero in the compensation network

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_c} \quad (19)$$

where

- C_C is the zero capacitor compensation

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (20)$$

where

- C_P is the pole capacitor compensation

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- R_C is the resistor of the compensation network

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (21)$$

8.2.2.8.2 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Crossover Frequency, f_C .**

   The first step is to set the loop crossover frequency, f_C. The higher the crossover frequency, the faster the loop response is. It is generally accepted that the loop gain crosses over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. Then, calculate the loop compensation network values of R_C, C_C, and C_P by the following equations.

2. **Set the Compensation Resistor, R_C .**

   By placing f_Z below f_C, for frequencies above f_C, R_C | | R_{EA} ~ = R_C, so R_C × G_{EA} sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at f_Z results in the total loop gain, $T_{(s)} = K_{PS(s)} \times H_{EA(s)}$, being zero at f_C.

   Therefore, to approximate a single-pole rolloff up to f_{P2}, rearrange Equation 18 to solve for RC so that the compensation gain, K_{EA}, at f_C is the negative of the gain, K_{PS}. Read at frequency f_C for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \quad (22)$$

   where

   - K_{EA} is gain of the error amplifier network
   - K_{PS} is the gain of the power stage
   - G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 200μA / V

3. **Set the Compensation Zero capacitor, C_C .**

   Place the compensation zero at the power stage , get the position of R_{OUT} ,C_{OUT} pole:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (23)$$

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \quad (24)$$

4. **Set the Compensation Pole Capacitor, C_P .**

   Place the compensation pole at the zero produced by R_{ESR} and C_{OUT}. It is useful for canceling unhelpful effects of the ESR zero.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (25)$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (26)$$

   Set f_{P2} = f_{ESR}, and get:

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$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad (27)$$

If the calculated value of C_P is less than 10pF, neglecte this capacitor.

8.2.3 Application Curves

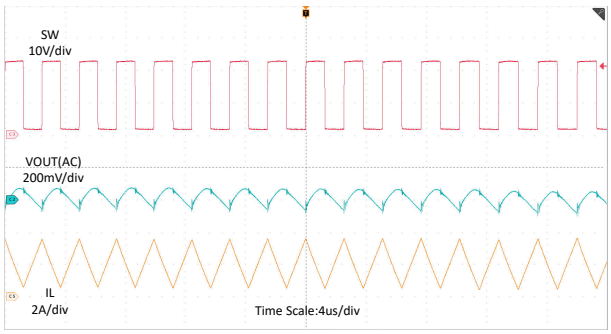

Figure 8-6. Switching Waveform V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A, FPWM 400kHz

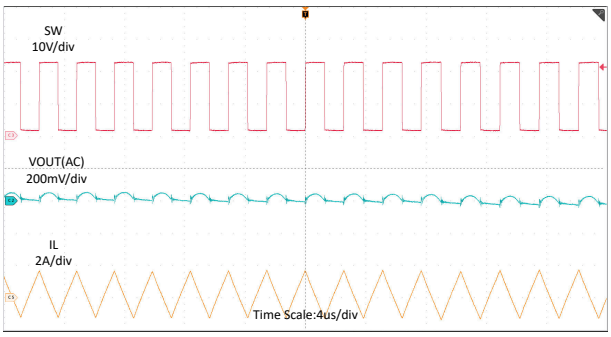

Figure 8-7. Switching Waveform V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 100mA, FPFM 400kHz

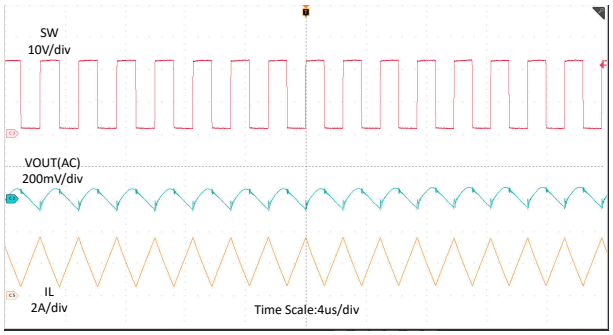

Figure 8-8. Switching Waveform V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A, PFM 400kHz

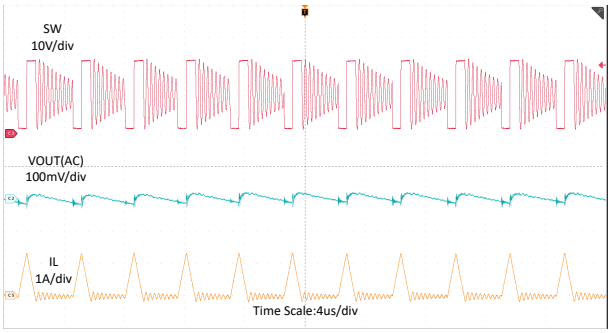

Figure 8-9. Switching Waveform V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 100mA, PFM 400kHz

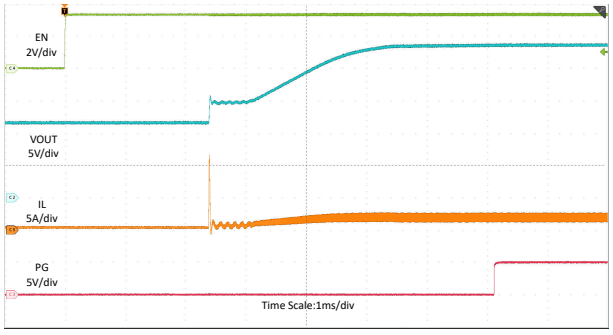

Figure 8-10. Start-up from EN Waveform V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A, FPWM

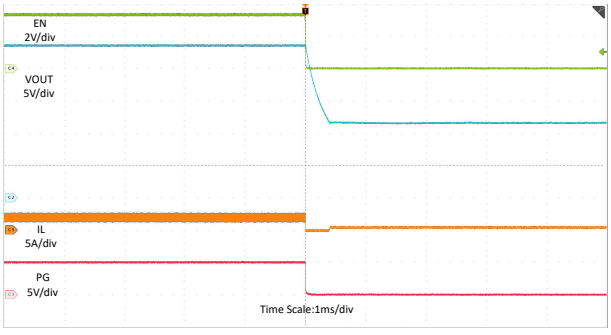

Figure 8-11. Shutdown from EN Waveforms V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A, FPWM

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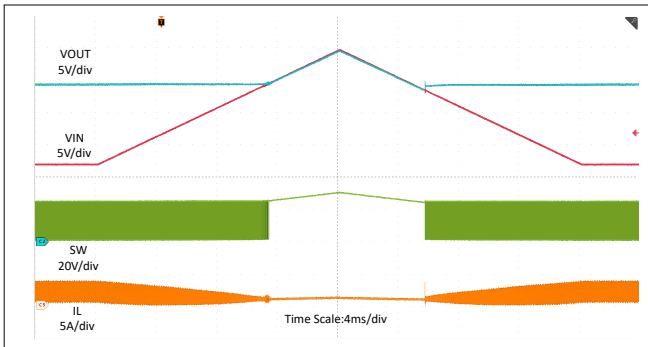

Figure 8-12. Pass-through Behavior $V_{OUT-SET}$ = 24V, I_{OUT} = 1A, PFM, 400kHz

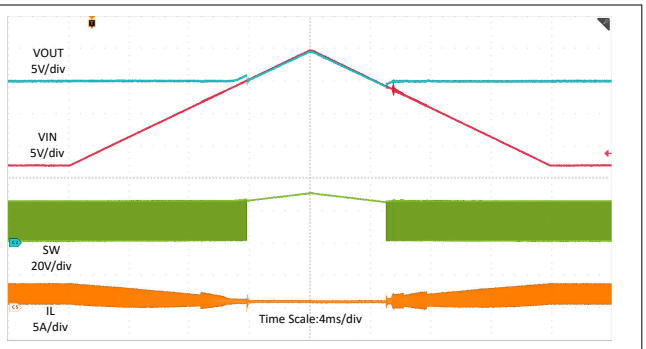

Figure 8-13. Pass-through Behavior $V_{OUT-SET}$ = 24V, I_{OUT} = 1A, FPWM, 400kHz

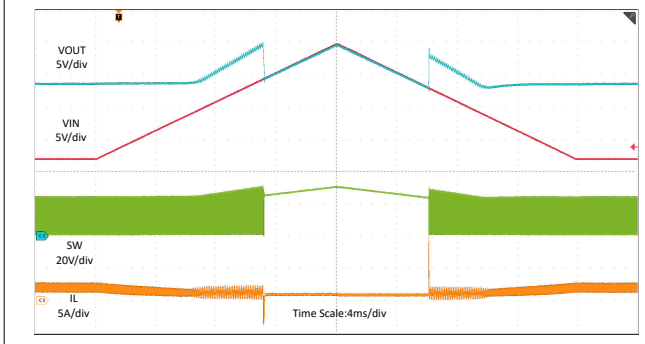

Figure 8-14. Pass-through Behavior $V_{OUT-SET}$ = 24V, I_{OUT} = 1A, FPWM, 2200kHz, Fixed Frequency

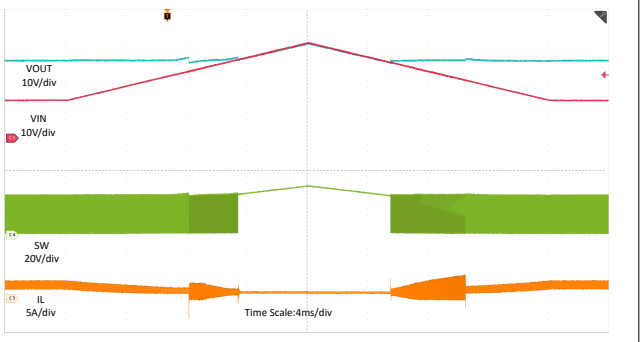

Figure 8-15. Pass-through Behavior $V_{OUT-SET}$ = 24V, I_{OUT} = 1A, FPWM, 2200kHz, Frequency Foldback

8.3 Power Supply Recommendations

The TPS61388-Q1 is designed to operate from an input voltage supply range between 2.5V to 36V. Choose input supply to be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance is required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47µF is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator shows stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor ought to be placed as close as possible to the IC.

8.4.2 Layout Example

The bottom layer is a large GND plane connected by vias.

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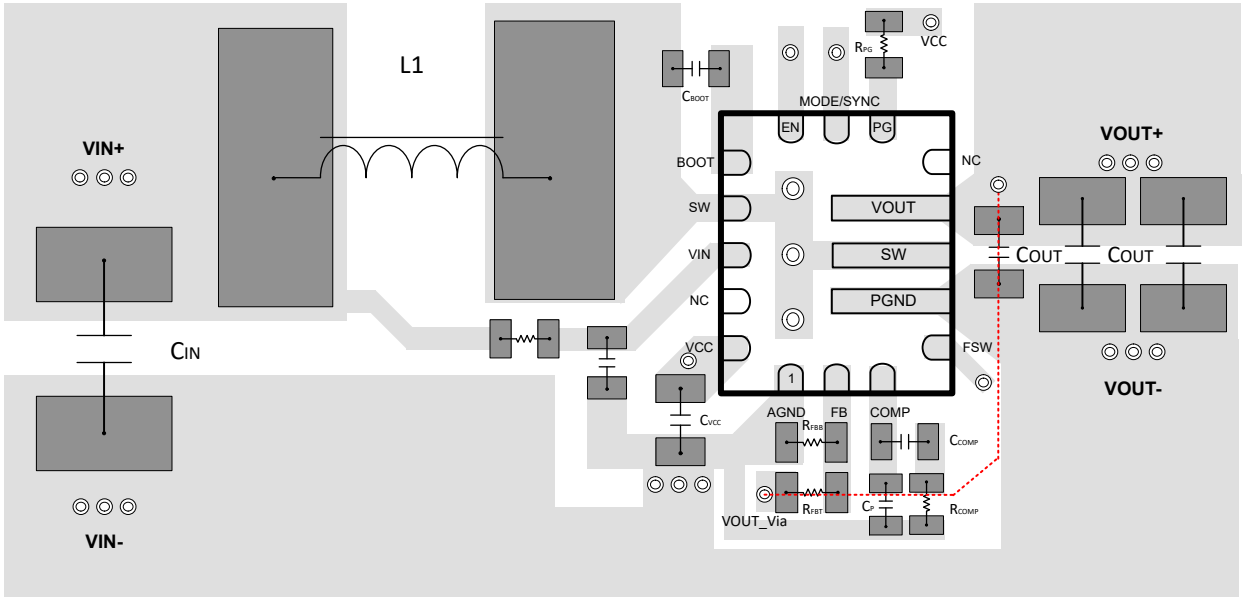

Figure 8-16. Recommended Layout

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9 Device and Documentation Support

9.1 Device Support

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9.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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10 Revision History

DATE	REVISION	NOTES
October 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTPS61388QVASRQ1	Active	Preproduction	WQFN-HR (VAS) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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