# TPS60150 5V, 140mA Charge-Pump

## 1 Features

- 2.7V to 5.5V input voltage range
- 5V fixed output voltage
- 140mA maximum output current
- 1.5MHz switching frequency
- Typical 90μA quiescent current at no load condition (skip mode)
- X2 charge pump
- Hardware enable and disable function
- Built-in soft start
- Built-in undervoltage lockout protection
- Thermal and overcurrent protection
- Available in a 2mm × 2mm 6-pin SON package with 0.8mm height

## 2 Applications

- USB on-the-go (OTG)
- HDMI
- Portable communication devices
- PCMCIA cards
- Mobile phones, smart phones
- Handheld meters

## 3 Description

The TPS60150 device is a switched capacitor voltage converter that produces a regulated, low noise, and low-ripple output voltage of 5V from an unregulated input voltage.

The 5V output can supply a minimum of 140mA current.

The TPS60150 device operates in skip mode when the load current falls less than 8mA under typical condition. In skip mode operation, quiescent current is reduced to 90μA.

Only three external capacitors are needed to generate the output voltage, therefore saving PCB space.

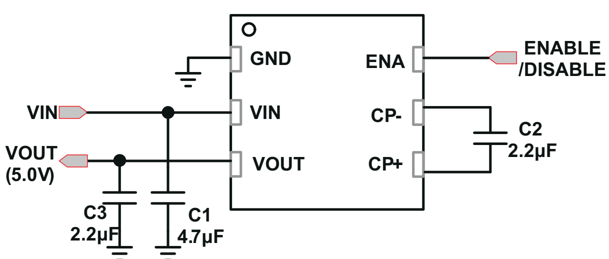
Inrush current is limited by the soft-start function during power on and power transient states.

The TPS60150 device operates over a free-air temperature range of –40°C to 85°C. The device is available with a small 2mm × 2mm 6-pin SON package (QFN).

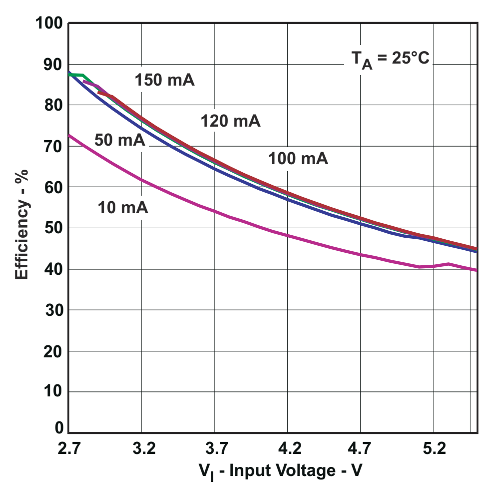
**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS60150 | DRV (WSON, 6) | 2mm × 2mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Schematic**




**Efficiency vs Input Voltage**

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# 4 Pin Configuration and Functions

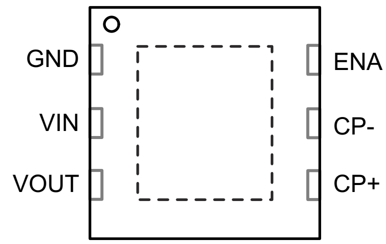



**Figure 4-1. DRV Package 6-Pin WSON (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CP+ | 4 | — | Connect to the flying capacitor |
| CP– | 5 | — | Connect to the flying capacitor |
| ENA | 6 | IN | Hardware enable/disable pin (High = Enable) |
| GND | 1 | — | Ground |
| VIN | 2 | IN | Supply voltage input |
| VOUT | 3 | OUT | Output, connect to the output capacitor |

(1) IN = input, OUT = output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [(1)]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage (all pins) | –0.3 | 7 | V |
| $T_A$ | Operating temperature | –40 | 85 | °C |
| $T_J$ | Maximum operating junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] [(2)] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22C101[(3)] | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDECs EIA/JESD22A114.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.7 | | 5.5 | V |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |
| $C_{in}$ | Input capacitor | 2.2 | | | µF |
| $C_o$ | Output capacitor | 2.2 | | | µF |
| $C_f$ | Flying capacitor | 1 | | | µF |

## 5.4 Thermal Information

| THERMAL METRIC[(1)] | | TPS60150 DRV (WSON) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 69.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 79.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 38.6 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 38.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 9.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

$V_{IN}$ = 3.6V, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C, C1 = C3 = 2.2µF, C2 = 1µF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER STAGE** | | | | | | |
| $V_{IN}$ | Input voltage range | | 2.7 | | 5.5 | V |
| $V_{UVLO}$ | Undervoltage lockout threshold | | | 1.9 | 2.1 | V |
| $I_Q$ | Operating quiescent current | $I_{OUT}$ = 140mA, Enable = $V_{IN}$ | | 4.7 | | mA |
| $I_{Qskip}$ | Skip mode operating quiescent current | $I_{OUT}$ = 0mA, Enable=$V_{IN}$ (no switching) | | 80 | | µA |
| | | $I_{OUT}$ = 0mA, Enable = $V_{IN}$(minimum switching) | | 90 | | µA |
| $I_{SD}$ | Shutdown current | 2.7V ≤ $V_{IN}$ ≤ 5.5V, Enable = 0V, $V_{OUT}$ = 0V | | | 1 | µA |
| $V_{OUT}$ | Output voltage(1) | $I_{OUT}$ ≤ 50mA, 2.7V ≤ $V_{IN}$ < 5.5V | 4.8 | 5 | 5.2 | V |
| $V_{OUT(skip)}$ | Skip mode output voltage | $I_{OUT}$ = 0mA, 2.7V ≤ $V_{IN}$ ≤ 5.5V | | $V_{OUT}$ + 0.1 | | V |
| $F_{SW}$ | Switching frequency | | | 1.5 | | MHz |
| $SS_{TIME}$ | Soft-start time | From the rising edge of enable to 90% output | | 150 | | µs |
| **OUTPUT CURRENT** | | | | | | |
| $I_{OUT\_nom}$ | Maximum output current | $V_{OUT}$ remains from 4.8V to 5.2V, 3.1V ≤ $V_{IN}$ ≤ 5.5V | 120 | | | mA |
| | | 3.3V < $V_{IN}$ < 5.5V | 140 | | | |
| $I_{OUT\_short}$ | Short-circuit current(2) | $V_{OUT}$ = 0V | | 80 | | mA |
| **RIPPLE VOLTAGE** | | | | | | |
| $V_R$ | Output ripple voltage | $I_{OUT}$ = 140mA | | 30 | | mV |
| **ENABLE CONTROL** | | | | | | |
| $V_{HI}$ | Logic high input voltage | 2.7V ≤ $V_{IN}$ ≤ 5.5V | 1.3 | | $V_{IN}$ | V |
| $V_{LI}$ | Logic low input voltage | | –0.2 | | 0.4 | V |
| $I_{HI}$ | Logic high input current | | | | 1 | µA |
| $I_{LI}$ | Logic low input current | | | | 1 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Shutdown temperature | | | 160 | | °C |
| $T_{RC}$ | Shutdown recovery | | | 140 | | °C |

(1) When in skip mode, output voltage can exceed $V_{OUT}$ spec because $V_{OUT(skip)} = V_{OUT}+0.1$.
(2) The TPS60150 device has internal protection circuit to protect IC when $V_{OUT}$ shorted to GND.

## 5.6 Typical Characteristics

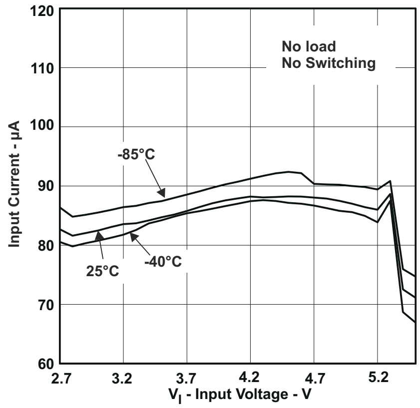



**Figure 5-1. Quiescent Current vs Input Voltage**

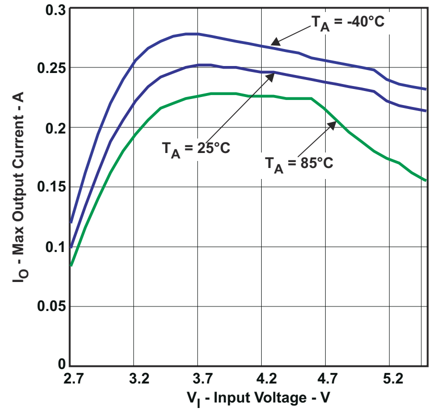



**Figure 5-2. Maximum Output Current vs Input Voltage at Temperature**

# 6 Detailed Description

## 6.1 Overview

The TPS60150 regulated charge pump provides a regulated output voltage for various input voltages. The TPS60150 device regulates the voltage across the flying capacitor to 2.5V and controls the voltage drop of Q1 and Q2 while a conversion clock with 50% duty cycle drives the FETs.

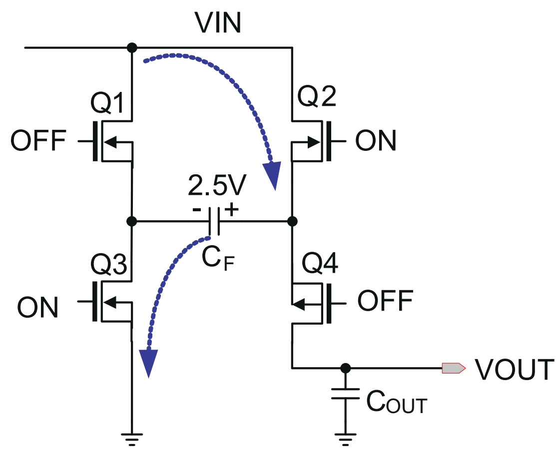



**Figure 6-1. Charging Mode**

During the first half cycle, Q2 and Q3 transistors are turned on and flying capacitor, $C_F$, is charged to 2.5V.

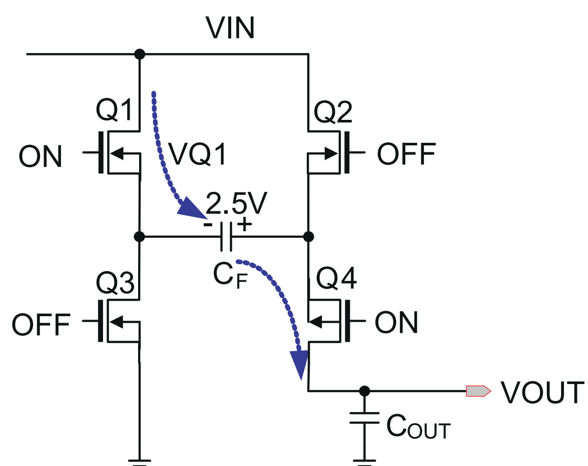



**Figure 6-2. Discharging Mode**

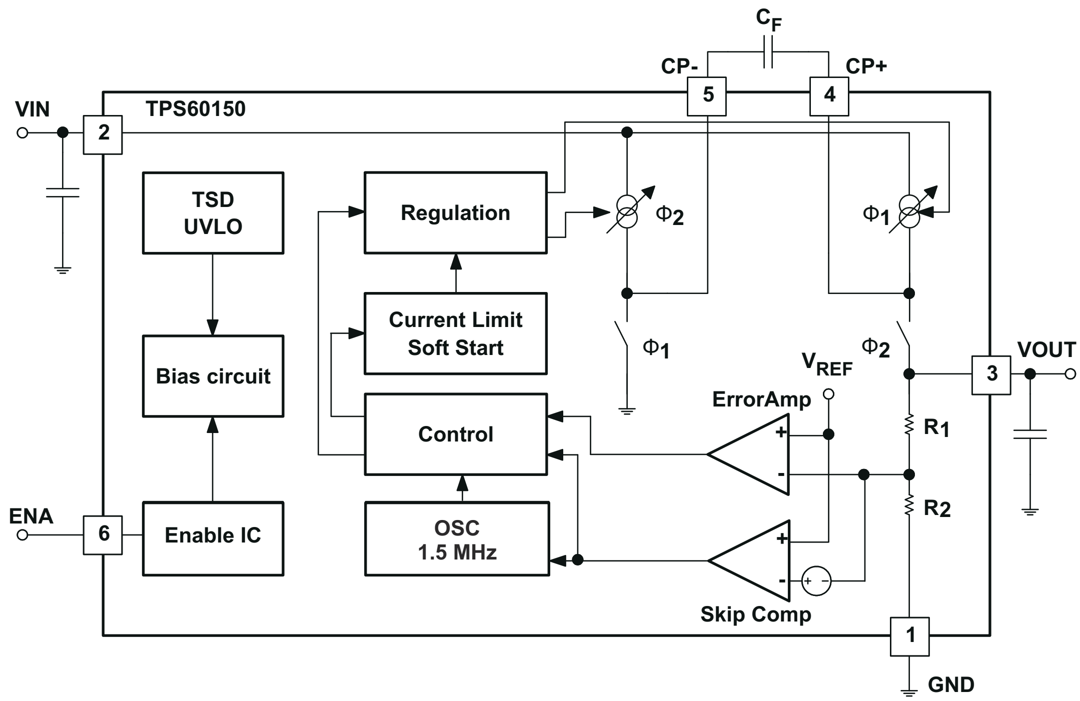
During the second half cycle, Q1 and Q4 transistors are turned on. Capacitor $C_F$ is then discharged to output.

Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{IN} - VQ1 + V(C_F) - VQ4 = V_{IN} - VQ1 + 2.5\ V - VQ4 = 5\ V \quad \text{(Ideal)} \tag{1}$$

The output voltage is regulated by output feedback and an internally compensated voltage control loop.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### 6.3.1 Enable

An enable pin on the regulator is used to place the device into an energy-saving shutdown mode. In this mode, the output is disconnected from the input, and the input quiescent current is reduced to 10µA maximum.

### 6.3.2 Undervoltage Lockout

When the input voltage drops, the undervoltage lockout prevents misoperation by switching off the device. The converter starts operation again when the input voltage exceeds the threshold, provided the enable pin is high.

### 6.3.3 Thermal Shutdown Protection

The regulator has thermal shutdown circuitry that protects the regulator from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reached approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled. Continuously running the regulator into thermal shutdown can degrade reliability. The regulator also provides current limit to protect the regulator and the load.

## 6.4 Device Functional Modes

### 6.4.1 Soft Start

An internal soft start limits the inrush current when the device is being enabled.

### 6.4.2 Normal Mode and Skip Mode Operation

The TPS60150 device has skip mode operation as shown in Figure 6-3. The TPS60150 device enters skip mode if the output voltage reaches 5V +0.1V and the load current is less than 8mA (typical). In skip mode, the TPS60150 device disables the oscillator and decreases the prebias current of the output stage to reduce the power consumption. Once the output voltage dips less than the threshold voltage of 5V +0.1V, the TPS60150 device begins switching to increase output voltage until the output reaches 5V +0.1V. When the output voltage dips less than 5V, the TPS60150 device returns to normal pulse width modulation (PWM) mode; thereby reenabling the oscillator and increasing the prebias current of the output stage to supply output current.

The skip threshold voltage and current depend on input voltage and output current conditions.

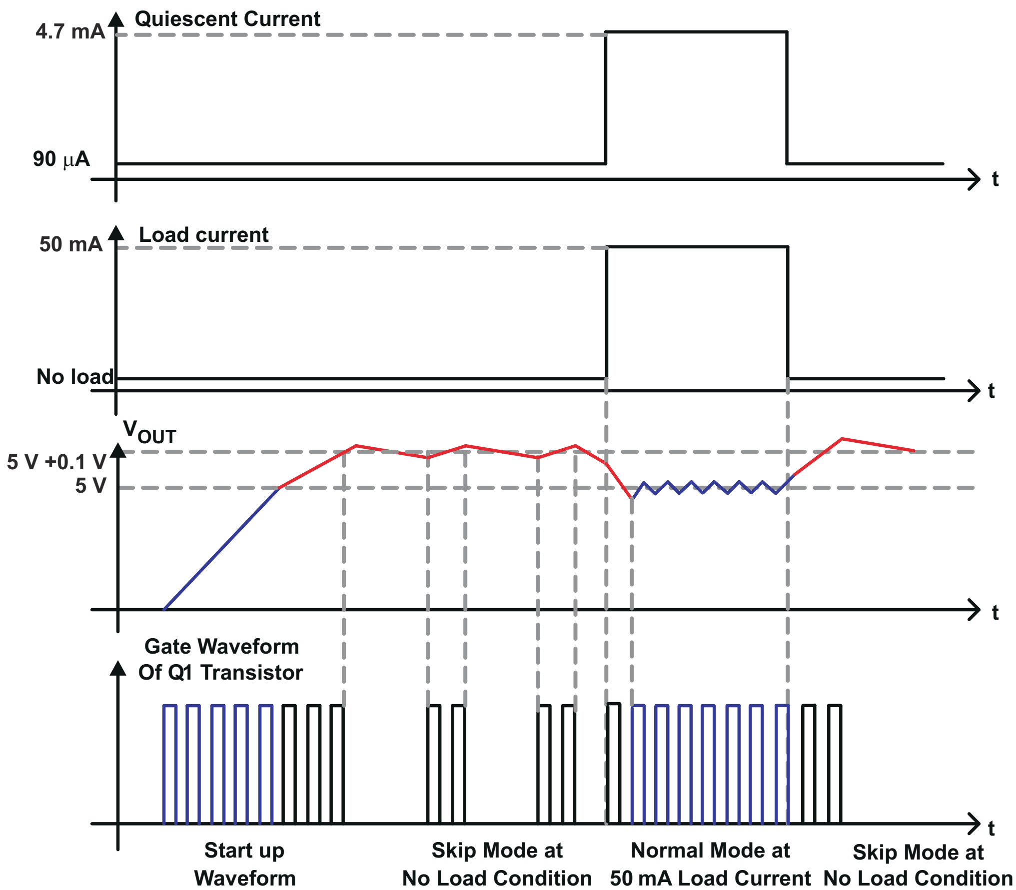



**Figure 6-3. Normal Mode and Skip Mode Operation**

#### *6.4.3 Short-Circuit Protection*

The TPS60150 device has internal short-circuit protection to protect the IC when the output is shorted to ground. To avoid damage when output is shorted to ground, the short-circuit protection circuitry senses output voltage and clamps the maximum output current to 80mA (typical).

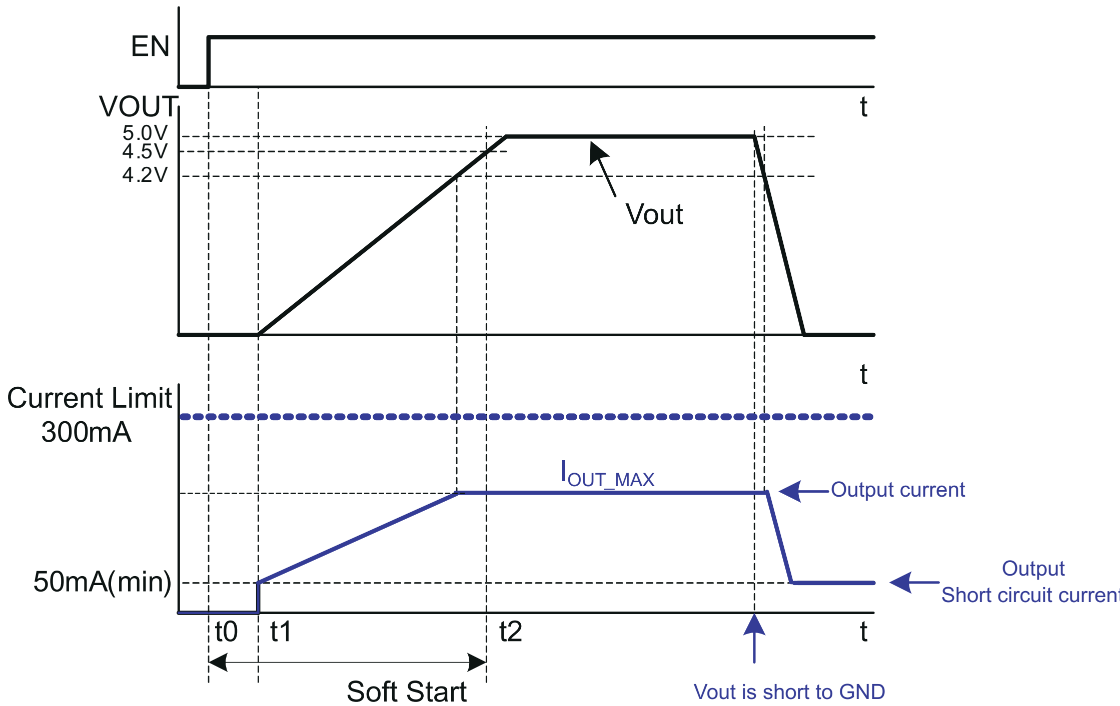



**Figure 6-4. Maximum Output Current Capability and Short-Circuit Protection**

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

Most battery-powered portable electronics allow and require data transfer with a PC. One of the fastest data transfer protocols is through USB On-the-Go (OTG). As Figure 7-1 shows, the USB OTG circuitry in the portable device requires a 5V power rail and up to 140mA of current. The TPS60150 device can be used to provide a 5V power rail in a battery powered system.

## 7.2 Typical Application

### *7.2.1 USB On the Go Circuitry*

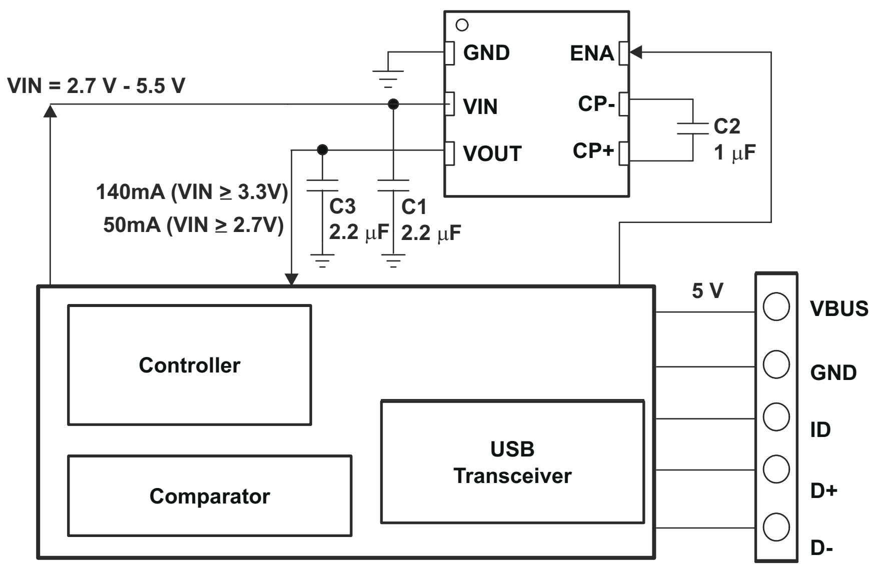



**Figure 7-1. Application Circuit for OTG System**

#### 7.2.1.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions* section.

#### 7.2.1.2 Detailed Design Procedure

##### *7.2.1.2.1 Capacitor Selection*

For minimum output voltage ripple, the output capacitor ($C_{OUT}$) must be a surface-mount ceramic capacitor. Tantalum capacitors generally have a higher effective series resistance (ESR) and can contribute to higher output voltage ripple. Leaded capacitors also increase ripple due to the higher inductance of the package. To achieve the best operation with low input voltage and high load current, the input and flying capacitors ($C_{IN}$ and $C_F$, respectively) must also be surface-mount ceramic types.

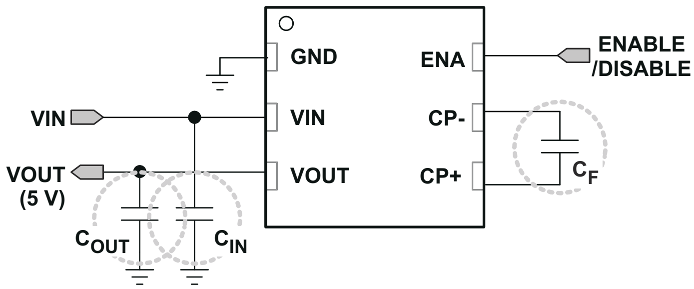



**Figure 7-2. Capacitors**

Generally, $C_{FLY}$ can be calculated using Equation 2.

$$Q_{charging} = c \times v = C_{FLY} \times \Delta V_{CFLY},$$
$$Q_{discharging} = i_{discharge} \times t = 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right), \text{ half duty.} \quad (2)$$

Both equation must be the same, $\therefore 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right) = C_{FLY} \times \Delta V_{CFLY}$

$$\therefore C_{FLY} \geq \frac{2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right)}{\Delta V_{CFLY}} = \frac{I_{LOAD(MAX)}}{\Delta V_{CFLY} \times f} \quad (3)$$

If $I_{LOAD}$ = 140mA, f = 1.5MHz, and $\Delta V_{CFLY}$ = 100mV, the minimum value of the flying capacitor must be 1 µF.

Output capacitance, $C_{OUT}$, is also strongly related to output ripple voltage and loop stability,

$$V_{OUT(RIPPLE)} = \frac{I_{LOAD(MAX)}}{(2 \times f \times C_{OUT})} + 2I_{LOAD(MAX)} \times ESR_{COUT} \quad (4)$$

The minimum output capacitance for all output levels is 2.2µF due to control stability. Larger ceramic capacitors or low ESR capacitors can be used to lower the output ripple voltage.

**Table 7-1. Suggested Capacitors (Input, Output, and Flying Capacitor)**

| VALUE | DIELECTRIC MATERIAL | PACKAGE SIZE | RATED VOLTAGE |
|---|---|---|---|
| 4.7µF | X5R or X7R | 0603 | 10V |
| 2.2µF | X5R or X7R | 0603 | 10V |

The efficiency of the charge pump regulator varies with the output voltage, the applied input voltage and the load current.

Use Equation 5 and Equation 6 to calculate the approximate efficiency in normal operating mode is given by:

$$\text{Efficiency}(\%) = \frac{PD(out)}{PD(in)} \times 100 = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100,\ I_{IN} = 2 \times I_{OUT} + I_Q \quad (5)$$

$$\text{Efficiency}(\%) = \frac{V_{OUT}}{2 \times V_{IN}} \times 100 \ (I_{IN} = 2 \times I_{OUT}) \quad \text{Quiescent current was neglected.} \quad (6)$$

#### 7.2.1.3 Application Curves

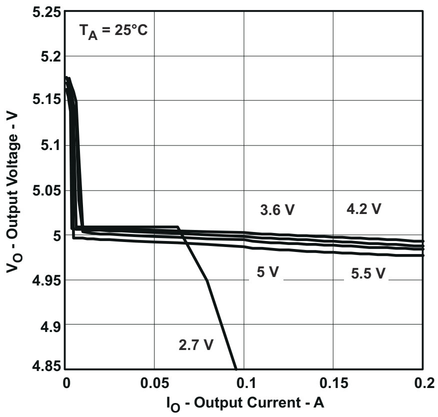



**Figure 7-3. Output Voltage vs Output Current**

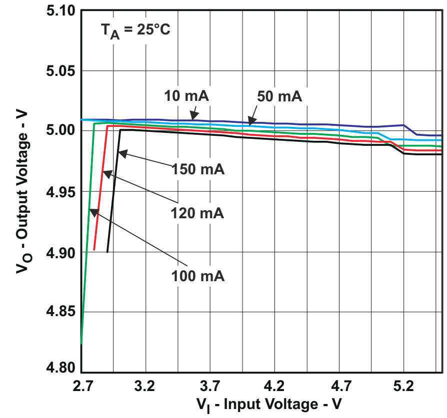



**Figure 7-4. Output Voltage vs Input Voltage**

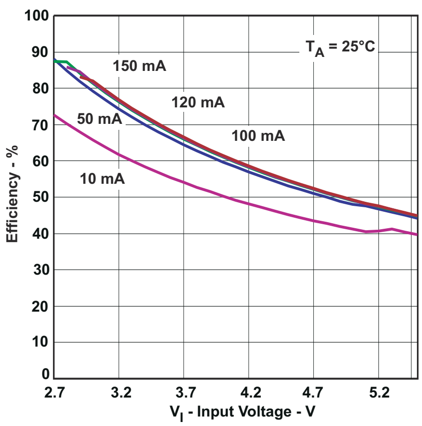
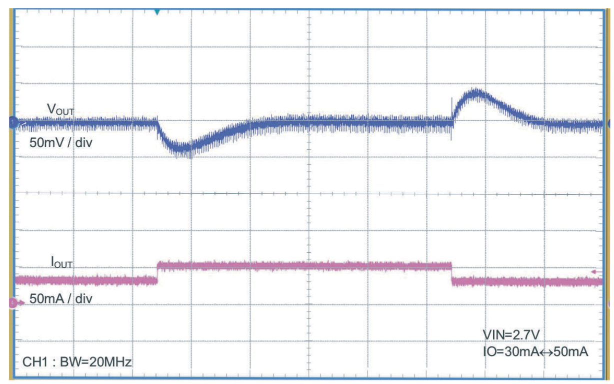
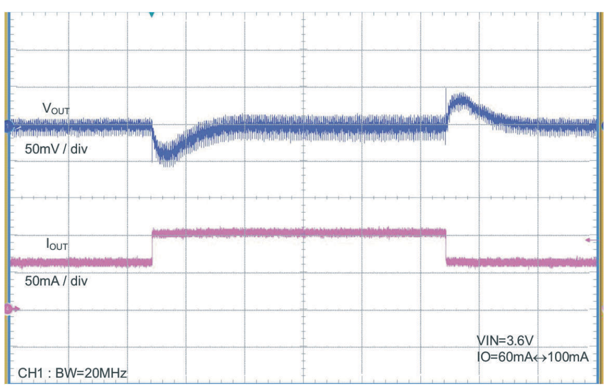



**Figure 7-5. Efficiency vs Input Voltage**



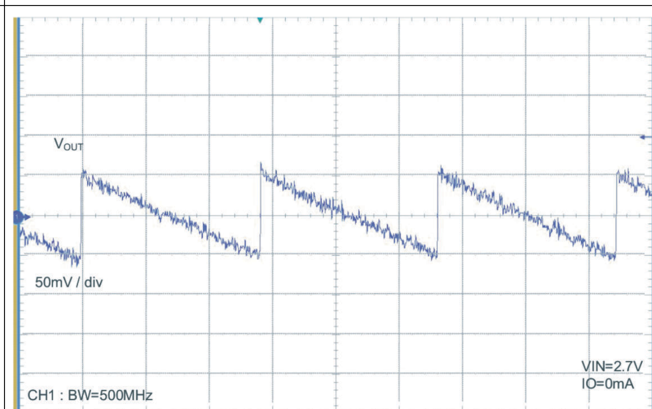

20 µs/div

**Figure 7-6. Load Transient Response $V_{IN}$ = 2.7V, IO = 30mA to 50mA**



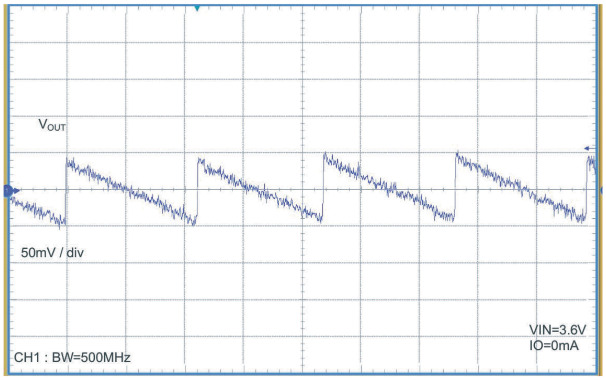

20 µs/div

**Figure 7-7. Load Transient Response $V_{IN}$ = 3.6V, IO = 60mA to 100mA**



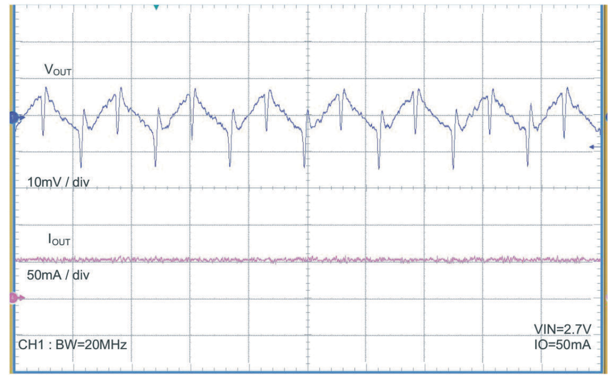

5 ms/div

**Figure 7-8. Output Ripple Voltage (Skip Mode) $V_{IN}$ = 2.7V, IO = 0mA**



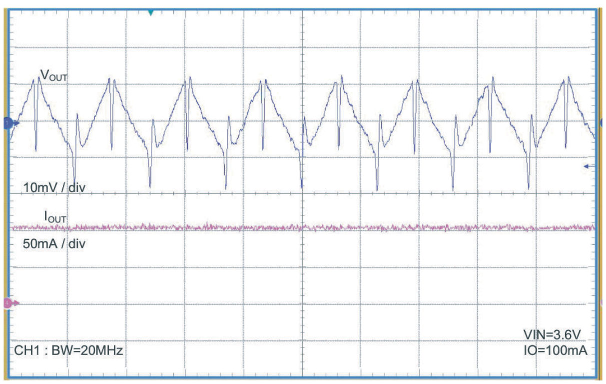

5 ms/div

Figure 7-9. Output Ripple Voltage (Skip Mode) $V_{IN}$ = 3.6V, IO = 0mA



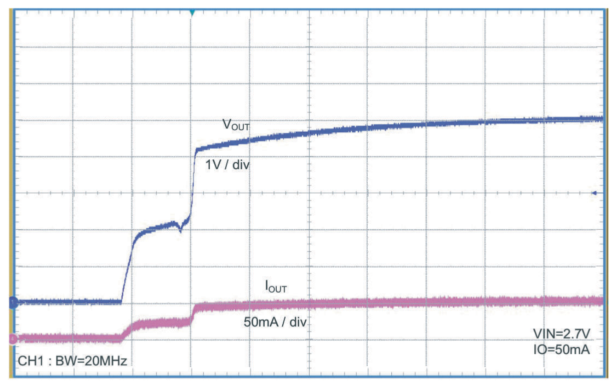

500 ns/div

Figure 7-10. Output Ripple Voltage (Normal Mode) $V_{IN}$ = 2.7V, IO = 50mA



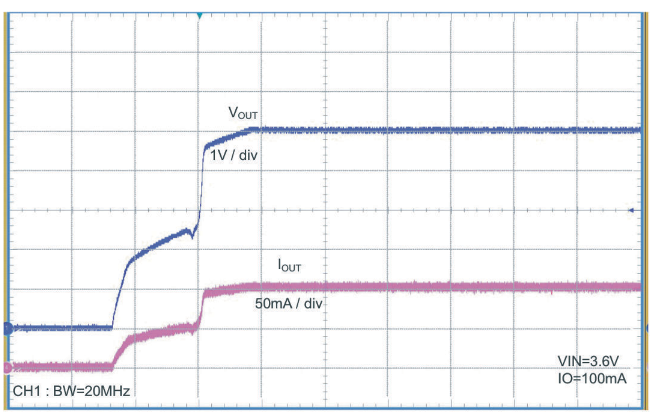

500 ns/div

Figure 7-11. Output Ripple (Normal Mode) $V_{IN}$ = 3.6V, IO = 100mA



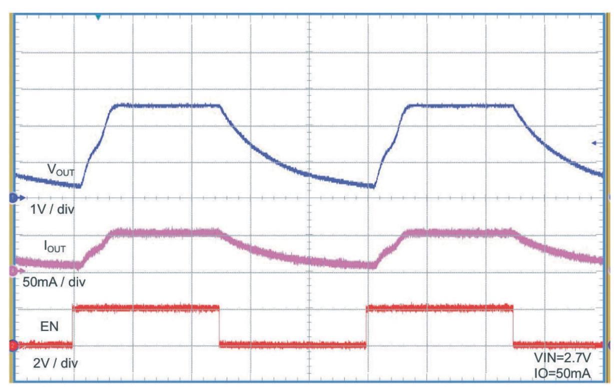

1 ms/div

Figure 7-12. Power On $V_{IN}$ = 2.7V, IO = 50mA




1 ms/div

Figure 7-13. Power On $V_{IN}$ = 3.6V, IO = 100mA




200 µs/div

Figure 7-14. Enable / Disable $V_{IN}$ = 2.7V, IO = 50mA

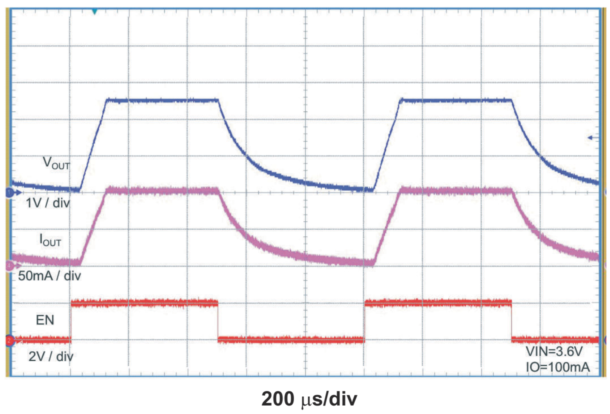



Figure 7-15. Enable / Disable $V_{IN}$ = 3.6V, IO = 100mA

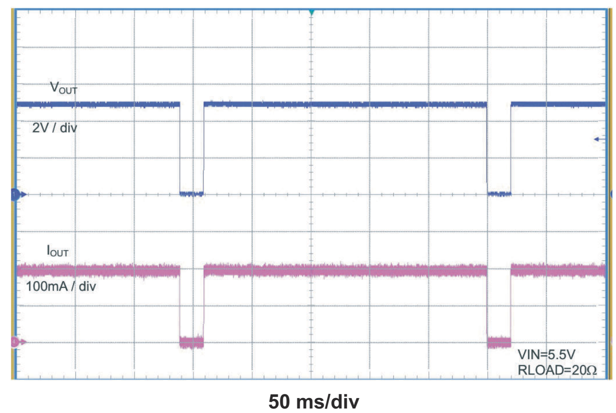



Figure 7-16. Thermal Shutdown Operation $V_{IN}$ = 5.5V, $R_{LOAD}$= 20 Ω

### *7.2.2 System Example*

Low-cost portable electronics with small LCD displays require a low-cost design for providing the WLED backlight. As shown in Figure 7-17, the TPS60150 device can also be used to drive several WLEDs in parallel, with the help of ballast resistors.

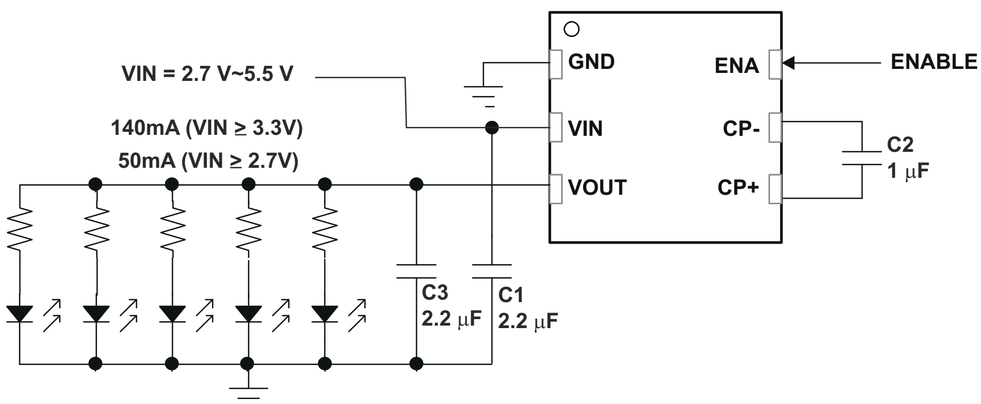



Figure 7-17. Application Circuit for Driving White LEDs

## 7.3 Power Supply Recommendations

The TPS60150 device has no special requirements for the input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS60150 device.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

Large transient currents flow in the VIN, VOUT, and GND traces. To minimize both input and output ripple, keep the capacitors as close as possible to the regulator using short, direct circuit traces.

#### *7.4.2 Layout Example*

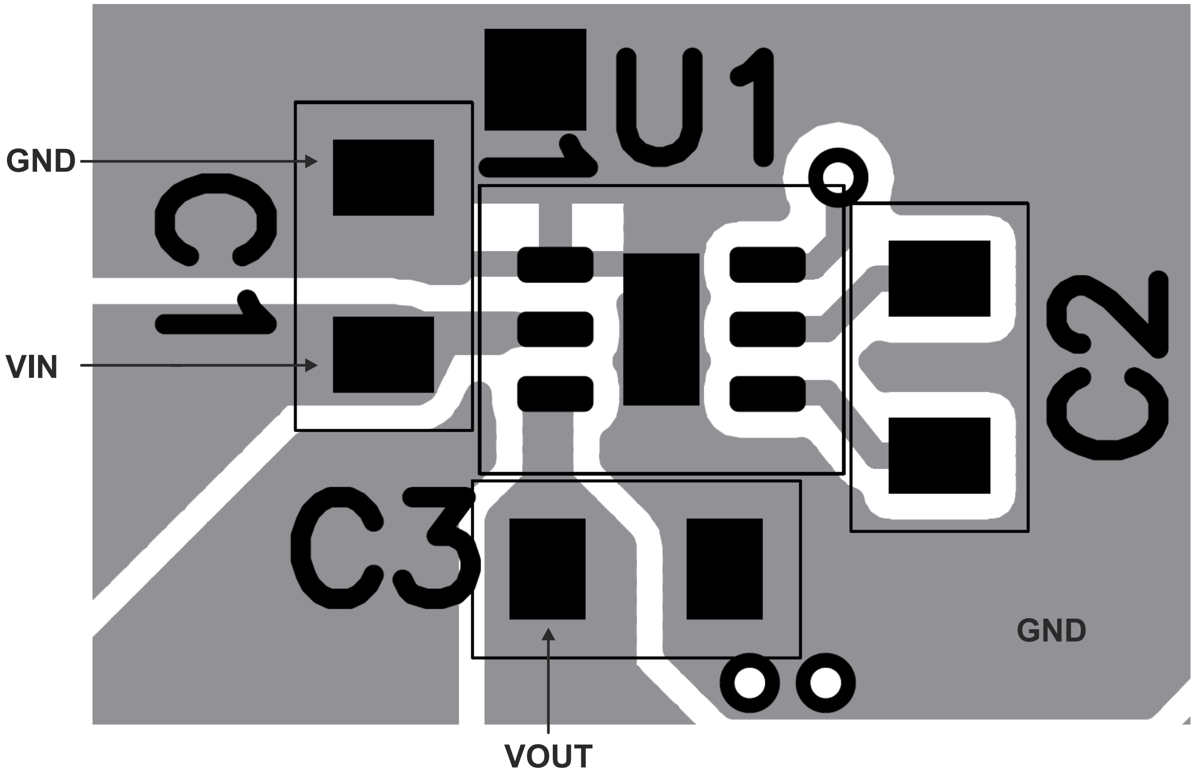



**Figure 7-18. Recommended PCB Layout**

# 8 Device and Documentation Support

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Add VOUT = 0V to test condition about shutdown current spec in Electrical Characteristics.

**Changes from Revision C (October 2015) to Revision D (April 2026)** — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Add $V_{OUT}$ = 0V to test condition about shutdown current spec in the *Electrical Characteristics* table............... 5

**Changes from Revision B (February 2011) to Revision C (October 2015)** — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ........................................................................................................................................ 1

**Changes from Revision A (April 2009) to Revision B (February 2011)** — **Page**

- Added the Thermal Table and deleted the Dissipation Rating Table................................................................ 4

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS60150DRVR | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVR.A | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVR.B | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVRG4 | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVRG4.A | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVRG4.B | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVT | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU \| SN \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVT.A | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CGO |
| TPS60150DRVT.B | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CGO |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

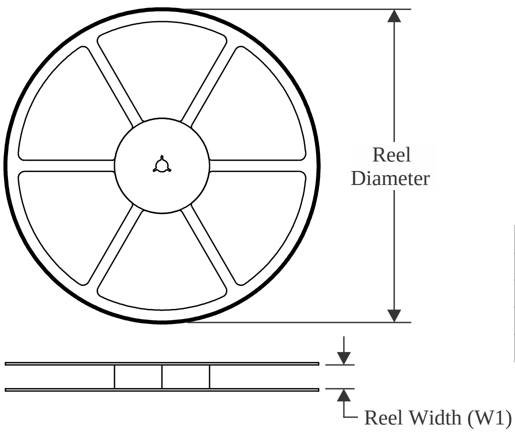
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

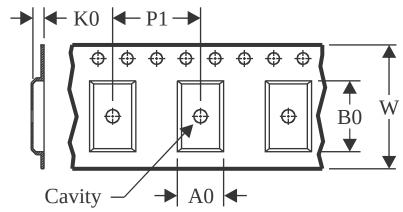
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

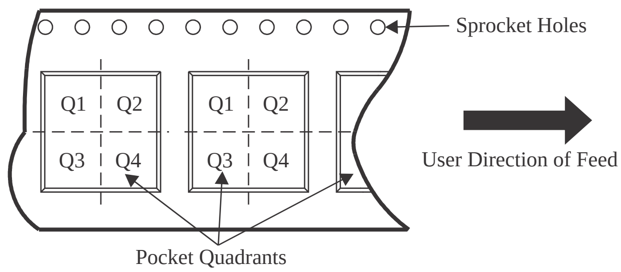



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

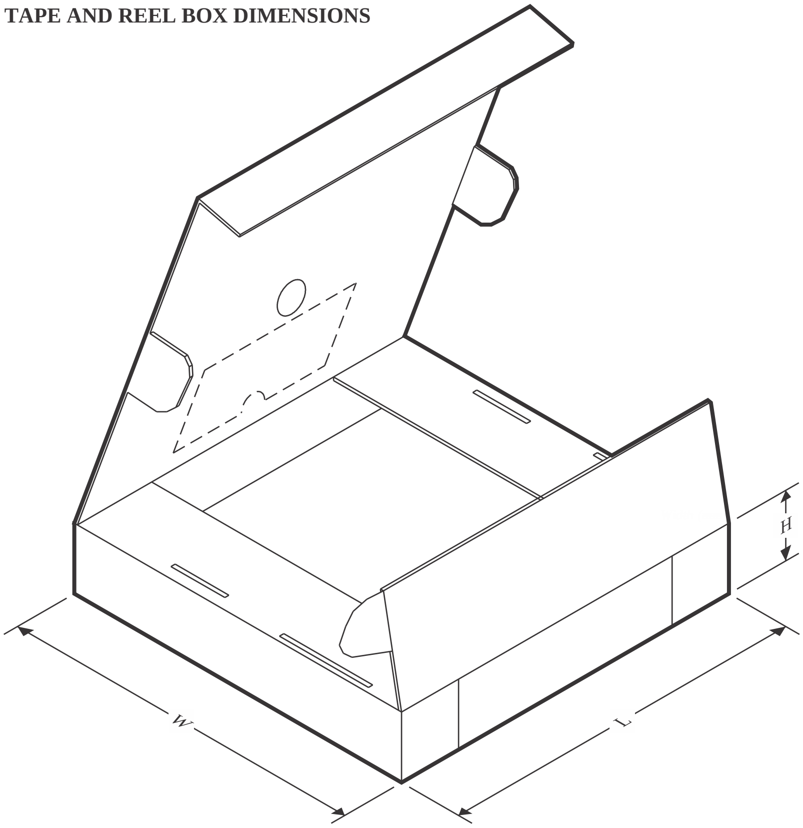
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

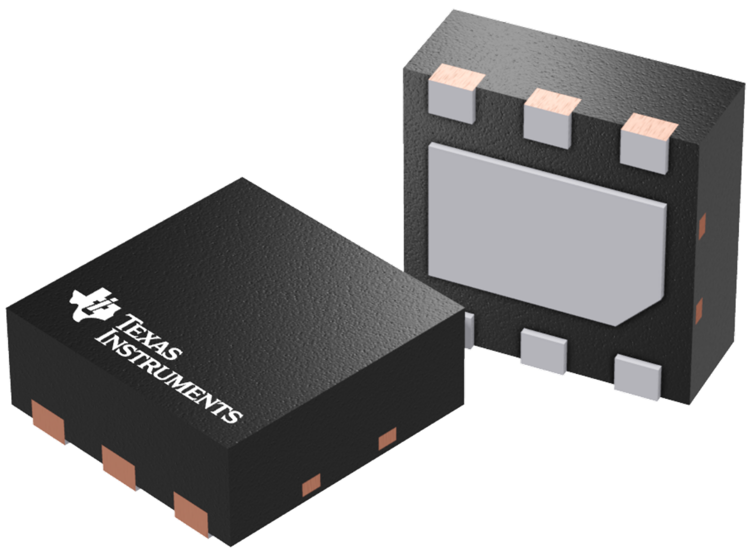
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS60150DRVR | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS60150DRVR | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS60150DRVRG4 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS60150DRVT | WSON | DRV | 6 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

## TAPE AND REEL BOX DIMENSIONS

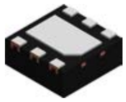



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS60150DRVR | WSON | DRV | 6 | 3000 | 213.0 | 191.0 | 35.0 |
| TPS60150DRVR | WSON | DRV | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS60150DRVRG4 | WSON | DRV | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS60150DRVT | WSON | DRV | 6 | 250 | 182.0 | 182.0 | 20.0 |



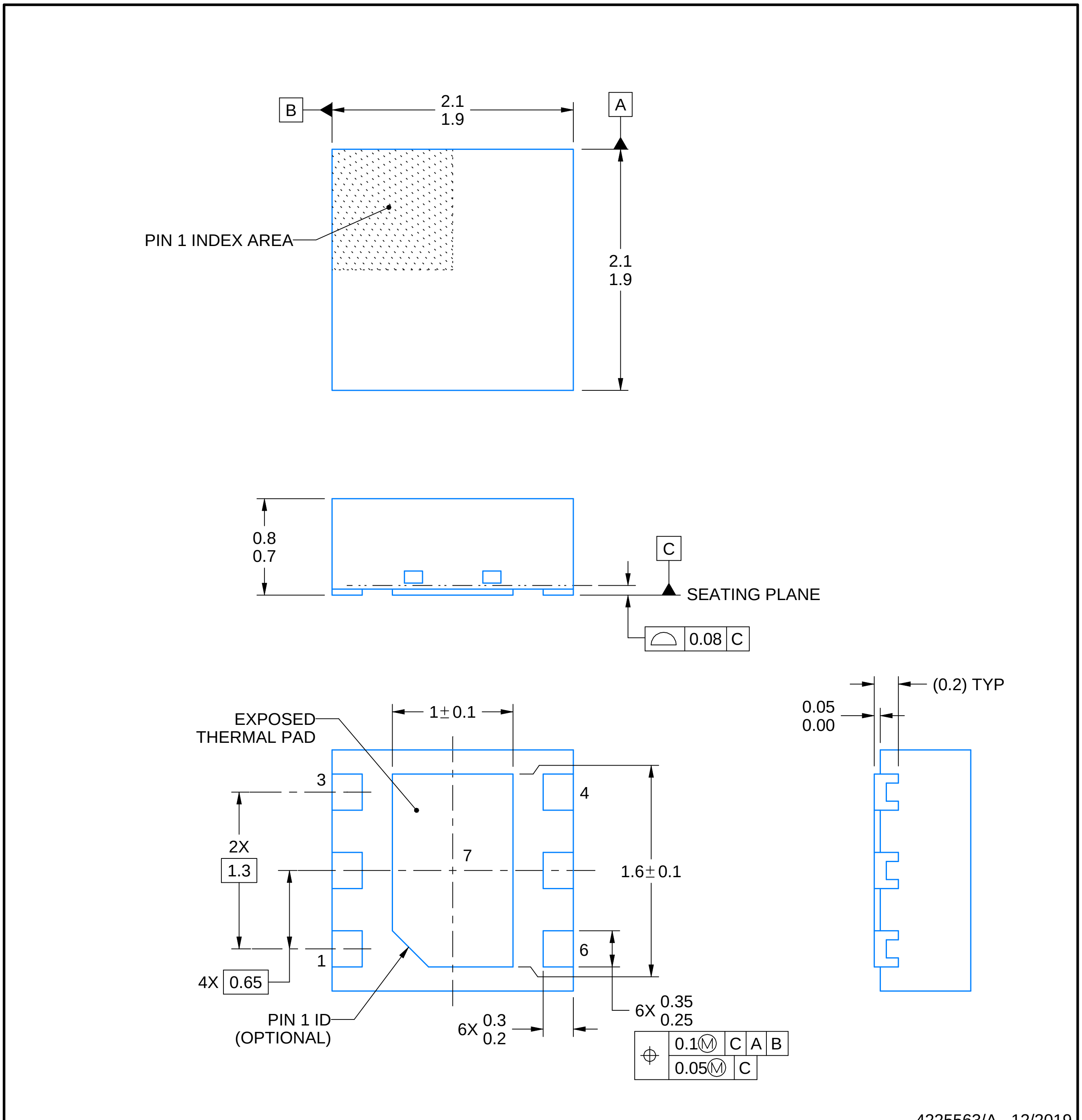
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



# PACKAGE OUTLINE

## WSON - 0.8 mm max height

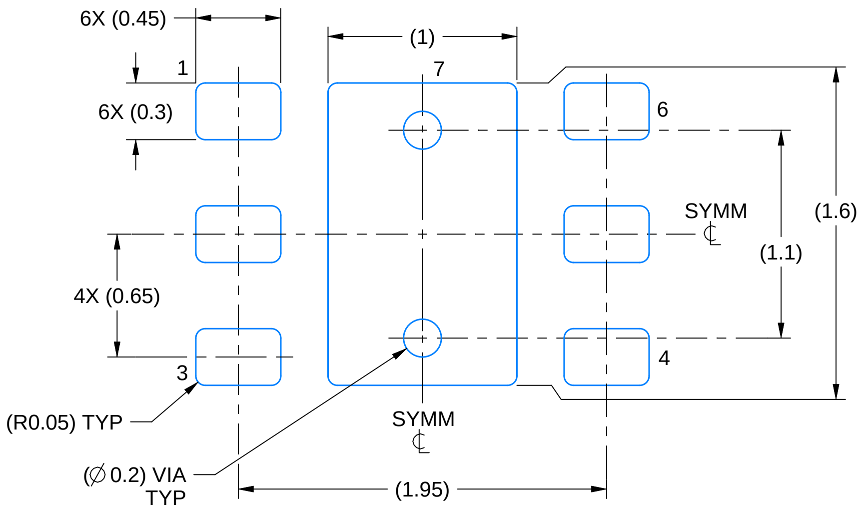
PLASTIC SMALL OUTLINE - NO LEAD



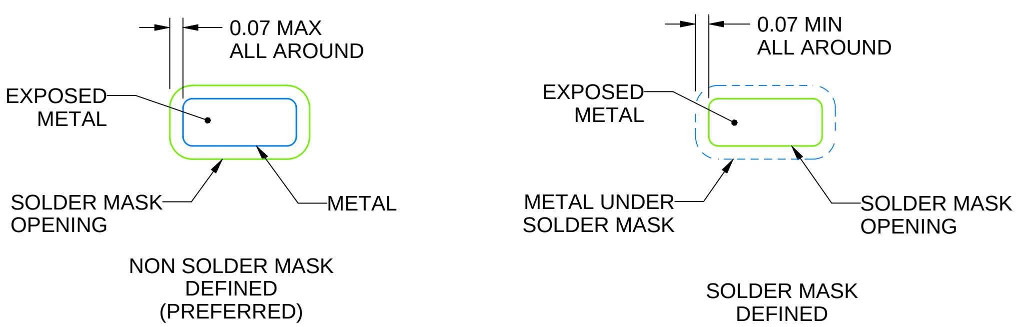

4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

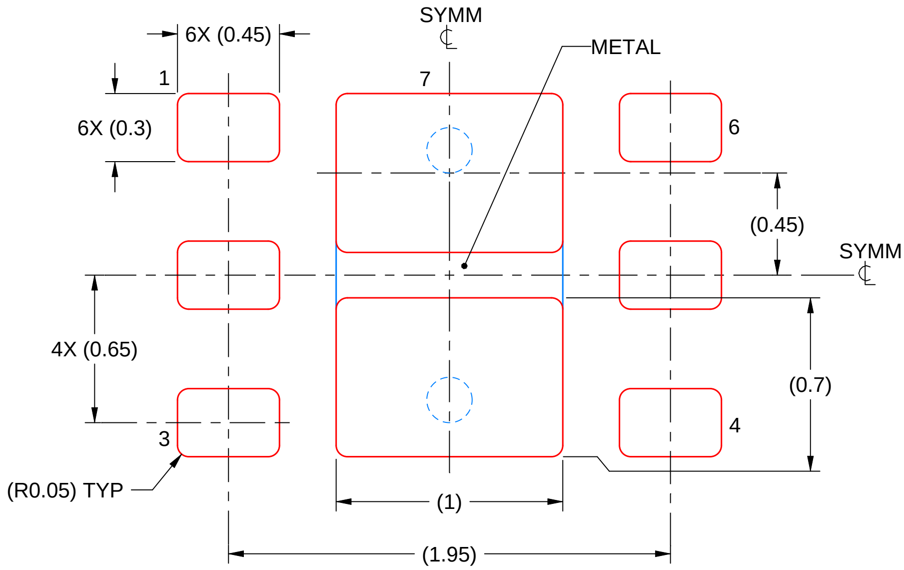



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



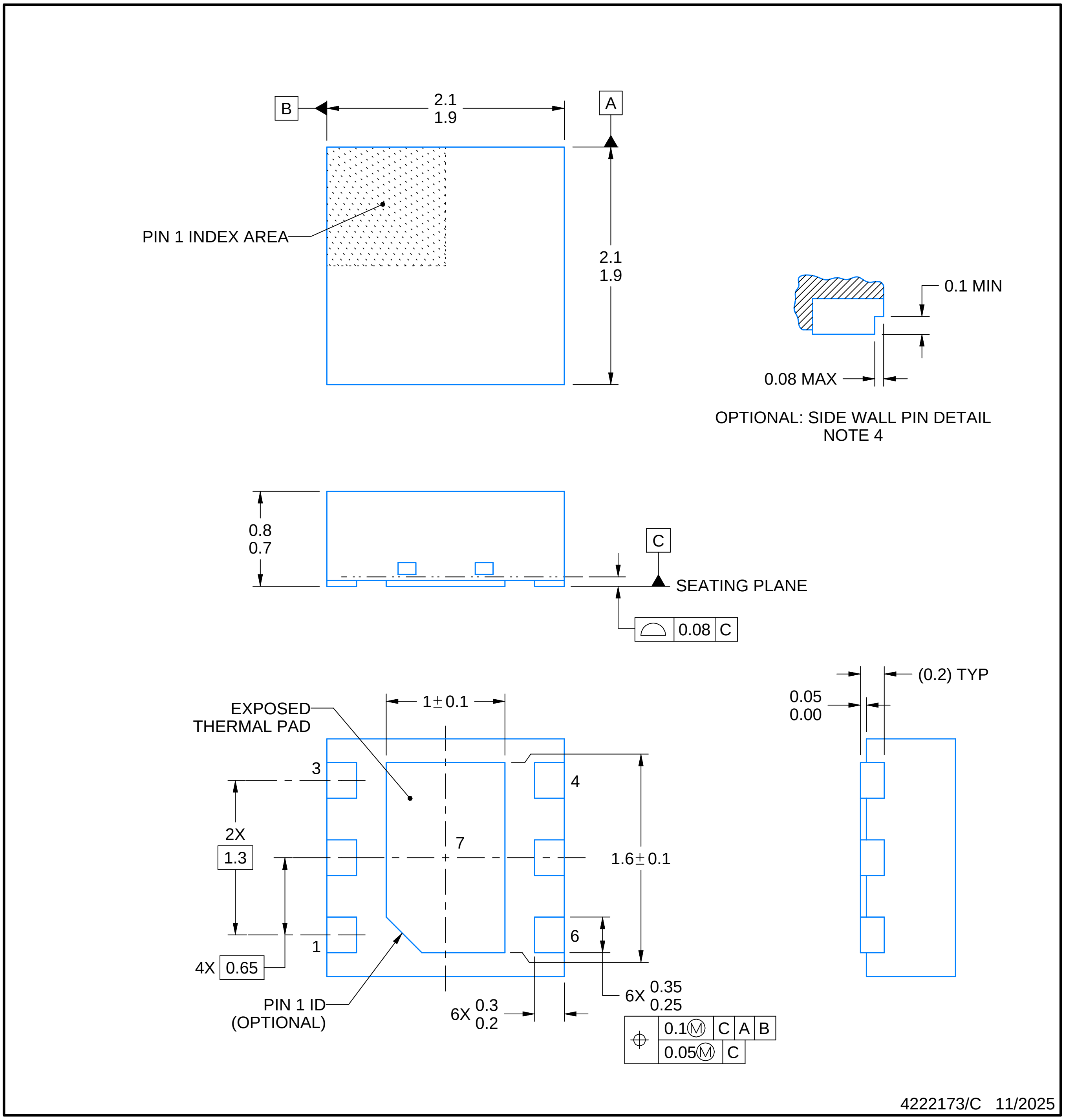

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

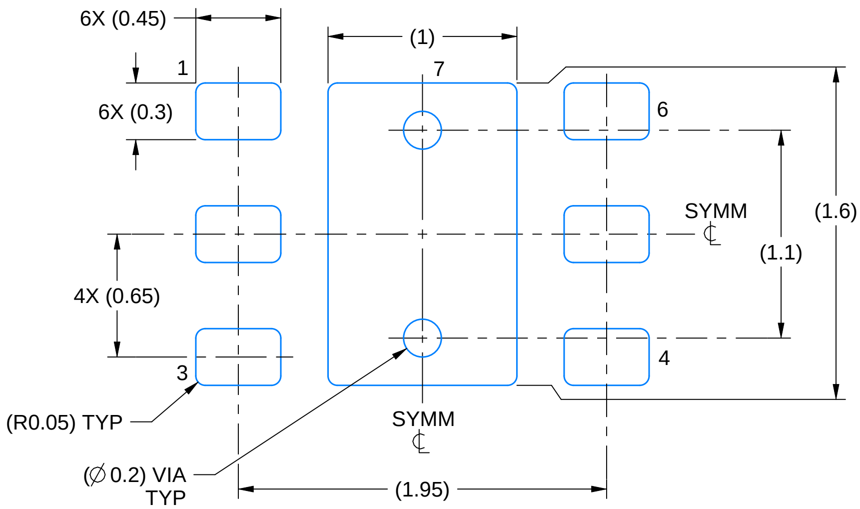
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

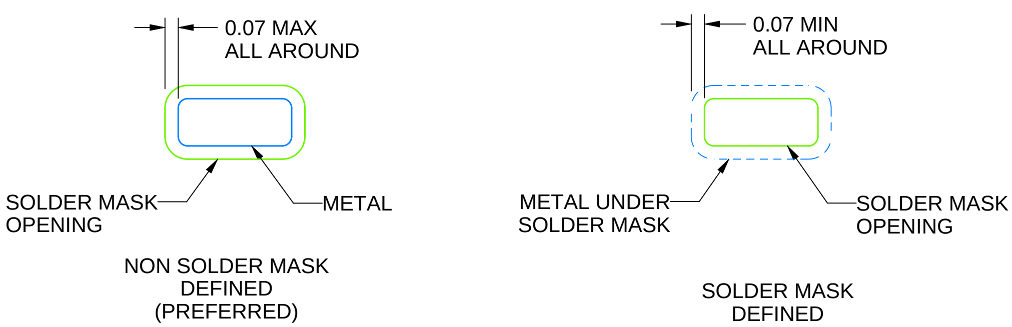



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.




LAND PATTERN EXAMPLE
SCALE:25X

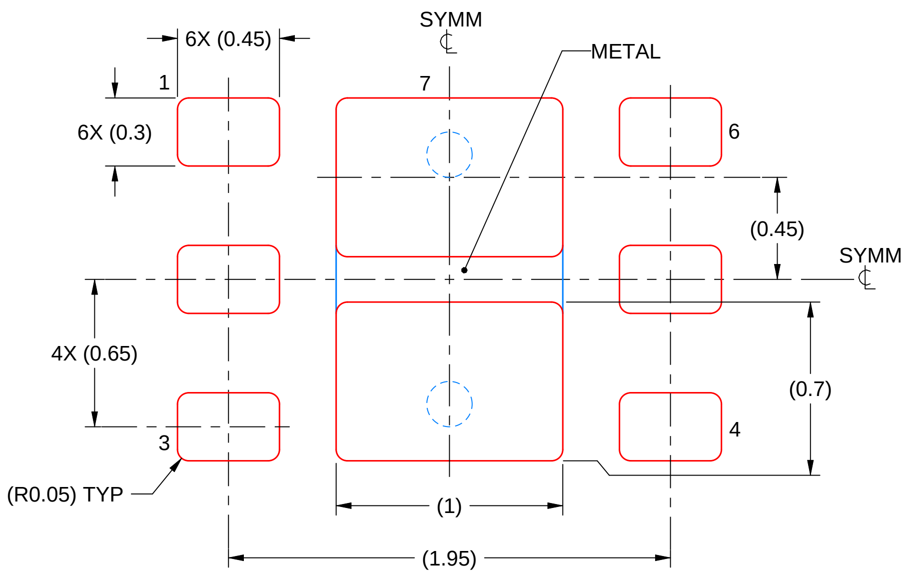



SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.