TEXAS INSTRUMENTS
TPS59632-Q1
SLUSDL4 – FEBRUARY 2020

TPS59632-Q1 2.5-V To 24-V, 3-, 2-, and 1-Phase Step-Down Driverless Controller for Automotive ADAS Applications

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C
  - Human body model ESD classification level H2
  - Charged device model ESD classification level C3B
- Selectable phase count: 3, 2, or 1
- 2.5-V to 24-V conversion voltage range (Phase count, switching frequency and maximum output voltage limitations apply)
- 7-Bit DAC voltage range: 0.50 V to 1.52 V
- Pre-set boot with DAC voltage of 0.800 V
- Accurate, adjustable DC load line (droop) or zero slope load-line
- D-CAP+™ control for fast transient response
- Patented AutoBalance™ phase balancing
- 8 Switching frequency settings from 300 kHz to 1 MHz
- 8 independent levels of Output voltage overshoot reduction (OSR) and undershoot reduction (USR)
- Selectable 8-level current limit
- Load current monitor (Analog and Digital)
- Selectable 8-level voltage slew rate
- Optimized efficiency at light and heavy loads
- I^2C interface for VID control, phase management and telemetry with 8 device addresses
- 5-mm x 5-mm, 32-Pin, 0.5-mm pitch QFN power-pad package with wettable flanks

2 Applications

- Advanced driver assistance systems (ADAS)
- Conditionally automated drive controller
- Vehicle infotainment and cluster

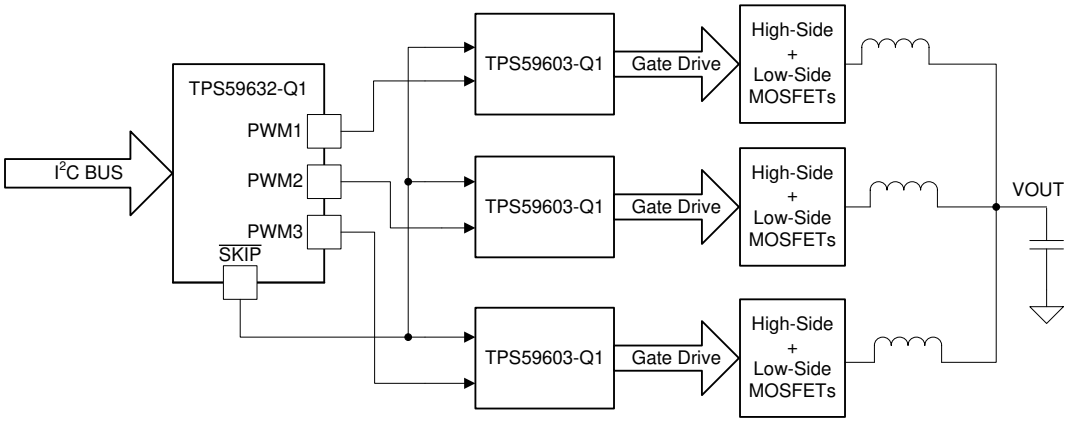
3 Description

The TPS59632-Q1 device is a three-phase driverless step-down controller with advanced features such as D-CAP+™ control architecture with output voltage overshoot reduction (OSR) and undershoot reduction (USR) providing very fast transient response, lowest output capacitance, and high efficiency. The device supports I^2C for dynamic control of the output voltage, phase management for optimized efficiency and current monitor telemetry. The TPS59603-Q1 MOSFET gate driver is designed specifically to accompany this controller to drive the synchronous buck converter powerstage MOSFETs. The TPS59632-Q1 device is packaged in a 5-mm by 5-mm space saving, thermally-enhanced 32-pin, 0.5-mm pitch QFN and is rated to operate at a range between –40°C and 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS59632-Q1	VQFN (32)	5 mm × 5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2020	*	Initial Release

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5 Pin Configuration and Functions

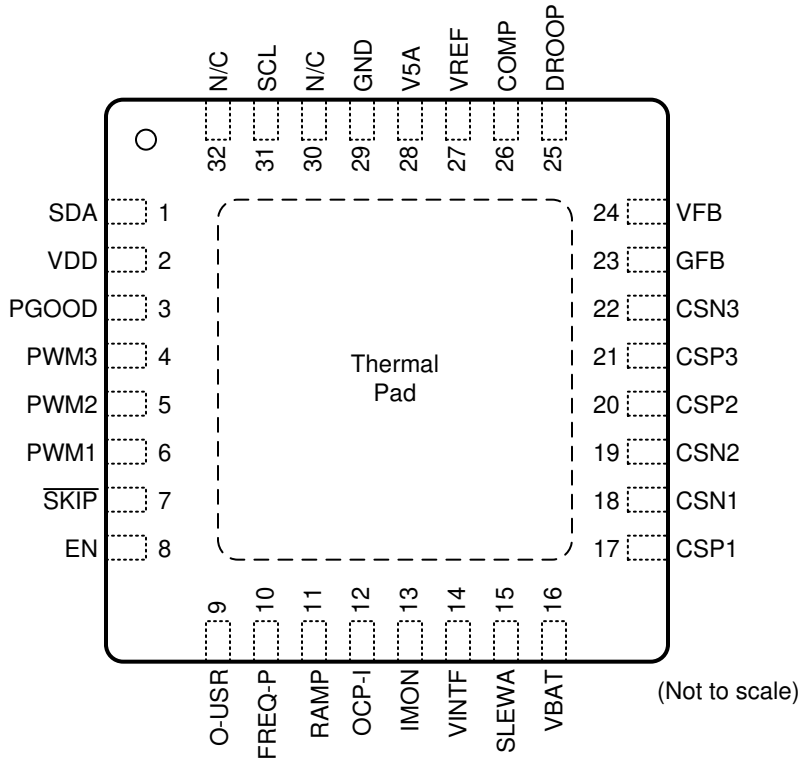


Figure 5-1. RHB Package 32-Pin QFN (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	26	I	Error amplifier summing node. Resistors from VREF to COMP (R_{COMP}) and COMP to DROOP (R_{DROOP}) set the droop gain.
CSP1	17	I	Positive current sense inputs. Connect to the most positive node of current sense resistor or inductor DCR sense network. Tie CSP3, CSP2, or CSP1 (in that order) to 3.3 V to disable the phase.
CSP2	20		
CSP3	21		
CSN1	18	I	Negative current sense inputs. Connect to the most negative node of current sense resistor or inductor DCR sense network. CSN1 has a secondary OVP comparator and includes the soft-stop pulldown transistor.
CSN2	19		
CSN3	22		
DROOP	25	O	Error amplifier output. A resistor pair from VREF to COMP to DROOP sets the droop gain. A_{DROOP} = 1 + R_{DROOP} / R_{COMP}.
EN	8	I	Enable; 100-ns de-bounce. Regulator enters low-power mode, but retains start-up settings when brought low.
FREQ-P	10	I	R to GND sets the per phase switching frequency. MUST connect a resistor to VREF to ensure this pin voltage is above 0.8 V for proper operation.
GFB	23	I	Voltage sense return. Tie to GND on PCB with a 10-Ω resistor to provide feedback when µP is not populated.
GND	29	–	Analog circuit reference; tie to a quiet point on the ground plane.
IMON	13	O	Analog current monitor output. V_{IMON} = Σ V_{ISENSE} × (1 + R_{IMON} / R_{OCP}).
OCP-I	12	I/O	Voltage divider to IMON. Resistor ratio sets the IMON gain (see IMON pin). R to GND (R_{OCP}) selects 1 of 8 OCP levels (per phase, latched at start-up).

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Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
O-USR	9	I	Voltage divider to the VREG pin. Connect a resistor to GND to select the pulse-truncation level and OSR level. Voltage at O-USR selects the USR level.
PU	9	I	Provides pullup resistance to VREF through 10-kΩ resistor.
PAD	GND	–	Thermal pad; tie to the ground plane with multiple vias.
PGOOD	3	O	Power Good output; Open-drain. PGOOD can be configured to go low when the current reaches 70% of the OCP setting value.
PWM1	6	O	PWM controls for the external driver; 5-V logic level. Controller forces signal to the 3-state level when needed.
PWM2	5		
PWM3	4		
RAMP	11	I	Voltage divider to VREF. Connect a resistor to GND to set the ramp setting voltage. The RAMP setting can override the factory ramp setting.
NC	30	NC	No connect. Leave pins floating.
	32		
SCL	31	I	I^2C digital clock line.
SDA	1	I/O	I^2C digital data line.
$\overline{SKIP}$	7	O	This pin is active high to operate synchronous buck MOSFETs in Forced Continuous Conduction Mode (FCCM) active low for skip mode operation. This pin must be connected to the corresponding pin of the drivers for this function.
SLEWA	15	I	The voltage sets the 3 LSBs of the I^2C address. The resistance to GND selects 1 of 8 slew rates. The start-up slew rate (EN transitions high) is SLEWRATE / 2. The ADDRESS and SLEWRATE values are latched at start-up.
VINTF	14	I	Input voltage to power I^2C interface logic. Can be tied to VDD if 3.3-V logic signals are needed.
V5A	28	I	5-V power input for analog circuits; connect through resistor to 5-V plane and bypass to GND with ≥ 1-µF ceramic capacitor
VBAT	16	I	10-kΩ resistor to VBAT provides VBAT information to the on-time circuits for both converters.
VDD	2	I	3.3-V digital power input; bypass to GND with ≥ 1-µF capacitor.
VFB	24	I	Voltage sense line. Tie directly to V_{OUT} sense point of processor. Tie to V_{OUT} on PCB with a 10-Ω resistor to provide feedback when the microprocessor is not populated. The resistance between VFB and GFB is > 1 MΩ.
VREF	27	O	1.7-V, 500-µA reference. Bypass to GND with a 0.22-µF ceramic capacitor.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V5A	–0.3	6.0	V
	VDD, O-USR, RAMP, OCP-I, VFB, CSP1, CSP2, CSP3, CSN1, CSN2, CSN3, VINTF, SDA, SCL, FREQ-P, SLEWA, EN, NC	-0.3	3.6	
	VBAT	–0.3	30	
	COMP	–0.3	3.6	
	GFB	–0.2	0.2	
Output voltage	PGOOD, IMON, VREF, DROOP	–0.3	3.6	V
	PWM3, PWM2, PWM1, $\overline{SKIP}$	–0.3	6.0	
Junction temperature range, T_J		–40	150	°C
Storage Temperature T_{stg}		–55	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per AEC-Q100 Classification Level H2	±2000	V
		Charged device model (CDM), per AEC-Q100 Classification Level C3B	±750	

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V5A	–0.1	5.5	V
	VDD, O-USR, RAMP, OCP-I, VFB, CSP1, CSP2, CSP3, CSN1, CSN2, CSN3, VINTF, SDA, SCL, FREQ-P, SLEWA, EN, NC	-0.1	3.5	
	VBAT	–0.1	28	
	COMP	–0.1	3.5	
	GFB	–0.1	0.1	
Output voltage	PGOOD, IMON, VREF, DROOP	–0.1	3.5	V
	PWM3, PWM2, PWM1, $\overline{SKIP}$	–0.1	5.5	
Operating junction temperature, T_J		–40	125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		TPS59632-Q1 RSM (VQFN) 32 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	31.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.1	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	7.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

6.5 Electrical Characteristics

Over recommended temperature range, 4.5 V ≤ V_{V5A} ≤ 5.5 V, 3.0 V ≤ V_{VDD} ≤ 3.6 V, V_{GFB} = GND, V_{VFB} = V_{OUT}, 0.7 < VFREQ-P ≤ V_{VREF} (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY: CURRENTS, UVLO AND POWER-ON-RESET						
I_{V5-3P}	V5A supply current, 3-phase	V_{VDAC} < V_{VFB} < (V_{VDAC} + 100 mV), EN = 'HI'		3.6	6.0	mA
I_{VDD-3P}	VDD supply current, 3-phase	V_{VDAC} < V_{VFB} < (V_{VDAC} + 100 mV) , EN = 'HI'; digital buses idle		0.2	0.8	
I_{V5-1P}	V5A supply current, 1-phase	VDAC < VFB < (V_{VDAC} + 100 mV) EN = 'HI'		3.5	6.0	
I_{VDD-1P}	VDD supply current, 1-phase	VDAC < VFB < (V_{VDAC} + 100 mV), EN = 'HI'; digital buses idle		0.2	0.8	
I_{V5STBY}	V5A standby current	EN = 'LO'		125	200	µA
$I_{VDDSTBY}$	VDD standby current	EN = 'LO'		23	40	
I_{VINTF}	VINTF supply current	All conditions; digital buses idle		1.7	5.0	
V_{UVLOH}	V5A UVLO 'OK' threshold	V_{VFB} < 200 mV. Ramp up; V_{VDD} > 3 V; EN = 'HI'; Switching begins.	4.2	4.4	4.52	V
V_{UVLOL}	V5A UVLO fault threshold	Ramp down; EN = 'HI'; V_{VDD} > 3 V; V_{VFB} = 100 mV. Switching stops	4.00	4.2	4.35	
V_{5POR}	V5A fault latch reset threshold	Ramp down. EN = 'HI'; V_{VDD} > 3 V. Can restart if V5A rises to V_{UVLOH}, and no other faults present.	1.2	1.9	2.5	
V_{3UVLOH}	VDD UVLO 'OK' threshold	V_{VFB} < 200 mV. Ramp up; V_{V5A} > 4.5 V; EN = 'HI'; Switching begins.	2.5	2.8	3.0	
V_{3UVLOL}	Fault threshold	Ramp down; EN = 'HI'; V5A > 4.5 V; VFB = 100 mV. Switching stops.	2.4	2.6	2.8	
V_{3POR}	VDD fault latch	Ramp down. EN = 'HI'; V5A > 4.5 V. Can restart if VDD goes up to V_{3UVLOH}, and no other faults present.	1.2	1.9	2.5	
$V_{INTFUVLOH}$	VINTF UVLO OK	Ramp up; EN = 'HI'; V5A > 4.5 V; VFB = 100 mV.	1.4	1.5	1.6	
$V_{INTFUVLOL}$	VINTF UVLO falling	Ramp down; EN = 'HI'; V5A > 4.5 V; VFB = 100 mV.	1.3	1.4	1.5	
REFERENCES: VDAC, VREF, BOOT Voltage						
V_{VIDSTP}	VID step size	Change VID0 HI to LO to HI		10		mV
V_{DAC1}	VFB tolerance	1.36 V ≤ V_{VFB} ≤ 1.52 V, I_{OUT} = 0 A	–9		9	
V_{DAC2}		1.0 V ≤ V_{VFB} ≤ 1.35 V; I_{OUT} = 0 A	–8		8	
V_{DAC3}		0.5 V ≤ V_{VFB} ≤ 0.99 V; I_{OUT} = 0 A	–7		7	
V_{VREF}	VREF output	VREF output 4.5 V ≤ V_{V5A} ≤ 5.5 V, I_{VREF} = 0 A	1.66	1.700	1.74	V
$V_{VREFSRC}$	VREF output source	0 A ≤ I_{REF} ≤ 500 µA, HP-2	–4	–3		mV
$V_{VREFSNK}$	VREF output sink	–500 A ≤ I_{REF} ≤ 0 A, HP-2		3	4	
V_{VBOOT}	Internal VFB initial boot voltage	Initial DAC boot voltage		0.8		V
DIFFERENTIAL VOLTAGE SENSE: VFB AND GFB						

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6.5 Electrical Characteristics (continued)

Over recommended temperature range, 4.5 V ≤ V_{V5A} ≤ 5.5 V, 3.0 V ≤ V_{VDD} ≤ 3.6 V, V_{GFB} = GND, V_{VFB} = V_{OUT}, 0.7 < VFREQ-P ≤ V_{VREF} (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
R_{VFB}	VFB/GFB Input resistance	Not in fault, disable, or UVLO, V_{VFB} = V_{DAC} = 1.5 V V_{GFB} = 0 V, measure from VFB to GFB		50		MΩ
V_{DELGND}	GFB Differential	GND to GFB		±100		mV
ERROR AMPLIFIER, CURRENT AMPLIFIER, CURRENT SHARE						
A_{V-EA}	Error amplifier total voltage gain(1)	VFB to DROOP	80			dB
I_{EA_SR}	Error amplifier source current	I_{DROOP}, V_{VFB} = V_{DAC} + 50 mV, R_{COMP} = 1 kΩ		1		mA
I_{EA_SK}	Error amplifier sink current	I_{DROOP}, V_{VFB} = V_{DAC} –50 mV, R_{COMP} = 1 kΩ		–1		
I_{CS}	CS pin input bias current	CSPx and CSNx	–500	0.2	500	nA
A_{CSINT}	Internal current sense gain	Gain from CSPx – CSNx to PWM comparator, $R_{\overline{SKIP}}$ = Open	5.8	6.0	6.2	V/V
I_{BAL_TOL}	Internal current share tolerance	V_{DAC} = 1.70 V, V_{CSP1} – V_{CSN1} = V_{CSP2} – V_{CSN2} = V_{CSP3} – V_{CSN3} = V_{OCPP_MIN}	–3%		+3%	
RAMP SETTINGS						
V_{RAMP}	Compensation ramp amplitude	R_{RAMP} = 20 kΩ +/- 1%		20		mV
		R_{RAMP} = 30 kΩ +/- 1%		60		
		R_{RAMP} = 39 kΩ +/- 1%		100		
		R_{RAMP} ≥ 150 kΩ +/- 1%		40		
SLEW SETTINGS						
SL_{SET}	Slew rate setting for VID change	R_{SLEW} = 20 kΩ +/- 1%	6		10	mV/µs
		R_{SLEW} = 24 kΩ +/- 1%	12		20	
		R_{SLEW} = 30 kΩ +/- 1%	18		30	
		R_{SLEW} = 39 kΩ +/- 1%	24		40	
SL_{START}	Slew rate setting for start-up(1)	EN goes high, R_{SLEW} = 20 kΩ	3		5	mV/µs
ADDRESS SETTINGS						
ADDR	Address setting 3 LSB of I^2C Address (ADDR = 100 0xxx)	V_{SLEWA} ≤ 0.25 V		000b		
		0.35 V ≤ V_{SLEWA} ≤ 0.45 V		001b		
		0.55 V ≤ V_{SLEWA} ≤ 0.65 V		010b		
		0.75 V ≤ V_{SLEWA} ≤ 0.85 V		011b		
		0.95 V ≤ V_{SLEWA} ≤ 1.05 V		100b		
		1.15 V ≤ V_{SLEWA} ≤ 1.25 V		101b		
		1.35 V ≤ V_{SLEWA} ≤ 1.45 V		110b		
		1.55 V ≤ V_{SLEWA} ≤ V_{VREF}		111b		
OVERSHOOT REDUCTION (OSR) SETTINGS						
V_{OSR}	Overshoot Reduction (OSR) Voltage set (1)	R_{O-USR} = 20 kΩ +/- 1%		100		mV
		R_{O-USR} = 24 kΩ +/- 1%		150		
		R_{O-USR} = 30 kΩ +/- 1%		200		
		R_{O-USR} = 39 kΩ +/- 1%		250		
		R_{O-USR} = 56 kΩ +/- 1%		300		
		R_{O-USR} = 75 kΩ +/- 1%		400		
		R_{O-USR} = 100 kΩ +/- 1%		500		
		R_{O-USR} = 150 kΩ +/- 1%		OFF		
UNDERSHOOT REDUCTION (USR) SETTINGS						

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6.5 Electrical Characteristics (continued)

Over recommended temperature range, 4.5 V ≤ V_{V5A} ≤ 5.5 V, 3.0 V ≤ V_{VDD} ≤ 3.6 V, V_{GFB} = GND, V_{VFB} = V_{OUT}, 0.7 < VFREQ-P ≤ V_{VREF} (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{USR}	Undershoot Reduction (USR) Voltage set (1)	V_{O-USR} < 0.25 V		40		mV
		0.35 < V_{O-USR} < 0.45 V		60		
		0.55 < V_{O-USR} < 0.65 V		80		
		0.75 < V_{O-USR} < 0.85 V		120		
		0.95 < V_{O-USR} < 1.05 V		160		
		1.15 < V_{O-USR} < 1.25 V		200		
		1.35 < V_{O-USR} < 1.45 V		240		
		1.55 < V_{O-USR} < V_{VREF}		OFF		
OVER CURRENT PROTECTION (OCP) SETTINGS						
V_{OCP}	OCP voltage (valley current limit at CSPx – CSNx)	R_{OCP-I} = 20 kΩ +/- 1%	5.0	7.0	9.0	mV
		R_{OCP-I} = 24 kΩ +/- 1%	7.0	10.0	13.0	
		R_{OCP-I} = 30 kΩ +/- 1%	10.0	14.0	18.0	
		R_{OCP-I} = 39 kΩ +/- 1%	15.0	19.0	23.0	
		R_{OCP-I} = 56 kΩ +/- 1%	21.0	25.0	29.0	
		R_{OCP-I} = 75 kΩ +/- 1%	28.0	32.0	36.0	
		R_{OCP-I} = 100 kΩ +/- 1%	36.0	40.0	44.0	
		R_{OCP-I} = 150 kΩ +/- 1%	45.0	49.0	53.0	
CURRENT MONITOR (IMON)						
VAL_{ADC}	IMON ADC output	∑ΔCS = 0 mV, A_{IMON} = 3.867	00h	00h	03h	
		∑ΔCS = 4.5 mV, A_{IMON} = 3.867	12h	19h	20h	
		∑ΔCS = 22 mV, A_{IMON} = 3.867	79h	80h	87h	
		∑ΔCS = 44 mV, A_{IMON} = 3.867	FAh	FFh	FFh	
LR_{IMON}	IMON linear range	Each phase, CSPx – CSNx	50			mV
PROTECTION: OVP, UVP, PGOOD						
V_{OVPH}	Fixed OVP voltage	V_{CSN1} > V_{OVPH} for 1 µs	1.60	1.70	1.80	V
R_{SFTSTP}	Soft-stop transistor resistance	Connected to CSN1		100	200	Ω
V_{PGDH}	PGOOD high threshold	Measured at the VFB pin with respect to VID code, device latches OFF	185		245	mV
V_{PGDL}	PGOOD low threshold	Measured at the VFB pin with respect to VID code, device latches OFF	–348		–280	
PWM AND $\overline{SKIP}$ OUTPUTS: I/O VOLTAGE AND CURRENT						
V_{P-S_L}	PWMx / $\overline{SKIP}$ – Low	I_{LOAD} = ± 1 mA		0.15	0.3	V
V_{P-S_H}	PWMx / $\overline{SKIP}$ – High	I_{LOAD} = ± 1 mA	4.2			
$V_{PW-SKLK}$	PWMx / $\overline{SKIP}$ 3-state	I_{LOAD} = ± 100 µA	1.6	1.7	1.8	
LOGIC INTERFACE: VOLTAGE AND CURRENT						
R_{VRTTL}	Pulldown resistance	SDA, V = 0.31 V	4		15	Ω
R_{VRPG}		PGOOD, V = 0.31 V		36	50	
I_{VRTTLK}	Logic leakage current	SDA, SCL = 1.8 V, PGOOD = 3.3 V	–2	0.2	2	µA
$V_{IL,I2C}$	Low-level input voltage	SCL, SDA, VINTF = 1.8 V			0.6	V
$V_{IH,I2C}$	High-level input voltage		1.2			
$V_{IL,EN}$	EN Low-level input voltage				0.5	V
$V_{IH,EN}$	EN High-level input voltage		1.3			
I_{ENH}	I/O leakage, EN	Leakage current , V_{EN} = 1.8 V		24	40	µA
VBAT INPUT RESISTANCE						
R_{VBAT}	VBAT resistance	EN = HI		550		kΩ
		EN = LOW		50		MΩ

(1) Specified by design. Not production tested.

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6.6 Timing Requirements

The device, TPS59632Q1, requires the ENABLE signal on Pin 8 to go from low to high only after the V5A (5-V supply), the VDD (3.3-V supply) and the VBAT rails have gone high.

6.7 Switching Characteristics

Over recommended temperature range, 4.5 V ≤ V_{V5A} ≤ 5.5 V, 3.0 V ≤ V_{VDD} ≤ 3.6 V, V_{GFB} = GND, V_{VFB} = V_{CORE} (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
TIMERS: START-UP, PWM ON-TIME AND I/O TIMING						
$t_{START-CB}$	Cold boot time	V_{BOOT} > 0V , EN = high, time from UVLO to VOUT ramp, C_{REF} = 0.33 µF			1.2	ms
t_{STBY-E}	STBY exit time	Time from EN assertion until PGOOD goes high. V_{VID} = 1.28 V, R_{SLEW} = 39 kΩ			250	µs
$t_{PGDDGLTO}$	PGOOD deglitch time	Time from VFB out of 250 mV VDAC boundary to PGOOD low.		1		µs
$t_{PGDDGLTU}$	PGOOD deglitch time	Time from VFB out of –300 mV VDAC boundary to PGOOD low.		31		µs
t_{ON}	PWM ON-time	R_F = 24 kΩ, V_{BAT} = 12 V, V_{VFB} = 1 V (400 kHz)		230		ns
		R_F = 39 kΩ, V_{BAT} = 12 V, V_{VFB} = 1 V (600 kHz)		164		ns
		R_F = 75 kΩ, V_{BAT} = 12 V, V_{VFB} = 1 V (800 kHz)		140		ns
		R_F = 150 kΩ, V_{BAT} = 12 V, V_{VFB} = 1 V (1 MHz)		122		ns
t_{OFF_MIN}	Controller minimum OFF time	Fixed value	20			ns
t_{ON_MIN}	Controller minimum ON time	R_{CF} = 150 kΩ, V_{BAT} = 20 V, V_{VFB} = 0 V	20			ns
t_{VCCVID}	VID change to VFB change(1)	ACK of VID change command to start of voltage ramp			1	µs
t_{PG2}	PGOOD low after enable goes low	Low-state time after EN goes low.	225	250	275	µs
PWM OUTPUTS: I/O VOLTAGE AND CURRENT						
t_{P-S_H-L}	PWMx H-L transition time	10 to 90%, both edges		7	20	ns
t_{P-S_TRI}	PWMx 3-state transition	10 or 90% to 3-state level, both edges		5	20	ns

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6.8 Typical Characteristics

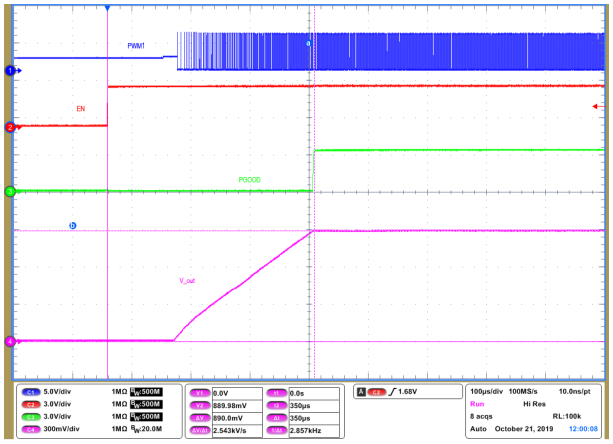


Figure 6-1. 3-phase start up behavior showing EN input and PGOOD output. Input Voltage = 5V, Load current = 10A.

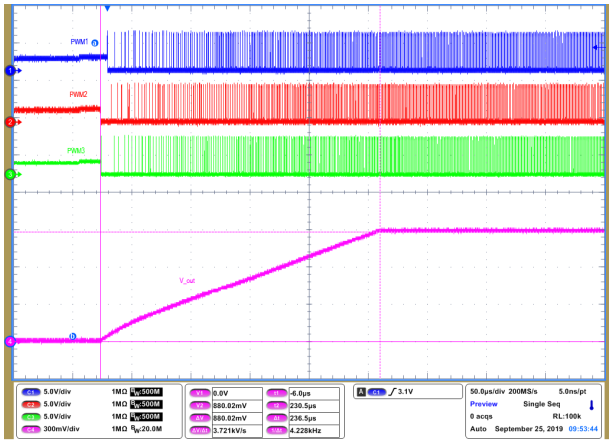


Figure 6-2. 3-phase start up behavior showing switching at startup. Input Voltage = 5V, Load current = 10A.

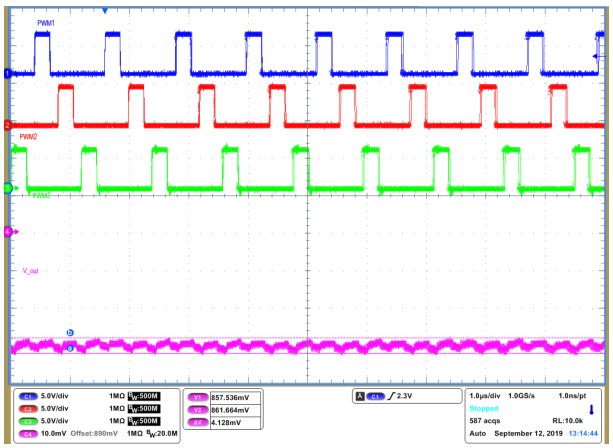


Figure 6-3. 3-phase switching ripple at Input Voltage = 5 V, Load current = 50A, Switching Frequency = 800kHz. Persistence mode.

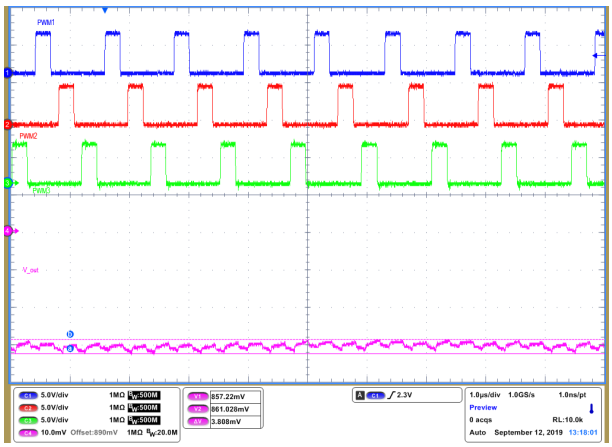


Figure 6-4. 3-phase switching ripple at Input Voltage = 5 V, Load current = 50A, Switching Frequency = 800kHz. Single mode.

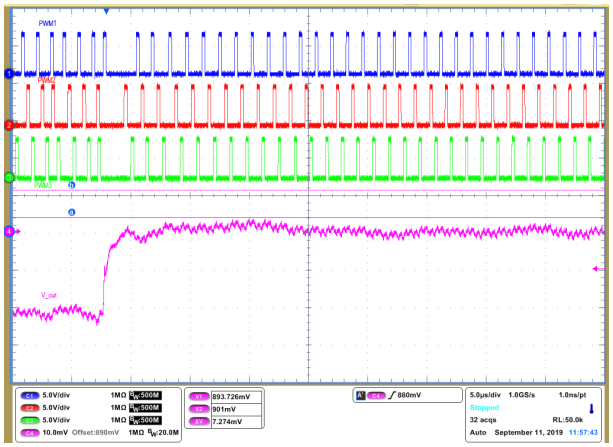


Figure 6-5. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 36A to 0A. Single mode.

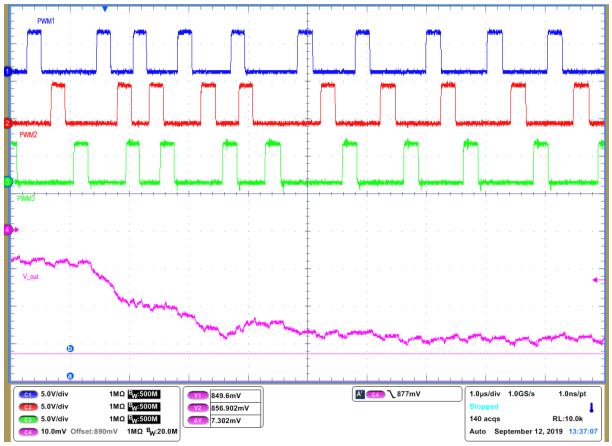


Figure 6-6. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 14A to 50A. Single mode.

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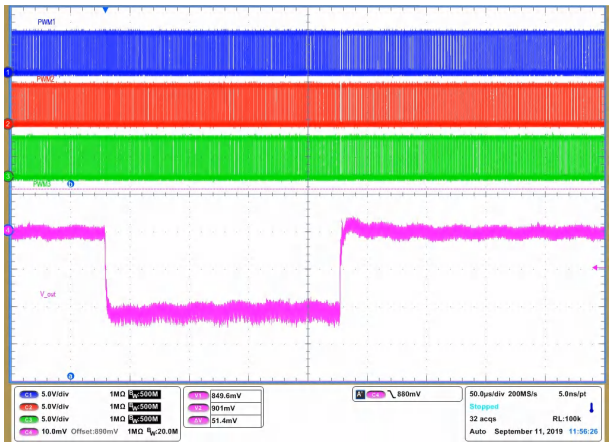


Figure 6-7. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 0A to 36A. Persistence mode

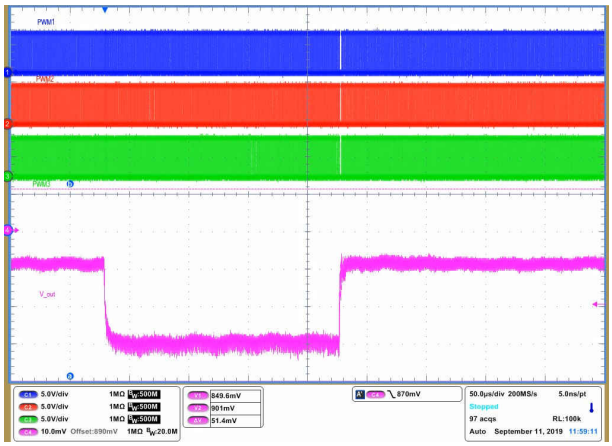


Figure 6-8. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 14A to 50A. Persistence mode

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7 Detailed Description

7.1 Overview

The TPS59632-Q1 device is a DCAP+ mode adaptive on-time controller. The DAC outputs a reference in accordance with the 8-bit VID code, as defined in Table 7-3. This DAC sets the output voltage.

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. With conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS59632-Q1 device, the cycle begins when the current feedback reaches an error voltage level, which corresponds to the amplified difference between the DAC voltage and the feedback output voltage. In the case of 2-phase or 3-phase operation, the device sums the current feedback from all the phases at the output of the internal current-sense amplifiers.

This approach has two advantages:

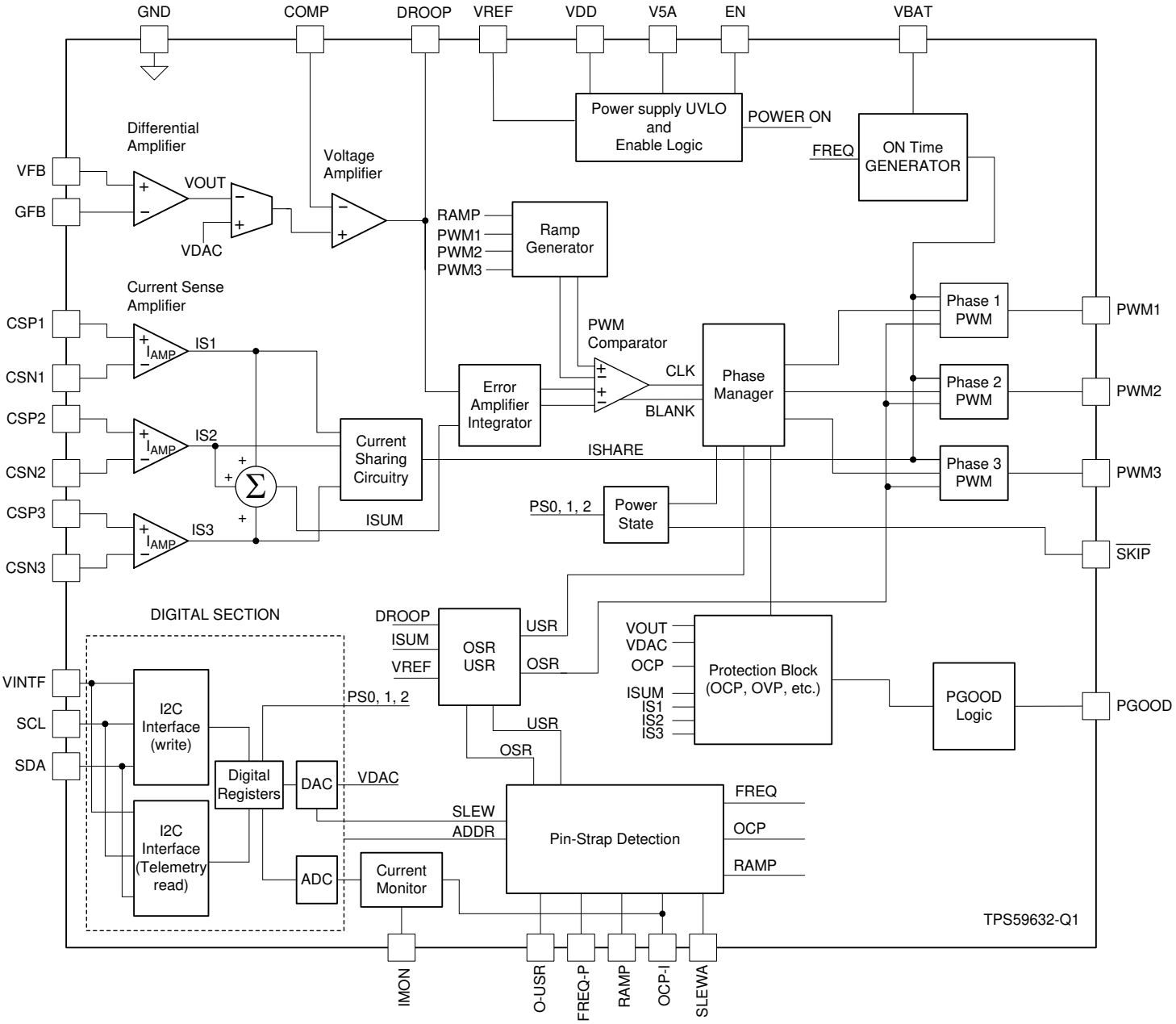
- The amplifier DC gain sets an accurate linear load-line slope, which is required for CPU core applications.
- The device filters the error voltage input to the PWM comparator to improve the noise performance.

In addition, the difference between the DAC-to-output voltage and the current feedback goes through an integrator to give an approximately linear load-line slope even at light loads where the inductor current is in discontinuous conduction mode (DCM).

During a steady-state condition, the phases of the TPS59632-Q1 device switch 180° phase-displacement for 2-phase mode and 120° phase-displacement for 3-phase mode. The phase displacement is maintained both by the architecture and current ripple. The architecture does not allow the high-side gate drive outputs of more than one phase to be ON in any condition except transients. The current ripple forces the pulses to be spaced equally. The controller forces current-sharing adjusting the ON time of each phase. Current balancing requires no user intervention, compensation, or extra components.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

The functional block diagram and Figure 7-1 shows how the converter operates in CCM.

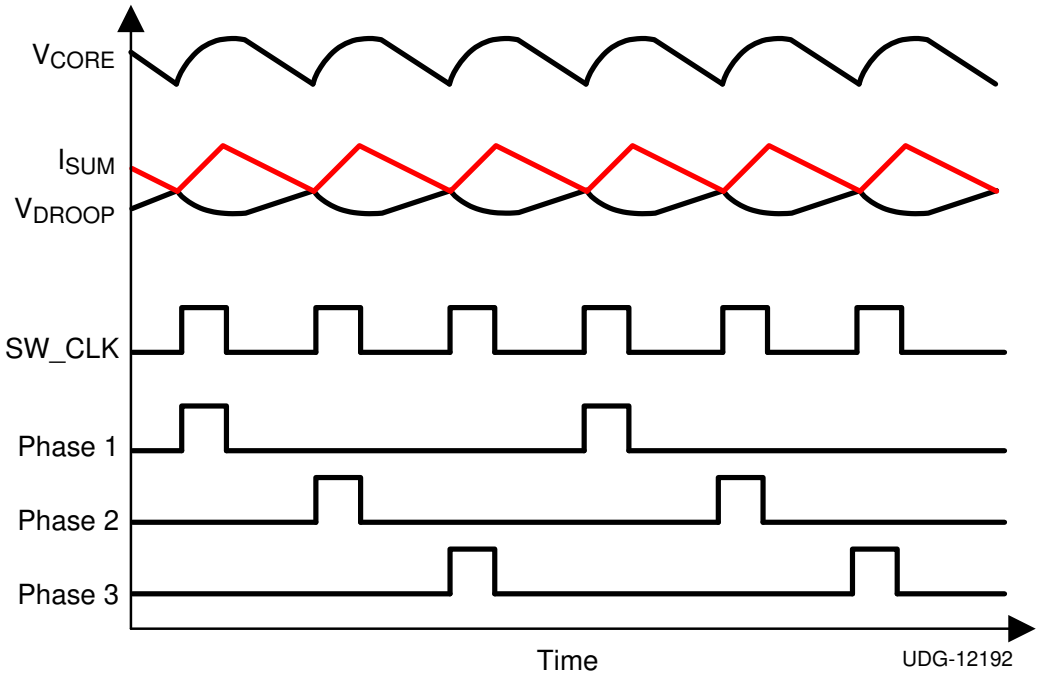


Figure 7-1. D-Cap+ Mode Basic Waveforms

Starting with the condition that the high-side FETs are off and the low-side FETs are on, the summed current feedback (I_{SUM}) is higher than the error amplifier output (V_{DROOP}). I_{SUM} falls until it hits V_{DROOP}, which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator, which generates the internal SW_CLK signal. Each SW_CLK signal corresponds to one switching ON pulse for one phase.

During single-phase operation, every SW_CLK signal generates a switching pulse on the same phase. Also, I_{SUM} voltage corresponds to a single-phase inductor current only.

During multi-phase operation, the controller distributes the SW_CLK signal to each of the phases in a cycle. Using the summed inductor current and cyclically distributing the ON pulses to each phase automatically gives the required interleaving of 360 / n, where n is the number of phases.

7.3.2 Current Sensing

The TPS59632-Q1 provides independent channels of current feedback for every phase, to increase the system accuracy and reduce the dependence of circuit performance on layout compared to an externally summed architecture. The design can use *inductor DCR sensing* to yield the best efficiency or *resistor current sensing* to yield the most accuracy across wide temperature ranges. As inductor DCR sensing is not suitable for automotive applications due to wide variation in current sensing across temperature, resistor sensing is recommended. This sense resistor must be connected in series with the inductor and requires Kelvin sensing terminals for improved current sense accuracy.

The pins CSP1, CSN1, CSP2, CSN2, CSP3, and CSN3 are the inductor current sensing pins for the each of the three phases of the converter.

7.3.3 Load-line (Droop)

The TPS59632-Q1 features programmable droop enabling significant reduction of output capacitors. Figure 7-2 shows the output voltage droop with increasing load current.

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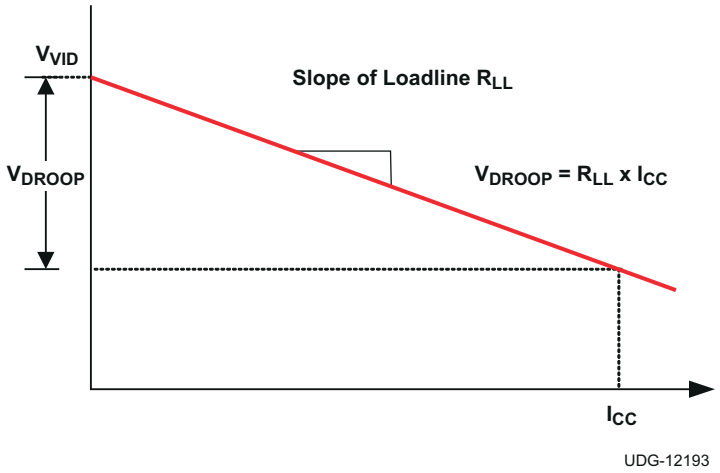


Figure 7-2. Load-Line Slope

$$V_{DROOP} = R_{LL} \times I_{CC} = \frac{R_{CS(eff)} \times A_{CS} \times I_{CC}}{A_{DROOP}} \quad (1)$$

where

- $R_{CS(eff)}$ is the effective current sense resistance, when using either a sense resistor or inductor DCR
- A_{CS} is the gain of the current sense amplifier
- I_{CC} is the load current
- A_{DROOP} is the DROOP gain (see Equation 2)

$$A_{DROOP} = 1 + \left(\frac{R_{DROOP}}{R_{COMP}} \right) \quad (2)$$

where

- resistor, R_{DROOP} is connected between the DROOP pin and the COMP pin
- resistor R_{COMP} is connected between the COMP pin and the VREF pin

This load-line aids in the transient performance as discussed in the following section.

7.3.4 Load Transients

When the load increases suddenly, the output voltage immediately drops. This voltage drop is reflected as a rising voltage on the DROOP pin. This rising voltage forces the PWM to pulse sooner and more frequently, which causes the inductor current to rapidly increase. As the inductor current reaches the new load current, a steady-state operating condition is reached and the PWM switching resumes the steady-state frequency. Similarly, when the load releases suddenly, the output voltage rises. This rise is reflected as a falling voltage on the DROOP pin. This rising voltage forces a delay in the PWM pulses until the inductor current reaches the new load current, when the switching resumes and steady-state switching continues.

For simplicity, neither Figure 7-3 or Figure 7-4 show the ripple on the output V_{CORE} nor the DROOP waveform.

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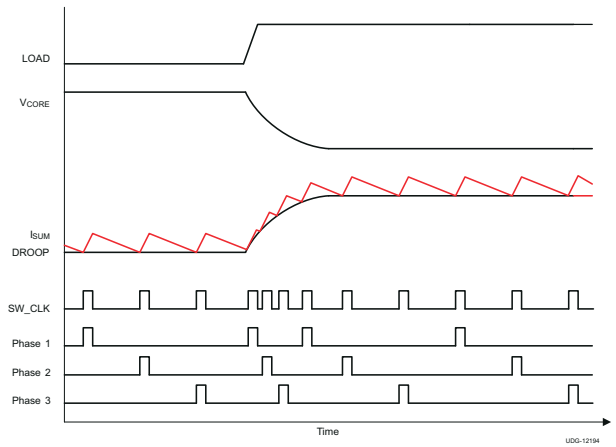


Figure 7-3. Operation During Load Transient (Insertion)

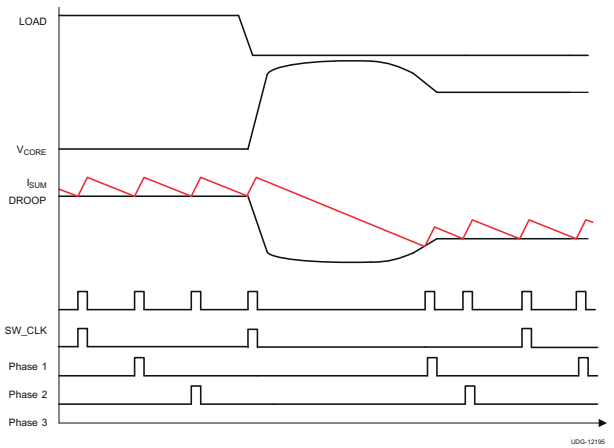


Figure 7-4. Operation During Load Transient (Release)

7.3.5 Overshoot Reduction (OSR)

The problem of overshoot in synchronous buck converters results from the output inductor having a small voltage (V_{OUT}) with which to respond to a transient load release.

With overshoot reduction feature enabled, when the output voltage increases beyond a value that corresponds to a voltage difference between the ISUM voltage and the DROOP pin voltage exceeding the specified OSR voltage (as specified in the Section 6.5 table), at the instant that the low-side drivers are turned OFF. When the low-side driver is turned OFF, the energy in the inductor is partially dissipated by the body diodes. As the overshoot reduces, the low-side drivers are turned ON again. Figure 7-5 shows overshoot reduction by turning off the low-side MOSFET during load transient release.

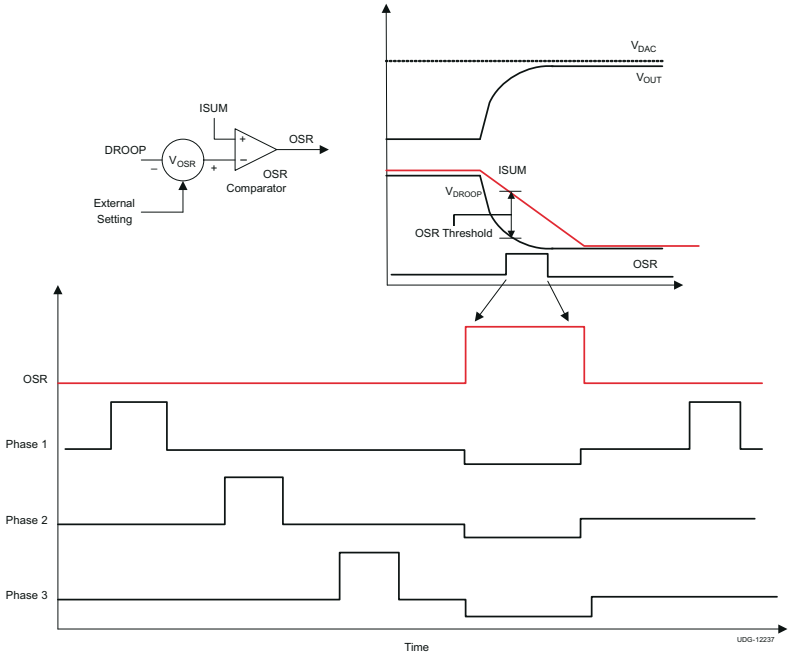


Figure 7-5. Overshoot Reduction

7.3.6 Undershoot Reduction (USR)

When the transient load increase becomes quite large, it is difficult to meet the energy demanded by the load especially at lower input voltages. Then it is necessary to quickly increase the energy in the inductors

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during the transient load increase. This increase is achieved by enabling pulse overlapping. In order to maintain the interleaving of the multi-phase configuration while maintaining pulse-overlapping during load-insertion, the undershoot reduction (USR) mode is entered only when necessary. This device enters this mode is when the difference between DROOP voltage and ISUM voltage exceeds the USR voltage level specified in the Section 6.5 table.

Figure 7-6 shows the undershoot reduction operation. This feature allows for the use of reduced output capacitance while continuing to meet the specification. The device achieves undershoot reduction by overlapping of pulses on all the phases.

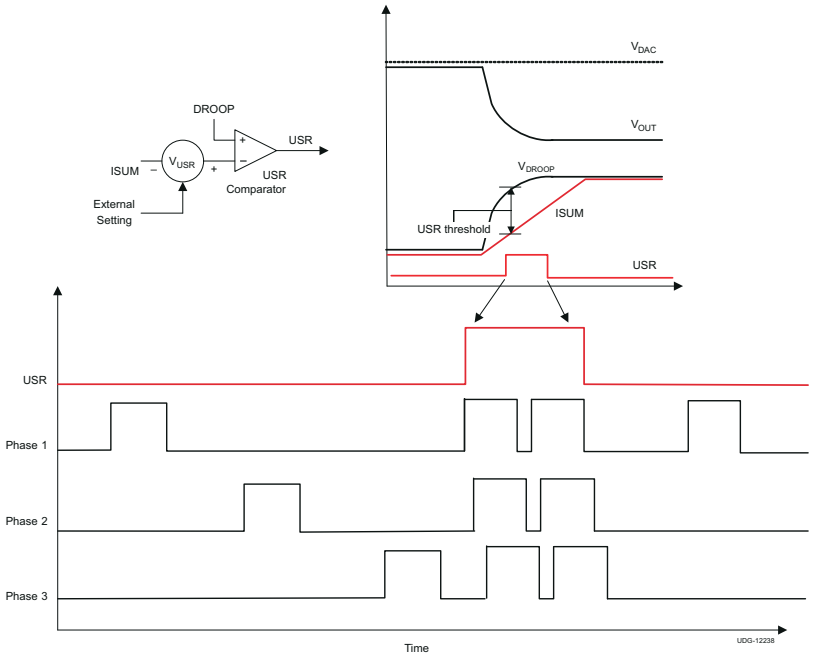


Figure 7-6. Undershoot Reduction

When the transient condition is completed, the interleaving of the phases is resumed.

It should be noted that single-phase mode there is no USR mode of operation.

7.3.7 Autobalance Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase.

The PWM comparator (not shown) starts a pulse when the feedback voltage equals the reference voltage. The VBAT voltage charges $C_{t(on)}$ through the resistor $R_{t(on)}$. The pulse is terminated when the voltage at capacitor $C_{t(on)}$ matches the on-time (t_{ON}) reference, usually the DAC voltage (V_{DAC}).

A current sharing circuit is shown in Figure 7-7. For example, assume that the 5-µs-averaged value of I1 = I2 = I3. In this case, the PWM modulator terminates at V_{DAC}, and the typical pulse width is delivered to the system. If instead, I1 > I_{AVG}, then an offset is subtracted from V_{DAC}, and the pulse width for phase one is shortened, reducing the current in phase one to compensate. If I1 < I_{AVG}, then a longer pulse is produced, again compensating on a pulse-by-pulse basis.

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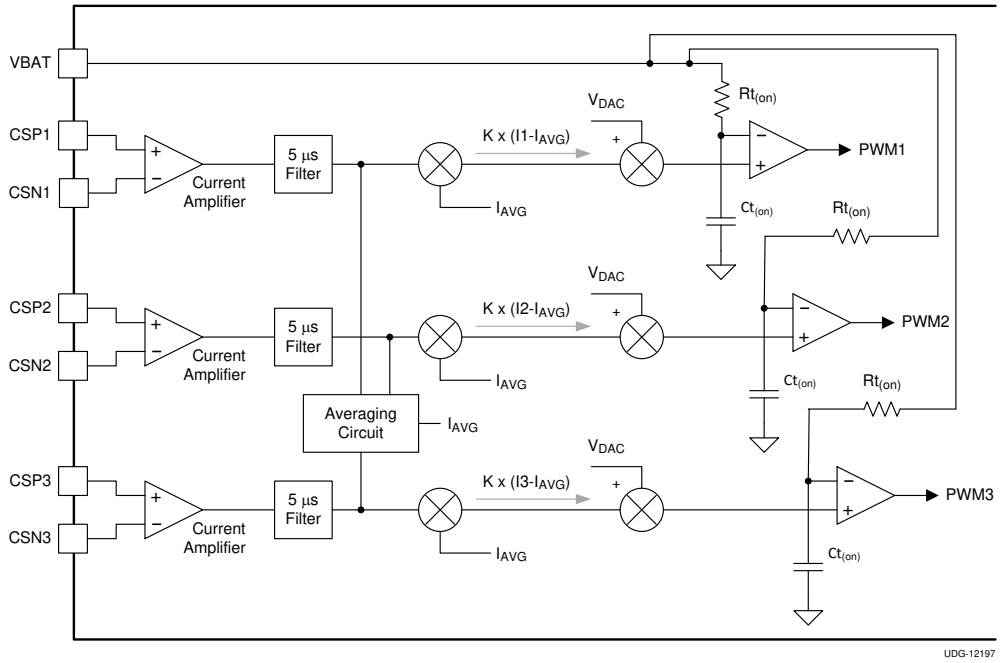


Figure 7-7. Autobalance Current Sharing

7.3.8 PWM And $\overline{\text{SKIP}}$ Signals

The PWM and $\overline{\text{SKIP}}$ signals are outputs of the controller and serve as input to the MOSFET gate driver or DrMOS-type devices. Both signals are 5-V logic signals. The PWM signals are logic high to allow the high-side drive of the external gate driver to turn ON. The PWM signal must be low for the low-side drive of the external gate driver to turn ON. To drive both the signals are OFF, the PWM is set to tri-state. The $\overline{\text{SKIP}}$ signal is active low to set all the phases in Continuous Conduction Mode (CCM) of operation. If $\overline{\text{SKIP}}$ signal is high then the external gate driver turns OFF the Low-side drive to operate in the boundary of CCM and Discontinuous Conduction Mode (DCM).

7.3.9 Bias Power (V5A, VDD, And VINTF) UVLO

The TPS59632-Q1 device continuously monitors the voltage on the V5A, VDD, and VINTF pin to ensure a value high enough to bias the device properly and provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.4 V and has a nominal 200 mV of hysteresis. Once the 5VA,VDD, or VINTF goes below the V_{UVLOL} , the corresponding voltage must fall below V_{POR} (1.5 V) to reset the device.

The input (V_{BAT}) does not include a UVLO function, so the circuit runs with power inputs as low as approximately 3 × V_{OUT}.

7.3.10 Start-Up Sequence

The TPS59632-Q1 device initializes when all of the supplies rise above the UVLO thresholds. This function is also know as a *cold boot*. The device then reads all of the various settings (such as frequency and overcurrent protection). This process takes less than 1.2 ms. During this time, the VSR initializes to the BOOT voltage. The output voltage rises to the VSR level when the EN pin (enable) goes high. Once the BOOT sequence completes, PGOOD is HIGH and the I^2C interface can be used to change the voltage select register (VSR). The current VSR value is held when EN goes low and returns to a high state This function is also known as a *warm boot*.

7.3.11 Power Good Operation

PGOOD is an open-drain output pin that is designed to be pulled-up with an external resistor to a voltage 3.6 V or less. Normal PGOOD operation (exclusive of activation of any faults) is shown in Figure 7-8. On initial power-up PGOOD happens within 6 µs of the DAC reaching its target value. When EN is brought low, PGOOD is also brought low for 250 µs, then is allowed to float. The TPS59632-Q1 device pulls down the PGOOD signal when the EN signal subsequently goes high and returns high again within 6 µs of the end of the DAC ramp. The

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delay period between EN going high and PGOOD going low in this case is less than 1 µs. Figure 7-8 shows the power good operation at initial start-up and with falling and rising EN.

For applications where it is undesirable to have PGOOD high when EN is low, an alternate method of pulling up the open-drain PGOOD signal is possible. In this method, the PGOOD is pulled up to EN logic signal. This ensures that the PGOOD is low when EN goes low.

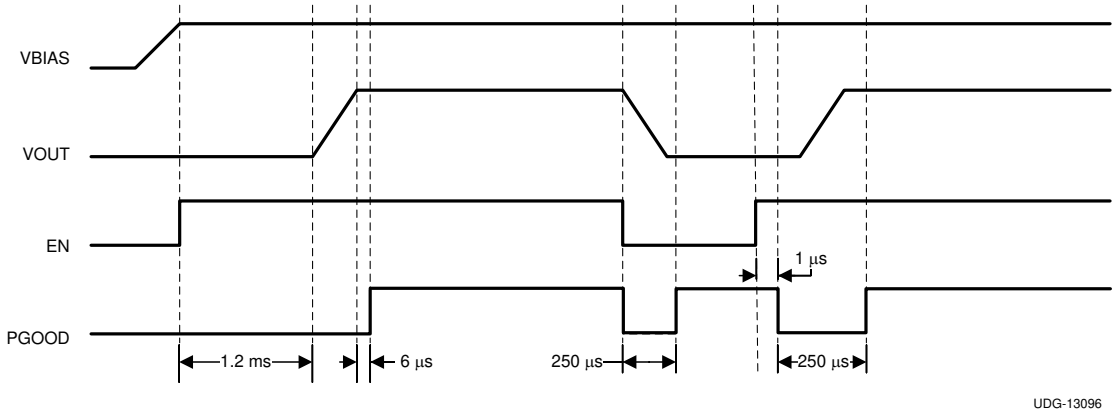


Figure 7-8. Power Good Operation

7.3.12 Analog Current Monitor, IMON, And Corresponding Digital Output Current

The TPS59632-Q1 device includes a current monitor function. The current monitor supplies an analog voltage, proportional to the load current, on the IMON pin.

The current monitor function is related to the OCP selection resistors. The R_{OCP} is the resistor between the OCP-I pin and GND and R_{CIMON} is the resistor between the IMON pin to the OCP-I pin that sets the current monitor gain. Equation 3 shows the calculation for the current monitor gain.

$$V_{IMON} = 10 \times 1 + \frac{(R_{IMON})}{(R_{OCP})} \times \sum V_{CSn} \xrightarrow{yields} V \tag{3}$$

where

- ΣV_{CS} is the sum of the DC voltages at the inputs to the current sense amplifiers

To ensure stable current monitor operation, and at the same time, provide a fast dynamic response, connect a 4.7-nF to 10-nF capacitor from the IMON pin to GND. Connecting higher capacitance will reduce the response time accordingly.

The analog current monitor should be set so that at the maximum processor current ($I_{CC(max)}$) the IMON voltage should be 1.7 V. This setting corresponds to a digital output current value of 'FF' in the telemetry register 03H through I2C. For any other IMON voltage output in the range of 0 to 1.7 V, the digital output varies linearly.

7.3.13 Fault Behavior

TPS59632-Q1 device has a complete suite of fault detection and protection functions, including input under-voltage lockout on all power inputs, over voltage and over current limiting, and output under voltage detection. The protection limits are given in the tables above. The converter suspends switching when the limits are exceeded and PGOOD goes low. In this state, the fault register 14h can be read. To exit fault protection mode, the bias power (V5A, VDD and VINTF) must be cycled as described in Section 7.3.9.

7.3.14 Output Under Voltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the Section 7.3.16 section. If V_{OUT} drops below the low PGOOD voltage threshold, then the PWM is tri-stated. The device stays off until the V5A, VDD or VINTF power is cycled and EN goes high.

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7.3.15 Output Over Voltage Protection (OVP)

An OVP condition is detected when the output voltage is greater than the PGDH voltage, and greater than VDAC. V_{OUT} > + V_{PGDH} greater than VDAC. In this case, the controller device sets PGOOD inactive, and keeps all the PWM signals low so as to keep the low-side driver ON at the converter. The converter remains in this state until the controller device is reset by cycling V5A, VDD or VINTF. This is the first level of OVP. This first level of OVP is inactive during VID transitions. There is a second OVP level fixed at V_{OVPH} which is always active. If the fixed OVP condition is detected, the PGOOD is forced inactive and the PWM signals are kept low and the operation is similar to the first level of OVP detection

7.3.16 Over Current Protection (OCP)

The TPS59632-Q1 device uses a inductor valley current limiting scheme, so the ripple current must be considered. The DC current value at OCP is the OCP limit value plus half of the ripple current. Current limiting occurs on a phase-by-phase and pulse-by-pulse basis. Generally, the current is sensed using the sense resistor in series with the inductor for automotive applications giving a voltage between the CSPx and CSNx pins. If this sensed voltage is above the OCP limit, the converter delays the next ON pulse until that voltage difference drops below the OCP limit.

In OCP mode, the voltage drops until the UVP limit is reached. When UVP limit is reached the operation follows as described in the Section 7.3.14.

7.3.17 Over Current Warning

I^2C programming enables this function. The TPS59632-Q1 device pulls down the voltage on the PGOOD pin whenever the valley current reaches 70% of the OCP value (or higher). PGOOD resumes normal function when the value falls below 65% of the OCP value.

7.3.18 Input Voltage Limits

The minimum input voltage is limited by the number of input phases, the switching frequency and the output voltage. The minimum input voltage increases with required maximum output voltage and switching frequency. See Table 7-1 for limits in 3-phase operating mode and Table 7-2 for limits in 2-phase operating mode . In 1-phase mode, the operation is limited by controller's capability to 2.5 V for all output voltages and switching frequency.

Table 7-1. Minimum Input Voltage ($V_{IN, MIN}$) Limits Versus Switching Frequency (F_{SW}) and Maximum Output Voltage ($V_{OUT, MAX}$) in 3-phase operation

$V_{OUT,MAX}$ (V)	F_{SW} (kHz)	$V_{IN, MIN}$ (V)
0.8	800	3.6
	1000	4.0
0.9	800	4.0
	1000	4.5
1.0	800	4.5
	1000	5.0

Table 7-2. Minimum Input Voltage ($V_{IN, MIN}$) Limits Versus Switching Frequency (F_{SW}) and Maximum Output Voltage ($V_{OUT, MAX}$) in 2-phase operation

$V_{OUT,MAX}$ (V)	F_{SW} (kHz)	$V_{IN, MIN}$ (V)
0.8	1000	2.5
0.9	1000	2.5
1.0	1000	2.8

7.3.19 VID Table

The Table 7-3 shows the VID table for all the programmable DAC voltage levels.

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Table 7-3. TPS59632-Q1 VID Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	0	1	1	0	0	1	19	0.5000
0	0	1	1	0	1	0	1A	0.5100
0	0	1	1	0	1	1	1B	0.5200
0	0	1	1	1	0	0	1C	0.5300
0	0	1	1	1	0	1	1D	0.5400
0	0	1	1	1	1	0	1E	0.5500
0	0	1	1	1	1	1	1F	0.5600
0	1	0	0	0	0	0	20	0.5700
0	1	0	0	0	0	1	21	0.5800
0	1	0	0	0	1	0	22	0.5900
0	1	0	0	0	1	1	23	0.6000
0	1	0	0	1	0	0	24	0.6100
0	1	0	0	1	0	1	25	0.6200
0	1	0	0	1	1	0	26	0.6300
0	1	0	0	1	1	1	27	0.6400
0	1	0	1	0	0	0	28	0.6500
0	1	0	1	0	0	1	29	0.6600
0	1	0	1	0	1	0	2A	0.6700
0	1	0	1	0	1	1	2B	0.6800
0	1	0	1	1	0	0	2C	0.6900
0	1	0	1	1	0	1	2D	0.7000
0	1	0	1	1	1	0	2E	0.7100
0	1	0	1	1	1	1	2F	0.7200
0	1	1	0	0	0	0	30	0.7300
0	1	1	0	0	0	1	31	0.7400
0	1	1	0	0	1	0	32	0.7500
0	1	1	0	0	1	1	33	0.7600
0	1	1	0	1	0	0	34	0.7700
0	1	1	0	1	0	1	35	0.7800
0	1	1	0	1	1	0	36	0.7900
0	1	1	0	1	1	1	37	0.8000
0	1	1	1	0	0	0	38	0.8100
0	1	1	1	0	0	1	39	0.8200
0	1	1	1	0	1	0	3A	0.8300
0	1	1	1	0	1	1	3B	0.8400
0	1	1	1	1	0	0	3C	0.8500
0	1	1	1	1	0	1	3D	0.8600
0	1	1	1	1	1	0	3E	0.8700
0	1	1	1	1	1	1	3F	0.8800
1	0	0	0	0	0	0	40	0.8900
1	0	0	0	0	0	1	41	0.9000
1	0	0	0	0	1	0	42	0.9100
1	0	0	0	0	1	1	43	0.9200
1	0	0	0	1	0	0	44	0.9300
1	0	0	0	1	0	1	45	0.9400

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Table 7-3. TPS59632-Q1 VID Table (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
1	0	0	0	1	1	0	46	0.9500
1	0	0	0	1	1	1	47	0.9600
1	0	0	1	0	0	0	48	0.9700
1	0	0	1	0	0	1	49	0.9800
1	0	0	1	0	1	0	4A	0.9900
1	0	0	1	0	1	1	4B	1.0000
1	0	0	1	1	0	0	4C	1.0100
1	0	0	1	1	0	1	4D	1.0200
1	0	0	1	1	1	0	4E	1.0300
1	0	0	1	1	1	1	4F	1.0400
1	0	1	0	0	0	0	50	1.0500
1	0	1	0	0	0	1	51	1.0600
1	0	1	0	0	1	0	52	1.0700
1	0	1	0	0	1	1	53	1.0800
1	0	1	0	1	0	0	54	1.0900
1	0	1	0	1	0	1	55	1.1000
1	0	1	0	1	1	0	56	1.1100
1	0	1	0	1	1	1	57	1.1200
1	0	1	1	0	0	0	58	1.1300
1	0	1	1	0	0	1	59	1.1400
1	0	1	1	0	1	0	5A	1.1500
1	0	1	1	0	1	1	5B	1.1600
1	0	1	1	1	0	0	5C	1.1700
1	0	1	1	1	0	1	5D	1.1800
1	0	1	1	1	1	0	5E	1.1900
1	0	1	1	1	1	1	5F	1.2000
1	1	0	0	0	0	0	60	1.2100
1	1	0	0	0	0	1	61	1.2200
1	1	0	0	0	1	0	62	1.2300
1	1	0	0	0	1	1	63	1.2400
1	1	0	0	1	0	0	64	1.2500
1	1	0	0	1	0	1	65	1.2600
1	1	0	0	1	1	0	66	1.2700
1	1	0	0	1	1	1	67	1.2800
1	1	0	1	0	0	0	68	1.2900
1	1	0	1	0	0	1	69	1.3000
1	1	0	1	0	1	0	6A	1.3100
1	1	0	1	0	1	1	6B	1.3200
1	1	0	1	1	0	0	6C	1.3300
1	1	0	1	1	0	1	6D	1.3400
1	1	0	1	1	1	0	6E	1.3500
1	1	0	1	1	1	1	6F	1.3600
1	1	1	0	0	0	0	70	1.3700
1	1	1	0	0	0	1	71	1.3800
1	1	1	0	0	1	0	72	1.3900

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Table 7-3. TPS59632-Q1 VID Table (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
1	1	1	0	0	1	1	73	1.4000
1	1	1	0	1	0	0	74	1.4100
1	1	1	0	1	0	1	75	1.4200
1	1	1	0	1	1	0	76	1.4300
1	1	1	0	1	1	1	77	1.4400
1	1	1	1	0	0	0	78	1.4500
1	1	1	1	0	0	1	79	1.4600
1	1	1	1	0	1	0	7A	1.4700
1	1	1	1	0	1	1	7B	1.4800
1	1	1	1	1	0	0	7C	1.4900
1	1	1	1	1	0	1	7D	1.5000
1	1	1	1	1	1	0	7E	1.5100
1	1	1	1	1	1	1	7F	1.5200

7.4 User Selections

After the V5A, VDD, and VINTF voltages are applied to the controller and all these voltage levels are above their respective UVLO levels, the following information is latched and cannot be changed during operation. The defines the values of the selections.

- **Operating Frequency.** The resistor from FREQ-P pin to GND sets the switching frequency. See the Section 8.2.1.2 for the resistor settings corresponding to each frequency selection. Note that the operating frequency is a quasi-fixed frequency in the sense that the ON time is fixed based on the input voltage (at the VBAT pin) and output voltage (set by VID). The OFF time varies based on various factors such as load and power-stage components.
- **Overcurrent Protection (OCP) Level.** The resistor from OCP-I to GND sets the OCP level of the CPU channel. See the Section 8.2.1.2 for the resistor settings corresponding to each OCP level.
- **IMON Gain.** The resistors from IMON to OCP-I and OCP-I to GND set the DC load current monitor (IMON) gain.
- **Slew Rate.** The SetVID fast slew rate is set by the resistor from SLEWA pin to GND. See the Section 8.2.1.2 for the resistor settings corresponding to each slew rate setting.
- **Base Address.** The voltage on SLEWA pin sets the device base address.
- **Ramp Selection.** The resistor from RAMP to GND sets the ramp compensation level. See the Section 8.2.1.2 for the resistor settings corresponding to each ramp level.
- **Overshoot Reduction (OSR) Level.** The resistor from O-USR to GND sets the OSR level. Section 8.2.1.2 provides all the possible selections for OSR.
- **Undershoot Reduction Level (USR)** The voltage on O-USR pin sets the USR level. Section 8.2.1.2 provides all the possible selections for USR.
- **Active Phases.** Normally, the controller is configured to operate in 3-phase mode. To enable 2-phase mode, tie the CSP3 pin to a 3.3-V supply and the CSN3 pin to GND. To enable 1-phase mode, tie the CSP2 and CSP3 pins to a 3.3-V supply and tie the CSN2 and CSN3 pins to GND.

7.5 I²C Interface Operation

The TPS59632-Q1 device includes a slave I²C interface accessed via the SCL (serial clock) and SDA (serial data) pins. The interface sets the base VID value, receives IMON telemetry, and controls functions described in this section. It operates with EN = low, with the bias supplies in regulation. It is compliant with I²C specification UM10204, Revision 3.0; characteristics are detailed as following:

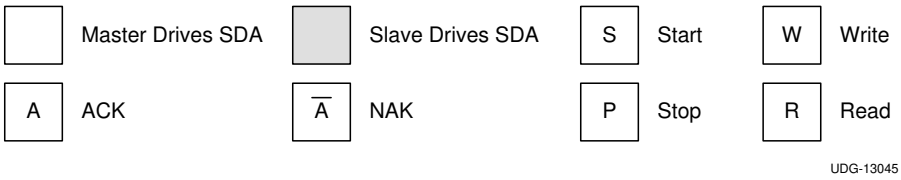
- Addressing
  - 7-bit addressing; address range is 100 0xxx (binary)
  - Last three bits are determined by the voltage on SLEWA pin at start-up
- Byte read and byte write protocols only (see the following figures)

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- Frequency
  - 100 kHz
  - 400 kHz
  - 1 MHz
  - 3.4 MHz
- Logic inputs are 1.8-V logic levels (3.3-V tolerant)

The TPS59632-Q1 device can be configured for eight different device addresses by setting a voltage on the SLEWA pin. Configure a resistor divider on SLEWA from VREF to GND. Once the slew rate resistor is selected, the resistor from the VREF pin to the SLEWA pin can be chosen based on the required device address. For a device address of 40h, the VREF to SLEWA resistor can be left open.

7.5.1 Key For Protocol Examples



7.5.2 Protocol Examples

The good byte read transaction the controller ACKs and the master terminates with a NAK/stop

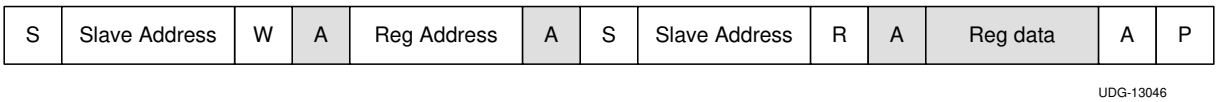


Figure 7-9. Good Byte Read Transaction

The controller NAKs a read with an invalid register address.

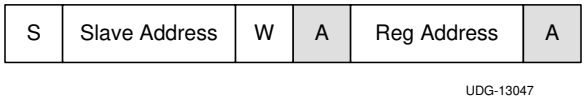


Figure 7-10. NAK Invalid Register Address

A good byte write is illustrated in Figure 7-11.

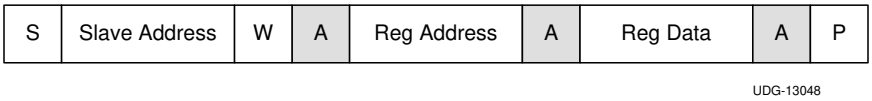


Figure 7-11. Good Byte Write

The controller NAKs a write with an invalid register address.

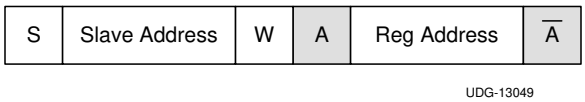


Figure 7-12. Invalid NAK Register Address

The controller will NAK a write for the condition of invalid data.

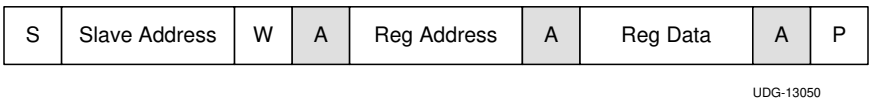


Figure 7-13. Invalid NAK Register Data

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7.6 I²C Register Maps

The I²C interface shall support 400 kHz, 1 MHz, and 3.4-MHz clock frequencies. The I²C interface shall be accessible even when EN is low. The following registers are accessible via I²C.

7.6.1 Voltage Select Register (VSR) (Address = 00h)

- Type: read and write
- Power-up value: BOOT[6:0]
- EN rising (after power-up): prior programmed value
- See Table 7-3 for exact values
- A command to set VSR < 19h (minimum VID) generates an NAK and the VBR remains at the prior value

b7	b6	b5	b4	b3	b2	b1	b0
—	VID6	—	—	—	—	—	VID0

7.6.2 IMON Register (Address = 03h)

- Type: read only
- Power-up value: 00h
- EN rising (after power-up):00h

b7	b6	b5	b4	b3	b2	b1	b0
MSB	—	—	—	—	—	—	LSB

7.6.3 VMAX Register (Address = 04h)

- Type: read or write (see the following bit definitions)
- Power-up value: 7Fh
- EN rising (after power-up): last written value

b7	b6	b5	b4	b3	b2	b1	b0
Lock	MSB	—	—	—	—	—	LSB

Bit definitions:

BIT	NAME	DEFINITION
0 - 6	VMAX	Maximum VID setting
7	Lock	Access protection of the VMAX register 0: No protection, R/W access to bits 0-6 1: Access is read only; reset after UVLO event.

7.6.4 Power State Register (Address = 06h)

- Type: read and write
- Power-up value: 00h
- EN rising (after power-up): 00h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	MSB	LSB

Bit definitions:

VALUE	DEFINITION
b1 = 0, b0 = 0	Multi-phase CCM
b1 = 0, b0 = 1	Single-phase CCM

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VALUE	DEFINITION
b1 = 1, b0 = 0	Single-phase DCM

7.6.5 Slew Register (Address = 07h)

- Type: read and write (see below)
- Power-up value: defined by SLEWA pin at power-up
- EN rising (after power-up): last written value
- Write only a single 1 for the minimum SLEW rate desired for voltage changes. The start-up slew rate is half of the normal voltage change slew rate.

b7	b6	b5	b4	b3	b2	b1	b0
48 mV/µs	42 mV/µs	36 mV/µs	30 mV/µs	24 mV/µs	18 mV/µs	12 mV/µs	6 mV/µs

7.6.6 Lot Code Registers (Address = 10-13h)

- Type: 8 bits, read only
- Power-up value: programmed at factory

7.6.7 Fault Register (Address = 14h)

- Type: 8 bits; read only
- Power-up value: 00h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	Device thermal shutdown	OVP	UVP	OCP

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8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS59632Q1 device has a very simple design procedure. A Microsoft Excel®-based component value calculation tool is available. Please contact your local TI representative to get a copy of the spreadsheet.

8.2 Typical Application

8.2.1 3-Phase D-CAP+™, Step-Down Application

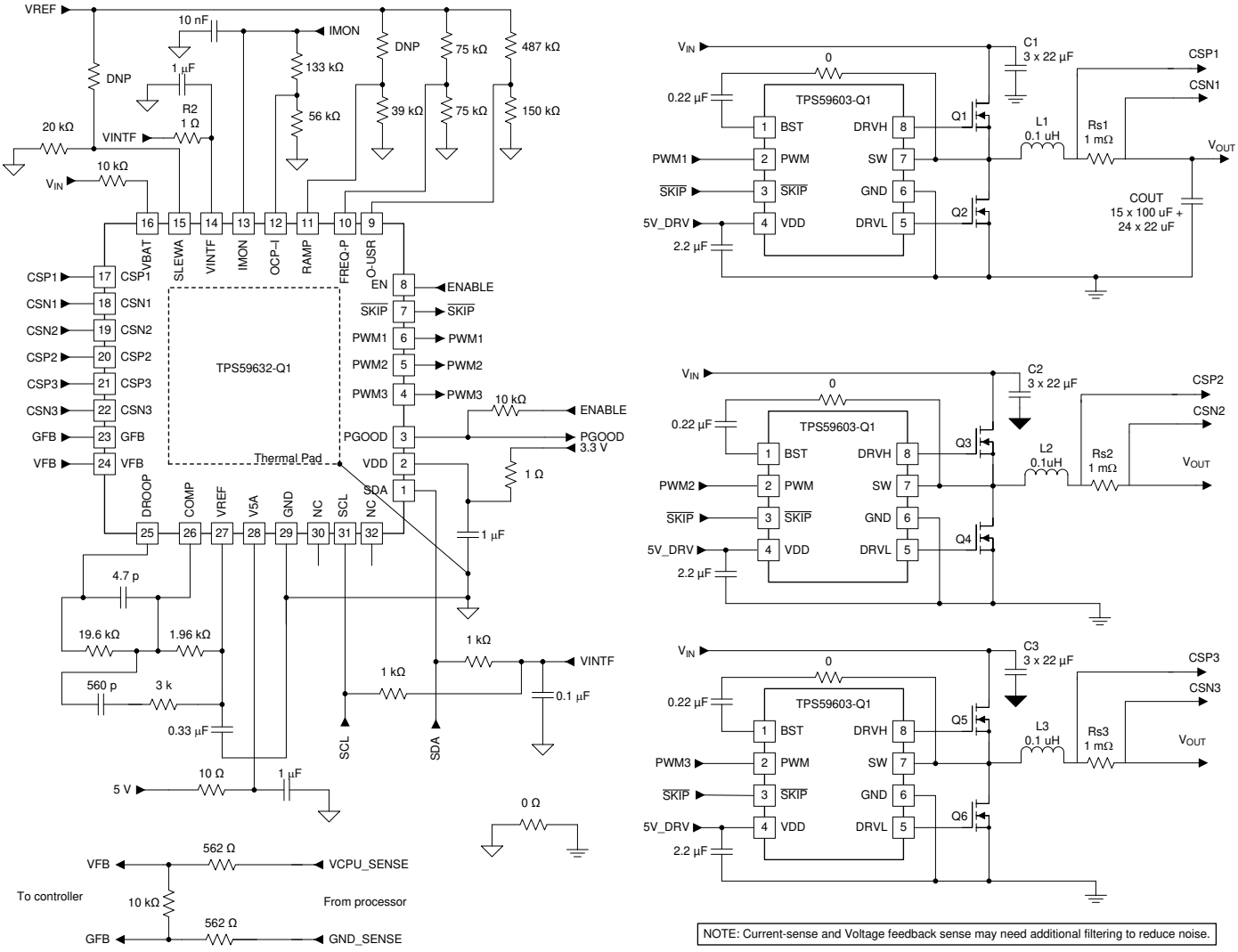


Figure 8-1. 3-Phase D-CAP+™, Step-Down Application with Power Stages

8.2.1.1 Design Requirements

Design example specifications:

- Number of phases, N_{ph}: 3
- Conversion Input voltage, V_{IN} range: 5 V +/- 10%
- Converter Output Voltage V_{OUT} = 0.875 +/- 3% V (including DC and AC)
- Load Current, $I_{CC(max)}$ = 50 A
- Voltage Rise time (at start-up) > 100µs
- Load Transient step = 36A
- Load Transient Slew rate = 36A/µs
- Effective Switching Frequency > 2.0 MHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Step 1: Select Switching Frequency

The switching frequency is selected by a resistor (R_F) between the FREQ_P pin and GND. The frequency is approximate and expected to vary based on load and input voltage.

Table 8-1. TPS59632-Q1 Device Frequency Selection Table

SELECTION RESISTOR (R_F) VALUE (kΩ)	OPERATING FREQUENCY (f_{SW}) (kHz)
20	300
24	400
30	500
39	600
56	700
75	800
100	900
150	1000

For this design, choose a switching frequency of 800 kHz so that the effective switching frequency in 3-phase operation = 2.4 MHz. So, R_F = 75 kΩ.

Note

The voltage on the FREQ-P pin MUST be set higher than 0.7V for proper operation of the device, TPS59632Q1. This can easily be achieved by connecting a resistor of the same value as $R_F$from FREQ-P to VREF (1.7 V).

As per the note above, in this design, a resistor of value 75 kΩ is connected from FREQ-P to VREF.

8.2.1.2.2 Step 2: Set The Slew Rate

A resistor to GND (R_{SLEWA}) on SLEWA pin sets the slew rate. For a minimum start-up time of 100 µs, the maximum allowed slew rate would be VOUT/100 µs. This would mean a maximum start-up slew rate of 8.8 mV/µs. Hence, from Table 8-2 the maximum start-up slew rate setting of 5mV/µs is chosen. It should be noted that the slew rate corresponding to start-up rate is half of the slew rate during voltage changes due to VID changes as specified in the EC table. The table below provides the minimum and maximum start-up slew rate for each resistor selection. The resistor selection chosen for this design is R_{SLEWA} = 20 kΩ.

Table 8-2. Slew Rate Versus Selection Resistor

SELECTION RESISTOR R_{SLEWA} (kΩ)	MINIMUM START-UP SLEW RATE (mV/µs)	MAXIMUM START-UP SLEW RATE (mV/µs)
20	3	5

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Table 8-2. Slew Rate Versus Selection Resistor (continued)

SELECTION RESISTOR R_{SLEWA} (kΩ)	MINIMUM START-UP SLEW RATE (mV/µs)	MAXIMUM START-UP SLEW RATE (mV/µs)
24	6	10
30	9	15
39	12	20

8.2.1.2.3 Step 3: Set The I²C Address

The voltage on the SLEWA pin also sets the I²C address for the device. For an I2C address of 40, the SLEWA pin should only have a resistor, RSLEW to GND and the SLEW pin to VREF pin should be left open. For other I²C addresses, a resistor must be connected between the SLEWA pin and the VREF pin (1.7 V). This resistor can be calculated to set the corresponding voltage for the required address listed in Table 8-3.

Table 8-3. I²C Address Selection

SLEWA VOLTAGE	I²C ADDRESS
$V_{SLEWA} \le 0.30$ V	0
$0.35\text{ V} \le V_{SLEWA} \le 0.45$ V	1
$0.55\text{ V} \le V_{SLEWA} \le 0.65$ V	2
$0.75\text{ V} \le V_{SLEWA} \le 0.85$ V	3
$0.95\text{ V} \le V_{SLEWA} \le 1.05$ V	4
$1.15\text{ V} \le V_{SLEWA} \le 1.25$ V	5
$1.35\text{ V} \le V_{SLEWA} \le 1.45$ V	6
$1.55\text{ V} \le V_{SLEWA} \le 1.65$ V	7

8.2.1.2.4 Step 4: Determine Inductor Value And Choose Inductor

Applications with smaller inductor values have better transient performance but also have higher voltage ripple and lower efficiency. Applications with higher inductor values have the opposite characteristics. Choice of inductance is a trade off between transient, ripple, size, efficiency, cost and availability.

For this design, we chose an inductance value of 0.1 µH. The chosen inductor should have the following characteristics:

- As flat as an inductance versus current curve as possible.
- Either high saturation or soft saturation. A saturation current of at least the per phase maximum current of $I_{CC(max)} / N_{ph} + I_{ripple}/2$
- Low DCR for high efficiency.

8.2.1.2.5 Step 5: Current Sensing Resistance

The TPS59632 device supports both resistor sensing and inductor DCR sensing. However, inductor DCR sensing is not suitable for automotive applications due to wide variation in current sensing across temperature. The sense resistance, R_S must be chosen large enough to give sufficient current signal to the controller and small enough to keep the power dissipation low. Choosing max power dissipation to about 0.5W per phase, we get R_S = 1 mΩ.

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8.2.1.2.6 Step 6: Select Over Current Protection (OCP) Setting

The OCP level is chosen such that it is 30% above the maximum load current, $I_{CC(max)}$. In the equation, here R_{CS} is the current sense resistor.Equation 4. I_{VALLEY} is the load current less half the ripple.

$$I_{VALLEY} \times R_{CS(eff)} = V_{CS(ocp)} \tag{4}$$

Set the OCP threshold level just greater than the calculated I_{VALLEY} for the required OCP level. Equation 4. In this design, the minimum required OCP is 65A. Therefore, an OCP selection resistor of 56k is chosen to meet the requirement.

Table 8-4 shows the minimum OCP level for all the selection resistors.

Table 8-4. OCP Selection(1)

SELECTION RESISTOR R_{OCP} (kΩ)	Minimum $V_{CS(OCP)}$ (mV)
20	3
24	7
30	11
39	15
56	21
75	28
100	36
150	45

(1) If a corresponding match is not found, then select the next higher setting.

8.2.1.2.7 Step 7: Current Monitor (IMON) Setting

Set the analog current monitor so that at $I_{CC(max)}$ the IMON pin voltage is 1.7 V. This corresponds to a digital I_{OUT} value of 'FF' in I^2C register 03H. The voltage on the IMON pin is shown in Equation 5.

$$1.7 = 10 \times \left(1 + \frac{R_{IMON}}{R_{OCP}}\right) \times R_{CS(eff)} \times I_{CC(max)} \tag{5}$$

where, $I_{CC(max)}$is 50 A; $R_{CS(eff)}$ is 1.0 mΩ and R_{OCP} is 56 kΩ

Solving, R_{IMON} = 133 kΩ. R_{IMON} is connected from IMON pin to OCP-I pin.

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8.2.1.2.8 Step 8: Set the Load-Line Slope

Setting a load line slope is effective in significantly reducing the output capacitors. Therefore, although the design requirement does not call for a load-line, we use the output voltage tolerance specification to determine an appropriate load-line. Figure 8-2 shows how we first determine the load-line window.

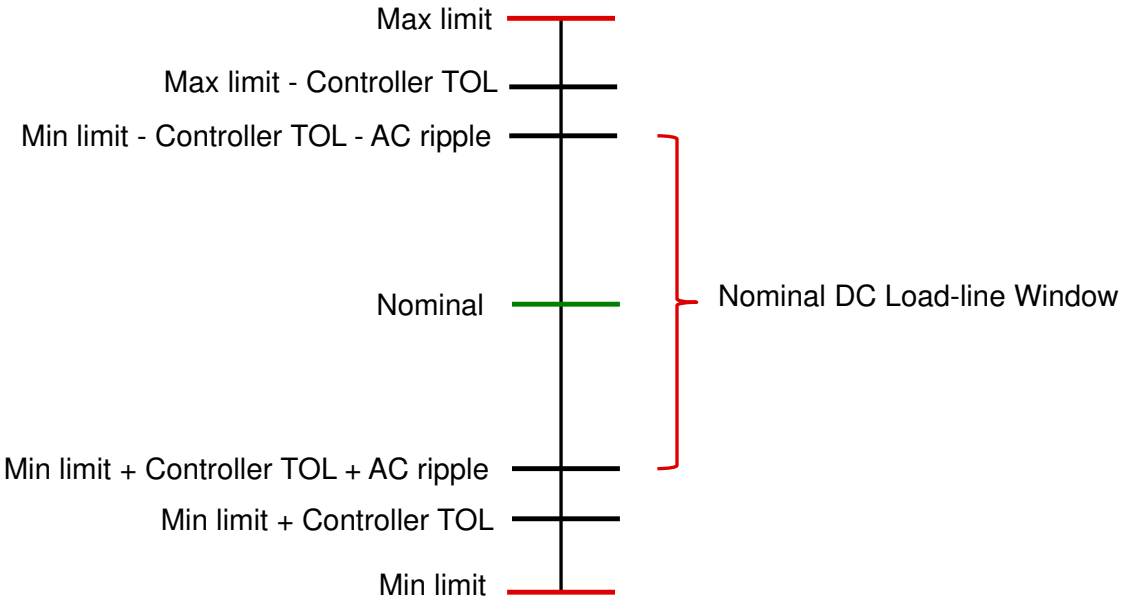


Figure 8-2. Determination of Nominal DC Load-line window

This nominal DC load-line window is now used to set the load-line slope across the range of load current from 0 to $I_{cc,max}$ as shown in Figure 8-3.

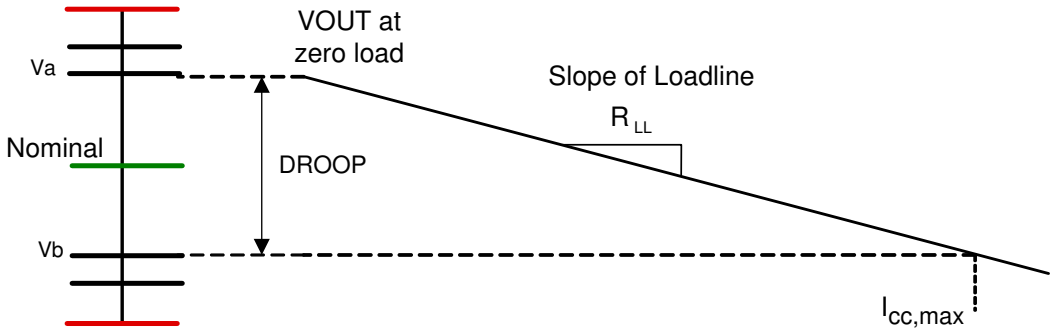


Figure 8-3. Determination of the Slope of the Load-line

The load-line slope R_{LL} is first determined as shown in Figure 8-3 using the equation in Equation 6. In the device, TPS59632-Q1, the load-line is determined by the current sense resistance, R_{CS}, the current sense amplifier gain, A_{CS}, and the gain of the droop amplifier (A_{DROOP}) as shown in Equation 7.

$$R_{LL} = \frac{Va - Vb}{I_{cc\,max}} \tag{6}$$

$$R_{LL} = \frac{R_{CS,eff} \times A_{CS}}{A_{DROOP}} \tag{7}$$

The gain of the droop amplifier, (A_{DROOP} can therefore be determined by Equation 7. This gain is set by the external resistors R_{DROOP} (between the DROOP pin and the COMP pin) and resistor R_{COMP} (between the COMP pin and the VREF pin) as shown in Equation 8. We fix the value of R_{DROOP} to 19.6 kΩ, and thereby R_{COMP} is calculated to 1.87 kΩ.

$$A_{DROOP} = \left(1 + \left(\frac{R_{DROOP}}{R_{COMP}}\right)\right) \tag{8}$$

8.2.1.2.9 Step 9: Voltage Feedback Resistor Calculation

In the device TPS59632-Q1, the internal DAC voltage is set to 0.80 V. To adjust the output voltage above or below this voltage we need to use feedback resistor divider setting. Since we are sensing the voltage using differential remote sense we adopt the circuit shown in Figure 8-4 to increase the voltage above 0.80 V and the and circuit shown in Figure 8-5 to decrease the voltage below 0.80 V.

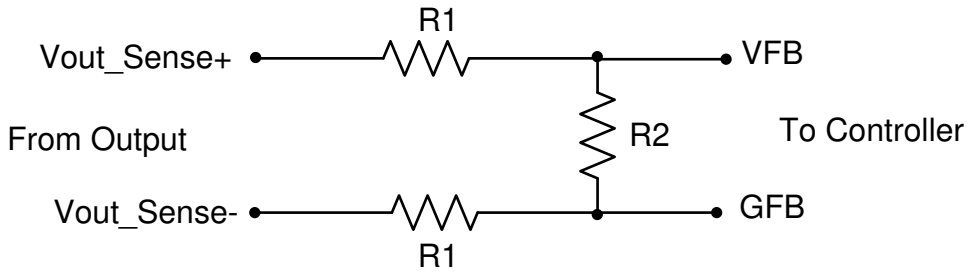


Figure 8-4. Feedback resistor divider circuit to increase the output voltage above internal DAC voltage

In this design, we need to calculate the feedback resistor values, R1 and R2, to increase the voltage above the DAC, the equation shown in Equation 9 is used. Here, V_{DAC} = 0.80 V, and Va from load-line setting is determined as 0.890 V. R2 is set to 10 kΩ and R1 is calculated to 562.

$$Va\frac{R2}{R2+2R1} = V_{DAC} \tag{9}$$

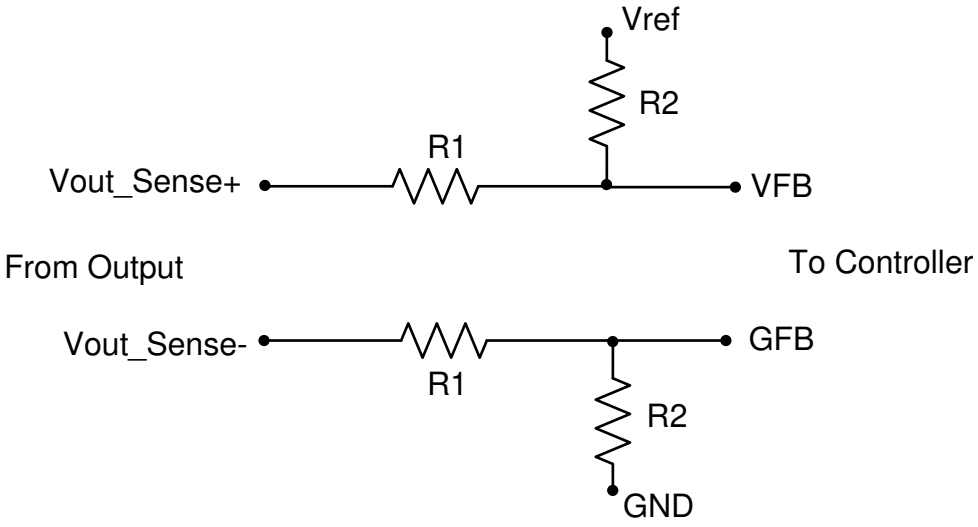


Figure 8-5. Feedback resistor divider circuit to decrease the output voltage above internal DAC voltage

To calculate the feedback resistor values, R1 and R2, to decrease the voltage below the DAC, the equation shown in Equation 10 is used. Here, V_{DAC} = 0.80 V, and Va from load-line setting for the specific application. Vref

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is the TPS59632-Q1 reference voltage at Pin 27 (VREF) which is nominally 1.7 V. Using this, and setting R2 to 10 kΩ, R1 can be determined.

$$\frac{Vref - VDAC}{R2} = \frac{VDAC - Va}{R1} \quad (10)$$

8.2.1.2.10 Step 10: Ramp Compensation Selection

The Ramp compensation is selected to minimize the jitter. Higher ramp gives lower jitter but can worsen the transient response. The ramp compensation selection is a trade off between transient response and jitter.

Table 8-5 shows the available ramp selections.

Table 8-5. Ramp Compensation Selection

SELECTION RESISTOR R_{RAMP} (kΩ)	RAMP COMPENSATION VOLTAGE (mV)
20	20
30	60
39	100
150	40

8.2.1.2.11 Step 11 Overshoot Reduction (OSR) selection

The OSR level selection is based on the load-transient performance and amount of actual output capacitance to get the best performance with least output capacitance. The suggested method is to begin with OSR OFF and perform the load transient test based on a calculated amount of output capacitance. If the overshoot is higher then specified voltage limits, the OSR can be enabled by lowering the OSR threshold level. If the overshoot is acceptable with OSR OFF, then e reduction in output capacitance can be made and then an appropriate OSR level can be selected to meet the load transient specification. While reducing the output capacitance, other considerations like output ripple, undershoot, stability, and so on needs to be considered simultaneously.

Table 8-6 shows the available OSR selections.

Table 8-6. OSR Selection

SELECTION RESISTOR R_{OSR} (kΩ)	OSR THRESHOLD LEVEL (mV)
20	100
24	150
30	200
39	250
56	300
75	400
100	500
150	OFF

8.2.1.2.12 Step 12: Undershoot Reduction (USR) selection

Once the the R_{OSR} value is fixed, then the USR level can be set by the voltage on the O-USR pin. The resistor R_{USR} (between the O-USR pin and the VREF pin) sets the voltage.

Table 8-7. USR Selection

LEVEL	V_{O-USR} SELECTION VOLTAGE (V)		V_{USR} UNDERSHOOT REDUCTION LEVEL (mV)
	MIN	MAX	
1		0.25	60

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Table 8-7. USR Selection (continued)

LEVEL	V_{O-USR} SELECTION VOLTAGE (V)		V_{USR} UNDERSHOOT REDUCTION LEVEL (mV)
	MIN	MAX	
2	0.35	0.45	90
3	0.55	0.65	120
4	0.75	0.85	180
5	0.95	1.05	240
6	1.15	1.25	420
7	1.35	1.45	480
8	1.55	V_{VREF}	540

The USR level is also selected similar to the OSR setting. First, begin with least undershoot reduction and lower the level until pulse-overlap between two phases happens sufficiently to meet the load insertion transient requirement. The USR level can be approximately estimated by multiplying one-third of the droop voltage for the specified load transient with the A_{DROOP} determined in Section 8.2.1.2.8. The actual level needs to be tuned based on measurement. In this design, OSR is set to OFF and USR is set to 90-mV level. Therefore R_{OSR} = 150k and R_{USR} = 487k.

8.2.1.2.13 Step 13: Loop Compensation

The controller device TPS59632-Q1 does not require any additional loop compensation for stability as the load-line setting droop amplifier gain automatically stabilizes the DCAP+ control loop. However, to further increase the response time to fast load transients, an additional resistor (3 kΩ) in series with a capacitor (560 pF) is placed from COMP to VREF. Frequency response is measured to ensure the stability while meeting the transient requirements. Some key results for this design are given in Section 8.2.1.3.

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8.2.1.3 Application Performance Plots

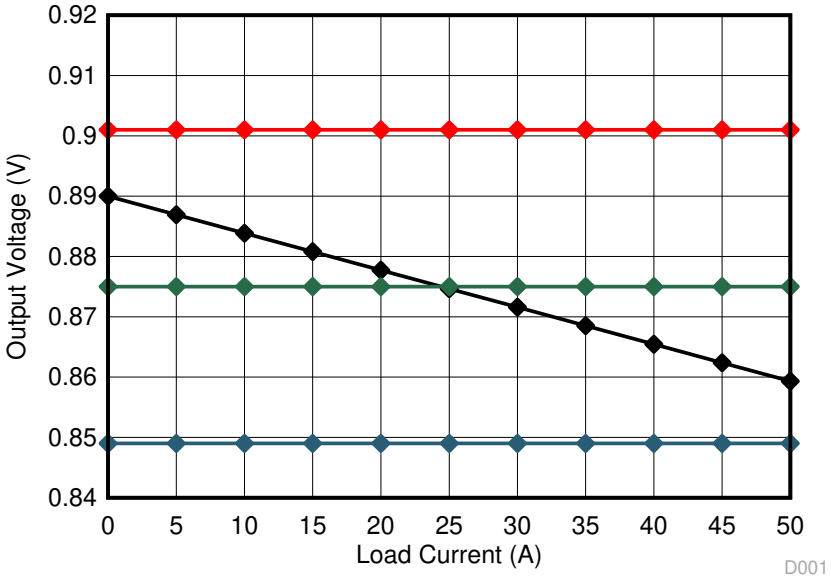


Figure 8-6. Output Voltage vs Output Current

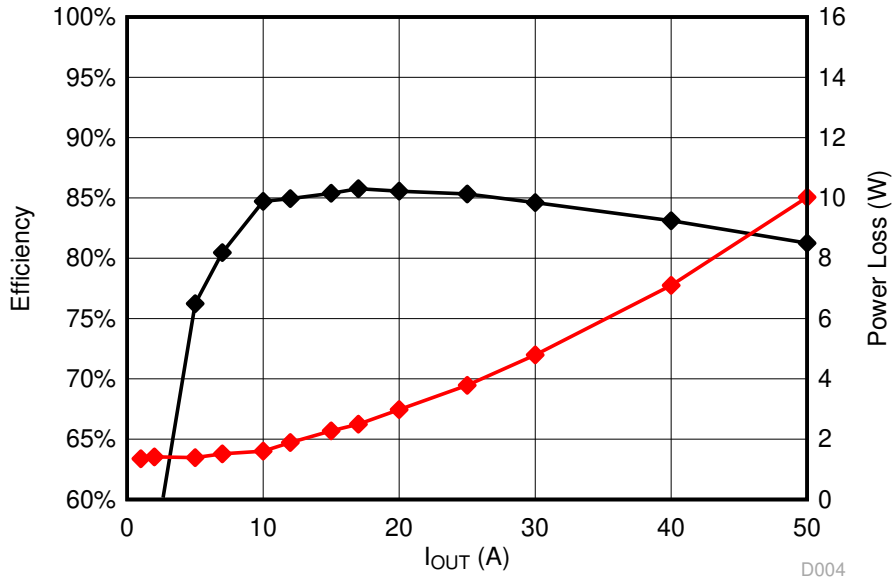


Figure 8-7. Efficiency and Power Loss Vs. Load Current

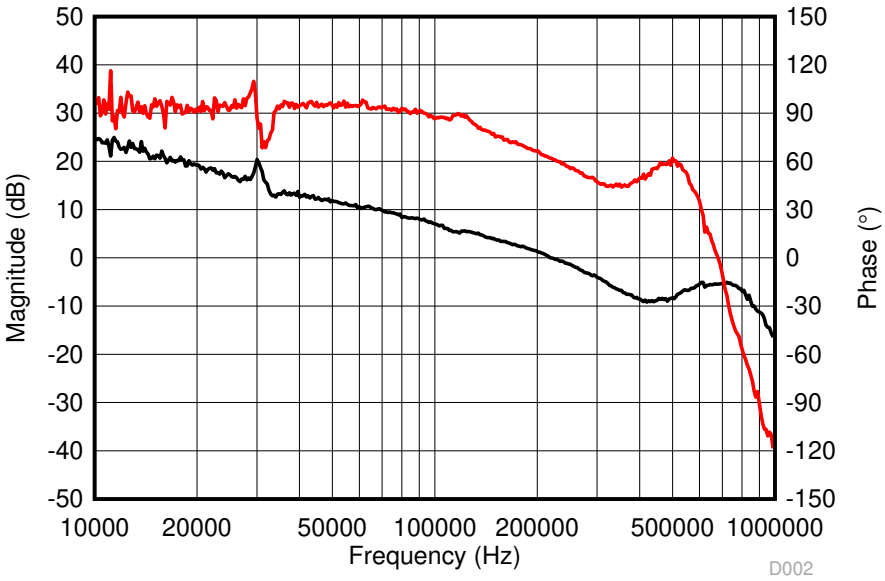


Figure 8-8. Control-loop Gain-Phase measurement Vs. frequency

9 Power Supply Recommendations

This device is designed to operate from a supply voltage at the V5A pin (5-V power input for analog circuits) from 4.5 V to 5.5 V and a supply voltage at the VDD pin (3.3-V digital power input) from 3.1 V to 3.5 V, and a supply voltage at VINTF from 1.7 V to 3.5 V. Use only a well-regulated supply. The VBAT input must be connected to the conversion input voltage and must not exceed 28 V. Proper bypassing of the V5A, VDD, and VINTF input supplies is critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the Section 10 section.

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10 Layout

10.1 Layout Guidelines

- Confirm the pinout of the controller on schematic against the pinout of the data sheet.
- Have a component value calculator tool ready to check component values.
- Carefully check the choice of inductor and sense resistor.
- Carefully check the choice of output capacitors.
- Because the voltage and current feedback signals are fully differential, double check their polarity.
  - CSP1 / CSN1
  - CSP2 / CSN2
  - CSP3 / CSN3
  - VOUT_SENSE to VFB / GND_SENSE to GFB
- Make sure the pull up on the SDA, SCL lines are correct. Check if there is a bypass capacitor close to the device on the pull up VINTF rail to GND of the device.
- TI strongly recommends that the device GND be separate from the system and Power GND.

Note

Make sure to separate noisy driver interface lines. This is a critical layout rule.

The driver (TPS59603-Q1) is outside of the device. All gate-drive and switch-node traces must be local to the inductor and MOSFETs.

10.2 Layout Example

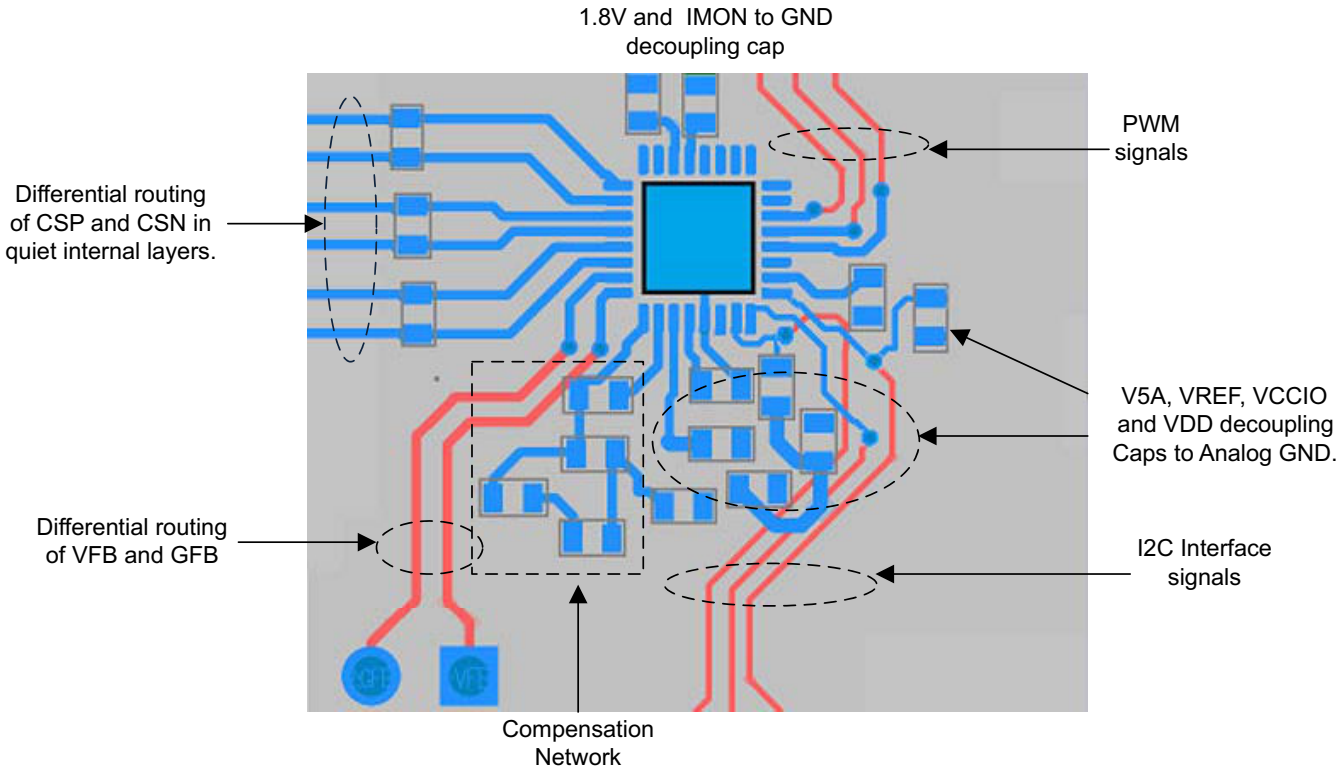


Figure 10-1. Example Layout

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10.3 Current Sensing Lines

Given the physical layout of most systems, the current feedback (CSPx and CSNx) may have to pass near the power chain. Clean current feedback is required for good load-line, current sharing, and current limiting performance of the TPS59632-Q1 device, so take the following precautions:

- Ensure all vias in the CSPx and CSNx traces are isolated from all other signals.
- TI recommends dotted signal traces be run in internal planes.
- If possible, change the name of the CSNx trace if possible to prevent automatic ties to the V_{CORE} plane.
- Run CSPx and CSNx as a differential pair in a quiet layer to the device.
- Isolate the lines from noisy signals by a voltage or ground plane.
- Make a Kelvin connection to the pads of the resistor used for current sensing.
- Place any noise filtering capacitors directly under or near the TPS59632-Q1 device and connect to the CS pins with the shortest trace length possible.

10.4 Feedback Voltage Sensing Lines

The voltage feedback coming from the CPU socket must be routed as a differential pair all the way to the VFB and GFB pins of the TPS59632-Q1 device. Care should be taken to avoid routing over switch-node and gate-drive traces.

10.5 PWM And $\overline{\text{SKIP}}$ Lines

The PWM and $\overline{\text{SKIP}}$ lines should be routed from the TPS59632-Q1 device to the MOSFET gate driver without crossing any switch-node or the gate drive signals.

10.6 Power Chain Symmetry

The TPS59632-Q1 device does not require special care in the layout of the power chain components because independent isolated current feedback is provided. Lay out the phases in a symmetrical manner, if possible. The rule is: the current feedback from each phase needs to be clean of noise and have the same effective current-sense resistance.

10.7 Component Location

Place components as close to the device in the following order:

1. CS pin noise filtering components
2. COMP pin and DROOP pin compensation components
3. Decoupling capacitors for VREF, VDD, V5A
4. Decoupling cap for VINTF rail, which is pullup voltage for the digital lines. This decoupling should be placed near the device to have good signal integrity.
5. OCP-I resistors, FREQ-P resistors, SLEWA resistors, RAMP resistors, and O-USR resistors

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10.8 Grounding Recommendations

The TPS59632-Q1 device has an analog ground and a thermal pad. The usual procedure for connecting these is:

- Keep the analog GND of the device and the power GND of the power circuit separate. The device analog GND and the power circuit power GND can be connected at one single quiet point in the layout.
- The thermal pad does not have an electrical connection to device. But, the thermal pad must be connected to pin 29 GND of the device to give good ground shielding. Do not connect this to system GND.
- Tie the thermal pad to a ground island with at least 4 vias. All the analog components can connect to this analog ground island.
- The analog ground can be connected to any quiet spot on the system ground. A quiet spot is defined as a spot where no power supply switching currents are likely to flow. Use a single point connection from analog ground to the system ground.
- Make sure the bottom FET source connection and the input decoupling capacitors have plenty of vias.

10.9 Decoupling Recommendations

- Decouple V5A and VDD to GND with a ceramic capacitor (with a value of at least 1 µF).
- Decouple VINTF to GND with a capacitor (with a value of at least 0.1 µF) to GND.

10.10 Conductor Widths

- Maximize the widths of power, ground, and drive signal connections.
- For conductors in the power path, be sure there is adequate trace width for the amount of current flowing through the traces.
- Make sure there are sufficient vias for connections between layers. Use 1 via minimum per ampere of current.

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11 Device and Documentation Support

11.1 Documentation Support

TPS59603-Q1 Synchronous Buck FET Driver for High-Frequency CPU Core Power in Automotive Applications data sheet.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS59632QRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TPS 59632
TPS59632QRHBRQ1.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 59632
TPS59632QRHBTQ1	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TPS 59632
TPS59632QRHBTQ1.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 59632

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

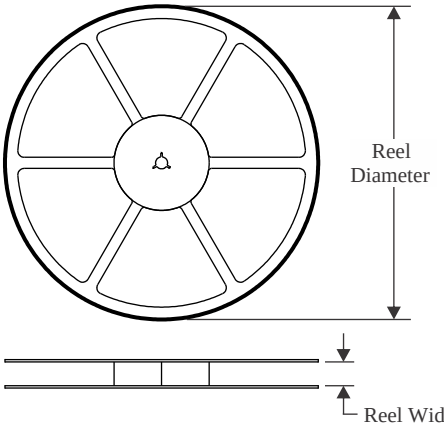
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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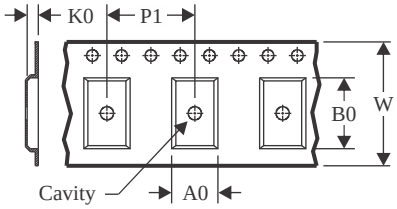
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

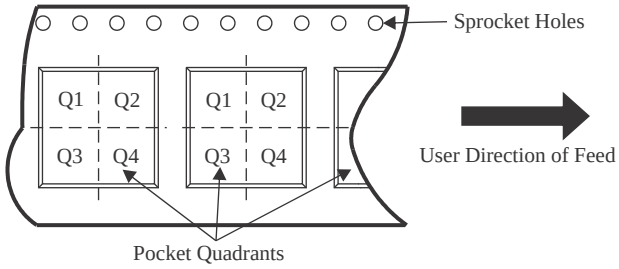


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

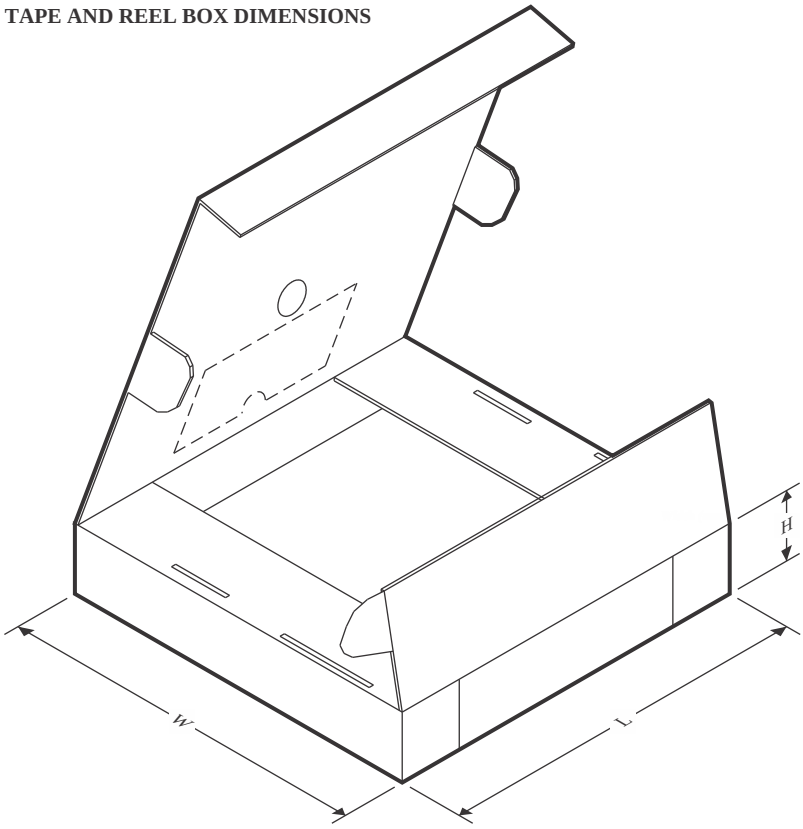
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS59632QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS59632QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS59632QRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS59632QRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS59632QRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS59632QRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	38.0
TPS59632QRHBTQ1	VQFN	RHB	32	250	213.0	191.0	35.0
TPS59632QRHBTQ1	VQFN	RHB	32	250	210.0	185.0	35.0

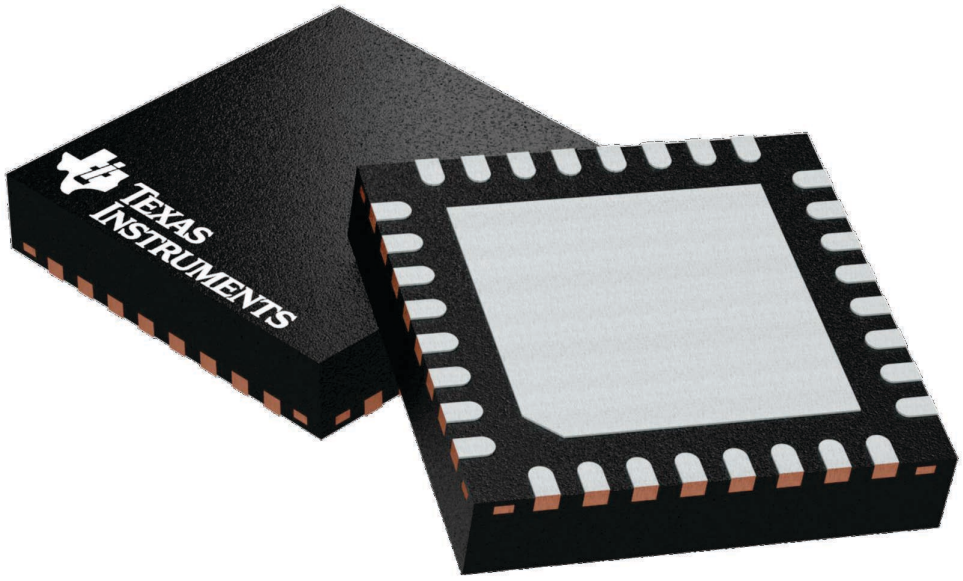
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

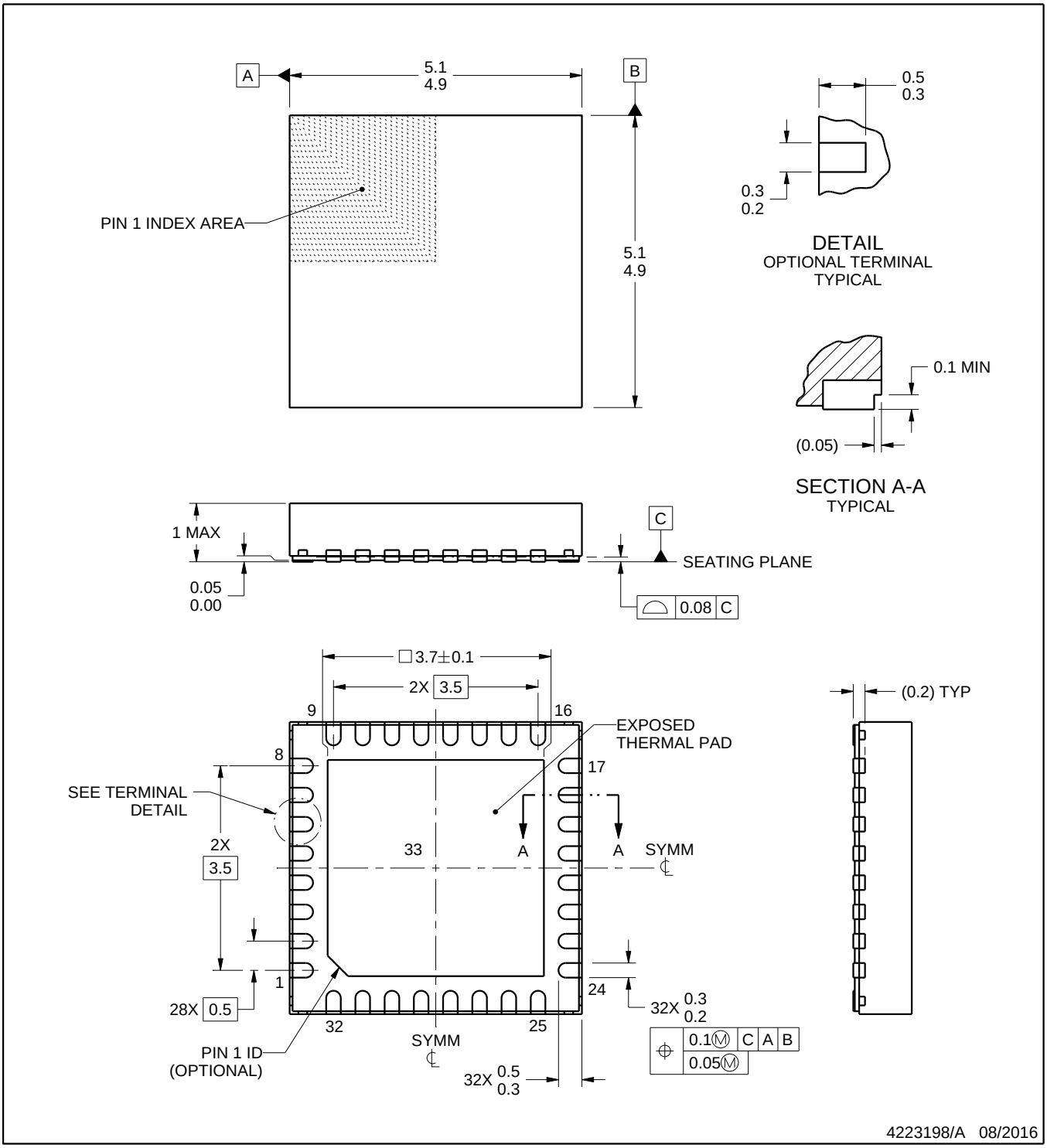
4224745/A

PACKAGE OUTLINE

RHB0032P

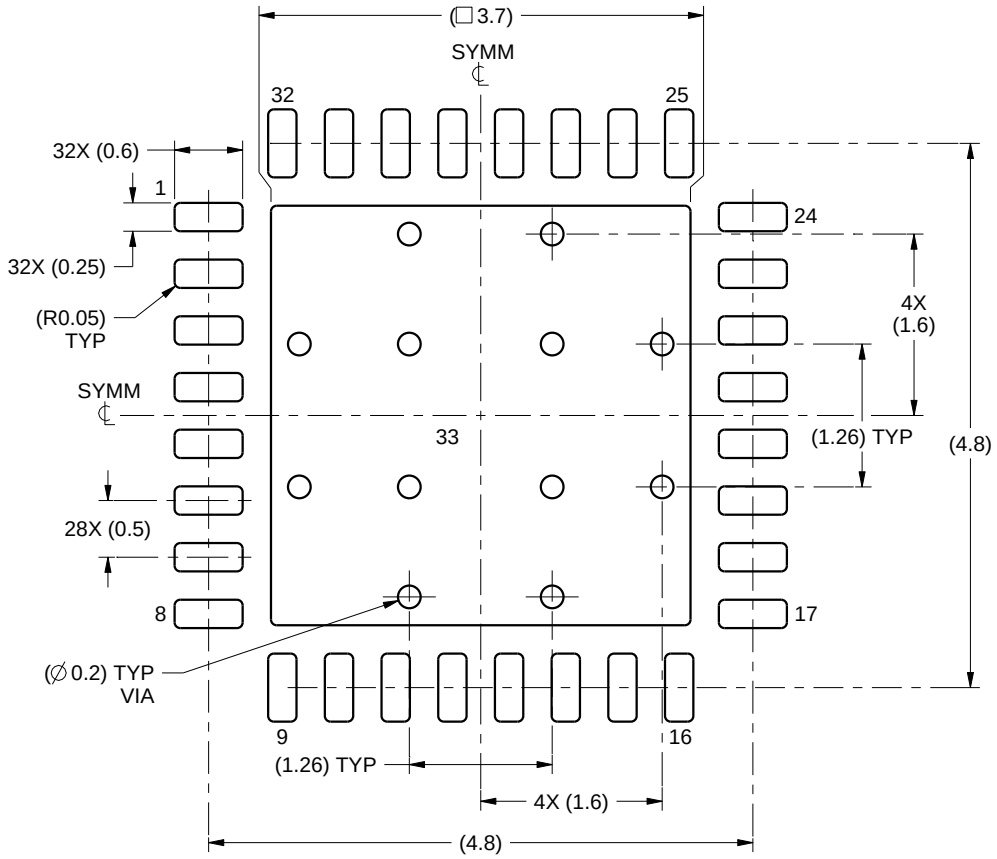
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

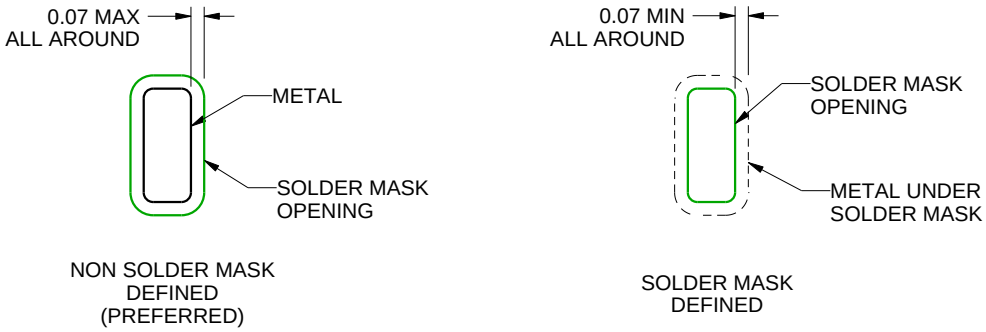


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

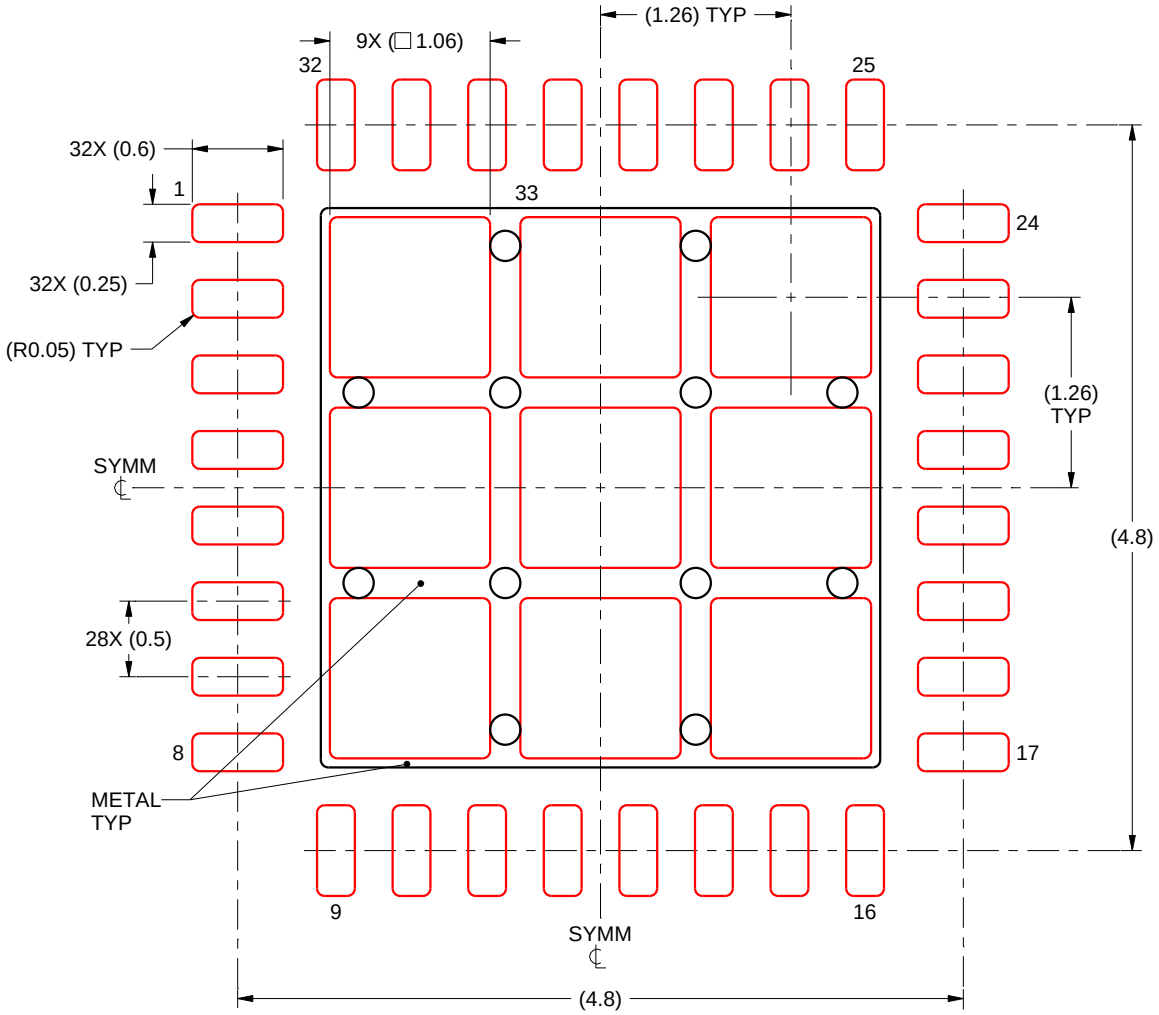


SOLDER MASK DETAILS

4223198/A 08/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223198/A 08/2016

NOTES: (continued)

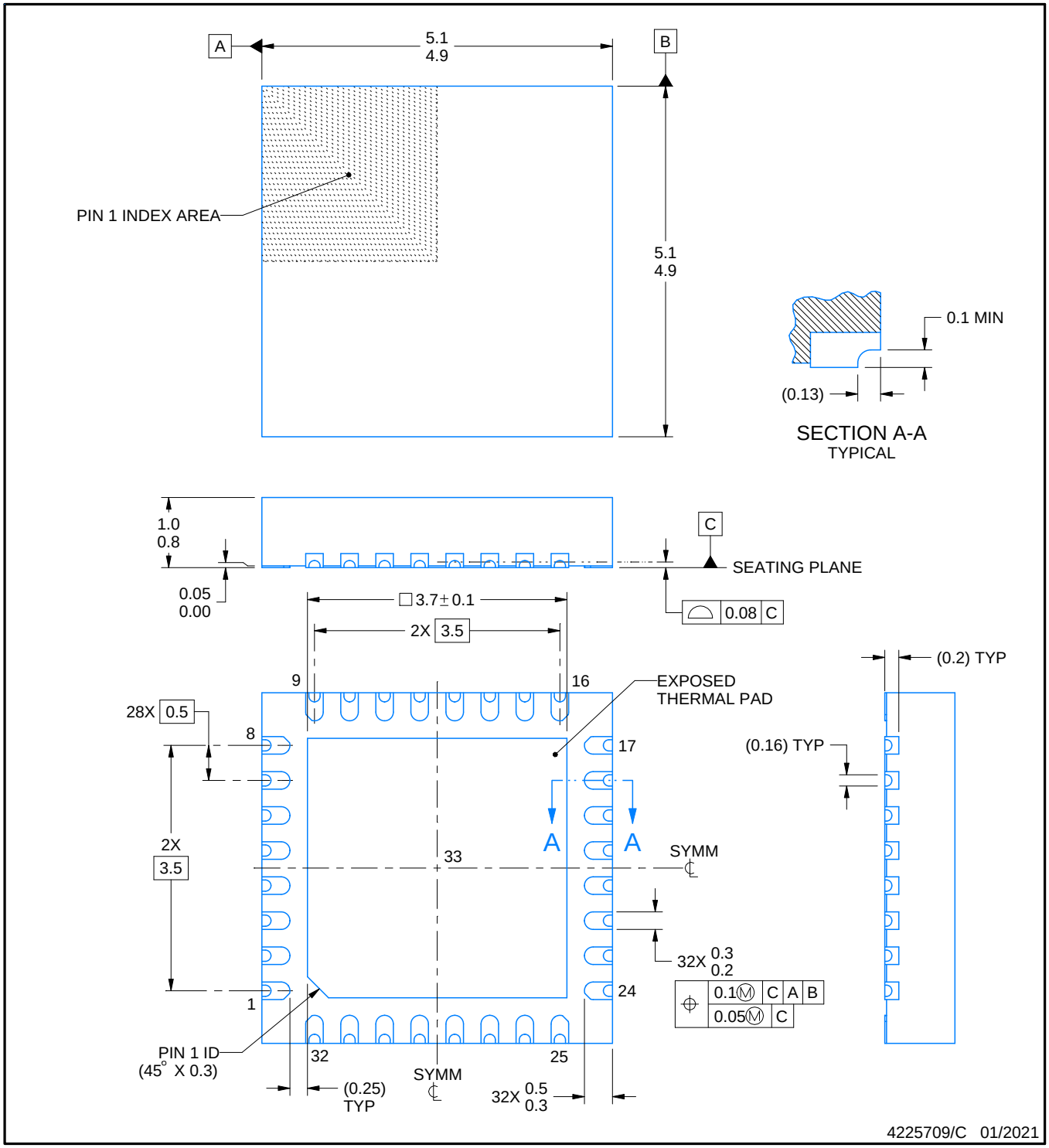
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RHB0032U

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

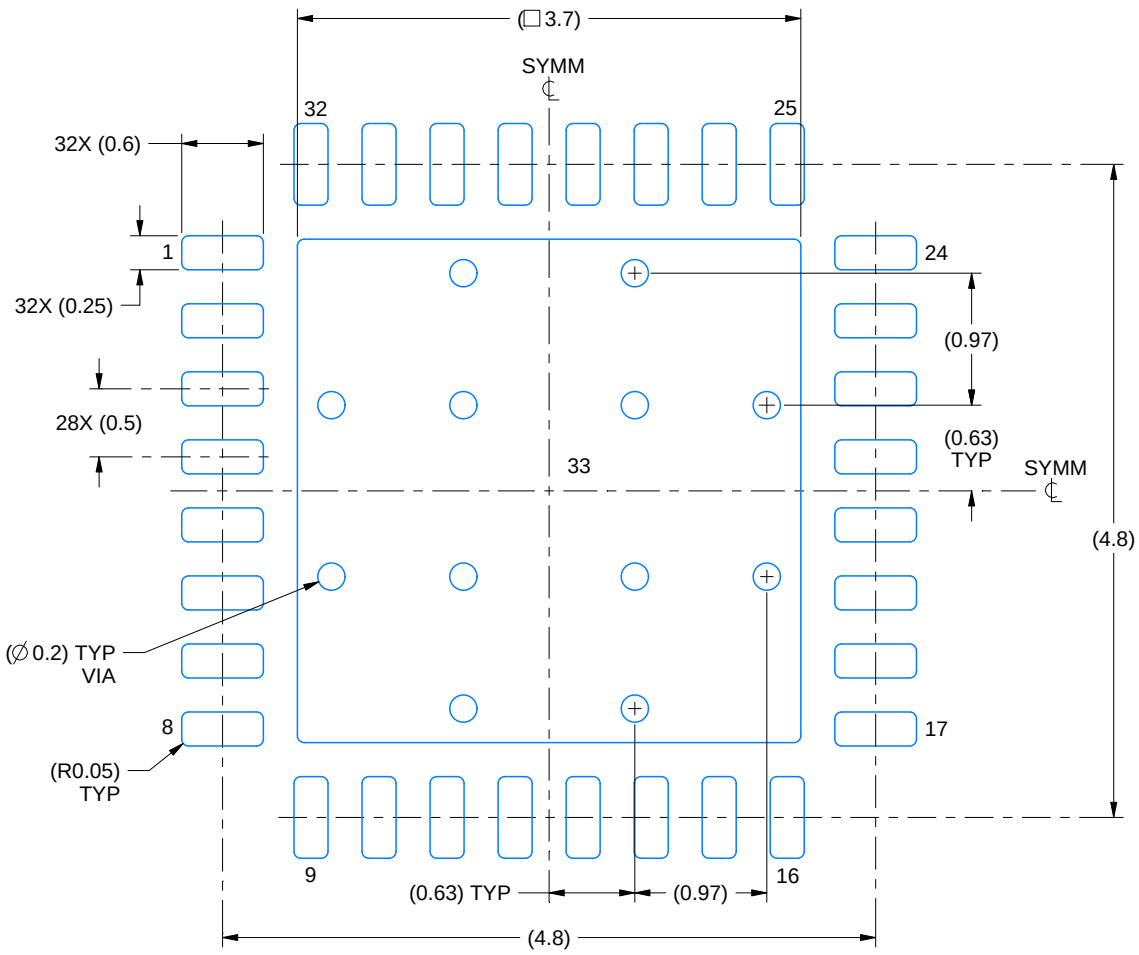
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

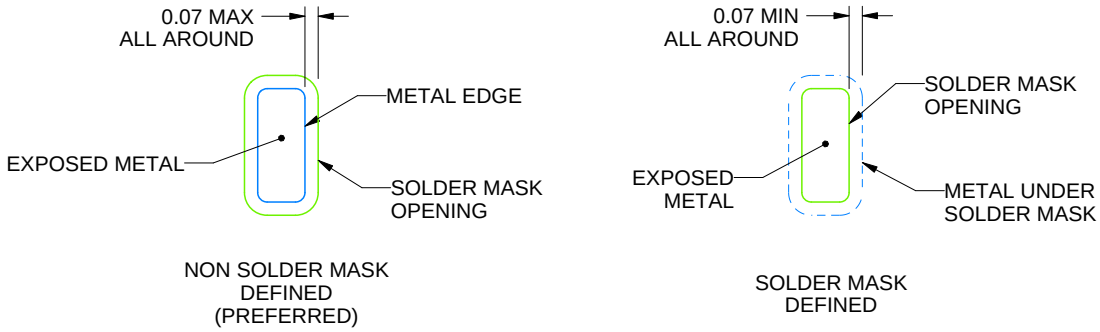
RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

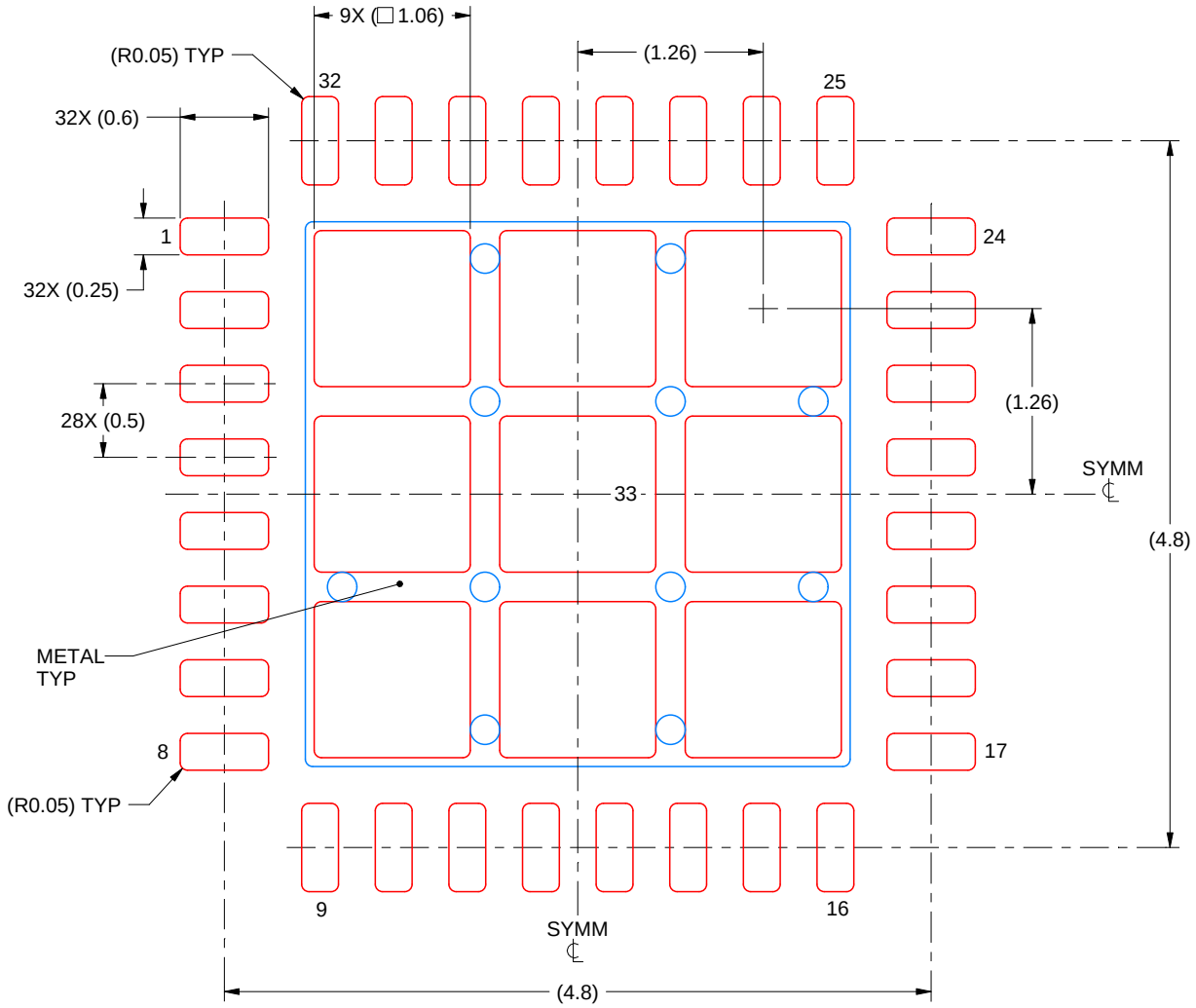


SOLDER MASK DETAILS

4225709/C 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225709/C 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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