TPS5450 5-A, Wide Input Range, Step-Down Converter

1 Features

- Wide input voltage range: 5.5 V to 36 V
- Up to 5-A continuous (6-A peak) output current
- High efficiency greater than 90% enabled by 110-mΩ integrated MOSFET switch
- Wide output voltage range: adjustable down to 1.22 V with 1.5% initial accuracy
- Internal compensation minimizes external part count
- Fixed 500-kHz switching frequency for small filter size
- 18-µA shutdown supply current
- Improved line regulation and transient response by input voltage feedforward
- System protected by overcurrent limiting, overvoltage protection, and thermal shutdown
- –40°C to 125°C operating junction temperature range
- Available in small thermally enhanced 8-pin SOIC PowerPAD™ package

2 Applications

- High density point-of-load regulators
- LCD displays, plasma displays
- Battery chargers
- 12-V and 24-V distributed power systems

3 Description

The TPS5450 is a high-output-current PWM converter that integrates a low-resistance, high-side N-channel MOSFET. Included on the substrate with the listed features are a high-performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V; an internally set slow-start circuit to limit inrush currents; and a voltage feed-forward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 µA typically. Other features include an active-high enable, overcurrent limiting, overvoltage protection and thermal shutdown. To reduce design complexity and external component count, the TPS5450 feedback loop is internally compensated.

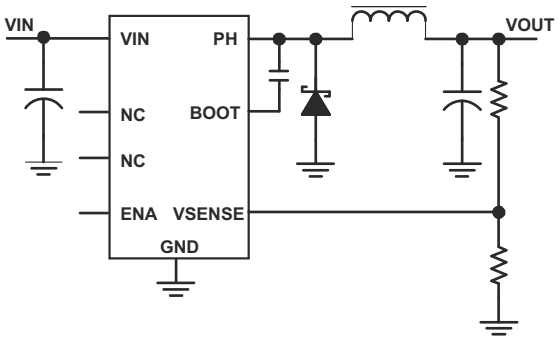
The TPS5450 device is available in a thermally-enhanced, 8-pin SOIC PowerPAD package. TI provides evaluation modules and software tool to aid in achieving high-performance power supply designs to meet aggressive equipment development cycles.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS5450	HSOP (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency vs Output Current

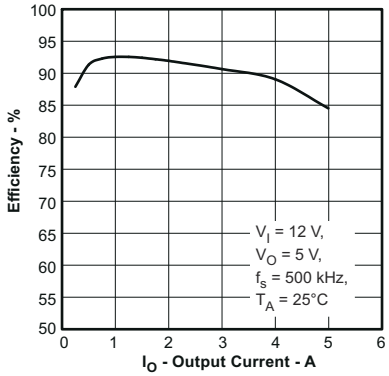


Table of Contents

4 Revision History

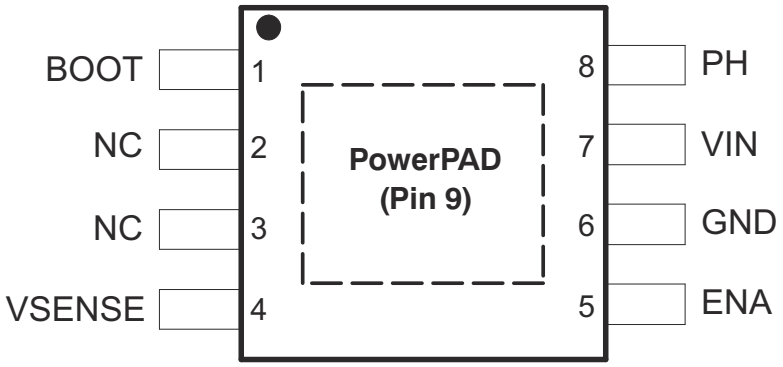
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2014) to Revision E (July 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision C (October 2013) to Revision D (September 2014)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

DDA PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	Boost capacitor for the high-side FET gate driver. Connect 0.01-µF, low-ESR capacitor from BOOT pin to PH pin.
NC	2, 3	–	Not connected internally.
VSENSE	4	I	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	I	On and off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	–	Ground. Connect to PowerPAD.
VIN	7	I	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high-quality, low-ESR ceramic capacitor.
PH	8	O	Source of the high-side power MOSFET. Connected to external inductor and diode.
PowerPAD	9	–	GND pin must be connected to the exposed pad for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V	Voltage	VIN	–0.3	40(2)	V
		PH (steady-state)	–0.6	40(2)	
		PH (transient < 10 ns)	–1.2		
		ENA	–0.3	7	
		BOOT-PH	–0.3	10	
		VSENSE	–0.3	3	
I_O	Source current	PH	Internally Limited		
I_{lkg}	Leakage current	PH		10	µA
T_J	Operating virtual junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Section 6.1* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_I	Input voltage range	5.5	36	V
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2) (3)		TPS5450 DDA 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (custom board) (4)	30	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	42.3	
ψ_{JT}	Junction-to-top characterization parameter	4.9	
ψ_{JB}	Junction-to-board characterization parameter	20.7	
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.4	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	0.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	20.8	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Maximum power dissipation may be limited by overcurrent protection
(3) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See Section 10.3 for more information.

(4) Test boards conditions:

a. 2 in x 1.85 in, 4 layers, thickness: 0.062 inch (1.57 mm).
b. 2 oz. copper traces located on the top of the PCB
c. 2 oz. copper ground planes on the 2 internal layers and bottom layer
d. 4 thermal vias (10mil) located under the device package

6.5 Electrical Characteristics

T_J = –40°C to 125°C, VIN = 5.5 V - 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	µA
UNDERVOLTAGE LOCK OUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T_J = 25°C	1.202	1.221	1.239	V
		I_O = 0 A – 5 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87%	89%		
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0~100%)		6.6	8	10	ms
CURRENT LIMIT						
	Current limit		6.0	7.5	9.0	A
	Current limit hiccup time		13	16	20	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		°C
OUTPUT MOSFET						
$r_{DS(on)}$	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
				110	230	

6.6 Typical Characteristics

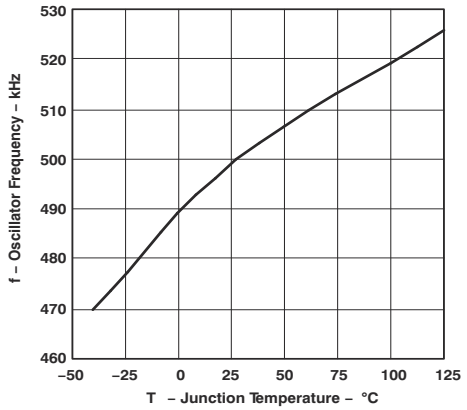


Figure 6-1. Oscillator Frequency vs Junction Temperature

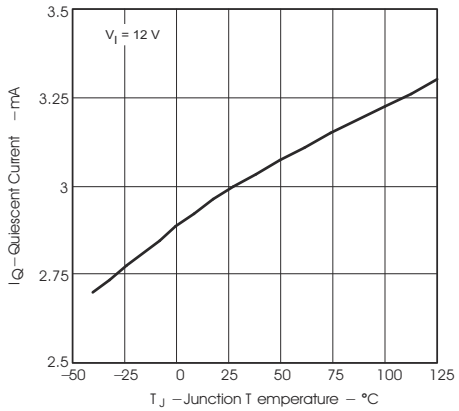


Figure 6-2. Non-Switching Quiescent Current vs Junction Temperature

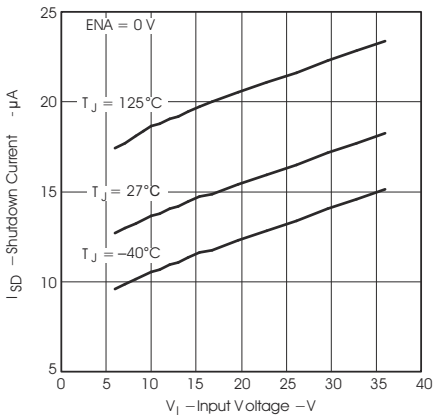


Figure 6-3. Shutdown Quiescent Current vs Input Voltage

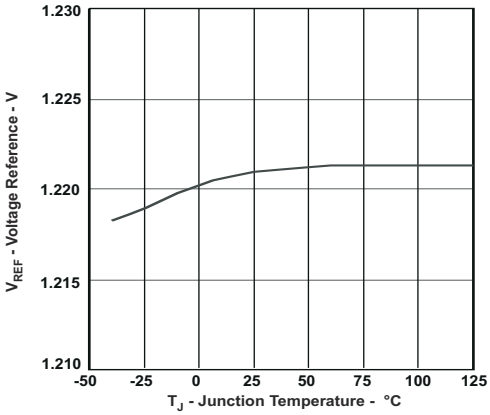


Figure 6-4. Voltage Reference vs Junction Temperature

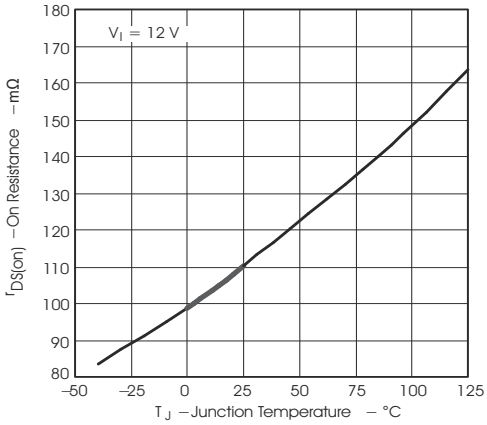


Figure 6-5. On Resistance vs Junction Temperature

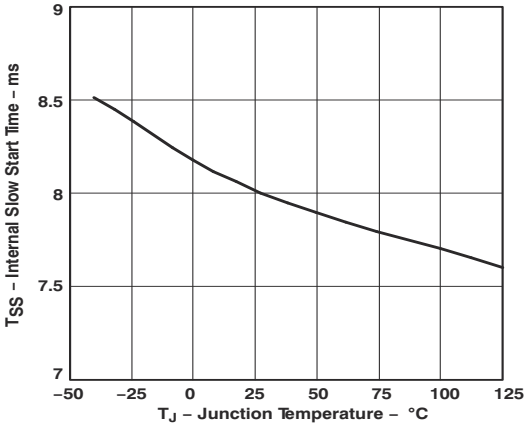


Figure 6-6. Internal Slow Start Time vs Junction Temperature

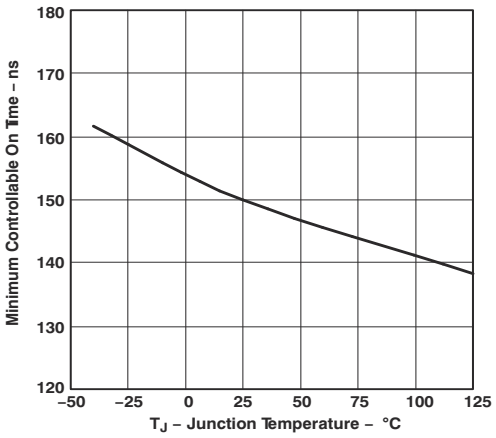


Figure 6-7. Minimum Controllable On Time vs Junction Temperature

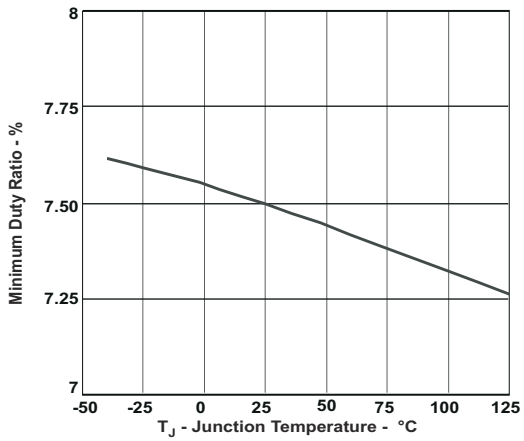


Figure 6-8. Minimum Controllable Duty Ratio vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS5450 device is a 36-V, 5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. The device implements constant-frequency voltage-mode control with voltage feed forward for improved line regulation and line transient response. Internal compensation reduces design complexity and external component count.

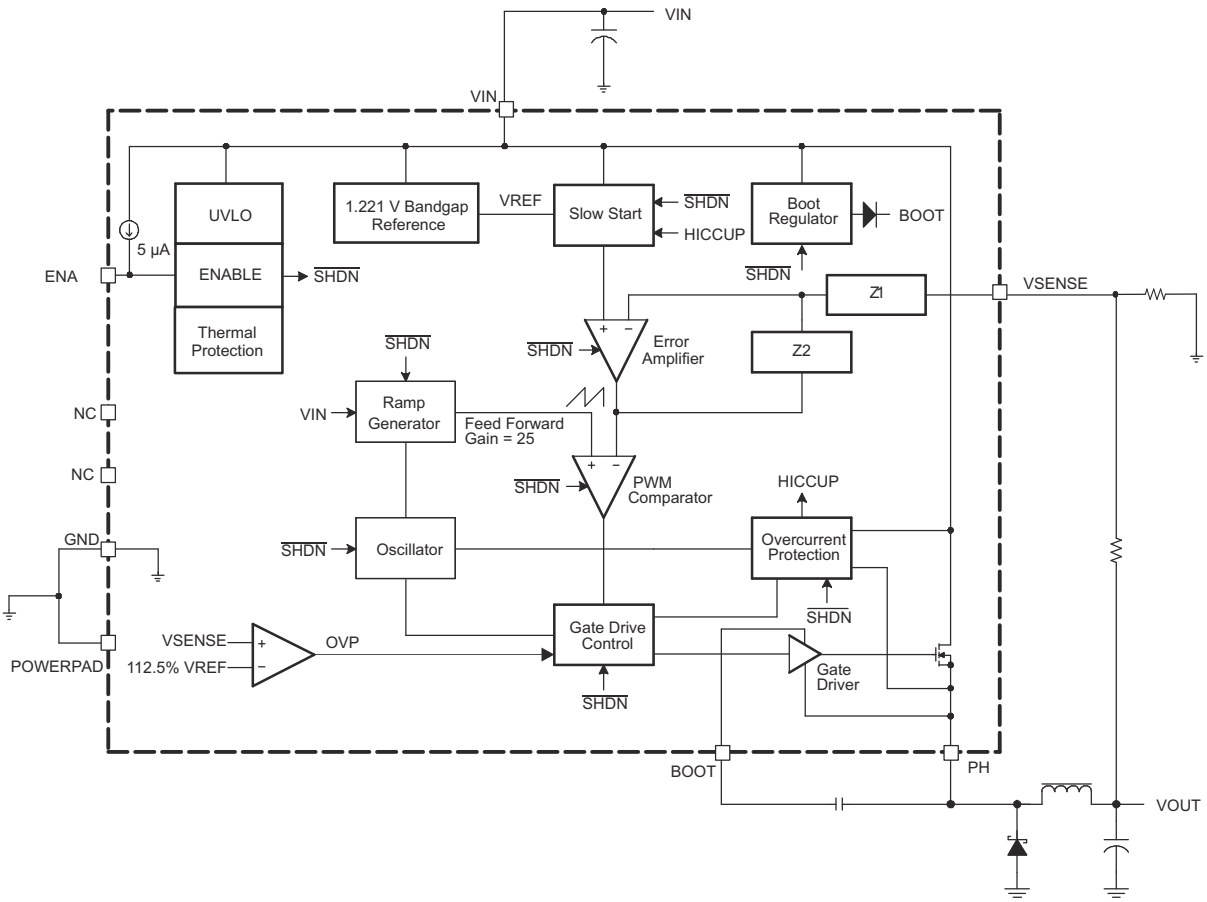
The integrated 110-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 5-A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to PH pins. The TPS5450 device reduces the external component count by integrating the bootstrap recharge diode.

The TPS5450 device has a default input start-up voltage of 5.3 V typical. The ENA pin can be used to disable the TPS5450 reducing the supply current to 18 µA. An internal pullup current source enables operation when the EN pin is floating. The TPS5450 includes an internal slow-start circuit that slows the output rise time during start-up to reduce in rush current and output voltage overshoot.

The minimum output voltage is the internal 1.221-V feedback reference. Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET is turned off and remains off until the output voltage is less than 112.5% of the desired output voltage.

Internal cycle-by-cycle overcurrent protection limits the peak current in the integrated high-side MOSFET. For continuous overcurrent fault conditions the TPS5450 will enter hiccup mode overcurrent limiting. Thermal protection protects the device from overheating.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Oscillator Frequency

The internal free running oscillator sets the PWM switching frequency at 500 kHz. The 500-kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

7.3.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable band-gap circuit. The band-gap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

7.3.3 Enable (ENA) and Internal Slow-Start

The ENA pin provides electrical on and off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow-start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow-start resets. Connecting the pin-to-ground or to any voltage less than 0.5 V will disable the regulator and activate the shutdown mode. The quiescent current of the TPS5450 in shutdown mode is typically 18 µA.

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open-drain or open-collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value, linearly. The internal slow-start time is 8 ms typically.

7.3.4 Undervoltage Lockout (UVLO)

The TPS5450 incorporates an UVLO circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power-up, internal circuits are held inactive and the internal slow-start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow-start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

7.3.5 Boost Capacitor (BOOT)

Connect a 0.01-µF, low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate-drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

7.3.6 Output Feedback (VSENSE) and Internal Compensation

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

The TPS5450 implements internal compensation to simplify the regulator design. Since the TPS5450 uses voltage mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Section 8.2.2.9.2* for more details.

7.3.7 Voltage Feed-Forward

The internal voltage feed-forward provides a constant DC power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed-forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed-forward gain, that is.

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk}-\text{pk}}} \quad (1)$$

The typical feed-forward gain of TPS5450 is 25.

7.3.8 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high-gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate-drive circuit to control the on-time of the high-side MOSFET.

7.3.9 Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system will ignore the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting mode is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, that is, hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow-start circuit.

7.3.10 Overvoltage Protection

The TPS5450 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% x VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET will be forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

7.3.11 Thermal Shutdown

The TPS5450 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow-start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

7.4 Device Functional Modes

7.4.1 Operation near Minimum Input Voltage

The device is recommended to operate with input voltages above 5.5 V. The typical VIN UVLO threshold is 5.3 V and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage the device will not switch. If EN is floating or externally pulled up to greater up than 1.3 V, when $V_{(VIN)}$ passes the UVLO threshold the device will become active. Switching is enabled and the slow-start sequence is initiated. The TPS5450 device starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time.

7.4.2 Operation With ENA Control

The enable start threshold voltage is 1.3 V maximum. With ENA held below the 0.5-V minimum stop threshold voltage the device is disabled and switching is inhibited even if VIN is above its UVLO threshold. The IC quiescent current is reduced in this state. If he EN voltage is increased above the threshold while VIN is above its UVLO threshold, the device becomes active. Switching is enabled and the slow-start sequence is initiated. The TPS5450 device starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS5450 device is a 36-V, 5-A, step-down regulator with an integrated high-side MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 5 A. Example applications are: High Density Point-of-Load Regulators, LCD and Plasma Displays, Battery Chargers, and 12-V and 24-V Distributed Power Systems. Use the following design procedure to select component values for the TPS5450 device. This procedure illustrates the design of a high-frequency switching regulator.

8.2 Typical Application

Figure 8-1 shows the schematic for a typical TPS5450 application. The TPS5450 can provide up to 5-A output current at a nominal output voltage of 5 V. For proper thermal performance, the exposed PowerPAD underneath the device must be soldered down to the printed-circuit board.

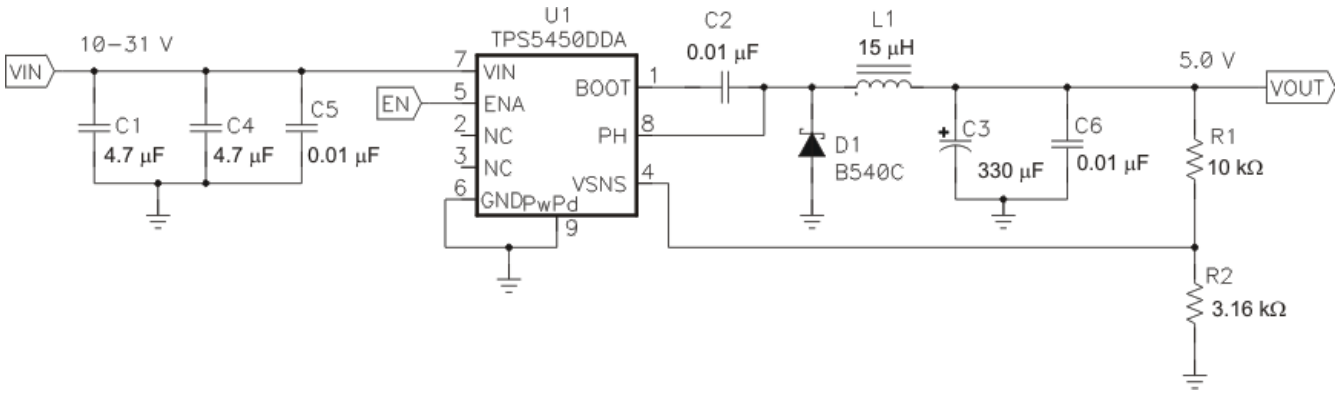


Figure 8-1. Application Circuit, 12 V to 5.0 V

8.2.1 Design Requirements

To begin the design process a few parameters must be decided upon. These requirements are typically determined at the system levels. This example is designed to the following known parameters:

Table 8-1. Design Parameters

DESIGN PARAMETER[1]	EXAMPLE VALUE
Input voltage range	10 V to 31 V
Output voltage	5 V
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

8.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS5450. Alternately, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2.2.1 Switching Frequency

The switching frequency for the TPS5450 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPS5450 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using Equation 2:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \tag{2}$$

For any TPS5450 design, start with an R1 value of 10 kΩ. For an output voltage closest to but at least 5 V, R2 is 3.16 kΩ.

8.2.2.3 Input Capacitors

The TPS5450 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum recommended decoupling capacitance is 4.7 µF. A high-quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, so long as the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple.

This input ripple voltage can be approximated by Equation 3:

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} = I_{OUT(MAX)} \times ESR_{MAX} \tag{3}$$

where

- $I_{OUT(MAX)}$ is the maximum load current
- f_{SW} is the switching frequency
- C_{IN} is the input capacitor value
- ESR_{MAX} is the maximum series resistance of the input capacitor

For this design, the input capacitance consists of two 4.7-µF capacitors, C1 and C4, in parallel. An additional high frequency bypass capacitor, C5 is also used.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 4:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \tag{4}$$

In this case the input ripple voltage would be 281 mV and the RMS ripple current would be 2.5 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen input decoupling capacitor is rated for 50 V and the ripple current capacity is greater than 2.5 A each, providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Additionally some bulk capacitance may be needed, especially if the TPS5450 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to

handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

8.2.2.4 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Since the TPS5450 is an internally compensated device, a limited range of filter component types and values can be supported.

8.2.2.5 Inductor Selection

To calculate the minimum value of the output inductor, use Equation 5:

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW(MIN)}} \quad (5)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak to peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5450, K_{IND} of 0.2 to 0.3 yields good results. Low-output ripple voltages can be obtained when paired with the proper output capacitor, the peak switch current will be well below the current limit set point and relatively low-load currents can be sourced before discontinuous operation.

For this design example use K_{IND} = 0.2 and the minimum inductor value is calculated to be 10.4 µH. A higher standard value is 15 µH, which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 6:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}}\right)^2} \quad (6)$$

The peak inductor current can be determined with Equation 7:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}} \quad (7)$$

For this design, the RMS inductor current is 5.004 A, and the peak inductor current is 5.34 A. The chosen inductor is a Sumida CDRH1127/LD-150 15µH. It has a minimum rated current of 5.65 A for both saturation and RMS current. In general, inductor values for use with the TPS5450 are in the range of 10 µH to 100 µH.

8.2.2.6 Capacitor Selection

The important design factors for the output capacitor are DC voltage rating, ripple current rating, and equivalent series resistance (ESR). The DC voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor ripple current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is desirable to keep the closed-loop crossover frequency in the range 3 kHz to 30 kHz as this frequency range has adequate phase boost to allow for stable operation. For this design example, it is assumed that the intended closed-loop crossover frequency will be between 2590 Hz and 24 kHz and also below the ESR zero of the output capacitor. Under these conditions the closed-loop crossover frequency is related to the LC corner frequency by:

$$f_{CO} = \frac{f_{LC}^{2}}{85\ V_{OUT}} \tag{8}$$

And the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \tag{9}$$

For a desired crossover of 12 kHz and a 15-µH inductor, the calculated value for the output capacitor is 330 µF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR should be:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \tag{10}$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}\ (MAX) = \frac{ESR_{MAX}\ x\ V_{OUT}\ x\ \left(V_{IN(MAX)}\ -\ V_{OUT}\right)}{N_C\ x\ V_{IN(MAX)}\ x\ L_{OUT}\ x\ F_{SW}} \tag{11}$$

where

- ΔV_{PP} is the desired peak-to-peak output ripple.
- N_C is the number of parallel output capacitors.
- F_{SW} is the switching frequency.

For this design example, a single 330-µF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 40 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 10TPB330M, rated at 10 V with a maximum ESR of 35 mΩ and a ripple current rating of 3 A. An additional small 0.1-µF ceramic bypass capacitor, C6 is also used in this design.

The minimum ESR of the output capacitor should also be considered. For good phase margin, the ESR zero when the ESR is at a minimum should not be too far above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 12:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C}\right) \tag{12}$$

where

- N_C is the number of output capacitors in parallel.
- F_{SW} is the switching frequency.

Other capacitor types can be used with the TPS5450, depending on the needs of the application.

8.2.2.7 Boot Capacitor

The boot capacitor should be 0.01 µF.

8.2.2.8 Catch Diode

The TPS5450 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is V_{INMAX} + 0.5 V. Peak current must be greater than I_{OUTMAX} plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on-time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B540A is chosen, with a reverse voltage of 40 V, forward current of 5 A, and a forward voltage drop of 0.5 V.

8.2.2.9 Advanced Information

8.2.2.9.1 Output Voltage Limitations

Due to the internal design of the TPS5450, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230\right) + V_D\right) - \left(I_{OMAX} \times R_L\right) - V_D \quad (13)$$

where

- V_{INMIN} = minimum input voltage
- I_{OMAX} = maximum load current
- V_D = catch diode forward voltage.
- R_L= output inductor series resistance.

This equation assumes maximum on resistance for the internal high-side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D \quad (14)$$

where

- V_{INMAX} = maximum input voltage
- I_{OMIN} = minimum load current
- V_D = catch diode forward voltage.
- R_L= output inductor series resistance.

This equation assumes nominal on resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

8.2.2.9.2 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5450. These designs are based on certain assumptions and will tend to always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS5450. Equation 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \quad (15)$$

where

- Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz
- Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz
- Fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed-forward gain and output filter characteristics, the closed-loop transfer function can be derived.

8.2.3 Application Curves

The performance graphs (Figure 8-2 through Figure 8-8) are applicable to the circuit in Figure 8-1. T_A = 25°C. unless otherwise specified.

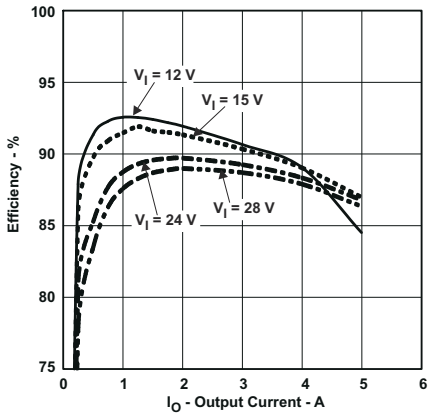


Figure 8-2. Efficiency vs. Output Current

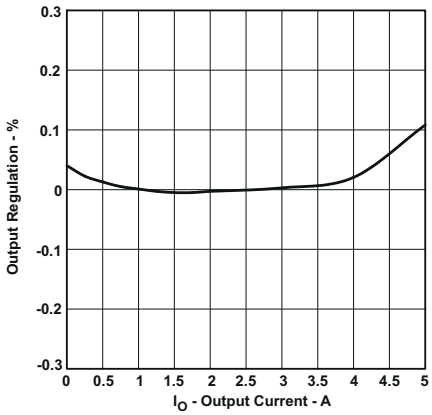


Figure 8-3. Output Regulation % vs. Output Current

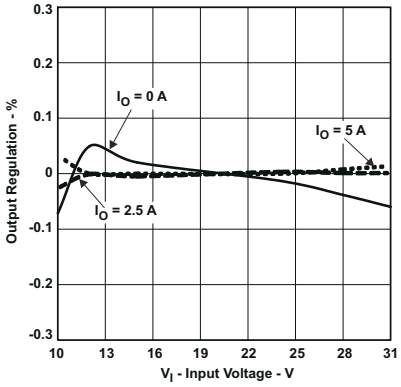


Figure 8-4. Output Regulation % vs. Input Voltage

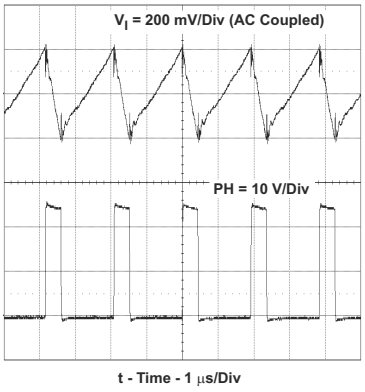


Figure 8-5. Input Voltage Ripple and PH Node, I_O = 5 A.

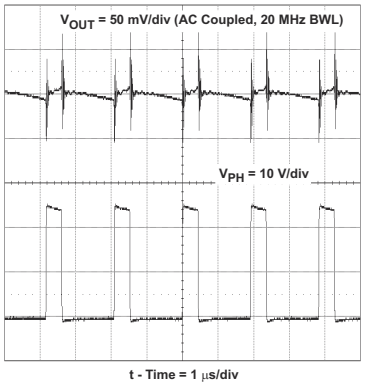


Figure 8-6. Output Voltage Ripple and PH Node, I_O = 5 A

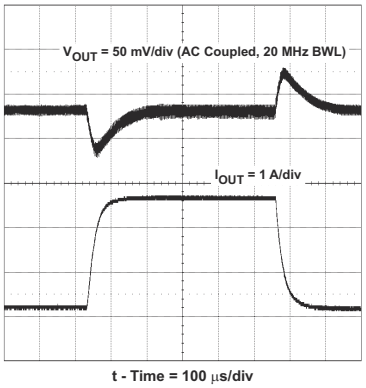


Figure 8-7. Transient Response, I_O Step 1.25 to 3.75 A.

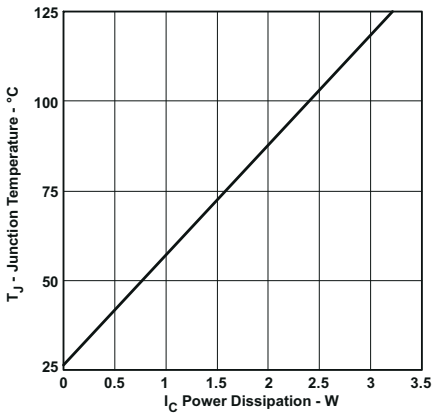


Figure 8-8. TPS5450 Power Dissipation vs Junction Temperature.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 5.5 V and 36 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS5450 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Connect a low-ESR ceramic bypass capacitor to the VIN pin. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5450 ground pin. The best way to do this is to extend the top-side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7-µF ceramic with a X5R or X7R dielectric.

There should be a ground area on the top layer directly underneath the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown below.

The PH pin should be routed to the output inductor, catch diode and boot capacitor. Since the PH connection is the switching node, the inductor should be located very close to the PH pin and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pin-out, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If using the grounding scheme shown in Figure 10-1, use a via connection to a different layer to route to the ENA pin.

10.2 Layout Example

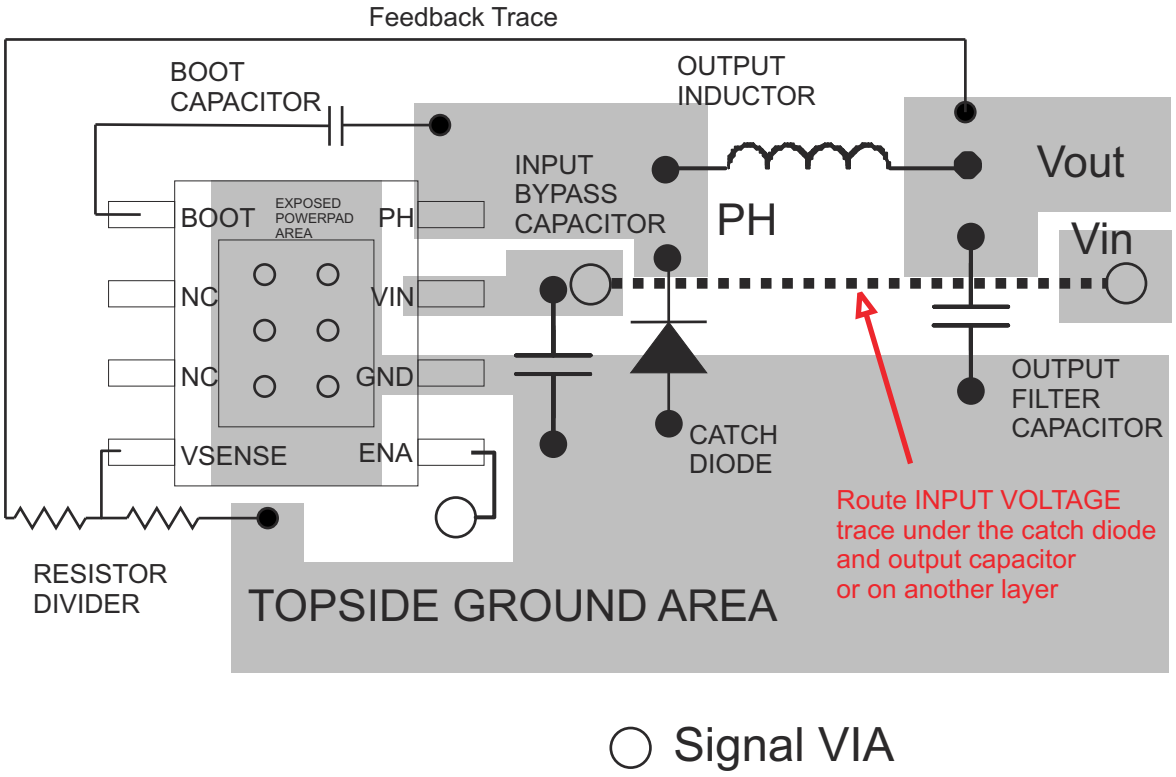


Figure 10-1. Design Layout

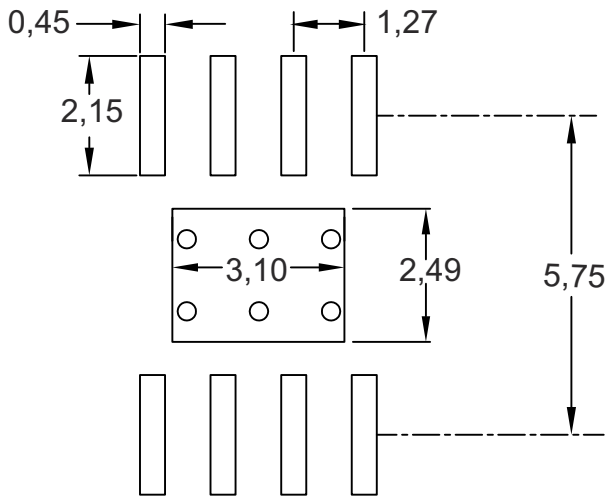


Figure 10-2. TPS5450 Land Pattern

10.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: $Pcon = I_{OUT}^{2} \times R_{DS(on)} \times V_{OUT}/V_{IN}$

Switching Loss: $Psw = V_{IN} \times I_{OUT} \times 0.01$

Quiescent Current Loss: $Pq = V_{IN} \times 0.01$

Total Loss: $Ptot = Pcon + Psw + Pq$

Given T_A → Estimated Junction Temperature: $T_J = T_A + Rth \times Ptot$

Given T_{JMAX} = 125°C → Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX} - Rth \times Ptot$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS5450DDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5450
TPS5450DDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5450
TPS5450DDAG4	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5450
TPS5450DDAR	NRND	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5450
TPS5450DDAR.A	NRND	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5450
TPS5450DDARG4	NRND	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5450

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

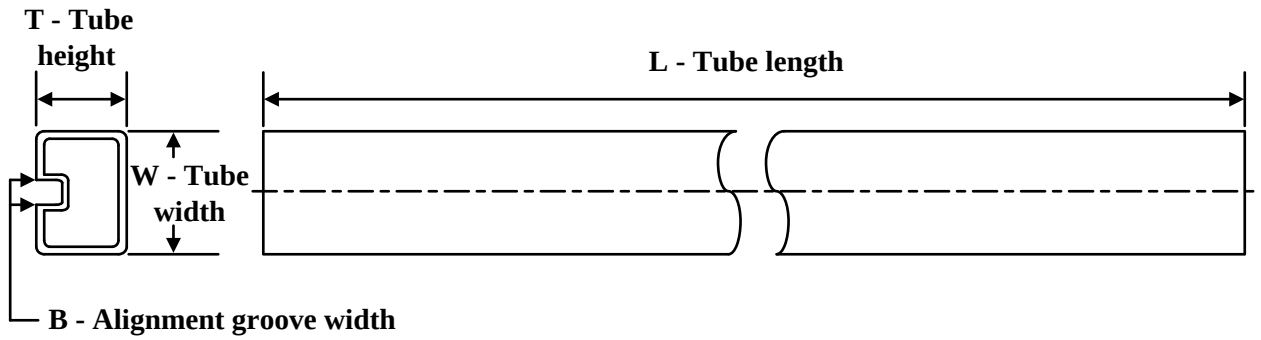
OTHER QUALIFIED VERSIONS OF TPS5450 :

- Automotive : TPS5450-Q1
- Enhanced Product : TPS5450-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TUBE

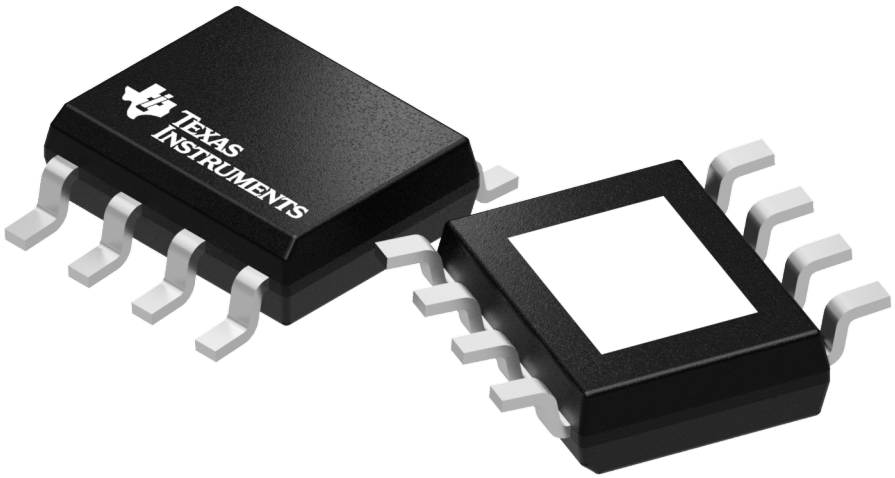


*All dimensions are nominal

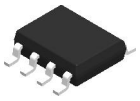
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS5450DDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
TPS5450DDA.A	DDA	HSOIC	8	75	506.6	8	3940	4.32
TPS5450DDAG4	DDA	HSOIC	8	75	506.6	8	3940	4.32

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

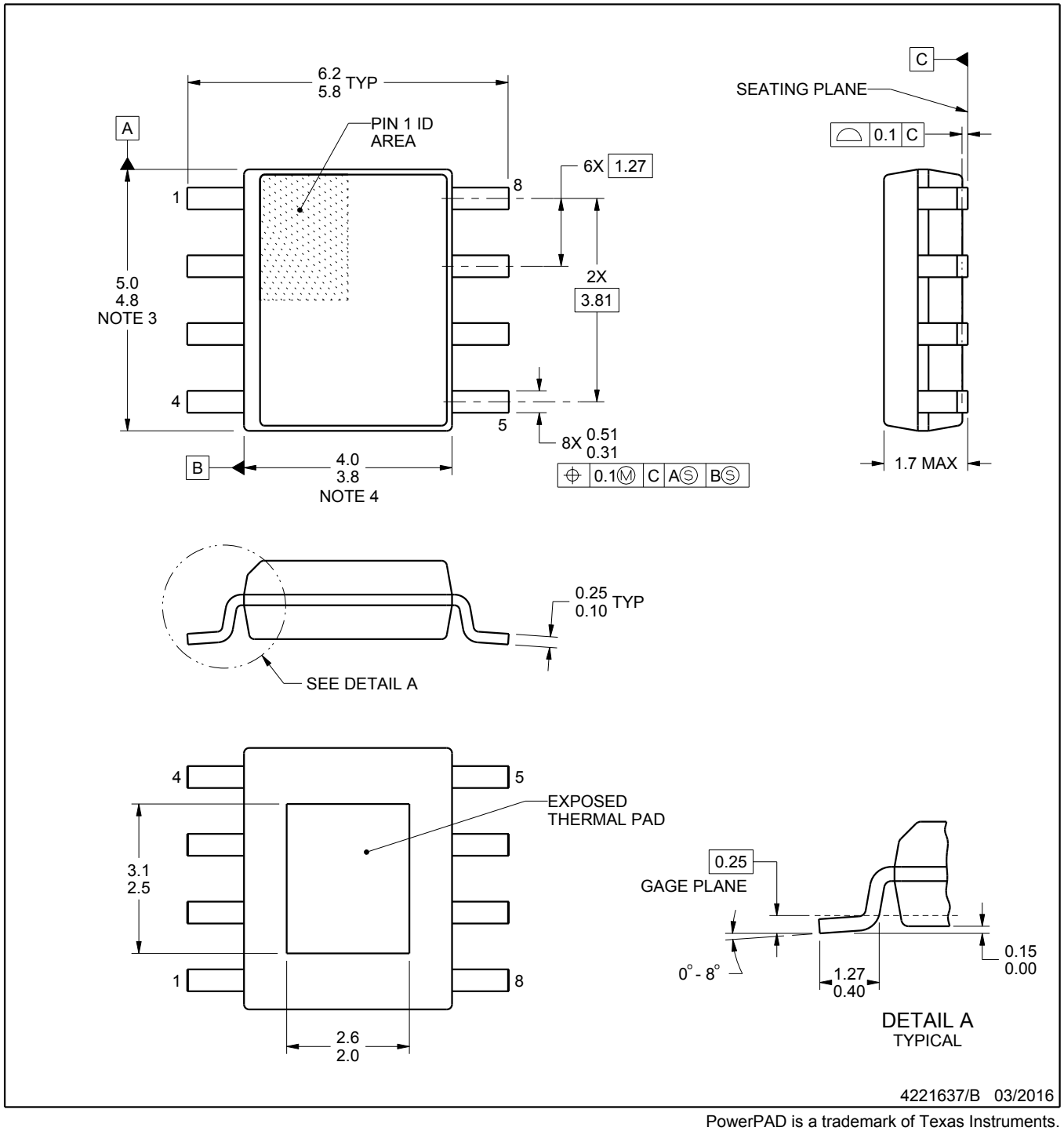


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



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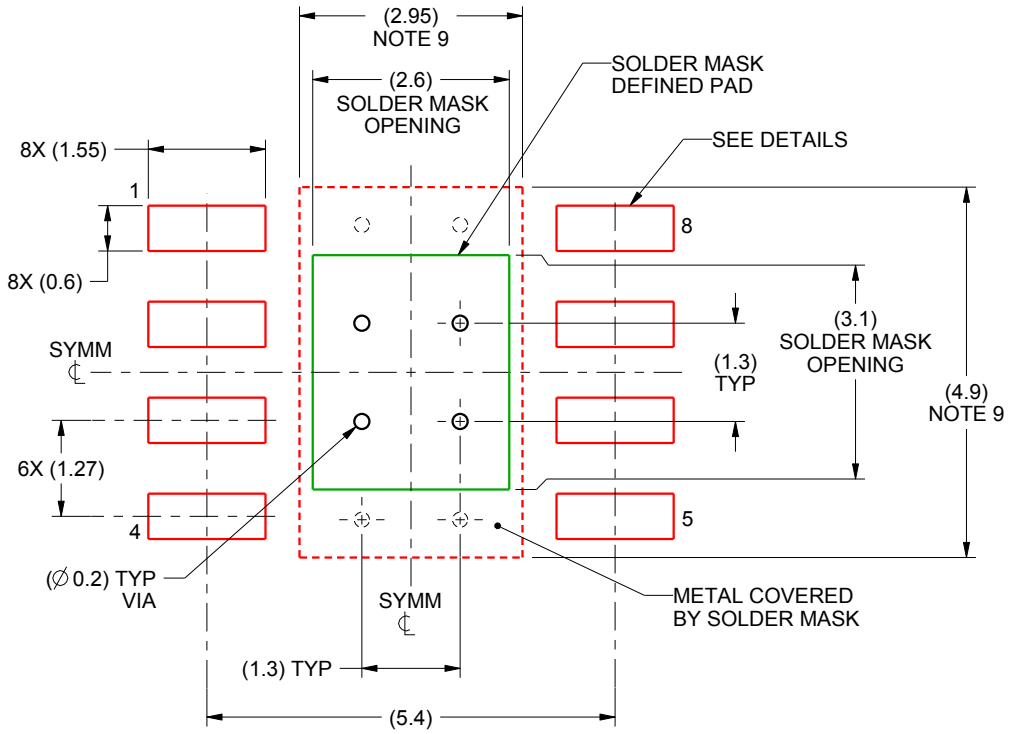
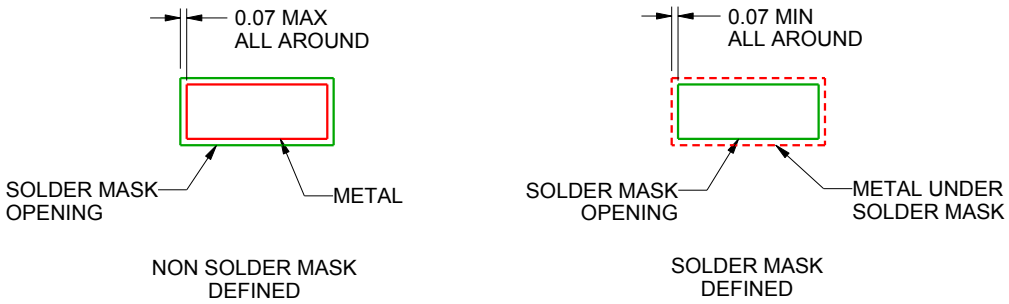
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

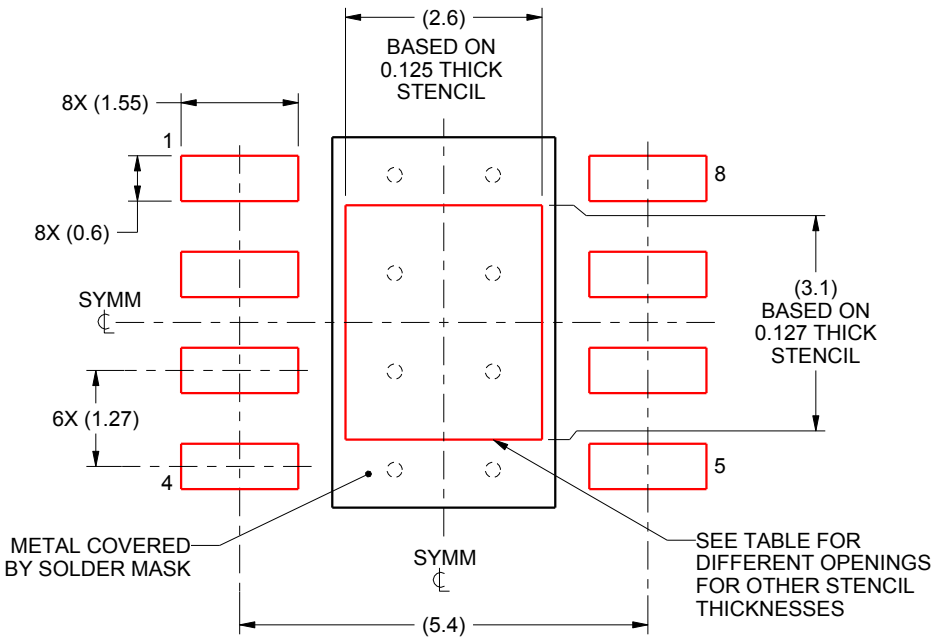


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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