TPS51215A Single Phase, D-CAP2™ Controller with 2-Bit VID Control and Low Power Mode

1 Features

- Differential voltage feedback
- DC compensation for accurate regulation
- Wide input voltage range: 3 V to 28 V
- Flexible, 2-bit VID supports output voltage from 0.5-V to 2.0-V and 0-V V_{OUT}
- D-CAP2™ mode at 600kHz for Ultra-Low/Low ESR Output Capacitor
- 4700 ppm/°C, low-side $R_{DS(on)}$ current sensing
- Programmable soft-start time and output voltage transition time
- Built-in output discharge
- Power good output
- Integrated boost switch
- Built-in OVP/UVP/OCP
- Thermal shutdown (non-latched)
- 3-mm × 3-mm, 20-Pin, QFN (RUK) package

2 Applications

- Notebook computers
- Desktop computers
- Industrial PC

3 Description

The TPS51215A is a single-phase, D-CAP2™ synchronous buck controller with a 2-bit VID input supporting 0 V and three other independent externally programmable output voltage levels, where full external programmability of the voltage level, step setting and voltage-change slew rate is desired. It is used for Intel IMVP8/9 applications where multiple voltage levels are desired.

The TPS51215A supports all POS/SPCAP and/or all ceramic MLCC output capacitor options in applications where remote sense is a requirement. Tight DC load regulation is achieved through external programmable integrator capacitor. The TPS51215A provides full protection suite, including OVP, OCL, 5-V UVLO and thermal shutdown. It supports the conversion voltage up to 28 V, and output voltages adjustable from 0.5 V to 2 V.

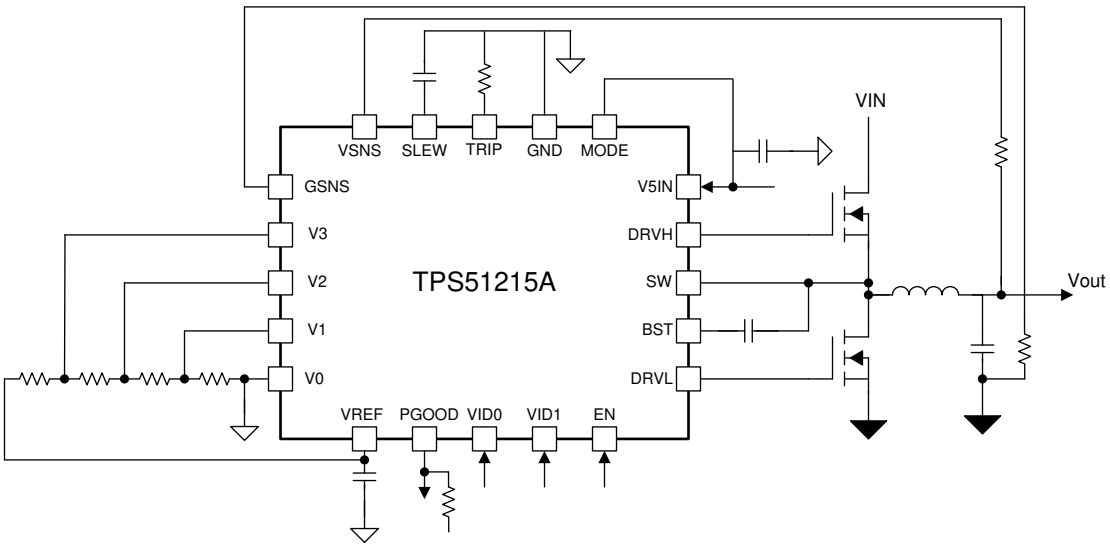
The TPS51215A is available in the 3 mm × 3 mm, QFN, 0.4-mm pitch package and is specified from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51215A	WQFN (20)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2020	A	initial release

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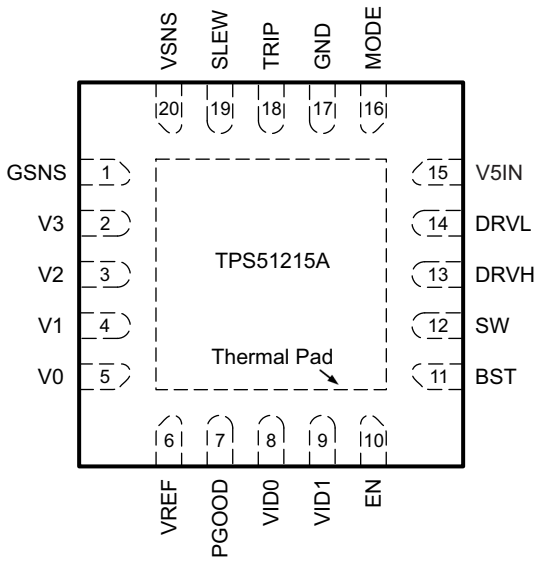
5 Pin Configuration and Functions

RUK Package
20-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	11	I	Supply input for high-side MOSFET driver (bootstrap terminal). Connect a capacitor from this pin to the SW pin. Internally connected to V5IN via the bootstrap MOSFET switch.
DRVH	13	O	High-side MOSFET gate driver output.
DRVL	14	O	Synchronous low-side MOSFET gate driver output.
EN	10	I	Enable input for the device. Support 3.3-V logic
GND	17	I	Combined AGND and PGND point. The positive on-resistance current sensing input.
GSNS	1	I	Voltage sense return tied directly to GND sense point of the load. Tie to GND with a 10-Ω resistor to close feedback if remote sensing is used. Short to GND if remote sense is not used.
MODE	16	I	connect to V5IN
PGOOD	7	O	PGOOD output. Connect pull-up resistor.
SLEW	19	I	Program the startup using 4.5 µA and voltage transition time using 45 µA from an external capacitor via current source.
SW	12	I/O	High-side MOSFET gate driver return. The $R_{DS(on)}$ current sensing input (–).
TRIP	18	I	Connect resistor to GND to set OCL at V_{TRIP}/8. Output 10 µA current at room temperature, T_C = 4700ppm/°C.
V0	5	I	Voltage need to be set to 0V, corresponding to 00
V1	4	I	Voltage set-point programming resistor input, corresponding to 01
V2	3	I	Voltage set-point programming resistor input, corresponding to 10
V3	2	I	Voltage set-point programming resistor input, corresponding to 11
V5IN	15	I	5-V power supply input for internal circuits and MOSFET gate drivers
VID0	8	I	Logic input for set-point voltage selector. Use in conjunction with VID1 pin to select among four set-point reference voltages. Support 1-V and 3.3-V logic.
VID1	9	I	Logic input for set-point voltage selector. Use in conjunction with VID0 pin to select among four set-point reference voltages. Support 1-V and 3.3-V logic.
VREF	6	O	2 V, 300-µA voltage reference. Bypass to GND with a 1-µF ceramic capacitor.
VSNS	20	I	Voltage sense return tied directly to the load voltage sense point. Tie to V_{OUT} with a 10-Ω resistor to close feedback if remote sensing is used.
Thermal Pad	—	—	Connect directly to system GND plane with multiple vias.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Input voltage range(2)	BST		–0.3	36	V
	BST(3)		–0.3	6	
		transient < 20 ns	–2	6.5	
	SW		–5	30	
		transient < 20 ns	–5	32	
	EN, TRIP, MODE, VID1, VID0		–0.3	5.5	
	V5IN		–0.3	5.3	
	SLEW, VSNS		–0.3	3.6	
	GSNS		–0.35	0.35	
	GND		–0.3	0.3	
Output voltage range(2)	DRVH		–5	36	V
	DRVH(3)		–0.3	6	
		transient < 20 ns	–2	6.5	
	DRVL		–0.3	6	
		transient < 20 ns	–2	6.5	
	PGOOD		–0.3	6	
	VREF, V0, V1, V2, V3		–0.3	3.6	
Junction temperature, T_J			–40	150	°C
Storage temperature, T_{STG}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage	V5IN		4.5	5.25	V
Input voltage range	BST		–0.1	33.5	V
	BST(1)		–0.1	5.5	
	SW		–3	28	
	SW(2)		–4.5	28	
	EN, TRIP, MODE, VID1, VID0		–0.1	5.5	
	SLEW, VSNS		–0.1	3.5	
	GSNS		–0.3	0.3	
	GND		–0.1	0.1	
Output voltage range	DRVH		–3	33.5	V
	DRVH(2)		–4.5	33.5	
	DRVH(1)		–0.1	5.5	
	DRVL		–0.1	5.5	
		transient < 20 ns	–1.5	5.5	
	PGOOD		–0.1	5.5	
	VREF, V0, V1, V2, V3		–0.1	3.5	
Operating free-air temperature, T_J			–40	125	°C

(1) Voltage values are with respect to the SW terminal.
(2) This voltage should be applied for less than 30% of the repetitive period.

6.4 Thermal Information

THERMAL METRIC(1)		TPS51215A RUK (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended free-air temperature range, VIN = 12 V, V5IN = 5V, T_J = -40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input Voltage Range	VIN	3		28	V
I_{V5IN}	V5IN Supply Current	No load, V_{EN}=3.3V,Vout ≠0, Non Switching, V_{MODE}=5V		610		µA
	V5IN Stand-by Current	No load, V_{EN}=3.3V, Vout=0		250		µA
$I_{V5INSDN}$	V5IN Shutdown Current	No load, V_{EN}=0V		1		µA
UVLO						
V_{V5IN_UVLO}	V5IN Under-Voltage Lockout	Wake up V5IN voltage		4.4	4.6	V
		Shut down V5IN voltage	3.8	4		V
		Hysteresis V5IN voltage		400		mV
VREF VOLTAGE						

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Electrical Characteristics (continued)

Over recommended free-air temperature range, VIN = 12 V, V5IN = 5V, T_J = -40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREF}	Output Voltage	I_{VREF} = 30 µA, w/r/t GSNS		2		V
$V_{VREFTOL}$	Output Voltage Tolerance	0 µA ≤I_{VREF} ≤ 30 µA, 0°C ≤T_J ≤ 85°C	–0.8		0.8	%
		0 µA ≤I_{VREF} ≤ 300 µA, -40°C ≤T_J ≤ 125°C	–1		1	%
$I_{VREFOCL}$	Current Limit	$V_{VREF-GSNS}$ = 1.7V	0.4	1		mA
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching Frequency (1)	V_{IN} = 12 V, V_{VSNS} = 1.8 V, VMODE =5V		600		kHz
$T_{ON(MIN)}$	Minimum On-time	DRVH rising to falling		40		ns
$T_{OFF(MIN)}$	Minimum Off-time	DRVH falling to rising		320		ns
DRIVERS						
R_{DRVH}	High-side Driver Resistance	Source, I_{DRVH} = 50 mA		1.5		Ω
		Sink, I_{DRVH} = 50 mA		0.6		Ω
R_{DRVL}	Ligh-side Driver Resistance	Source, I_{DRVL} = 50 mA		0.9		Ω
		Sink, I_{DRVL} = 50 mA		0.4		Ω
t_D	Dead Time	DRVH-off to DRVL-on		14		ns
		DRVL-off to DRVH-on		21		ns
SOFTSTART AND SLEWRATE						
I_{SLEW}	During Soft Start			4.5		µA
	During Vout Dynamic Scaling			45		µA
POWER GOOD						
T_{PGDLY}	PG Deglitch Time	PG from low to high		1		ms
		PG from high to low		0.2		us
V_{PGTH}	PG Threshold	VOUT falling (fault)		84		%
		VOUT rising (good)		92		%
		VOUT rising (fault)		116		%
		VOUT falling (good)		108		%
I_{PGMAX}	PG Sink Current	V_{PGOOD} =0.5V		6		mA
I_{PGLK}	PG Leak Current	V_{PGOOD} =5.5V			1	uA
CURRENT LIMIT						
I_{TRIP}	TRIP source current	T_J = 25°C, V_{TRIP} = 0.4 V	9	10	11	µA
TC_{TRIP}	TRIP source current temperature coefficient(1)			4700		ppm/C
V_{TRIP}	VTRIP Voltage Range		0.2		3	V
V_{OCL}	Current Limit Threshold	V_{TRIP} = 3.0V	360	375	390	mV
		V_{TRIP} = 1.6V	188	200	212	
		V_{TRIP} = 0.2V	20	25	30	
V_{NOCL}	Negative Current Limit Threshold	V_{TRIP} = 3.0V	–390	–375	–360	mV
		V_{TRIP} = 1.6V	–212	–200	–188	
		V_{TRIP} = 0.2V	–30	–25	–20	
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN Threshold High-level		1.5			V
$V_{EN(OFF)}$	EN Threshold Low-level				0.5	V
$V_{EN(HSYS)}$	EN Hysteresis			250		mV
I_{EN}	EN Leakage Current		–1		1	uA
$V_{VIDx(HI)}$	VIDx Threshold High-level		0.9			V

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Electrical Characteristics (continued)

Over recommended free-air temperature range, VIN = 12 V, V5IN = 5V, T_J = -40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VIDx(LI)}$	VIDx Threshold Low-level				0.3	V
I_{VIDx}	VIDx Leakage Current		–1		1	uA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP Trip Threshold		118	120	123	%
T_{OVPDLY}	OVP Deglitch Time			0.2		us
V_{UVP}	UVP Trip Threshold		65	68	70	%
T_{UVPDLY}	UVP Deglitch Time			1		ms
VOUT VOLTAGE						
$V_{SLEWCLP}$	SLEW Clamp Voltage	V_{REFIN} = 1.1 V	1.012		1.188	V
g_M	Error Amplifier Transconductance	V_{REFIN} = 1.1 V		60		us
I_{SNS}	VSNS Input Current	V_{VSNS} = 1.1 V		20		uA
$I_{VSNSDIS}$	VSNS Discharge Current	EN=0, V_{VSNS}=0.5V,VMODE = 5V		12		mA
OUTPUT DISCHARGE						
R_{DIS}	Discharge Resistance	T_J=25°C, V_{VOUT} =0.5V, V_{EN}=0V		42		Ω
Thermal protection						
T_{OTP}	OTP Trip Threshold			140		°C
T_{OTPHSY}	OTP Hysteresis			10		°C

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6.6 Typical Characteristics

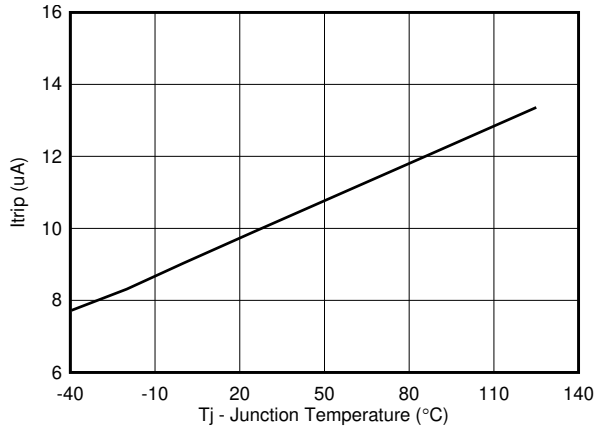

Figure 1. Trip Current Vs Temperature

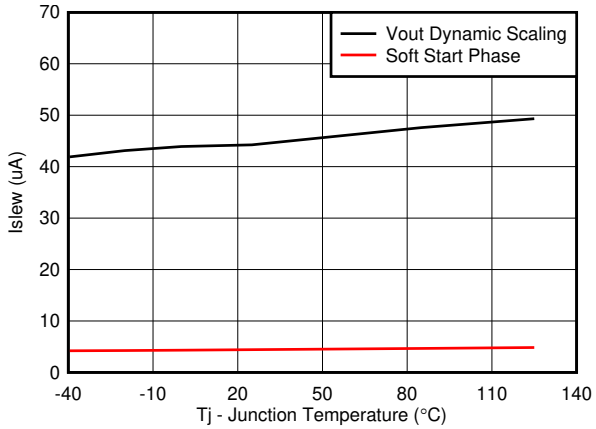

Figure 2. Slew Current Vs Temperature

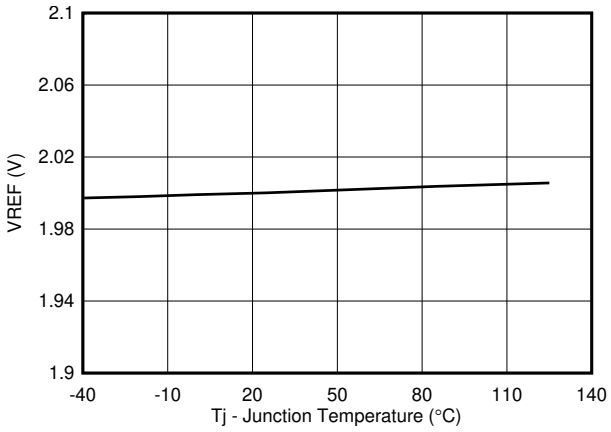

Figure 3. VREF Voltage Vs Temperature, I_{VREF}=0A

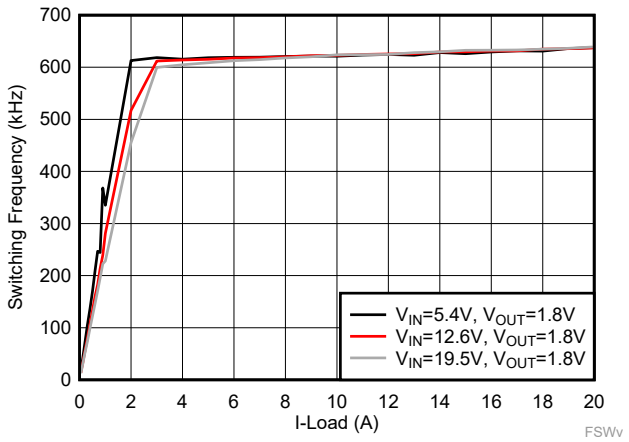

Figure 4. Switching frequency Vs Loading Current

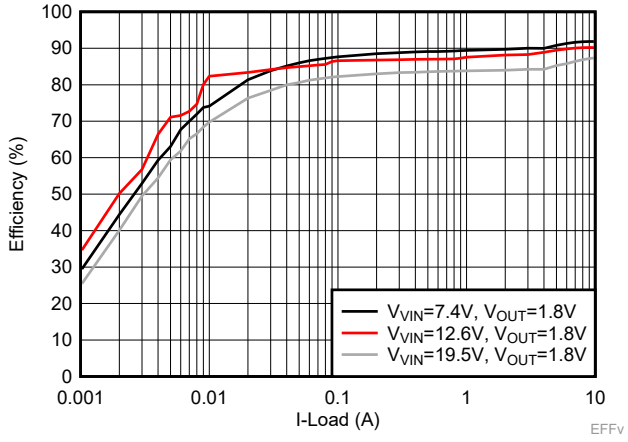

Figure 5. Efficiency Curve, Vout=1.8V

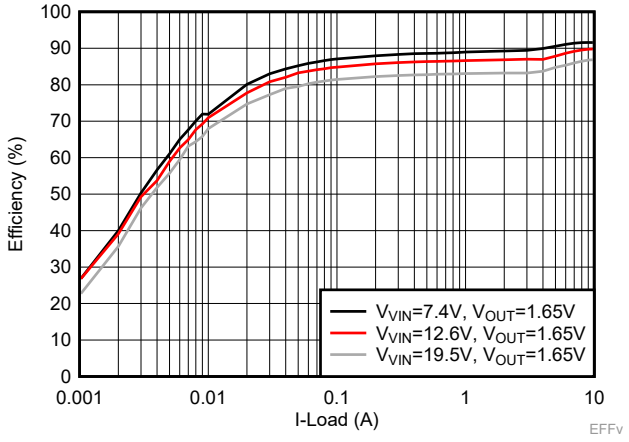

Figure 6. Efficiency Curve, Vout=1.65V

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7 Detailed Description

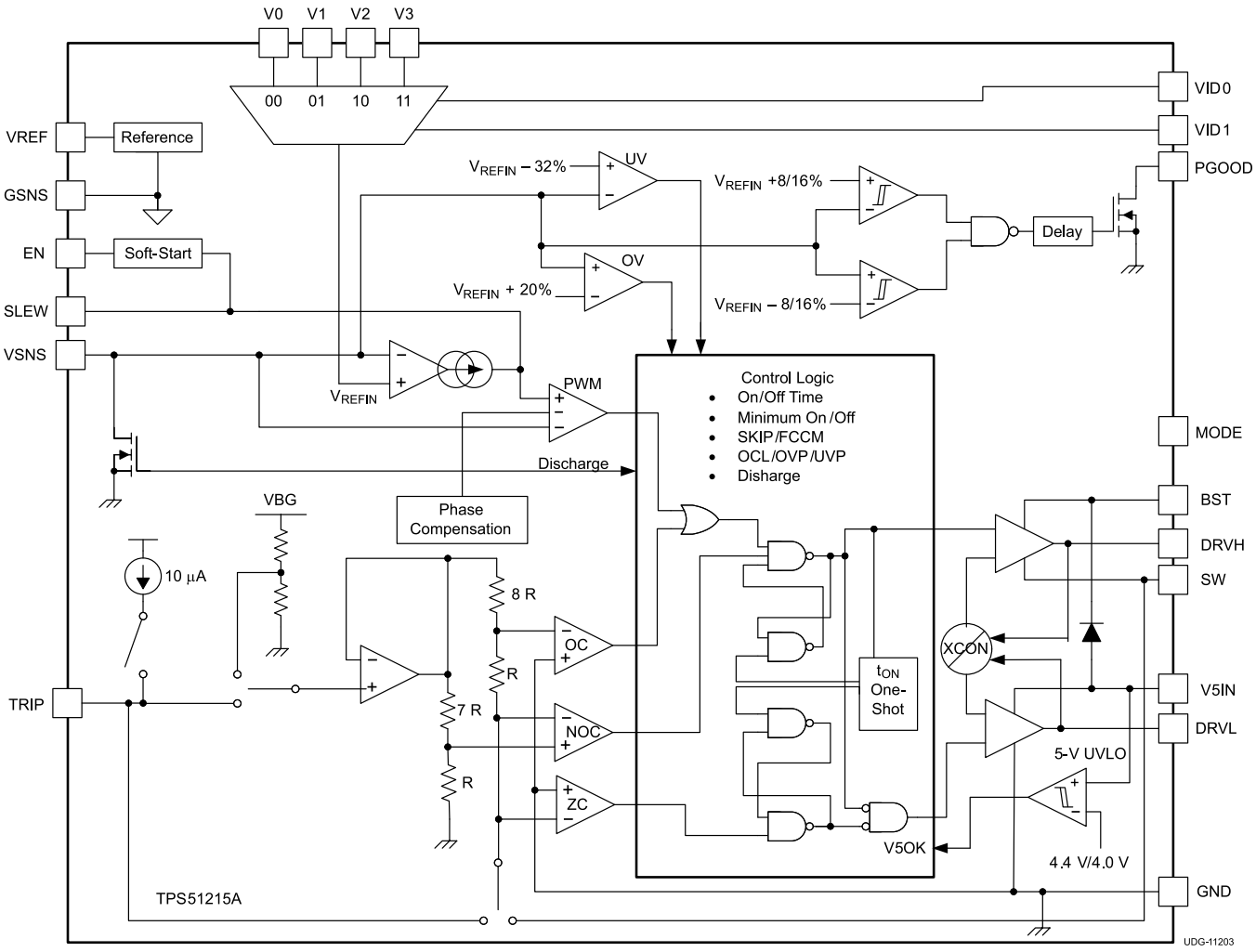
7.1 Overview

TPS51215A is a synchronous step-down controller which can operate from 3 V to 28 V input voltage (V_{IN}). The proprietary D-CAP2™ mode enables low external component count, ease of design, optimization of the power rail for cost, size and efficiency. TPS51215A is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The TPS51215A needs an external 5V supply to power the internal control circuitry. The undervoltage lockout (UVLO) circuit monitors the V5IN pin voltage to protect the internal circuitry from low input voltages. TPS51215A operates in fixed 600kHz switching frequency.

The TPS51215A supports 2-bits VID and Low Power Mode(LPM) to dynamically change the Vout voltage to satisfy the Intel IMVP8/9 applications — VCCIN_AUX, VCCIO_0, VCCIO_1_2 applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Switch Mode Power Supply Control

The TPS51215A is a high performance, single-synchronous step-down controller with differential voltage feedback. It realizes accurate regulation at the specific load point over wide load range.

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Feature Description (continued)

The TPS51215A is using D-CAP2 mode which do not require complex external compensation networks and can minimize the external components counts. An adaptive on-time control scheme is used to achieve pseudo-constant frequency. The TPS51215A adjusts the on-time (t_{ON}) to be inversely proportional to the input voltage (V_{IN}) and proportional to the SMPS output voltage (V_{OUT}). The switching frequency remains nearly constant over the variation of input voltage at the steady-state condition.

7.3.2 VREF, V0, V1, V2, V3 and Output Voltage

The device provides a 2.0-V, accurate voltage reference from the VREF pin. This output has a 300-µA current sourcing capability to drive V1, V2 and V3 input voltages through a voltage divider circuit as shown in Figure 7. If higher overall system accuracy is required, the sum of total resistance (R1+R2+R3+R4+R5) from VREF to GND should be designed to be more than 67 kΩ. A MLCC capacitor with a value of 0.1-µF or larger should be placed close to the VREF pin.

The device also provides 2-bit VID flexible output voltage control. Fixed 0V output voltage and up to three voltage levels can be programmed externally by a voltage divider circuit. Fixed 0V output voltage corresponds to VID 00, V1 corresponds to VID 01, V2 corresponds to VID 10 and V3 corresponds to VID 11. It is not necessary to match the voltage set point (V_{SET1}, V_{SET2} or V_{SET3}) to any particular V1, V2 or V3 input. Assignment of the input voltage is entirely dependent on the user requirement, which makes the device very easy and flexible to use.

The device can also be configured to provide 1-bit VID flexible output voltage operation. In the applications where fewer than four input voltage levels are needed, the remaining input voltage pins cannot be left floating.

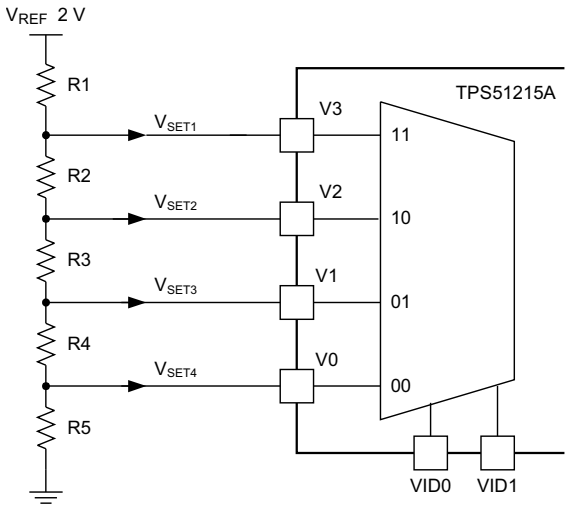

Figure 7. Setting the Output Voltage

7.3.3 Soft-Start and Power Good

Prior to asserting EN high, the power stage conversion voltage and V5IN voltage should be ready. When EN is asserted high, TPS51215A provides soft start to suppress in-rush current during start-up. The soft start action is achieved by an internal SLEW current of 4.5 µA (typ) sourcing into a external MLCC capacitor connected from SLEW pin to GND.

Use Equation 1 to determine the soft-start timing.

$$t_{SS} = C_{SLEW} \times \frac{V_{OUT}}{I_{SLEW}} \quad (1)$$

where

- C_{SLEW} is the soft start capacitance
- V_{OUT} is the output voltage
- I_{SLEW} is the internal 4.5-µA current source

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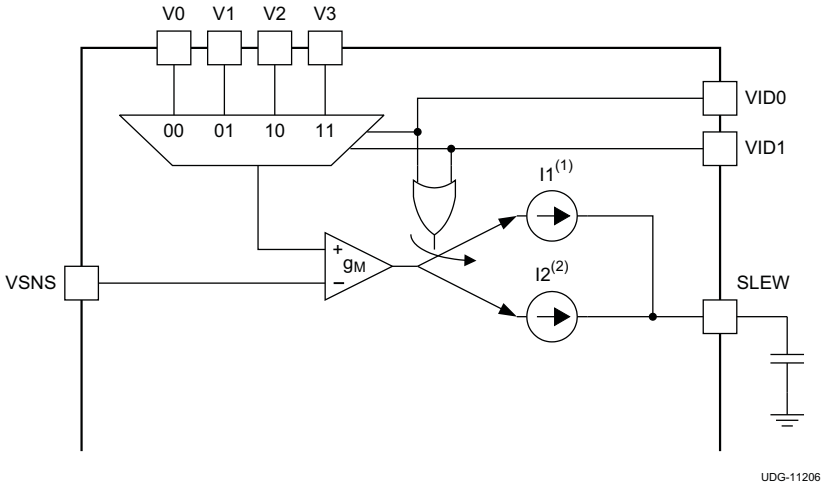
Feature Description (continued)

The TPS51215A has a open-drain PowerGood output pin that indicates the Vout voltage is within the target range. The target voltage window and transition delay times of the PGOOD comparator are ±8% (typ) and 1-ms delay for assertion from low to high, and ±16% (typ) and 0.2-µs delay for de-assertion from high to low during operation.

7.3.4 SLEW and VID Function

In addition to providing soft start function, SLEW is also used to program the VID transition time. TPS51215A supports 2-bit VID and 1-bit VID operations. VID0 and VID1 works with 1.05-V logic level signals with capability of supporting up to 3.3-V logic high.



(1) I1: Enable during VID transitioning, 45 µA.

(2) I2: Soft start, 4.5 µA.

Figure 8. VID Configuration

During VID transition:

- SLEW current is increased to 45 µA. Based on the VID transition time of the system, the amount of the SLEW capacitance can be calculated to meet such requirement. The minimum SLEW capacitance can be supported by the device is 2nF.

$$C_{SLEW} = I_{SLEW} \times \frac{dt}{dV} \quad (2)$$

  where

  - I_{SLEW} is 45 µA, dV is the voltage change during VID transition
  - dt is the required transition time

- FCCM (forced continuous conduction mode) operation is used regardless of the load level. In the meantime, the overcurrent level is temporality increased to 125% times the normal OCL level to prevent false OC trip during fast SLEW up transition. Power good, UVP and OVP functions are all blanked as well. All normal functions are resumed 16 internal clock cycles (64 µs) after VID transition is completed.
- Additional SLEW CLAMP is implemented. If severe output short occurs (either to GND or to some other high voltage rails in the system), SLEW is engaged into SLEW CLAMP, approximately 50 mV above or below the output voltage reference point. After 32 internal clockcycles, the CLAMP is engaged, UVP and OVP functions are activated to disable the controller at fault.
- If VID 00 is selected, part will enter low power mode where the DRVL and DRVH will be stop switching and Vout will decay to 0V. At mean time, the PGOOD pin still keeps high. The Vout transition time can be calculated by Equation 2
- VID is fixed to 11 internally until soft-start end which means that Vout ramp to V3 in soft start period. Figure 10 showed the power up sequence

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Feature Description (continued)

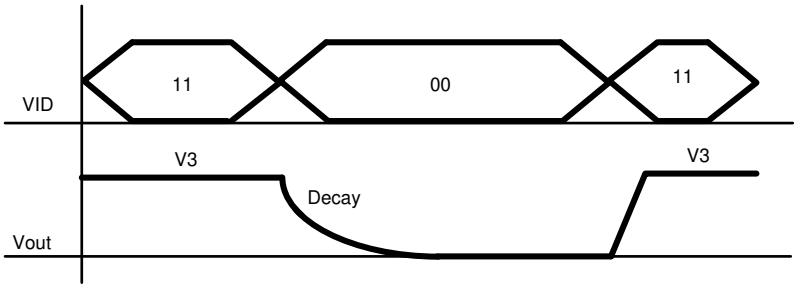

Figure 9. Low Power Mode Enter and Exit

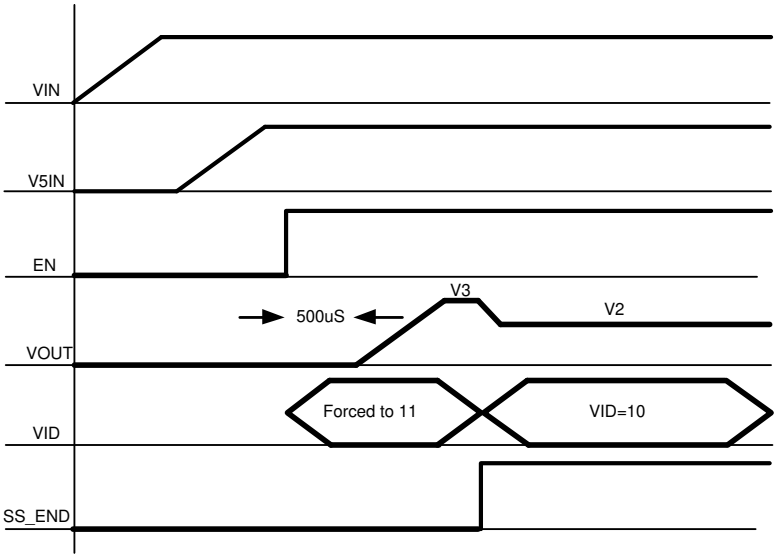

Figure 10. Power up Sequence

7.3.5 MODE Pin Configuration

MODE pin should be connected to V5IN pin.

7.3.6 Light-Load Operation

In auto-skip mode, the TPS51215A SMPS control logic automatically reduces its switching frequency to improve light-load efficiency. To achieve this intelligence, a zero cross detection comparator is used to prevent negative inductor current by turning off the low-side MOSFET. Equation 3 shows the boundary load condition of this skip mode and continuous conduction operation.

$$I_{LOAD(LL)} = \frac{(V_{IN} - V_{OUT})}{2 \times L_X} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (3)$$

7.3.7 Out-of-Bound Operation

When the output voltage rises to 8% above the target value, the out-of-bound operation starts. During the out-of-bound condition, the controller operates in forced PWM-only mode. Turning on the low-side MOSFET beyond the zero inductor current quickly discharges the output capacitor. During this operation, the cycle-by-cycle negative overcurrent limit is also valid. Once the output voltage returns to within regulation range, the controller resumes to auto-skip mode.

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Feature Description (continued)

7.3.8 Current Sensing and Overcurrent Protection

In order to provide both cost effective solution and good accuracy, TPS51215A supports MOSFET $R_{DS(on)}$ sensing. For $R_{DS(on)}$ sensing scheme, TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. In this scheme, TRIP terminal sources 10µA of I_{TRIP} current (at T_J = 25°C) and the trip level is set to 1/8 of the voltage across the R_{TRIP}. The inductor current is monitored by the voltage between the GND pin and the SW pin so that the SW pin is connected to the drain terminal of the low-side MOSFET. I_{TRIP} has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the sense resistor or the source terminal of the low-side MOSFET.

TPS51215A has cycle-by-cycle overcurrent limiting protection. The inductor current is monitored during the off-state and the controller maintains the off-state when the inductor current is larger than the overcurrent trip level. The overcurrent trip level, V_{OCTRIP}, is determined by Equation 4.

$$V_{OCTRIP} = R_{TRIP} \times \left(\frac{I_{TRIP}}{8} \right) \tag{4}$$

Because the comparison is made during the off-state, V_{OCTRIP} sets the valley level of the inductor current. The load current OCL level, I_{OCL}, can be calculated by considering the inductor ripple current.

Overcurrent limiting using $R_{DS(on)}$ sensing is shown in Equation 5.

$$I_{OCL} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{I_{IND(ripple)}}{2} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L_X} \times \frac{V_{OUT}}{f_{SW} \times V_{IN}} \tag{5}$$

where

- $I_{IND(ripple)}$ is inductor ripple current

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down.

7.3.9 Overvoltage and Undervoltage Protection

The TPS51215A sets the overvoltage protection (OVP) when VSNS voltage reaches a level 20% (typ) higher than the target voltage. When an OV event is detected, the controller changes the output target voltage to 0 V. This usually turns off DRVH and forces DRVL to be on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, DRVL is turned off and DRVH is turned on, for a minimum on-time.

After the minimum on-time expires, DRVH is turned off and DRVL is turned on again. This action minimizes the output node undershoot due to LC resonance. When the VSNS reaches 0 V, the driver output is latched as DRVH off, DRVL on.

The undervoltage protection (UVP) latch is set when the VSNS voltage remains lower than 68% (typ) of the REFIN voltage for 1 ms or longer. In this fault condition, the controller latches DRVH low and DRVL low and discharges the V_{OUT}. UVP detection function is enabled after 1.2 ms of SMPS operation to ensure startup.

To release the OVP and UVP latches, toggle EN or adjust the V5IN voltage down and up beyond the undervoltage lockout threshold.

7.3.10 V5IN Undervoltage Lockout Protection

TPS51215A has a 5-V supply undervoltage lockout protection (UVLO) threshold. When the V5IN voltage is lower than UVLO threshold voltage, typically 4.0 V, V_{OUT} is shut off. This is a non-latch protection.

7.3.11 Thermal Shutdown

TPS51215A includes an internal temperature monitor. If the temperature exceeds the threshold value, 140°C (typ), V_{OUT} is shut off. The state of V_{OUT} is open at thermal shutdown. This is a non-latch protection and the operation is restarted with soft-start sequence when the device temperature is reduced by 10°C (typ).

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7.4 D-CAP2 Control Mode

Figure 11 shows a simplified model of D-CAP2 mode architecture in the TPS51215A.

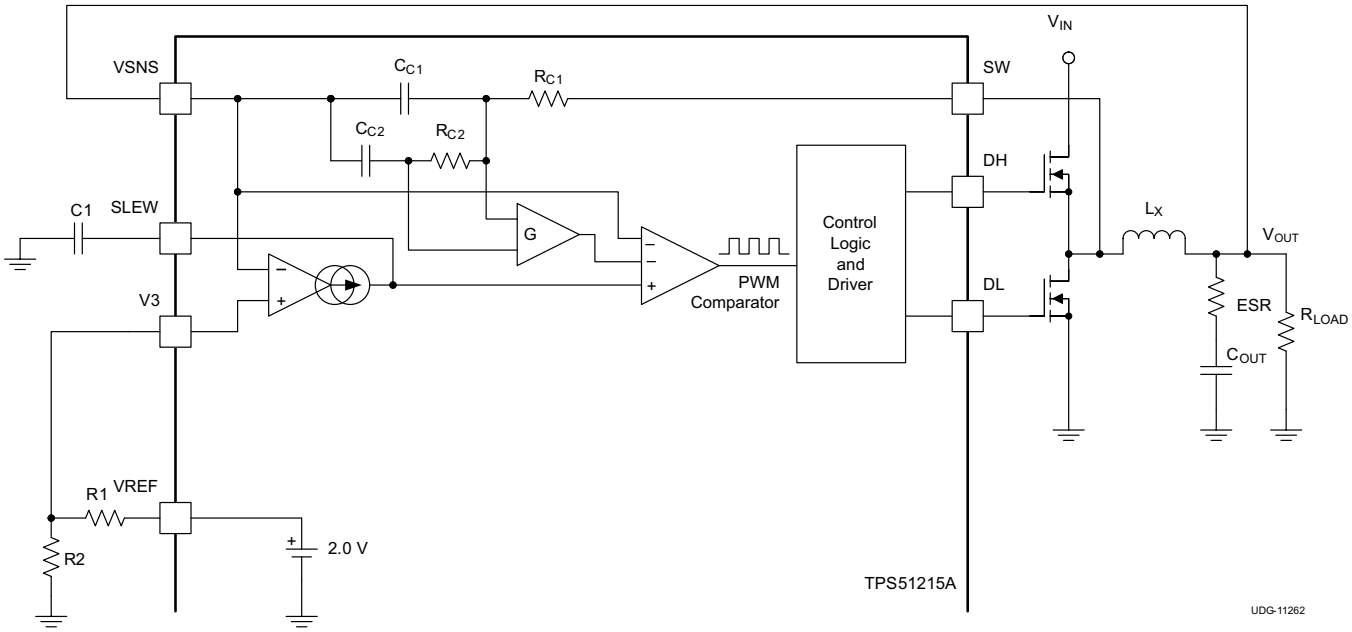

Figure 11. Simplified D-CAP2 Mode Architecture

When TPS51215A operates in D-CAP2 mode, it uses an internal phase compensation network (R_{C1}, R_{C2}, C_{C1} and C_{C2} and G) to work with very low ESR output capacitors such as multi-layer ceramic capacitors (MLCC) and POSCAP. The role of such network is to sense and scale the ripple component of the inductor current information and then use it in conjunction with the voltage feedback to achieve loop stability of the converter.

The switching frequency used for D-CAP2 mode is 600 kHz and it is generally recommended to have a unity gain crossover (f0) of 1/4 of the switching frequency, which is approximately 150 kHz for the purpose of this application.

Given the range of the recommended unity gain frequency, the power stage design is flexible, as long as Equation 6 is true.

$$\frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \leq \frac{1}{10} \times f_0 \tag{6}$$

When TPS51215A is configured in D-CAP2 mode, the overall loop response is dominated by the internal phase compensation network. The compensation network is designed to have two identical zeros at 7.7 kHz in the frequency domain, which serves the purpose of splitting the L-C double pole into one low frequency pole (same as the L-C double pole frequency) and one high-frequency pole (greater than the unity gain crossover frequency).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section describes two different applications for the TPS51215A controller. Design 1 is a 2-Bit VID $I_{CC(max)}$ = 30A, application for VCCIN_AUX application in Intel IMVP9 platform. Design 2 is a 1-Bit VID $I_{CC(max)}$ =10A, for VCCIO_1_2 in Intel RocketLake-S platform.

8.2 Typical Applications

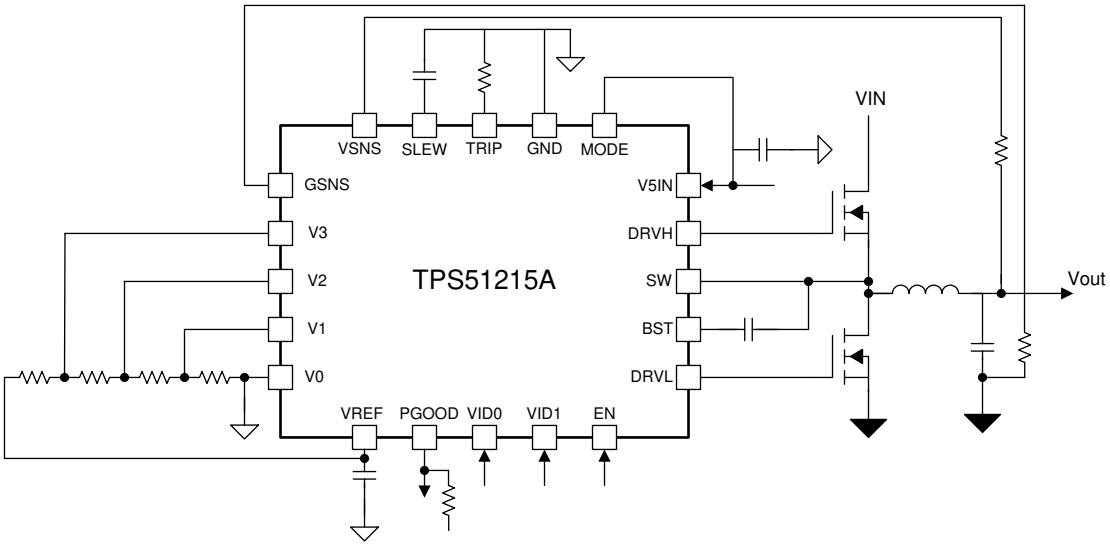

Figure 12. Typical 2-Bit VID Application

8.2.1 Design Requirements

The *Step One: Determine the Specifications* section and the *Step Two: Determine System Parameters* section itemize the system agent rail application requirements.

8.2.2 Detailed Design Procedure

The simplified design procedure creates VCCIN-AUX rail for IMVP9 Intel platform application using the TPS51215A controller.

8.2.2.1 Step One: Determine the Specifications

- V_{00} = 0 V
- V_{01} = 1.1 V
- V_{10} = 1.65 V
- V_{11} = 1.8 V
- $I_{CC(max)}$ = 30 A
- $I_{DYN(max)}$ = 12 A

8.2.2.2 Step Two: Determine System Parameters

The input voltage range and operating frequency are of primary interest.

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Typical Applications (continued)

In this example:

- 5.5 V ≤ V_{IN} ≤ 20 V
- f_{SW} = 600 kHz

8.2.2.3 Step Three: Determine Inductor Value and Choose Inductor

Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. In this example, use 25%:

I_{P-P} = 30 A × 0.4 = 12 A

At f_{SW} = 600 kHz with a 20-V input and a 1.8-V output:

$$L = \frac{(V_{OUT} - V_{IN}) \times T_{ON}}{I_{P-P}} = \frac{(V_{OUT} - V_{IN}) \times D \times T}{I_{P-P}} = \frac{(20\,V - 1.8\,V) \times \frac{1.8\,V}{20\,V} \times \frac{1}{600\,kHz}}{12\,A} \quad (7)$$

For this application, a 0.22-µH, 1.15-mΩ inductor from Cyntec with part number CMLE063T-R22MS is used.

8.2.2.4 Step Four: Set the Output Voltages

Set the output voltage levels. for V0, V1, V2 and V3 pins).

- VID 00, V0 = V_{SET1} = 0 V
- VID 10, V2 = V_{SET2} = 1.1 V
- VID 01, V1 = V_{SET3} = 1.65 V
- VID 11, V3 = V_{SET4} = 1.8 V

The resistor value:

- V_{REF} = 2 V
- R1 = 20 kΩ
- R2 = 15 kΩ
- R3 = 54.9 kΩ
- R4 = 110 kΩ
- R5 = 0Ω

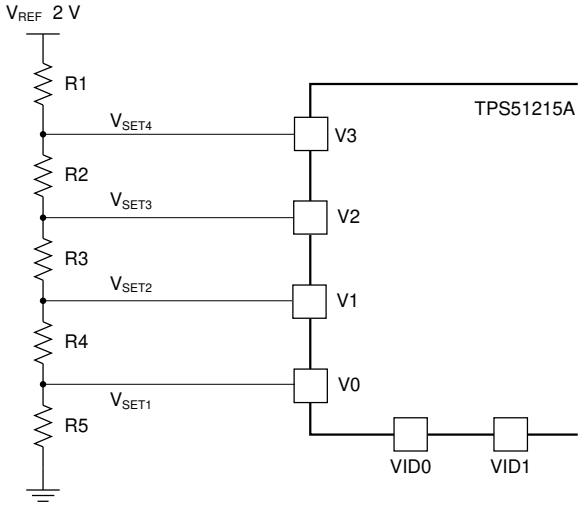

Figure 13. Setting the Output Voltage

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Typical Applications (continued)

8.2.2.5 Step Five: Calculate SLEW Capacitance

SLEW can be used to program the soft-start time and voltage transition timing. During soft-start operation, the current source used to program the SLEW rate is 4.5 µA (nominal). During VID transition, the current source is switched to a higher current of 45 µA.

In this design example, the requirement is to complete VID_00 to VID_11 transition within 120 µs, calculate the SLEW capacitance based on Equation 8.

$$C_{SLEW} = I \times \frac{dT}{dV} = 45\,\mu A \times \frac{120\,\mu s}{1.8\,V} = 3\,nF \tag{8}$$

For V_{OUT} = 1.8 V, the soft start timing based on C_{SLEW} is 1.2 ms.

The slower slew rate is desired to minimize large inductor current perturbation during startup and voltage transition, thus reducing the possibility of acoustic noise.

8.2.2.6 Step Six

TPS51215A uses a low-side on-resistance ($R_{DS(on)}$) sensing scheme. The TRIP pin sources 10 µA of current and the trip level is set to 1/8 of the voltage across the TRIP resistor (R_{TRIP}). The overcurrent trip level is determined by R_{TRIP} × (I_{TRIP} /8). Because the comparison is done during the off state, the trip voltage sets the valley current. The load current can be calculated by considering the inductor ripple current.

$$R_{TRIP} = \frac{8 \times \left(I_{OCL} - \left(\frac{(V_{IN} - V_{OUT})}{(2 \times Lx)} \right) \times \frac{(V_{OUT})}{(f_{SW} \times V_{IN})} \right) \times R_{DS(on)}}{I_{TRIP}} \tag{9}$$

where

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- f_{SW} is the switching frequency (600 kHz)
- $R_{DS(on)}$ is the low-side FET on resistance
- I_{TRIP} is the trip current, 10 µA (nominal)
- Lx is the output inductance

8.2.2.7 Step Seven: Determine the Output Capacitance

The switching frequency for D-CAP2 mode is 600 kHz and it is generally recommend to have a unity gain crossover (f_0) of 1/4 of the switching frequency, which is approximately 150kHz for the purpose of this application.

Given the range of the recommended unity gain frequency, the power stage design is flexible, as long as the LC double pole frequency is less than 10% of f_0.

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \le \frac{1}{10} \times f_0 = 9\,kHz \Leftrightarrow 12\,kHz \tag{10}$$

As long as the LC double pole frequency is designed to be less than 1/10 of f_0, the internal compensation network provides sufficient phase boost at the unity gain crossover frequency in order for the converter to be stable with enough margin.

When the ESR frequency of the output bulk capacitor is in the vicinity of the unity gain crossover frequency of the loop, additional phase boost is achieved. This applies to POSCAP and/or SPCAP output capacitors.

When the ESR frequency of the output capacitor is beyond the unity gain crossover frequency of the loop, no additional phase boost is achieved. This applies to low/ultra low ESR output capacitors, such as MLCCs.

Equation 11 and Equation 12 can be used to estimate the amount of capacitance needed for a given dynamic load step/release. Note that there are other factors that may impact the amount of output capacitance for a specific design, such as ripple and stability. Equation 11 and Equation 12 are used only to estimate the transient requirement, the result should be used in conjuction with other factors of the design to determine the necessary output capacitance for the application.

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Typical Applications (continued)

$$C_{OUT(min\_under)} = \frac{L \times \left(\Delta I_{LOAD(max)}\right)^2 \times \left(\frac{V_{OUT} \times t_{SW}}{V_{IN(min)}} + t_{MIN(off)}\right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)}}\right) \times t_{SW} - t_{MIN(off)}\right) \times V_{OUT}} \quad (11)$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)}\right)^2}{2 \times \Delta V_{LOAD(release)} \times V_{OUT}} \quad (12)$$

Equation 11 and Equation 12 calculate the minimum C_{OUT} for meeting the transient requirement, which is 480 µF assuming ±7.5% voltage allowance for load step and release.

8.2.2.8 Step Eight: Select Decoupling and Peripheral Components

For the TPS51215A, peripheral capacitors use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

- V5IN decoupling ≥2.2 µF, ≥ 6.3 V
- VREF decoupling 0.22 µF to 1 µF, ≥ 4 V
- Bootstrap capacitors ≥ 0.1 µF, ≥ 10 V
- Pull-up resistors on PGOOD, 100 kΩ

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Typical Applications (continued)

8.2.3 Application Examples

8.2.3.1 Design 1: 2-Bit VID $I_{CC(max)}$ = 30 A, DCAP2 600-kHz Application for VCCIN_AUX in Intel TigerLake platform

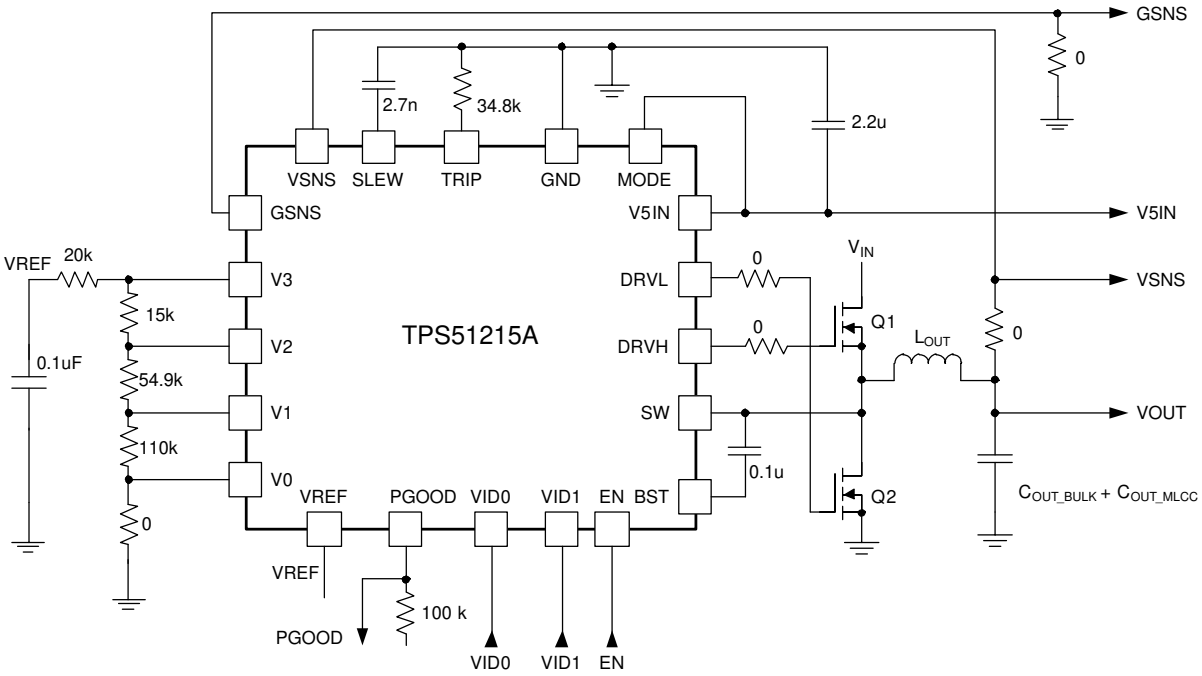

Figure 14. Application Circuit for Design 1

Table 1. VID Table for Design 1

VID1	VID0	OUTPUT VOLTAGE (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table 2. List of Materials for Design 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN} (not shown)	6	10 µF, 25 V	TDK	C3216X5R1V106M160AB
C_{OUT_BULK}	1	220 µF, 6.3 V, 5 mΩ	Panasonic	6TPF220M5L
C_{OUT_MLCC}	12	22 µF, 6.3 V	Murata	GRM21BR60J226ME39L
L_{OUT}	1	0.22 µH, 38 A, 1.15 mΩ	Cyntec	CMLE063T-R22MS-68
Q1 Q2	1	30 V, 45A	Texas Instruments	CSD87355Q5D

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8.2.3.2 Design 2: 2-Bit VID, $I_{CC(max)}$ = 10 A, for VCCIO_1_2 in Intel RocketLake - S platform

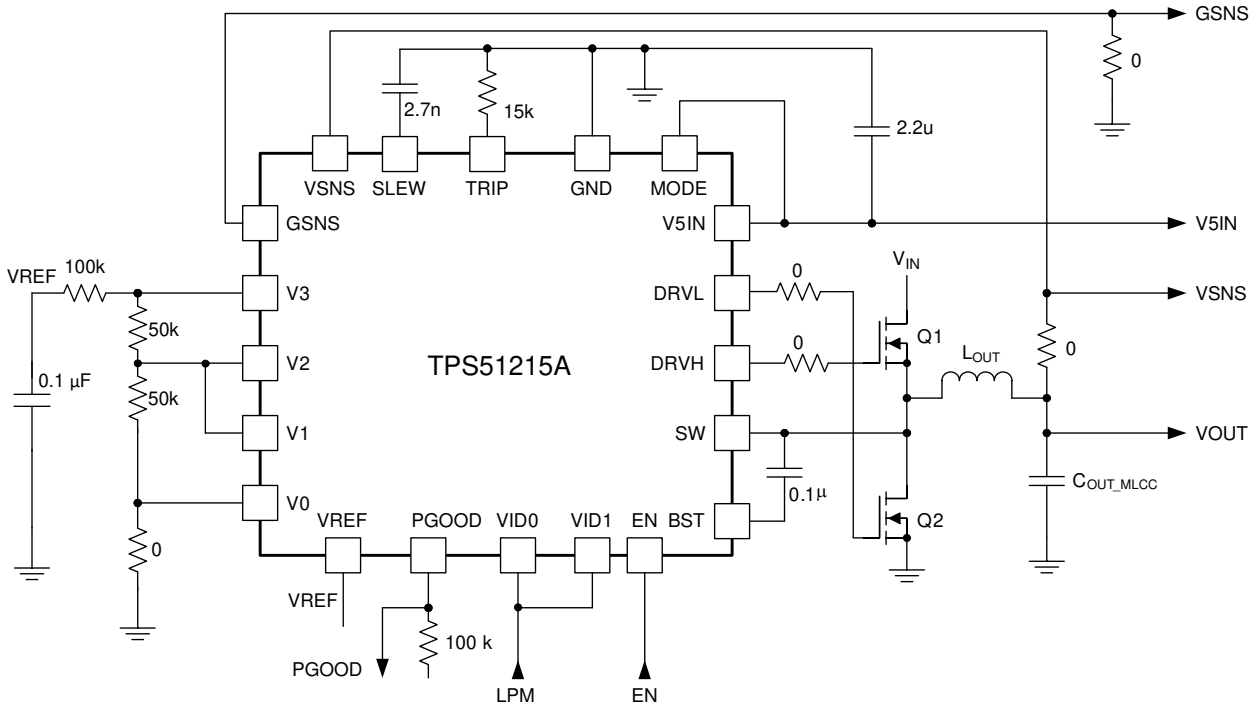

Figure 15. Application Circuit for Design 2

Table 3. VID Table for Design 2

VID1	VID0	OUTPUT VOLTAGE (V)
0	0	0
0	1	Not Used
1	0	Not Used
1	1	1.0

Table 4. List of Materials for Design 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN} (not shown)	3	10 µF, 25 V	TDK	C3216X5R1V106M160AB
C_{OUT_MLCC}	6	22 µF, 6.3 V	Murata	GRM21BR60J226ME39L
L_{OUT}	1	0.47 µH, 25 A,2.9 mΩ	Cyntec	CMLE063T-R47MS-68
Q1 Q2	1	30 V, 45A	Texas Instruments	CSD87355Q5D

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8.2.4 Application Curves of Design 1

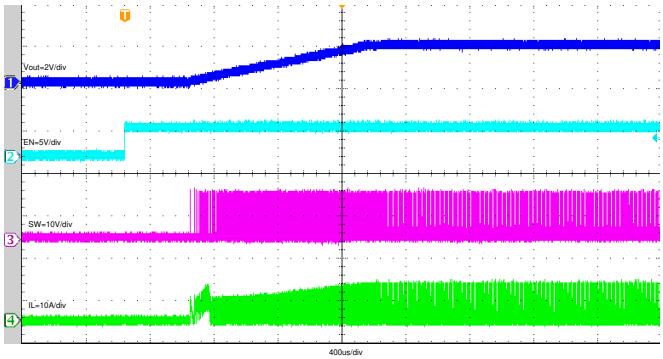

Figure 16. Start Up Relative to EN Rising

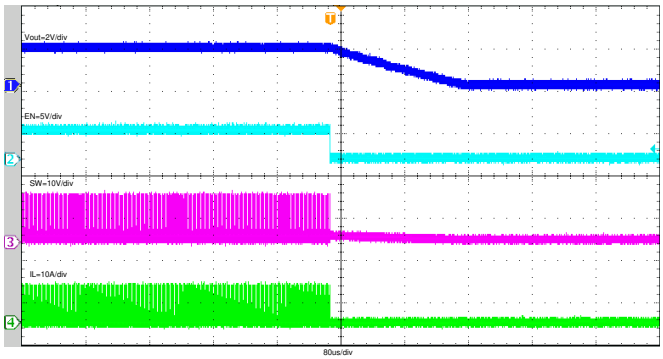

Figure 17. Shut Down Relative to EN Falling

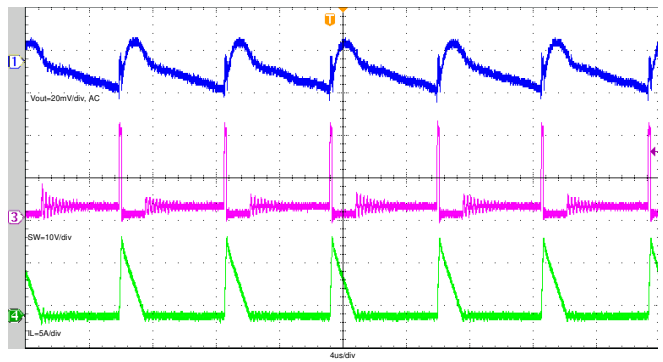

Figure 18. Steady State I_{OUT} = 1 A

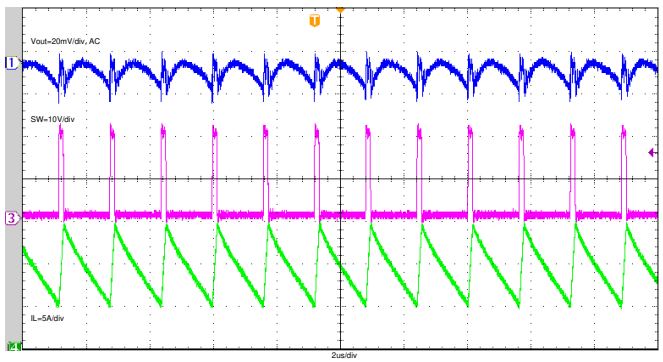

Figure 19. Steady State I_{OUT} = 10 A

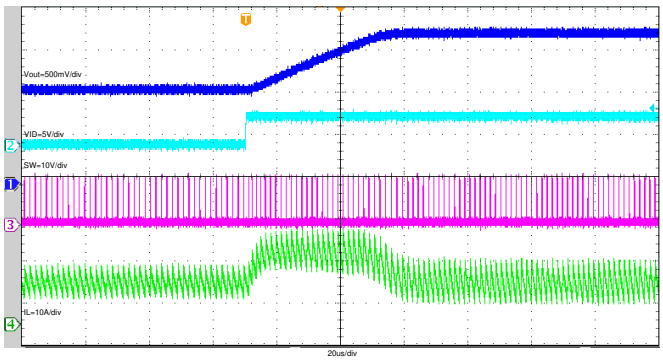

Figure 20. VID Transient, VID = 01 to 11, V_{OUT} = 1.1 V to 1.8 V

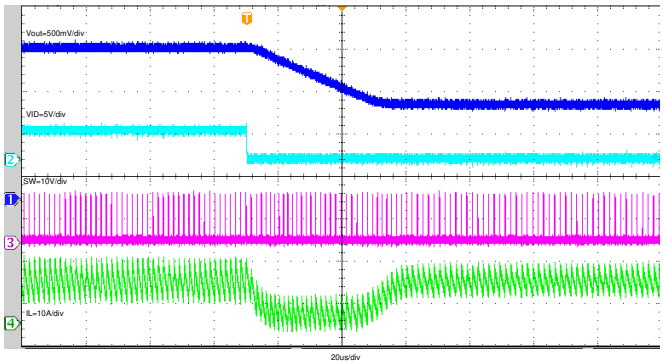

Figure 21. VID Transient, VID = 11 to 01, V_{OUT} = 1.8 V to 1.1 V

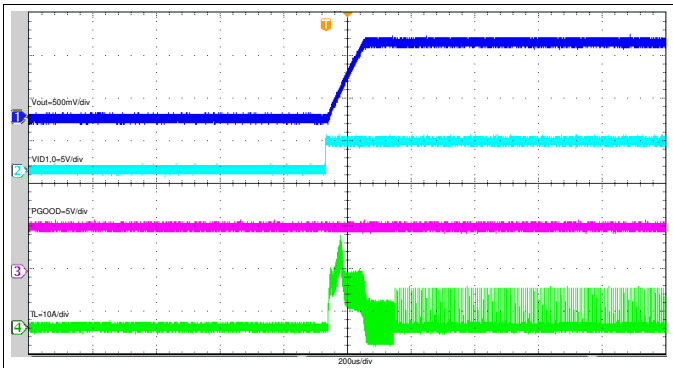

Figure 22. Low Power Mode Exit V_{OUT} = 0 V to 1.8 V

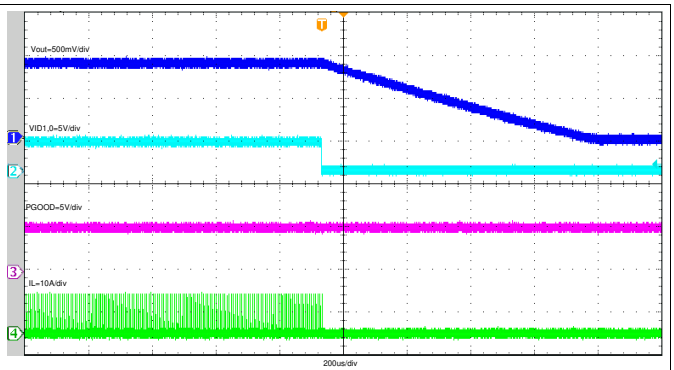

Figure 23. Low Power Mode Enter V_{OUT} = 1.8 V to 0 V

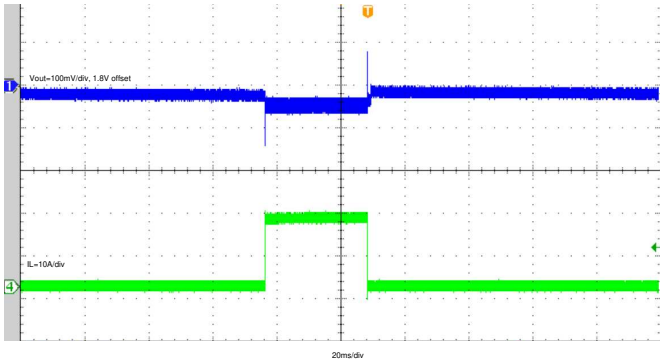

Figure 24. Load Transient, I_{OUT} = 0 A to 16 A, T_r = T_f = 1 µs

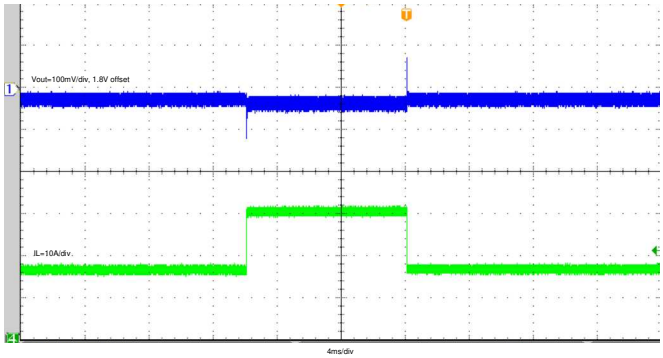

Figure 25. Load Transient, I_{OUT} = 16 A to 30 A, T_r = T_f = 1 µs

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9 Power Supply Recommendations

The TPS51215A is intended to be powered by a well regulated dc voltage. and input voltage is 3 V to 28 V. Input supply must be appropriate for th desired output current. If the input voltage supply is located for from the part, come additional input buck capacitance is recommended. Typical value is 50uF and 0.1uF Vin capacitor is needed.

- VIN is the power of input for buck, V5IN is power supply for internal control logic.
- EN is high before VIN has the power input, V5IN power supply must be provided after or same time with VIN, otherwise the output will be latched, this latch can be recovered by toggling the EN pin or re-power up the V5IN
- EN is low before VIN and V5IN have the power input, then there is no power supply input sequence requirement

10 Layout

10.1 Layout Guidelines

Certain issues must be considered before designing a layout using the TPS51215A.

- V_{IN} capacitor(s), V_{OUT} capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VSNS, SLEW, MODE, V0, V1, V2, V3, VREF and TRIP should be placed away from high-voltage switching nodes such as SW, DH, DL or BST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components. Need to placed close to the part and minimized length of routing trace.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - Loop #1. The most important loop to minimize the area of is the path from the V_{IN} capacitor(s) through the high and low-side MOSFETs, and back to the capacitor(s) through ground. Connect the negative node of the V_{IN} capacitor(s) and the source of the low-side MOSFET at ground as close as possible. (Refer to loop #1 of Figure 26)
  - Loop #2. The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of V_{OUT} capacitor(s) at ground as close as possible. (Refer to loop #2 of Figure 26)
  - Loop #3. The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5 capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND, and back to source of the low-side MOSFET through ground. Connect negative node of V5 capacitor, source of the low-side MOSFET and PGND at ground as close as possible. (Refer to loop #3 of Figure 26)
- VSNS can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side. For additional noise filtering, insert a 10-Ω, 1-nF, R-C filter between the sense point and the VSNS pin. Connect GSNS to ground return point at the load device or the general ground plane/layer. VSNS and GSNS can be used for the purpose of remote sensing across the load device, however, care must be taken to minimize the routing trace to prevent excess noise injection to the sense lines.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as SW node, which connects to the source of the switching MOSFET, the drain of the rectifying MOSFET and the high-voltage side of the inductor, should be as short and wide as possible.
- In order to effectively remove heat from the package, prepare the thermal land and solder to the package

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Layout Guidelines (continued)

thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps to dissipate heat Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation.

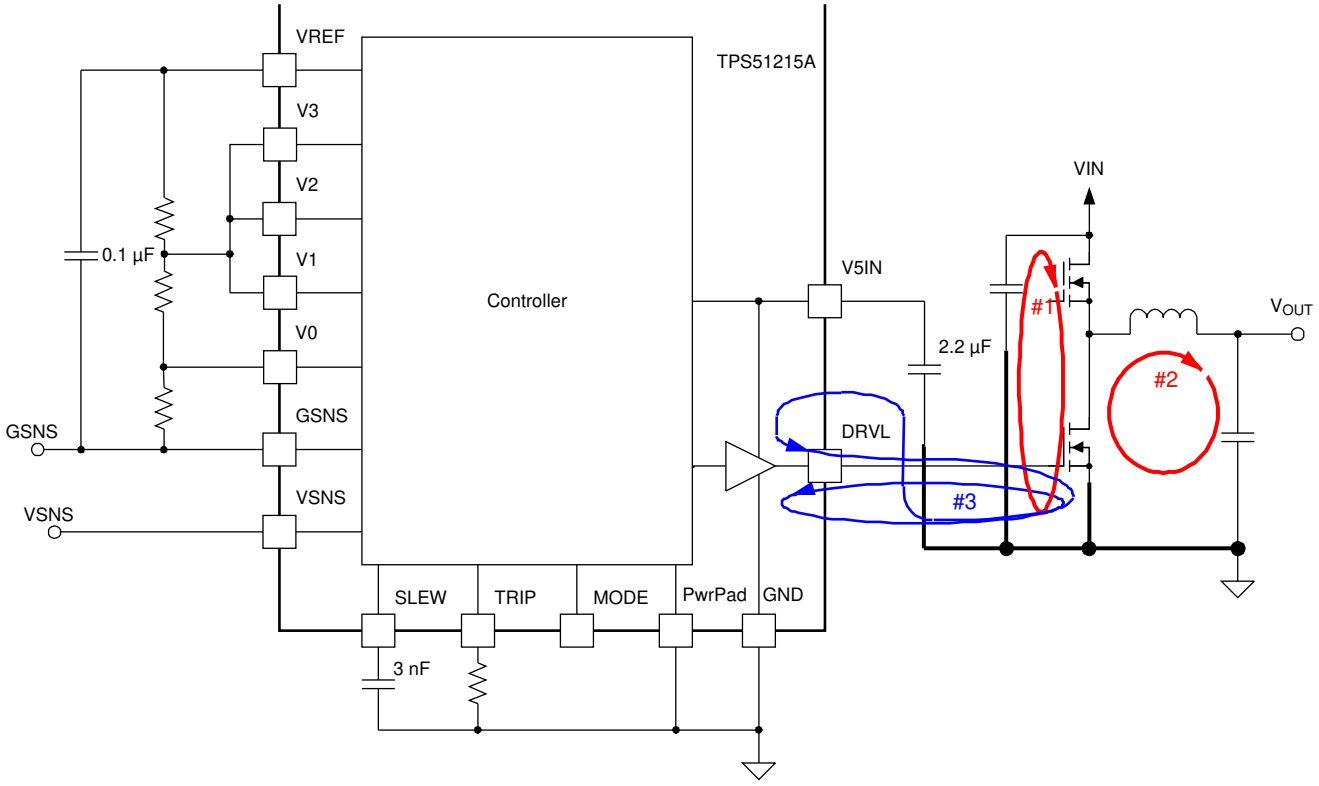

Figure 26. DC/DC Converter Ground System

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

D-CAP2, E2E are trademarks of Texas Instruments.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS51215ARUKR	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	51215A
TPS51215ARUKR.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	51215A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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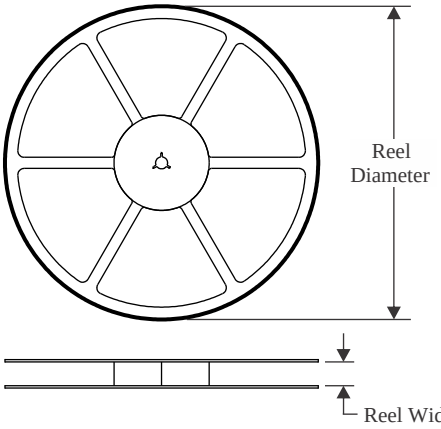
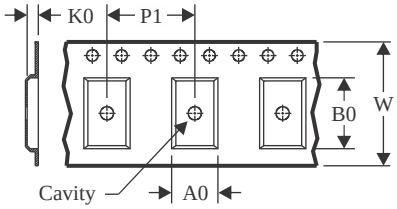
TAPE AND REEL INFORMATION

REEL DIMENSIONS

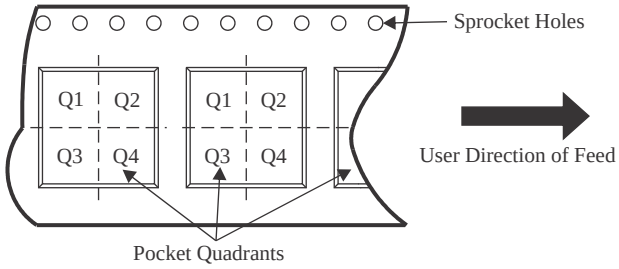


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

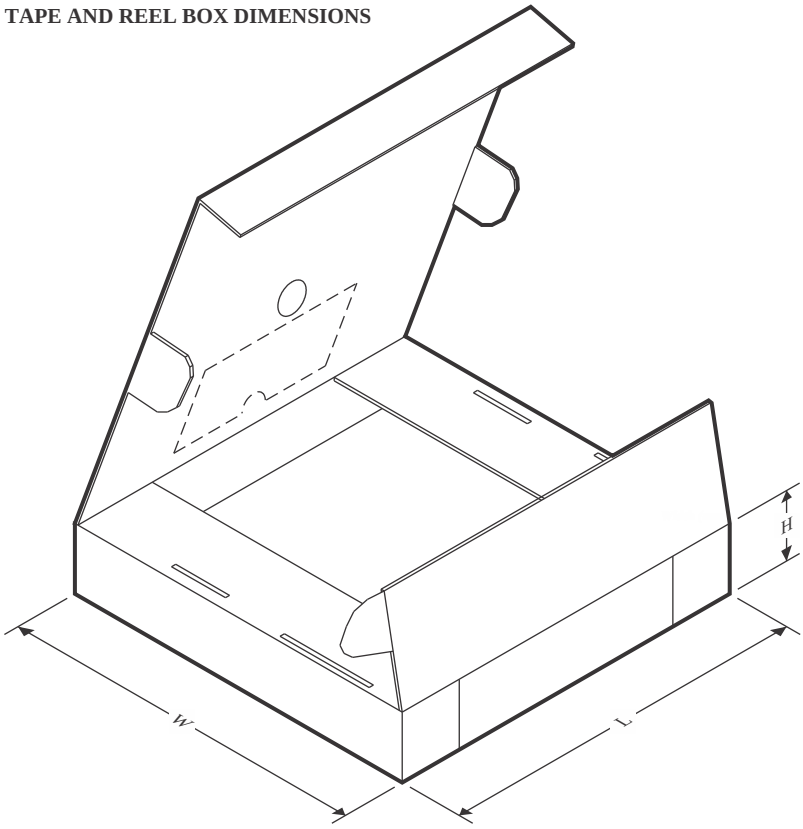
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51215ARUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51215ARUKR	WQFN	RUK	20	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

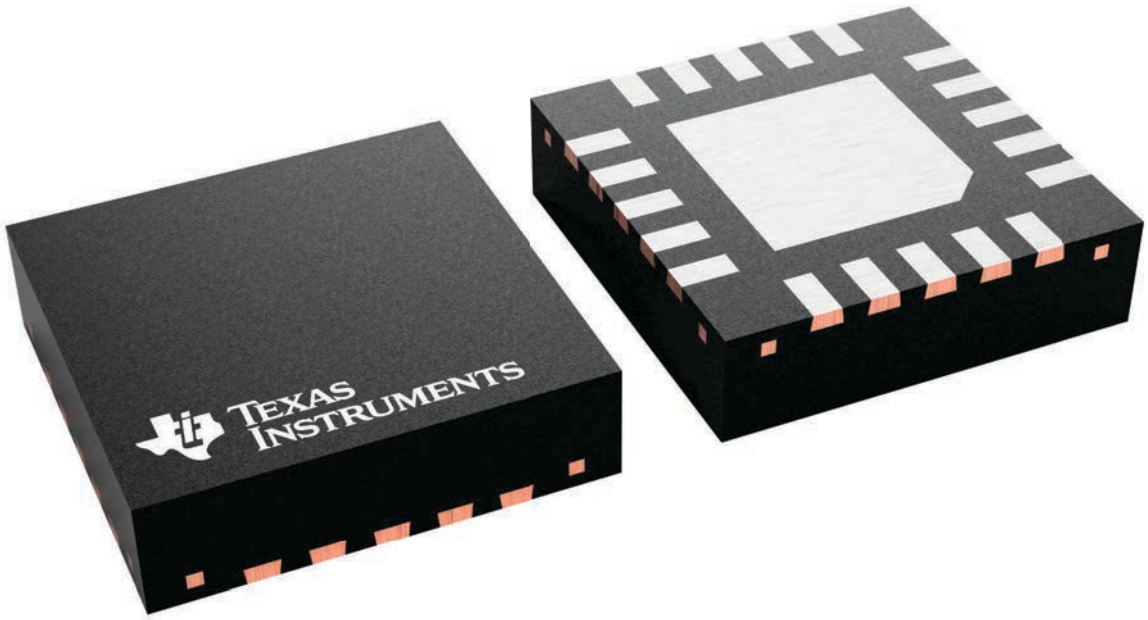
RUK 20

WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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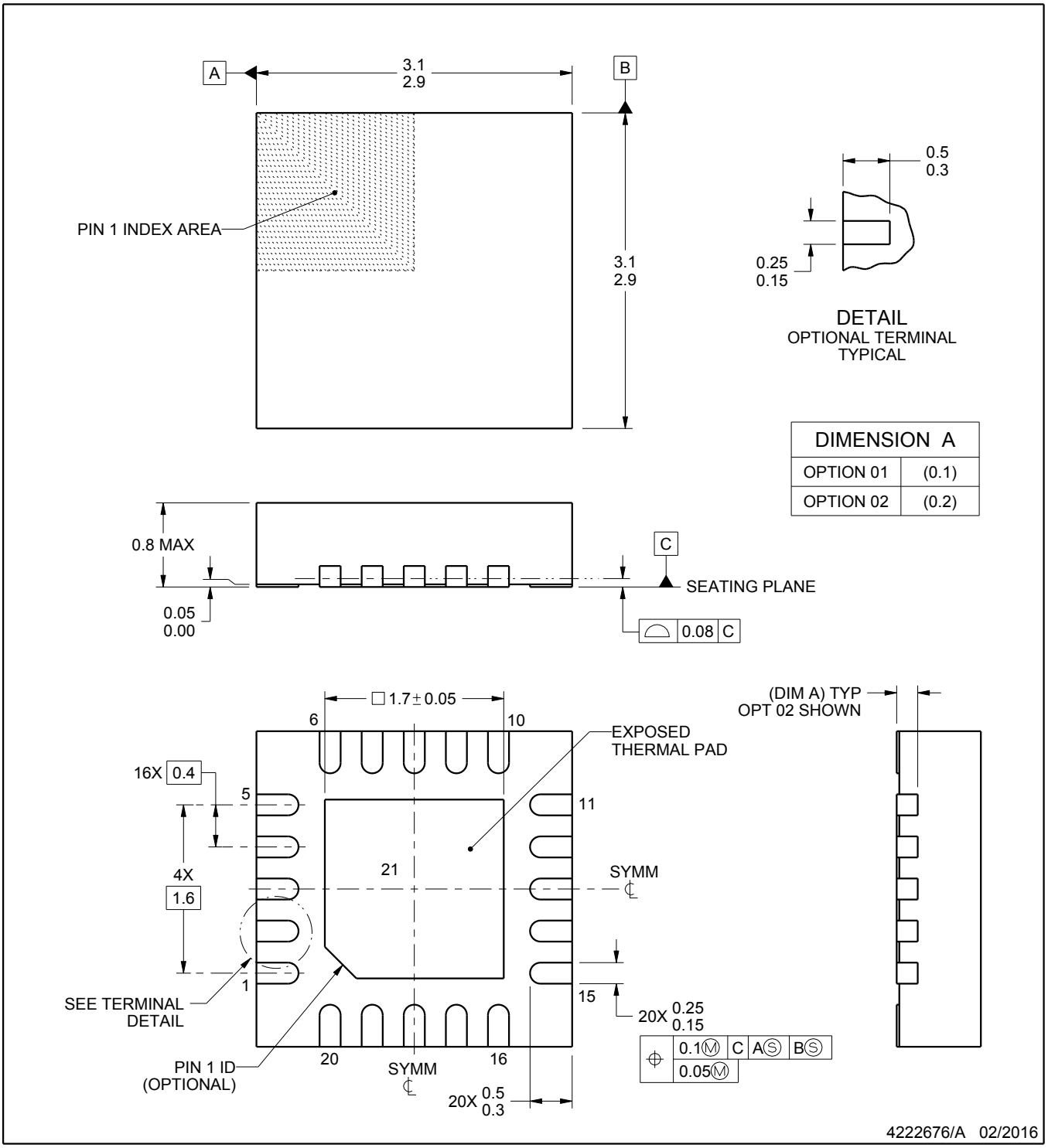
PACKAGE OUTLINE

RUK0020B

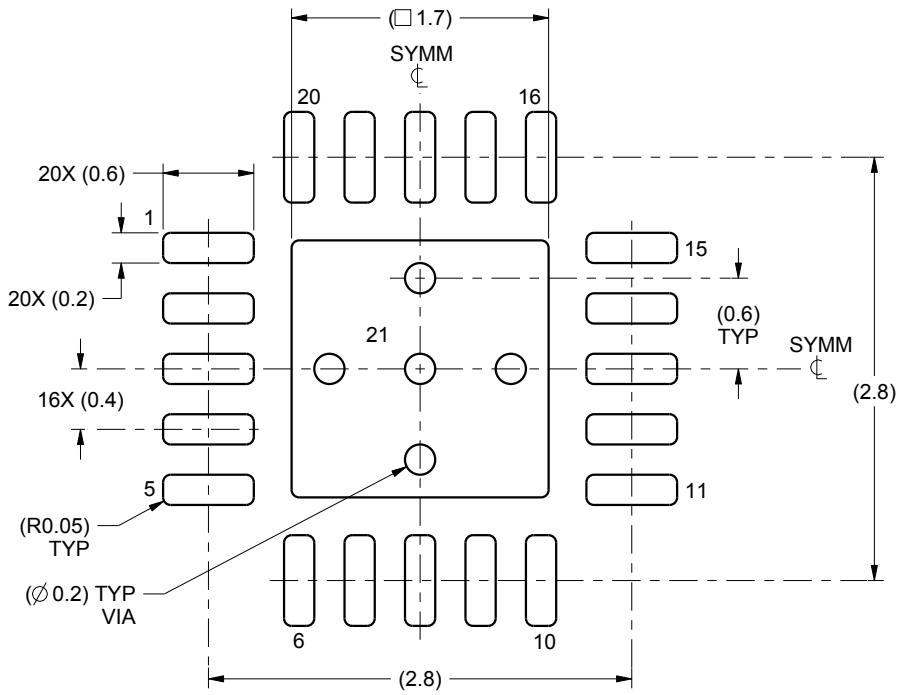
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

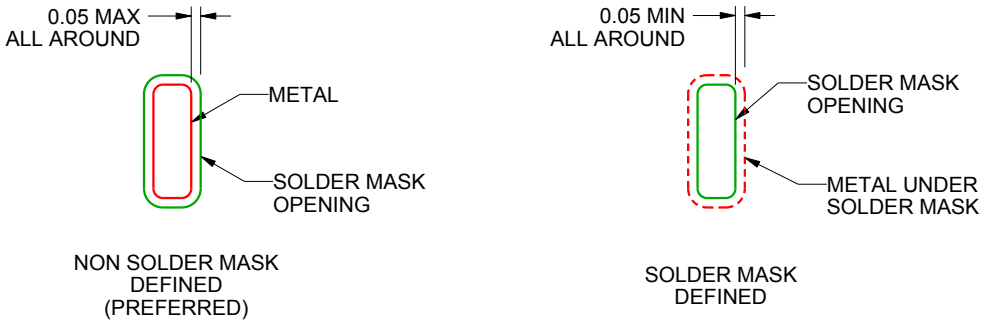


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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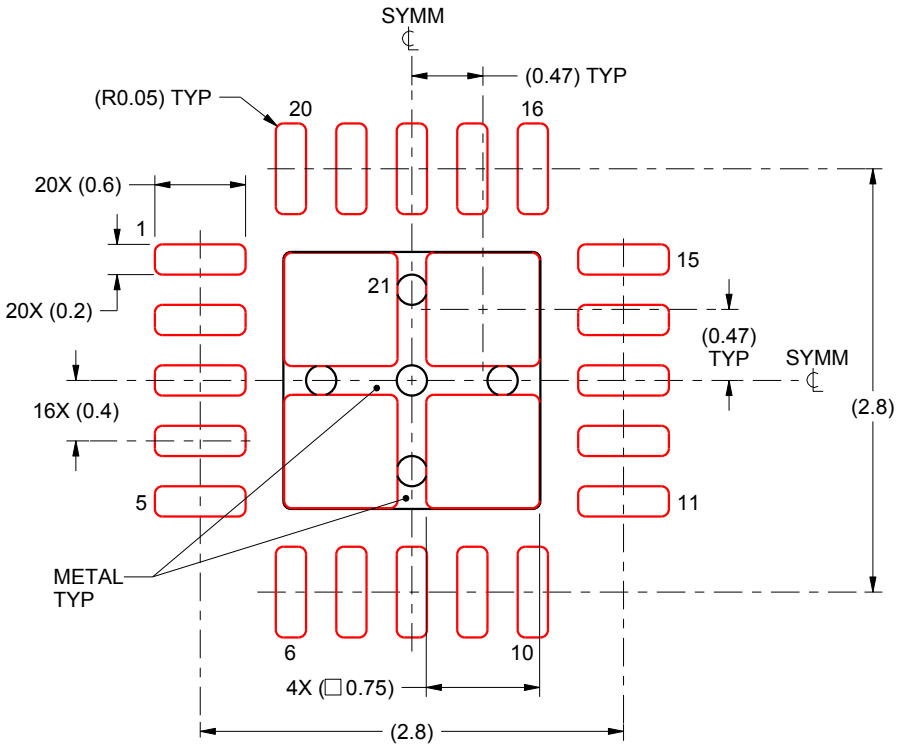
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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