TEXAS INSTRUMENTS

TPS3808G01-Q1, TPS3808G12-Q1, TPS3808G125-Q1, TPS3808G15-Q1
TPS3808G18-Q1, TPS3808G30-Q1, TPS3808G33-Q1, TPS3808G50-Q1

SBVS085J – JANUARY 2007 – REVISED JUNE 2017

TPS3808Gxx-Q1 Low-Quiescent-Current Programmable-Delay Supervisory Circuit

1 Features

- Qualified for Automotive Applications
- Power-On Reset Generator With Adjustable Delay Time: 1.25 ms to 10 s
- Very Low Quiescent Current: 2.4 μA Typical
- High Threshold Accuracy: 0.5% Typical
- Fixed Threshold Voltages for Standard Voltage Rails From 1.2 V to 5 V and Adjustable Voltage Down to 0.4 V Are Available
- Manual Reset ($\overline{MR}$) Input
- Open-Drain $\overline{RESET}$ Output
- Temperature Range: –40°C to +125°C
- Small SOT-23 Package and WSON Package (TPS3808G01QDRVRQ1 only)

2 Applications

- DSP or Microcontroller Applications
- FPGA and ASIC Applications
- Automotive Vision
- Automotive Radar

3 Description

The TPS3808Gxx-Q1 microprocessor supervisory circuits monitor system voltages from 0.4 V to 5 V, asserting an open-drain $\overline{RESET}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{MR}$) pin drops to a logic low. The $\overline{RESET}$ output remains low for the user-adjustable delay time after the SENSE voltage and $\overline{MR}$ return above their thresholds.

The TPS3808Gxx-Q1 device uses a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3$ V. The reset delay time can be set to 20 ms by disconnecting the C_T pin, 300 ms by connecting the C_T pin to V_{DD} using a resistor, or can be user-adjusted from 1.25 ms to 10 s by connecting the C_T pin to an external capacitor. The TPS3808Gxx-Q1 has a very low typical quiescent current of 2.4 μA, so it is well suited for battery-powered applications. The device is available in a small SOT-23 package (one option available in WSON) and is fully specified over a temperature range of –40°C to +125°C (T_J).

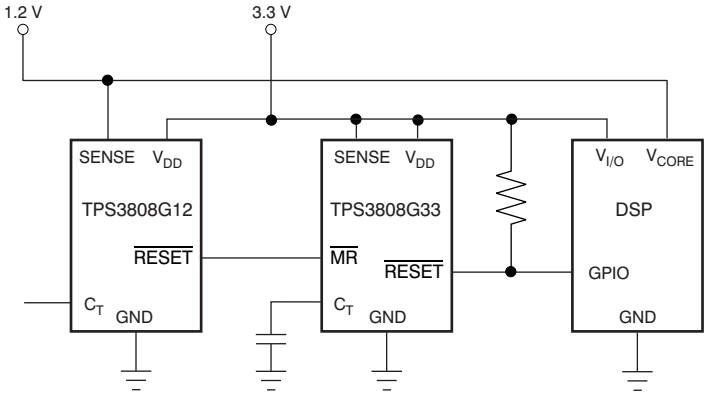
For more information about TI's voltage supervisor portfolio, visit the Supervisor and Reset IC Overview Page page.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3808Gxx-Q1	SOT-23 (6)	2.90 mm × 1.60 mm
	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (June 2015) to Revision J — **Page**

- Added column for WSON pins ... 3
- Changed unit for last row of t_d row in *Timing Requirements* from "ms" to "s" and "TYP" to "NOM" in middle unit column ... 6

Changes from Revision H (June 2012) to Revision I — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision G (November, 2010) to Revision H — **Page**

- Changed I_{SENSE} from µA to nA ... 5

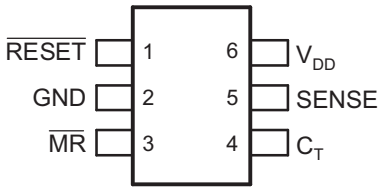
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5 Device Comparison Table

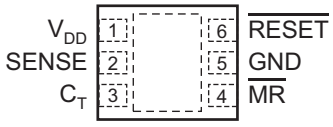
ORDERABLE PART NUMBER	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V_{IT})
TPS3808G01QDRVRQ1	Adjustable	0.405 V
TPS3808G01QDBVRQ1		
TPS3808G12QDBVRQ1	1.2 V	1.12 V
TPS3808G125QDBVRQ1	1.25 V	1.16 V
TPS3808G15QDBVRQ1	1.5 V	1.4 V
TPS3808G18QDBVRQ1	1.8 V	1.67 V
TPS3808G30QDBVRQ1	3 V	2.79 V
TPS3808G33QDBVRQ1	3.3 V	3.07 V
TPS3808G50QDBVRQ1	5 V	4.65 V

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



DRV Package
6-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
C_T	4	3	I	Reset period programming pin. Connecting this pin to VDD through a 40-kΩ to 200-kΩ resistor or leaving it open results in fixed delay times (see *Electrical Characteristics*). Connecting this pin to a ground referenced capacitor ≥ 100 pF gives user-programmable delay time. See the *Selecting the Reset Delay Time* for more information.
GND	2	5	—	Ground
$\overline{MR}$	3	4	I	Manual reset. Driving this pin low asserts $\overline{RESET}$. $\overline{MR}$ is internally tied to V_{DD} by a 90-kΩ pullup resistor.
$\overline{RESET}$	1	6	O	Reset. This is an open-drain output that is driven to a low impedance state when $\overline{RESET}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{MR}$ pin is set to a logic low). $\overline{RESET}$ remains low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{MR}$ is set to a logic high. A pullup resistor from 10 kΩ to 1 MΩ must be used on this pin and allows the reset pin to attain voltages higher than V_{DD}.
SENSE	5	2	I	Voltage sense. This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage (V_{IT}), $\overline{RESET}$ is asserted.
V_{DD}	6	1	I	Supply voltage. It is good analog design practice to place a 0.1-μF ceramic capacitor close to this pin.
Thermal Pad	—	Pad	—	Thermal pad; connect to ground plan to enhance thermal performance of the package.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Input voltage	–0.3	7	V
V_{CT}	C_T voltage	–0.3	(V_{DD} + 0.3)	V
V_{MR}, V_{RESET}, V_{SENSE}	$\overline{MR}$, $\overline{RESET}$, SENSE voltage	–0.3	7	V
I_{RESET}	$\overline{RESET}$ pin current		5	mA
T_J	Operating junction temperature(2)	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electric Characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Due to the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
TPS3808G125QDBVRQ1 IN SOT-23 PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	
		Machine Model (MM)	±50	
TPS3808GXX-Q1 IN SOT-23 PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	
TPS3808G01QDRVRQ1 IN SON PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	
		Machine Model (MM)	±50	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{DD} input supply	1.8		6.5	V
V_{SENSE} SENSE pin voltage	0		V_{DD}	V
$\overline{MR}$ Manual reset pin voltage	0		V_{DD}	V

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7.4 Thermal Information

THERMAL METRIC[1]		TPS3808Gxx-Q1		UNIT
		DBV (SOT-23)	DRV (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.9	178.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	117.8	95.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.8	135	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.9	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	136.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	7.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

1.8 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = –40°C to +125°C) (unless otherwise noted), typical values at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.8		6.5	V
I_{DD}	Supply current (into V_{DD} pin)	V_{DD} = 3.3 V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, C_T open			2.4	5	µA
		V_{DD} = 6.5 V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, C_T open			2.7	6	
V_{OL}	Low-level output voltage	1.3 V ≤ V_{DD} < 1.8 V, I_{OL} = 0.4 mA				0.3	V
		1.8 V ≤ V_{DD} ≤ 6.5 V, I_{OL} = 1 mA				0.4	
	Power-up reset voltage[1]	V_{OL} (max) = 0.2 V, I $\overline{RESET}$ = 15 µA				0.8	V
V_{IT}	Negative-going input threshold accuracy	TPS3808G01-Q1		–2%	±1%	2%	
		V_{IT} ≤ 3.3 V		–1.5%	±0.5%	1.5%	
		3.3 V < V_{IT} ≤ 5 V		–2%	±1%	2%	
		V_{IT} ≤ 3.3 V	–40°C < T_J < 85°C	–1.25%	±0.5%	1.25%	
		3.3 V < V_{IT} ≤ 5 V		–1.5%	±0.5%	1.5%	
V_{HYS}	Hysteresis on V_{IT} pin	TPS3808G01-Q1			1.5	3	%V_{IT}
		–40°C < T_J < 85°C			1	2	
					1	2.5	
$R_{\overline{MR}}$	$\overline{MR}$ internal pullup resistance	V_{SENSE} = V_{IT}		70	90		kΩ
I_{SENSE}	Input current at SENSE pin	TPS3808G01-Q1		–25		25	nA
		V_{SENSE} = 6.5 V			1.7		µA
I_{OH}	$\overline{RESET}$ leakage current	V $\overline{RESET}$ = 6.5 V, $\overline{RESET}$ not asserted				300	nA
C_{IN}	Input capacitance, any pin	C_T pin	V_{IN} = 0 V to V_{DD}		5		pF
		Other pins	V_{IN} = 0 V to 6.5 V		5		
V_{IL}	$\overline{MR}$ logic low input			0		0.3 V_{DD}	V
V_{IH}	$\overline{MR}$ logic high input			0.7 V_{DD}		V_{DD}	V

(1) Power-up reset voltage is the lowest supply voltage (V_{DD}) at which $\overline{RESET}$ becomes active ($t_{rise(VDD)}$ ≥ 15 µs/V).

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7.6 Timing Requirements

				MIN	NOM	MAX	UNIT
t_d	$\overline{\text{RESET}}$ delay time	C_T = Open	See Figure 1	12	20	28	ms
		C_T = V_{DD}		180	300	420	
		C_T = 100 pF		0.75	1.25	1.75	
		C_T = 180 nF		0.7	1.2	1.7	s
t_{pHL}	Propagation delay	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		150		ns
	High-level to low-level $\overline{\text{RESET}}$ delay	$\overline{\text{SENSE}}$ to $\overline{\text{RESET}}$	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		µs
t_w	Maximum transient duration	SENSE	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		µs
		$\overline{\text{MR}}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		0.001		

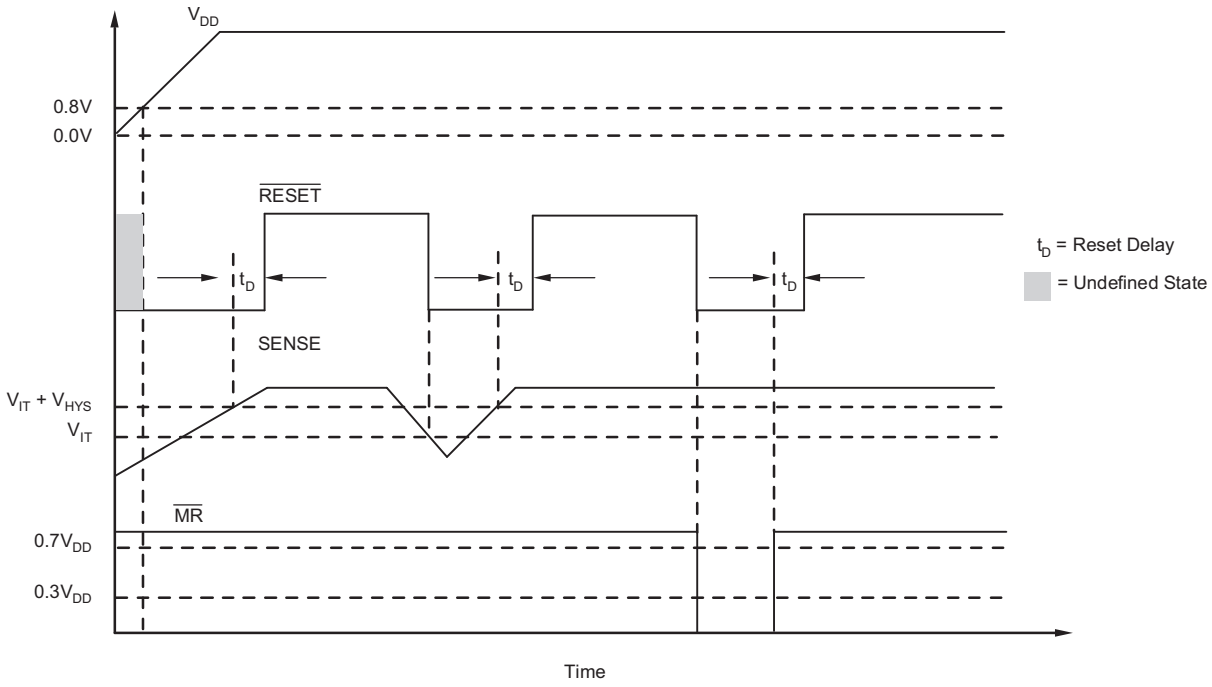


Figure 1. $\overline{\text{MR}}$ and SENSE Reset Timing Diagram

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7.7 Typical Characteristics

At T_J = 25°C, V_{DD} = 3.3 V, R_{LRESET} = 100 kΩ, and C_{LRESET} = 50 pF (unless otherwise noted)

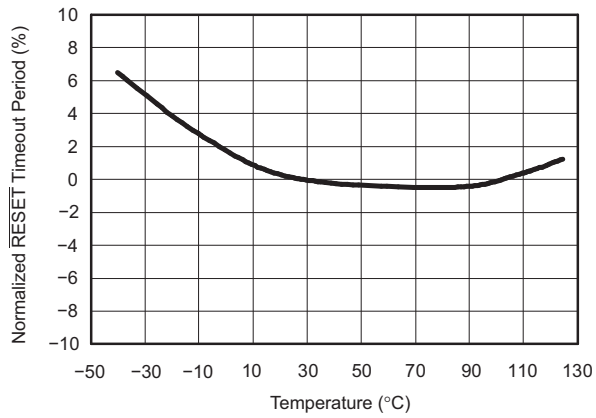


Figure 2. Normalized $\overline{\text{RESET}}$ Time-out Period vs Temperature (C_T = Open, C_T = V_{DD}, C_T = Any)

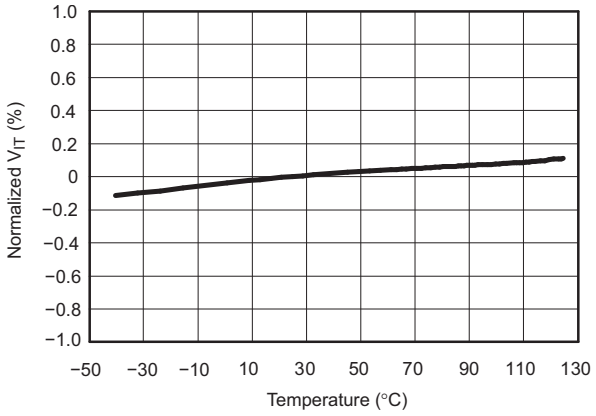


Figure 3. Normalized Sense Threshold Voltage (V_{IT}) vs Temperature

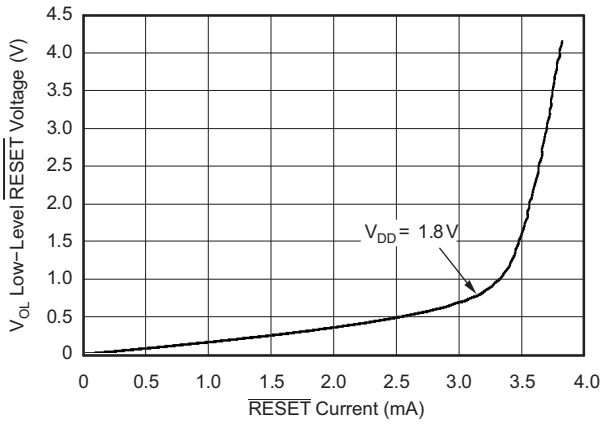


Figure 4. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current

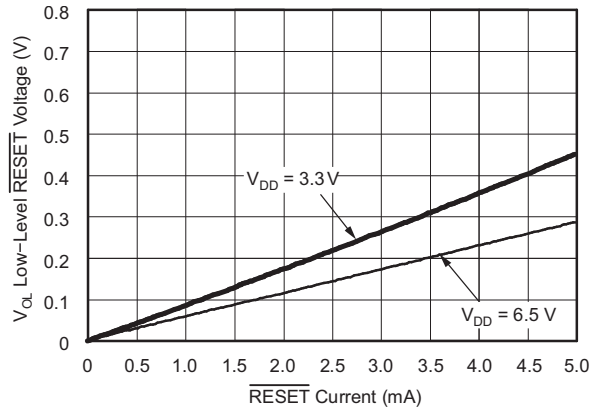


Figure 5. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current

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8 Detailed Description

8.1 Overview

The TPS3808Gxx-Q1 devices are low-current supervisory circuits used to monitor system voltages ranging from 0.4 V to 5 V. The devices assert an active low, open-drain RESET signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin is asserted to a logic low. The RESET output remains low for the user-adjustable delay time after the SENSE voltage and MR return above their thresholds. The devices are also designed to be immune to short negative transients on the SENSE pin. The reset delay time can be configured by using the C_T pin. The delay can be configured to 20 ms by leaving the C_T pin floating, it can be configured to 300 ms by connecting the C_T pin to V_{DD} using a resistor, or can be configured from 1.25 ms to 10 s by connecting the C_T pin to an external capacitor.

8.2 Functional Block Diagrams

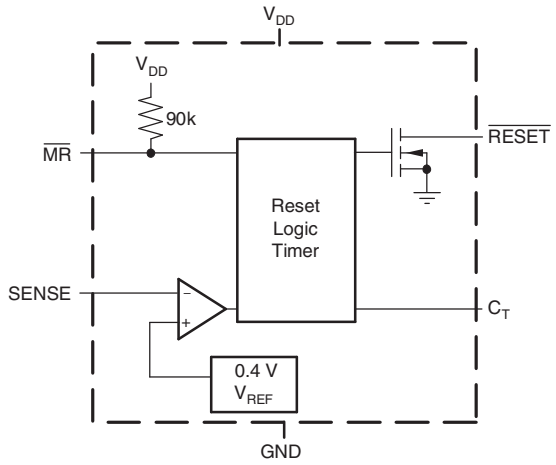


Figure 6. Adjustable-Voltage Version

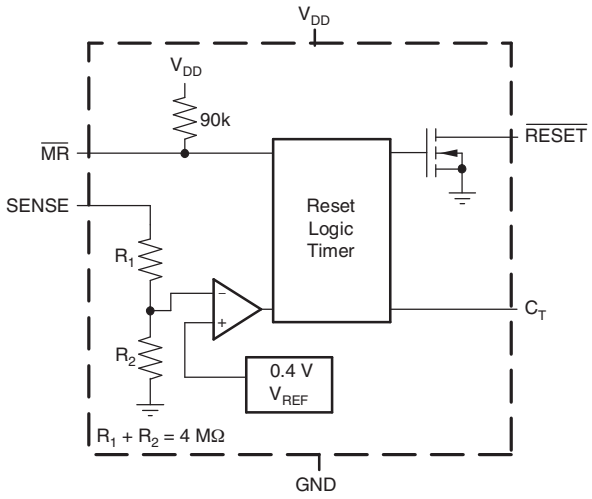


Figure 7. Fixed-Voltage Version

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8.3 Feature Description

8.3.1 Immunity to SENSE Pin Voltage Transients

The TPS3808Gxx-Q1 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 9). This graph shows the duration that the transient is below V_{IT} compared to the magnitude of the voltage drop below V_{IT}, or overdrive voltage. The overdrive voltage is expressed as a percentage of the V_{IT} threshold value. Any combination of transient duration and overdrive voltage that lies above the curve results in $\overline{\text{RESET}}$ being asserted low. Any transient that lies below the curve is ignored by the device.

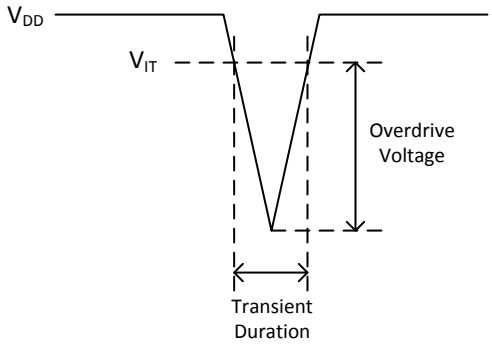


Figure 8. Threshold Overdrive Voltage

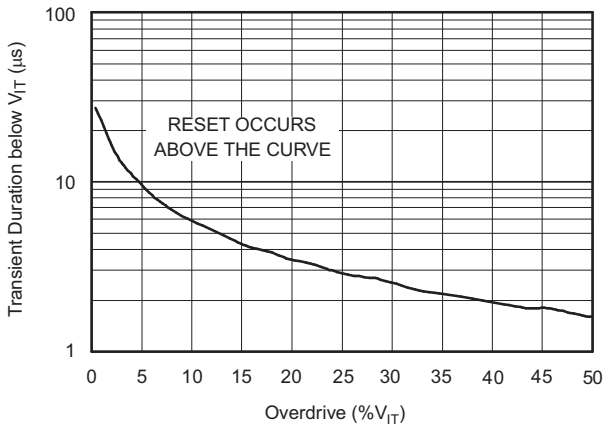


Figure 9. Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage

8.3.2 SENSE Input

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, $\overline{\text{RESET}}$ is asserted low. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and deassertions. It is good analog design practice to put a 1-nF to 10-nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

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Feature Description (continued)

The TPS3808G01-Q1 can be used to monitor any voltage rail down to 0.405 V using the circuit shown in Figure 10.

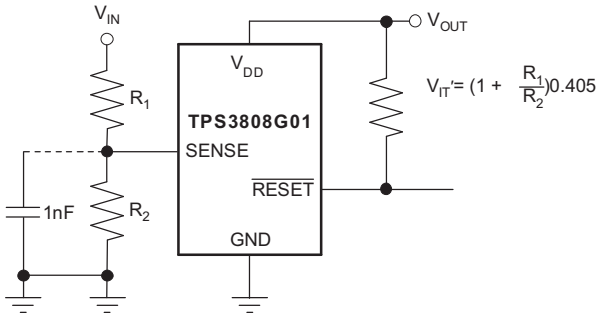


Figure 10. Using the TPS3808G01-Q1 to Monitor a User-Defined Threshold Voltage

8.3.3 Manual Reset ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a processor or other logic circuits to initiate a reset. A logic low (0.3 V_{DD}) on $\overline{MR}$ causes $\overline{RESET}$ to assert low. After $\overline{MR}$ returns to a logic high and SENSE is above its reset threshold, $\overline{RESET}$ is deasserted high after the user-defined reset delay expires. $\overline{MR}$ is internally tied to V_{DD} using a 90-kΩ resistor, so this pin can be left unconnected if $\overline{MR}$ is not used.

See Figure 11 for how $\overline{MR}$ can be used to monitor multiple system voltages. If the logic signal driving $\overline{MR}$ does not go fully to V_{DD}, there will be some additional current draw into V_{DD} as a result of the internal pullup resistor on $\overline{MR}$. To minimize current draw, a logic-level FET can be used as shown in Figure 12.

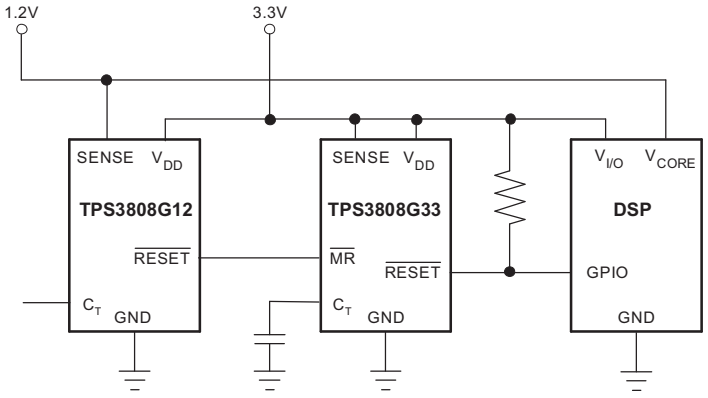


Figure 11. Using $\overline{MR}$ to Monitor Multiple System Voltages

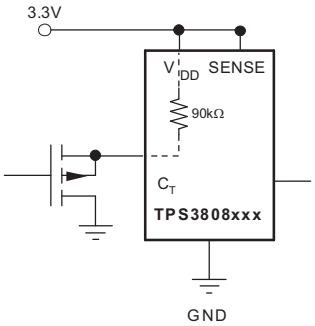


Figure 12. Using an External MOSFET to Minimize I_{DD} When $\overline{MR}$ Signal Does Not Go to V_{DD}

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Feature Description (continued)

8.3.4 Selecting the Reset Delay Time

The TPS3808Gxx-Q1 device has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure 13. Figure 13 (a) shows the configuration for a fixed 300-ms typical delay time by tying C_T to V_{DD}; a resistor from 40 kΩ to 200 kΩ must be used. Supply current is not affected by the choice of resistor. Figure 13 (b) shows a fixed 20-ms delay time by leaving the C_T pin open. Figure 13 (c) shows a ground referenced capacitor connected to C_T for a user-defined program time from 1.25 ms to 10 s.

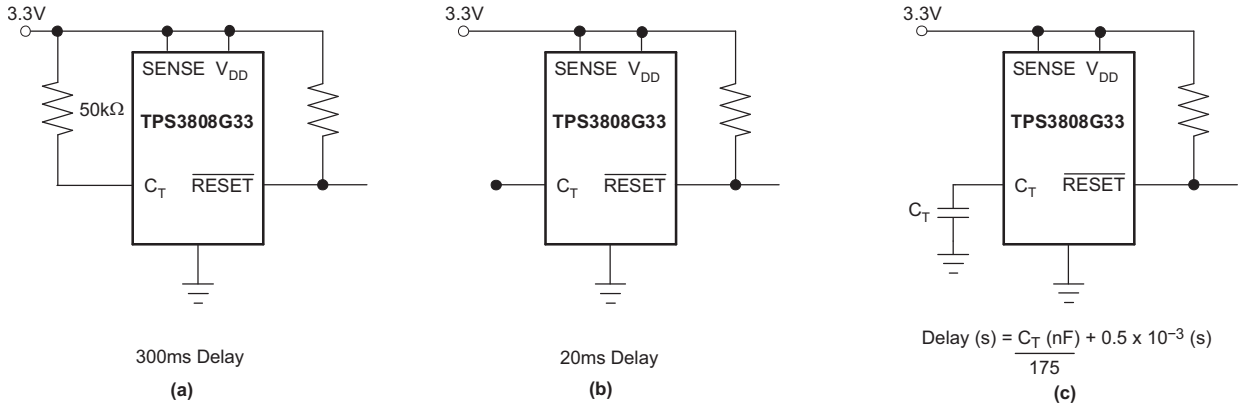


Figure 13. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time

The capacitor C_T should be ≥100 pF nominal value for the TPS3808Gxx-Q1 to recognize the capacitor is present. Use Equation 1 to calculate the capacitor value for a given delay time.

$$C_T(\text{nF}) = \left[t_D(\text{s}) - 0.5 \times 10^{-3}(\text{s}) \right] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220-nA current source to charge the external capacitor to 1.23 V. When $\overline{\text{RESET}}$ asserts low, the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23 V, $\overline{\text{RESET}}$ deasserts. A low-leakage type capacitor such as a ceramic should be used and that stray capacitance around this pin may cause errors in the reset delay time.

8.4 Device Functional Modes

Whenever $\overline{\text{MR}}$ pin is set to a logic high and the SENSE input pin is higher than V_{IT}, the open-drain $\overline{\text{RESET}}$ signal is deasserted high. If $\overline{\text{MR}}$ pin is set to a logic low or the SENSE input pin falls lower than V_{IT}, then $\overline{\text{RESET}}$ is asserted low. Table 1 is a truth table that describes these operating modes.

Table 1. Truth Table

$\overline{\text{MR}}$	SENSE > V_{IT}	$\overline{\text{RESET}}$
L	0	L
L	1	L
H	0	L
H	1	H

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS3808Gxx-Q1 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{IT} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a variety of applications. Reset threshold voltages can be factory-set from 0.82 V to 3.3 V or from 4.4 V to 5 V, while the TPS3808G01-Q1 can be set to any voltage above 0.405 V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300-ms reset delay, while leaving the C_T pin open yields a 20-ms reset delay. Additionally, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25 ms to 10 s.

9.2 Typical Application

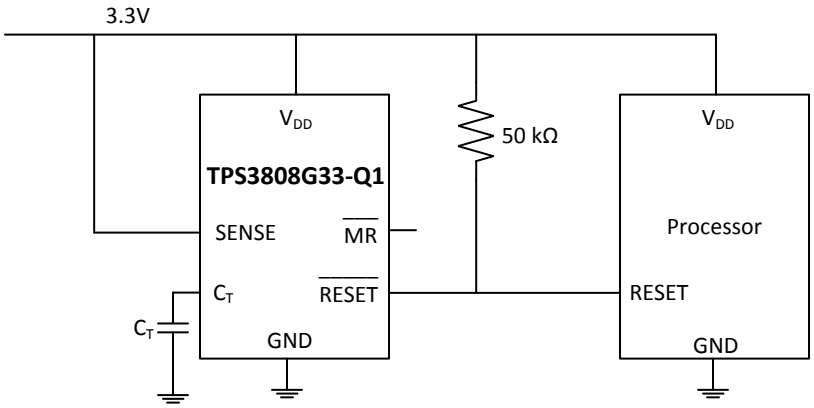


Figure 14. TPS3808G33-Q1 Typical Application

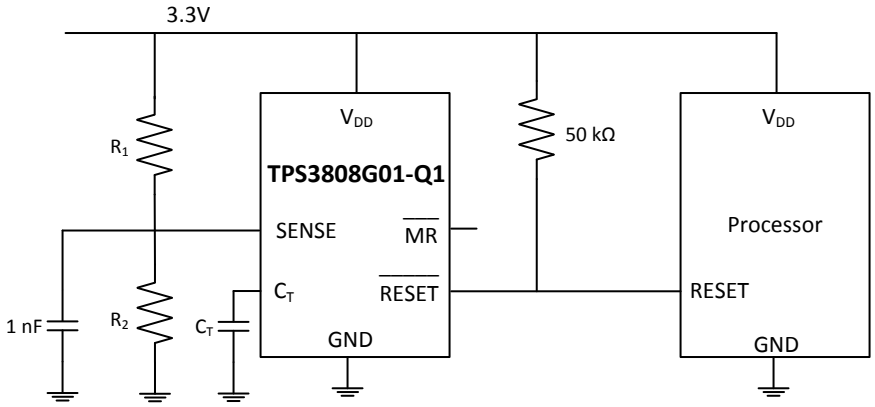


Figure 15. TPS3808G01-Q1 Typical Application

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Typical Application (continued)

9.2.1 Design Requirements

The TPS3808Gxx-Q1 device must monitor a 3.3-V input voltage, and drive an active-low reset to the processor when the input voltage drops below the recommended operating voltage of the processor.

9.2.2 Detailed Design Procedure

To monitor the 3.3-V input voltage, TPS3808G33-Q1 is used and the 3.3-V supply is connected directly to the SENSE pin. The open-drain $\overline{\text{RESET}}$ output is connected to V_{DD} through a 50-kΩ resistor. To select the output delay on the $\overline{\text{RESET}}$ pin, connect the C_T pin to V_{DD}, left floating, or connect through a capacitor to GND. For more details on selecting this delay, see *Selecting the Reset Delay Time*.

When using TPS3808G01-Q1, select R1 and R2 resistor values to select the threshold voltage based on the following equation: $V_{IT} = (1 + R1 / R2) \times 0.405$.

9.2.3 Application Curves

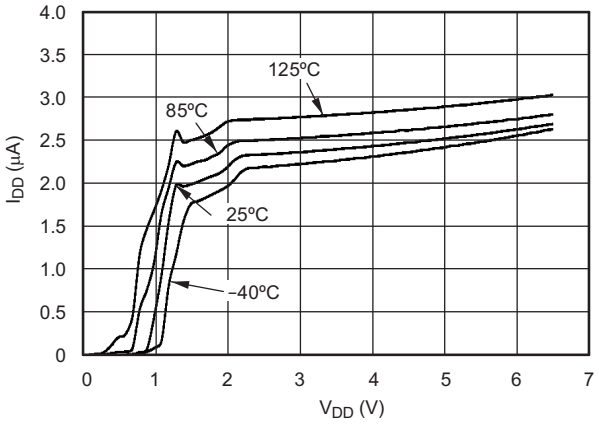


Figure 16. Supply Current vs Supply Voltage

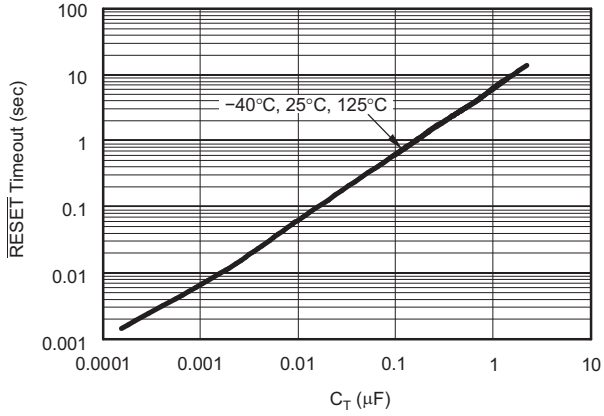


Figure 17. $\overline{\text{RESET}}$ Time-out Period vs C_T

10 Power Supply Recommendations

The TPS3808Gxx-Q1 devices are designed to operate from an input supply from 1.8 V to 6.5 V. TI recommends placing a 0.1-µF capacitor near the V_{DD} pin.

11 Layout

11.1 Layout Guidelines

TI recommends placing the 0.1-µF decoupling capacitor close to the V_{DD} pin. The V_{DD} trace should be able to carry 6 µA without a significant drop in voltage.

11.2 Layout Example

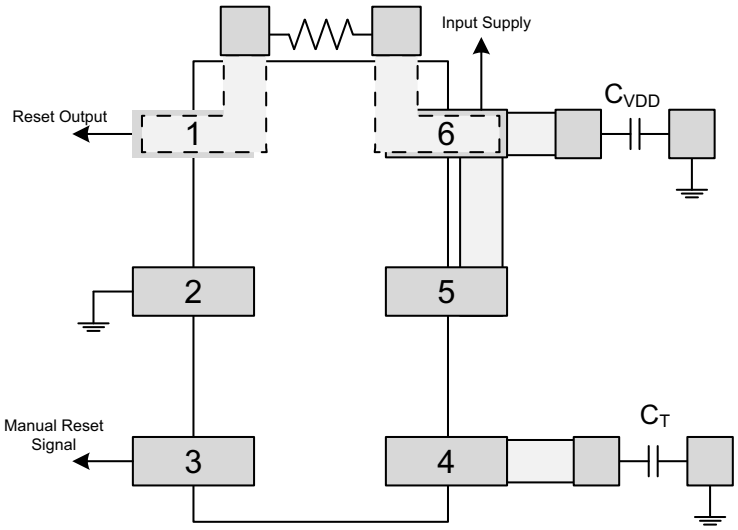


Figure 18. Recommended Layout

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12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3808G01-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G12-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G125-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G15-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G18-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G30-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G33-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G50-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3808G01QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAZ
TPS3808G01QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAZ
TPS3808G01QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSJQ
TPS3808G01QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSJQ
TPS3808G125QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(EQ125, QWZ)
TPS3808G125QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(EQ125, QWZ)
TPS3808G12QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEM
TPS3808G12QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEM
TPS3808G15QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFV
TPS3808G15QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFV
TPS3808G18QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBZ
TPS3808G18QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBZ
TPS3808G30QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP
TPS3808G30QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP
TPS3808G33QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ
TPS3808G33QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ
TPS3808G50QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEL
TPS3808G50QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS3808-Q1 :

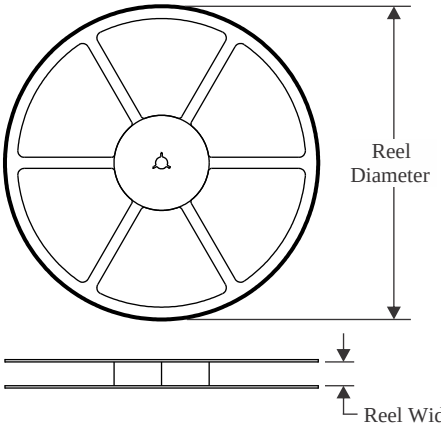
- Catalog : TPS3808
- Enhanced Product : TPS3808-EP

NOTE: Qualified Version Definitions:

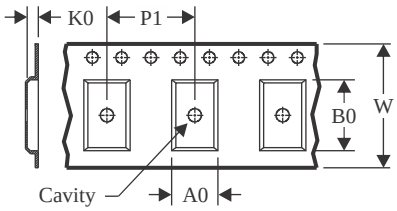
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

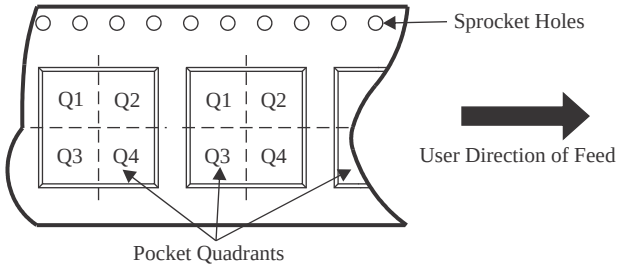


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

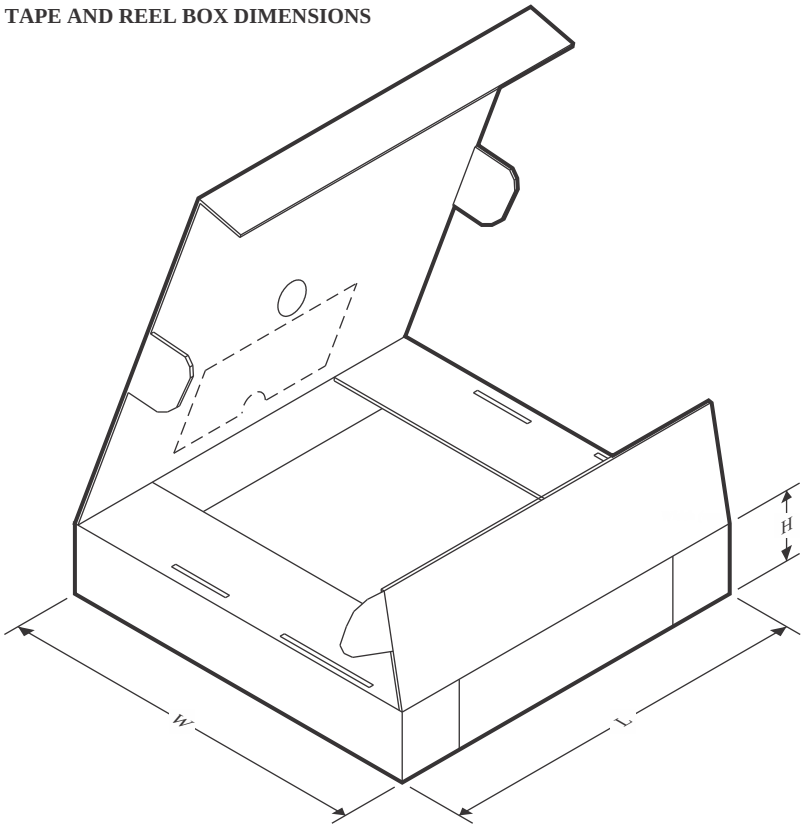
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G01QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G01QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS3808G125QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G12QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G15QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G18QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G30QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G33QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G50QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

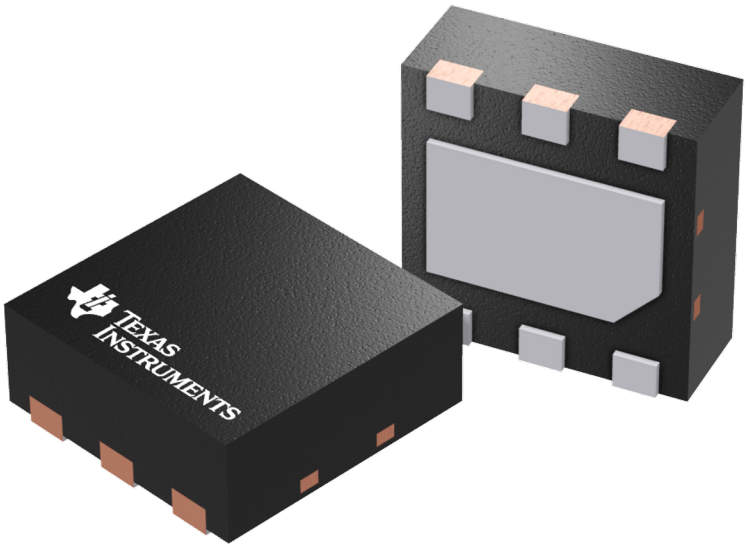


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G01QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3808G01QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS3808G125QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3808G12QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3808G15QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3808G18QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3808G30QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3808G33QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3808G50QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



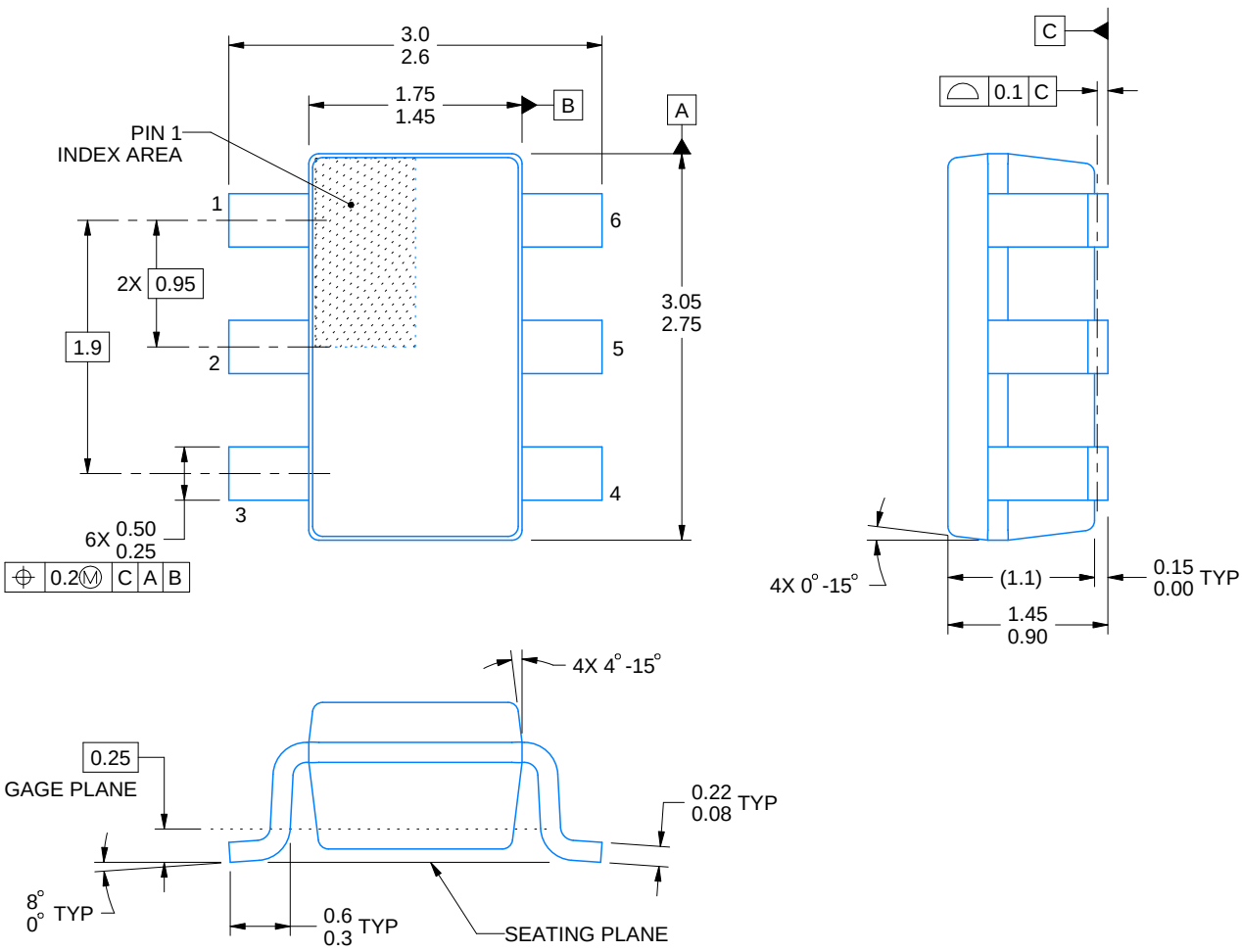
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

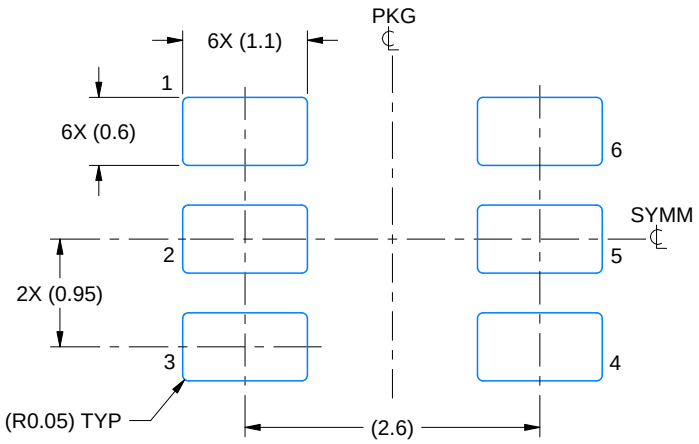
SMALL OUTLINE TRANSISTOR



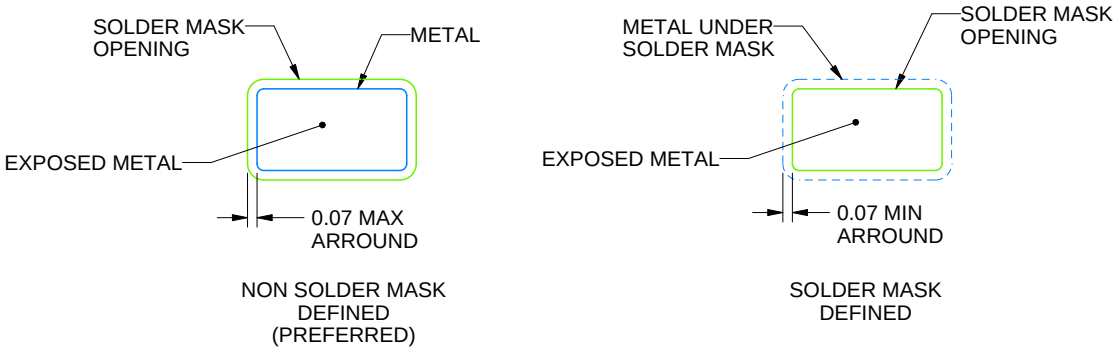
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

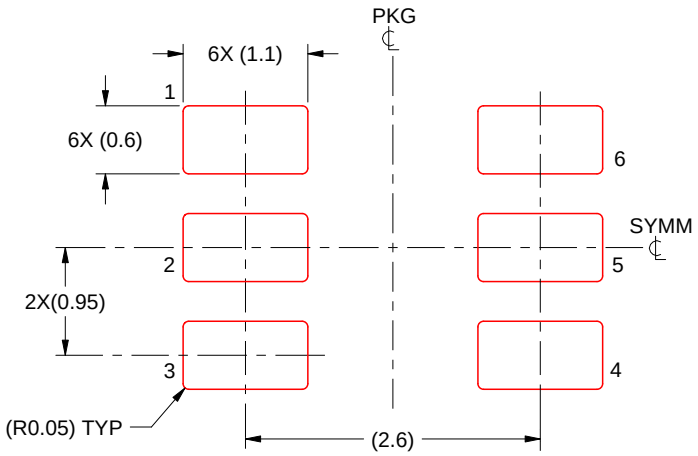


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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