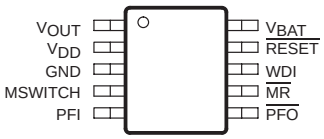
features

- Supply Current of 40 μA (Max)
- Precision 3.3-V Supply Voltage Monitor Other Voltage Options on Request
- Watchdog Timer With 800-ms Time-Out
- Backup-Battery Voltage Can Exceed V_{DD}
- Power-On Reset Generator With Fixed 100-ms Reset Delay Time
- Voltage Monitor for Power-Fail or Low-Battery Monitoring
- Manual Switchover to Battery-Backup Mode
- Manual Reset
- Battery Freshness Seal
- 10-Pin MSOP Package
- Temperature Range . . . −40°C to 85°C

typical applications

- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point-of-Sale Equipment

MSOP (DGS) Package
(TOP VIEW)



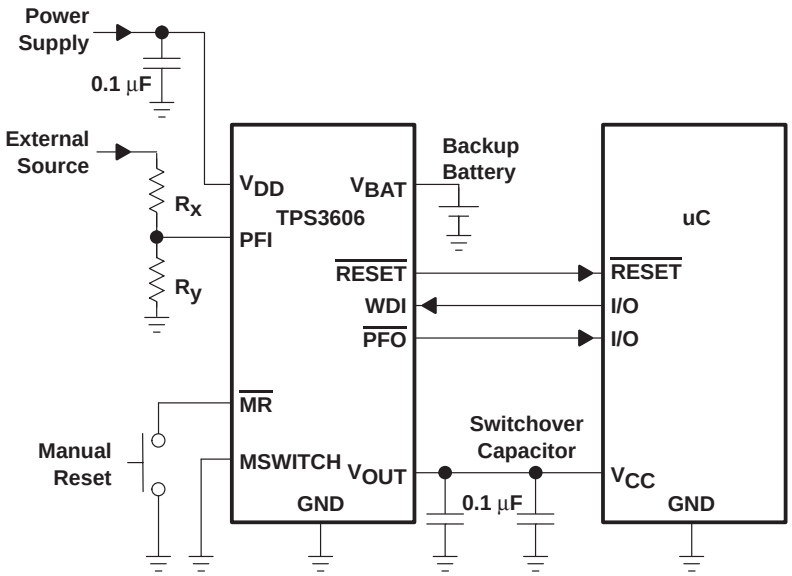


ACTUAL SIZE
3,05 mm x 4,98 mm

description

The TPS3606-33 supervisory circuit monitors and controls the processor activity. In case of power-fail or brownout conditions, the backup-battery switchover function of the TPS3606-33 allows a low-power processor and its peripherals to run from the installed backup battery without asserting a reset beforehand.

typical operating circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000−2007, Texas Instruments Incorporated

description (continued)

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{OUT} and keeps the $\overline{\text{RESET}}$ output active as long as V_{OUT} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{OUT} has risen above V_{IT}. When the supply voltage drops below V_{IT}, the output becomes active (low) again.

The TPS3606-33 is available in a 10-pin MSOP package and is characterized for operation over a temperature range of −40°C to 85°C.

PACKAGE INFORMATION

T_A	DEVICE NAME	MARKING
−40°C to 85°C	TPS3606−33DGSR†	AKE

† The DGSR passive indicates tape and reel of 2500 parts.

ordering information application specific versions (see Note)

TPS360 6 − 33 DGS R

- **R** — Reel
- **DGS** — Package
- **33** — Nominal Supply Voltage
- **6** — Functionality
- **TPS360** — Family

DEVICE NAME	NOMINAL VOLTAGE‡, V_{NOM}
TPS3606−33 DGS	3.3 V

‡ For other threshold voltages, contact the local TI sales office for availability and lead-time.

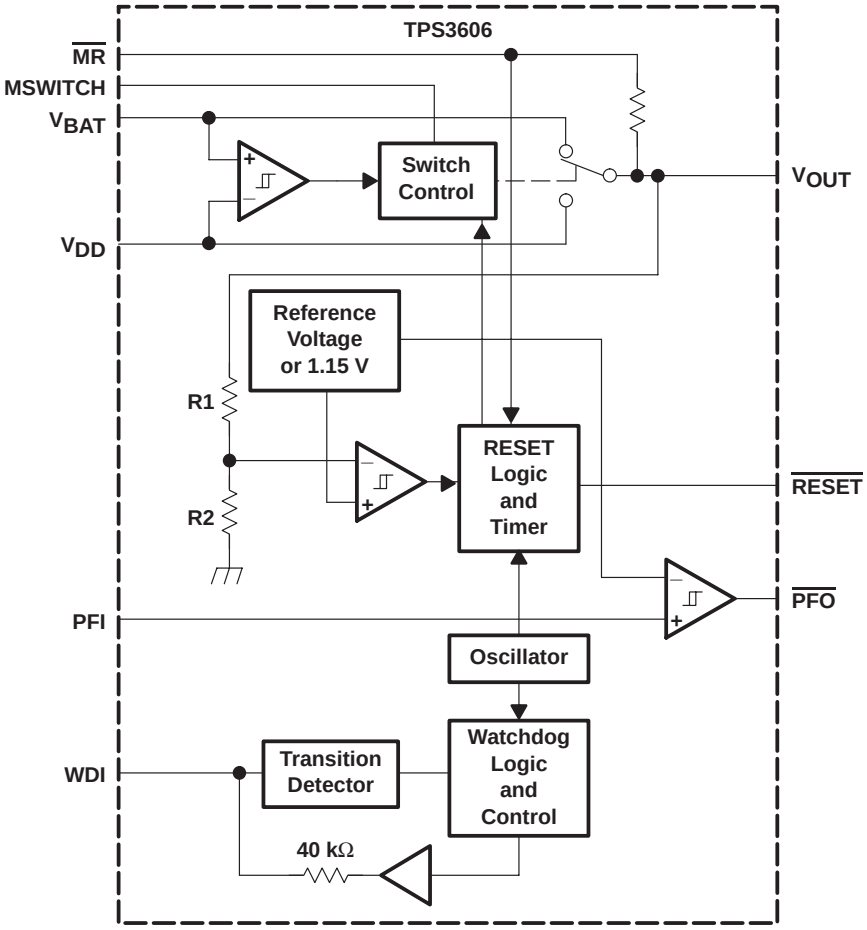
FUNCTION TABLES TPS3606

$V_{DD} > V_{SW}$	$V_{OUT} > V_{IT}$	$V_{DD} > V_{BAT}$	V_{OUT}	$\overline{\text{RESET}}$
0	0	0	V_{BAT}	0
0	0	1	V_{DD}	0
0	1	0	V_{BAT}	1
0	1	1	V_{DD}	1
1	1	0	V_{DD}	1
1	1	1	V_{DD}	1

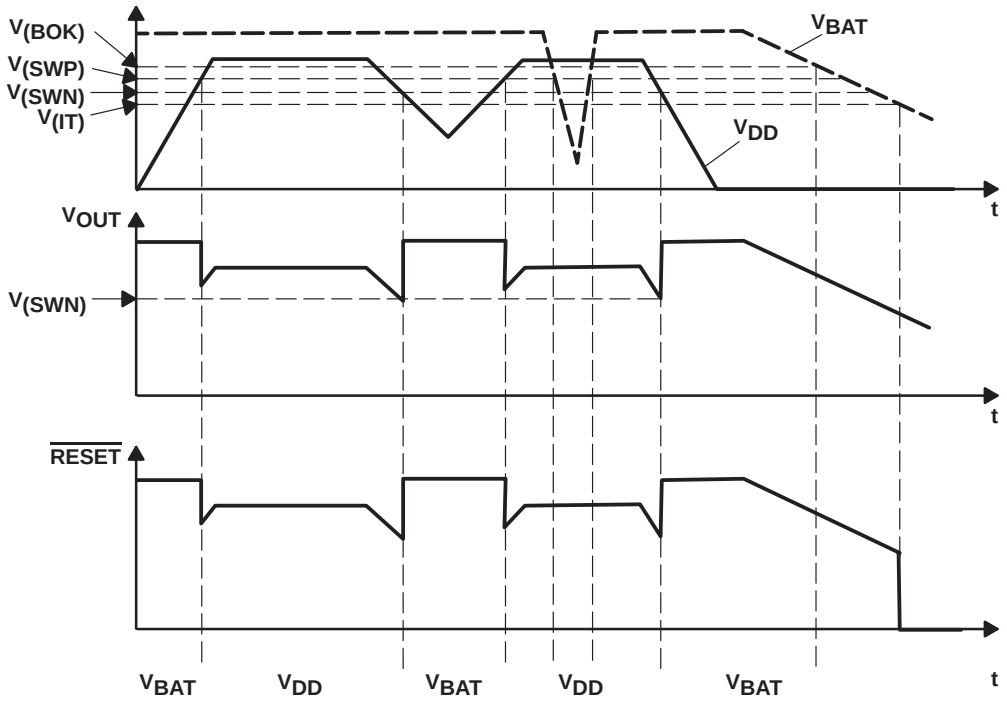
PFI > V_{PFI}	$\overline{\text{PFO}}$
0	0
1	1

CONDITION.: $V_{OUT} > V_{DD(min)}$

functional schematic



timing diagram



NOTES: A. MSWITCH = 0, $\overline{MR}$ = 1

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	3	I	Ground
$\overline{MR}$	7	I	Manual reset input
MSWITCH	4	I	Manual switch to force device into battery-backup mode
PFI	5	I	Power-fail comparator input
$\overline{PFO}$	6	O	Power-fail comparator output
$\overline{RESET}$	9	O	Active-low reset output
V_{BAT}	10	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output
WDI	8	I	Watchdog timer input

detailed description

battery freshness seal

The battery freshness seal of the TPS3606 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to V_{BAT} is fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect V_{BAT} ($V_{BAT} > V_{BAT(min)}$)
2. Ground $\overline{PFO}$
3. Connect PFI to V_{DD} or PFI > $V_{(PFI)}$
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$)
5. Ground $\overline{MR}$
6. Power down V_{DD}
7. The freshness seal mode is entered and pins $\overline{PFO}$ and $\overline{MR}$ can be disconnected.

The battery freshness seal mode is disabled by the positive-going edge of $\overline{RESET}$ when V_{DD} is applied.

power-fail comparator (PFI and $\overline{PFO}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ($V_{(PFI)}$) of 1.15 V typical, the power-fail output ($\overline{PFO}$) goes low. If it goes above $V_{(PFI)}$ plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage.

If the power-fail comparator is unused, connect PFI to ground and leave $\overline{PFO}$ unconnected.

backup-battery switchover

In the event of a brownout or power failure, it may be necessary to keep a processor running. If a backup battery is installed at V_{BAT}, the devices automatically connect the processor to backup power when V_{DD} fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, this family of supervisors does not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 2-Ω switch) when V_{OUT} falls below $V_{(SWN)}$ and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or when V_{DD} rises above the threshold ($V_{(SWP)}$.

$V_{DD} > V_{BAT}$	$V_{DD} > V_{(SWN)}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

detailed description (continued)

manual switchover (MSWITCH)

While operating in the normal mode from V_{DD}, the device can be manually forced to operate in the battery-backup mode by connecting MSWITCH to V_{DD}. The table below shows the different switchover modes.

	MSWITCH	Status
V_{DD} mode	GND	V_{DD} mode
	V_{DD}	Switch to battery-backup mode
Battery-backup mode	GND	Battery-backup mode
	V_{DD}	Battery-backup mode

If the manual switchover feature is not used, MSWITCH must be connected to ground.

watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure the correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or the DSP has to toggle the watchdog input within typically 0.8 s to avoid a time-out from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and is retriggered internally.

saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g. 5 V/40 kΩ ≈ 125 μA can flow into WDI.

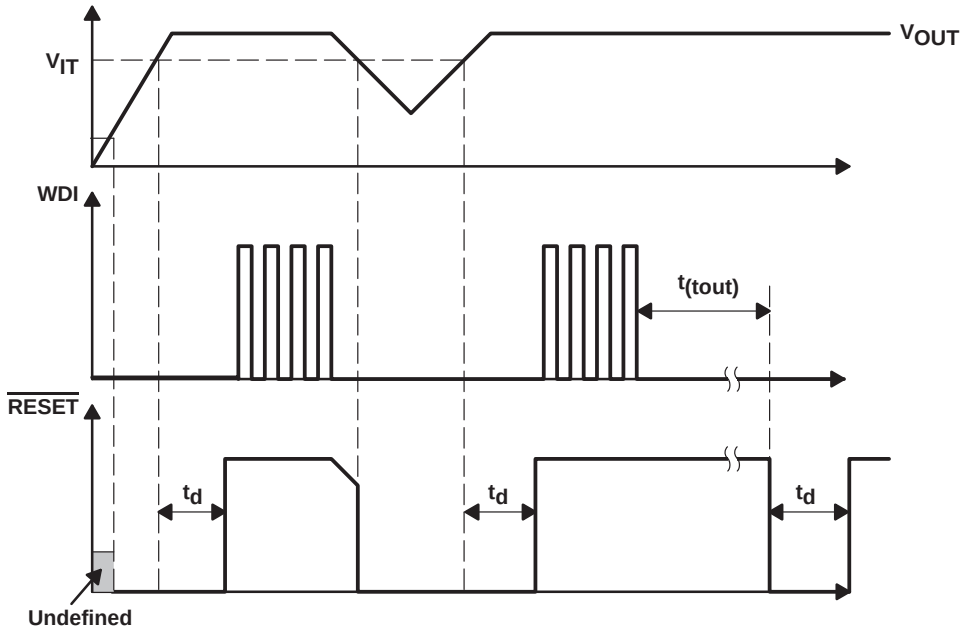


Figure 1. Watchdog Timing

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{DD} (see Note1) . . . . . 7 V
$\overline{MR}$, WDI, and PFI pins (see Note 1) . . . . . −0.3 V to (V_{DD} + 0.3 V)
Continuous output current at V_{OUT}: I_O . . . . . 300 mA
All other pins, I_O . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGS	424 mW	3.4 mW/°C	271 mW	220 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_O + 0.3	V
High-level input voltage, V_{IH}	0.7 x V_O		V
Low-level input voltage, all other pins, V_{IL}		0.3 x V_O	V
Continuous output current at V_{OUT}, I_O		200	mA
Input transition rise and fall rate at WDI, MSWITCH, $\Delta t/\Delta V$		100	ns/V
Slew rate at V_{DD} or V_{BAT}		34	mV/µs
Operating free-air temperature range, T_A	−40	85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{OUT} = 2 V, I_{OH} = −400 µA	V_{OUT} − 0.2 V			V
			V_{OUT} = 3.3 V I_{OH} = −2 mA V_{OUT} = 5 V, I_{OH} = −3 mA	V_{OUT} − 0.4 V			
		$\overline{PFO}$	V_{OUT} = 1.8 V, I_{OH} = −20 µA	V_{OUT} − 0.3 V			
			V_{OUT} = 3.3 V, I_{OH} = −80 µA V_{OUT} = 5 V, I_{OH} = −120 µA	V_{OUT} − 0.4 V			
V_{OL}	Low-level output voltage	$\overline{RESET}$ $\overline{PFO}$	V_{OUT} = 2 V, I_{OL} = 400 µA			0.2	V
			V_{OUT} = 3.3 V, I_{OL} = 2 mA V_{OUT} = 5 V, I_{OL} = 3 mA			0.4	
V_{res}	Power-up reset voltage (see Note 2)		V_{BAT} > 1.1 V or V_{DD} > 1.4 V, I_{OL} = 20 µA			0.4	V
V_{OUT}	Normal mode		I_O = 5 mA, V_{DD} = 1.8 V	V_{DD} − 50 mV			V
			I_O = 75 mA, V_{DD} = 3.3 V	V_{DD} − 150 mV			
			I_O = 150 mA, V_{DD} = 5 V	V_{DD} − 250 mV			
	Battery-backup mode		I_O = 4 mA, V_{BAT} = 1.5 V	V_{BAT} − 50 mV			
			I_O = 75 mA, V_{BAT} = 3.3 V	V_{BAT} − 150 mV			
$r_{ds(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 3.3 V		1	2	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{BAT} = 3.3 V		1	2	
V_{IT}	Negative-going input threshold voltage (see Notes 3 and 4)	TPS3606x33		2.87	2.93	2.99	V
$V_{(PFI)}$	Power-fail input threshold voltage	PFI		1.13	1.15	1.17	
$V_{(SWN)}$	Battery switch threshold voltage negative-going V_{OUT}			V_{IT} + 1%	V_{IT} + 2%	V_{IT} + 3.2%	V

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r(VDD)} \geq 15$ µs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.
4. Voltage is sensed at V_{OUT}
5. For details on how to optimize current consumption when using WDI refer to section detailed description.

electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis	V_{IT}	1.65 V < V_{IT} < 2.5 V		20		mV
			2.5 V < V_{IT} < 3.5 V		40		
			3.5 V < V_{IT} < 5.5 V		50		
		V_{PFI}			12		
		$V_{(SWN)}$	1.65 V < $V_{(SWN)}$ < 2.5 V		85		
			2.5 V < $V_{(SWN)}$ < 3.5 V		100		
			3.5 V < $V_{(SWN)}$ < 5.5 V		110		
I_{IH}	High-level input current	WDI	WDI = V_{DD} = 5.5 V			150	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 5 V	−33		−76	
I_{IL}	Low-level input current	WDI	WDI = 0 V, V_{DD} = 5 V			−150	
		$\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 5 V	−110		−255	
I_I	Input current	PFI, MSWITCH	V_I < V_{DD}	−25		25	nA
I_{OS}	Short-circuit current	$\overline{PFO}$	$\overline{PFO}$ = 0 V, V_{DD} = 1.8 V			−0.3	mA
			$\overline{PFO}$ = 0 V, V_{DD} = 3.3 V			−1.1	
			$\overline{PFO}$ = 0 V, V_{DD} = 5 V			−2.4	
I_{DD}	V_{DD} supply current		V_{OUT} = V_{DD}			40	µA
			V_{OUT} = V_{BAT}			8	
$I_{(BAT)}$	V_{BAT} supply current		V_{OUT} = V_{DD}	−0.1		0.1	µA
			V_{OUT} = V_{BAT}			40	
C_i	Input capacitance		V_I = 0 V to 5 V		5		pF

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = −40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	V_{DD}	V_{IH} = V_{IT} + 0.2 V, V_{IL} = V_{IT} − 0.2 V	5			µs
		$\overline{MR}$	V_{DD} > V_{IT} + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	100			ns
		WDI					

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = −40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		V_{DD} ≥ V_{IT} + 0.2 V, $\overline{MR}$ ≥ 0.7 x V_{DD}, See timing diagram	60	100	140	ms
$t_{(tout)}$	Watchdog time-out		V_{DD} > V_{IT} + 0.2 V, See timing diagram	0.48	0.8	1.12	s
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$	V_{IL} = V_{IT} − 0.2 V, V_{IH} = V_{IT} + 0.2 V		2	5	µs
		PFI to $\overline{PFO}$	V_{IL} = $V_{(PFI)}$ − 0.2 V, V_{IH} = $V_{(PFI)}$ + 0.2 V		3	5	µs
		$\overline{MR}$ to $\overline{RESET}$	V_{DD} ≥ V_{IT} + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}		0.1	1	µs
	Transition time	V_{DD} to V_{BAT}	V_{IL} = $V_{(BAT)}$ − 0.2 V, V_{IH} = $V_{(BAT)}$ + 0.2 V, $V_{(BAT)}$ < V_{IT}			3	µs

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance (V_{DD} to V_{OUT})	vs Output current	2
	Static drain-source on-state resistance (V_{BAT} to V_{OUT})	vs Output current	3
I_{DD}	Supply current	vs Supply voltage	4
		vs Battery supply	5
V_{IT}	Input threshold voltage at $\overline{\text{RESET}}$	vs Free-air temperature	6
V_{OH}	High-level output voltage at $\overline{\text{RESET}}$	vs High-level output current	7, 8
	High-level output voltage at $\overline{\text{PFO}}$		9, 10
V_{OL}	Low-level output voltage at $\overline{\text{RESET}}$	vs Low-level output current	11, 12
	Minimum pulse duration at V_{DD}	vs Threshold voltage overdrive at V_{DD}	13
	Minimum pulse duration at PFI	vs Threshold voltage overdrive at PFI	14

STATIC DRAIN SOURCE ON-STATE RESISTANCE (V_{DD} TO V_{OUT}) vs OUTPUT CURRENT

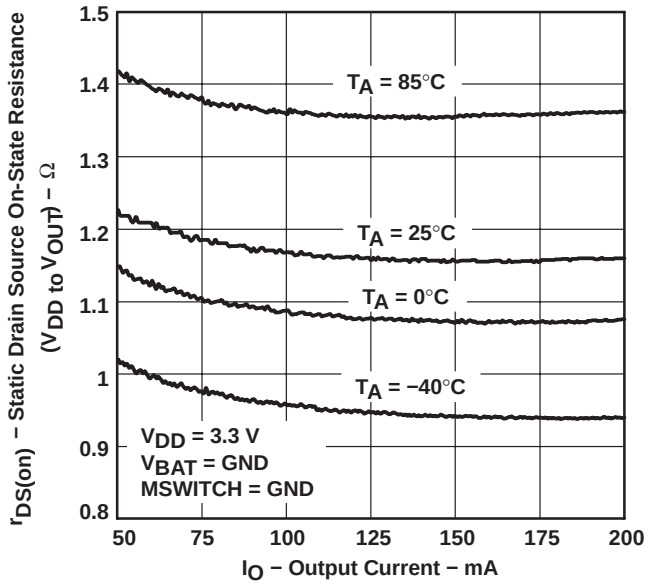


Figure 2

STATIC DRAIN SOURCE ON-STATE RESISTANCE (V_{BAT} TO V_{OUT}) vs OUTPUT CURRENT

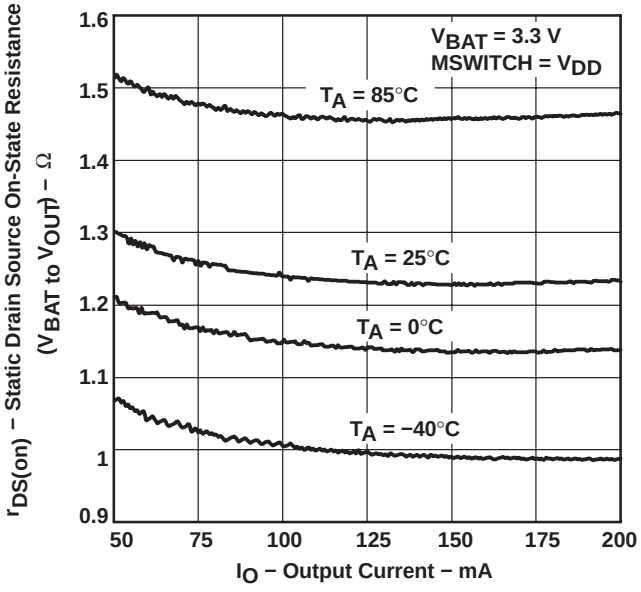


Figure 3

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

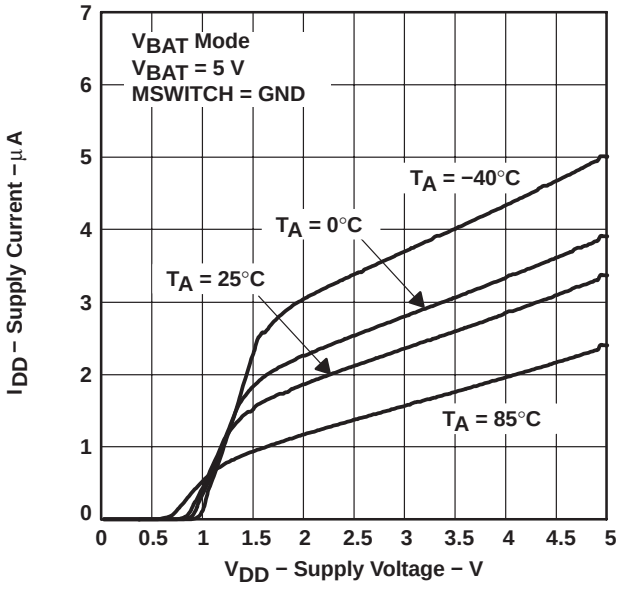


Figure 4

SUPPLY CURRENT
vs
BATTERY SUPPLY

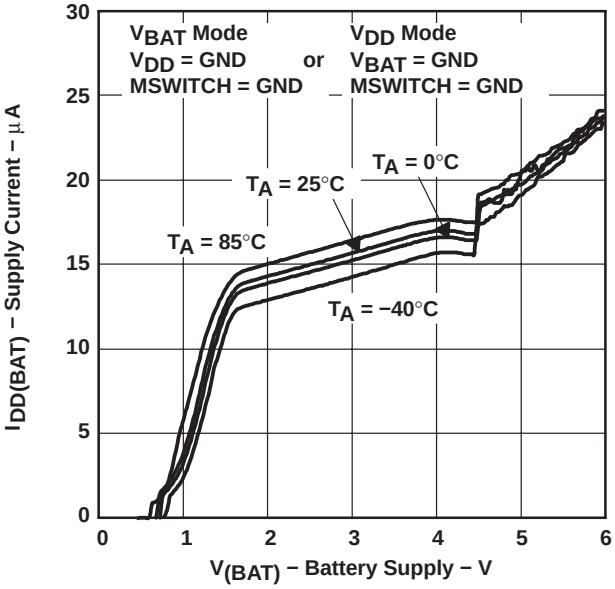


Figure 5

INPUT THRESHOLD VOLTAGE AT $\overline{\text{RESET}}$
vs
FREE-AIR TEMPERATURE

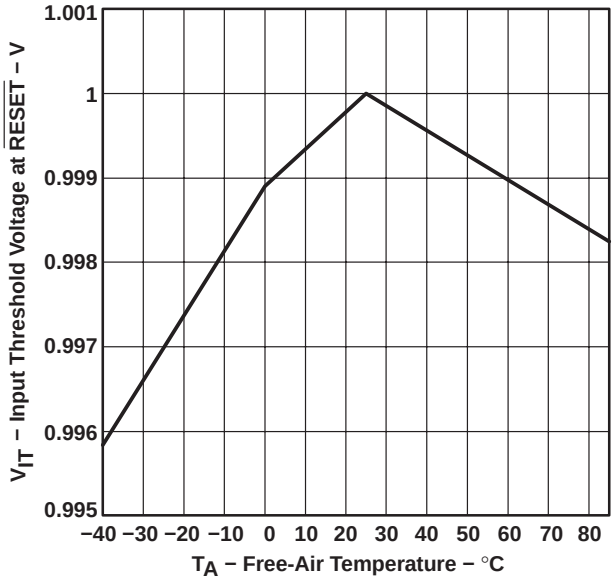


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
HIGH-LEVEL OUTPUT CURRENT

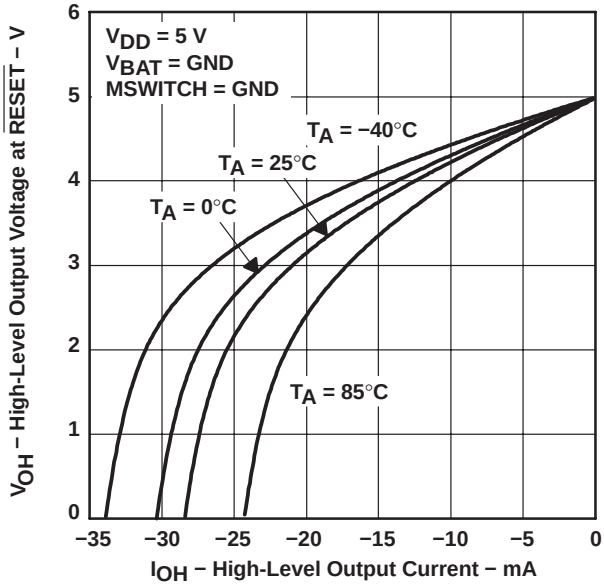


Figure 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
HIGH-LEVEL OUTPUT CURRENT

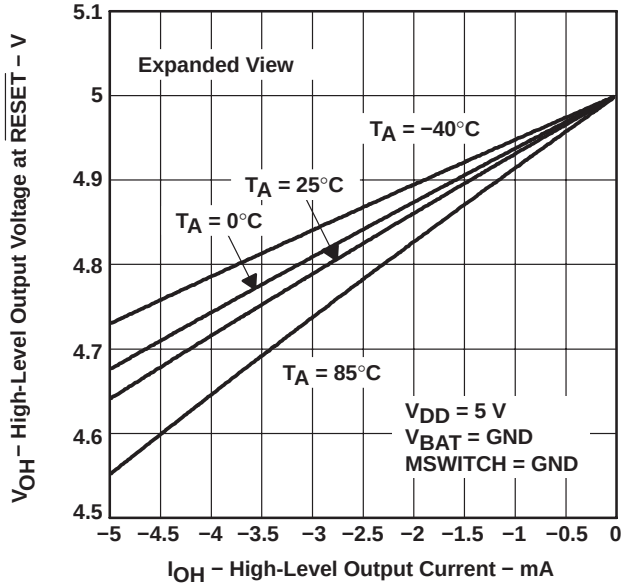


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{PFO}}$
vs
HIGH-LEVEL OUTPUT CURRENT

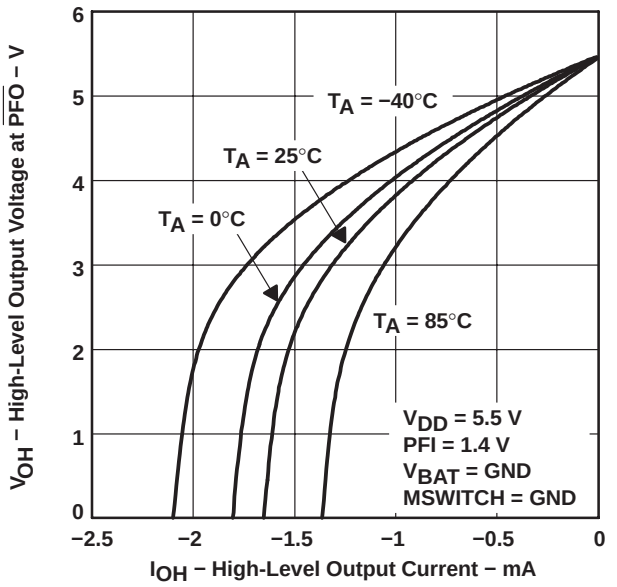


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{PFO}}$
vs
HIGH-LEVEL OUTPUT CURRENT

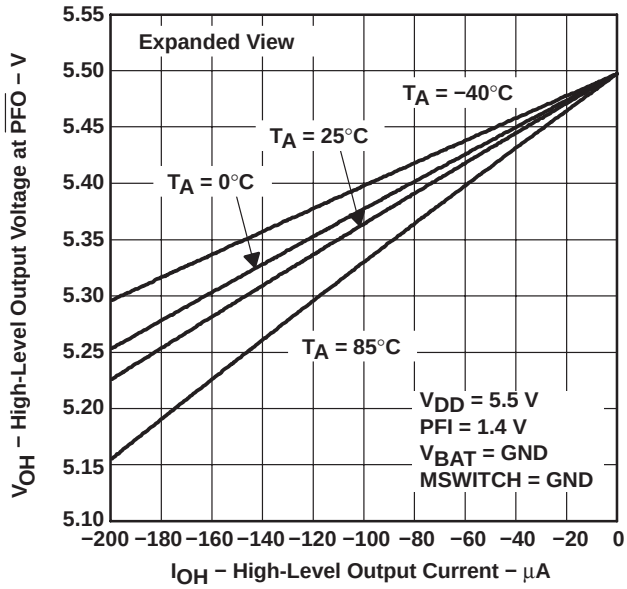


Figure 10

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
LOW-LEVEL OUTPUT CURRENT

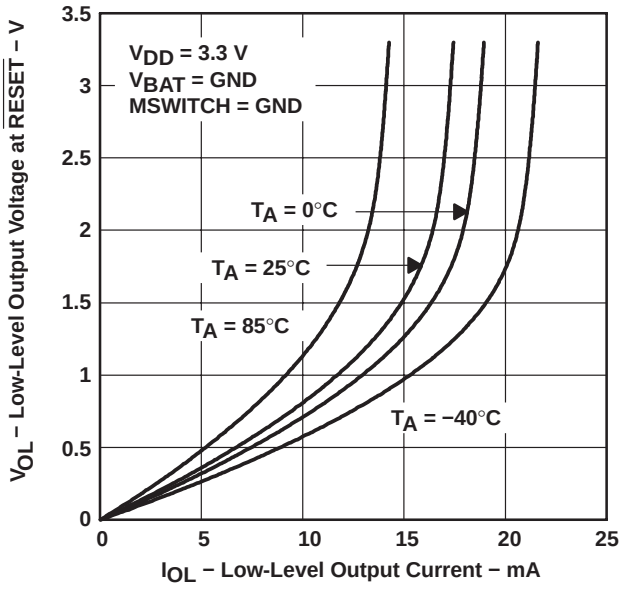


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
LOW-LEVEL OUTPUT CURRENT

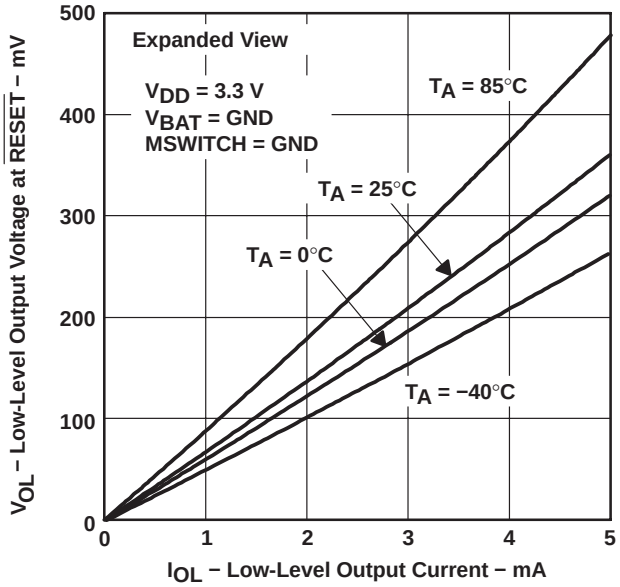


Figure 12

MINIMUM PULSE DURATION AT V_{DD}
vs
THRESHOLD VOLTAGE OVERDRIVE AT V_{DD}

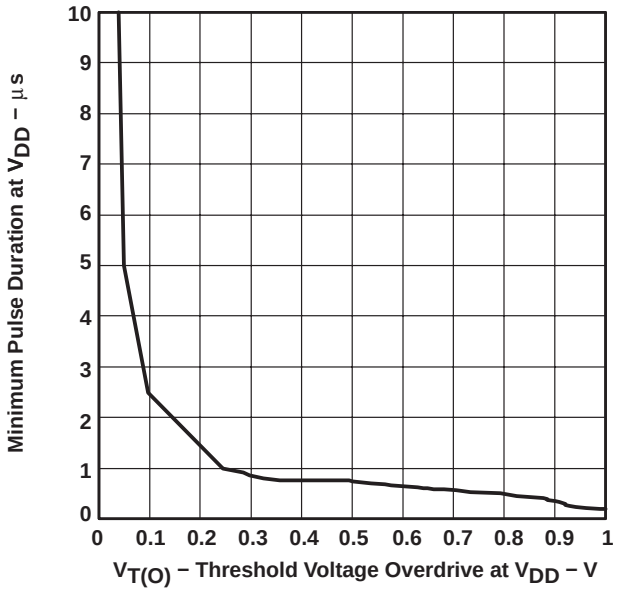


Figure 13

MINIMUM PULSE DURATION AT PFI
vs
THRESHOLD VOLTAGE OVERDRIVE AT PFI

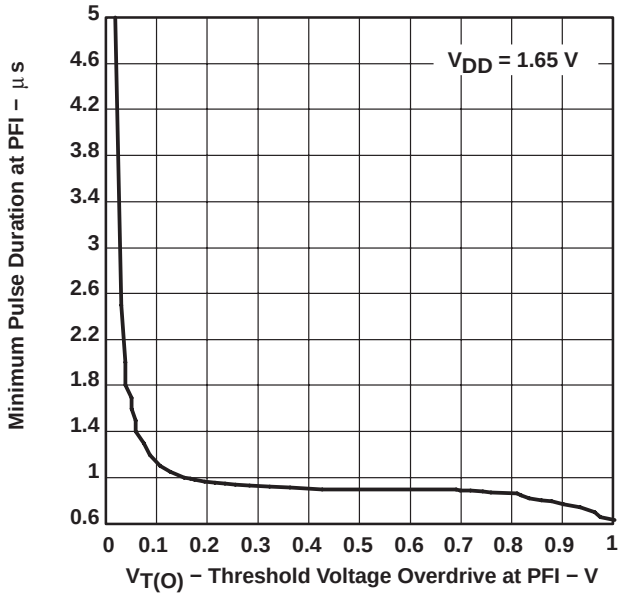


Figure 14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3606-33DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE
TPS3606-33DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE
TPS3606-33DGSR	NRND	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE
TPS3606-33DGSR.A	NRND	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AKE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

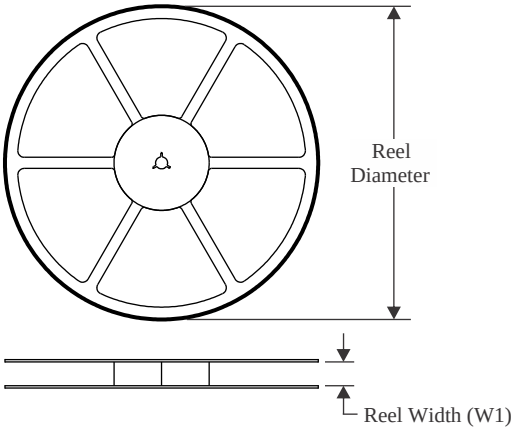
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

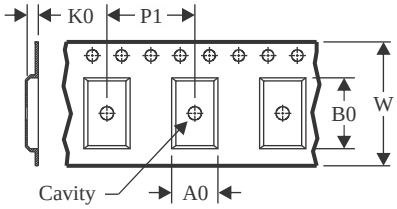
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

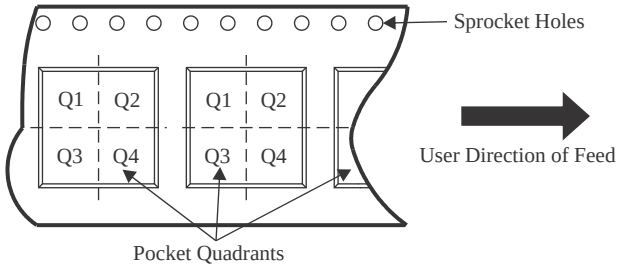


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

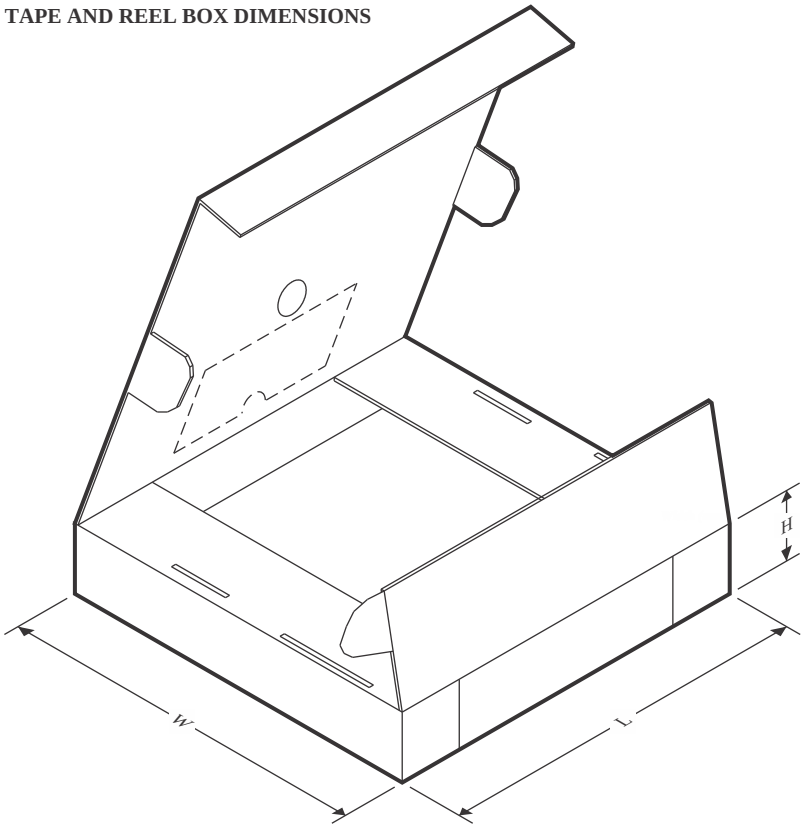
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3606-33DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

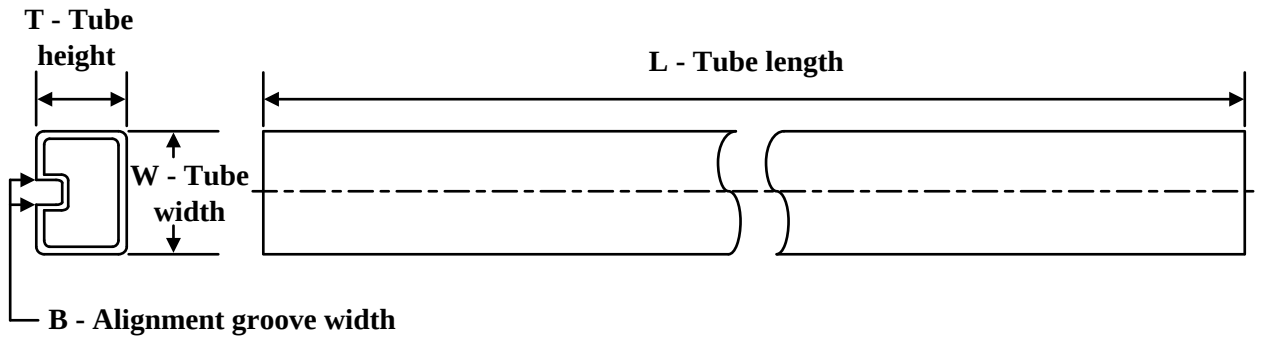
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3606-33DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0

TUBE



*All dimensions are nominal

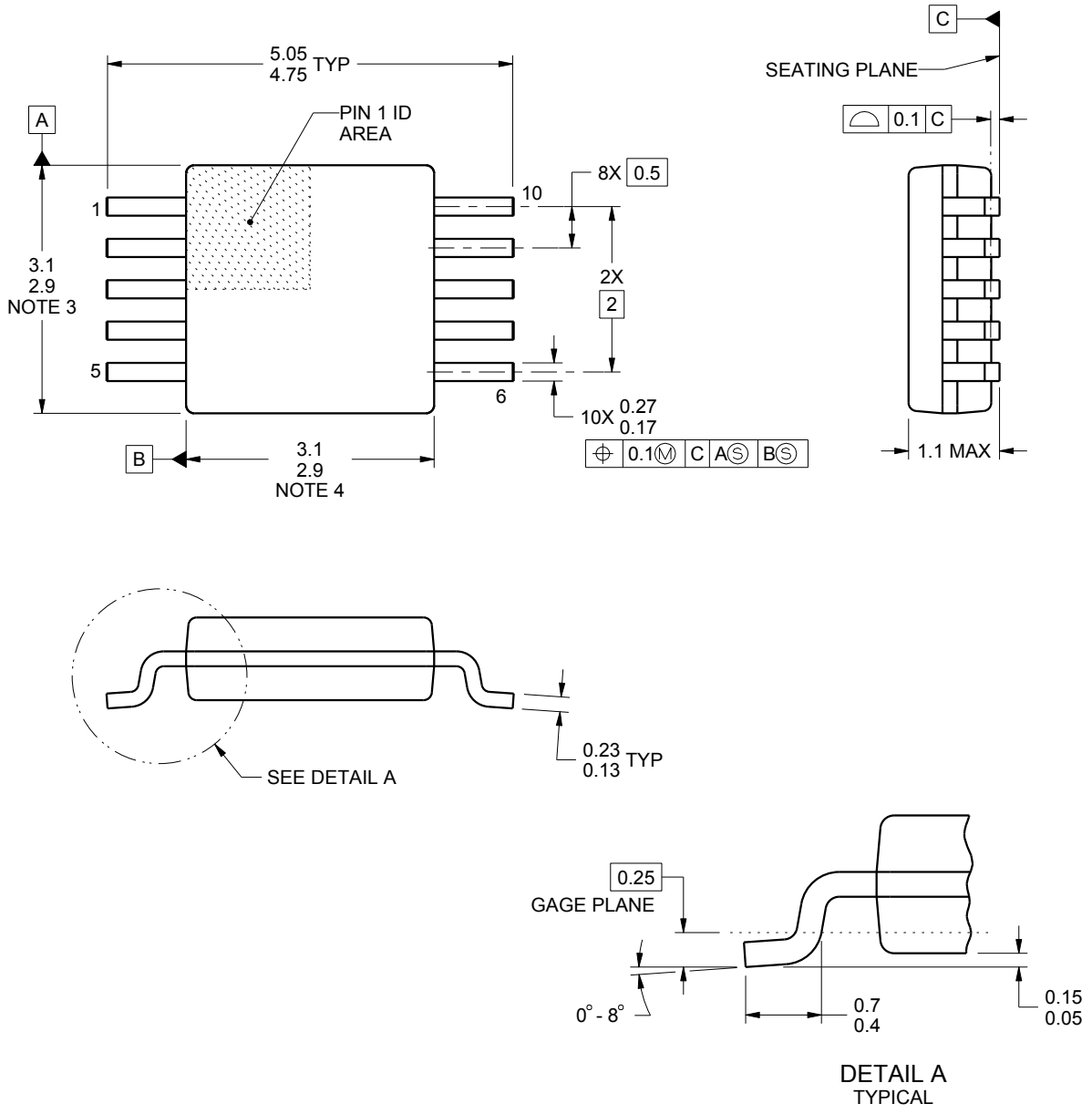
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS3606-33DGS	DGS	VSSOP	10	80	274	6.2	2540	2.5
TPS3606-33DGS.A	DGS	VSSOP	10	80	274	6.2	2540	2.5

PACKAGE OUTLINE

DGS0010A

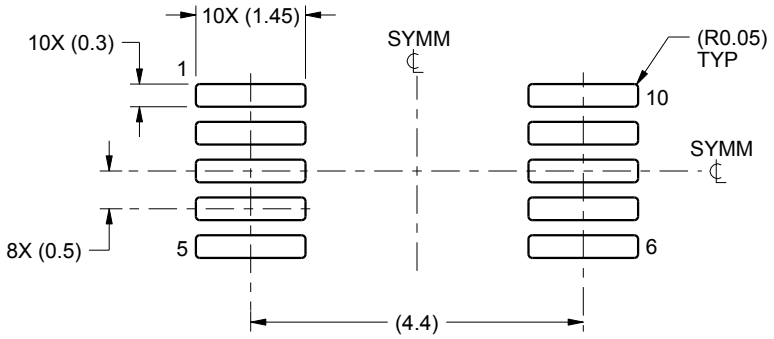
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

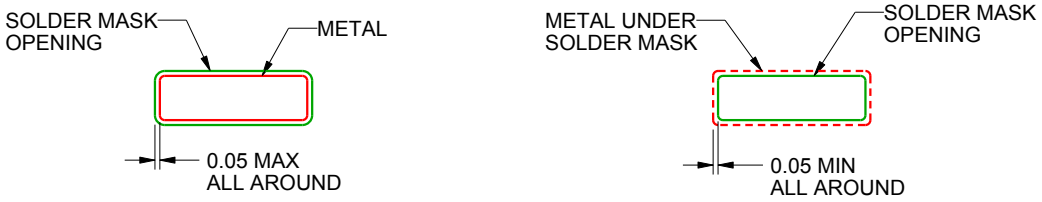


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

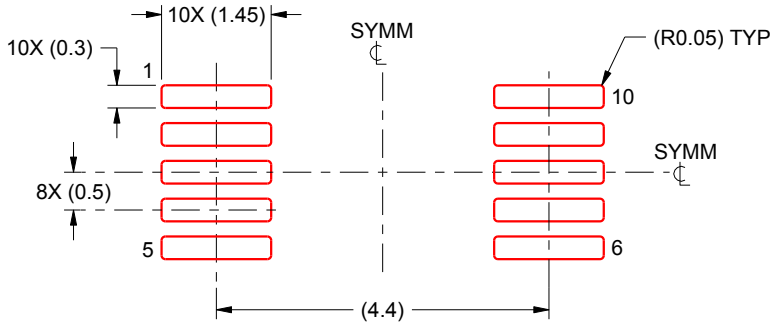


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025