



DUAL PROCESSOR SUPERVISORS

FEATURES

- Dual Supervisory Circuits for DSP- and Processor-Based Systems
- Power-On Reset Generator with Fixed Delay Time of 200ms; no External Capacitor Needed
- Watchdog Timer Retriggeres the $\overline{\text{RESET}}$ Output at $\text{SENSEn} \geq V_{IT+}$
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40 μA
- Supply Voltage Range: 2.7V to 6V
- Defined $\overline{\text{RESET}}$ Output From $V_{DD} \geq 1.1\text{V}$
- MSOP-8 and SO-8 Packages
- Temperature Range: -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

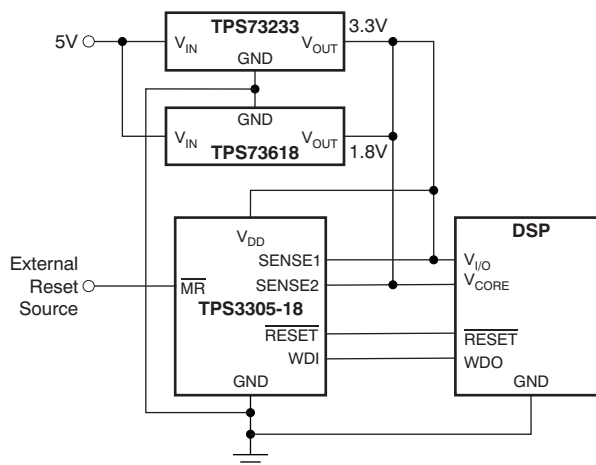
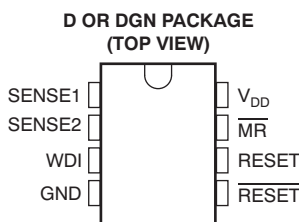
- Processor Supply Monitoring
- Industrial Equipment
- Automotive Systems
- Portable/Battery-Powered Equipment
- Wireless Communication Systems
- Notebook/Desktop Computers

DESCRIPTION

The TPS3305 family is a series of micropower supply voltage supervisors designed for circuit initialization. Its dual monitor topology is well-suited to use in DSP and processor-based systems, which often require two supply voltages, core and I/O.

$\overline{\text{RESET}}$ is asserted when the voltage at either SENSEn pin falls below its threshold voltage, V_{IT-} . When both SENSEn pins are again above their respective threshold voltages, $\overline{\text{RESET}}$ is held low for the factory-programmed delay time (200ms typ). $\overline{\text{RESET}}$ is also asserted if the watchdog input (WDI) is not toggled for more than 1.6s typ.

The TPS3305-xx devices are available in either 8-pin MSOP or SO packages, and are specified for operation over a temperature range of -40°C to $+85^{\circ}\text{C}$.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3305-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3305-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3305-33	5.0 V	3.3 V	4.55 V	2.93 V

- (1) For the most current specifications and package information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Over operating junction temperature range (unless otherwise noted).

	UNIT
Supply voltage range, V_{DD}	–0.3V to +7V
V_{MR} , V_{WDI}	–0.3V to $V_{DD} + 0.3V$
Input voltage at SENSE1 and SENSE2, V_I	$(V_{DD} + 0.3)V_{IT} / 1.25V$
V_{RESET} , V_{RESET}	–0.3V to +7V
Maximum low output current, I_{OL}	5mA
Maximum high output current, I_{OH}	–5mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20mA
Continuous total power dissipation	See Dissipation Ratings Table
Operating junction temperature range, T_J	–40°C to +85°C
Storage temperature range, T_{stg}	–65°C to +150°C
Soldering temperature	+260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

DISSIPATION RATINGS TABLE

PACKAGE	$T_A \leq +25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25^\circ\text{C}$	$T_A = +70^\circ\text{C}$ POWER RATING	$T_A = +85^\circ\text{C}$ POWER RATING
DGN	2.14W	17.1mW/°C	1.37W	1.11W
D	725mW	5.8mW/°C	464mW	377mW

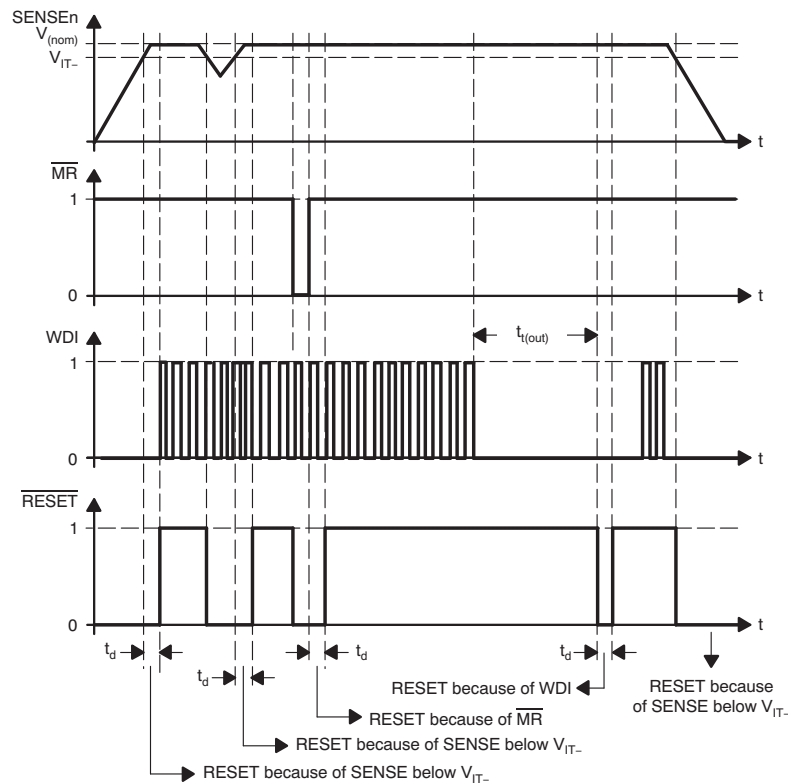
ELECTRICAL CHARACTERISTICS

Over operating junction temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	TPS3305-xx			UNIT
				MIN	TYP	MAX	
V _{DD}	Input supply range			2.7		6.0	V
T _J	Operating junction temperature range			−40		+85	°C
V _{OH}	High-level output voltage		V _{DD} = 2.7V to 6V, I _{OH} = −20μA	V _{DD} − 0.2V			V
			V _{DD} = 3.3V, I _{OH} = −2mA	V _{DD} − 0.4V			V
			V _{DD} = 6V, I _{OH} = −3mA	V _{DD} − 0.4V			V
V _{OL}	Low-level output voltage		V _{DD} = 2.7V to 6V, I _{OL} = 20μA	0.2			V
			V _{DD} = 3.3V, I _{OL} = 2mA	0.4			V
			V _{DD} = 6V, I _{OL} = 3mA	0.4			V
Power-up reset voltage ⁽¹⁾			V _{DD} ≥ 1.1V, I _{OL} = 20μA	0.4			V
V _{IT−}	Negative-going input threshold voltage ⁽²⁾	VSENSE1, VSENSE2	V _{DD} = 2.7V to 6V, T _A = 0°C to +85°C	1.64	1.68	1.72	V
				2.20	2.25	2.30	V
				2.86	2.93	3.0	V
				4.46	4.55	4.64	V
		VSENSE1, VSENSE2	V _{DD} = 2.7V to 6V, T _A = −40°C to +85°C	1.64	1.68	1.73	V
				2.20	2.25	2.32	V
				2.86	2.93	3.02	V
				4.46	4.55	4.67	V
V _{hys}	Hysteresis at VSENSEn input		V _{IT−} = 1.68V	15			mV
			V _{IT−} = 2.25V	20			mV
			V _{IT−} = 2.93V	30			mV
			V _{IT−} = 4.55V	40			mV
I _{H(AV)}	Average high-level input current	WDI	WDI = V _{DD} = 6V Time average (dc = 88%)	100		150	μA
I _{L(AV)}	Average low-level input current	WDI	WDI = 0V, V _{DD} = 6V Time average (dc = 12%)	−15		−20	μA
V _{IH}	High-level input voltage at $\overline{\text{MR}}$ and WDI			0.7 × V _{DD}			V
V _{IL}	Low-level input voltage at $\overline{\text{MR}}$ and WDI			0.3 × V _{DD}			V
Δt / ΔV	Input transition rise and fall rate at $\overline{\text{MR}}$			50			ns/V
I _H	High-level input current	WDI	WDI = V _{DD} = 6V	120		170	μA
		$\overline{\text{MR}}$	$\overline{\text{MR}}$ = 0.7 × V _{DD} , V _{DD} = 6V	−130		−180	μA
		SENSE1	VSENSE1 = V _{DD} = 6V	5		8	μA
		SENSE2	VSENSE2 = V _{DD} = 6V	6		9	μA
I _L	Low-level input current	WDI	WDI = 0V, V _{DD} = 6V	−120		−170	μA
		$\overline{\text{MR}}$	$\overline{\text{MR}}$ = 0V, V _{DD} = 6V	−430		−600	μA
		SENSEn	VSENSE1,2 = 0V	−1		1	μA
I _{DD}	Supply current			40			μA
C _I	Input capacitance		V _I = 0V to V _{DD}	10		pF	

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. t_r, V_{DD} ≥ 15 μs/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1 μF ceramic) should be placed close to the supply terminals.

TIMING DIAGRAM**TIMING REQUIREMENTS**

At $V_{DD} = 2.7V$ to $6V$, $R_L = 1M\Omega$, $C_L = 50pF$, and $T_J = +25^\circ C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2V$, $V_{SENSEnH} = V_{IT+} + 0.2V$	6			μs
	$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns
	WDI	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

SWITCHING CHARACTERISTICS

At $V_{DD} = 2.7V$ to $6V$, $R_L = 1M\Omega$, $C_L = 50pF$, and $T_J = +25^\circ C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(out)}$ Watchdog time-out		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$ See Timing Diagram	1.1	1.6	2.3	s
t_d Delay time		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$ See Timing Diagram	140	200	280	ms
t_{PHL} Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PLH} Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PHL} Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$, SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	μs
t_{PLH} Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$, SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	μs

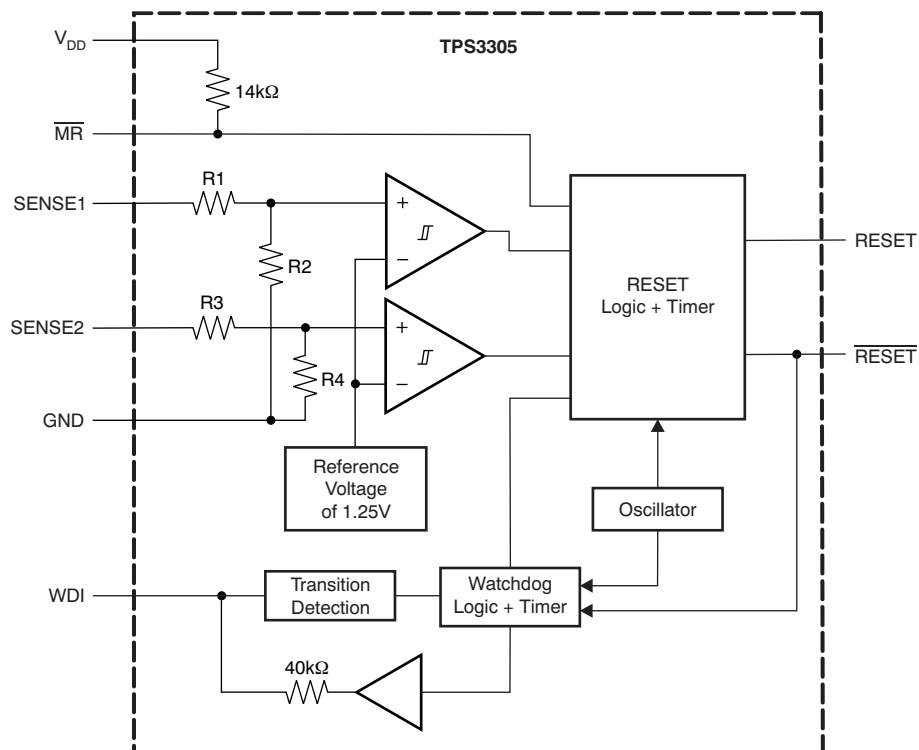
DEVICE INFORMATION

FUNCTION/TRUTH TABLE⁽¹⁾

MR	SENSE1 > V _{IT1}	SENSE2 > V _{IT2}	RESET	RESET
L	X	X	L	H
H	0	0	L	H
H	0	1	L	H
H	1	0	L	H
H	1	1	H	L

(1) X = Don't care

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
GND	4	Ground
MR	7	Manual reset
RESET	5	Active-low reset output
RESET	6	Active-high reset output
SENSE1	1	Sense voltage input 1
SENSE2	2	Sense voltage input 2
WDI	3	Watchdog timer input
V _{DD}	8	Supply voltage

TYPICAL CHARACTERISTICS

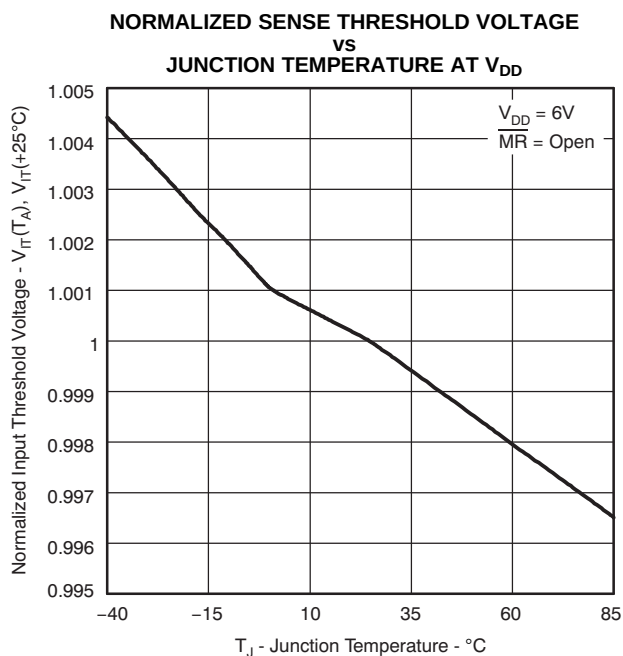


Figure 1.

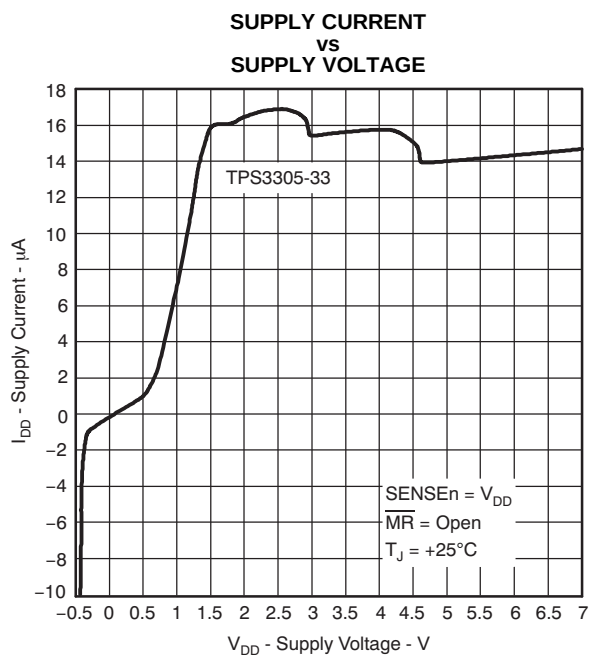


Figure 2.

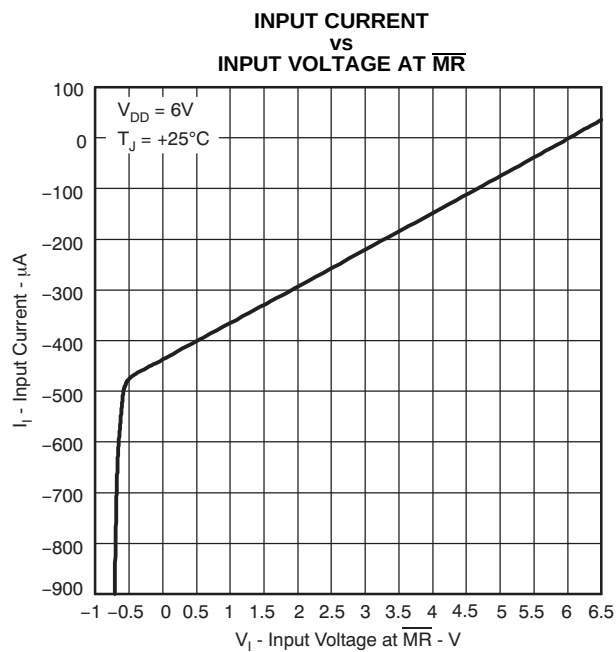


Figure 3.

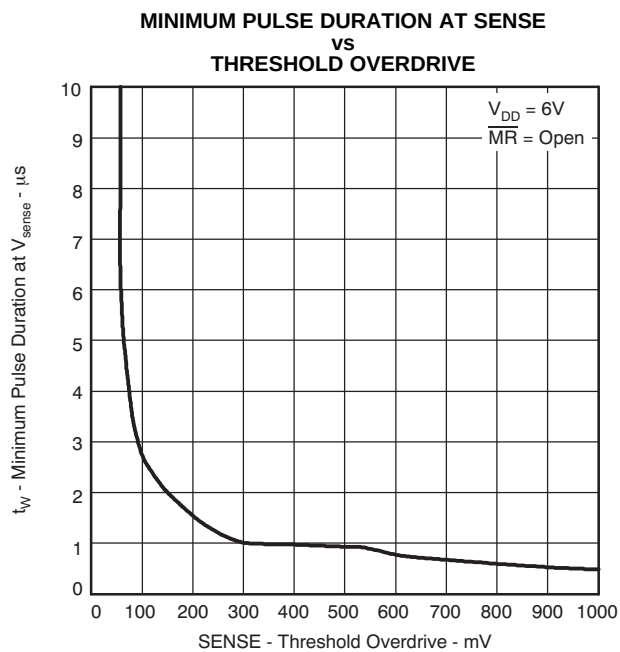


Figure 4.

TYPICAL CHARACTERISTICS (continued)

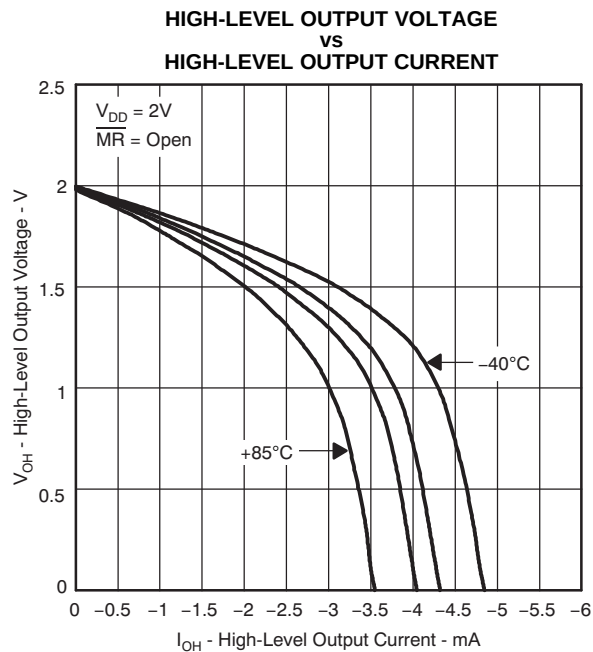


Figure 5.

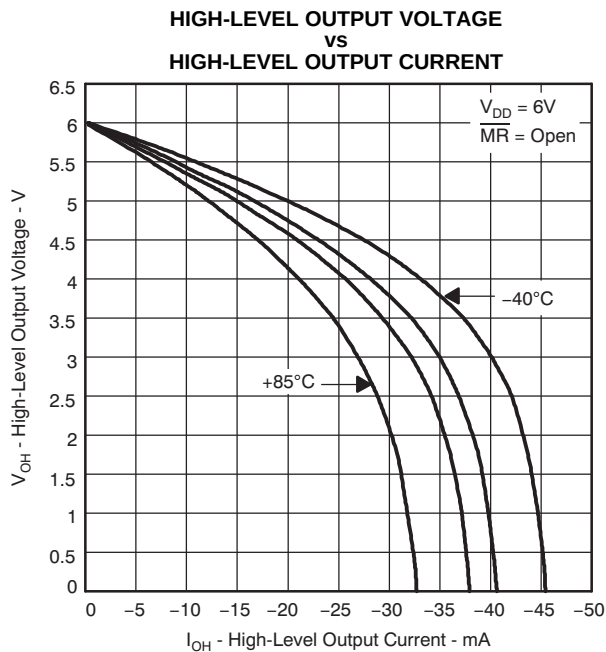


Figure 6.

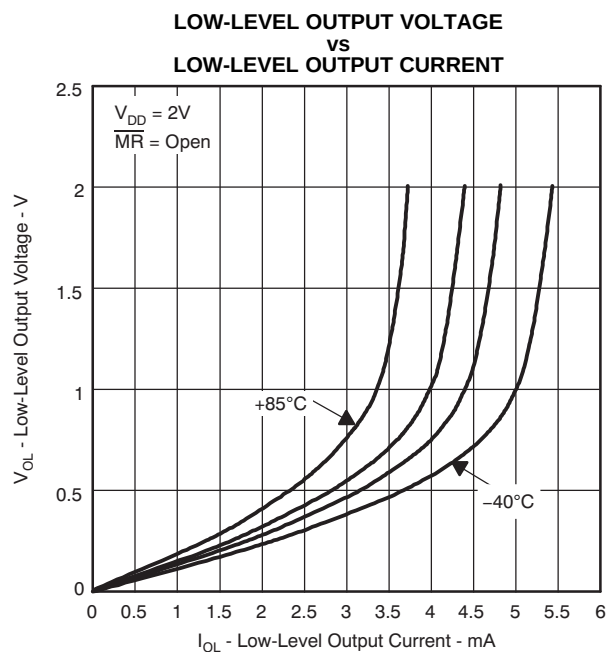


Figure 7.

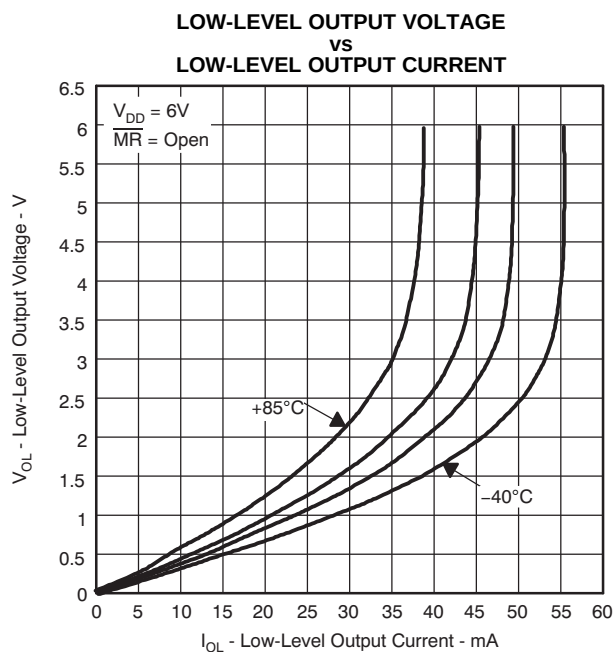


Figure 8.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3305-18D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518
TPS3305-18D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518
TPS3305-18DGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM
TPS3305-18DGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM
TPS3305-18DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM
TPS3305-18DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM
TPS3305-18DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518
TPS3305-18DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518
TPS3305-25D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525
TPS3305-25D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525
TPS3305-25DGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN
TPS3305-25DGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN
TPS3305-25DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN
TPS3305-25DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN
TPS3305-25DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525
TPS3305-25DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525
TPS3305-33D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533
TPS3305-33D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533
TPS3305-33DGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO
TPS3305-33DGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO
TPS3305-33DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO
TPS3305-33DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO
TPS3305-33DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533
TPS3305-33DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

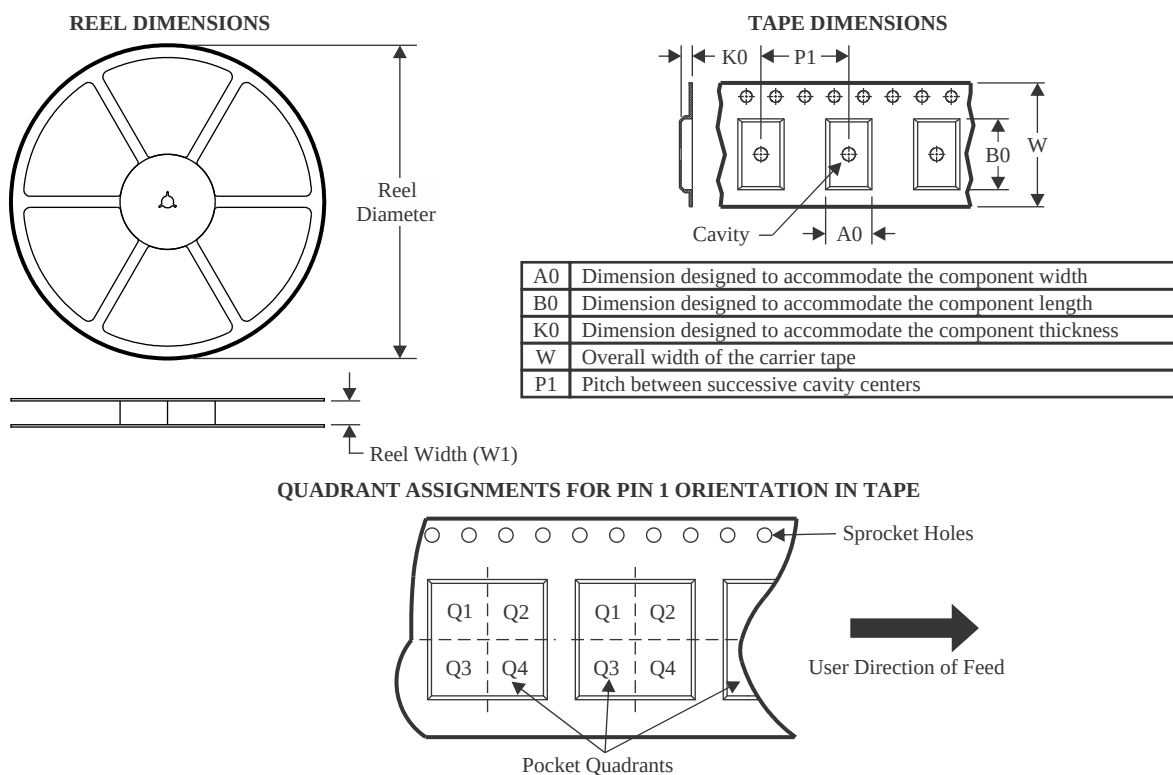
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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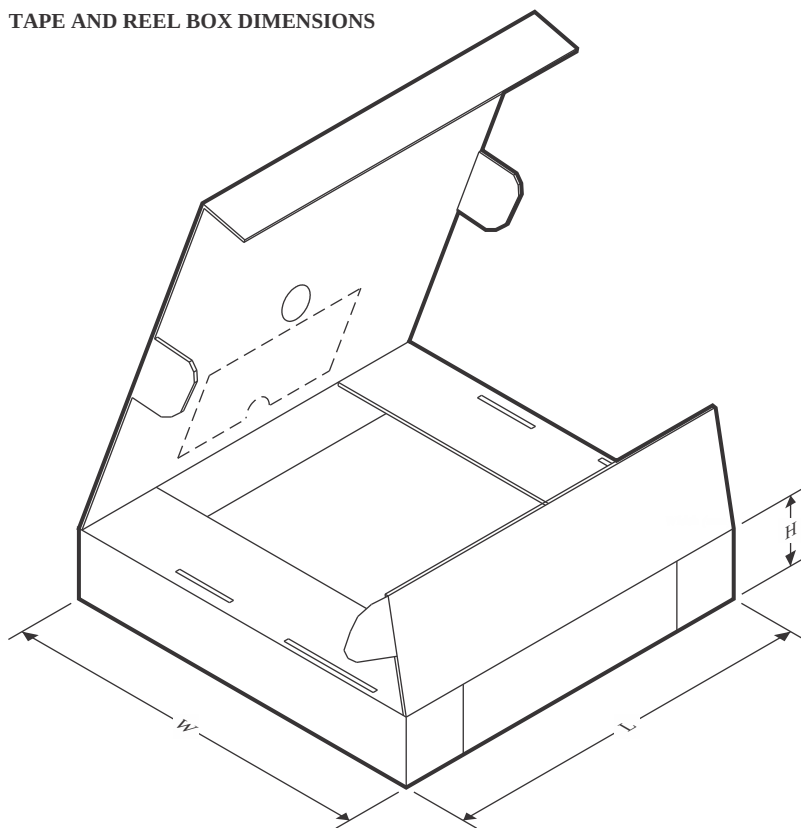
TAPE AND REEL INFORMATION



*All dimensions are nominal

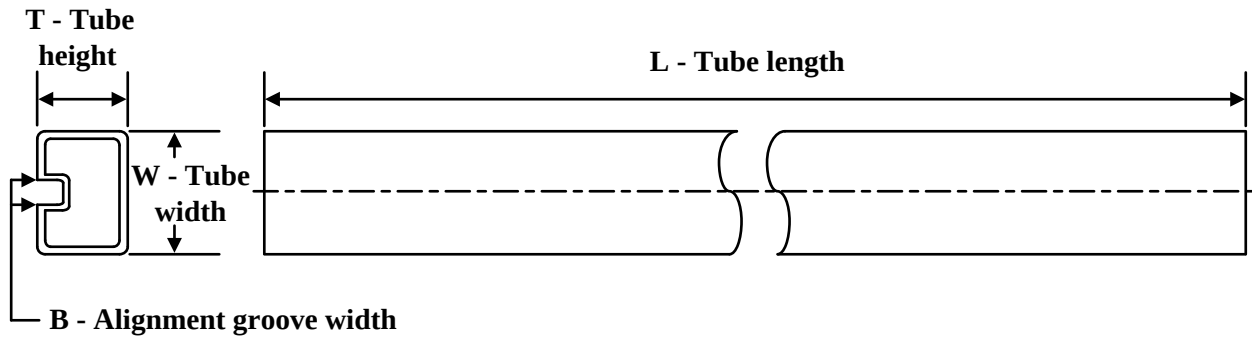
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3305-18DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-18DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-25DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-33DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3305-18DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3305-18DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3305-25DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3305-25DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3305-33DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3305-33DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS3305-18D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3305-18D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3305-18DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3305-18DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3305-25D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3305-25D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3305-25DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3305-25DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3305-33D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3305-33D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3305-33DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3305-33DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5

GENERIC PACKAGE VIEW

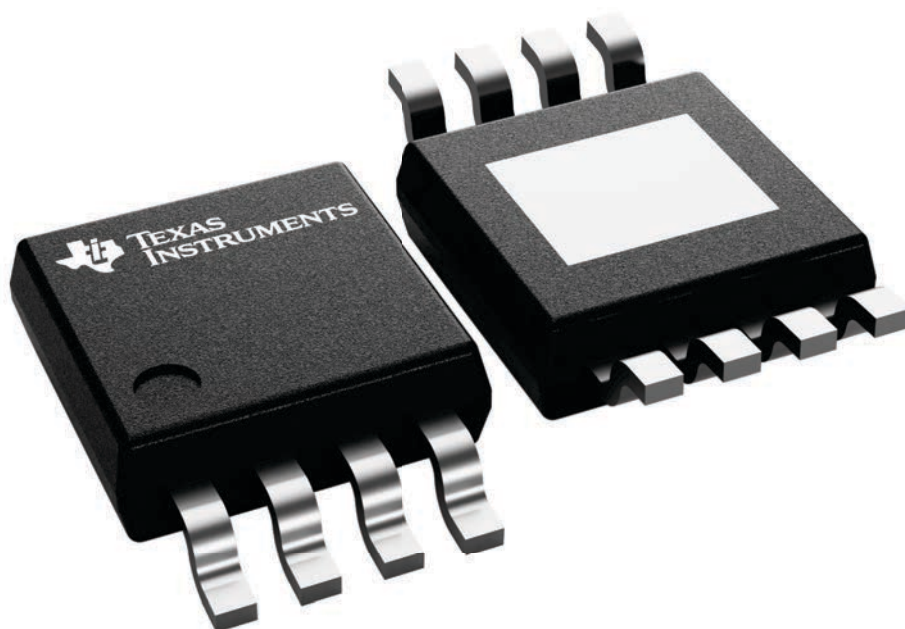
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

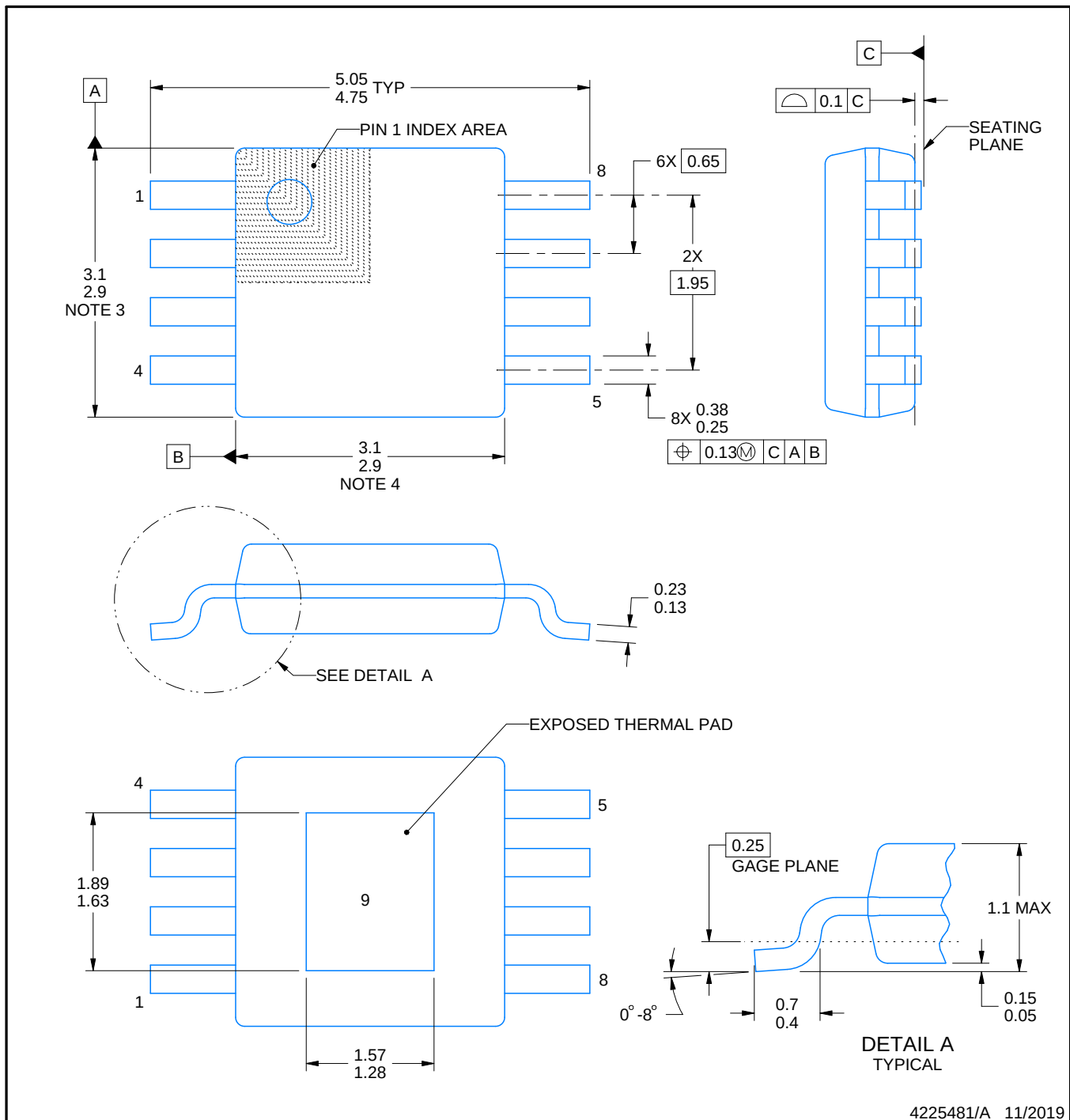
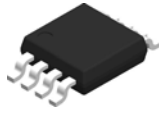
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



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NOTES:

PowerPAD is a trademark of Texas Instruments.

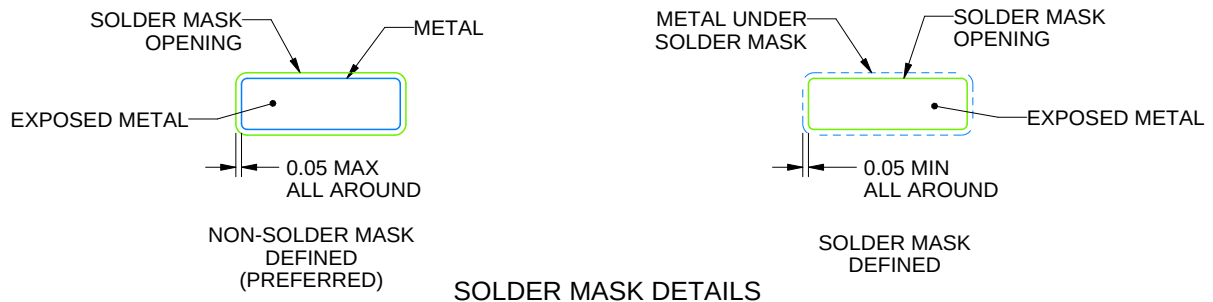
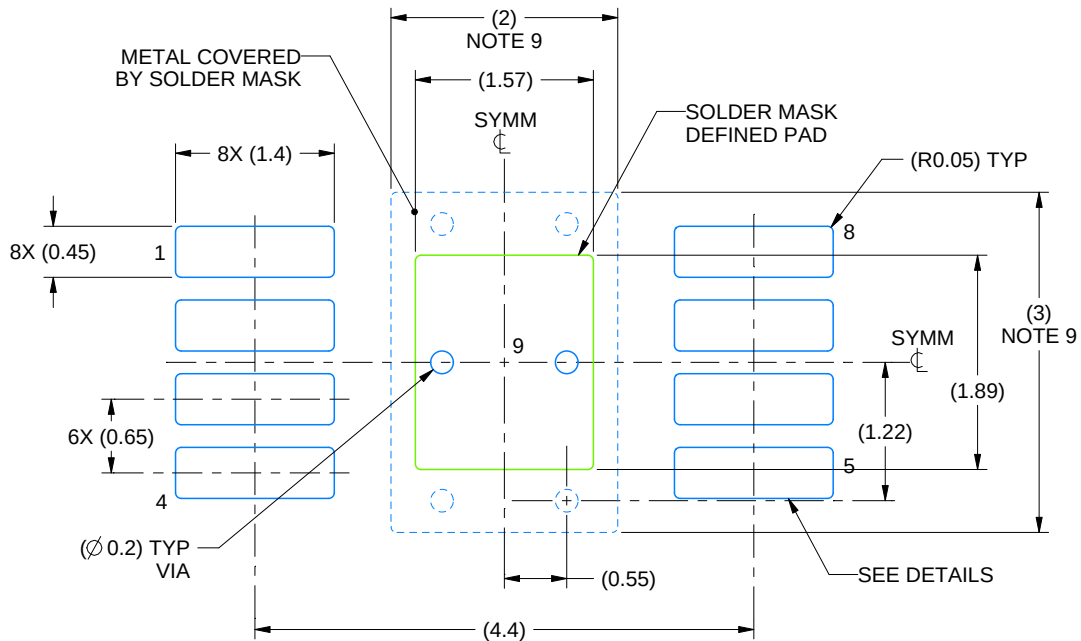
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES: (continued)

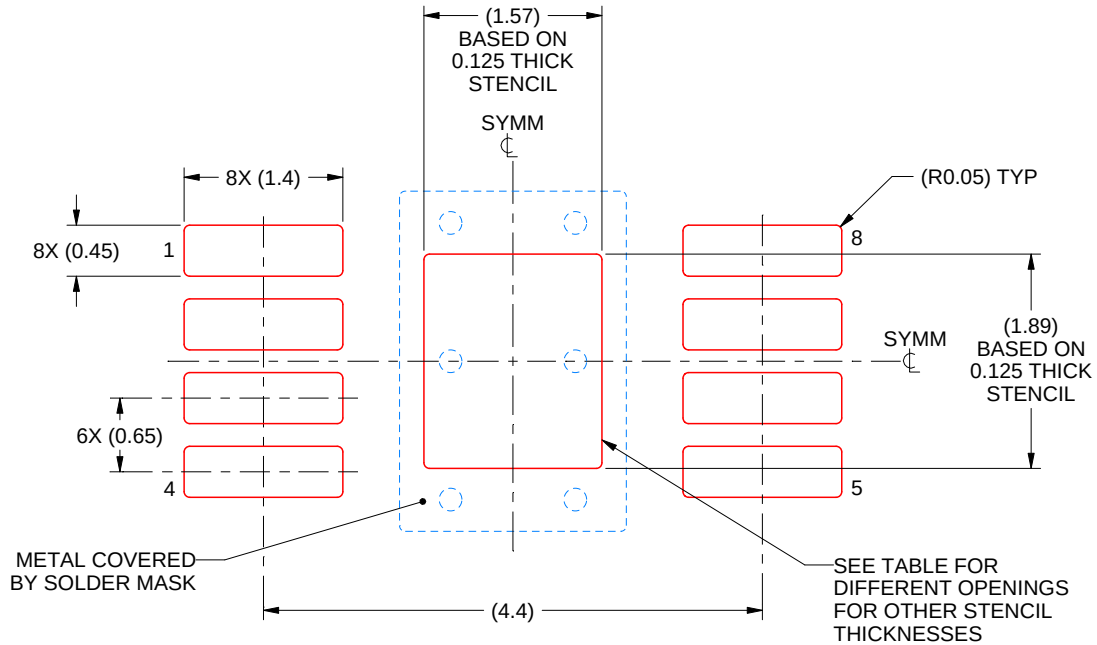
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



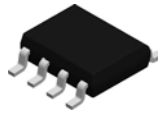
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

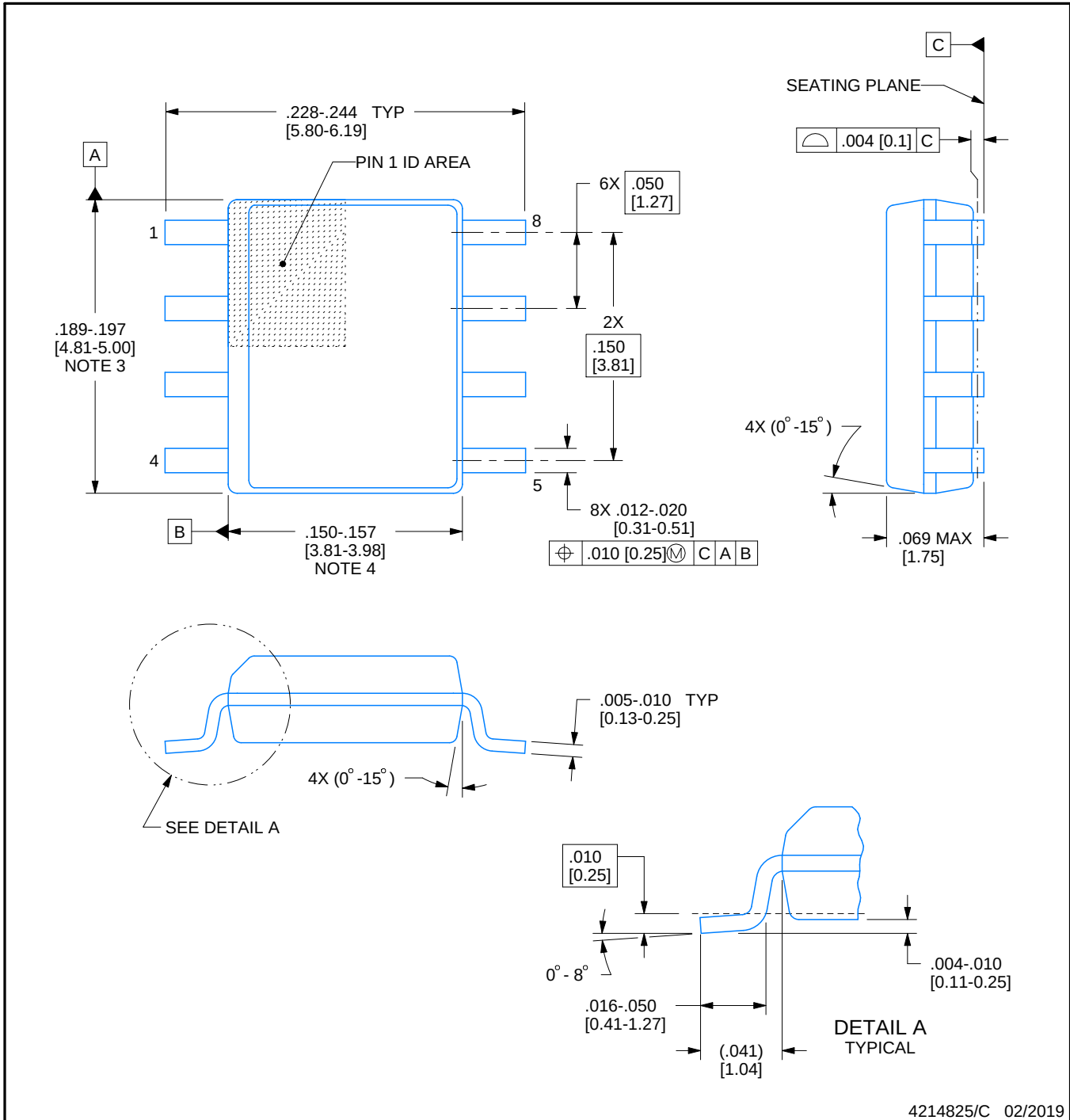


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

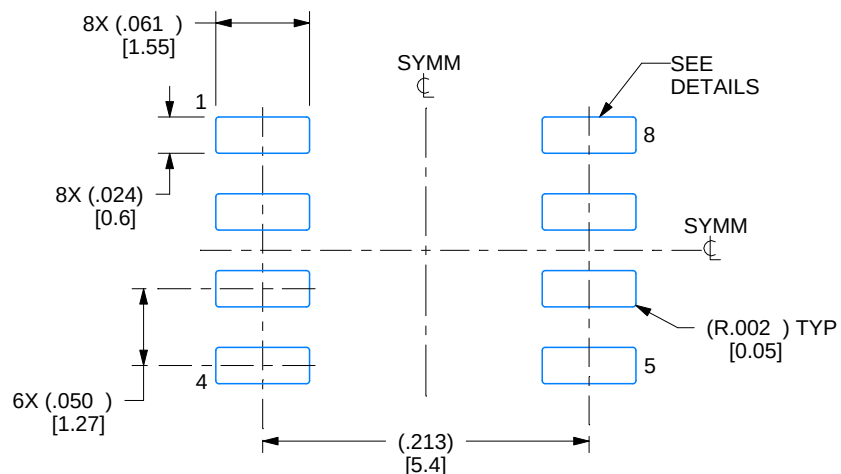
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

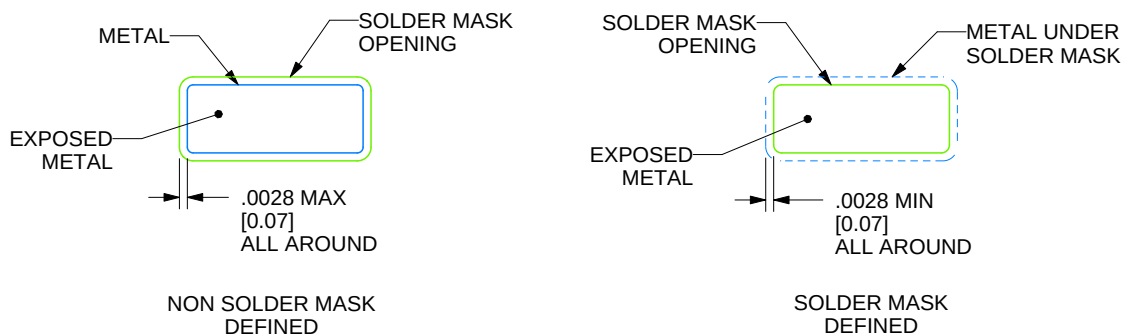
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

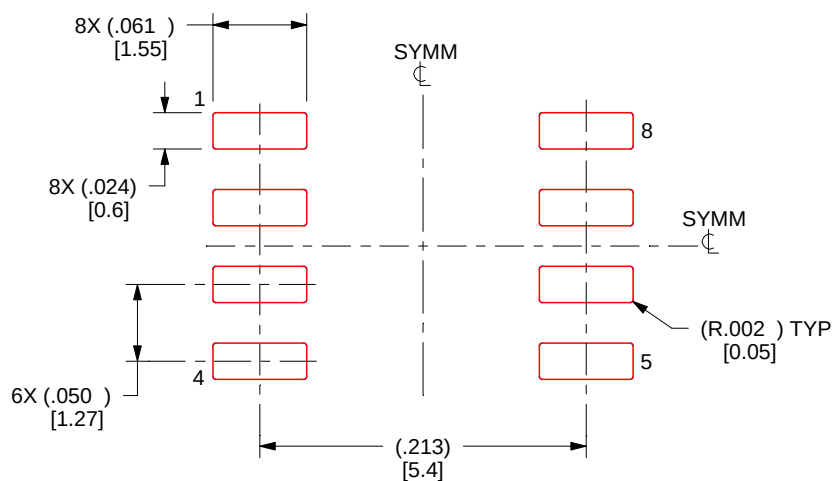
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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