TPS2HCS05-Q1 5mΩ, Automotive Dual-Channel, SPI Controlled High-Side Switch With Integrated I2T Wire Protection and Low Power Mode

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C
  - Withstands 36V load dump
- Dual-channel SPI controlled smart high-side switch with integrated nFETs.
- Integrated wire-harness protection without MCU involvement and a SPI programmable fuse curve
  - Protection against persistent overload condition
- User programmable EEPROM
- Improve system-level reliability through SPI programmable adjustable overcurrent protection
- SPI configurable capacitive charging mode to drive a wide range of capacitive input ECUs load current needs.
- Low quiescent current, low-power ON-state to supply always-ON loads with automatic wake on load current increase with wake signal to MCU
- Robust integrated output protection:
  - Integrated thermal protection
  - Protection against short-to-ground
  - Protection against reverse battery events including automatic switch on of FET with reverse supply voltage
  - Automatic shutoff on loss of battery
  - Integrated output clamp to demagnetize inductive loads
- Digital sense output using SPI is configurable to measure:
  - Load current accurately with integrated ADC
  - Output or supply voltage, FET temperature
- Provides full fault diagnostics through SPI and indication through FLT pin
  - Detection of open load and short-to-battery

2 Applications

- Automotive zone ECU
- Power distribution modules
- Body control modules

3 Description

The TPS2HCS05-Q1 device is a dual-channel, smart high-side switch controlled through a serial peripheral interface (SPI), and is intended for power distribution and actuator drive applications. The device integrates robust protection to establish output wire and load protection against short-circuit or overload conditions. The device features overcurrent protection configurable through SPI, with sufficient flexibility to support loads that require large inrush currents and provide improved protection. The device also integrates a programmable fuse profile (current versus time) that turns off the switch under persistent overload conditions. Together, the two features allow for the optimization of the wire harness for any load profile with full protection.

The device supports an SPI-configurable capacitive charging mode for ECU loads in power distribution switch applications. The device also includes two low-power mode (LPM) states, an auto-entry mode and a manual entry mode, that enables the device to provide current to the load ECU while only consuming from 10µA to 32µA of current.

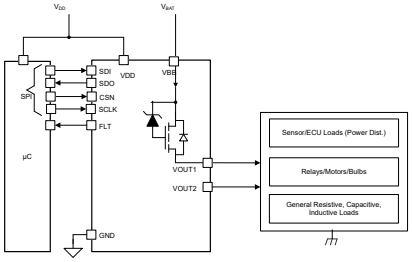
The TPS2HCS05-Q1 device also provides a high-accuracy digital-current sense over SPI that allows for improved load diagnostics. By reporting load current and the channel output voltage and output FET temperature to a system MCU, the device enables the diagnosis of switch and load failures.

The TPS2HCS05-Q1 is available in a HTSSOP package which allows for a reduced PCB footprint.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS2HCS05-Q1	PWC (HTSSOP, 18)	7.8mm × 6.4mm

(1) For more information, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison Table....3
5 Pin Configuration and Functions....4
5.1 Package....4
5.2 Pinout A-version....4
5.3 Version B Package....5
5.4 Pinout B-version....5
6 Specifications....6
6.1 Absolute Maximum Ratings....6
6.2 ESD Ratings....6
6.3 Recommended Operating Conditions....6
6.4 Thermal Information....7
6.5 Electrical Characteristics....7
6.6 SPI Timing Requirements....14
6.7 Switching Characteristics....14
6.8 Typical Characteristics....16
7 Parameter Measurement Information....19
8 Detailed Description....20
8.1 Overview....20
8.2 Functional Block Diagram....21
8.3 Device Functional Modes....21
8.4 Feature Description....50
9 TPS2HCS05-Q1 Registers....72
10 Application and Implementation....125
10.1 Application Information....125
10.2 Typical Application....126
10.3 Power Supply Recommendations....129
10.4 Layout....130
11 Device and Documentation Support....132
11.1 Device Support....132
11.2 Support Resources....132
11.3 Trademarks....132
11.4 Electrostatic Discharge Caution....132
11.5 Glossary....132
12 Revision History....132
13 Mechanical, Packaging, and Orderable Information....132

Copyright © 2026 Texas Instruments Incorporated

4 Device Comparison Table

Table 4-1. Device Options

DEVICE VERSION	PART NUMBER	OUTPUT CONTROL IN ACTIVE STATE	I2T RANGE BASED ON R_{SNS} = 700Ω	OVERCURRENT PROTECTION (I_{OCP}) RANGE	LIMP HOME STATE	PIN 5 FUNCTION (s)
A	TPS2HCS05A-Q1	Set through SPI	**DCR = 1:** 17A^2s to 688A^2s **DCR = 0:** 39A^2s to 1573A^2s	14.5A to 76.2A	Yes	DI / OUT_DIS
B	TPS2HCS05B-Q1	Set through DIx pins only			No	DI1

Note

TPS2HCS05B-Q1 is in preview. Please contact TI for more information.

Copyright © 2026 Texas Instruments Incorporated

5 Pin Configuration and Functions

5.1 Package

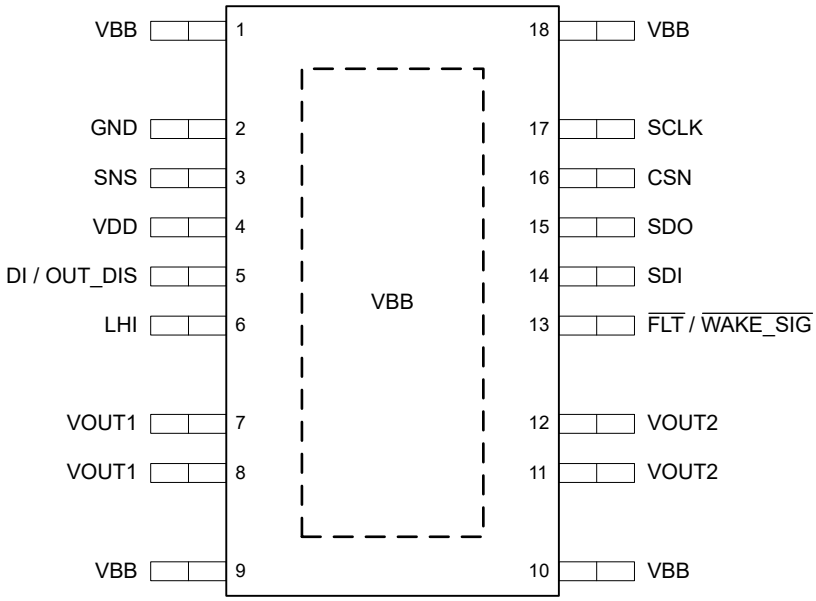


Figure 5-1. PWC Package, 18-Pin HTSSOP (Top View) - TPS2HCS05A-Q1

5.2 Pinout A-version

Pin Number	Pin Name	Type	Description
1	VBB	Power	Power Supply
2	GND	GND	Device ground
3	SNS	O	SNS current output – use a parallel RC network to the GND pin of the IC.
4	VDD	Power	Logic Supply Input – connect a ceramic capacitor to module ground
5	DI / OUT_DIS	I	Configurable through EEPROM through DI_OUT_DIS_FN bit. If programmed as **DI:** Sets the output behavior in the LIMP HOME mode, if configured to do with CHx_LH_IN bits If programmed as **OUT_DIS:** Disables VOUTx if asserted high if OUT_DIS_MASK_CHx = 0. *The pin needs to be connected to MCU or other HI/LO source through a 10K resistor for protection and enabling the reverse polarity FET turn-on function.*
6	LHI	I	External input (active high) to enable LIMP HOME mode.
7, 8	VOUT1	O	Output of channel 1
9, 10	VBB	Power	Power Supply
11, 12	VOUT2	O	Output of channel 2
13	$\overline{\text{FLT}}$ / $\overline{\text{WAKE_SIG}}$	O	Fault output – on any (one or more) channel - open drain, pull up with a 4.7K resistor to VDD pin. Also functions as a wake signal to the MCU upon load current demand in key-off mode.
14	SDI	I	SPI device (secondary) data input
15	SDO	O	SPI Data Output from the device
16	CSN	I	Chip select. Internally pulled up to VDD
17	SCLK	I	SPI Clock input
18	VBB	Power	Power Supply
Thermal Pad	VBB	Power	Power Supply

Copyright © 2026 Texas Instruments Incorporated

5.3 Version B Package

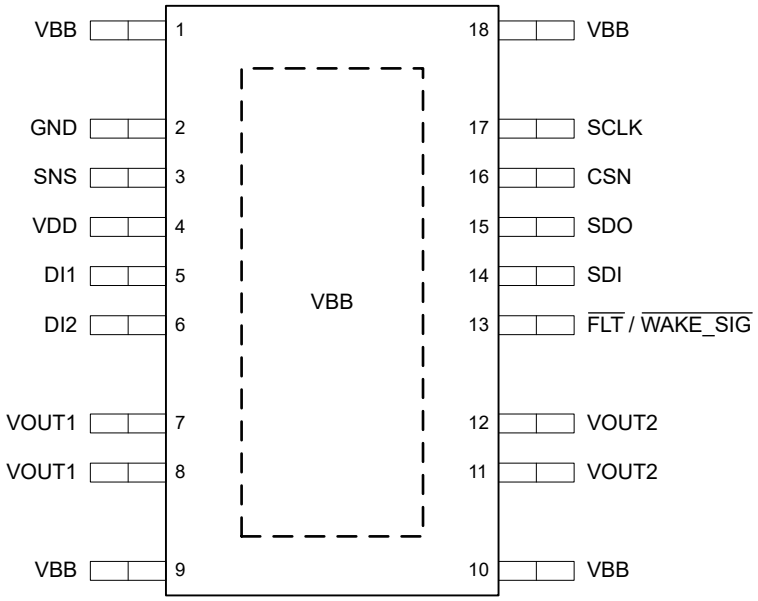


Figure 5-2. PWC Package, 18-Pin HTSSOP (Top View) - TPS2HCS05B-Q1

5.4 Pinout B-version

Pin Number	Pin Name	Type	Description
1	VBB	Power	Power Supply
2	GND	GND	Device ground
3	SNS	O	SNS current output – use a parallel RC network to the GND pin of the IC.
4	VDD	Power	Logic Supply Input – connect a ceramic capacitor to module ground
5	DI1	I	Enables channel 1 output to turn ON. The pin needs to be connected to MCU or other HI/LO source through a 10K resistor for protection and enabling the reverse polarity FET turn-on function.
6	DI2	I	Enables channel 2 output to turn ON
7, 8	VOUT1	O	Output of channel 1
9, 10	VBB	Power	Power Supply
11, 12	VOUT2	O	Output of channel 2
13	$\overline{\text{FLT}}$ / $\overline{\text{WAKE_SIG}}$	O	Fault output – on any (one or more) channel - open drain, pull up with a 4.7K resistor to VDD pin. Also functions as a wake signal to the MCU upon load current demand in key-off mode.
14	SDI	I	SPI device (secondary) data input
15	SDO	O	SPI Data Output from the device
16	CSN	I	Chip select. Active Low. Internally pulled up to VDD
17	SCLK	I	SPI Clock input
18	VBB	Power	Power Supply
Thermal Pad	VBB	Power	Power Supply

Copyright © 2026 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, V_{VBB}			28	V
Load dump voltage	ISO16750-2:2010(E)		36	V
Maximum transient voltage on VBB pin, (example during ISO 7637 pulse 2a transient) V_{BBt}			54	V
VOUT voltage		–30	V_{VS}+0.3	V
Reverse polarity voltage, continuous on VBB pin		–18		V
Low voltage supply pin voltage, V_{DD}		–0.3	7	V
Digital input pin voltages, V_{DIG}	SDI, SDO, SCLK, $\overline{CS}$	–0.3	7	V
Sense pin voltage, V_{SNS}		–0.3	7	V
$\overline{FLT}$ pin voltage, $V_{\overline{FLT}}$		–0.3	7	V
Limp home activation pin voltage, V_{LHI}			V_{BB}	V
Limp home direct input pin voltages, V_{DI}		–0.3	7	V
Reverse ground current, I_{GND}	V_{BB} < 0V		–50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002 Classification Level H2	All pins including VBB and VOUTx	±2000	V
		Human-body model (HBM), per AEC Q100-002 Classification Level H3A(2)	VBB and VOUTx	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.
(2) ESD strikes are with reference from the pin mentioned to GND

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BB_NOM}	Nominal supply voltage		6	18	V
V_{BB_EXT}	Extended supply voltage	See the conditions in Power Supply Recommendations, operating voltage range	3	28	V
V_{DD}	Low voltage supply voltage		3.0	5.5	V
V_{DIG}	All digital input pin voltage		–0.3	5.5	V
$V_{\overline{FLT}}$	$\overline{FLT}$ pin voltage		–0.3	5.5	V
V_{LHI}	Limp home activation pin voltage, LHI		–0.3	V_{BB}	V
V_{DI}	Limp home direct pin input voltage, DI		–0.3	5.5	V
T_A	Operating free-air temperature		–40	125	°C

Copyright © 2026 Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS2HCS05-Q1 PWC 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{Clamp}	VDS clamp voltage	V_{BB} > 28V, I_{OUT} = 10mA,	T_J = 25°C to 150°C	35	40	45	V
		12V < V_{BB} ≤ 28V, I_{OUT} = 10mA	T_J = –40°C to 150°C	30	34	38	V
		V_{BB} = 3V, I_{OUT} = 10mA	T_J = –40°C to 150°C	27.5		36.5	V
V_{BB_UVLOR}	V_{BB} undervoltage lockout rising	Measured with respect to the GND pin of the device.		3.0	3.9	4.2	V
V_{BB_UVLOF}	V_{BB} undervoltage lockout falling			2.6	2.8	3.05	V
$V_{BB_UV_WRN_R}$	VBB voltage UV_WRN rising threshold	Measured with respect to the GND pin of the device.			4.9		V
$V_{BB_UV_WRN_F}$	VBB voltage UV_WRN falling threshold threshold				4.5		V
V_{DD_UVLOR}	V_{DD} undervoltage lockout rising	Measured with respect to the GND pin of the device		2.81		3.11	V
V_{DD_UVLOF}	V_{DD} undervoltage lockout falling			2.7		3.03	V
V_{DD_UVLOH}	V_{DD} undervoltage lockout hysteresis				0.09		V
$I_{SLEEP,VBB}$	Sleep current (total device leakage including all MOSFET channels)	Device in SLEEP state, V_{OUT} = 0V	T_J = 25°C			1.5	µA
			T_J = 85°C			9.8	µA
$I_{OUT(OFF)}$	Output leakage current (per channel)	V_{OUT} = 0V Channel disabled, ACTIVE state	T_J = –40 to 125°C			42	µA
$I_{Q,VDD}$	VDD quiescent current	ACTIVE state, SCLK off	V_{DD} = 5.5V			1.66	mA
			V_{DD} = 3.0V			70	µA

Copyright © 2026 Texas Instruments Incorporated

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q,VBB}$	V_{BB} quiescent current	All channels enabled, I_{OUTx} = 0A, SCLK off, Diagnostics disabled	V_{DD} = 5.5V		3.3	4	mA
			V_{DD} = 3.0V		3.8	4.6	mA
		All channels enabled, I_{OUTx} = 0A, SCLK off, Diagnostics enabled (ISNS, ADC)	V_{DD} = 5.5V		4.3	6	mA
		All channels enabled, I_{OUTx} = 0A, SCLK off, Diagnostics enabled (ISNS, ADC)	V_{DD} = 0V		4.8	6	mA
$I_{L,CONT}$	Continuous load current, per channel	All channels enabled, T_{AMB} = 85°C			12		A
		One channel enabled, T_{AMB} = 85°C			17		A
RON CHARACTERISTICS							
R_{ON_OL}	On-resistance, OL ON mode	6V ≤ V_{BB} ≤ 28V, I_{OUTx} = 0.3A, OL_ON_EN_CHx = 1	T_J = 25°C		28.4		mΩ
			T_J = 150°C			55.3	mΩ
R_{ON}	On-resistance	6V ≤ V_{BB} ≤ 28V, I_{OUTx} = 1A	T_J = 25°C		6		mΩ
			T_J = 150°C			12.5	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	–18V ≤ V_{BB} ≤ –7V V_{DI} = 8V	T_J = 25°C		6.5		mΩ
			T_J = 150°C			15	mΩ
CURRENT SENSE CHARACTERISTICS							
K_{SNS1}	Current sense ratio I_{OUTx} / I_{SNS}	I_{OUT} = 2.0A, OL_ON_EN_CHx = 0			6500		
K_{SNS2}	Current sense ratio I_{OUTx} / I_{SNS}	I_{OUT} = 200mA, OL_ON_EN_CHx = 1			1150		
I_{SNS_SAT}	Saturated sense current	V_{BB} > 6V, R_{SNS} = 374Ω OL_ON_EN_CHx =0	I_{OUT} = > 42A		7		mA
K_{SNS1}	K_{SNS1} ratio I_{OUT} / I_{SNS1} across I_{OUT}	RSNS = 374Ω OL_ON_EN_CHx = 0	I_{OUT} = 40A		6500		
				-6		6	%
		RSNS = 698Ω OL_ON_EN_CHx = 0	I_{OUT} = 20A		6500		
				-6		6	%
			I_{OUT} = 10A		6500		
				-6		6	%
			I_{OUT} = 5A		6500		
				-6		6	%
			I_{OUT} = 3A		6500		
				-6		6	%
			I_{OUT} = 1A		6500		
				-7		7	%
			I_{OUT} = 500mA		6500		
				-9		9	%

Copyright © 2026 Texas Instruments Incorporated

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
K_{SNS2}	K_{SNS2} ratio I_{OUT} / I_{SNS2} across I_{OUT}	RSNS = 698Ω OL_ON_EN_CHx = 1	I_{OUT} = 200mA		1150		
				-11		11	%
			I_{OUT} = 100mA		1150		
				-14		14	%
			I_{OUT} = 40mA		1150		
				-20		20	%
			I_{OUT} = 20mA		1150		
				-35		35	%
IENTRY_OL_ON	IOUT current to enter OL_ON mode (OL_ON_EN_CHx = 1)				0.5		A
IEXIT_OL_ON	IOUT current to exit OL_ON mode (OL_ON_EN_CHx = 1)				1.5		A
ADC CHARACTERISTICS							
$V_{ADCREFHI}$	ADC reference voltage			2.73	2.82	2.93	V
Isample	Current sense sampling time	Including mux timing and ADC conversion time		50			µs
SNS CHARACTERISTICS							
$ISNS_{ADC,ACC}$	ISNS ADC accuracy	OL_ON_EN_CHx =0, ISNS_SCALE_CHx = 0	SNS pin voltage = 2.7V	-4.6		2.7	%
			SNS pin voltage = 1.4V	-4.8		3.2	%
			SNS pin voltage = 0.7V	-5.5		3.6	%
			SNS pin voltage = 0.1V	-30		23.7	%
		OL_ON_EN_CHx =1, ISNS_SCALE_CHx = 1	SNS pin voltage = 0.04V	-31		25	%
$TSNS_{ACC}$	T_{SNS} measurement accuracy	T_J = 25°C		-15.7		18.2	°C
$VSNS_{ACC}$	VOUT SNS (VSNS) measurement accuracy	VBB = 13.5V		-6.5		6.5	%
$VBBSNS_{ACC}$	VBB SNS (VBBSNS) measurement accuracy	VBB = 13.5V		-5.1		5.1	%
OVERCURRENT PROTECTION CHARCTERISTICS							
I_{OCP_RANGE}	Overcurrent protection threshold, immediate shutdown mode - range	VBB = 13.5V		14.5		76.2	A
I_{OCP}	Overcurrent protection threshold, immediate shutdown mode, enable into short	L_{IN} = 0.1µH L_{OUT} = 1µH T_J = –40°C to 150°C	ILIMIT_SET_CHx = 0x0		14.5		A
			ILIMIT_SET_CHx = 0x1		18.2		A
			ILIMIT_SET_CHx = 0x2		20.5		A
			ILIMIT_SET_CHx = 0x3		24.2		A
			ILIMIT_SET_CHx = 0x4		28.5		A
			ILIMIT_SET_CHx = 0x5		30.6		A
			ILIMIT_SET_CHx = 0x6		33.5		A
			ILIMIT_SET_CHx = 0x7		44.3		A
			ILIMIT_SET_CHx = 0x8		53.4		A
			ILIMIT_SET_CHx = 0x9		66		A
			ILIMIT_SET_CHx = 0xA		76.2		A
$I_{OCP_RETRY_FLBK}$	Overcurrent protection foldback threshold, immediate shutdown mode	Applicable to only I_{OCP} > 66A, $n_{RETRY,INT}$ > 6, L_{OUT} = 5µH, T_J = –40°C to 150°C			66		A
$I_{OCP_VBB_COMP}$	I_{OCP} V_{BB} compensation	V_{BB} > 19V, I_{OCP} > 66A only			66		A

Copyright © 2026 Texas Instruments Incorporated

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{OCP_DETECT}	Immediate shutdown detection time	T_J = -40°C to 150°C	From I_{OUT} = I_{OCP} to I_{OCP} detection R_{OUT} = 150% of I_{OCP} , L_{IN} = 0nH, L_{OUT} = 0nH	0.3	0.45	1.45	us
t_{OCP_TOFF}	Immediate shutdown turn off time	T_J = -40°C to 150°C	From I_{OCP} detection to 10% of V_{OUTx} R_{OUT} = 150% of I_{OCP} , L_{IN} = 0nH, L_{OUT} = 0nH		2	3	us
CAP CHRG CURRENT LIMITATION							
I_{CL_Reg}	Regulation mode current	T_J = –40°C to 150°C	INRUSH_LIMIT_CHx = 0		2		A
			INRUSH_LIMIT_CHx = 1		2.3		A
			INRUSH_LIMIT_CHx = 2		2.7		A
			INRUSH_LIMIT_CHx = 3		3.2		A
			INRUSH_LIMIT_CHx = 4		3.7		A
			INRUSH_LIMIT_CHx = 5		4.2		A
			INRUSH_LIMIT_CHx = 6		4.6		A
			INRUSH_LIMIT_CHx = 7		6.2		A
			INRUSH_LIMIT_CHx = 8		7.6		A
			INRUSH_LIMIT_CHx = 9		9.1		A
			INRUSH_LIMIT_CHx = A		10.6		A
			INRUSH_LIMIT_CHx = B		12.1		A
			INRUSH_LIMIT_CHx = C		13.5		A
			INRUSH_LIMIT_CHx = D		15.1		A
			INRUSH_LIMIT_CHx = E		16.7		A
			INRUSH_LIMIT_CHx = F		18.2		A
CAPACITIVE CHARGING							
t_{INRUSH_RANGE}	Inrush duration settings range	INRUSH_DURATION_CHx range		0		100	ms
FAULT CHARACTERISTICS							
I_{OL_OFF}	Off state open-load (OL) detection internal pull-up current	Switch disabled, OL_OFF_EN_CHx = enabled	OL_PU_STR_CHx=00	19	27	67	µA
			OL_PU_STR_CHx=01	46	62	108	µA
			OL_PU_STR_CHx=10	100	128	189	µA
			OL_PU_STR_CHx=11	212	270	358	µA
R_{SHRT_VBB}	Off state short to VBB detection pulldown resistance	Channel disabled, off-state short_VBB diagnostics enabled		6	7.5	9	kΩ
$V_{DS_LT_2V}$	Drain-to-source (V_{DS}) detection voltage	Channel enabled, t > t_{VDS_DEGL}		1.9	2.7	2.97	V
t_{VDS_DEGL}	Drain-to-source (V_{DS}) detection deglitch time	Deglitch time until VDS detection is active after channel is enabled and out of inrush period (if configured)			1		ms
$V_{OL_OFF_TH}$	Off state Open-load (OL) and short to battery detection voltage	Channel Disabled, off-state open load or short to battery diagnostics enabled, V_{OUTx}		1.9	2.7	2.97	V
T_{ABS}	Thermal shutdown			155	180		°C
T_{OTW}	Thermal shutdown warning				145		°C
T_{REL}	Relative thermal shutdown temperature				100		°C
$t_{RETRY,\ INT}$	Retry time in initial retry window	Time from fault shutdown until switch re-enable (thermal shutdown or I_{OCP})			2		ms

Copyright © 2026 Texas Instruments Incorporated

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$n_{RETRY, INT}$	Number of retry cycles in initial retry window				6		
$t_{RETRY, EXTD}$	Retry time in extended overcurrent retry window	Time from fault shutdown until switch re-enable (thermal shutdown or I_{OCP_FLBK})			20		ms
$n_{RETRY, EXTD}$	Number of retry cycles in extended overcurrent retry window				7		
t_{WAKE_SIG}	WAKE_SIG / FLT pin indication for exit from MANUAL_LPM due to a load step				100		µs
PWM CHARACTERISTICS							
PWM_{FREQ}	PWM Frequency	PWM_EN = 1	PWM_FREQ_CHx = 000	0.76	0.86	0.96	Hz
PWM_{FREQ}	PWM Frequency	PWM_EN = 1	PWM_FREQ_CHx = 111	1566	1765	1956	Hz
LOW POWER MODE CHARACTERISTICS							
R_{ON,LPM_AUTO}	R_{ON} in AUTO_LPM mode		T_J = –40°C to 125°C		5.6		mΩ
R_{ON,LPM_MAN}	R_{ON} in MANUAL_LPM mode	MANUAL_LPM_MODE = 0	T_J = –40°C to 125°C		23.7		mΩ
	R_{ON} in MANUAL_LPM mode	MANUAL_LPM_MODE = 1	T_J = –40°C to 125°C		5.6		mΩ
$I_{ENTRY_LPM_AUTO}$	I_{OUT} current to enter AUTO_LPM state	AUTO_LPM_ENTRY = 1	T_J = –40°C to 150°C		1.4		A
$I_{EXIT_LPM_AUTO}$	I_{OUT} current to exit AUTO_LPM state	AUTO_LPM_ENTRY = 1	T_J = –40°C to 150°C		2.1		A
$I_{EXIT_LPM_MAN}$	IOUTx current to exit MANUAL_LPM state	MANUAL_LPM_MODE = 0 Current ramp at 1mA/µs	MAN_LPM_EXIT_CURR_CHx = 00		0.95		A
			MAN_LPM_EXIT_CURR_CHx = 01		1.2		A
			MAN_LPM_EXIT_CURR_CHx = 10		0.33		A
			MAN_LPM_EXIT_CURR_CHx = 11		0.64		A
		MANUAL_LPM_MODE = 1 Current ramp at 1mA/µs	MAN_LPM_EXIT_CURR_CHx = 00		3.1		A
			MAN_LPM_EXIT_CURR_CHx = 01		4.1		A
			MAN_LPM_EXIT_CURR_CHx = 10		1		A
			MAN_LPM_EXIT_CURR_CHx = 11		2		A

Copyright © 2026 Texas Instruments Incorporated

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{ENTRY_LPM_MAN}$	IOUTx current to enter MANUAL_LPM state	MANUAL_LPM_MODE = 0	MAN_LPM_EXIT_CURR_CHx = 00		0.85		A
			MAN_LPM_EXIT_CURR_CHx = 01		1.1		A
			MAN_LPM_EXIT_CURR_CHx = 10		0.3		A
			MAN_LPM_EXIT_CURR_CHx = 11		0.56		A
		MANUAL_LPM_MODE = 1	MAN_LPM_EXIT_CURR_CHx = 00		3		A
			MAN_LPM_EXIT_CURR_CHx = 01		4		A
			MAN_LPM_EXIT_CURR_CHx = 10		1		A
			MAN_LPM_EXIT_CURR_CHx = 11		2		A
$I_{SCP_LPM_AUTO}$	Short-circuit detection threshold for AUTO_LPM state	AUTO_LPM_ENTRY = 1 Current ramp at 2.5A/µs	T_J = –40°C to 150°C		25		A
$I_{SCP_LPM_MAN}$	Short-circuit detection threshold in MANUAL_LPM	MANUAL_LPM_MODE = 0 Current ramp at 1A/µs	T_J = –40°C to 150°C		9		A
		MANUAL_LPM_MODE = 1 Current ramp at 2.5A/µs			25		A
$t_{SCP_DETECT_MANUAL}$	Short-circuit detection time in MANUAL_LPM	MANUAL_LPM_MODE = 0			1.1		µs
		MANUAL_LPM_MODE = 1 Large			2.6		µs
$t_{SCP_OFF_MANUAL}$	Short-circuit detection shutdown time in MANUAL_LPM	MANUAL_LPM_MODE = 0			2.1		µs
		MANUAL_LPM_MODE = 1 Large			4.3		µs
$t_{SCP_DETECT_AUTO}$	Short-circuit detection time in AUTO_LPM				2.1		µs
$t_{SCP_OFF_AUTO}$	Short-circuit detection shutdown time in AUTO_LPM				4.3		µs
t_{RETRY_LPM}	Retry time after a $I_{SCP_LPM_MAN}$ detection in manual LPM state				100		µs
$t_{STBY_LPM_AUTO}$	standby time before enter AUTO_LPM state	$I_{OUTx} \le I_{ENTRY_LPM_AUTO}$			20		ms
t_{WAKE}	$I_{EXIT_LPM_MAN}$ detection time				0.5		µs
t_{SLEW}	Time to slew on the main FET after $I_{EXIT_LPM_MAN}$	MANUAL_LPM_MODE = 0			200		µs
t_{LPM_ENTRY}	Time to enter LPM state				200		µs
I_{Q,VDD,LPM_MAN}	VDD quiescent current in MANUAL_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C MANUAL_LPM_MODE = 0	both channels OFF		9.1	16.7	µA
			one channel ON		12.8	20.2	µA
			both channels ON		16.4	24	µA
		V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C MANUAL_LPM_MODE = 1	both channels OFF		9.7	17.4	µA
			one channel ON		13.4	21.6	µA
			both channels ON		17.2	25.1	µA
I_{Q,VDD,LPM_AUTO}	VDD quiescent current in AUTO_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C	both channels OFF		9.5	16.3	µA
			one channel ON		13.2	20.2	µA
			both channels ON		16.9	23.6	µA

Copyright © 2026 Texas Instruments Incorporated

V_{BB} = 6V to 18V, V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{Q,VBB,LPM_MAN}	VBB quiescent current in MANUAL_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C MANUAL_LPM_MODE = 0	both channels OFF		9.5	20.7	µA
			one channel ON		11	17.7	µA
			both channels ON		12.3	16.2	µA
		V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C MANUAL_LPM_MODE = 1	both channels OFF		11	20.9	µA
			one channel ON		12.6	19.3	µA
			both channels ON		14	18	µA
I_{Q,VBB,LPM_AUTO}	VBB quiescent current in AUTO_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, T_J = –40°C to 85°C	both channels OFF		11	19.3	µA
			one channel ON		12.4	18.3	µA
			both channels ON		13.8	19	µA
		V_{DD} = 0V, I_{OUTx} = 0A, T_J = –40°C to 85°C	both channels OFF		20.5	33.6	µA
			one channel ON		25.5	36.5	µA
			both channels ON		30.5	39.5	µA
DIGITAL INPUT PIN CHARACTERISTIC							
$V_{IH,SPI}$	Input voltage high-level (SCLK, SDI, CSN)	3.0V ≤ VDD ≤ 5.5V	3.0V ≤ VDD ≤ 5.5V	0.7 × V_{DD}			V
$V_{IL,SPI}$	Input voltage low-level (SCLK, SDI, CSN)	3.0V ≤ VDD ≤ 5.5V	3.0V ≤ VDD ≤ 5.5V			0.3 × V_{DD}	V
$R_{PD,SCLK}$	SCLK Internal pulldown resistor			1.6	1.9	2.3	MΩ
$I_{IH,SCLK}$	Input current high-level	SCLK	V_{SCLK} = 5V		2.5		µA
$R_{PD,SDI}$	SDI Internal pulldown resistor			1.6	1.9	2.3	MΩ
$I_{IH,SDI}$	Input current high-level	SDI	V_{SDI} = 5V		2.5		µA
$R_{PU,CSN}$	CSN Internal pullup resistor			77	90	97	kΩ
$V_{IH,DI}$	input voltage high-level	DI (version A)		1.65			V
$V_{IL,DI}$	Input voltage low-level					1.1	V
$R_{PD,DI}$	Internal pulldown resistor			659	850	963	kΩ
$I_{IH,DI}$	Input current high-level		V_{DI} = 5V		6		µA
$V_{IH,DI1}$	input voltage high-level	DI1 (version B)		1.65			V
$V_{IL,DI1}$	Input voltage low-level					1.1	V
$R_{PD,DI1}$	Internal pulldown resistor			659	850	962	kΩ
$I_{IH,DI1}$	Input current high-level		V_{DI1} = 5V		6		µA
$V_{IH,LHI}$	input voltage high-level	LHI (version A)		1.65			V
$V_{IL,LHI}$	Input voltage low-level					1.1	V
$R_{PD,LHI}$	Internal pulldown resistor			269	350	433	kΩ
$I_{IH,LHI}$	Input current high-level		V_{LHI} = 5V		14		µA
$V_{IH,DI2}$	input voltage high-level	DI2 (version B)		1.65			V
$V_{IL,DI2}$	Input voltage low-level					1.1	V
$R_{PD,DI2}$	Internal pulldown resistor			659	850	962	kΩ
$I_{IH,DI2}$	Input current high-level		V_{DI2} = 5V		6		µA
DIGITAL OUTPUT PIN CHARACTERISTICS							
V_{OH_SDO}	Output logic high voltage drop	SDO pin current = 2mA				0.22	V
$V_{OL,SDO}$	Output logic low voltage	SDO Pin current = 2mA				0.2	V
V_{OL_FLT}	Output logic high voltage drop	$\overline{FLT}$ pin current = 4mA				0.62	V

Copyright © 2026 Texas Instruments Incorporated

6.6 SPI Timing Requirements

Over operating junction temperature T_J = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SPI}	SPI clock (SCLK) frequency	C_{SDO} = 30pF, R_{SDO} = 768Ω			8	MHz
t_{SPI}	SPI clock (SCLK) period	C_{SDO} = 30pF, R_{SDO} = 768Ω	125			ns
t_{high}	High time: SCLK logic high-time duration		45			ns
t_{low}	Low time: SCLK logic low-time duration		45			ns
t_{sucs}	$\overline{CS}$ setup time: time delay between falling edge of $\overline{CS}$ and rising edge of SCLK		45			ns
t_{su_SDI}	SDI setup time: setup time of SDI before the falling edge of SCLK		15			ns
t_{h_SDI}	SDI hold time: hold time of SDI before the falling edge of SCLK		30			ns
t_{d_SDO}	Delay time: time delay from rising edge of SCLK to data valid at SDO				30	ns
t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of $\overline{CS}$		45			ns
t_{dis_cs}	$\overline{CS}$ disable time, $\overline{CS}$ high to SDO high impedance			10		ns
t_{hics}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high		500			ns

6.7 Switching Characteristics

V_{BB} = 13.5V, R_L = 2Ω, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Channel turnon delay time	50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 00		48		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 01		36		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 10 (default)		48		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 11		36		µs
t_{DF}	Channel turnoff delay time	50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 00		45		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 01		26		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 10 (default)		24		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 11		16		µs
SR_R	VOUT rising slew rate	20% to 80% of V_{OUT}, SLRT_CHx = 00		0.13		V/µs
		20% to 80% of V_{OUT}, SLRT_CHx = 01		0.22		V/µs
		20% to 80% of V_{OUT}, SLRT_CHx = 10		0.13		V/µs
		20% to 80% of V_{OUT}, SLRT_CHx = 11		0.22		V/µs
SR_F	VOUT falling slew rate	80% to 20% of V_{OUT}, SLRT_CHx = 00		0.15		V/µs
		80% to 20% of V_{OUT}, SLRT_CHx = 01		0.28		V/µs
		80% to 20% of V_{OUT}, SLRT_CHx = 10		0.3		V/µs
		80% to 20% of V_{OUT}, SLRT_CHx = 11		0.47		V/µs
t_{ON}	Channel turnon time	50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx= 00		138		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx= 01		93		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx=10 (default)		138		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx=11		93		µs

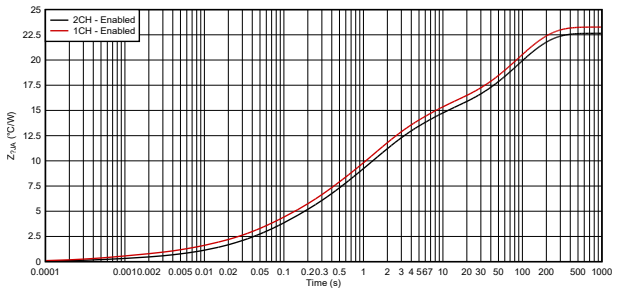
Copyright © 2026 Texas Instruments Incorporated

V_{BB} = 13.5V, R_L = 2Ω, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	Channel turnoff time	50% of CS or DI to 10% of VOUT, SLRT_CHx = 00		115		µs
		50% of CS or DI to 10% of VOUT, SLRT_CHx = 01		63		µs
		50% of CS or DI to 10% of VOUT, SLRT_CHx = 10		58		µs
		50% of CS or DI to 10% of VOUT, SLRT_CHx = 11		38		µs
$t_{OFF_OUT_DIS}$	OUT_DIS channel turnoff time	50% of OUT_DIS to 10% of VOUT, DI_OUT_DIS_FN = 1, OUT_DIS_MASK_CHx = 0			40.5	µs
E_{ON}	Switching energy losses during turn on	10% to 90% of VOUT, SLRT_CHx = 00		0.87		mJ
	Switching energy losses during turn on	10% to 90% of VOUT, SLRT_CHx = 01		0.6		mJ
	Switching energy losses during turn on	10% to 90% of VOUT, SLRT_CHx = 10		0.87		mJ
	Switching energy losses during turn on	10% to 90% of VOUT, SLRT_CHx = 11		0.6		mJ
E_{OFF}	Switching energy losses during turn off	90% to 10% of VOUT, SLRT_CHx = 00		0.85		mJ
	Switching energy losses during turn off	90% to 10% of VOUT, SLRT_CHx = 01		0.56		mJ
	Switching energy losses during turn off	90% to 10% of VOUT, SLRT_CHx = 10		0.40		mJ
	Switching energy losses during turn off	90% to 10% of VOUT, SLRT_CHx = 11		0.32		mJ

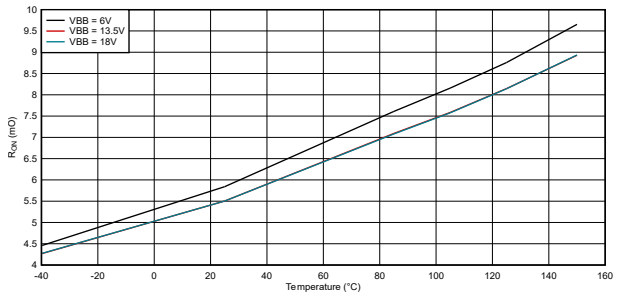
Copyright © 2026 Texas Instruments Incorporated

6.8 Typical Characteristics



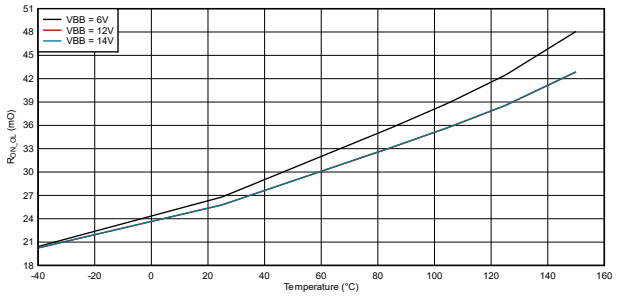
JEDEC 2s2p PCB
Board dimensions (W x L x H):
76.2mm x 114.3mm x 1.6mm

Figure 6-1. Transient Thermal Impedance



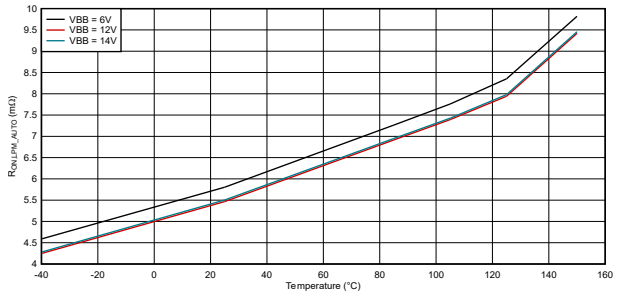
I_{OUT} = 500mA Active state
OL_ON_EN_CHx = 0

Figure 6-2. On Resistance (R_{ON}) vs Temperature



I_{OUT} = 500mA Active state
OL_ON_EN_CHx = 1

Figure 6-3. On Resistance, OL_ON Mode (R_{ON_OL}) vs Temperature



I_{OUT} = 500mA AUTO_LPM state

Figure 6-4. On Resistance in AUTO_LPM (R_{ON,LPM_AUTO}) vs Temperature

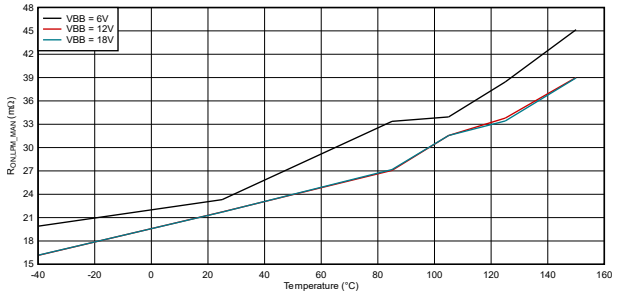
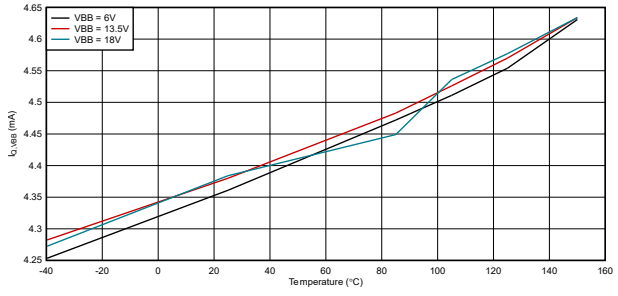


Figure 6-5. On Resistance in MANUAL_LPM (R_{ON,LPM_MAN}) vs Temperature

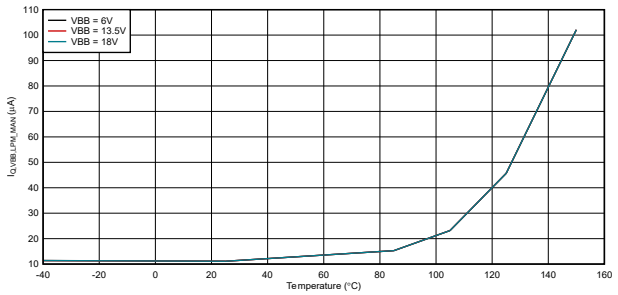


ACTIVE state Diagnostics enabled (ISNS, ADC)
IOUT = 0A SCLK off

Figure 6-6. VBB IQ Current ($I_{Q,VBB}$) vs Temperature

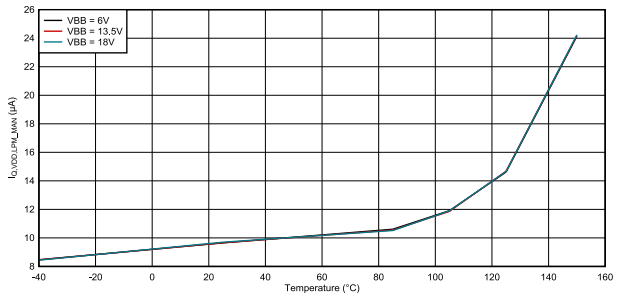
Copyright © 2026 Texas Instruments Incorporated

6.8 Typical Characteristics (continued)



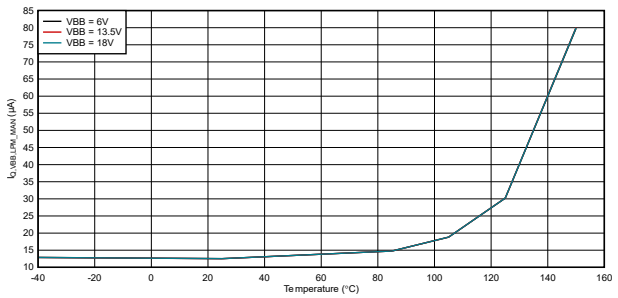
MANUAL_LPM state VDD = 5V
Channels off

Figure 6-7. VBB IQ Current in MANUAL_LPM (I_{Q,VBB,LPM_MAN}) - Channels Off vs Temperature



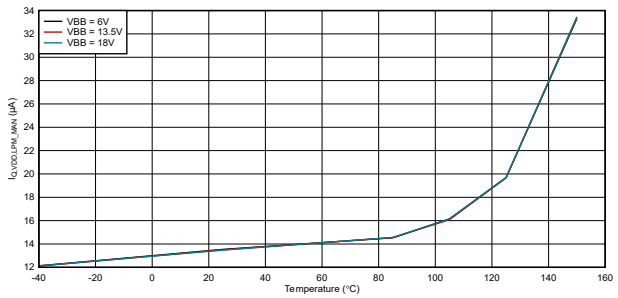
MANUAL_LPM state VDD = 5V
Channels off IOUT = 0A

Figure 6-8. VDD IQ Current in MANUAL_LPM (I_{Q,VDD,LPM_MAN}) - Channels Off vs Temperature



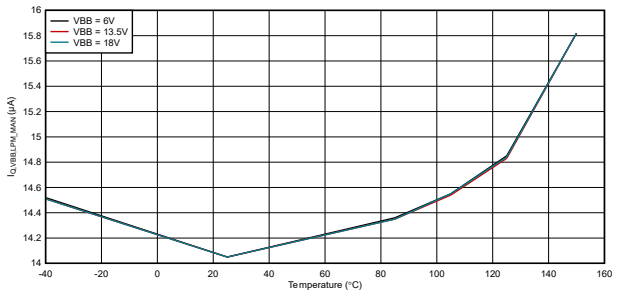
MANUAL_LPM state VDD = 5V
One channel enabled IOUT = 0A

Figure 6-9. VBB IQ Current in MANUAL_LPM (I_{Q,VBB,LPM_MAN}) - One Channel Enabled vs Temperature



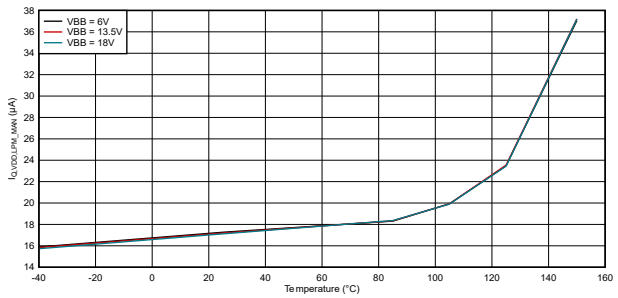
MANUAL_LPM state VDD = 5V
One channel enabled IOUT = 0A

Figure 6-10. VDD IQ Current in MANUAL_LPM (I_{Q,VDD,LPM_MAN}) - One Channel Enabled vs Temperature



MANUAL_LPM state VDD = 5V
Both channels enabled IOUT = 0A

Figure 6-11. VBB IQ Current in MANUAL_LPM (I_{Q,VBB,LPM_MAN}) - Both Channels Enabled vs Temperature

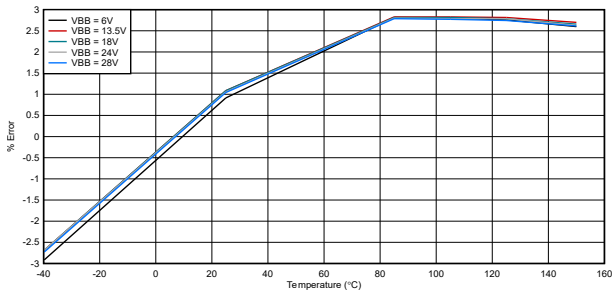


MANUAL_LPM state VDD = 5V
Both channels enabled IOUT = 0A

Figure 6-12. VDD IQ Current in MANUAL_LPM (I_{Q,VDD,LPM_MAN}) - Both Channels Enabled vs Temperature

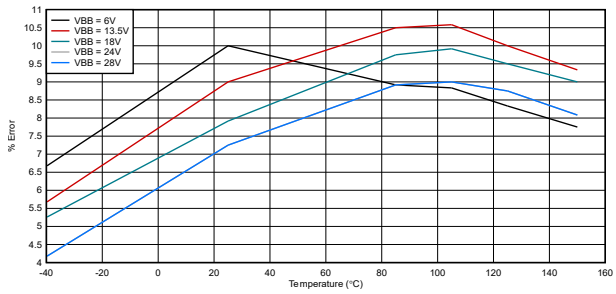
Copyright © 2026 Texas Instruments Incorporated

6.8 Typical Characteristics (continued)



K_{SNS1} reference = 6500
OL_ON_EN_CHx = 0 IOUT = 2A

Figure 6-13. K_{SNS1} % Error vs Temperature

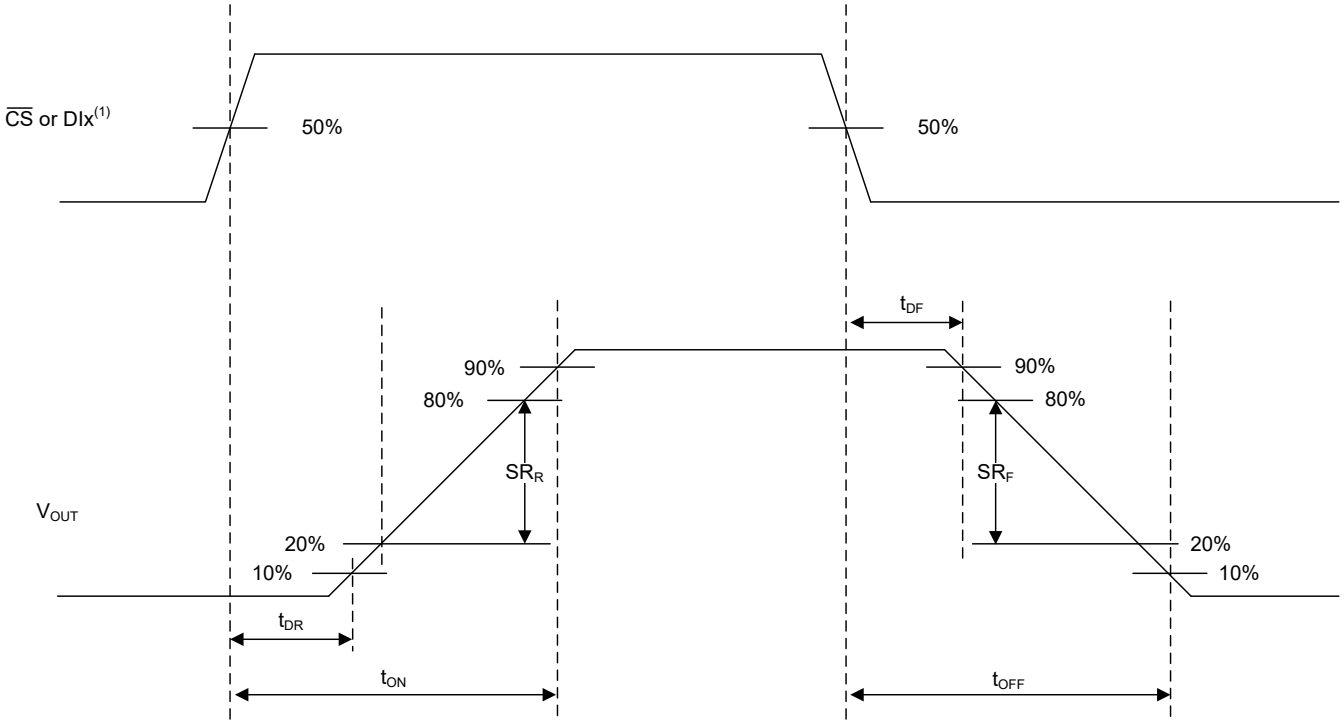


K_{SNS2} reference
= 1150
OL_ON_EN_C IOUT = 20mA
Hx = 1

Figure 6-14. K_{SNS2} % Error vs Temperature

Copyright © 2026 Texas Instruments Incorporated

7 Parameter Measurement Information



(1) Rise and fall time of $\overline{CS}$ or DIx is 100 ns.

Figure 7-1. Switching Characteristics Definitions

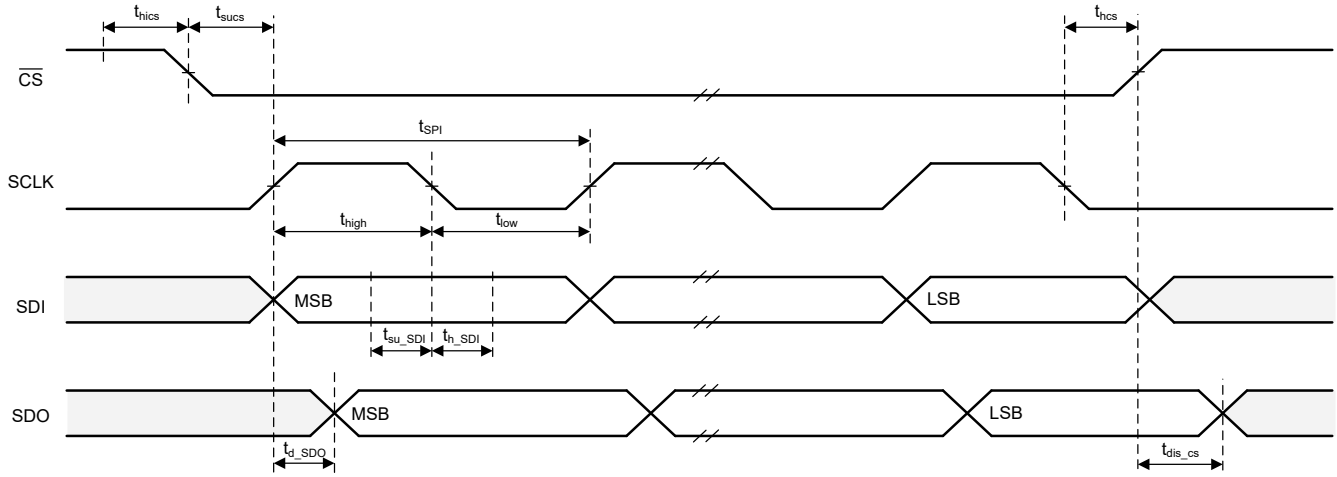


Figure 7-2. SPI Timing Characteristics Definitions

8 Detailed Description

8.1 Overview

The TPS2HCS05-Q1 device is a dual-channel smart high-side switch intended for use with 12V automotive batteries. The TPS2HCS05-Q1 device integrates SPI control and configuration as well digital readout with an ADC of key device and load diagnostics. The device incorporates all of the specific features needed for a power distribution switch as well as the traditional protective and diagnostic functions seen in high side switches for actuator drive applications.

Diagnostics features include a digital current, output voltage and FET temperature sense output that can be read over the SPI. The high-accuracy load current sense allows for diagnostics of complex loads. The output voltage sense and FET temperature sense features in the device enables diagnosis of the switch and load failures.

This device includes protection through thermal shutdown, overcurrent protection, transient withstand, and reverse battery operation. In addition, the device also includes an SPI-configurable wire-harness protection function through a defined fuse or time-current curve. The protection works in conjunction with an immediate switch-off overcurrent protection with an SPI-configurable threshold to fully protect against overload and short-circuit faults.

The TPS2HCS05-Q1 device also integrates a low quiescent current mode where the device can provide currents in the 100s of mA range while consuming only micro-amps of current. The device automatically switches to the high-current mode on an increase in load current and provide a wake signal to the MCU. Further, the device includes a capacitive charging mode that reduces the peak current load on the supply. Together, the two features support power distribution switch to off-board ECU applications.

For more details on the diagnosis, power distribution and protection features, refer to Section 8.4 and Section 10.1.

The TPS2HCS05-Q1 is one device in a family of TI high side switches. For each device, the part number indicates elements of the device behavior. The figure below gives an example of the device nomenclature.

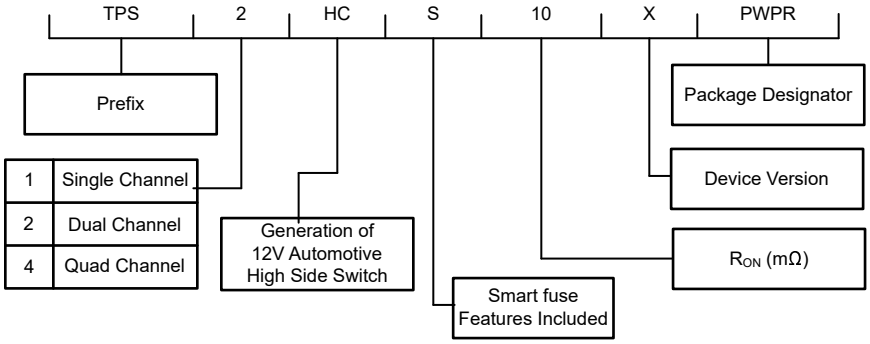


Figure 8-1. Naming Convention

Copyright © 2026 Texas Instruments Incorporated

8.2 Functional Block Diagram

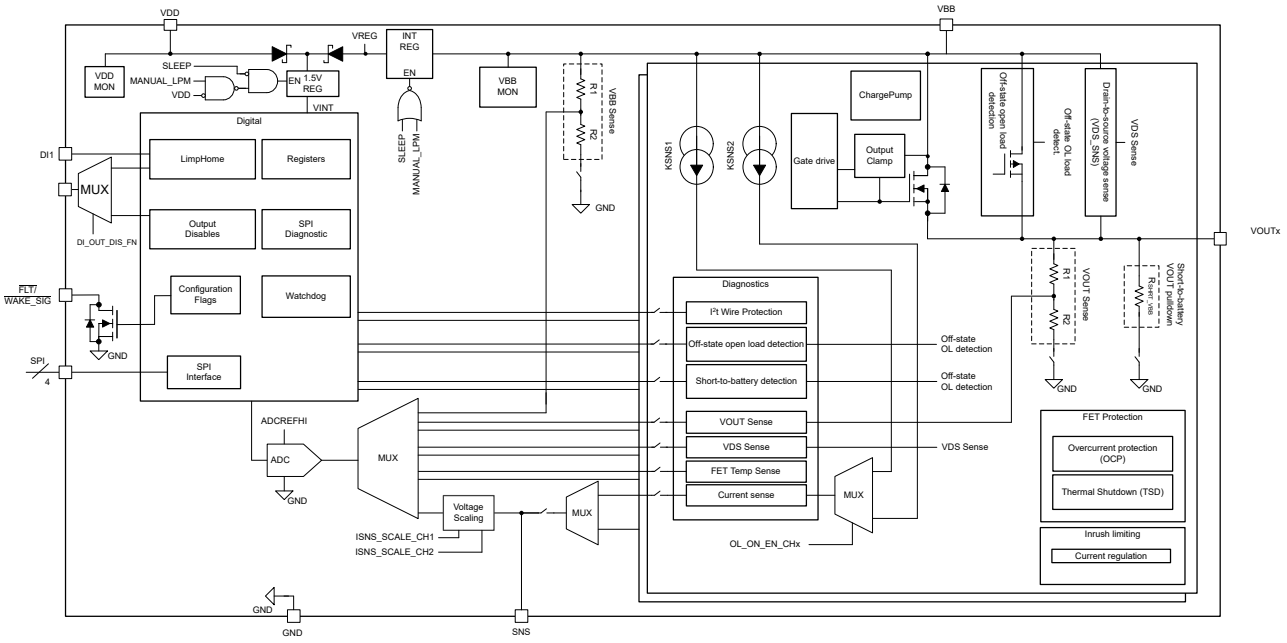


Figure 8-2. TPS2HCS05A-Q1 functional block diagram

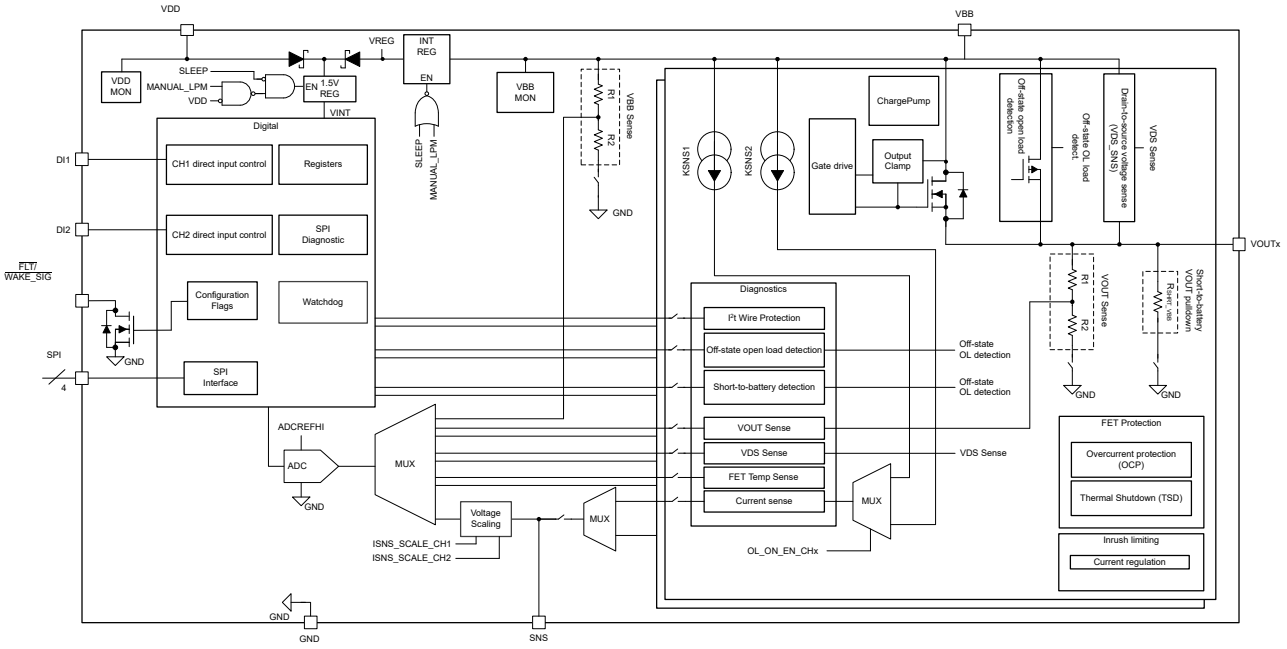


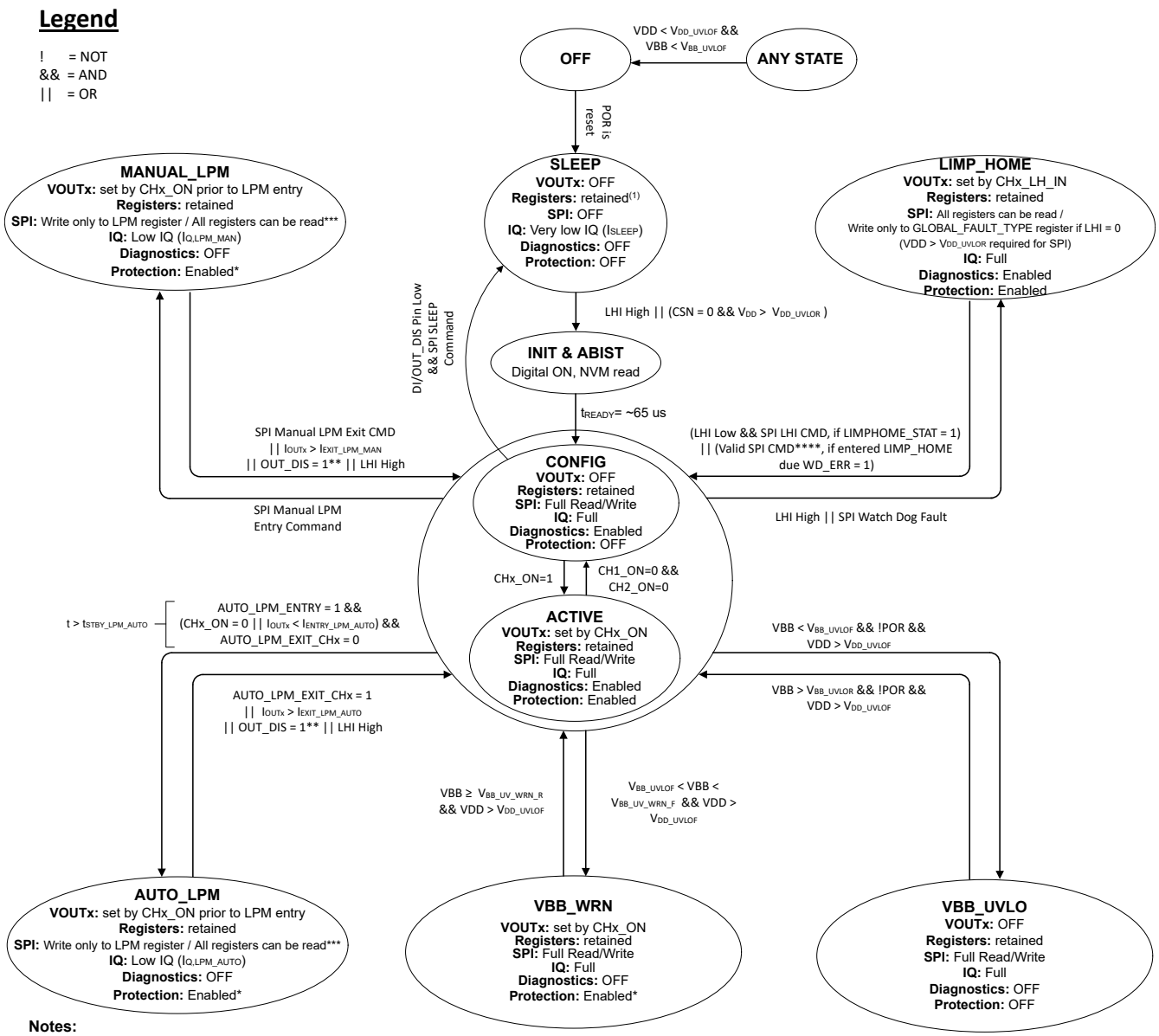
Figure 8-3. TPS2HCS05B-Q1 functional block diagram

8.3 Device Functional Modes

8.3.1 State Diagram

The device has three main categories of states it can transition into and out of low quiescent current, normal operation, and limp home. Inside of each of the categories are several states the device can be in. The state diagram for the TPS2HCS05A-Q1 device is shown in Figure 8-4 and the state diagram for the TPS2HCS05B-Q1 device is shown in Figure 8-5.

Copyright © 2026 Texas Instruments Incorporated



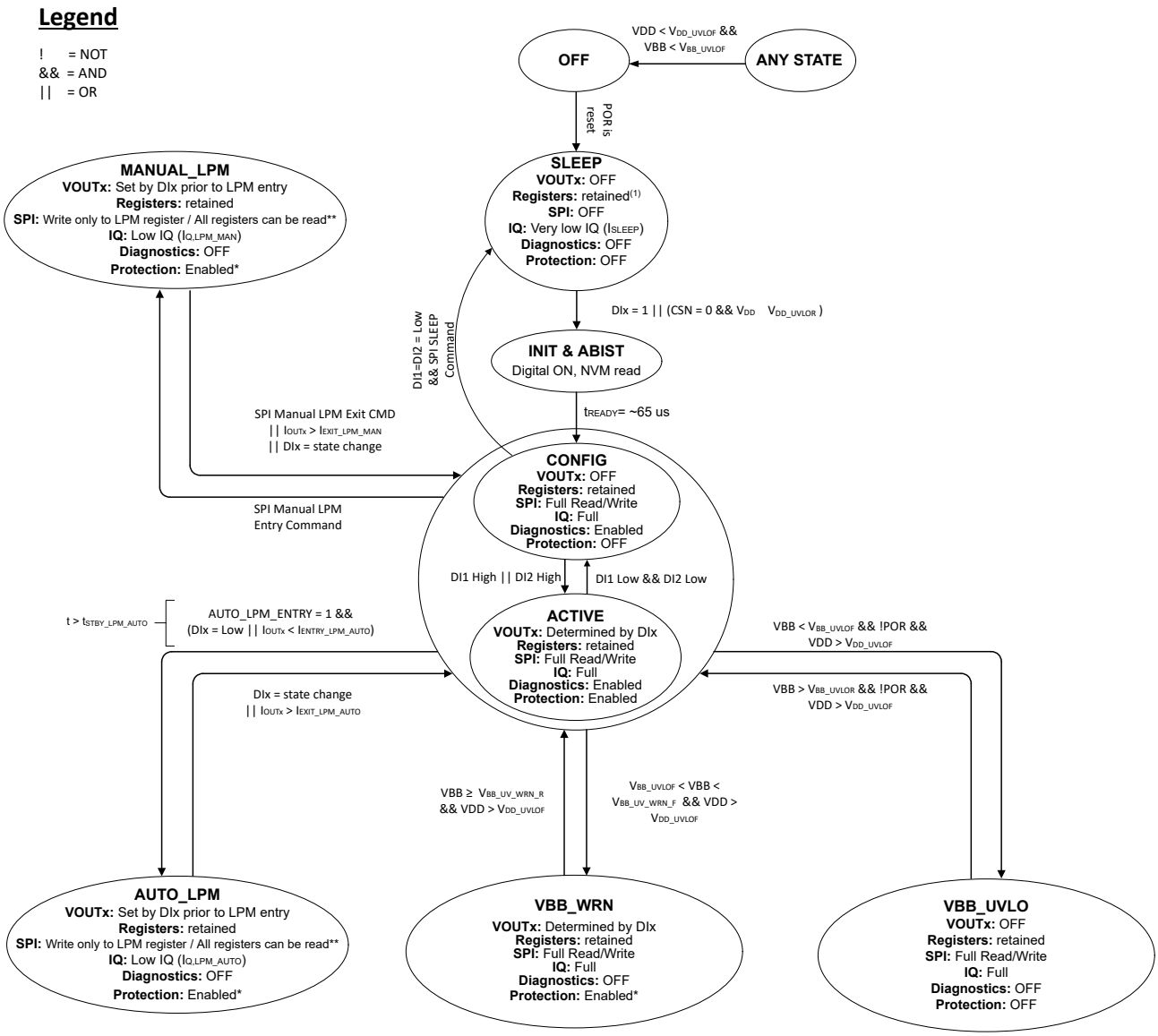
Notes:

- **Diagnostics =** Any ADC sensing, off-state open load detection, or VBB short-to-supply
- **Protection =** Overcurrent protection (I_{OCP}), Thermal shutdown (T_{REL} or T_{ABS}), and I2T protection (if enabled) **or** LPM short-circuit ($I_{SCP,LPM}$) in LPM states

* = I2T disabled
** = Only valid if DI_OUT_DIS_FN = 1 && OUT_DIS_MASK_CHx = 0
*** = Registers can be read in both LPM modes but the registers values will not be updated
**** = See “SPI watchdog function” section for more details
(1) = Registers can not be accessed but registers which are backed by EEPROM will retain their programmed values on next power up from sleep or OFF state

Figure 8-4. State Diagram - Version A

Copyright © 2026 Texas Instruments Incorporated



Notes:

- **Diagnostics =** Any ADC sensing, off-state open load detection, or VBB short-to-supply
- **Protection =** Overcurrent protection (I_{OCP}), Thermal shutdown (T_{REL} or T_{ABS}), and I2T protection (if enabled) **or** LPM short-circuit ($I_{SCP,LPM}$) in LPM states

* = I2T disabled
** = Registers can be read in both LPM modes but the registers values will not be updated
(1) = Registers can not be accessed but registers which are backed by EEPROM will retain their programmed values on next power up from sleep or OFF state

Figure 8-5. State Diagram - Version B

8.3.2 Output Control

Control of the eFuse channels varies depending on the device version. See the below sections for more details on the output control method for each of the device versions.

8.3.2.1 Output Control - Version A

The state of the eFuse outputs for ACTIVE state for TPS2HCS05A-Q1 is controlled by the CHx_ON bits in the SW_STATE register. The table below showcases the output control method in each state for the TPS2HCS05A-Q1 device.

Table 8-1. Output Control by State - TPS2HCS05A-Q1

State	Control Type	Output Control Description
SLEEP	N/A	Output OFF
CONFIG	SPI	Output OFF
ACTIVE	SPI	Set by CHx_ON
LIMP_HOME	SPI or DI pin (If DI_OUT_DIS_FN = 0)	Set by SPI through CHx_LH_IN bit See Section 8.3.8 for more details on output control settings
AUTO_LPM	SPI	Set by CHx_ON before AUTO_LPM entry
MANUAL_LPM	SPI	Set by CHx_ON before MANUAL_LPM entry
VBB_WRN	SPI	Set by CHx_ON
VBB_UVLO	N/A	Output OFF

8.3.2.2 Pin 5 Functions (DI or OUT_DIS) - Version A

Depending on the DI_OUT_DIS_FN bit in the DEV_CONFIG register, pin 5 for the device can either be a direct input (DI) pin to control the output state of the channel in LIMP_HOME state if configured to do so in the CHx_LH_IN bits or it can be an output disable function (OUT_DIS) to quickly disable the channel. For more details on the OUT_DIS function see Section 8.3.3. The table below shows the configuration settings for pin 5 based on the DI_OUT_DIS_FN bit in the DEV_CONFIG register.

Table 8-2. Pin 5 Function based on DI_OUT_DIS_FN

DI_OUT_DIS_FN	Function
0	**Direct input (DI) function -** control output state of channels in LIMP_HOME state if configured to do so in CHx_LH_IN bits
1	**Output disable (OUT_DIS) function -** Quickly disable the channels if configured through OUT_DIS_MASK_CHx bits

8.3.2.3 Output Control - Version B

The state of the eFuse outputs for ACTIVE state for TPS2HCS05B-Q1 is controlled exclusively by the DI1 for channel 1 and DI2 for channel 2. The CHx_ON bits in the SW_STATE register have no effect on the output state of the TPS2HCS05B-Q1. The table below showcases the output control method in each state for the TPS2HCS05B-Q1 device.

Table 8-3. Output Control by State - TPS2HCS05B-Q1

State	Control Type	Output Control Description
SLEEP	N/A	Output OFF
CONFIG	DIx	Output OFF
ACTIVE	DIx	Set by DIx pins
AUTO_LPM	DIx	Set by DIx pins before AUTO_LPM entry
MANUAL_LPM	DIx	Set by DIx pins before MANUAL_LPM entry
VBB_WRN	DIx	Set by DIx pins
VBB_UVLO	N/A	Output OFF

8.3.3 Output Disable Function (OUT_DIS)

TPS2HCS05A-Q1 provides a function to quickly disable one or both of the output channels in any state. If DI_OUT_DIS_FN = 1 in register DEV_CONFIG, pin 5 of the device becomes an active high, fast disable signal (OUT_DIS) which can turn off the outputs in $t_{OFF_OUT_DIS}$.

The TPS2HCS05A-Q1 device also offers the flexibility to determine if an output channel must be turned off when the OUT_DIS signal is asserted high. This can be programmed on a per channel basis in the CONFIG_CHx register with the OUT_DIS_MASK_CHx bit. If OUT_DIS_MASK_CHx = 0 then the device turns

Copyright © 2026 Texas Instruments Incorporated

off that respective channel if the OUT_DIS function goes high. If OUT_DIS_MASK_CHx = 1 then the respective channel does not turn off if OUT_DIS is asserted high and the respective channels output state instead follows either the LH_CH_IN or the CHx_ON bit depending on the device state.

The DI_OUT_DIS_FN and OUT_DIS_MASK_CHx bits are backed by EEPROM and can be re-programmed through the user EEPROM procedure.

Table 8-4 below shows the VOUT state based on the different pin and register configurations for TPS2HCS05A-Q1 for the OUT_DIS function. Figure 8-6 and Figure 8-7 shows the timing diagram of the OUT_DIS function with OUT_DIS_MASK_CHx = 0 and OUT_DIS_MASK_CHx = 1, respectively.

Table 8-4. TPS2HCS05A-Q1 - OUT_DIS Logic Table

OUT_DIS	LHI	OUT_DIS_MASK_CHx	VOUTx state
L	L	X	Follow CHx_ON
L	H	X	Follow CHx_LH_IN
H	L	0	OFF
H	L	1	Follow CHx_ON
H	H	0	OFF
H	H	1	Follow CHx_LH_IN

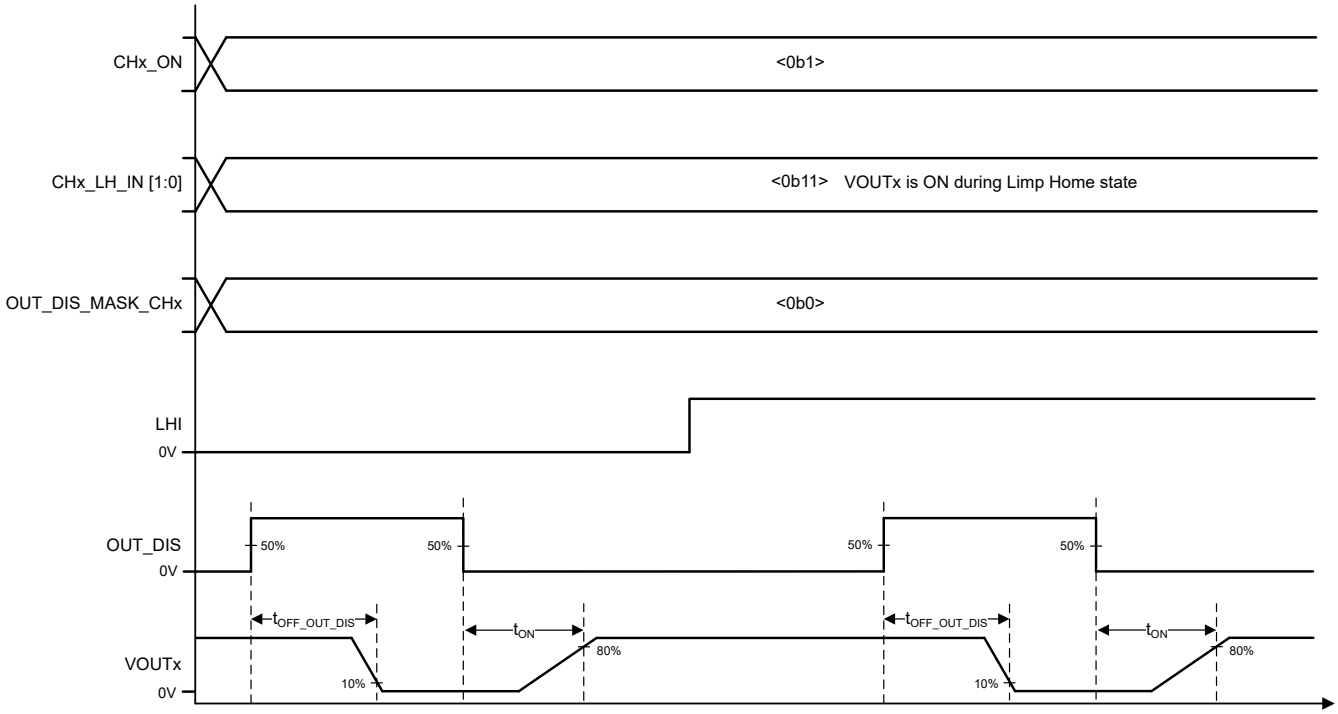


Figure 8-6. OUT_DIS timing diagram with OUT_DIS_MASK_CHx = 0

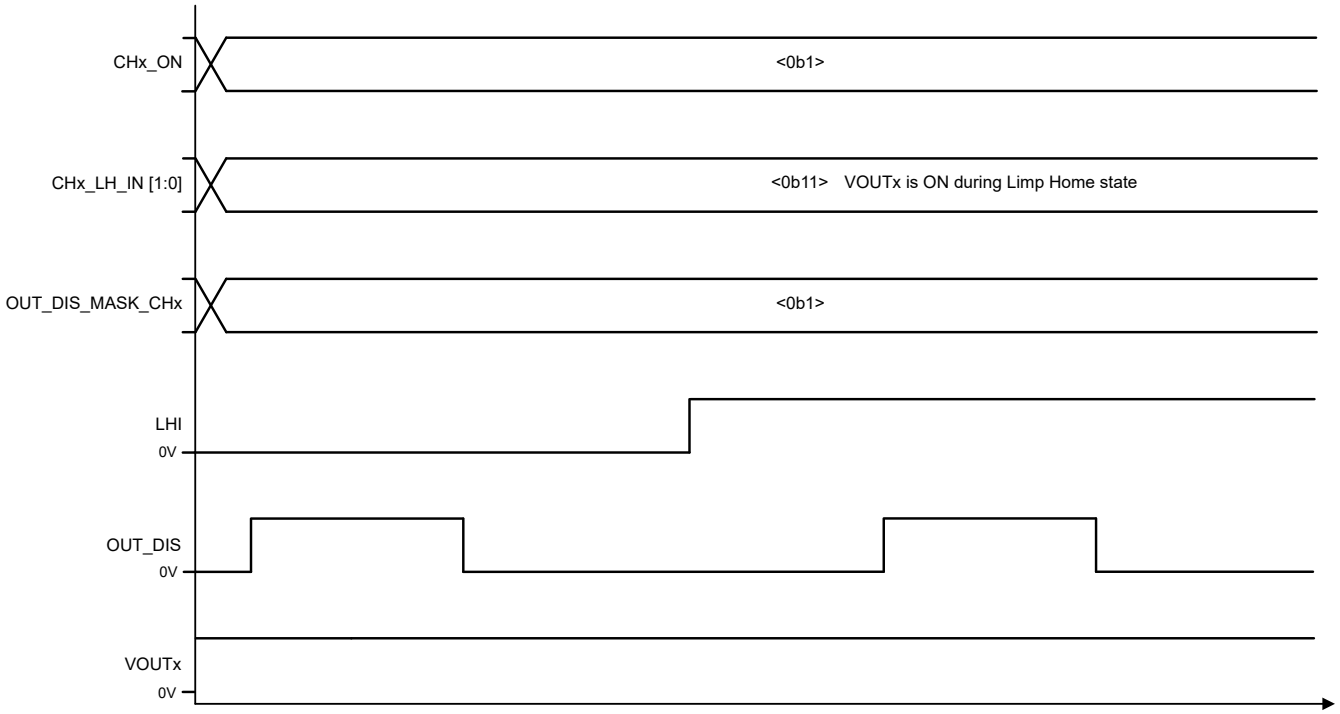


Figure 8-7. OUT_DIS timing diagram with OUT_DIS_MASK_CHx = 1

8.3.4 SPI Mode Operation

The TPS2HCS05-Q1 communicates with the host controller through a high-speed SPI. The interface has three logic inputs: clock (CLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is tri-stated when the $\overline{CS}$ pin is high. The maximum SPI clock rate is 8MHz, but is limited in practice by the series protection resistor.

The device supports simple daisy-chain SPI. This mode can be used with or without CRC.

The communication between the TPS2HCS05-Q1 IC and the controller or MCU is through a SPI bus in a primary-secondary configuration. The external MCU is always an SPI primary device that sends command requests on the SDI pin of the TPS2HCS05-Q1 IC and receives device responses on the SDO pin of the IC. The TPS2HCS05-Q1 device is always an SPI secondary device that receives command requests over the SDI line and sends responses (such as status and measured values) to the external MCU over the SDO line.

The TPS2HCS05-Q1 device can connect to the primary MCU in the following formats:

Copyright © 2026 Texas Instruments Incorporated

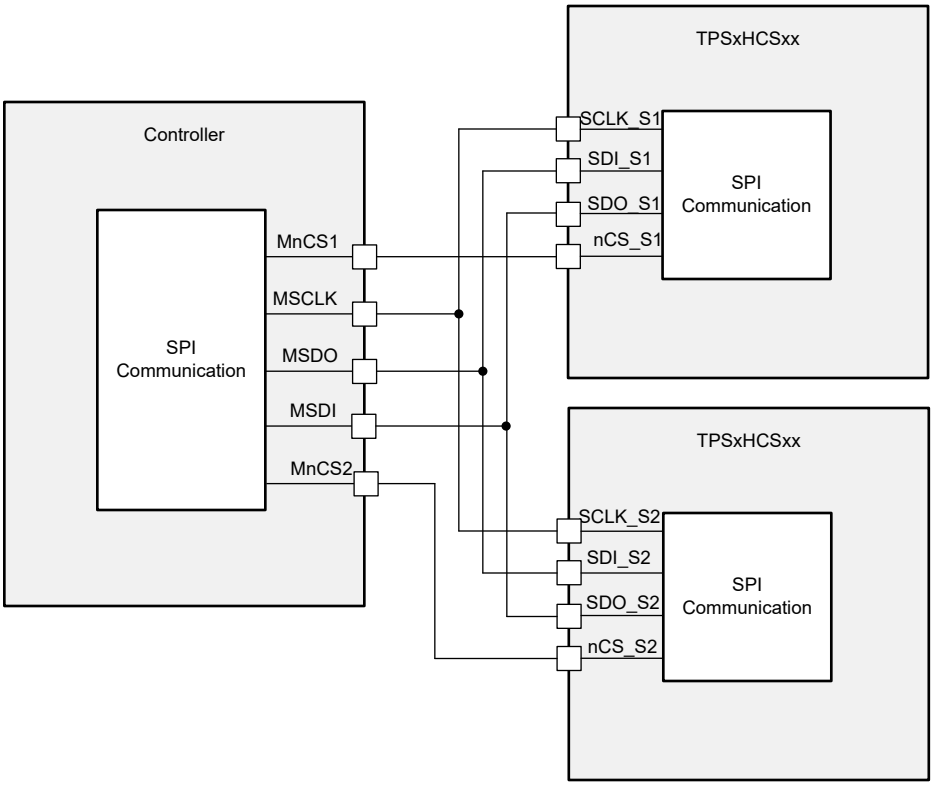


Figure 8-8. Independent Secondary Configuration (Separate nCS Signal)

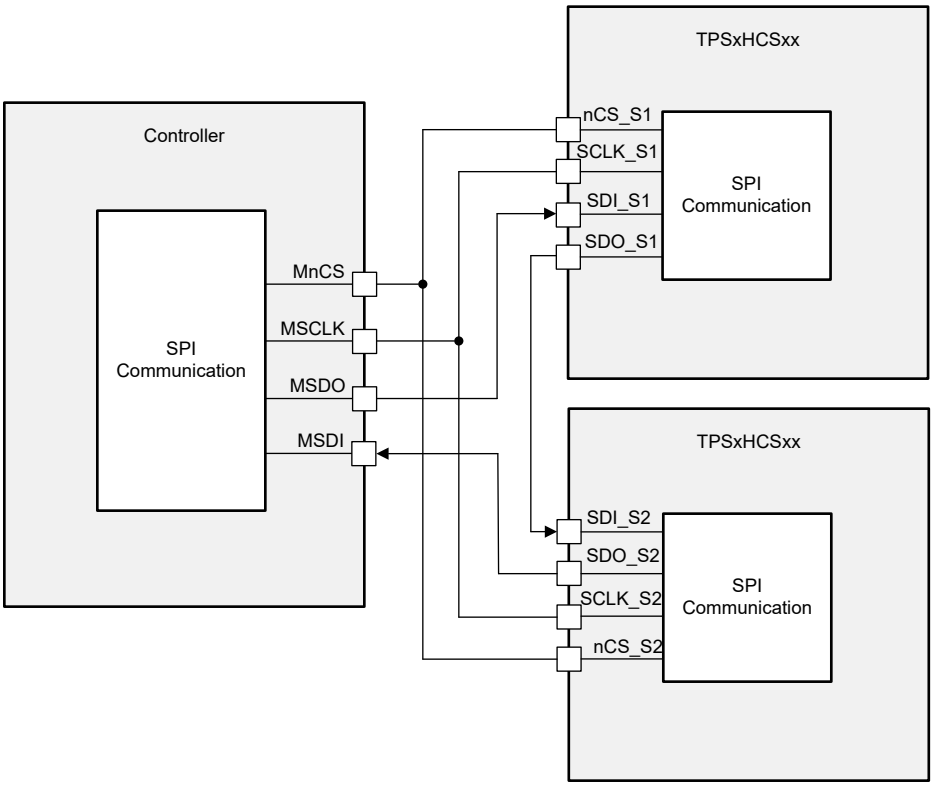


Figure 8-9. Daisy Chain Configuration

Copyright © 2026 Texas Instruments Incorporated

8.3.4.1 SPI

The SPI pin behavior is described in the following section.

8.3.4.2 Chip Select ($\overline{CS}$ or nCS)

The system microcontroller selects the TPS2HCS05-Q1 to receive communication using the $\overline{CS}$ pin. With the $\overline{CS}$ pin in a logic LOW state, command/configuration words can be sent to the TPS2HCS05-Q1 through the serial input (SDI) pin, and the device information can be retrieved by the microcontroller through the serial output (SDO) pin. The falling edge of the $\overline{CS}$ enables the SDO output and latches the content of the GLOBAL_FAULT_TYPE register that is sending out on SDO. The microcontroller can issue a READ command to retrieve information stored in the registers. The rising edge on the $\overline{CS}$ pin initiates the following actions:

1. Addressed registers are updated if there is no SPI communication error and if it is an SPI write command.
2. Read clear register is cleared if a READ command to this register is issued during $\overline{CS}$ = LOW.

To avoid any corrupted data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. A clean $\overline{CS}$ signal is needed to confirm no incomplete SPI words are sent to the device. This pin is internally pulled up to the VDD rail.

8.3.4.3 System Clock

The system clock (SCLK) pin clocks the internal shift register of the TPS2HCS05-Q1. The SDI data is latched into the input shift register on the falling edge of the SCLK signal. The SDO pin shifts the device stored information out on the rising edge of SCLK. The SDO data is available for the microcontroller to read on the falling edge of SCLK.

False clocking of the shift register must be avoided to confirm validity of data and it is essential the SCLK pin be in a logic LOW state whenever $\overline{CS}$ pin makes any transition. Therefore, it is recommended that the SCLK pin gets pulled to a logic LOW state as long as the device is not accessed and the $\overline{CS}$ pin is at a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SDI pins are ignored and the SDO pin remains as a high-impedance output.

8.3.4.4 Serial Data In (SDI) and Serial Data Out (SDO)

The SDI pin is used for serial instruction data input. SDI information is latched into the input shift register on the falling edge of the SCLK when $\overline{CS}$ is low.

The SDO pin is the output from the internal shift register. This pin is internally pulled up to the VDD rail. SDO pin is high impedance when the $\overline{CS}$ pin is high. Each successive **rising** SCLK edge makes the next data bit available for the microcontroller to read on the **falling** edge of SCLK. SDO goes back to high-impedance when $\overline{CS}$ is high.

8.3.4.5 CRC Error Detection and Checking of Clocks

Setting the CRC_EN bit high enables CRC error detection. A CRC-4-ITU-Normal Check Sequence (FCS) is then sent along with each serial transaction. The 4-bit CRC is based on the normal generator polynomial $X^4 + X + 1$ with CRC starting value = 1111. When CRC is enabled, the TPS2HCS05-Q1 expects a check byte appended to the SDI program/configure data that it receives.

To program a complete word, exact bits of information (shown in following table) must be entered into the device. When CRC is disabled, the IC enables register write only if exact number of bits have been clocked in. When CRC is enabled, the IC enables register write only if exact number of bits have been clocked in with no CRC errors. In case the word length exceeds or does not meet the required length or there is CRC errors, the SPI_ERR bit in the GLOBAL_FAULT_TYPE register is asserted to logic “1”, and the data received is considered invalid. Note the SPI_ERR bit is not flagged if SCLK is not present. The SPI_ERR is sent back to SPI Main device on SDO during next chip access. **Note that clear on read applies only when there is no SPI error when the register is read.**

Copyright © 2026 Texas Instruments Incorporated

8.3.4.6 SPI Frame Format

The device uses a 24-bit frame width (when CRC is not used) with the format as shown in Figure 8-10. Please note that the 16-bit wide "Data Out" in the SDO output is always for the previous SPI command frame (Read or Write).

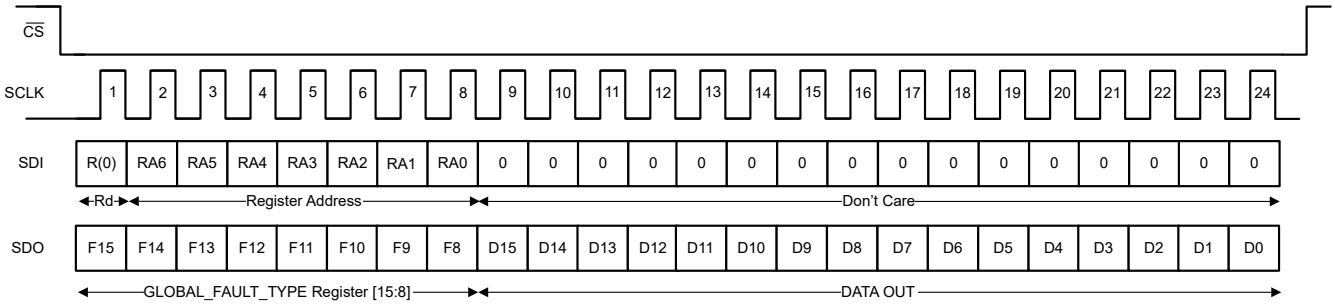


Figure 8-10. 24-Bit Read, No CRC (CRC_EN=0)

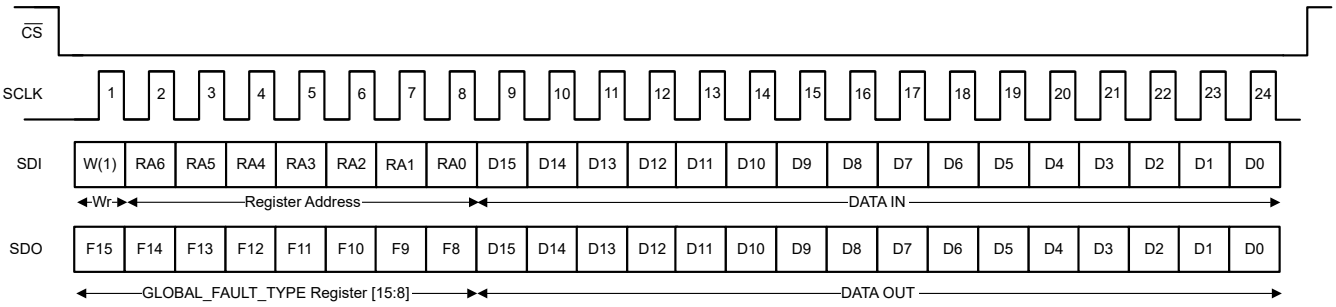


Figure 8-11. 24-Bit Write, No CRC (CRC_EN=0)

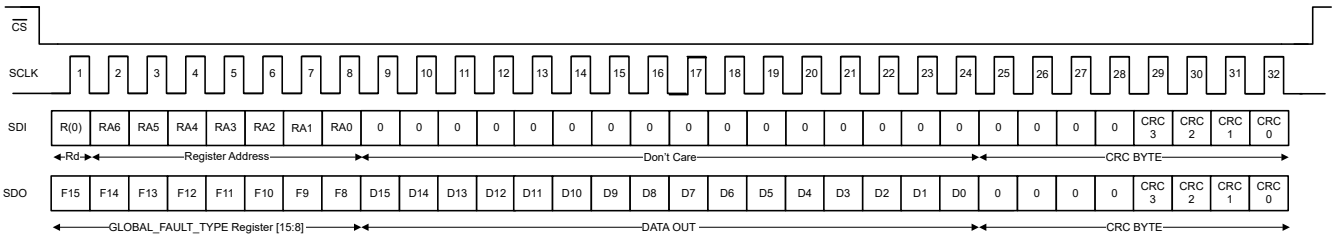


Figure 8-12. 32-Bit Read, CRC Enabled (CRC_EN=1)

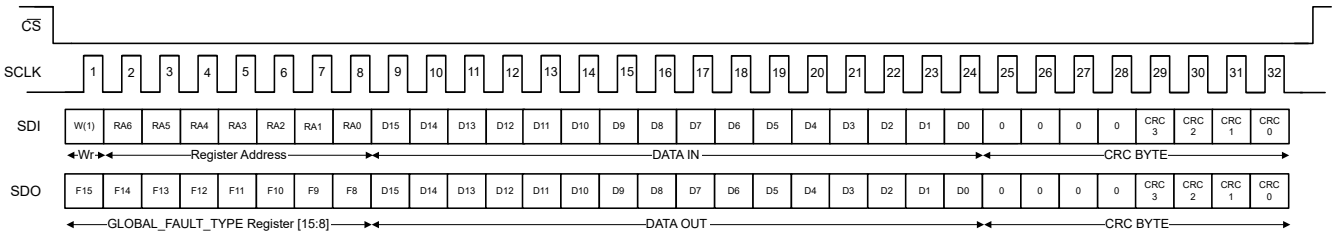


Figure 8-13. 32-Bit Write, CRC Enabled (CRC_EN=1)

8.3.4.7 GLOBAL_FAULT_TYPE [15:8] Bits

The TPS2HCS05-Q1 device, outputs the GLOBAL_FAULT_TYPE [15:8] bits on the SDO header so these status bits can be continuously read the during each SPI transaction. The GLOBAL_FAULT_TYPE [15:8] bits can configure as read clear or real time status bits based on the FLT_LTCH_DIS bit setting in the DEV_CONFIG register. The FLT_LTCH_DIS bit however does not apply to the LPM_STATUS bit.

Copyright © 2026 Texas Instruments Incorporated

If FLT_LTCH_DIS = 0, then the fault bits are latched and are cleared only when the associated register in the bit description is read and the fault no longer exists. The table below highlights which registers need to be read to clear each of the different fault bits if the fault no longer exists. This is also detailed in each of the bit descriptions in the register map.

Table 8-5. GLOBAL_FAULT_TYPE [15:8] Bits Behavior When FLT_LTCH_DIS = 0

BIT NO.	BIT NAME	REGISTER WHICH NEEDS TO BE READ TO CLEAR THE FAULT BIT IF THE FAULT NO LONGER EXISTS
15	Reserved	N/A
14	Reserved	N/A
13	CH2_FLT	FLT_STAT_CH2
12	CH1_FLT	FLT_STAT_CH1
10	CHAN_OCP_I2T_TSD	FLT_STAT_CHx
9	OL_SHRT_VBB_OFF_FLT	FLT_STAT_CHx
8	GLOBAL_ERR_WRN	GLOBAL_FAULT_TYPE

If FLT_LTCH_DIS = 1, then the fault bits are not latched and clears when the fault no longer exists.

The figure below highlights the FLT_LTCH_DIS function of the device in regard to the GLOBAL_FAULT_TYPE [15:8] bits.

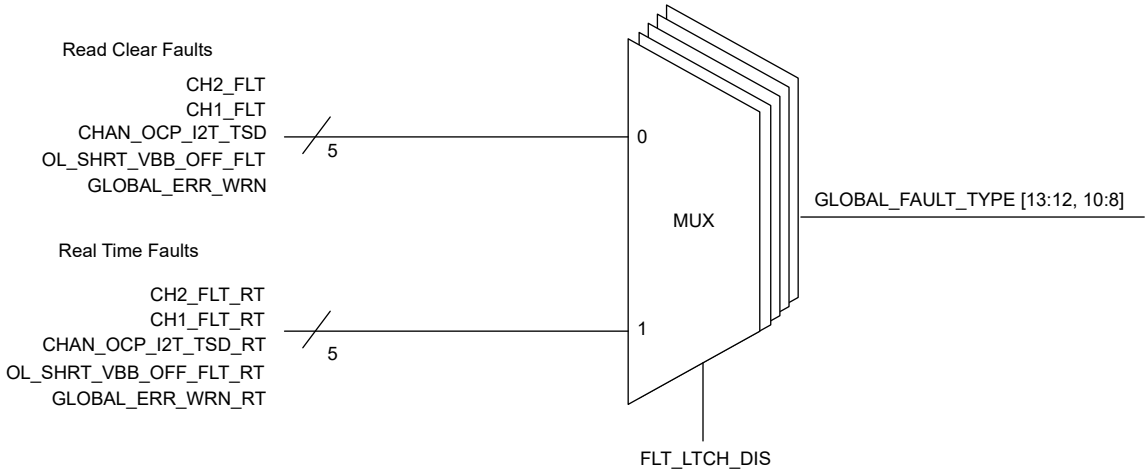


Figure 8-14. FLT_LTCH_DIS Implementation

8.3.4.8 SPI Watchdog Function

The TPS2HCS05-Q1 device offers an optional SPI watchdog function to monitor for valid SPI transactions from the host controller and loss of the VDD supply. If a valid SPI transaction does not occur in the configurable timeout period, WD_TO, then the FLT pin goes low and the WD_ERR bit in the GLOBAL_FAULT_TYPE register is set to 1. A valid SPI transaction consists of a SPI transaction with no SPI errors or CRC errors (if enabled). If the VDD supply to the device drops below the VDD_UVLO threshold then SPI on the device is not operational. If the VDD supply remains below the VDD_UVLO for longer than the watchdog time period, then the device issues a watchdog error where the WD_ERR bit is set to 1 and the FLT pin goes low.

The watchdog function is enabled through WD_EN bit in the DEV_CONFIG register. The table below showcases the t configurable watchdog timeout windows, WD_TO.

Table 8-6. Watchdog Timeout Settings

WD_TO Setting	Watchdog Timeout Period
00	400µs
01	400ms

Copyright © 2026 Texas Instruments Incorporated

Table 8-6. Watchdog Timeout Settings (continued)

WD_TO Setting	Watchdog Timeout Period
10	800ms
11	1200ms

8.3.4.9 SPI Watchdog Operation - TPS2HCS05A-Q1

If the watchdog function is enabled (WD_EN = 1) and a watchdog error occurs either due to no valid SPI transactions in the watchdog timeout window or due to a loss of VDD supply, WD_ERR = 1, FLT pin goes low, and the device transitions to the LIMP_HOME state where the output control of the channels are set by the CHx_LH_IN bits in the DEV_CONFIG register. Note, the LIMPHOME_STAT bit is not set to 1 as a result of watchdog error. Once a valid SPI transaction has been detected, the FLT pin goes high and the device automatically exits the LIMP_HOME state and will revert the output control of the channel back to the CHx_ON bit. The WD_ERR bit in the GLOBAL_FAULT_TYPE register is latched to 1 as a result of a SPI watchdog timeout error and is cleared only after read and the error no longer exists.

8.3.5 Fault Reporting

The device provides enhanced fault reporting through a $\overline{\text{FLT}}$ status pin and fault status bits through SPI.

The $\overline{\text{FLT}}$ status pin allows the device to interrupt the system when a fault has occurred on the device. The $\overline{\text{FLT}}$ status pin is an open-drain output that asserts low when a fault occurs on the device. For faults which are read clear, the $\overline{\text{FLT}}$ pin goes high if the fault no longer exists and the specific register to clear the fault is read. Indication on the $\overline{\text{FLT}}$ pin can be masked for some faults through FAULT_MASK register. See the FAULT_MASK register for more details.

The device also provides fault information through SPI through a global fault register (GLOBAL_FAULT_TYPE) and channel specific fault registers (FLT_STAT_CHx) to enable the system to quickly diagnose what caused the fault in the device. The device outputs the GLOBAL_FAULT_TYPE [15:8] bits on the SDO header so these status bits can be continuously read for each SPI transaction.

For more details on each of the individual fault status bits see the GLOBAL_FAULT_TYPE and FLT_STAT_CHx registers in the register map.

Table 8-7 highlights how the device signals different events through the $\overline{\text{FLT}}$ pin and the fault status bits.

When the device is in low-power mode no fault information is available through the $\overline{\text{FLT}}$ pin. If short circuit occurs in LPM, the device protects itself then transition to ACTIVE state and then signals fault on the $\overline{\text{FLT}}$ pin and in the fault status registers.

Table 8-7. Fault Reporting Table

EVENT / FAULT	DETECTION	PROTECTION	GLOBAL_FAULT_TYPE REPORTING	FLT_STAT_CHx REPORTING	$\overline{\text{FLT}}$ INDICATION
FET - Overtemperature Warning	Y	N	CHx_FLT(1)	THERMAL_WRN_CHx(1)	N
FET - Temperature shutdown (TSD)	Y	Y	CHx_FLT(1) and CHAN_OCP_I2T_TSD(1)	THERMAL_SD_CHx(1)	Y
I_{OCP} - Immediate shutdown	Y	Y	CHx_FLT(1) and CHAN_OCP_I2T_TSD(1)	ILIMIT_CHx(1)	Y
I_{CL_REG} - Current limit regulation	Y	Y	N/A	N/A	N
I_{CL_REG} - Current limit regulation - inrush period expiry	Y	Y	CHx_FLT(1) and CHAN_OCP_I2T_TSD(1)	ILIMIT_CHx(1)	Y
I_{CL_REG} - Current limit regulation - TSD	Y	Y	CHx_FLT(1) and CHAN_OCP_I2T_TSD(1)	ILIMIT_CHx(1) and THERMAL_SD_CHx(1)	Y
Channel in T_{RETRY} (LATCH_CHx = 0)	Y	N/A	N/A	FLT_CHx	Y
Channel is latched-off (LATCH_CHx = 1)	Y	N/A	N/A	LATCH_STAT_CHx and FLT_CHx	Y

Copyright © 2026 Texas Instruments Incorporated

Table 8-7. Fault Reporting Table (continued)

EVENT / FAULT		DETECTION	PROTECTION	GLOBAL_FAULT_TYPE REPORTING	FLT_STAT_CHx REPORTING	$\overline{\text{FLT}}$ INDICATION
Limp Home Entry (LHI = 1)		Y	N/A	GLOBAL_ERR_WRN(1) and LIMPHOME_STAT(2)	N/A	Y
Active I2T Accumulation or Decrement		Y	N/A	N/A	I2T_MOD_CHx	N
I2T Shutdown		Y	Y	CHx_FLT(1) and CHAN_OCP_I2T_TSD(1)	I2T_FLT_CHx(1) and FLT_CHx	Y
VOUTx error (V_{DS} > 2V)		Y	N	CHx_FLT(1)	VOUT_ERR_CHx(1)	N
VOUT shorted to VBB		Y	N	CHx_FLT(1) and OL_SHRT_VBB_OFF_FLT(1) (if OL_SVBB_EN_CHx = 01)	SHRT_VBB_CHx(1) (if OL_SVBB_EN_CHx = 01)	Y, unless masked
Open load	Off State	Y	N	CHx_FLT(1) and OL_SHRT_VBB_OFF_FLT(1) (if OL_SVBB_EN_CHx = 10)	OL_OFF_CHx(1) (if OL_SVBB_EN_CHx = 10)	Y, unless masked
	On State	Y	N	N/A	N/A	N
Reverse battery		Y	Y, with external components	N/A	N/A	N
VBB UV warning		Y	N	GLOBAL_ERR_WRN(1) and VBB_UV_WRN(1)	N/A	N
VBB_UVLO		Y	Y	GLOBAL_ERR_WRN(1) and VBB_UVLO(1)	N/A	Y
VDD_UVLO		Y	Y	GLOBAL_ERR_WRN(1) and VDD_UVLO(1)	N/A	Y*
Power on Reset (POR)		Y	Y	GLOBAL_ERR_WRN(1) and POR(1)	N/A	Y
SPI Watchdog Error		Y	N/A	GLOBAL_ERR_WRN(1) and WD_ERR(1) (if WD_EN = 1)	N/A	Y, unless masked
SPI Frame Error		Y	N/A	GLOBAL_ERR_WRN(1) and SPI_ERR(1)	N/A	Y, unless masked
SPI CRC Error		Y	N/A	GLOBAL_ERR_WRN(1)(1) and SPI_ERR(1) (if CRC_EN = 1)	N/A	Y, unless masked

(1) Read-clear (RC) fault bits
(2) Write 1 to clear (W1C) bits

Note

If VDD is not present, any reads from the SDO header returns all 0's.

8.3.6 SLEEP

The TPS2HCS05-Q1 device offers a SLEEP state where the device is placed into an ultra-low current consumption state. When the device is in SLEEP state, both channels are OFF, registers are cleared, and all digital circuits are powered off. The device transitions to this state if VBB < VBB_UVLO and VDD < VDD_UVLO. The device can manually be put into SLEEP state by pulling DI/OUT_DIS Low and writing a 1 to the SLEEP bit in the SLEEP register. After the device enters SLEEP mode, the DI/OUT_DIS pin can be released.

Copyright © 2026 Texas Instruments Incorporated

The device can be woken from the SLEEP state through the CSN pin going low. There are two methods to wake the device up from SLEEP through the CSN pin:

1. Pulse the CSN pin low for t < t_{READY}
2. Hold the CSN pin low for at least t_{READY} and continue to hold CSN pin low through the first SPI transaction

Both methods above result in the device waking up without a SPI_ERR fault. A psuedo-SPI transaction can be used to satisfy method number 1 if the psuedo-SPI transaction is completed in t < t_{READY}. Figure 8-15 below shows examples of the two proper wake-up scenarios which results in no SPI_ERR fault and one improper wake-up scenario which results in a SPI_ERR fault.

Upon wake-up from SLEEP state, the values in the registers are set to the reset values detailed in the register map below. Additionally, the FLT pin is asserted low and the POR, VDD_UVLO, and VBB_UVLO fault bits are asserted and are cleared when the GLOBAL_FAULT_TYPE register is read if none of these faults currently exist when read.

Copyright © 2026 Texas Instruments Incorporated

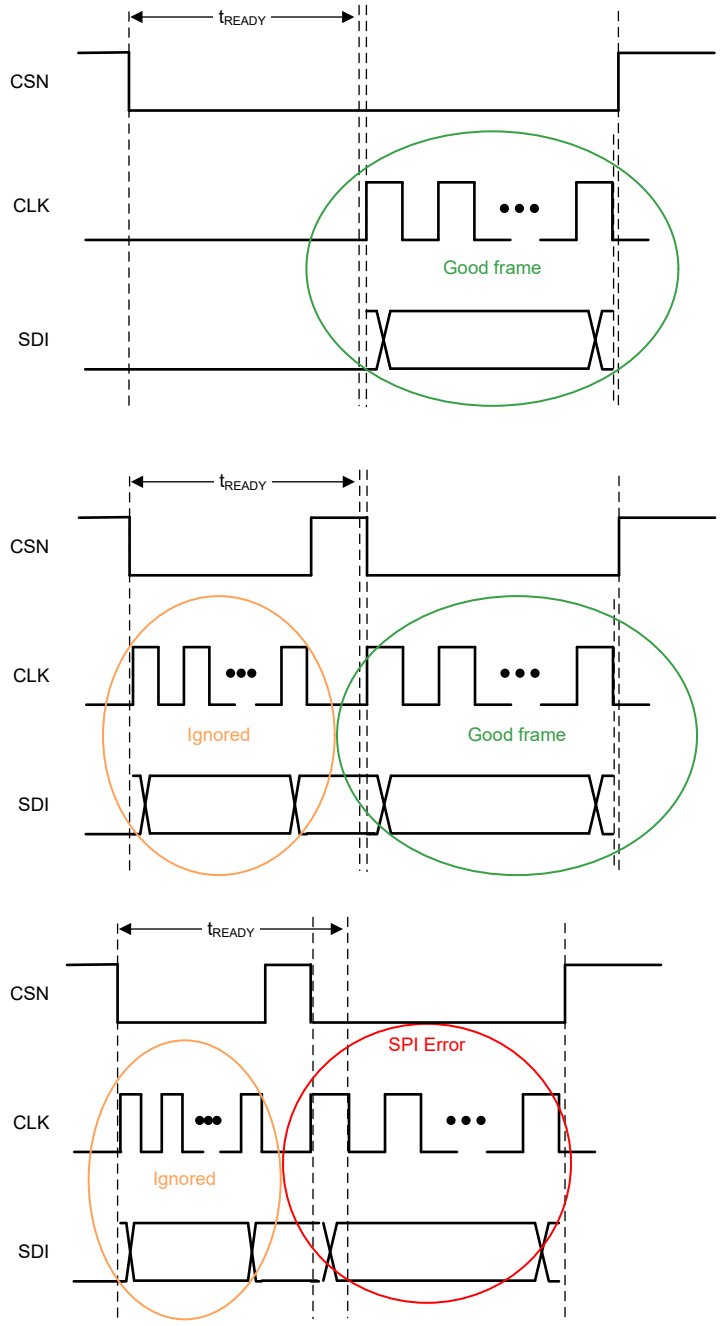


Figure 8-15. Startup Communication Timing

8.3.7 CONFIG/ACTIVE

The CONFIG/ACTIVE state is where the device stays during normal operation when the outputs are OFF (CONFIG) or ON (ACTIVE). The difference between the two is that in the CONFIG state (with the outputs OFF) all of the registers can be configured. The configuration registers (especially ones needed to successfully enable the channel) are expected to be written to before the outputs can be turned ON, when transitioning from the SLEEP state (and all the registers are lost). However, the configuration registers are retained while in the LPM state and so the device does not need to be reconfigured while transitioning from the LPM state to the ACTIVE state. The quiescent current draw from VBB, ($I_{Q,VBB}$) and VDD, ($I_{Q,VDD}$) is higher than in the other states to support the load and device diagnostics. SPI communication and diagnostics checks are fully supported in this state.

Copyright © 2026 Texas Instruments Incorporated

The device can be transitioned into the CONFIG state from the SLEEP state by the CSN pin going low (a psuedo-SPI command serves this purpose). The device completes the transition through all initializations and safety checks. The device transitions to and from the LIMP HOME state depending on the internal SPI watchdog monitor and the status of the LHI input pin. The device can transition into and out of the LPM state by a write to the LPM register.

In the CONFIG state, the device uses a gate to source pulldown to achieve the configured slew rate when the channel is enabled and disabled. As a result, when the channel is off there is a 1µA bias path to VOUT which creates a 1µA leakage current to VOUT. If there is no load on the output this can cause the output to float up. To reduce the open load VOUT voltage, the R_{SHRT_VBB} pulldown resistor can be enabled to reduce the output voltage to low levels. The R_{SHRT_VBB} pulldown resistor can be enabled through the OL_SVBB_EN_CHx [1:0] bits in the CHx_CONFIG registers. In SLEEP and LPM states, to achieve the lowest IQ the device instead uses a gate to ground pulldown so the 1µA bias path does not exist in these states.

8.3.8 LIMP_HOME State (Version A Only)

The LIMP_HOME state is intended to place the outputs in the desired safe state when there is a failure of SPI communication (if WD_EN=1), loss of VDD supply (if WD_EN = 1), or another system-level fault which causes the LHI pin to go high. When the ECU detects a system-level fault, the system controller raises the LHI pin high to signal to the device to go to the LIMP_HOME state. If the device detects a SPI watchdog timeout error and thus a SPI communication error, the device goes to the LIMP HOME state. In both cases, the output state is as specified on a per channel basis through the CHx_LH_IN bits of the DEV_CONFIG register. The settings for the CHx_LH_IN bits are detailed in Table 8-8 and Table 8-9 for DI_OUT_DIS_FN = 0 and DI_OUT_DIS_FN = 1, respectively.

Table 8-8. CHx_LH_IN bit Settings With DI_OUT_DIS_FN = 0

Setting	Setting Description
00	Output state is set by the DI pin when in LIMP_HOME state • If DI = HI, then CHx = ON in LIMP_HOME state • If DI = LO, then CHx = OFF in LIMP_HOME state
01	Keeps the same output state from CHx_ON bit when entering LIMP_HOME state
10	Output is OFF in LIMP_HOME state
11	Output is ON in LIMP_HOME state

Table 8-9. CHx_LH_IN bit Settings With DI_OUT_DIS_FN = 1

Setting	Setting Description
00	Output is OFF in LIMP_HOME state
01	Keeps the same output state from CHx_ON bit when entering LIMP_HOME state
10	Output is OFF in LIMP_HOME state
11	Output is ON in LIMP_HOME state

The register values are retained in the LIMP HOME state, which means that the appropriate overcurrent protection threshold values, duration and retry behavior are all set with the outputs corresponding to the state based on the CHx_LH_IN bits. If the device entered into the LIMP_HOME state as a result of the LHI pin going high, the LIMPHOME_STAT bit in the GLOBAL_FAULT_TYPE register is set to 1 which lets the MCU or controller know that the device is in the LIMP HOME state. The MCU cannot write to any of the registers until the device is out of the LIMP HOME state.

If the device entered the LIMP_HOME state as a result of LHI going high, the device transitions out of the LIMP_HOME state when the LHI pin is brought low and a is written to the LIMPHOME_STAT bit in the GLOBAL_FAULT_TYPE register. The register settings are retained while in LIMP HOME state and the device transitions back into normal operation in the ACTIVE state.

Copyright © 2026 Texas Instruments Incorporated

If the device entered LIMP_HOME state as a result of a SPI watchdog timeout error, the outputs are set according to the CHx_LH_IN bits but the LIMPHOME_STAT bit is not set to 1. The device automatically exits the LIMP_HOME state if a valid SPI transaction is detected. The WD_ERR bit in the GLOBAL_FAULT_TYPE register is latched to 1 as a result of a SPI watchdog timeout error and can be cleared only after read and the error no longer exists.

If VDD < VDD_UVLO, the device can still transition to LIMP_HOME state through the LHI input if LHI = 1.

8.3.8.1 LIMP HOME State Exceptions

The device can receive an LHI signal during cap charging or inrush duration. If the desired state is ON, the device continues cap charging per programmed register values. If the desired state is OFF, then the channel is turned off.

In LIMP_HOME state, if a short circuit occurs that causes an overcurrent fault (ILIMIT_CHx) or a thermal shutdown fault (THERMAL_SD_CHx), the output channels continues to retry regardless of the LATCH_CHx bit setting if the channels are configured to be ON by the CHx_LH_IN bits. If LATCH_CHx = 1 and the output channels are latched off due to an overcurrent fault or thermal shutdown fault and the device enters LIMP_HOME state either through LHI = 1 or a watchdog fault (if WD_EN = 1), the channels are re-enabled and continue to retry if a persistent short exists regardless of the LATCH_CHx setting if the channels configure to be ON through the CHx_LH_IN bits.

In LIMP_HOME state, if an I2T fault (I2T_FLT_CHx) must occur on the channels and TCLDN_CHx = 00 (indefinite cooldown), the channels remains in indefinite cooldown and does not retry even if the channels are configured to be ON through the CHx_LH_IN bits. If an I2T fault occurs in active state and TCLDN_CHx = 00 (indefinite cooldown) and the device enters LIMP_HOME state either through LHI = 1 or a watchdog fault (if WD_EN = 1), the channels remains in indefinite cooldown and does not retry even if the channels configure to be ON through the CHx_LH_IN bits.

8.3.9 Battery Supply Input (VBB) Under-Voltage

The device includes a battery supply (VBB) undervoltage monitoring and a VDD undervoltage monitoring. Some of the internal reference and regulators and the output FETs are turned OFF when the VBB supply falls below the V_{BB_UVLOF} threshold. When the input VBB supply is lost, the device relies on the VDD supply input to keep the digital functions and registers alive. The SPI communication is also available as long as the VDD input is greater than V_{DD_UVLOF}. If VDD < V_{DD_UVLOF} and VBB > V_{BB_UVLOF} then the device is still able to enter LIMP_HOME state if LHI = 1. The VBB_UVLO fault and the VDD_UVLO bits can be read over SPI from the GLOBAL_FAULT_TYPE register. The VBB_UVLO and VDD_UVLO fault bits are latched if there is a fault for either and are cleared on read if the UVLO condition no longer exists. The following table indicates the device operation under a loss of supply condition.

Table 8-10. Device Operation Under Supply Loss Condition

	VDD < VDD_UVLO	VDD > VDD_UVLO
VBB < VBB_UVLO	• Channels are OFF • Registers are reset and digital core OFF • SPI communication not possible	• Channels are OFF • Registers are maintained and digital core is ON • SPI communication possible

Copyright © 2026 Texas Instruments Incorporated

Table 8-10. Device Operation Under Supply Loss Condition (continued)

	VDD < VDD_UVLO	VDD > VDD_UVLO
VBB > VBB_UVLO	• If WD_EN = 1 and LHI = 0 – Device is in LIMP_HOME state after watchdog timeout expires, channels output states are set by the CHx_LH_IN bits. • If WD_EN = 0 and LHI = 0 – Channels are based on CHx_ON setting • Registers are maintained and digital core is ON • Device is still able to enter LIMP_HOME state if LHI = 1 when VDD < VDD_UVLO • SPI communication not possible	• Channel output states are set by the CHx_ON bits. • Registers are maintained and digital core is ON • SPI communication possible

The register information can be lost when both the VBB and VDD supplies are below the POR and UVLO conditions respectively. The device can indicate with a register read of the POR bit in the GLOBAL_FAULT_TYPE register that a reset of the digital has occurred. This verifies that the SPI controller can identify that the register contents are all lost and the configuration registers must be rewritten. It is recommended that the bit be read if any undervoltage fault is detected.

8.3.9.1 V_{BB} During Short-to-Ground

When V_{OUT} is shorted to ground, the module power supply (V_{BB}) can have a transient decrease. This is caused by the sudden increase in current flowing through the wiring harness cables. To achieve ideal system behavior, it is recommended that the module maintain V_{BB} above the maximum V_{BB_UVLOF} threshold during V_{OUT} short-to-ground. This is typically accomplished by placing bulk capacitance on the module power supply node (V_{BB}).

8.3.10 LOW POWER MODE (LPM) States

The device offers two low-power mode (LPM) states where the device can remain on but the device operates in a low quiescent current (IQ) state to extend battery life. The device offers a manual LPM (MANUAL_LPM) state which can be entered through a SPI write to the LPM register and an automatic LPM (AUTO_LPM) state which can be entered automatically if the output current in the enabled channels is below a certain threshold for $t_{STBY_LPM_AUTO}$.

When the device is in either LPM state, SPI writes and reads are only available to the LPM register. In either LPM state, the device can continue to pass SPI data to successive devices in a daisy chain configuration and the status bits in the SDO frame can still be read. When the device transitions in and out of LPM, the fault bits in the SDO frame updates to alert the system the device has exited LPM mode.

The device can operate in the AUTO_LPM and MANUAL_LPM states if VDD is removed. However a valid VDD voltage greater than V_{DD_UVLOF} is required for the device to enter MANUAL_LPM or AUTO_LPM state. For AUTO_LPM state, if the device exits out of AUTO_LPM due to a load increase or short-circuit event VDD must be present for the device to re-enter AUTO_LPM state. If a fault occurs while VDD is removed in this state, the WAKE_SIG / FLT pin pulls low and remains low until VDD rises above V_{DD_UVLOR}.

In MANUAL_LPM state, the device disables all diagnostics as well as the watchdog timer and I2T protection to help reduce the IQ of the device. Once the device exits MANUAL_LPM, the diagnostics which are enabled before LPM entry automatically re-enable. I2T protection and the watchdog timer also re-enable after LPM exit. For AUTO_LPM state, the system must first disable the watchdog timer and all ADC diagnostics except ISNS before the device can transition into the AUTO_LPM state. The device automatically disables the I2T protection and ISNS for AUTO_LPM state and re-enables these functions when the device exits the AUTO_LPM state to the ACTIVE state. In terms of protection, short-circuit protection remains enabled in the both the LPM states. Different short-circuit thresholds are used in the LPM states compared to the short-circuit thresholds in ACTIVE state.

Copyright © 2026 Texas Instruments Incorporated

When in either of the LPM states, the device automatically responds to load current increases by transitioning to active state. If the current increase is too high the device trips its short-circuit protection. For MANUAL_LPM state, the device provides a wake signal to the microcontroller (which is in sleep mode) to wake the system up through the $\overline{FLT}$ / $\overline{WAKE_SIG}$ pin for either load increase scenario. For the AUTO_LPM state, only a load increase above the LPM short-circuit threshold (I_{SCP_AUTO}) triggers the $\overline{FLT}$ / $\overline{WAKE_SIG}$ pin to be pulled low. If a load increase in AUTO_LPM is above the exit threshold ($I_{EXIT_LPM_AUTO}$) but below the $I_{SCP_LPM_AUTO}$ threshold, the device does not pull the $\overline{FLT}$ / $\overline{WAKE_SIG}$ pin low. For both LPM states, the device only signals an overcurrent protection fault if the overcurrent is confirmed in the ACTIVE state as well.

If needed, the system can manually wake up the device from the LPM states through different SPI writes depending on the LPM state that the device is in. If LHI goes high in either of the LPM states, the device exits LPM and transitions to ACTIVE state and then to LIMP_HOME state. If OUT_DIS goes high in either of the LPM states, the device exits LPM and transitions to ACTIVE state to disable the channels if configured to be disabled.

Table Table 8-11 and Table 8-12 below highlights the key parameters for the MANUAL_LPM and AUTO_LPM states, respectively. For more information on how each LPM state operates, see the below sections on the MANUAL_LPM and AUTO_LPM states.

Table 8-11. MANUAL_LPM Characteristics

ENTRY METHOD	SPECIFICATION	DESCRIPTION	TYPICAL VALUES		UNIT
			MANUAL_LPM_MODE = 0	MANUAL_LPM_MODE = 1	
Write 1 to LPM bit in LPM register	I_{Q,VBB,LPM_MAN}	VBB IQ in LPM_MAN, Both channels enabled	12.3	14	µA
	I_{Q,VDD,LPM_MAN}	VDD IQ in LPM_MAN, Both channels enabled	16.4	17.2	µA
	R_{ON,LPM_MAN}	R_{ON} in MANUAL_LPM	24.8	5.1	mΩ
	$I_{EXIT_LPM_MAN}$	IEXIT_LPM_MAN_CHx = 00	0.95	3.1	A
		IEXIT_LPM_MAN_CHx = 01	1.2	4.1	A
		IEXIT_LPM_MAN_CHx = 10	0.33	1	A
		IEXIT_LPM_MAN_CHx = 11	0.64	2	A
	$I_{SCP_LPM_MAN}$	short-circuit threshold in MANUAL_LPM	9	25	A

Table 8-12. AUTO_LPM Characteristics

ENTRY METHOD	SPECIFICATION	DESCRIPTION	TYPICAL VALUES	UNIT
AUTO_LPM_ENTRY =1 && I_{OUTx} < $I_{ENTRY_LPM_AUTO}$ for t > $t_{STBY_LPM_AUTO}$	I_{Q,VBB,LPM_AUTO}	Both channels enabled	13.8	µA
	I_{Q,VDD,LPM_AUTO}	Both channels enabled	16.9	µA
	R_{ON,LPM_AUTO}	R_{ON} in AUTO_LPM	5.6	mΩ
	$t_{STBY_LPM_AUTO}$		20	ms
	$I_{ENTRY_LPM_AUTO}$	I_{OUTx} current to enter AUTO_LPM	1.4	A
	$I_{EXIT_LPM_AUTO}$	I_{OUTx} current to exit AUTO_LPM	2.1	A
	$I_{SCP_LPM_AUTO}$	short-circuit threshold in AUTO_LPM	25	A

8.3.10.1 MANUAL_LPM State

The MANUAL_LPM state provides a mode where the system can manually put the device into a low IQ state while keeping the channels on, if desired, and protected through short-circuit protection. To enter the MANUAL_LPM state the LPM bit in the LPM register must be set to 1. Depending on the version, before the LPM command is written to enter MANUAL_LPM the device must meet the following conditions:

- Version A
  - In active or config state with no channel state changes through CHx_ON bits
  - Enabled channels are not in the inrush period
  - I_{OUT} < $I_{ENTRY_LPM_MAN}$ for enabled channels

Copyright © 2026 Texas Instruments Incorporated

- Version B
  - In active or config state with no channel state changes through DIx pins
  - Enabled channels are not in the inrush period
  - I_{OUT} < $I_{ENTRY_LPM_MAN}$ for enabled channels

Note

It is recommended to confirm THERMAL_WARN_CHx = 0 before the system sending the device into the MANUAL_LPM state.

FLT / WAKE_SIG pin assertion during exit from MANUAL_LPM_MODE = 0 is specified for VBB levels of 7V and above.

If the above conditions are not met, the device does not transition to the MANUAL_LPM state and the MANUAL_LPM_ENTRY bit is set back to 0 and the LPM_STATUS bit in the SDO frame remains 0. If all conditions are met and 1 is written to the LPM bit the device updates the LPM_STATUS bit in the SDO frame and then transitions to the MANUAL_LPM state in t_{LPM_ENTRY}.

In the MANUAL_LPM state, the device gives the flexibility to either use the larger or smaller internal FET when in the MANUAL_LPM state. This can be set through the MANUAL_LPM_MODE bit in the LPM register. When the larger internal FET is used the RON is lower compared to the smaller internal FET and the configurable exit thresholds and short-circuit threshold is higher compared to the smaller internal FET.

8.3.10.1.1 System Wakeup from MANUAL_LPM

For TPS2HCS05A-Q1, the MCU or controller can write a 0 to the LPM bit in the LPM register to manually transition the device out of MANUAL_LPM state to the ACTIVE state. The device evaluates the AUTO_LPM_EXIT_CHx bits when a 0 is written to the LPM bit to exit the MANUAL_LPM state. If either AUTO_LPM_EXIT_CHx are 1 then the corresponding channel is enabled if not already enabled when the device is in ACTIVE state.

For TPS2HCS05B-Q1, the MCU or controller can also write a 0 to the LPM bit in the LPM register to manually transition the device out of MANUAL_LPM state to the ACTIVE state except the TPS2HCS05B-Q1 device does not evaluate the AUTO_LPM_EXIT_CHx bits. The AUTO_LPM_EXIT_CHx bits have no effect on the TPS2HCS05B-Q1. The TPS2HCS05B-Q1 also transitions out of the MANUAL_LPM state to ACTIVE state if DI1 or DI2 change states in MANUAL_LPM state.

8.3.10.1.2 Automatic Exit from MANUAL_LPM

When in MANUAL_LPM state, the device wakes up and the system through the $\overline{FLT}$ / $\overline{WAKE_SIG}$ pin when there is a load current increase beyond the programmed $I_{EXIT_LPM_MAN}$ threshold. An ECU load current demand increase above the programmed threshold activates the transition to the ACTIVE state. The threshold for $I_{EXIT_LPM_MAN}$ for each channel depends on the MAN_LPM_EXIT_CURR_CHx and MANUAL_LPM_MODE bit settings. The $I_{EXIT_LPM_MAN}$ thresholds to switchover can be programmed to the following wake up settings detailed in table xx.

If there is a larger ECU load current demand increase or output short circuit above the $I_{SCP_LPM_MAN}$, the device turns off the smaller internal FET or larger MOSFET for that channel depending on the MANUAL_LPM_MODE setting and retries with the larger MOSFET in t_{RETRY_LPM} with I_{OCP} set as the overcurrent protection threshold.

The additional load current demand and the transition to the active state is signaled to the MCU or the System Basis Chip (SBC) with a falling edge of the $\overline{FLT}$ or $\overline{WAKE_SIG}$ (active low pull-up resistor to VDD) that can be used as an interrupt by the MCU or the SBC to wake up the system. The device can then be polled over SPI to see if the $\overline{FLT}$ or $\overline{WAKE_SIG}$pin transition is caused by the load ECU current demand or a short circuit. The device registers a fault as over-current protection fault only if the overcurrent is also confirmed in the ACTIVE state.

Depending on the load step magnitude, the device transitions to the ACTIVE state in different ways. Figure 8-16 through Figure 8-21 showcase how the device responds to different load step magnitudes.

Copyright © 2026 Texas Instruments Incorporated

Once the device transitions to ACTIVE because of a load current increase, the LPM bit in the LPM register remains set to 1. To go to LPM state again, the LPM bit in the LPM register must be set to 0 and then to 1 again.

When exiting MANUAL_LPM state due to a load increase above $I_{EXIT_LPM_MAN}$ (and below $I_{SCP_LPM_MAN}$) with MANUAL_LPM_MODE = 0, the small FET remains on throughout the transition while the large FET turns on after t_{WAKE}, ramping up over t_{SLEW}. Note that t_{SLEW} in this transition is a fixed timing parameter independent of the output slew rate configured by the SLRT_CHx bits in the CHx_CONFIG register.

Table 8-13. Load Wake Up Settings - MANUAL_LPM State

MAN_LPM_EXIT_CURR_CHx in LPM Register	$I_{EXIT_LPM_MAN}$		Unit
	MANUAL_LPM_MODE = 0	MANUAL_LPM_MODE = 1	
00 (default)	0.95	3.1	A
01	1.2	4.1	A
10	0.33	1	A
11	0.64	2	A

Copyright © 2026 Texas Instruments Incorporated

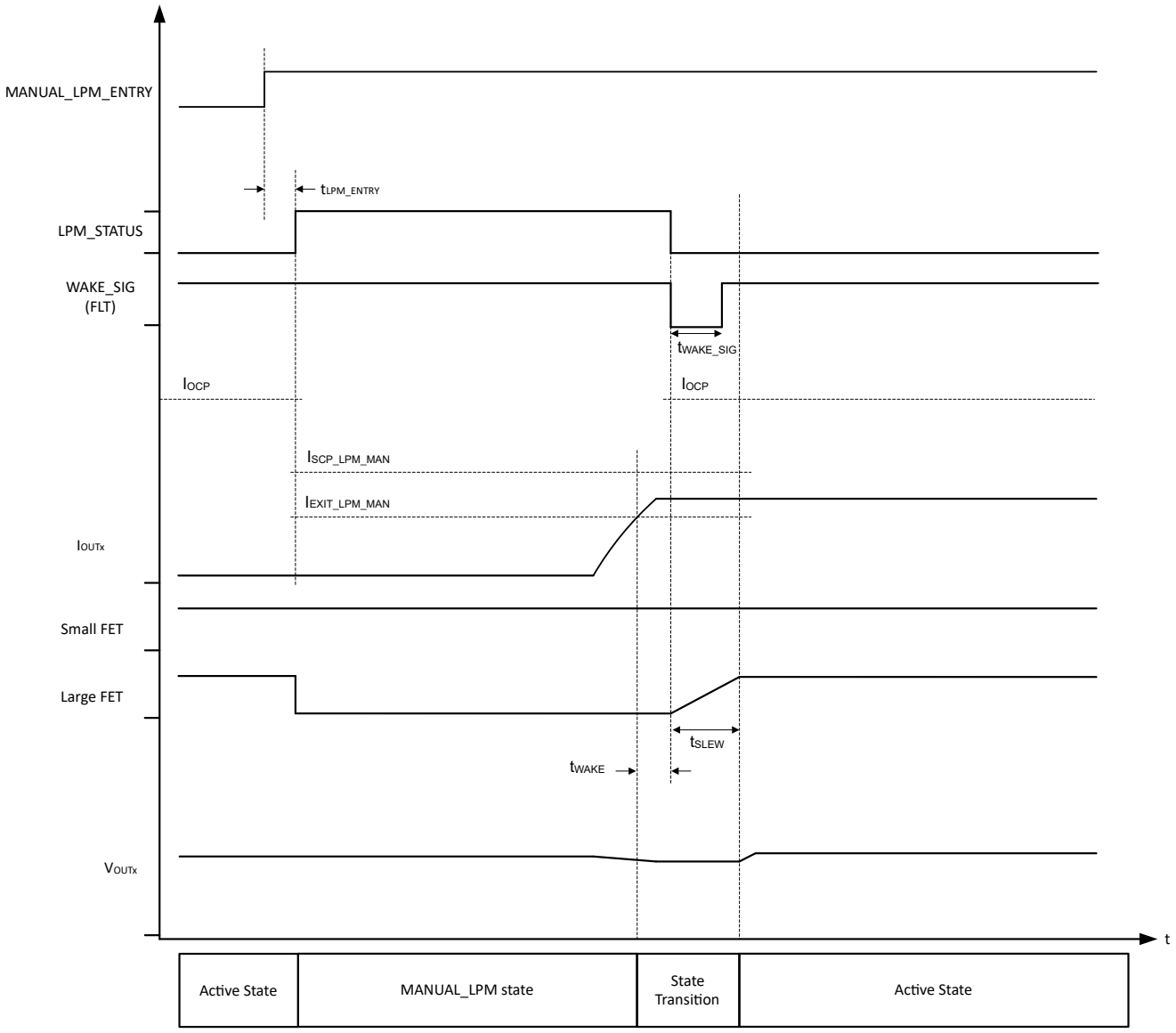


Figure 8-16. Load Increase Above $I_{EXIT_LPM_MAN}$ and Below $I_{SCP_LPM_MAN}$ in MANUAL_LPM State, MANUAL_LPM_MODE = 0

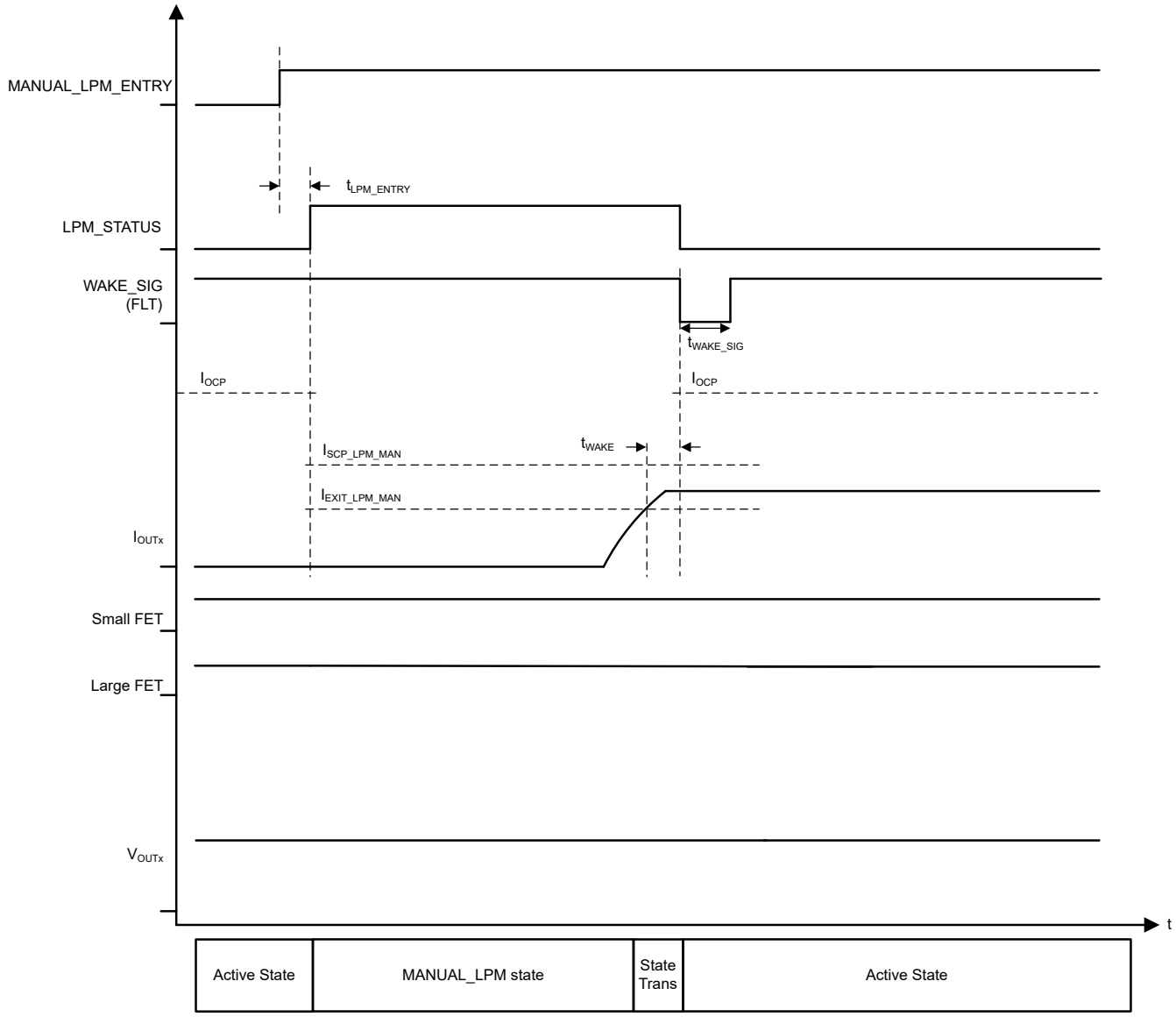


Figure 8-17. Load Increase Above $I_{EXIT_LPM_MAN}$ and Below $I_{SCP_LPM_MAN}$ in MANUAL_LPM State, MANUAL_LPM_MODE = 1

Copyright © 2026 Texas Instruments Incorporated

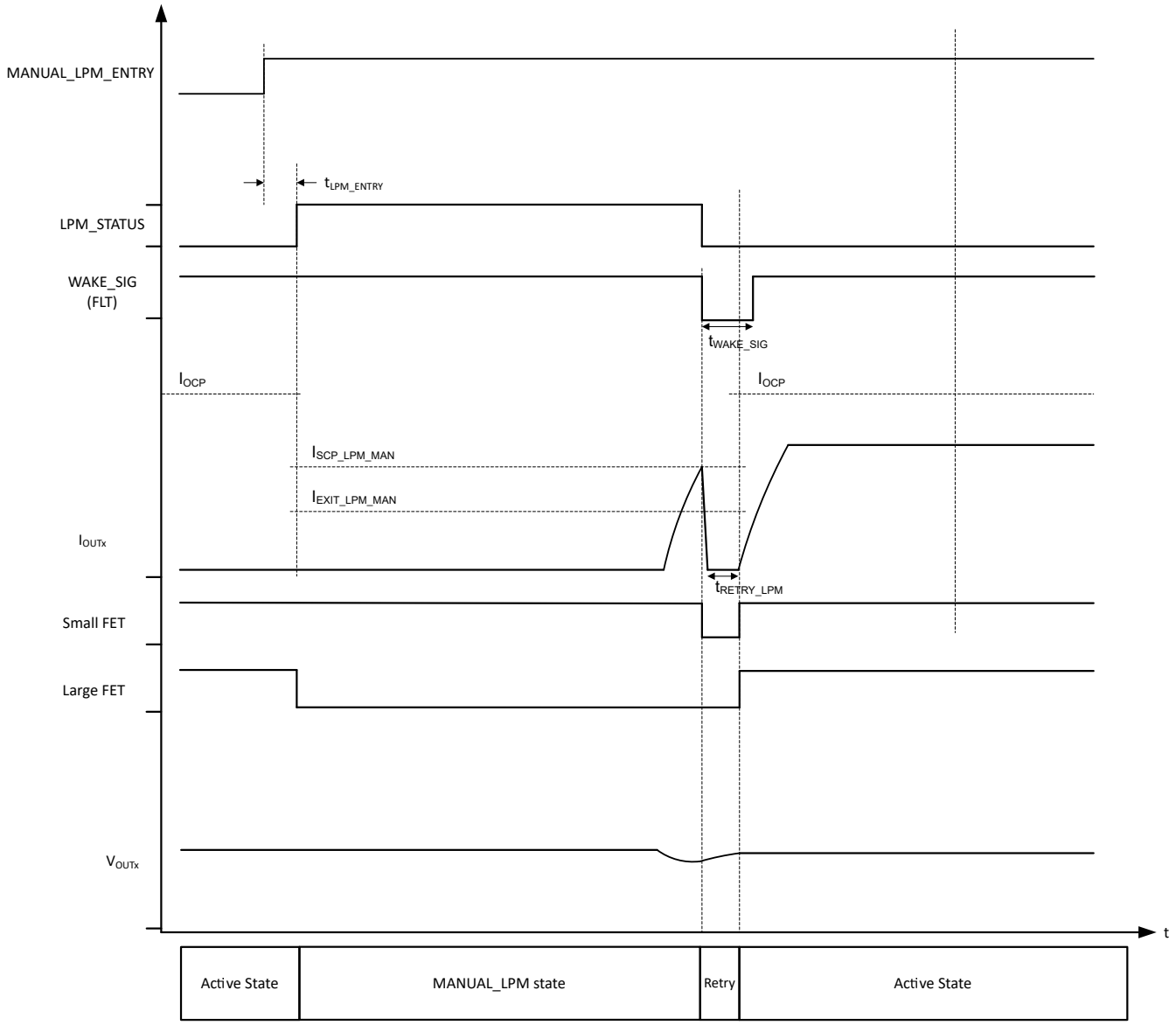


Figure 8-18. Load Increase Above $I_{SCP_LPM_MAN}$ and Below I_{OCP} in MANUAL_LPM State, MANUAL_LPM_MODE = 0

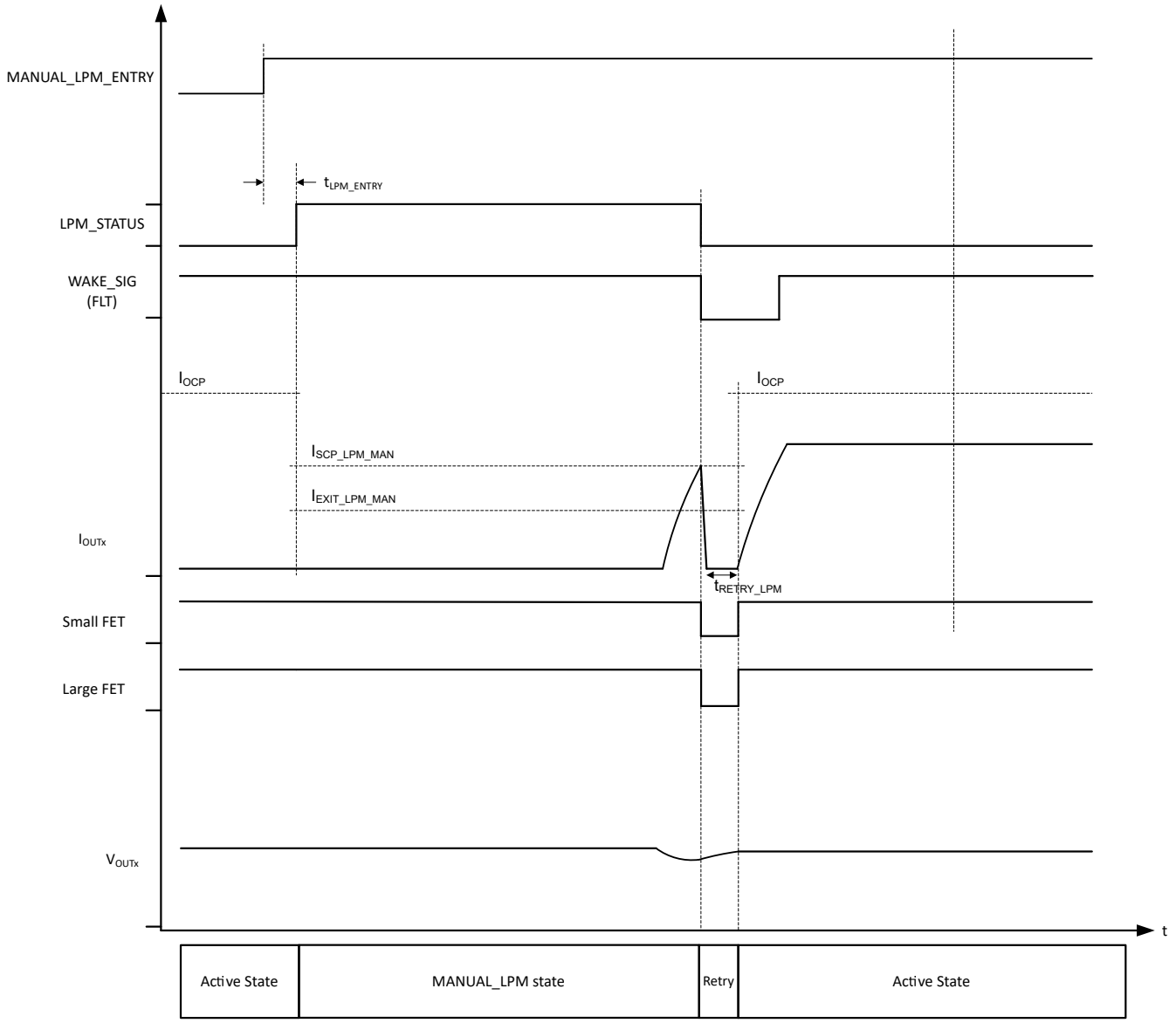


Figure 8-19. Load Increase Above $I_{SCP_LPM_MAN}$ and Below I_{OCP} in MANUAL_LPM State, LPM_MANUAL_MODE =1

Copyright © 2026 Texas Instruments Incorporated

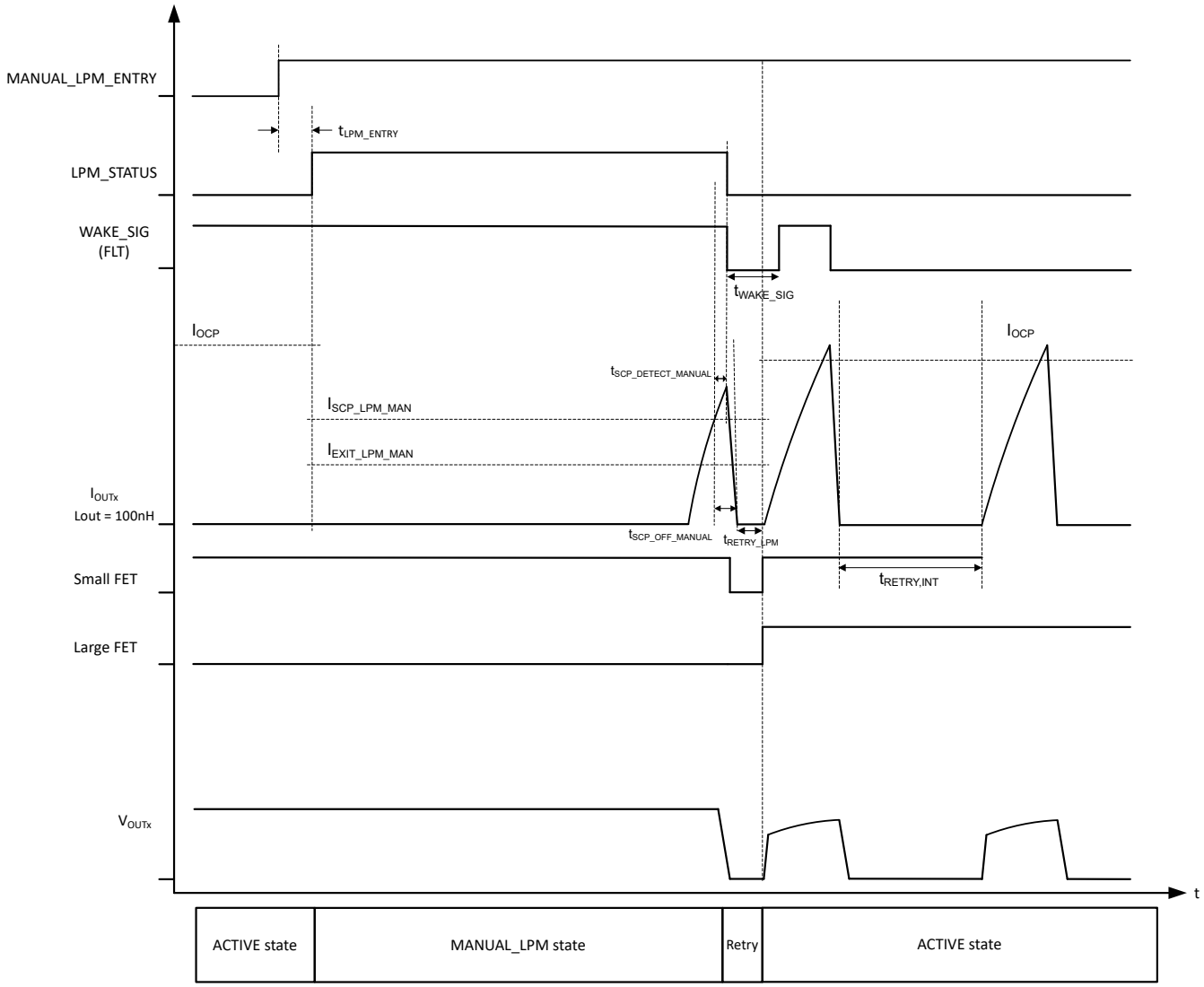


Figure 8-20. Load Increase Above I_{OCP} in MANUAL_LPM State, MANUAL_LPM_MODE = 0

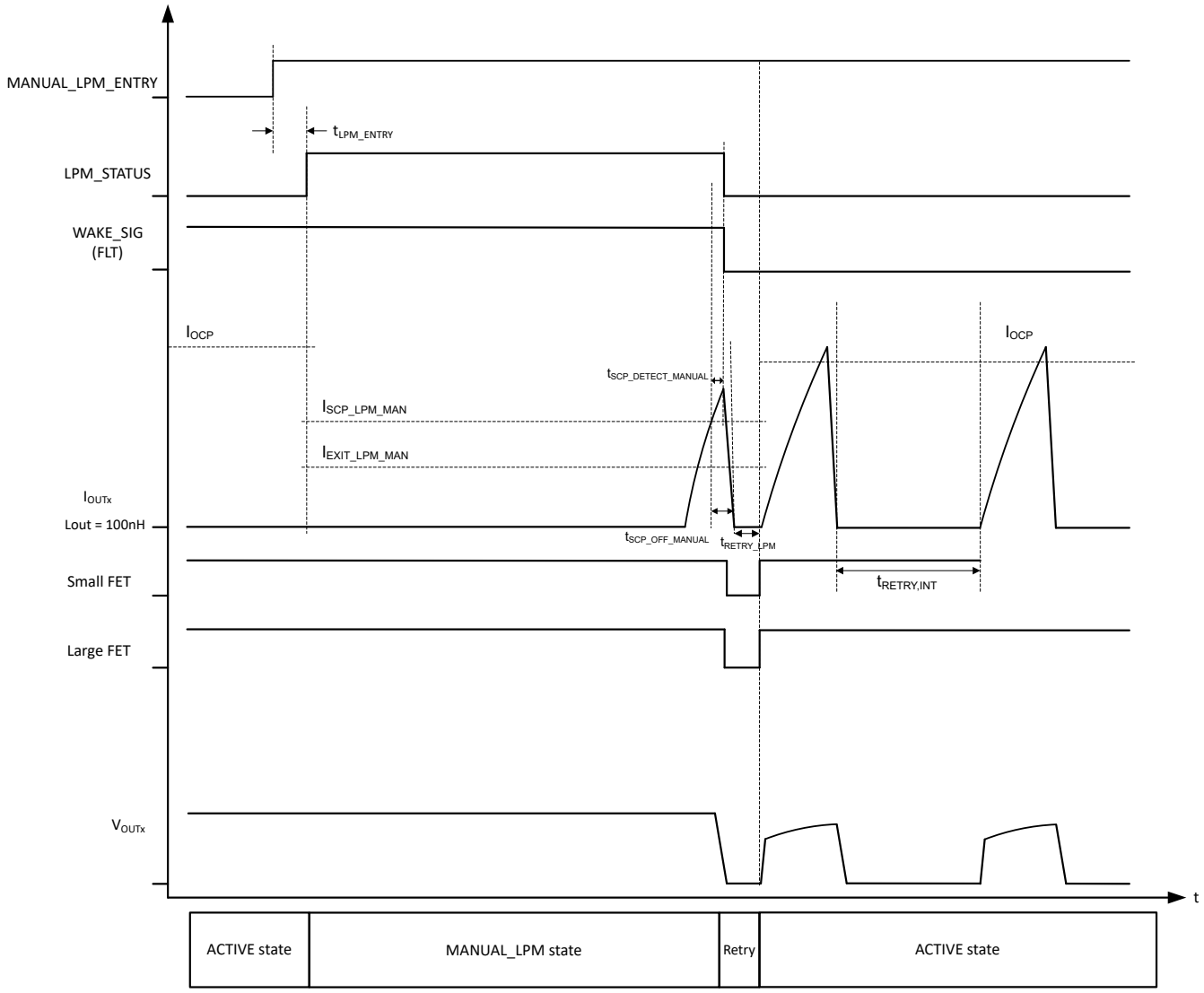


Figure 8-21. Load Increase Above I_{OCP} in MANUAL_LPM State, MANUAL_LPM_MODE = 1

8.3.10.2 AUTO_LPM State

The AUTO_LPM state provides a mode where the device can automatically transition to a low IQ state while keeping the channels on, if desired, and protected through short-circuit protection. Depending on the device version used, to enter the AUTO_LPM state the AUTO_LPM_ENTRY bit in the DEV_CONFIG register must be set to 1 and the following conditions need to be met for at least $t_{STBY_LPM_AUTO}$:

- Version A
  - In active or config state with no channel state changes through CHx_ON bits
  - Enabled channels are not in the inrush period
  - All ADC diagnostics (VSNS, VBBSNS, TSNS, and VDS_SNS) are disabled except ISNS
  - OL_ON_EN_CHx = 0
  - $I_{OUT} < I_{ENTRY_LPM_AUTO}$ for enabled channels
  - AUTO_LPM_EXIT_CHx bits must both be set to 0
  - THERMAL_WRN_CHx = 0
  - Watchdog timer is disabled (WD_EN = 0)
  - No faults exist on the device
- Version B

Copyright © 2026 Texas Instruments Incorporated

- In active or config state with no channel state changes through DIx pins
- Enabled channels are not in the inrush period
- All ADC diagnostics (VSNS, VBBSNS, TSNS, and VDS_SNS) are disabled except ISNS
- OL_ON_EN_CHx = 0
- $I_{OUT} < I_{ENTRY_LPM_AUTO}$ for enabled channels
- AUTO_LPM_EXIT_CHx bits must both be set to 0
- THERMAL_WRN_CHx = 0
- Watchdog timer is disabled (WD_EN = 0)
- No faults exist on the device

Once the conditions are met, the device updates the LPM_STATUS bit in the SDO frame/ GLOBAL_FAULT_TYPE register and the LPM_STATUS_1 bit in the GLOBAL_FAULT_TYPE register before entering the AUTO_LPM state to alert the system that device has transitioned to AUTO_LPM. The device enters AUTO_LPM state in t_{LPM_ENTRY}.

Note

Note: If the device is configured to the MANUAL_LPM state before setting the AUTO_LPM_ENTRY bit to 1, additional SPI commands are required to enable Auto LPM Entry. To specify a safe transition from Manual LPM to Auto LPM, if the device exits Manual LPM due to a Load Step or Short Circuit event, the MANUAL_LPM bit must be set to 1 and then reset to 0. After this entry and exit from the Manual LPM state is complete, the AUTO_LPM_ENTRY bit can be set to 1, and the device enters Auto LPM once all conditions are met.

In the AUTO_LPM state, the larger internal FET is used to allow for larger load steps. The R_{ON} for the larger internal FET is defined by the R_{ON,LPM_AUTO} in the electrical characteristics section. The IQ in AUTO_LPM is higher compared to the small FET operation in MANUAL_LPM state and roughly the same as the MANUAL_LPM state with the larger FET operation. In AUTO_LPM, the entry threshold is specified by $I_{ENTRY_LPM_AUTO}$ and the exit threshold is specified by $I_{EXIT_LPM_AUTO}$.

8.3.10.2.1 System Wakeup from AUTO_LPM

For TPS2HCS05B-Q1, the AUTO_LPM_EXIT_CH bit has no effect on the TPS2HCS05B-Q1. The system can manually transition the TPS2HCS05B-Q1 device out of AUTO_LPM by changing the state of the DI pin in AUTO_LPM state.

For TPS2HCS05A-Q1, the MCU or controller can write a 1 to the either or both AUTO_LPM_EXIT_CHx bits to manually transition the device out of the AUTO_LPM state to the ACTIVE state. If either AUTO_LPM_EXIT_CHx are 1 then the corresponding channel is enabled if not already enabled when the device is in ACTIVE state. For TPS2HCS05A-Q1, both AUTO_LPM_EXIT_CHx bits have to be set back to 0 before the device is allowed to transition back to the AUTO_LPM state.

For TPS2HCS05B-Q1, the AUTO_LPM_EXIT_CHx bits have no effect on the TPS2HCS05B-Q1. The system can manually transition the TPS2HCS05B-Q1 device out of AUTO_LPM by changing the state of DI1 or DI2 or both in AUTO_LPM state.

8.3.10.2.2 Automatic Exit from AUTO_LPM

When in AUTO_LPM state, the device wakes up and changes the LPM_STATUS bit to 0 when there is a load current increase beyond the $I_{EXIT_LPM_AUTO}$ threshold. The LPM_STATUS_1 bit in the GLOBAL_FAULT_TYPE register is set to 1 when in AUTO_LPM state and is read clear which enables the system to tell if the device had transitioned to the AUTO_LPM state since the GLOBAL_FAULT_TYPE register is last read. An ECU load current demand increase above the $I_{EXIT_LPM_AUTO}$ threshold activates the transition to the ACTIVE state. Note, in this load increase scenario the device does not pull the $\overline{FLT}$ / $\overline{WAKE_SIG}$ low.

If there is a larger ECU load current demand increase or output short circuit above the $I_{SCP_LPM_AUTO}$, the device turns off the internal FET for that channel and retries in $t_{RETRY,INT}$ with I_{OCP} set as the overcurrent protection threshold. In this scenario, the device pulls the $\overline{FLT}$ / $\overline{WAKE_SIG}$ pin low when there is a load current increase

Copyright © 2026 Texas Instruments Incorporated

beyond the $I_{SCP_LPM_AUTO}$ threshold. The device registers a fault as over-current protection fault only if the overcurrent is also confirmed in the ACTIVE state.

Depending on the load step magnitude, the device transitions to the ACTIVE state in different ways. Figure 8-22, Figure 8-23, and Figure 8-24 showcase how the device responds to different load step magnitudes.

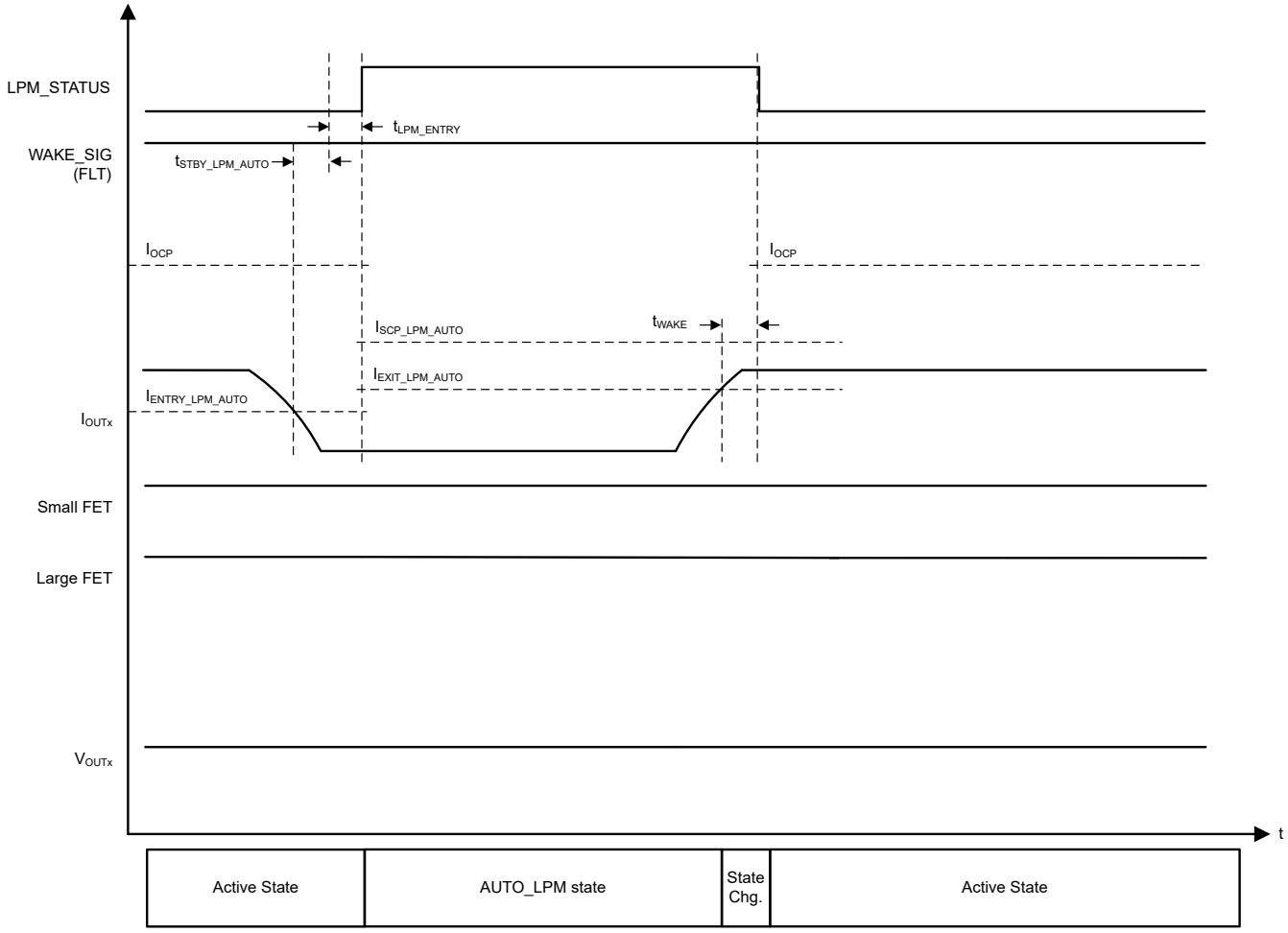


Figure 8-22. Load Increase Above $I_{EXIT_LPM_AUTO}$ and Below $I_{SCP_LPM_AUTO}$ in AUTO_LPM State

Copyright © 2026 Texas Instruments Incorporated

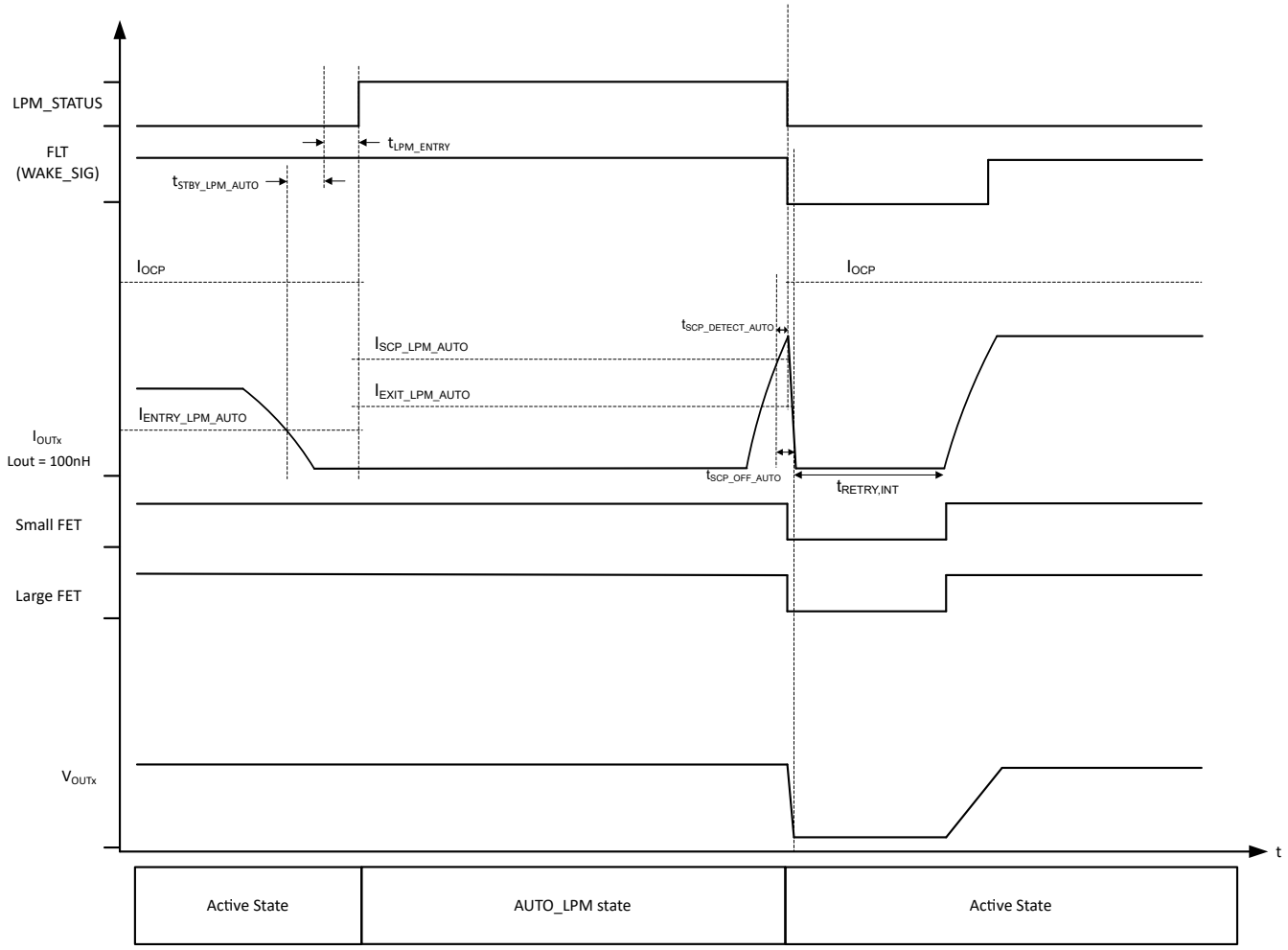


Figure 8-23. Load Increase Above $I_{SCP_LPM_AUTO}$ and Below I_{OCP} in AUTO_LPM State

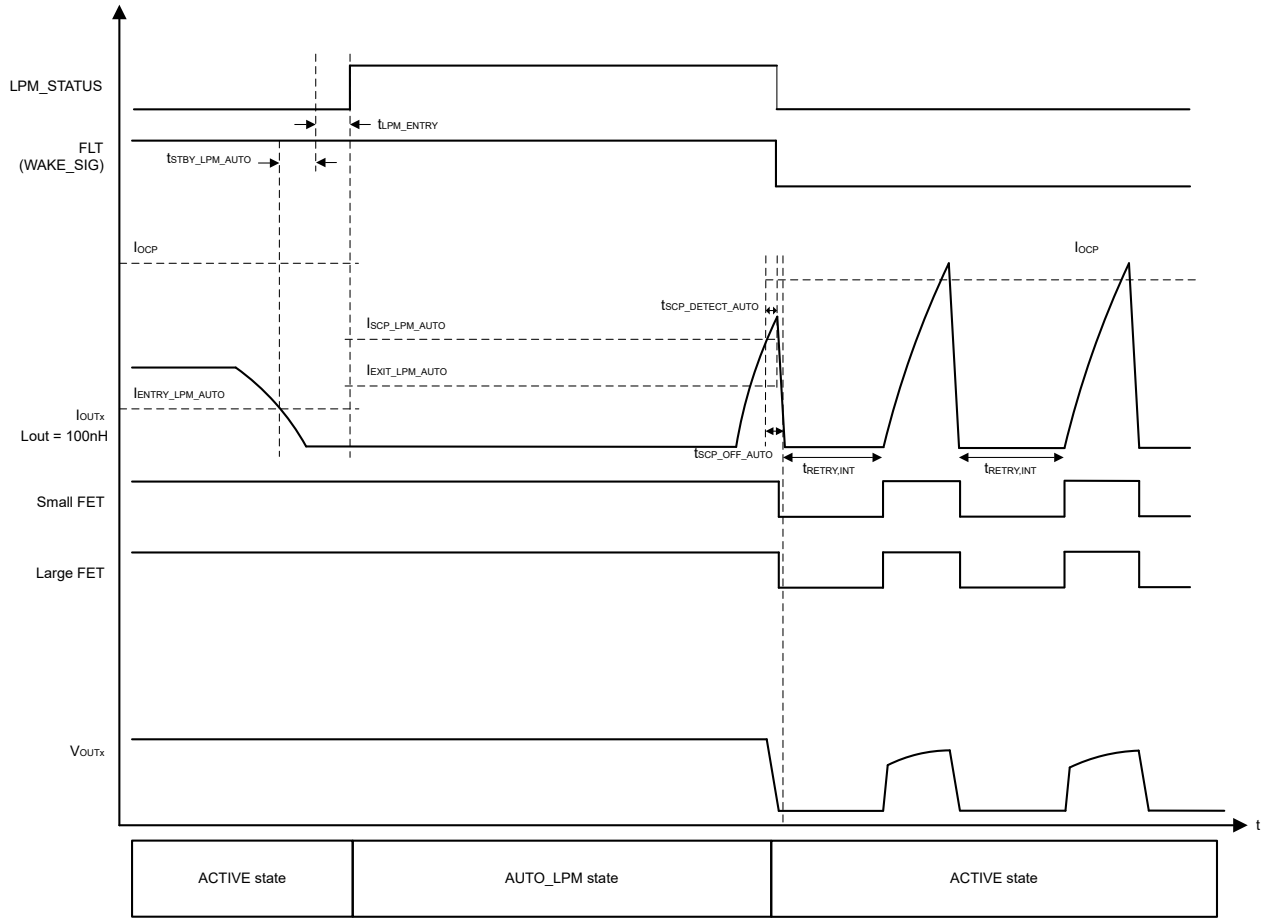


Figure 8-24. Load Increase Above I_{OCP} in AUTO_LPM State

8.4 Feature Description

8.4.1 Protection Mechanisms

8.4.1.1 Overcurrent Protection

The TPS2HCS05-Q1 device offers the following functions to protect the device from different overcurrent events:

- Capacitive load charging in inrush period
- Immediate shutdown overcurrent protection (I_{OCP})
- Programmable fuse protection (or I2T protection) (if enabled)
- Thermal shutdown (T_{REL} and T_{ABS})
- Short-circuit protection ($I_{SCP_LPM_MAN}$ or $I_{SCP_LPM_AUTO}$) in LPM states

In regard to overcurrent protection, the device has two operation modes, an optional inrush period at channel startup and during steady state operation. The optional inrush period can be configured to allow the device to handle different inrush currents such as bulbs, motor stall currents, or capacitive loads at the initial turn on of a channel. The CAP_CHRG_CHx, INRUSH_DURATION_CHx, and INRUSH_LIMIT_CHx bits in the ILIM_CONFIG_CHx registers control the operation of the device in the inrush period. I2T protection (if enabled) is only active in the inrush period if CAP_CHRG_CHx = 00 and if $V_{DS} < V_{DS_LT_2V}$. Steady state operation takes over after the inrush period has completed. During steady state operation, overcurrent protection (I_{OCP}) is active and I2T protection is active (if enabled).

During the inrush period all voltage sensing (VBB, VOUT, and VDS) and FET temperature sensing can be used if enabled. Current sensing is only available in CAP_CHRG_CHx = 00 when $V_{DS} < V_{DS_LT_2V}$ or after the inrush period has completed and the device is in steady state operation. All voltage sensing, FET temperature sensing, and current sensing is available in the steady operation.

Copyright © 2026 Texas Instruments Incorporated

Figure 8-25 provides an overview of the overcurrent protection in the optional inrush period and steady state operation.

For more details on the different protections available in the inrush period and in steady state, see the following sections. Overcurrent protection in the LPM states is covered in the LPM section.

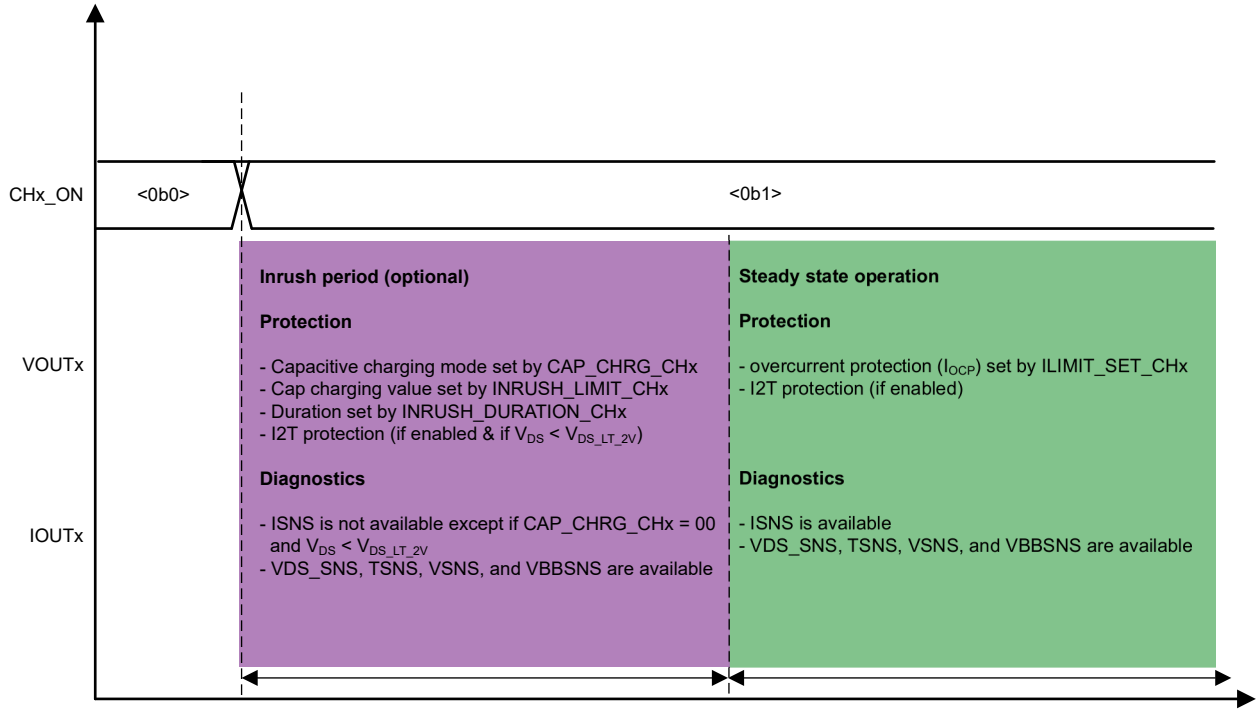


Figure 8-25. Overcurrent Protection Modes Overview

8.4.1.1.1 Inrush Period - Overcurrent Protection

The inrush period is an optional mode of the device where it can be configured to allow the device to handle different inrush currents such as bulbs, motor stall currents, or capacitive loads at the initial turn on of a channel. The inrush period can be configured through the CAP_CHRG_CHx, INRUSH_DURATION_CHx, and INRUSH_LIMIT_CHx bits in the ILIM_CONFIG_CHx registers. If the inrush period is enabled, it takes effect in both the ACTIVE state and the LIMP_HOME state if a channel is enabled in either of these states.

The device offers two different overcurrent protection settings in the inrush period which can be set through the CAP_CHRG_CHx bits:

- No capacitive charging - immediate shutdown overcurrent protection (I_{OCP}) only
- Current limit regulation (I_{CL_REG})

The no capacitive charging setting, enables the device to have a different overcurrent protection (I_{OCP}) value in the inrush period compared to steady state to allow for bulb current inrush or motor stall current. Additionally, in the no capacitive charging setting, I2T protection (if enabled) is active if $V_{DS} < V_{DS_LT_2V}$. The current limit regulation mode, allows for the device to charge up large capacitances such as input capacitors on downstream ECUs. Depending on the CAP_CHRG_CHx bit settings, the values of the INRUSH_LIMIT_CHx change. The overcurrent protection for each channel is independent and can be set on an per channel basis. Table 8-14 provides an overview of the two overcurrent protections in the inrush period.

Copyright © 2026 Texas Instruments Incorporated

Table 8-14. Overview of Capacitive Charging Mode in Inrush Period

CAPACITIVE CHARGING MODE (CAP_CHRG_CHx)	OVERCURRENT TYPE	RANGE	DURATION SET BY	VALUE SET BY	I2T SUPPORTED
00	Immediate shutdown (I_{OCP})	14.5A to 76A	INRUSH_DURATION_CHx [2:0]	INRUSH_LIMIT_CHx [3:0]	Yes, if $V_{DS} < V_{DS_LT_2V}$
01	Not supported				
10	Current limit regulation (I_{CL_REG})	2A to 18.2A	INRUSH_DURATION_CHx [2:0]	INRUSH_LIMIT_CHx [3:0]	No
11	Not supported				

The INRUSH_DURATION_CHx bits set the duration of the inrush period. It can be set from 0ms to 100ms. If the INRUSH_DURATION_CHx = 0, the inrush period duration sets to 0ms and the inrush period is not entered when the channel is initially enabled. If a retry occurs due to an overcurrent or thermal shutdown fault in the inrush period, the timer for exiting the inrush period resets after each retry.

8.4.1.1.1.1 No Capacitive Charging - CAP_CHRG_CHx [1:0] = 00

The no capacitive charging setting, enables the device to have a different immediate shutdown overcurrent protection (I_{OCP}) value in the inrush period compared to steady state operation to allow for different inrush events at startup such as bulb current inrush or motor stall current.

If CAP_CHRG_CHx [1:0] = 00, the immediate shutdown overcurrent protection (I_{OCP}) value in the inrush period is set by the INRUSH_LIMIT_CHx [3:0] bits and the duration is set by the INRUSH_DURATION_CHx [2:0] bits. Once the inrush period duration timer expires the immediate shutdown overcurrent protection (I_{OCP}) value is set by the ILIMIT_SET_CHx [3:0] bits in steady state operation.

If CAP_CHRG_CHx [1:0] = 00, I2T protection (if enabled) and current sensing is available if $V_{DS} < V_{DS_LT_2V}$.

An example of this is shown in the figure below.

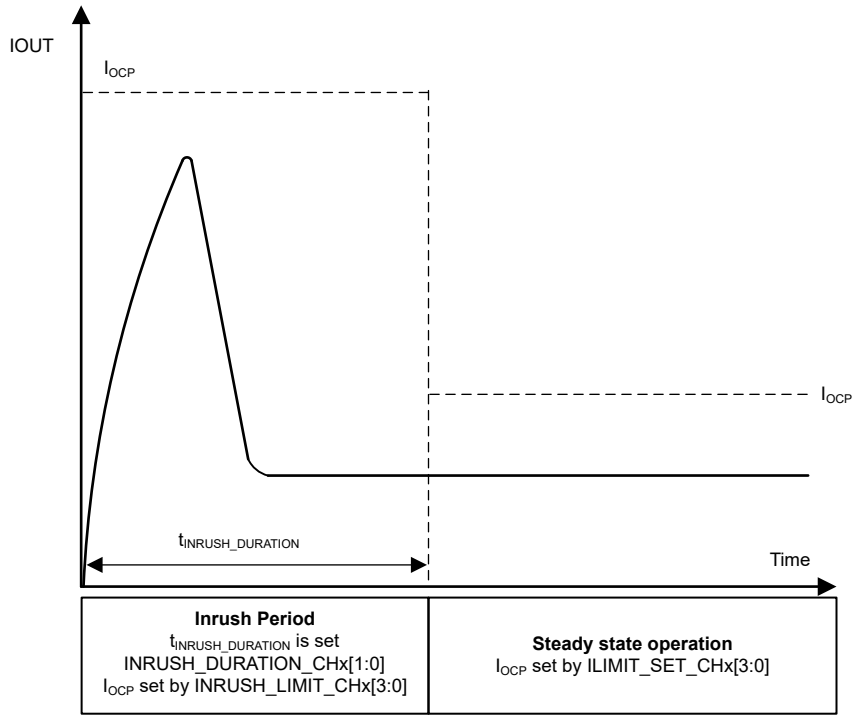


Figure 8-26. No Capacitive Charging (CAP_CHRG_CHx [1:0] = 00) - Bulb Driving Example

Copyright © 2026 Texas Instruments Incorporated

8.4.1.1.1.2 Current Limit Regulation Capacitive Charging Mode - CAP_CHRG_CHx [1:0] = 10

The device offers a current limit regulation capacitive charging mode to charge up large downstream capacitive loads such as bulk input capacitors on ECUs. If CAP_CHRG_CHx [1:0] = 10, the current limit regulation mode clamps the output current when the channel is initially enabled at a value set by the INRUSH_LIMIT_CHx [3:0]. The device limits the current continuously until the capacitive load has finished charging, the inrush period expires, or a thermal shutdown has occurred. The range of settings which can be programmed through the INRUSH_LIMIT_CHx [3:0] are from 2A to 18.2A and are specified in the electrical characteristic table as I_{CL_REG}. If the VOUT voltage is greater than VBB - 2V and the inrush period timer has not expired, the device can slowly exit the current limit regulation without a large spike. An example of the current limit regulation capacitive charging mode and the slow exit before the inrush period timer expiration is shown in the figure below.

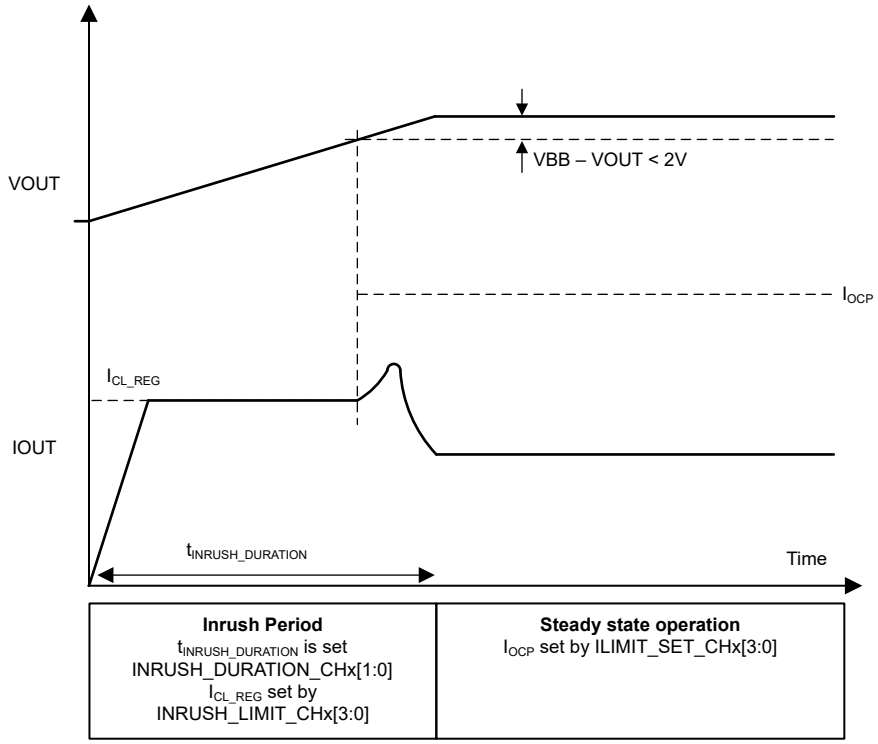


Figure 8-27. Current Limit Regulation Capacitive Charging (CAP_CHRG_CHx [1:0] = 10) - ECU Input Bulk Capacitance Driving Example

8.4.1.1.2 Overcurrent Protection - Steady State Operation

After the device has completed the optional inrush period (if enabled) the device enters the steady operation. In this operation, the overcurrent protection is provided by the immediate shutdown overcurrent protection (I_{OCP}) and I2T protection (if enabled). The I_{OCP} is an overcurrent protection function that immediately turns off the channel if the output current exceeds I_{OCP} threshold that is set by the ILIMIT_SET_CHx [3:0] bits. The I_{OCP} function cannot be disabled and is always active in the steady state operation while the device is enabled. The I2T protection provides a programmable fuse protection that is based on a defined time-current curve. The intent of the I2T protection is to match the behavior of a melting fuse. The time-current curve of the I2T protection can be set through the NOM_CUR_CHx [2:0] bits and I2T_TRIP_CHx [3:0] bits. The ISWCL_CHx [1:0] and I_{OCP} also help to define the time-current curve for the I2T protection. The I_{OCP} and I2T protection (if enabled) are active in the ACTIVE state and the LIMP_HOME state if the channel is in the steady state operation after the inrush period.

The next sections describes the I2T protection and the I_{OCP} protection.

Copyright © 2026 Texas Instruments Incorporated

8.4.1.1.3 Programmable Fuse Protection

The device includes a programmable fuse protection for each channel, that is based on a defined time-current curve and is commonly referred to as I2t protection in melting fuse datasheets. The intent is to match the switch turnoff behavior of a melting fuse. The NOM_CUR_CHx [2:0] bits and I2T_TRIP_CHx [3:0] bits set the time-current curve but the device also uses a fixed delay shutdown (I_{SWCL}) and immediate shutdown protection (I_{OCP}) to create the full I2T protection for the device. The I2T protection of the TPS2HCS05-Q1 consists of four regions:

1. Nominal current
2. Fuse shutdown
3. Fixed delay shutdown
4. Immediate shutdown protection (I_{OCP})

The nominal current region (1) defines the region where the device can supply current indefinitely without turning off. This is roughly equivalent to the fuse current rating of a melting fuse. This region is set by the NOM_CUR_CHx [2:0] bits and if the output current is less than the NOM_CUR_CHx setting then the device can supply current indefinitely as previously stated and does not start the I2T accumulation. If the output current is greater than or equal to the NOM_CUR_CHx setting then the device enters the I2T accumulation loop and starts to accumulate until the I2T_TRIP_CHx [3:0] threshold is met. If the output current falls back below the NOM_CUR_CHx before the I2T_TRIP_CHx value is reached then the device stops the I2T accumulation but still keeps track of the accumulated energy as long as power is provided to the device.

Above the nominal current region, is the fuse shutdown region (2) which is set by the I2T_TRIP_CHx [3:0] bits. This region defines the curvature of time-current curve and the region where the I2T accumulation of the device is active. Based on the output current level and the NOM_CUR_CHx setting the device trips at different time intervals based on the I2T_TRIP value that is set. The time-current curve of the device is defined by the following equations.

If DCR_CHx = 0, then the device accumulates according to Equation 1 and decrements according to Equation 2.

$$\text{I2T_TRIP} = (\text{I}_{\text{OUT}})^2 \times \text{t} \quad (1)$$

$$\text{I2T_TRIP} = \left(\text{I}_{\text{OUT}}{}^2 - \text{k} \times \text{NOM_CUR_CHx}^2\right) \times \text{t} \quad (2)$$

Note

The decrement factor "k" in Equation 2 is determined by ACC_DCR0_CHx bits in the I2T_CONFIG_CHx register.

If DCR_CHx = 1, then devices accumulates and decrements according to Equation 3.

$$\text{I2T_TRIP} = \left(\text{I}_{\text{OUT}}{}^2 - \text{NOM_CUR_CHx}^2\right) \times \text{t} \quad (3)$$

If the accumulation does not exceed the I2T_TRIP value and the current falls below NOM_CUR_CH then Equation 2 or Equation 3 depending on the DCR_CHx setting is used to decrement the accumulated energy based on the ISNS value until the accumulated energy reaches zero. While the device continues to decrement down to zero, the I2T_MOD bit remains 1 until accumulated energy returns back to zero and then the I2T_MOD bit sets back to zero. If any conversions are disabled due to a channel entering the I2T loop then those conversions are re-enabled when I2T_MOD = 0.

Above the fuse shutdown region, is the fixed delay shutdown region (3) where the device provides a fixed delayed shutdown that is set by the ISWCL_CHx [1:0] and SWCL_DLY_TMR_CHx [1:0] bits. The ISWCL_CHx [1:0] sets the output current value and the SWCL_DLY_TMR_CHx sets the time. If the output current exceeds the ISWCL_CHx level continuously for SWCL_DLY_TMR_CHx then the channel immediately turns off.

Copyright © 2026 Texas Instruments Incorporated

If a shutdown occurs either due to the I2T_TRIP_CHx value being exceeded or due to the ISWCL_CHx function, the device remains off for a period set by the TCLDN_CHx [1:0]. If the TCLDN_CHx [1:0] = 00 then the device remains off and does not retry. To retry in this setting, the TCLDN_CHx [1:0] bits need to be changed to another setting. Once the setting has been changed, the device retries after the defined cool down time of the new setting. Note, when the channel enters the I2T shutdown state the accumulator value resets to 0 so the retry time must be adjusted to make sure enough time has elapsed for the wire harness to cool down. Also note, when the channel enters the I2T shutdown state, the values for NOM_CUR_CHx, I2T_TRIP_CHx, and ISWCL_CHx cannot be changed.

Above the fixed delay shutdown region, is the immediate shutdown overcurrent protection (I_{OCP}) region (4). This region is set by the ILIMIT_SET_CHx [3:0] bits. If the output current exceeds the I_{OCP} level then the device turns off immediately. The retry or latched off behavior for the I_{OCP} is set by the LATCH_CHx bit and described in the next section.

These operational regions for the I2T protection are show in Figure 8-28.

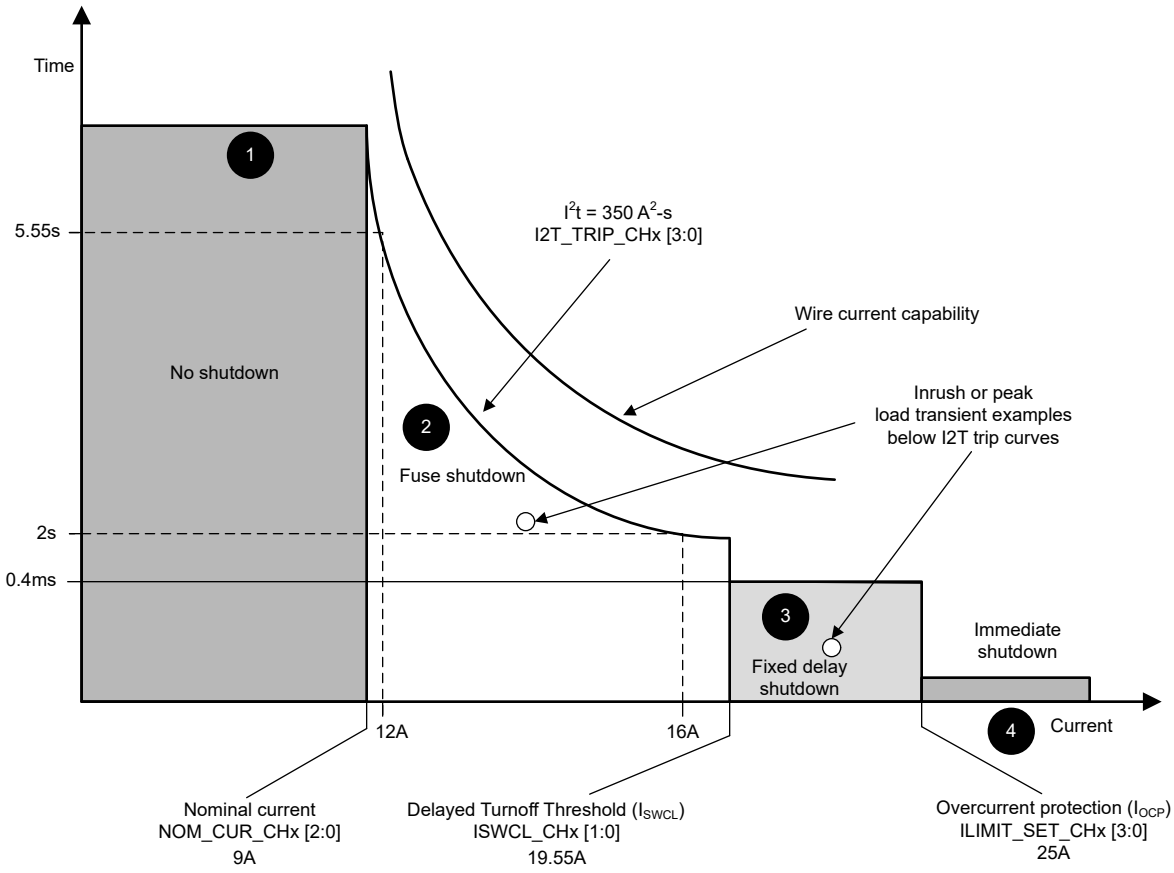


Figure 8-28. Operational Region of Fuse Based Shutdown

The values for the NOM_CUR_CHx, I2T_TRIP_CHx, and ISWCL_CHx in the register map are based on an R_{SNS} value of 700Ω. The device offers the flexibility for these values to be scaled based on different R_{SNS} values. The equations for scaling the NOM_CUR_CHx, I2T_TRIP_CHx, and the ISWCL_CHx are defined below.

$$NOM_CUR_{ADJ,\,TYP} = \frac{NOM_CUR_{700} \times 700}{R_{SNS,\,ADJ,\,TYP}} \quad (4)$$

$$I_{SWCL,\,ADJ,\,TYP} = \frac{I_{SWCL,\,700} \times 700}{R_{SNS,\,ADJ,\,TYP}} \quad (5)$$

Copyright © 2026 Texas Instruments Incorporated

$$I2T_{ADJ.TYP} = I2T_{700} \times \left(\frac{700}{R_{SNS,ADJ,TYP}}\right)^2 \quad (6)$$

where,

$$NOM_CUR_{700} = \text{NOM_CUR_CHx value in the datasheet based on } R_{SNS} \text{ of } 700\Omega \quad (7)$$

$$I_{SWCL,700} = I_{SWCL} \text{ value in the datasheet based on } R_{SNS} \text{ of } 700\Omega \quad (8)$$

$$I2T_{700} = \text{I2T trip value in the datasheet based on } R_{SNS} \text{ of } 700\Omega \quad (9)$$

8.4.1.1.4 Immediate Shutdown Overcurrent Protection (I_{OCP})

In steady state operation, the device offers immediate shutdown overcurrent protection (I_{OCP}) which is an overcurrent protection function that immediately turns off the channel if the output current exceeds the I_{OCP} threshold that is set by the ILIMIT_SET_CHx [3:0] bits. The ILIMIT_SET_CHx [3:0] bits enable the I_{OCP} function to be set on a per channel basis. The IOCP limit can vary within a device from the typical value mentioned in the specifications, particularly at higher ILIMIT_SET_CHx [3:0] settings. The I_{OCP} function cannot be disabled and is always active in the steady state operation while the device is enabled.

If the I_{OCP} level is exceeded, the channel turns off immediately and the channel either retries or latches-off based on the setting of the LATCH_CHx bit. If LATCH_CHx = 0, the channel retries after $t_{RETRY,INT}$. After the retry time expires, the channel starts up into the inrush period if configured. If the short-circuit condition persists, the channel continues to retry with $t_{RETRY,INT}$ between retries for up to $n_{RETRY,INT}$ times. If still the short-circuit condition exists, the channel retries an additional $n_{RETRY,EXTD}$ times with $t_{RETRY,EXTD}$ between retries before the channel is latched off. To remove the device out of the latch off state with LATCH_CHx = 0, the CHx_ON bit (version A) must be toggled or the DIx pin (version B) must be toggled. If LATCH_CHx = 1 and the I_{OCP} level is exceeded, the device latches-off and does not retry until the CHx_ON bit (version A) is toggled or the DIx pin (version B) is toggled or the LATCH_CHx bit is toggled. For more details on how the retry and latch off works for different device settings, see the retry and latch-off behavior section below.

Under certain combinations of ILIMIT_SET_CHx[3:0] setting, VBB voltage, and operating temperature, the WAKE_SIG / FLT pin may exhibit toggling behavior during OCP retry cycles instead of remaining continuously asserted until the fault clears. At lower ILIMIT_SET_CHx[3:0] settings, the WAKE_SIG / FLT pin typically asserts on the initial fault event and stays latched low until the fault is cleared, as expected. At higher ILIMIT_SET_CHx[3:0] settings, the WAKE_SIG/FLT pin may instead toggle with each retry cycle rather than staying latched, with the behavior becoming more consistent (fully latching as expected) as VBB increases. Because this behavior can vary with ILIMIT_SET_CHx[3:0] setting, VBB, and temperature, designers monitoring the WAKE_SIG / FLT pin under high-current fault conditions should account for possible transient toggling during initial retry cycles and should not rely solely on the first WAKE_SIG / FLT transition to confirm a latched fault condition.

Note, in LIMP_HOME state the device continuously retries regardless of the LATCH_CHx setting if the channel is configured to be ON in LIMP_HOME state through the CHx_LH_IN bits.

8.4.1.1.5 Auto retry and latch-off behavior

When a thermal shutdown or an immediate shutdown overcurrent protection fault occurs, the channel with the fault will either auto-retry for fixed number of retries or latch off based on the LATCH_CHx bit setting in the CHx_CONFIG registers. Depending on the CAP_CHRG_CHx settings and the I_{OCP} level, the auto retry response behaves differently.

Note, in LIMP_HOME state the device continuously retries regardless of the LATCH_CHx setting if the channel is configured to be ON in LIMP_HOME state through the CHx_LH_IN bits. The retry behavior in LIMP_HOME state follows the below sections depending on the I_{OCP} level and how the CAP_CHRG_CHx bits are configured.

Copyright © 2026 Texas Instruments Incorporated

8.4.1.1.5.1 Auto retry behavior - No capacitive charging mode (CAP_CHRG_CHx = 00)

If CAP_CHRG_CHx = 00 and LATCH_CHx = 0 and a short-circuit event occurs, after the channel turns off and $t_{RETRY,INT}$ expires the device retries in the inrush period with the I_{OCP} level set through the INRUSH_LIMIT_CHx [3:0] bits. The INRUSH_DURATION_CHx [2:0] still sets the duration of the inrush period. If the I_{OCP} level is greater than the $I_{OCP_RETRY_FLBK}$ and the number of retries is greater than n_{RETRY} then the device foldsback to the $I_{OCP_RETRY_FLBK}$ level and then retries and continues to retry at this level until the short is removed or the channel is toggled. The figures below showcases these hot short cases that occur in steady state operation with I_{OCP} below $I_{OCP_RETRY_FLBK}$ and I_{OCP} above $I_{OCP_RETRY_FLBK}$, respectively. Starting into a short in the inrush period results in the same retry behavior as a hot short in steady state except the first initial overcurrent shutdown level is determined by the INRUSH_LIMIT_CHx [3:0].

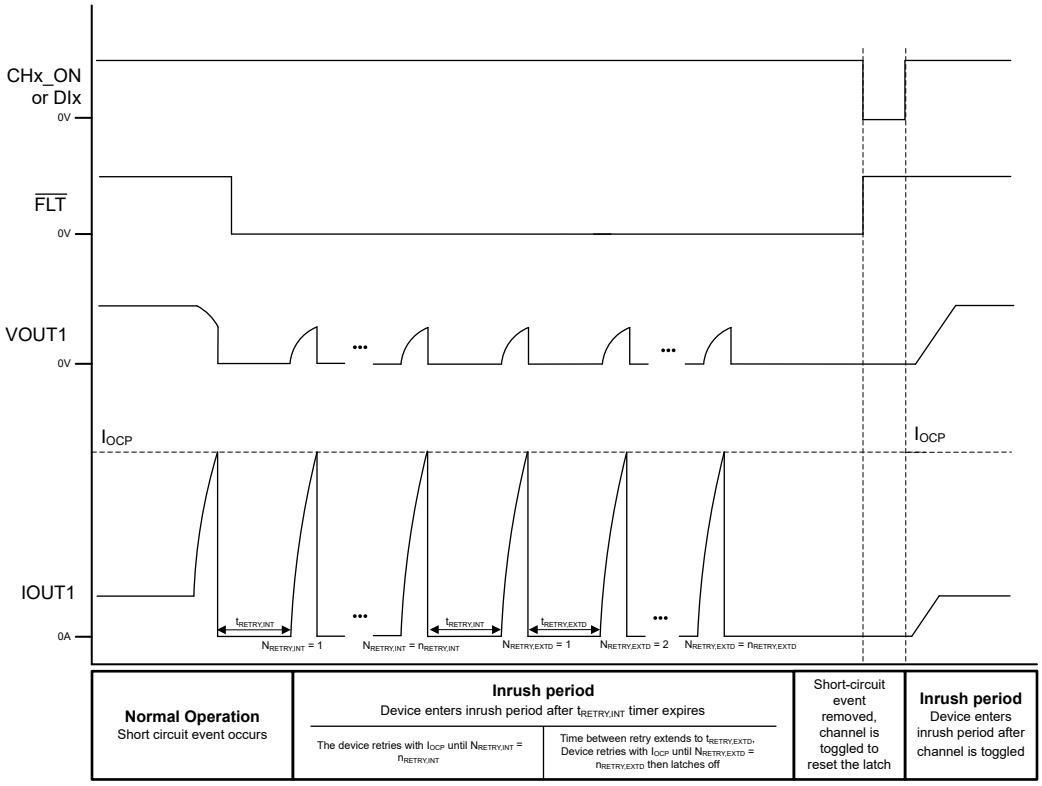


Figure 8-29. Hot short During Steady State Operation With CAP_CHRG_CHx = 00, Auto-retry (LATCH_CHx = 0), and $I_{OCP} < I_{OCP_RETRY_FLBK}$

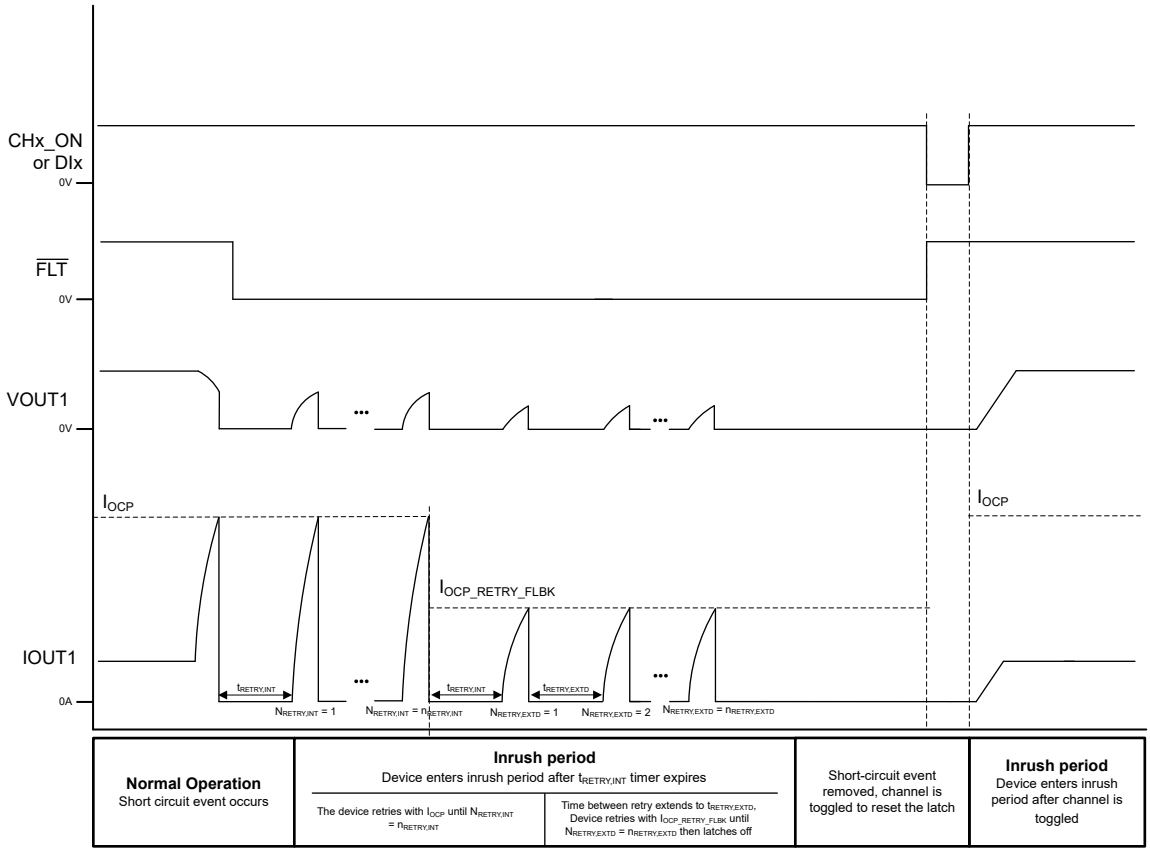


Figure 8-30. Hot Short During Steady State Operation With CAP_CHRG_CHx = 00, Auto-retry (LATCH_CHx = 0), and I_{OCP} > $I_{OCP_RETRY_FLBK}$

8.4.1.1.5.2 Latch-off Behavior - No Capacitive Charging Mode (CAP_CHRG_CHx = 00)

If LATCH_CHx = 1 and CAP_CHRG_CHx = 00 and the I_{OCP} level is exceeded, the device latches-off and does not retry until the CHx_ON bit (version A) is toggled or the DIx pin (version B) is toggled or the LATCH_CHx bit is toggled. Upon resetting the latch either through LATCH_CHx bit toggle, the channel starts up into the inrush period if configured. The figures below shows the latch behavior of a hot short circuit during steady state and a start into a short-circuit event in the inrush period respectively with LATCH_CHx = 1.

Copyright © 2026 Texas Instruments Incorporated

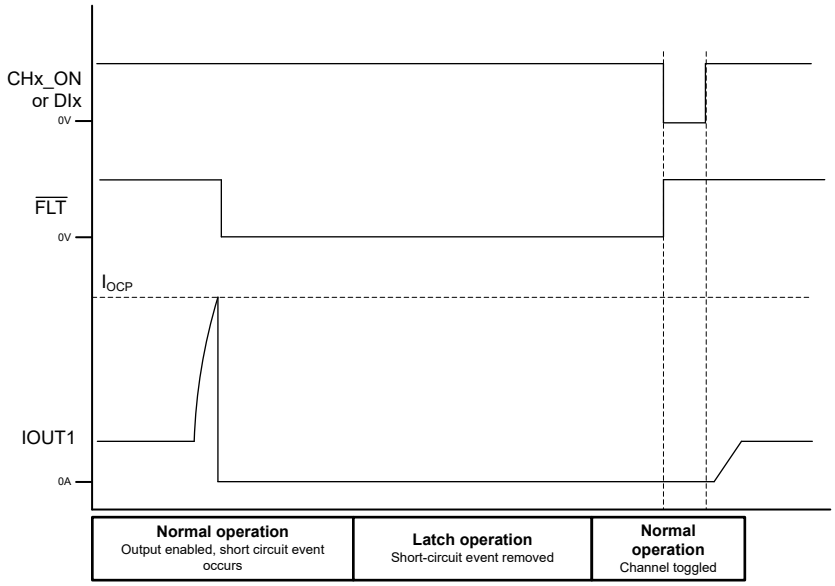


Figure 8-31. Hot Short During Steady State Operation With CAP_CHRG_CHx = 00, Latch-off (LATCH_CHx = 1)

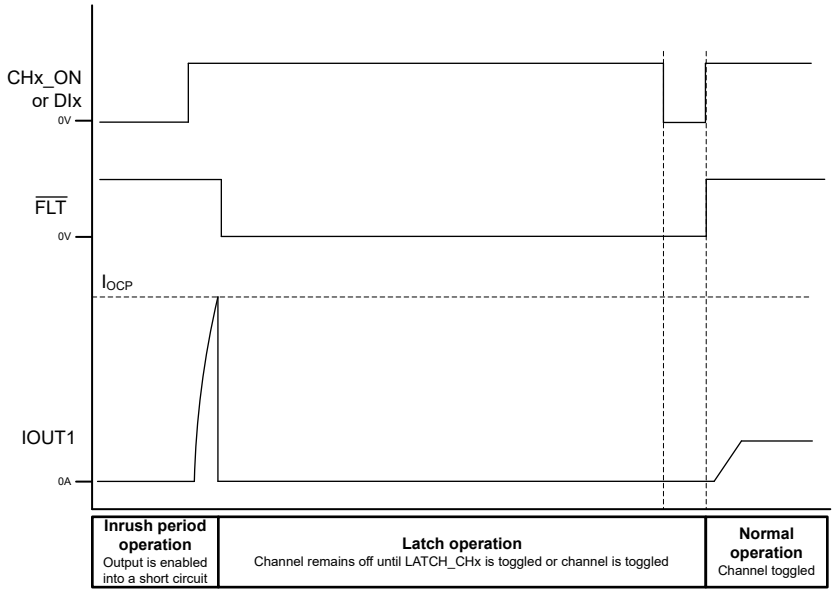


Figure 8-32. Start Into a Short Circuit Event With CAP_CHRG_CHx = 00, Latch-off (LATCH_CHx = 1)

8.4.1.1.5.3 Auto Retry Behavior - Current Limit Regulation Charging Mode (CAP_CHRG_CHx = 10)

If a short-circuit event occurs in steady state operation with CAP_CHRG_CHx = 10 and LATCH_CHx = 0, after the channel turns off and $t_{RETRY,INT}$ expires the device retries into the inrush period with the current limit regulation (I_{CL_REG}) set through the INRUSH_LIMIT_CHx [3:0] bits. The figures below shows a hot short circuit during steady state and a start into a short-circuit event in the inrush period respectively with CAP_CHRG_CHx = 10 and LATCH_CHx = 0.

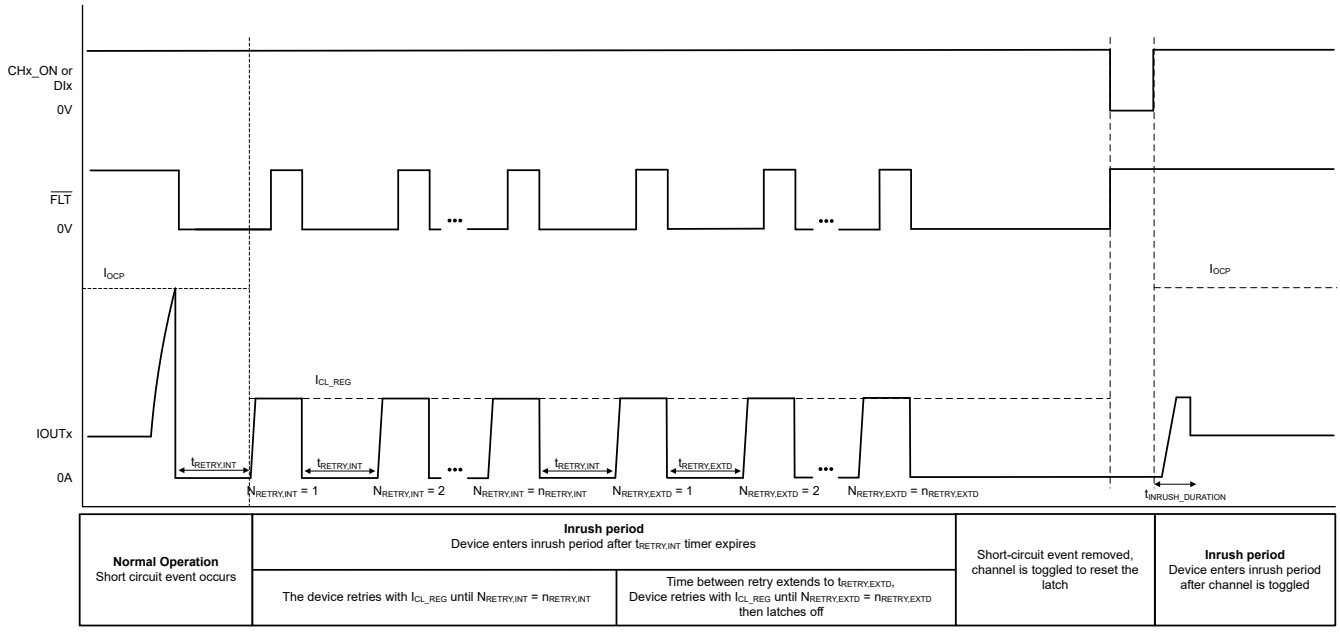


Figure 8-33. Hot Short During Steady State Operation With CAP_CHRG_CHx = 10 and auto-retry (LATCH_CHx = 0)

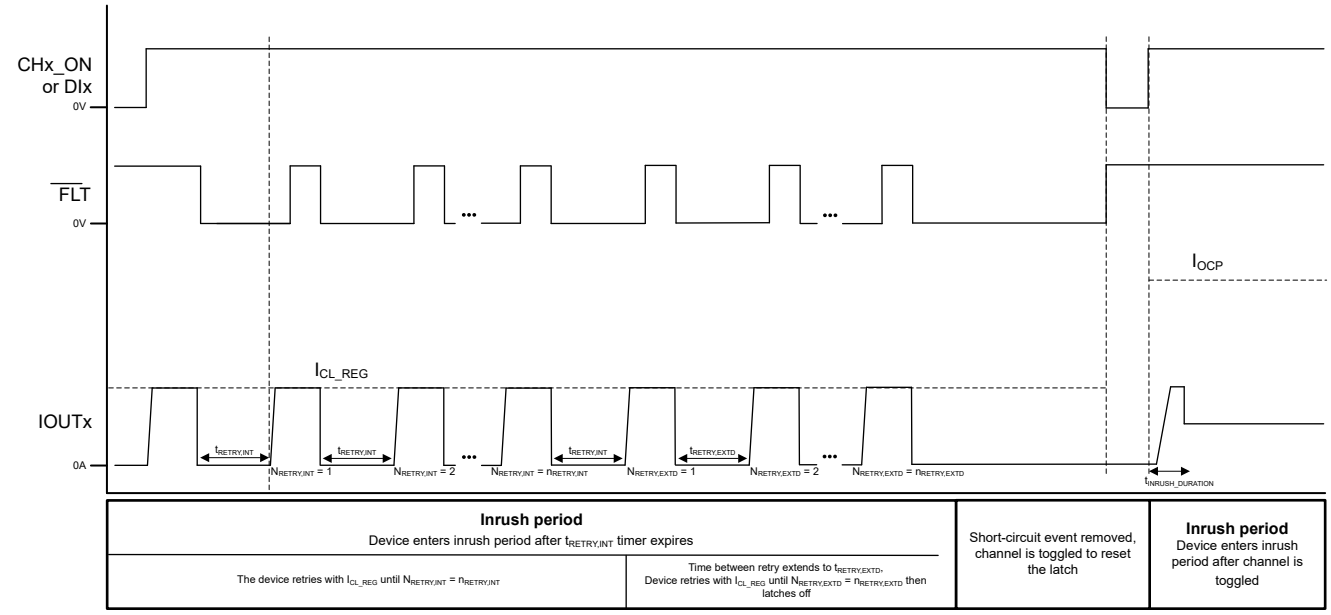


Figure 8-34. Start into a short circuit event with CAP_CHRG_CHx = 10 and auto-rety (LATCH_CHx = 0)

8.4.1.1.5.4 Latch-off Behavior - Current Limit Regulation Capactive Charging Mode (CAP_CHRG_CHx = 10)

If LATCH_CHx = 1 and CAP_CHRG_CHx = 10 and the I_{OCP} level is exceeded, the device latches-off and does not retry until the CHx_ON bit (version A) is toggled or the DIx pin (version B) is toggled or the LATCH_CHx bit is toggled. Upon resetting the latch either through an output toggle or through the LATCH_CHx bit toggle, the channel starts up into the inrush period if configured. The figures below shows a hot short circuit during steady state and a start into a short-circuit event in the inrush period respectively with CAP_CHRG_CHx = 10 and LATCH_CHx = 1.

Copyright © 2026 Texas Instruments Incorporated

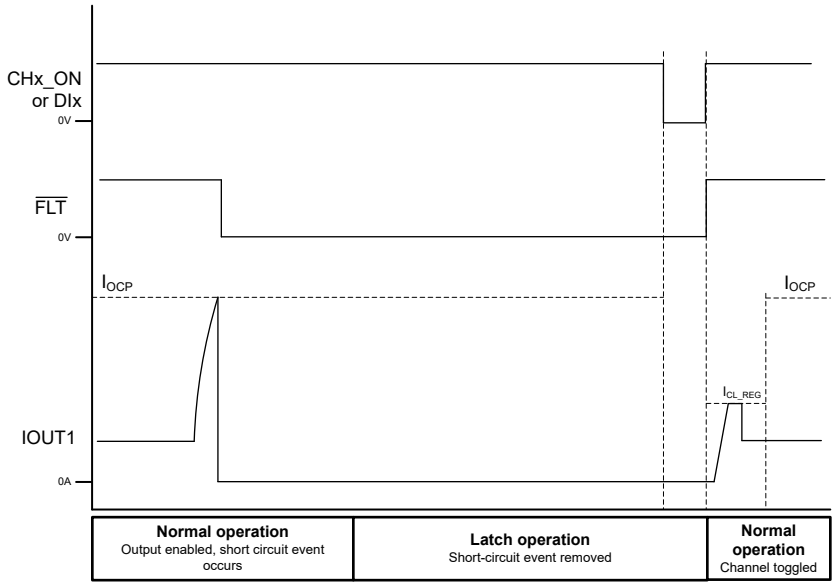


Figure 8-35. Hot Short During Steady State Operation With CAP_CHRG_CHx = 10, Latch-off (LATCH_CHx = 1)

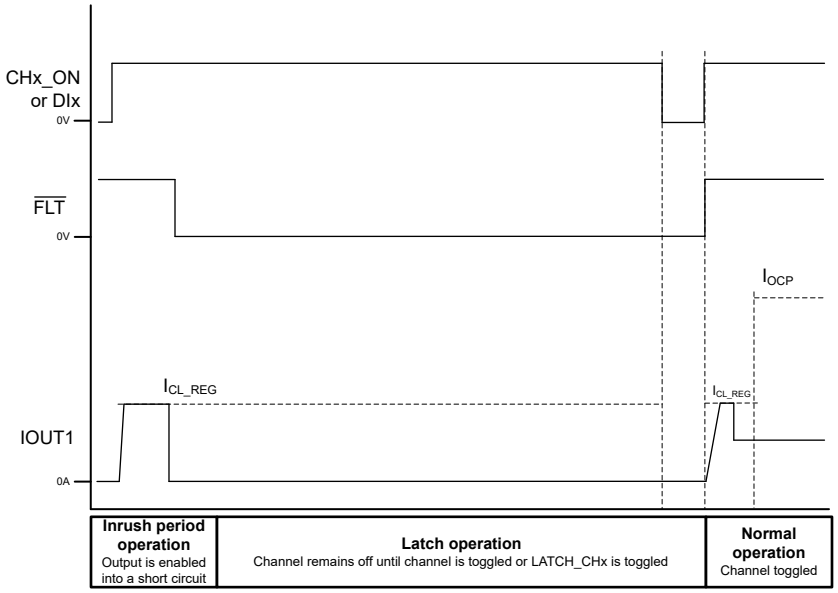


Figure 8-36. Start Into a Short Circuit Event With CAP_CHRG_CHx = 10, Latch-off (LATCH_CHx = 1)

8.4.1.2 Thermal Shutdown

The device includes a temperature sensor on each power FET and within the controller portion of the device to monitor the temperature of each FET ($T_{J,FET}$) and the temperature of the controller ($T_{J,CONTROLLER}$). There are two cases that the device considers to be a thermal shutdown fault:

- **Relative Thermal Shutdown (T_{REL}):** $T_{J,FET} - T_{J,CONTROLLER} > T_{REL}$
- **Absolute Thermal Shutdown (T_{ABS}):** $T_{J,FET} > T_{ABS}$

If either the above faults occur, the relevant switch will be turned off. Each channel is turned off based on the measurement of the temperature sensor for that channel. As result, if the thermal fault is detected on only one channel, the other channel continues operation.

Copyright © 2026 Texas Instruments Incorporated

8.4.1.2.1 Relative Thermal Shutdown (T_{REL})

A relative thermal shutdown event can occur when there is a large peak power event such as a short-to-ground event where the FET temperature ($T_{J,FET}$) quickly rises relative to the controller temperature ($T_{J,CONTROLLER}$). Once the relative temperature ($T_{J,FET} - T_{J,CONTROLLER}$) exceeds T_{REL} the relevant channel is turned off.

8.4.1.2.2 Absolute Thermal Shutdown (T_{ABS})

An absolute thermal shutdown occurs when the FET temperature ($T_{J,FET}$) rises above T_{ABS}. This can occur when a channel is subjected to long durations of overcurrent such as a permanent short use case. Once the FET temperature ($T_{J,FET}$) exceeds T_{ABS} the relevant channel is turned off.

8.4.1.3 Reverse Battery

In the reverse battery condition, the switch automatically enables regardless of the state of the output (set by the SW_STATE register) to prevent excess power dissipation inside the MOSFET body diode. In many applications (for example, resistive loads), the full load current can be present during reverse battery. To activate the automatic switch on feature, the DI pin must have a path to ground from either from the MCU or it must be tied to ground through R_{PROT} if unused.

There are two options for handling reverse battery in the system. The first option is to place a blocking device (FET or diode) in series with the battery supply, blocking all current paths. The second option is to place a blocking diode in parallel with a resistor on the GND node of the high-side switch. This method protects the controller portion of the switch (path 2) by limiting the current through the internal circuits. Additionally in the second option, the automatic switch on feature of the device allows the device to be put into low R_{ON} state to allow current to flow through the switch efficiently and through the load (path 3). The diode used for the second option can be shared amongst multiple high-side switches.

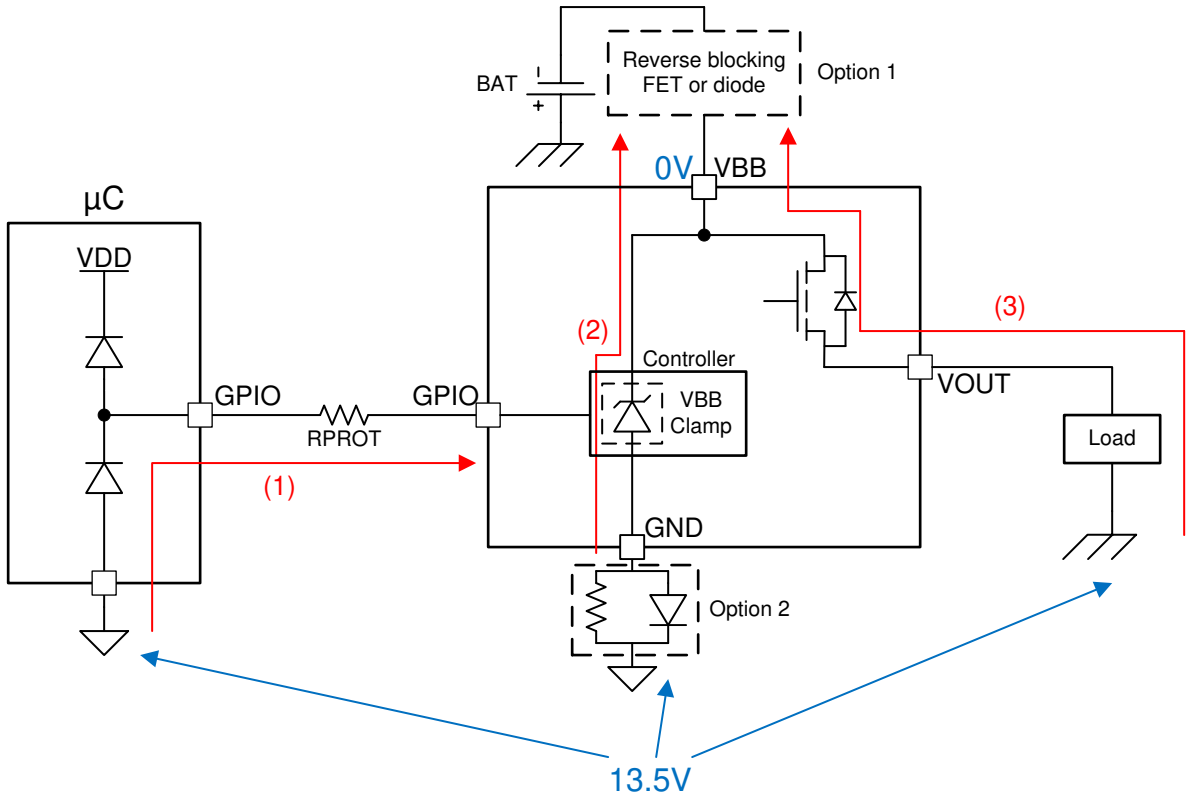


Figure 8-37. Current Path During Reverse Battery

For more information on reverse battery protection, refer to TI's *Reverse Battery Protection for High Side Switches* application note.

Copyright © 2026 Texas Instruments Incorporated

8.4.2 Diagnostic Mechanisms

8.4.2.1 Integrated ADC

The TPS2HCS05-Q1 provides an integrated successive approximation 10-bit ADC which can convert different analog signals to digital signals which can be read out through SPI. The ADC can convert the following analog signals:

- CH1 and CH2 current sense (ISNS1/2)
- CH1 and CH2 MOSFET temperature sense (TSNS1/2)
- VBB voltage sense (VBB_SNS)
- CH1 and CH2 VOUT voltage sense (VSNS1/2)
- CH1 and CH2 MOSFET drain-to-source voltage (VDS) sense (VDS_SNS1/2)

Figure 8-40 provides a functional block diagram of the integrated ADC along with the analog signal inputs to the ADC.

Conversion of any of the analog signals can either be disabled globally through the ADC_CONFIG register or on a per channel basis through CHx_CONFIG registers with the exception of temperature sensing. The temperature sensing cannot be disabled on a per channel basis and can only be disabled globally through the ADC_TSNS_DIS bit.

To help reduce the quiescent current, the device only enables the current sense circuitry when the ADC is converting either of the ISNSx signals and disables it during all other signal conversions. The device also provides a configurable delay which can also help to further reduce the quiescent current of the device by reducing the sampling rate of the ADC. The configurable delay is set by the ADC_ISNS_SAMPLE_CONFIG [1:0] bits in the ADC_CONFIG register.

If I2T protection is enabled (I2T_EN_CHx = 1) and either channel is not in I2T mode (I2T_MOD_CHx = 0), then the device converts each of the analog signals in a round robin sequence with the configurable delay. Figure 8-38 below shows the ADC scheduling if no channel is in I2T mode (I2T_MOD_CHx = 0) and all analog signal conversions are enabled. If I2T protection is disabled then the round robin sequence below also applies.

	ISNS1	ISNS2	TSNS1	TSNS2	VBB_SNS	VSNS1	VSNS2	VDS_SNS 1	VDS_SNS 2	Configurable delay ADC_ISNS_SAMPLE_CONFIG [1:0]
ISNS_EN	1		0							
I2T_MOD_CHx	0									

Figure 8-38. ADC Sequence with I2T_MOD_CHx = 0

If I2T protection is enabled (I2T_EN_CHx = 1) and one or both of the channels are in I2T mode (I2T_MOD_CHx = 1), then the device disables all conversions except for the ISNSx conversions which are used for the internal I2T protection. The device also disables the configurable delay function as well. Figure 8-39 below shows the ADC scheduling if one or both of the channels are in I2T mode (I2T_MOD_CHx = 1).

	ISNS1	ISNS2	ISNS1	ISNS2	...	ISNS1	ISNS2
ISNS_EN	1						
I2T_MOD_CHx	1						

Figure 8-39. ADC Sequence with I2T_MOD_CHx = 1

The reference voltage for the ADC is fixed internally and is specified in the electrical characteristics table through the $V_{ADCREFHI}$ parameter. The ground reference of the ADC connects internally to the GND of the device. For accurate current sense results, the ground connection of the R_{SNS} resistor must be connected to the GND pin of the device. The conversion equation for each of the analog signals can be found in the respective sections below.

Copyright © 2026 Texas Instruments Incorporated

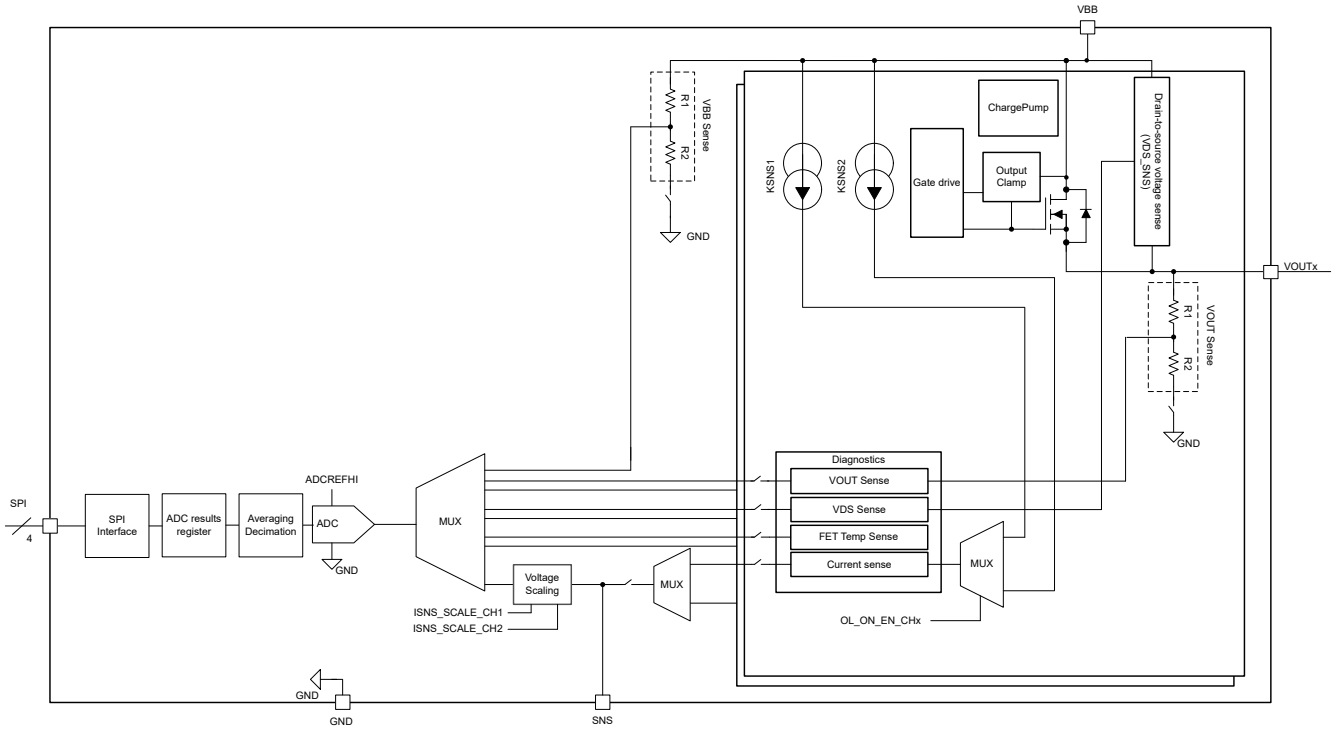


Figure 8-40. Integrated ADC Functional Block Diagram

8.4.2.2 Digital Current Sense Output

The integrated current sense circuit of the device provide a sense current (I_{SNS}) proportional to the load current (I_{OUTx}) of each channel through the SNS pin to an external sense resister (R_{SNS}) to create a voltage. The current sense of each channel is multiplexed internally and is outputted on the SNS pin by the ADC scheduler. The voltage created by the I_{SNS} and R_{SNS} is then sampled by the internal 10-bit ADC where the result of the ADC conversion is stored in ADC_RESULT_CHx_I for each channel. The ISNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register is last read.

To establish an accurate sensing measurement by the internal ADC, the sensing resistor must connect to the IC GND.

The device offers two current sense ratios (K_{SNS1}) and (K_{SNS2}) for each channel which can be set through the OL_ON_EN_CHx bit in the CHx_CONFIG registers. The higher K_{SNS1} ratio (OL_ON_EN_CHx = 0 mode) allows for the channel to accurately measure high output current levels where the lower K_{SNS2} ratio (OL_ON_EN_CHx = 1 mode) enables the channel to accurately measure low output current levels. The K_{SNS1} utilizes the full Mosfet where K_{SNS2} utilizes a small Mosfet with ON resistance, R_{ON_OL}, to provide the lower current sense ratio. To use the K_{SNS2} ratio, the output current level must be below $I_{ENTRY_OL_ON}$ before the OL_ON_EN_CHx bit is set to 1. If the current is not below $I_{ENTRY_OL_ON}$, the K_{SNS2} operation is not entered and the K_{SNS1} operation remains active. If the channel is operating with K_{SNS2} and the output current increases above $I_{EXIT_OL_ON}$, the device automatically transitions out of K_{SNS2} to K_{SNS1} where the OL_ON_EN_CHx bit resets to 0 and the full Mosfet is active. If the current falls below $I_{ENTRY_OL_ON}$ again then the OL_ON_EN_CHx bit must be set back to 1 to transition to K_{SNS2} operation again. The system can manually exit K_{SNS2} operation by writing OL_ON_EN_CHx = 0. When measuring the output current through the integrated ADC in K_{SNS2} operation, the system must continue to monitor the OL_ON_EN_CHx = 1 bit to confirm the device is still in K_{SNS2} operation when the output current measurement is read.

The device also offers a voltage scaling option to amplify the current sense voltage at the ADC input. At low output current levels this helps to allow the current sense voltage to be at higher levels of the integrated ADC. The voltage scaling is set through the ISNS_SCALE_CHx bit. The table below provides the different settings for the ISNS_SCALE_CHx. ISNS_SCALE_CHx = 1 operation is recommended only in OL_ON_EN_CHx = 1 mode.

Copyright © 2026 Texas Instruments Incorporated

It is recommended to only use OL_ON_EN_CHx = 1 mode or ISNS_SCALE_CHx = 1 with I2T disabled (I2T_EN = 0). If OL_ON_EN_CHx = 1 or ISNS_SCALE_CHx = 1 is used with I2T enabled (I2T_EN = 1) this can cause the channel to turn off at unintended lower I2T thresholds.

Table 8-15. ISNS_SCALE_CHx Settings

ISNS_SCALE_CHx	Value
0	x1
1	x8

The ISNS_SCALE_EFF_CHx bit in the ADC_RESULT_CHx_I register, provides an indication if the channel is operating with 1x or 8x voltage scaling so the system knows which voltage scaling factor to apply when converting the current sense measurement.

The ADC conversion equation for current sense for different OL_ON_EN_CHx settings are below:

with OL_ON_EN_CHx = 0,

$$\mathrm{IOUT}\left(\mathrm{A}\right) = \left(\frac{\mathrm{KSNS1} \times \mathrm{V_{ADCREFHI}}}{1023 \times \mathrm{R_{SNS}}}\right) \times \mathrm{ADC_RESULT_CHx_I} \quad (10)$$

with OL_ON_EN_CHx = 1,

$$\mathrm{IOUT}\left(\mathrm{A}\right) = \left(\frac{\mathrm{KSNS2} \times \mathrm{V_{ADCREFHI}}}{1023 \times \mathrm{R_{SNS}} \times \mathrm{ISNS_SCALE_CHx}}\right) \times \mathrm{ADC_RESULT_CHx_I} \quad (11)$$

The current sense function is enabled for each channel by default. The current sense function can be enabled or disabled globally through the ADC_ISNS_DIS bit in the ADC_CONFIG register. When the global ADC_ISNS_DIS bit is 0 the device enables or disable the current sense function on each channel according to the ISNS_DIS_CHx bit in the respective CHx_CONFIG registers.

If I2T protection is used, the current sense function has to be enabled before the I2T protection can be used. The current sense function is only available when the channel is enabled and in the steady state operation. The current sense function is not available in the inrush period.

8.4.2.3 Output Voltage Measurement

The TPS2HCS05-Q1 provides an output voltage measurement per channel through the integrated 10-bit ADC.

The output voltage measurement function is disabled by default. To enable the output voltage sense function it must be globally enabled in the ADC_CONFIG register through the ADC_VSNS_DIS bit. If the global bit is enabled then the device enables the output voltage measurement on each channel according to the VSNS_DIS_CHx bit in the respective CHx_CONFIG register.

The conversion equation for the output voltage measurement is detailed in Equation 12. The ADC measurement result is available in the ADC_RESULT_CHx_V register. The VSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register is the last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the output voltage measurement, if enabled, disables for all the channels and the VSNS_RDY_CHx bit is 0. Once the channels exit the I2T loop (I2T_MOD_CHx = 0), then the output voltage measurement automatically re-enables if previously enabled before the I2T event.

$$\mathrm{VOUT}\left(\mathrm{V}\right) = \left(\frac{17.89 \times \mathrm{V_{ADCREFHI}}}{1023 \times 1.667}\right) \times \mathrm{ADC_RESULT_CHx_V} \quad (12)$$

The output voltage measurement is referenced to the device ground so if there is a ground network used for reverse battery then there can be an offset in the voltage measurement.

Copyright © 2026 Texas Instruments Incorporated

8.4.2.4 MOSFET Temperature Measurement

The TPS2HCS05-Q1 provides a temperature measurement for each of the power MOSFETs through the 10-bit ADC.

The FET temperature sense function is disabled by default. To enable the FET temperature sense function for each channel it must be globally enabled in the ADC_CONFIG register through the ADC_TSNS_DIS bit.

The conversion equation for the FET temperature measurement is detailed in Equation 13. The ADC measurement result is available in the ADC_RESULT_CHx_T register. The TSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register is last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the FET temperature measurement, if enabled, is disabled for all the channels and the TSNS_RDY_CHx bit is 0. Once the channels exit the I2T loop (I2T_MOD_CHx = 0), then the FET temperature measurement is automatically re-enabled if previously enabled before the I2T event.

$$T_{J,FET}(°C) = 381.367 - (0.75157 \times ADC_RESULT_CHx_T) \quad (13)$$

8.4.2.5 Drain-to-Source Voltage (V_{DS}) Measurement

The TPS2HCS05-Q1 provides a drain-to-source voltage (V_{DS}) measurement per channel through the integrated 10-bit ADC.

The V_{DS} voltage measurement function is disabled by default. To enable the V_{DS} voltage sense function it must be globally enabled in the ADC_CONFIG register through the ADC_VDS_DIS bit. If the global bit is enabled, then the device enables the V_{DS} voltage measurement on each channel according to the VDS_SNS_DIS_CHx bit in the respective CHx_CONFIG register.

The conversion equation for the V_{DS} voltage measurement is detailed in Equation 14. The V_{DS} conversion equation is only valid for V_{DS} voltages up to 1.5V. The ADC measurement result is available in the ADC_RESULT_CHx_VDS register. The VDSSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register is last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the V_{DS} voltage measurement, if enabled, is disabled for all the channels and the VDSSNS_RDY_CHx bit is 0. Once the channels exit the I2T loop (I2T_MOD_CHx = 0), then the V_{DS} voltage measurement is automatically re-enabled if previously enabled before the I2T event.

$$VDS(V) = \frac{ADC_RESULT_CHx_VDS - 24}{288.267} \quad (14)$$

8.4.2.6 VBB Voltage Measurement

The TPS2HCS05-Q1 provides a VBB voltage measurement through the 10-bit ADC.

The VBB voltage measurement is disabled by default. The VBB voltage sense function can be enabled through the ADC_VBB_DIS bit in the ADC_CONFIG register.

The conversion equation for the VBB voltage measurement is detailed in Equation 15. The ADC measurement result is available in the ADC_RESULT_VBB register. The VBB_RDY bit is set to 1 if a new ADC conversion result exists since the register is last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the VBB voltage measurement, if enabled, is disabled and the VBB_RDY bit is 0. Once the channel(s) exit the I2T loop (I2T_MOD_CHx = 0), then the VBB voltage measurement is automatically re-enabled if previously enabled before the I2T event.

$$VBB(V) = \left(\frac{18.18 \times V_{ADCREFHI}}{1023 \times 1.667}\right) \times ADC_RESULT_VBB \quad (15)$$

The VBB voltage measurement is referenced to the device ground so if there is a ground network used for reverse battery then there can be an offset in the voltage measurement.

Copyright © 2026 Texas Instruments Incorporated

8.4.2.7 VOUT Short-to-Battery and Open-Load

The TPS2HCS05-Q1 is capable of detecting short-to-battery and open-load events regardless of whether the channel output is turned on or off, however the two conditions use different methods.

8.4.2.7.1 Measurement with Channel Output (FET) Enabled

When the channel output is enabled and the FET is on, the VOUT short-to-battery and open-load conditions can be measured with the current sense feature. In both cases, the load current is measured using the current sense circuit and the ADC (available in the ADC_RESULT_CHx_I registers). The current sense accuracy can be increased at low current levels by changing the current sense ratio from a nominal value of 6500 to a nominal lower value of 1150. This is accomplished by setting the OL_ON_EN_CHx bit to 1 in the individual CHx_CONFIG register. However, the load current must be below $I_{ENTRY_OL_ON}$ for this bit to take effect. In addition, the voltage input to the ADC can be scaled by eight times by setting the ISNS_SCALE_CHx bit in the same CHx_CONFIG register. This enables the ADC to measure the low load current with higher accuracy.

It is recommended to only use OL_ON_EN_CHx = 1 mode or ISNS_SCALE_CHx = 1 with I2T disabled (I2T_EN = 0). If OL_ON_EN_CHx = 1 or ISNS_SCALE_CHx = 1 is used with I2T enabled (I2T_EN = 1) this can cause the channel to turn off at unintended lower I2T thresholds.

8.4.2.7.2 Detection with Channel Output Disabled

The device can detect an open load or a short-to-battery event when the channel output is disabled (FET is off). These are referred to below as off state open load detection and off state short-to-battery detection. When the channel output is disabled, the device can distinguish between an open load event and a short-to-battery event through a defined sequence that are described below. A block diagram for the off-state open load and off-state short-to-battery detection is shown in Figure 8-41.

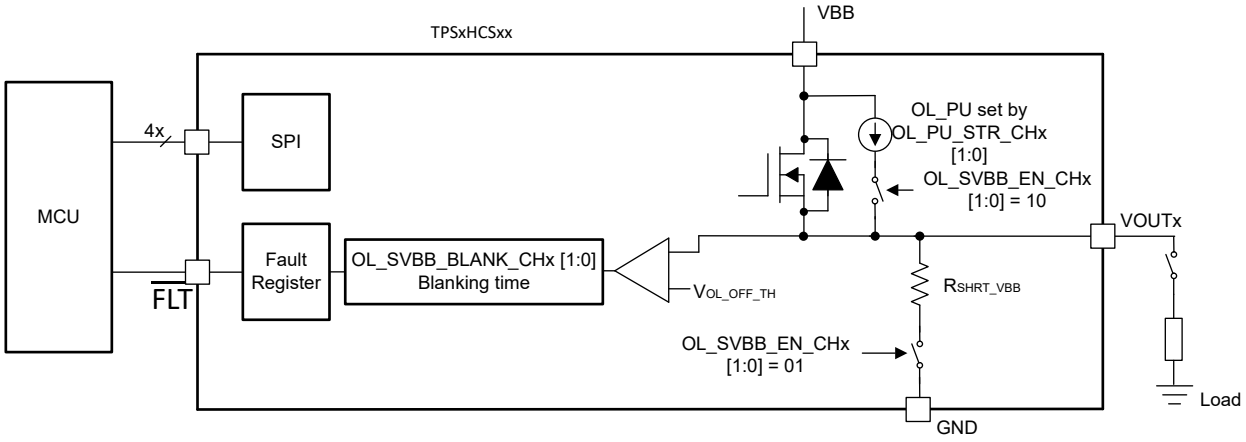


Figure 8-41. Open Load and Short-to-Battery Detection

Note

This figure assumes that the device ground and the load ground are at the same potential. In a real system, there can be a ground shift voltage of the order of 1V.

8.4.2.7.2.1 Off-State Open Load Detection

The device integrates a pull-up current source, OL_PU, for each channel which can be used to pull-up the output to determine if there is an open load or short-to-battery event. The pull-up current source is enabled when OL_SVBB_EN_CHx [1:0] = 10 along with an internal comparator which is used to detect when the output voltage rises above the $V_{OL_OFF_TH}$. The strength of the internal pull-up can be programmed through the OL_PU_STR_CHx bits for each channel in the CHx_CONFIG registers. The device also offers a programmable blanking timer per channel to allow the output to settle before determining if there is an open load or a

Copyright © 2026 Texas Instruments Incorporated

short-to-battery event. The blanking time can be programmed through the OL_SVBB_BLANK_CHx bits in the CHx_CONFIG registers.

When OL_SVBB_EN_CHx [1:0] = 10, the device is only able to report if there is either an open load or a short-to-battery event, it is not able to distinguish between the two with this setting alone. If either an open load or a short-to-battery fault has occurred, then the OL_OFF_CHx bit in the FLT_STAT_CHx register for the corresponding channel is set to 1. The OL_OFF_CHx bit is a read clear bit which clears when the FLT_STAT_CHx register is read and the fault no longer exists, either from the removal of the fault or from the open load circuitry being disabled. To distinguish between an open load and short-to-battery faults, a certain procedure must be followed. This is detailed in Section 8.4.2.7.2.3.

If OL_SVBB_EN_CHx [1:0] = 10 and the output is enabled, the device disables the pull-up current source and internal comparator before turning on the output. If OL_SVBB_EN_CHx [1:0] = 10 and the channel is enabled and then is disabled, the device automatically enables the pull-up source and internal comparator.

8.4.2.7.2.2 Off-State Short-to-Battery Detection

The device also integrates a pull-down resistor for each channel which can be used to help distinguish between an open load and a short-to-battery fault when the channel is disabled. The pull-down resistor is enabled when OL_SVBB_EN_CHx [1:0] = 01 along with an internal comparator which is used to detect when the output voltage rises above the $V_{OL_OFF_TH}$. The pull-down resistor is specified by the R_{SHRT_VBB} parameter in the electrical characteristics. The device offers a programmable blanking timer per channel to allow the output to settle before determining if there is a short-to-battery event. The blanking time can be programmed through the OL_SVBB_BLANK_CHx bits in the CHx_CONFIG registers.

When OL_SVBB_EN_CHx [1:0] = 01, the device is only able to report if there is a short-to-battery event. The device is not able to detect if an open load fault has occurred. If a short-to-battery fault has occurred, then the SHRT_VBB_CHx bit in the FLT_STAT_CHx register for the corresponding channel is set to 1. The SHRT_VBB_CHx bit is a read clear bit which clears when the FLT_STAT_CHx register is read and the fault no longer exists, either from the removal of the fault or from the short-to-battery detection circuitry being disabled. To distinguish between an open load and short-to-battery faults, a certain procedure must be followed. This is detailed in Section 8.4.2.7.2.3.

If OL_SVBB_EN_CHx [1:0] = 01 and the output is enabled, the device disables the pull-down resistor and internal comparator before turning on the output. If OL_SVBB_EN_CHx [1:0] = 01 and the channel is enabled and then is disabled the device automatically enables the pull-down resistor and the internal comparator.

8.4.2.7.2.3 Distinguishing Between Open Load and Short-to-Battery Faults

The TPS2HCS05-Q1 device can distinguish between an open load and a short-to-battery fault through a defined procedure. The figure below highlights the procedure that is recommended to distinguish between an open load and a short-to-battery fault.

When reading the OL_OFF_CHx bits and SHRT_VBB_CHx bits to determine if there is an open load fault or a short-to-battery fault, three read command must be used to determine which fault has occurred. The first read command is to set which register to read, the second read command is to see if a fault has occurred and a third read command is to see if the fault has persisted. After these three successive reads, then the determination of the fault can be done.

Copyright © 2026 Texas Instruments Incorporated

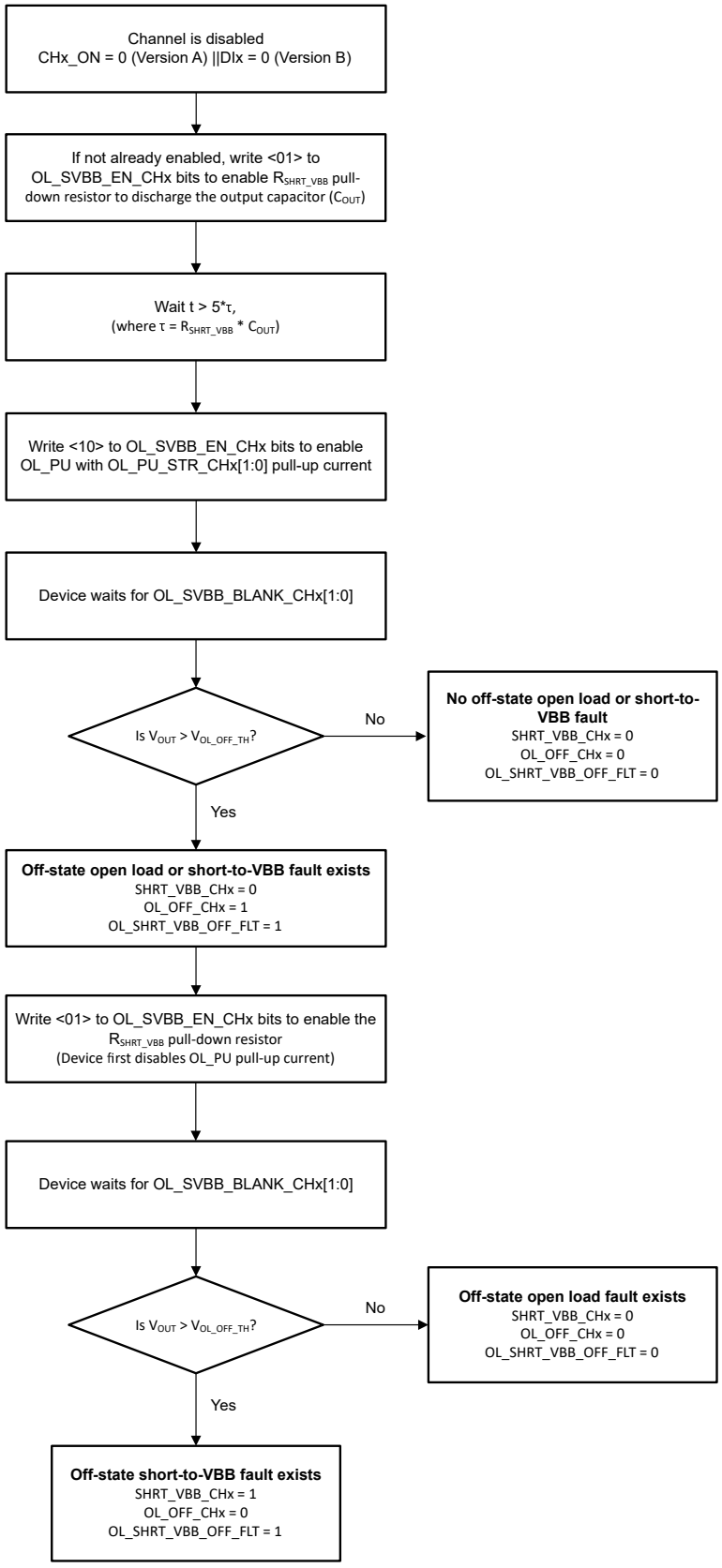


Figure 8-42. Logic Flow Chart to Distinguish Between Open Load and Short-to-Battery Faults

Copyright © 2026 Texas Instruments Incorporated

8.4.3 EEPROM Overview

TPS2HCS05-Q1 provides user programmable Electrically Erasable Programmable Read-Only Memory (EEPROM) for some configuration registers and some customer defined programmable registers. This enables the user to reprogram the default values for these registers. Table 8-16 shows which registers can be programmed through the EEPROM programming procedure.

8.4.3.1 EEPROM Programming Procedure

The default values for the user programmable registers can be reprogrammed through the below procedure. The following conditions need to be met to re-program the EEPROM correctly.

- VBB voltage ≥ 6V, referenced to device GND
- VDD voltage > VDD_UVLO, referenced to device GND

Figure 8-43 shows the procedure of how to re-program the default values. Note, TSNS_CAL_RESULT_CH1 and TSNS_CAL_RESULT_CH2 registers can be overwritten. Be careful not to write to these registers and reprogram the values if these registers are used for the TSNS measurement.

8.4.3.2 Customer Defined Programmable Registers

TPS2HCS05-Q1 provides six customer defined programmable registers which can be re-programmed by the user. These registers are read/write accessible.

Table 8-16. Register Overview

Offset	Register Name	EEPROM User Programmable	Reset Values
00h	DEV_ID	N	see register description
01h	SLEEP	N	see register description
02h	LPM	N	see register description
03h	GLOBAL_FAULT_TYPE	N	see register description
04h	FAULT_MASK	Y	initial reset value: 0xFF80
05h	RESERVED	N	see register description
06h	SW_STATE	N	see register description
07h	RESERVED	N	see register description
08h	DEV_CONFIG	Y	initial reset value: 0x7800
09h	ADC_CONFIG	N	see register description
0Ah	ADC_RESULT_VBB	N	see register description
0Bh	RESERVED	N	see register description
0Ch	FLT_STAT_CH1	N	see register description
0Dh	PWM_CH1	N	see register description
0Eh	ILIM_CONFIG_CH1	Y	initial reset value: 0x0000
0Fh	CH1_CONFIG	Y	initial reset value: 0xC000
10h	ADC_RESULT_CH1_I	N	see register description
11h	ADC_RESULT_CH1_T	N	see register description
12h	ADC_RESULT_CH1_V	N	see register description
13h	ADC_RESULT_CH1_VDS	N	see register description
14h	I2T_CONFIG_CH1	Y	initial reset value: 0x2000
15h	FLT_STAT_CH2	N	see register description
16h	PWM_CH2	N	see register description
17h	ILIM_CONFIG_CH2	Y	initial reset value: 0x0000
18h	CH2_CONFIG	Y	initial reset value: 0xC000
19h	ADC_RESULT_CH2_I	N	see register description
1Ah	ADC_RESULT_CH2_T	N	see register description
1Bh	ADC_RESULT_CH2_V	N	see register description

Copyright © 2026 Texas Instruments Incorporated

Table 8-16. Register Overview (continued)

Offset	Register Name	EEPROM User Programmable	Reset Values
1Ch	ADC_RESULT_CH2_VDS	N	see register description
1Dh	I2T_CONFIG_CH2	Y	initial reset value: 0x2000
50h	TSNS_CAL_RESULT_CH1	Y	0xXXXX, programmed at production
51h	TSNS_CAL_RESULT_CH2	Y	0xXXXX, programmed at production
52h	CUST_REG_52	Y	0x0000
53h	CUST_REG_53	Y	0x0000
54h	CUST_REG_54	Y	0x0000
55h	CUST_REG_55	Y	0x0000
56h	CUST_REG_56	Y	0x0000
57h	CUST_REG_57	Y	0x0000
3Fh	EEPROM_PROG	Y	see register description

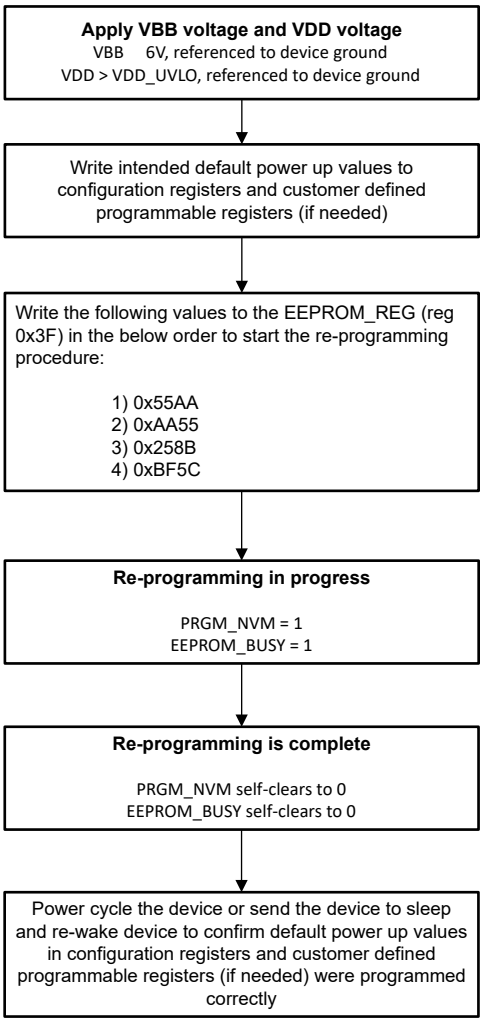


Figure 8-43. EEPROM re-programming procedure

Copyright © 2026 Texas Instruments Incorporated

9 TPS2HCS05-Q1 Registers

Table 9-1 lists the memory-mapped registers for the TPS2HCS05-Q1 registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. TPS2HCS05-Q1 Registers

Offset	Acronym	Register Name	Section
0h	DEV_ID	Read the device ID from NVM, can not be reconfigured through user EEPROM	Go
1h	SLEEP	Sets to go into SLEEP sate from ACTIVE or STANDBY state	Go
2h	LPM	Sets to go in or out of Low power mode (LPM STATE)	Go
3h	GLOBAL_FAULT_TYPE	Faults for any channel and global faults	Go
4h	FAULT_MASK	Mask the reporting of the faults on the fault pin	Go
6h	SW_STATE	Turn on/off OUTx	Go
8h	DEV_CONFIG	Device Configuration register	Go
9h	ADC_CONFIG	ADC configuration - disable ADC conversions or ADC entirely	Go
Ah	ADC_RESULT_VBB	ADC conversion result VBB	Go
Ch	FLT_STAT_CH1	Status of the channels and channel faults	Go
Dh	PWM_CH1	Set all PWM configurations for channel 1	Go
Eh	ILIM_CONFIG_CH1	Set all current limit configuration for channel 1	Go
Fh	CH1_CONFIG	Configuration register for channel 1	Go
10h	ADC_RESULT_CH1_I	ADC conversion result load current sense CH1	Go
11h	ADC_RESULT_CH1_T	ADC conversion result TJ sense CH1	Go
12h	ADC_RESULT_CH1_V	ADC conversion result VOUT sense CH1	Go
13h	ADC_RESULT_CH1_VDS	ADC conversion result VDS sense CH1	Go
14h	I2T_CONFIG_CH1	Set all I2T configuration bits	Go
15h	FLT_STAT_CH2	Status of the channels and channel faults	Go
16h	PWM_CH2	Set all PWM configurations for channel 2	Go
17h	ILIM_CONFIG_CH2	Set all current limit configuration for channel 2	Go
18h	CH2_CONFIG	Configuration register for channel 2	Go
19h	ADC_RESULT_CH2_I	ADC conversion result load current sense CH2	Go
1Ah	ADC_RESULT_CH2_T	ADC conversion result TJ sense CH2	Go
1Bh	ADC_RESULT_CH2_V	ADC conversion result VOUT sense CH2	Go
1Ch	ADC_RESULT_CH2_VDS	ADC conversion result VDS sense CH2	Go
1Dh	I2T_CONFIG_CH2	Set all I2T configuration bits	Go
3Fh	EEPROM_PROG	Customer EEPROM program control and status register	Go
50h	TSNS_CAL_RESULT_CH1	ADC calibration result for TSNS for CH1	Go
51h	TSNS_CAL_RESULT_CH2	ADC calibration result for TSNS for CH2	Go
52h	CUST_REG_52	Customer defined programmable register	Go
53h	CUST_REG_53	Customer defined programmable register	Go
54h	CUST_REG_54	Customer defined programmable register	Go
55h	CUST_REG_55	Customer defined programmable register	Go
56h	CUST_REG_56	Customer defined programmable register	Go
57h	CUST_REG_57	Customer defined programmable register	Go

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Copyright © 2026 Texas Instruments Incorporated

Table 9-2. TPS2HCS05-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

9.1 DEV_ID Register (Offset = 0h) [Reset = XXXXh]

DEV_ID is shown in Table 9-3.

Return to the Summary Table.

Table 9-3. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEV_ID	R	X	Part Number FF00h = TPS2HCS05A-Q1 FF01h = TPS2HCS05B-Q1

Copyright © 2026 Texas Instruments Incorporated

9.2 SLEEP Register (Offset = 1h) [Reset = FFFEh]

SLEEP is shown in Table 9-4.

Return to the Summary Table.

Table 9-4. SLEEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	7FFFh	Reserved
0	SLEEP	R/W	0h	Set this bit to 1 to send the device to SLEEP state 0h = No change 1h = Sends the device to SLEEP state

Copyright © 2026 Texas Instruments Incorporated

9.3 LPM Register (Offset = 2h) [Reset = FF00h]

LPM is shown in Table 9-5.

Return to the Summary Table.

Table 9-5. LPM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	FFh	Reserved
7-6	MAN_LPM_EXIT_CURR_CH2	R/W	0h	Set the threshold to exit from MANUAL_LPM mode due to load current increase - CH2 Depending on the MANUAL_LPM_MODE setting the thresholds for the exit will be different. If MANUAL_LPM_MODE = 0, the thresholds are: 0b00 = 0.95A 0b01 = 1.2A 0b10 = 0.33A 0b11 = 0.64A If MANUAL_LPM_MODE = 1, the thresholds are: 0h = 3.1A 1h = 4.1A 2h = 1A 3h = 2A
5-4	MAN_LPM_EXIT_CURR_CH1	R/W	0h	Set the threshold to exit from MANUAL_LPM mode due to load current increase - CH1 Depending on the MANUAL_LPM_MODE setting the thresholds for the exit will be different. If MANUAL_LPM_MODE = 0, the thresholds are: 0b00 = 0.95A 0b01 = 1.2A 0b10 = 0.33A 0b11 = 0.64A If MANUAL_LPM_MODE = 1, the thresholds are: 0h = 3.1A 1h = 4.1A 2h = 1A 3h = 2A
3	AUTO_LPM_EXIT_CH2	R/W	0h	This bit forces the device out of AUTO_LPM mode to ACTIVE state and enables CH2 if not already enabled. To re-enable the device to enter AUTO_LPM mode this bit must be set back to 0. 0h = Re-enables device to enter AUTO_LPM mode if all conditions are met 1h = Forces an exit from AUTO_LPM state to ACTIVE state. Enable CH2 if not already enabled
2	AUTO_LPM_EXIT_CH1	R/W	0h	This bit forces the device out of AUTO_LPM mode to ACTIVE state and enables CH1 if not already enabled. To re-enable the device to enter AUTO_LPM mode this bit must be set back to 0. 0h = Re-enables device to enter AUTO_LPM mode if all conditions are met 1h = Forces an exit from AUTO_LPM state to ACTIVE state. Enable CH1 if not already enabled
1	MANUAL_LPM_MODE	R/W	0h	The bit determines if the large or small internal FET should be used for both channels when the device is in MANUAL_LPM mode 0h = Smaller internal FET is used, higher RON, lower exit threshold currents 1h = Larger internal FET is used, lower RON, higher exit threshold currents

Copyright © 2026 Texas Instruments Incorporated

Table 9-5. LPM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MANUAL_LPM_ENTRY	R/W	0h	Setting this bit to 1 puts the device into MANUAL_LPM. Note: Both channels must be off or the current on any enabled channel(s) must be below MAN_LPM_EXIT_CURR_CHx to enter MANUAL_LPM mode. If the device is in MANUAL_LPM state and a 0 is written to the MANUAL_LPM_ENTRY bit the device will look at the contents of AUTO_LPM_EXIT_CHx bits and if any of the bits are set to 1 the device will exit MANUAL_LPM mode and will turn on the channel(s) if not already enabled. If the device exits MANUAL_LPM state to ACTIVE state due to a load current increase > MAN_LPM_EXIT_CURR_CHx, the MANUAL_LPM_ENTRY bit needs to be set 0 and then back to 1 to re-enter MANUAL_LPM state 0h = Sends the device to ACTIVE mode if device is in MANUAL_LPM 1h = Sends the device to MANUAL_LPM mode if all conditions are met

Copyright © 2026 Texas Instruments Incorporated

9.4 GLOBAL_FAULT_TYPE Register (Offset = 3h) [Reset = 0147h]

GLOBAL_FAULT_TYPE is shown in Table 9-6.

Return to the Summary Table.

Table 9-6. GLOBAL_FAULT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	CH2_FLT	R	0h	Fault status of channel 2. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CH2 register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No fault(s) have occurred on CH2 1h = Fault(s) have occurred on CH2
12	CH1_FLT	R	0h	Fault status of channel 1. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CH1 register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No fault(s) have occurred on CH1 1h = Fault(s) have occurred on CH1
11	LPM_STATUS	R	0h	The bit indicates if the device is in either MANUAL_LPM mode or AUTO_LPM mode and is cleared when the device is not in any LPM mode. 0h = Device is not in the AUTO_LPM or MANUAL_LPM state 1h = Device has entered either AUTO_LPM or MANUAL_LPM state
10	CHAN_OCP_I2T_TSD	R	0h	This bit indicates if there is an overcurrent protection or I2T protection or thermal shutdown fault in any one of the channels. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No overcurrent protection, I2T protection, or thermal shutdown fault in any of the channels 1h = Overcurrent protection, I2T protection, or thermal shutdown fault(s) in one or both of the channels
9	OL_SHRT_VBB_OFF_FLT	R	0h	This bit indicates if there is a short to VBB supply in the off-state fault in any one of the channels. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No off-state short to VBB or open load fault in any of the channels 1h = Off-state short to VBB or open load fault(s) in one or both of the channels

Copyright © 2026 Texas Instruments Incorporated

Table 9-6. GLOBAL_FAULT_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	GLOBAL_ERR_WRN	R	1h	This bit indicates if there is a global fault reported in FLT_GLOBAL_TYPE[7:0] bits. The faults that are reported through this bit are LIMPHOME_STATE, POR, SPI_ERR, WD_ERR, VDD_UVLO, VBB_UV_WRN, or VBB_UVLO. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the GLOBAL_FAULT_TYPE register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No global fault has occurred 1h = One of the following event(s) have occurred: LIMPHOME_STATE, POR, SPI_ERR, WD_ERR, VDD_UVLO, VBB_UV_WRN, or VBB_UVLO
7	LIMPHOME_STAT	R/W1C	0h	This bit indicates if the device is in LIMP_HOME state as a result of the LHI pin going high. Write 1 to clear and exit LIMP_HOME state. The LHI pin must be LOW when the bit is set to 1 to exit LIMP_HOME state. 0h = Device is not in LIMP_HOME state 1h = Device is in LIMP_HOME state due to LHI pin going high
6	POR	RC	1h	The bit is indicates if a power on reset (POR) has occurred since the last read This bit is cleared on read, so if read again and the bit is 0, this means that no power-on reset has occurred since the read. 0h = No power on reset (POR) has occured since the last register read 1h = A power-on reset has occurred since the last register read.
5	LPM_STATUS_1	RC	0h	This bit indicates if the device is in either MANUAL_LPM or AUTO_LPM modes. This bit is latched and cleared only when read and the device is not in any LPM mode. Note: If the conditons are not met for MANUAL_LPM entry, this bit will be set to 1 and cleared when read. 0h = Device is not in the AUTO_LPM or MANUAL_LPM state 1h = Device has entered either AUTO_LPM or MANUAL_LPM state
4	SPI_ERR	RC	0h	This bit indicates if there is a SPI communication error either from format, clock or CRC. The fault bit is latched and cleared only after read and the error(s) no longer exist. 0h = No SPI communication error(s) fault have occurred 1h = SPI communication error either from format, clock or CRC has occurred
3	WD_ERR	RC	0h	If WD_EN = 1, this bit indicates if there has not been an acceptable SPI command in the watchdog timeout window. The fault bit is latched and cleared only after read and the error no longer exists 0h = No SPI interface watchdog error 1h = SPI watchdog timeout error has occurred
2	VDD_UVLO	RC	1h	This bit indicates if the VDD supply is below VDD_UVLOF at any time. The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UVLO condition is removed 0h = No VDD_UVLO fault has occurred 1h = VDD_UVLO fault has occurred

Copyright © 2026 Texas Instruments Incorporated

Table 9-6. GLOBAL_FAULT_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VBB_UV_WRN	RC	1h	This bit indicates if the VBB supply is below the $V_{BB_UV_WRN}$ at any time. If VBB is below $V_{BB_UV_WRN}$, the diagnostics in the device are turned off The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UV condition no longer exists 0h = No VBB_UV_WRN fault has occurred 1h = VBB_UV_WRN fault has occurred
0	VBB_UVLO	RC	1h	This bit indicates if the VBB supply is below the V_{BB_UVLOF} at any time. The fault bit is cleared if the GLOBAL_FAULT_TYPE register is read and the UVLO condition is removed 0h = No VBB_UVLO fault has occurred 1h = VBB_UVLO fault has occurred

Copyright © 2026 Texas Instruments Incorporated

9.5 FAULT_MASK Register (Offset = 4h) [Reset = XXXXh]

FAULT_MASK is shown in Table 9-7.

Return to the Summary Table.

Table 9-7. FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	X	Reserved
6	RESERVED	R/W	X	Reserved
5	MASK_SHRT_VBB	R/W	X	This bit determines if the device should mask the signaling of an off-state short-to-battery fault on the FLT pin 0h = Short to VBB fault is signaled on the FLT pin 1h = Short to VBB fault is not signaled (masked from) on the FLT pin
4	MASK_OL_OFF	R/W	X	The bit determines if the device should mask the signaling of an off-state open load fault on the FLT pin 0h = Off-state wire-break fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = Off-state wire-break fault is not signaled (masked from) on the FLT pin
3	RESERVED	R	X	Reserved
2	MASK_SPI_ERR	R/W	X	The bit determines if the device should mask a SPI error (SPI_ERR) on the FLT pin and in the GLOBAL_FAULT_TYPE register 0h = SPI error is signaled on the FLT pin and in the GLOBAL_FAULT_TYPE register 1h = SPI error is not signaled on the FLT pin or in the GLOBAL_FAULT_TYPE register
1	MASK_WD_ERR	R/W	X	The bit determines if the device should mask a SPI watchdog error (WD_ERR) on the FLT pin and in the GLOBAL_FAULT_TYPE register 0h = SPI watchdog error is signaled on the FLT pin and in the GLOBAL_FAULT_TYPE register 1h = SPI watchdog error is not signaled on the FLT pin or in the GLOBAL_FAULT_TYPE register
0	MASK_VBB_UVLO	R/W	X	The bit determines if the device should mask the supply voltage VBB UVLO fault on the FLT pin 0h = VBB_UVLO fault is signaled on the FLT pin 1h = VBB_UVLO fault is not signaled (masked from) on the FLT pin

Copyright © 2026 Texas Instruments Incorporated

9.6 SW_STATE Register (Offset = 6h) [Reset = FFFCh]

SW_STATE is shown in Table 9-8.

Return to the Summary Table.

Table 9-8. SW_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	3FFFh	Reserved
1	CH2_ON	R/W	0h	This bit determines the output state of channel 2 for TPS2HCS05A-Q1 versions. 0h = CH2 Output set to OFF (FET is OFF) 1h = CH2 Output set to ON (FET is ON) Note: This bit has no effect on TPS2HCS05B-Q1. For TPS2HCS05B-Q1, control of channel 2 output is determined only through the DI2 pin.
0	CH1_ON	R/W	0h	This bit determines the output state of channel 1 for TPS2HCS05A-Q1 versions. 0h = CH1 Output set to OFF (FET is OFF) 1h = CH1 Output set to ON (FET is ON) Note: This bit has no effect on TPS2HCS05B-Q1 version. For TPS2HCS05B-Q1, control of channel 1 output is determined only through the DI1 pin

Copyright © 2026 Texas Instruments Incorporated

9.7 DEV_CONFIG Register (Offset = 8h) [Reset = XXXXh]

DEV_CONFIG is shown in Table 9-9.

Return to the Summary Table.

Table 9-9. DEV_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CRC_EN	R/W	X	Set this bit to 1 to enable CRC check of SPI command frame. 0h = No CRC check of SPI command frame 1h = CRC check of SPI command frame enabled
14-13	RESERVED	R/W	X	Reserved
12-11	RESERVED	R/W	X	Reserved
10-9	CH2_LH_IN	R/W	X	These bits determine how the channel 2 output should respond in LIMP_HOME state for the TPS2HCS05A-Q1 versions. Note: These bits have no effect on TPS2HCS05B-Q1. There is no LIMP_HOME state for TPS2HCS05B-Q1. If DI_OUT_DIS_FN = 0, the values are: 0h = DI pin controls the output when in LIMP_HOME state 1h = Keeps the same output state from CH2_ON bit when entering LIMP_HOME state 2h = Output will be OFF in LIMP_HOME mode 3h = Output will be ON in LIMP_HOME mode If DI_OUT_DIS_FN = 1, the values are: 0h = Output will be OFF in LIMP_HOME mode 1h = Keeps the same output state from CH2_ON bit when entering LIMP_HOME state 2h = Output will be OFF in LIMP_HOME mode 3h = Output will be ON in LIMP_HOME mode
8-7	CH1_LH_IN	R/W	X	These bits determine how the channel 1 output should respond in LIMP_HOME state for the TPS2HCS05A-Q1 versions. Note: These bits have no effect on TPS2HCS05B-Q1. There is no LIMP_HOME state for TPS2HCS05B-Q1. If DI_OUT_DIS_FN = 0, the values are: 0h = DI pin controls the output when in LIMP_HOME state 1h = Keeps the same output state from CH1_ON bit when entering LIMP_HOME state 2h = Output will be OFF in LIMP_HOME mode 3h = Output will be ON in LIMP_HOME mode If DI_OUT_DIS_FN = 1, the values are: 0h = Output will be OFF in LIMP_HOME mode 1h = Keeps the same output state from CH1_ON bit when entering LIMP_HOME state 2h = Output will be OFF in LIMP_HOME mode 3h = Output will be ON in LIMP_HOME mode
6	DI_OUT_DIS_FN	R/W	X	Set this bit to 1 to use the DI / OUT_DIS pin (pin 5) as a fast output disable 0h = The LH state is determined by a DI_OUT_DIS pin (DI pin function) 1h = Outputs are disabled when DI_OUT_DIS pin is set HI (OUT_DIS function)
5	AUTO_LPM_ENTRY	R/W	X	This bit determines if the device should enter AUTO_LPM mode if all the conditions are met to enter AUTO_LPM mode. 0h = Entry into AUTO_LPM mode is disabled 1h = Entry into AUTO_LPM mode is enabled and the device enters if all the conditions are met to enter

Copyright © 2026 Texas Instruments Incorporated

Table 9-9. DEV_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	R/W	0h	This bit should always be programmed and set to 0 If this bit is set to 1 and AUTO_LPM_ENTRY = 1, the device will be able to enter AUTO_LPM even if VSNS_DIS_CH2=0 and/or VDSSNS_DIS_CH2=0.
3	WD_EN	R/W	X	The bit determines if the SPI watchdog function is enabled. If enabled, the watchdog timout triggers if there is not a valid SPI command in the watchdog timeout window 0h = Watchdog is disabled 1h = Watchdog function is enabled
2-1	WD_TO	R/W	X	This bit determines the timeout period for the SPI watchdog function (if enabled). The watchdog timeout triggers if there is not a valid SPI command in the watchdog timeout window. 0h = Watchdog timeout period is 400µs 1h = Watchdog timeout period is 400ms 2h = Watchdog timeout period is 800ms 3h = Watchdog timeout period is 1200ms
0	FLT_LTCH_DIS	R/W	X	This bit determines if the fault bits in FAULT_GLOBAL_TYPE [13:8] should latch if a fault occurs. 0h = Fault bits [13:8] in FAULT_GLOBAL_TYPE register latched and cleared only on read of the associated register 1h = Fault bits [13:8] in FAULT_GLOBAL_TYPE register are not latched and are cleared when the fault no longer exists Note: See each fault bit description for more details on how to clear the individual fault bits when FLT_LTCH_DIS = 0. LPM_STATUS[0] is read only.

Copyright © 2026 Texas Instruments Incorporated

9.8 ADC_CONFIG Register (Offset = 9h) [Reset = FF3Ah]

ADC_CONFIG is shown in Table 9-10.

Return to the Summary Table.

Table 9-10. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	FFh	Reserved
7-6	ADC_ISNS_SAMPLE_CONFIG	R/W	0h	These bits determine the sampling and conversion rate for the current sense (ISNS). The slower the sampling and conversion rate the lower the IQ consumption. 0h = Current sense and ADC conversion at max rate 1h = Current sense and ADC conversion at max rate 2h = Current sense and ADC conversion at one half max rate 3h = Current sense and ADC conversion at one quarter max rate
5	ADC_VDS_DIS	R/W	1h	This bit determines if the VDS sense funciton should be disabled for all channels. If disabled, this excludes VDS conversion for all channels in the ADC conversion sequence. Note: The VDS sense function can also be enabled or disabled per channel through the VDS_SNS_DIS_CHx bit in the DIAG_CONFIG_CHx register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = VDS_SNS ADC function is enabled 1h = VDS SNS ADC functionality is disabled for all channels, VDS_SNS ADC conversion is excluded in the ADC conversion sequence for all channels
4	ADC_VSNS_DIS	R/W	1h	This bit determines if the VOUT sense (VSNS) funciton should be disabled for all channels. If disabled, this excludes the VOUT conversion for all channels in the ADC conversion sequence. Note: The VSNS function can also be enabled or disabled per channel through the VSNS_DIS_CHx bit in the DIAG_CONFIG_CHx register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = VSNS ADC function is enabled 1h = VSNS ADC functionality is disabled for all channels, VSNS ADC conversion is excluded in the ADC conversion sequence for all channels
3	ADC_TSNS_DIS	R/W	1h	This bit determines if the temperature sense function is disabled for all channels. If disabled, this excludes the temperature sense conversion for all channels in the ADC conversion sequence. Note: The temperature sense function can only be enabled or disabled globally 0h = TSNS ADC function is enabled 1h = TSNS ADC functionality is disabled for all channels, TSNS ADC conversion is excluded in the ADC conversion sequence for all channels
2	ADC_ISNS_DIS	R/W	0h	This bit determines if the current sense (ISNS) function is disabled for all channels. If disabled, this excludes the ISNS conversion for all channels in the ADC conversion sequence Note: The ISNS function can also be enabled or disabled per channel through the ISNS_DIS_CHx in DIAG_CONFIG_CHx register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = ISNS ADC function is enabled 1h = ISNS ADC functionality is disabled for all channels, ISNS ADC conversion is excluded in the ADC conversion sequence for all channels
1	ADC_VBB_DIS	R/W	1h	This bit determines if the VBB_SNS function is disabled. If disabled, this excludes supply voltage VBB conversion in the ADC conversion sequence. 0h = VBB_SNS ADC function is enabled, VBB_SNS ADC conversion is included in the ADC conversion sequence 1h = VBB_SNS ADC function is disabled, VBB_SNS ADC conversion is excluded in the ADC conversion sequence

Copyright © 2026 Texas Instruments Incorporated

Table 9-10. ADC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADC_DIS	R/W	0h	This bit determines if the ADC function should be disabled. If disabled, no VDS_SNS, VSNS, TSNS, or ISNS is possible. The ADC is enabled by default. 0h = ADC function enabled 1h = All ADC functions disabled

Copyright © 2026 Texas Instruments Incorporated

9.9 ADC_RESULT_VBB Register (Offset = Ah) [Reset = F800h]

ADC_RESULT_VBB is shown in Table 9-11.

Return to the Summary Table.

Table 9-11. ADC_RESULT_VBB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VBB_RDY	R	0h	This bit indicates if a new ADC result for VBB voltage conversion is available since the last read 0h = VBB ADC value not updated 1h = New VBB ADC value ready since last read
9-0	ADC_RESULT_VBB	R	0h	10-bit ADC result from the conversion of the VBB voltage

Copyright © 2026 Texas Instruments Incorporated

9.10 FLT_STAT_CH1 Register (Offset = Ch) [Reset = E000h]

FLT_STAT_CH1 is shown in Table 9-12.

Return to the Summary Table.

Table 9-12. FLT_STAT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	I2T_MOD_CH1	R	0h	This bit indicates if channel 1 in the I2T loop and is accumulating. When channel 1 is not in the I2T loop the value will be 0 0h = I2T is off or the channel is not in the I2T loop 1h = Channel is in the I2T loop and is accumulating
11	LATCH_STAT_CH1	RC	0h	This bit indicates if channel 1 has been latch off due to an overcurrent protection or thermal shutdown fault. The bit clears when the channel is toggled off and back on. Note: This bit does not signal when a shutdown occurs due to I2T 0h = This channel is not latched off 1h = This channel is currently latched off
10	FLT_CH1	R	0h	This bit indicates if channel 1 is currently in an auto retry wait time period, latched off, or in I2T cooldown 0h = This channel is currently not in auto retry wait time, latched off state, or I2T cooldown 1h = This channel is currently in auto retry wait time, latched off state, or I2T cooldown
9	SW_STATE_STAT_CH1	R	0h	This bit indicates the current state of channel 1 no matter which mode the device is in as long as SPI is functioning 0h = CH1 is OFF 1h = CH1 is ON
8	VOUT_ERR_CH1	R	0h	This bit indicates if the drain-to-source voltage (V_{DS}) of channel 1 < $V_{DS_LT_2V}$ after the channel is enabled and is out of the inrush period (if configured) for t > t_{VDS_DEGL}. 0h = The VDS voltage is correct (< 2V) when this channel is enabled 1h = The VDS voltage is incorrect (> 2V) when this channel is supposed to be enabled
7	I2T_FLT_CH1	RC	0h	This bit indicates if an I2T fault has occured on channel 1. I2T_EN must be set to 1 in order for this bit indicate an I2T fault. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists Note: This bit does not indicate an overcurrent protection or thermal shutdown fault 0h = no I2T fault has occurred or I2T is not enabled 1h = I2T fault has occurred on this channel
6	LPM_WAKE_CH1	R	0h	This bit indicates if channel 1 was the cause for the device to come out of AUTO_LPM or MANUAL_LPM regardless of the cause (load step, short-circuit) 0h = The device was not in LPM or this channel was not the cause the device came out of AUTO_LPM or MANUAL_LPM mode 1h = This channel was the reason the device came out of AUTO_LPM or MANUAL_LPM
5	THERMAL_SD_CH1	RC	0h	This bit indicates if thermal shutdown fault has occurred on channel 1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and the retry timer has expired and the channel temperature has fallen below the thermal shutdown hysteresis threshold 0h = No thermal shutdown fault has occurred on this channel 1h = A thermal shutdown fault has occurred on this channel

Copyright © 2026 Texas Instruments Incorporated

Table 9-12. FLT_STAT_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ILIMIT_CH1	RC	0h	This bit indicates if an overcurrent protection fault has occurred on channel 1 The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = No overcurrent protection fault has occurred on this channel 1h = Overcurrent protection fault has occurred on this channel
3	SHRT_VBB_CH1	RC	0h	This bit indicates if there was a short to VBB in the off-state on channel 1. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists Note: SVBB_EN_CH1 must be enabled for this bit to signal short to VBB in the off state. 0h = No Short to VBB fault in off-state has occurred on this channel or short to VBB in off-state is not enabled 1h = Short to VBB fault in the off-state has occurred on this channel
2	OL_OFF_CH1	R	0h	This bit indicates if there is an open load in the off-state on channel 1. The output of channel 1 is pulled up by the OL_PULLUP_STR setting. Note: OL_OFF_EN_CH1 must be enabled for this bit to signal an open load in the off-state. 0h = No off-state open load fault has occurred on this channel or off-state open load detection in off-state is not enabled 1h = Off-state open load fault has occurred on this channel
1	RESERVED	R	0h	Reserved
0	THERMAL_WRN_CH1	RC	0h	This bit indicates if the channel 1 FET temperature is above the overtemperature warning threshold. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = FET temperature is below the over-temperature warning threshold in this channel 1h = FET temperature is above the over-temperature warning threshold in this channel

Copyright © 2026 Texas Instruments Incorporated

9.11 PWM_CH1 Register (Offset = Dh) [Reset = F000h]

PWM_CH1 is shown in Table 9-13.

Return to the Summary Table.

Table 9-13. PWM_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-9	PWM_FREQ_CH1	R/W	0h	Set the PWM frequency 0h = 0.86Hz 1h = 3.5Hz 2h = 14Hz 3h = 112Hz 4h = 224Hz 5h = 448Hz 6h = 895Hz 7h = 1765Hz
8-1	PWM_DTY_CH1	R/W	0h	These bits are used to set the duty cycle for the PWM operation for channel 1. Each bit is ~0.39% duty cycle, linearly up to 100% duty cycle
0	PWM_EN_CH1	R/W	0h	This bit enables PWM operation of channel 1. Note: The duty cycle of PWM > 200us. If fault will occur in FLT_STAT_CH1 register. PWM mode can only be enabled if CAP_CHRG_CH1[1:0] = 0 0h = Output follows CH1_ON setting 1h = Output is PWM according to duty cycle and frequency set if CH1_ON is high

Copyright © 2026 Texas Instruments Incorporated

9.12 ILIM_CONFIG_CH1 Register (Offset = Eh) [Reset = XXXXh]

ILIM_CONFIG_CH1 is shown in Table 9-14.

Return to the Summary Table.

Table 9-14. ILIM_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	X	Reserved
13-12	CAP_CHRG_CH1	R/W	X	These bits set the capacitive charging mode during the inrush period after turn on. When CAP_CHRG_CH1 = 00, these are bits are programmed as the overcurrent protection threshold during the INRUSH_DURATION_CH1 period. The channel will immediately turn off if the threshold is reached. When CAP_CHRG_CH1 = 10, these bits are programmed as the current limit regulation threshold. The channel will turn on into the current limit and will continue to regulate the current until the output is fully charged or there is a thermal shutdown event. Note: PWM and I2T is not enabled during the INRUSH_DURATION. 0h = No cap charging mode, IOCP value set by INRUSH_LIMIT_CH1 bits 1h = Not supported 2h = Current limit regulation mode, value set by INRUSH_LIMIT_CH1 bits 3h = Not supported
11	I2T_EN_CH1	R/W	X	Enables the I2T functionality for channel 1. I2T can be enabled before the channel is enabled or while it is enabled, but the I2T calculation will only start after the inrush period ends. 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH1	R/W	X	These bits determine the inrush period duration during which the INRUSH_LIMIT_CH1 level applies. 0h = 0ms 1h = 2ms 2h = 4ms 3h = 6ms 4h = 10ms 5h = 20ms 6h = 50ms 7h = 100ms

Copyright © 2026 Texas Instruments Incorporated

Table 9-14. ILIM_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	INRUSH_LIMIT_CH1	R/W	X	These bits determine the inrush current limit on channel 1 for the different capacitive charging modes set by CAP_CHRG_CH1 bits. Note: If VBB > 19V, the device will limit the overcurrent threshold to 66A if the ILIMIT_SET_CH1 > 66A If no cap charging mode (CAP_CHRG_CH1 = 00) is used, the values are: 0x0 = 14.5A 0x1 = 18.2A 0x2 = 20.5A 0x3 = 24.2A 0x4 = 28.5A 0x5 = 30.6A 0x6 = 33.5A 0x7 = 44.3A 0x8 = 53.4A 0x9 = 66A 0xA = 76.2A Note: 0xB–0xF are not supported by design and shall never be selected. If current regulation mode (CAP_CHRG_CH1 = 10) is used, the values are: 0h = 2A 1h = 2.3A 2h = 2.7A 3h = 3.2A 4h = 3.7A 5h = 4.2A 6h = 4.6A 7h = 6.2A 8h = 7.6A 9h = 9.1A Ah = 10.6A Bh = 12.1A Ch = 13.5A Dh = 15.1A Eh = 16.7A Fh = 18.2A
3-0	ILIMIT_SET_CH1	R/W	X	These bits determine the overcurrent protection (I_{OCP}) threshold for channel 1 in steady state operation after the INRUSH_DURATION period expires. Note: If VBB > 19V, the device will limit the overcurrent threshold to 66A if the ILIMIT_SET_CH1 > 66A 0h = 14.5A 1h = 18.2A 2h = 20.5A 3h = 24.2A 4h = 28.5A 5h = 30.6A 6h = 33.5A 7h = 44.3A 8h = 53.4A 9h = 66A Ah = 76.2A

Copyright © 2026 Texas Instruments Incorporated

9.13 CH1_CONFIG Register (Offset = Fh) [Reset = XXXXh]

CH1_CONFIG is shown in Table 9-15.

Return to the Summary Table.

Table 9-15. CH1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH1	R/W	X	This bit determines if the VOUT VSNS ADC function for channel 1 is enabled. 0h = CH1 VOUT VSNS ADC functionality enabled 1h = CH1 VOUT VSNS ADC functionality is disabled
14	VDS_SNS_DIS_CH1	R/W	X	This bit determines if the VDS_SNS ADC function for channel 1 is enabled. 0h = CH1 VDS_SNS ADC functionality enabled 1h = CH1 VDS_SNS ADC functionality is disabled
13	ISNS_DIS_CH1	R/W	X	This bit determines if the ISNS ADC function for channel 1 is enabled. 0h = CH1 ISNS ADC functionality enabled 1h = CH1 ISNS ADC functionality is disabled
12	OUT_DIS_MASK_CH1	R/W	X	If DI_OUT_DIS_FN = 1, this bit determines if channel 1 should turn off if OUT_DIS = 1 If DI_OUT_DIS_FN = 0, then this bit has no effect 0h = CH1 will turn OFF when OUT_DIS pin is high 1h = CH1 will ignore OUT_DIS pin when high, CH1 will follow CH1_ON in active state or CH1_LH_IN in limp home state
11	RESERVED	R/W	X	Reserved
10	ISNS_SCALE_CH1	R/W	X	This bit determines the voltage scaling of the channel 1 ISNS for the input to the ADC Note: If I2T is enabled (I2T_EN_CH1 = 1) and ISNS_SCALE_CH1 = 1, the 8x voltage scaling will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. If this is not intended then it is recommended to only use the 8x voltage scaling option when in OL_ON_EN_CH1 = 1 mode and with I2T disabled (I2T_EN_CH1 = 0). 0h = ADC input voltage scale equals 1x 1h = ADC input voltage scale equals 8x
9	OL_ON_EN_CH1	R/W	X	This bit determines if channel 1 should enter a mode with a higher RON and a lower KSNS value to more accurately detect lower output current. Note: It is recommended to only use OL_ON_EN_CH1 = 1 mode with I2T disabled (I2T_EN_CH1 = 0). If I2T is enabled (I2T_EN_CH1 = 1) and OL_ON_EN_CH1 = 1, the lower K_{SNS2} will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. Note: The device can only enter this mode if there are no existing faults on the channel and the output current is below $I_{ENTRY_OL_ON}$. 0h = KSNS1 ratio and RON = RON 1h = KSNS2 ratio and RON = RON_OL
8-7	OL_SVBB_BLANK_CH1	R/W	X	These bits determine the blanking time for open load or short to VBB faults in the OFF state for channel 1 0h = Blanking time is 0.4ms 1h = Blanking time is 1.0ms 2h = Blanking time is 2.0ms 3h = Blanking time is 4.0ms
6-5	OL_PU_STR_CH1	R/W	X	These bits determine the pull-up current (I_pu) at the VOUT1 for the off-state open load detection circuitry. 0h = I_pu is 27µA 1h = I_pu is 62µA 2h = I_pu is 128µA 3h = I_pu is 270µA

Copyright © 2026 Texas Instruments Incorporated

Table 9-15. CH1_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	OL_SVBB_EN_CH1	R/W	X	The bits are used to enable open load and short to supply detection in OFF state. Setting to 0x02h Turns on the pull up to see if there is an open load or short to supply in the off state with an output comparator. If detected set to 0x1h to turn on a pull down to see if there is a short to VBB in the off state. 0h = Disabled 1h = Turns-on an output pulldown to differentiate Short to supply from open load. 2h = Turns on a pull-up from VBB supply to output to detect if either an open load or short-to-battery exists. 3h = Output comparator enabled, use external switches and pull-up/pull-down to detect open load or short-to-supply.
2	LATCH_CH1	R/W	X	This bit determines if channel 1 should auto-retry or latch off after an overcurrent or thermal shutdown event has occurred. 0h = Channel 1 will auto retry after tRETRY expires and THYS is reached 1h = Channel 1 latches off until SW_STATE register is written to again
1-0	SLRT_CH1	R/W	X	These bits determine the turn on and turn off slew rates for channel 1. 0h = 0.13V/µs (Rising) and 0.15V/µs (Falling) 1h = 0.22V/µs (Rising) and 0.28V/µs (Falling) 2h = 0.13V/µs (Rising) and 0.3V/µs (Falling) 3h = 0.22V/µs (Rising) and 0.47V/µs (Falling)

Copyright © 2026 Texas Instruments Incorporated

9.14 ADC_RESULT_CH1_I Register (Offset = 10h) [Reset = E000h]

ADC_RESULT_CH1_I is shown in Table 9-16.

Return to the Summary Table.

Table 9-16. ADC_RESULT_CH1_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	ISNS_CH1_ONOFF_STAT	R	0h	The bit is set to 1 if the ADC conversion of ISNS is done while the channel is ON 0h = ISNS read is done while the status of the CH1 FET is OFF 1h = ISNS read is done while the status of the CH1 FET is ON
11	ISNS_SCALE_EFF_CH1	R	0h	The bit indicates the voltage scaling factor used for the conversion 0h = 1x ISNS1 voltage scaling 1h = 8x ISNS1 voltage scaling
10	ISNS_RDY_CH1	R	0h	Making sure the ADC conversion is new from the last time this was read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_I	R	0h	ADC result (10-bits) from the conversion of the current in CH1

Copyright © 2026 Texas Instruments Incorporated

9.15 ADC_RESULT_CH1_T Register (Offset = 11h) [Reset = F800h]

ADC_RESULT_CH1_T is shown in Table 9-17.

Return to the Summary Table.

Table 9-17. ADC_RESULT_CH1_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 TSNS conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_T	R	0h	10-bit ADC result from the conversion of channel 1 FET temperature (TSNS)

Copyright © 2026 Texas Instruments Incorporated

9.16 ADC_RESULT_CH1_V Register (Offset = 12h) [Reset = F800h]

ADC_RESULT_CH1_V is shown in Table 9-18.

Return to the Summary Table.

Table 9-18. ADC_RESULT_CH1_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 VOUT voltage (VSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_V	R	0h	10-bit ADC result from the conversion of channel 1 VOUT voltage (VSNS)

Copyright © 2026 Texas Instruments Incorporated

9.17 ADC_RESULT_CH1_VDS Register (Offset = 13h) [Reset = F800h]

ADC_RESULT_CH1_VDS is shown in Table 9-19.

Return to the Summary Table.

Table 9-19. ADC_RESULT_CH1_VDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VDSSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 VDS voltage (VDSSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_VDS	R	0h	10-bit ADC result from the conversion of channel 1 VDS voltage (VDSSNS)

Copyright © 2026 Texas Instruments Incorporated

9.18 I2T_CONFIG_CH1 Register (Offset = 14h) [Reset = XXXXh]

I2T_CONFIG_CH1 is shown in Table 9-20.

Return to the Summary Table.

Table 9-20. I2T_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH1	R/W	X	These bits set the cool down time (or time to retry) after an I2T shutdown for Channel 1. Note: If setting 0x0 is used, the channel will remain off after an I2T shutdown with no retry. To retry in this setting, change the bits to 0.8s, 2.0s, or 4.0s options to allow the device to retry after an I2T shutdown. 0h = channel off 1h = 0.8s 2h = 2.0s 3h = 4.0s
13	DCR_CH1	R/W	X	Sets the mode of I2T operation for channel 1. If DCR = 0: the device accumulates according to I2T_TRIP = I_{OUT1}^2 x t and decrements according to I2T_TRIP = (I_{OUT1}^2 - k x (NOM_CUR_CH1)^2) x t If DCR = 1: the device accumulates and decrements according to I2T_TRIP = (I_{OUT1}^2 - NOM_CUR_CH1^2) x t. 0h = I2t Mode DCR0 1h = I2t Mode DCR1
12-11	ACC_DCR0_CH1	R/W	X	Decrement factor of accumulated energy when DCR_CH1 = 0 for the following equation: I2T_TRIP = (I_{OUT1}^2 - k x (NOM_CUR_CH1)^2) x t 0h = Decrement factor k = 0.25 1h = Decrement factor k = 0.5 2h = Decrement factor k = 1 3h = Decrement factor k = 2
10-9	SWCL_DLY_TMR_CH1	R/W	X	These bits set the timer at which Channel 1 will shut down if the IOUT current continuously exceeds the ISWCL level for the configured time. 0h = 0.06ms 1h = 0.4ms 2h = 1.0ms 3h = 2.0ms
8-7	ISWCL_CH1	R/W	X	These bits set the delayed turn off current sense value ($I_{SWCL,700}$) for channel 1. Once the IOUT current exceeds the $I_{SWCL,700}$ value, a timer starts and will turn off the channel if the current remains above the $I_{SWCL,700}$ threshold for a duration of SWCL_DLY_TMR_CH1. The threshold should be set below the current sense saturation value (I_{OUT_SAT} = K_{SNS1} * I_{SNS_SAT}). The current threshold below assume R_{SNS} = 700Ω. To calculate the new $I_{SWCL,700}$ thresholds based on a different R_{SNS} value, the following equation can be used: $I_{SWCL,ADJ}$ = ($I_{SWCL,700}$ * (700 / R_{SNS})) / ISNS_SCALE_CH1 Note: The ISWCL_CH1 value cannot be modified when the device is in the cool down time period. 0h = 27.3A 1h = 24.6A 2h = 22.4A 3h = 18.6A

Copyright © 2026 Texas Instruments Incorporated

Table 9-20. I2T_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-3	I2T_TRIP_CH1	R/W	X	These bits set the I2T trip value for Channel 1. Note: For reference the equations for the I2T trip value are below If DCR_CH1 = 0: $I2T_TRIP = I_{OUT1}^2 \times t$ If DCR_CH1 = 1: $I2T = (I_{OUT1}^2 - NOM_CUR_CH1^2) * t$ The below values assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $I2T_{ADJ} = (I2T_{700} * (700 / R_{SNS})^2) / ISNS_SCALE_CH1$ Note: The I2T_TRIP_CH1 value cannot be modified when the device is in the cool down time period. I2T settings with DCR = 0: 0h = 39A2s 1h = 59A2s 2h = 118A2s 3h = 177A2s 4h = 236A2s 5h = 295A2s 6h = 354A2s 7h = 413A2s 8h = 492A2s 9h = 570A2s Ah = 649A2s Bh = 747A2s Ch = 865A2s Dh = 983A2s Eh = 1180A2s Fh = 1573A2s I2T settings with DCR = 1: 0h = 17A2s 1h = 26A2s 2h = 52A2s 3h = 77A2s 4h = 103A2s 5h = 129A2s 6h = 155A2s 7h = 181A2s 8h = 215A2s 9h = 249A2s Ah = 284A2s Bh = 327A2s Ch = 378A2s Dh = 430A2s Eh = 516A2s Fh = 688A2s

Copyright © 2026 Texas Instruments Incorporated

Table 9-20. I2T_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	NOM_CUR_CH1	R/W	X	These bits set the nominal current value for channel 1 for the I2T function. If the I2T function is enabled for channel 1, above this value the device will enter the I2T accumulation mode. The nominal current values below assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $NOM_CUR_CH1_{ADJ} = (NOM_CUR_CH1_{700} * (700 / R_{SNS})) / ISNS_SCALE_CH1$ Note: The NOM_CUR_CH1 value cannot be modified when the device is in the cool down time period. 0h = 5.6A 1h = 7A 2h = 8A 3h = 9A 4h = 10.5A 5h = 12.6A 6h = 16.8A 7h = 21A

Copyright © 2026 Texas Instruments Incorporated

9.19 FLT_STAT_CH2 Register (Offset = 15h) [Reset = E000h]

FLT_STAT_CH2 is shown in Table 9-21.

Return to the Summary Table.

Table 9-21. FLT_STAT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	I2T_MOD_CH2	R	0h	This bit indicates if channel 2 in the I2T loop and is accumulating. When channel 2 is not in the I2T loop the value will be 0 0h = I2T is off or the channel is not in the I2T loop 1h = Channel is in the I2T loop and is accumulating
11	LATCH_STAT_CH2	R	0h	This bit indicates if channel 2 has been latch off due to an overcurrent protection or thermal shutdown fault. The bit clears when the channel is toggled off and back on. Note: This bit does not signal when a shutdown occurs due to I2T 0h = This channel is not latched off 1h = This channel is currently latched off
10	FLT_CH2	R	0h	This bit indicates if channel 2 is currently in an auto retry wait time period, latched off, or in I2T cooldown 0h = This channel is currently not in auto retry wait time, latched off state, or I2T cooldown 1h = This channel is currently in auto retry wait time, latched off state, or I2T cooldown
9	SW_STATE_STAT_CH2	R	0h	This bit indicates the current state of channel 2 no matter which mode the device is in as long as SPI is functioning 0h = CH2 is OFF 1h = CH2 is ON
8	VOUT_ERR_CH2	R	0h	This bit indicates if the drain-to-source voltage (V_{DS}) of channel 2 < $V_{DS_LT_2V}$ after the channel is enabled and is out of the inrush period (if configured) for t > t_{VDS_DEGL}. 0h = The VDS voltage is correct (< 2V) when this channel is enabled 1h = The VDS voltage is incorrect (> 2V) when this channel is supposed to be enabled
7	I2T_FLT_CH2	R	0h	This bit indicates if an I2T fault has occured on channel 2. I2T_EN must be set to 1 in order for this bit indicate an I2T fault. The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists Note: This bit does not indicate an overcurrent protection or thermal shutdown fault 0h = no I2T fault has occurred or I2T is not enabled 1h = I2T fault has occurred on this channel
6	LPM_WAKE_CH2	R	0h	This bit indicates if channel 2 was the cause for the device to come out of AUTO_LPM or MANUAL_LPM regardless of the cause (load step, short-circuit) 0h = The device was not in LPM or this channel was not the cause the device came out of AUTO_LPM or MANUAL_LPM mode 1h = This channel was the reason the device came out of AUTO_LPM or MANUAL_LPM
5	THERMAL_SD_CH2	R	0h	This bit indicates if thermal shutdown fault has occurred on channel 2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and the retry timer has expired and the channel temperature has fallen below the thermal shutdown hysteresis threshold 0h = No thermal shutdown fault has occurred on this channel 1h = A thermal shutdown fault has occurred on this channel

Copyright © 2026 Texas Instruments Incorporated

Table 9-21. FLT_STAT_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ILIMIT_CH2	R	0h	This bit indicates if an overcurrent protection fault has occurred on channel 2 The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists 0h = No overcurrent protection fault has occurred on this channel 1h = Overcurrent protection fault has occurred on this channel
3	SHRT_VBB_CH2	R	0h	This bit indicates if there was a short to VBB in the off-state on channel 2. The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists Note: SVBB_EN_CH2 must be enabled for this bit to signal short to VBB in the off state. 0h = No Short to VBB fault in off-state has occurred on this channel or short to VBB in off-state is not enabled 1h = Short to VBB fault in the off-state has occurred on this channel
2	OL_OFF_CH2	R	0h	This bit indicates if there is an open load in the off-state on channel 2. The output of channel 2 is pulled up by the OL_PULLUP_STR setting. Note: OL_OFF_EN_CH2 must be enabled for this bit to signal an open load in the off-state. 0h = No off-state open load fault has occurred on this channel or off-state open load detection in off-state is not enabled 1h = Off-state open load fault has occurred on this channel
1	RESERVED	R	0h	Reserved
0	THERMAL_WRN_CH2	R	0h	This bit indicates if the channel 2 FET temperature is above the overtemperature warning threshold. The fault is latched and cleared when FLT_STAT_CH2 register is read and the fault condition no longer exists 0h = FET temperature is below the over-temperature warning threshold in this channel 1h = FET temperature is above the over-temperature warning threshold in this channel

Copyright © 2026 Texas Instruments Incorporated

9.20 PWM_CH2 Register (Offset = 16h) [Reset = F000h]

PWM_CH2 is shown in Table 9-22.

Return to the Summary Table.

Table 9-22. PWM_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-9	PWM_FREQ_CH2	R/W	0h	Set the PWM frequency 0h = 0.86Hz 1h = 3.5Hz 2h = 14Hz 3h = 112Hz 4h = 224Hz 5h = 448Hz 6h = 895Hz 7h = 1765Hz
8-1	PWM_DTY_CH2	R/W	0h	These bits are used to set the duty cycle for the PWM operation for channel 2. Each bit is ~0.39% duty cycle, linearly up to 100% duty cycle
0	PWM_EN_CH2	R/W	0h	This bit enables PWM operation of channel 2. Note: The duty cycle of PWM > 200us. If fault will occur in FLT_STAT_CH2 register. PWM mode can only be enabled if CAP_CHRG_CH2[1:0] = 0 0h = Output follows CH2_ON setting 1h = Output is PWM according to duty cycle and frequency set if CH2_ON is high

Copyright © 2026 Texas Instruments Incorporated

9.21 ILIM_CONFIG_CH2 Register (Offset = 17h) [Reset = XXXXh]

ILIM_CONFIG_CH2 is shown in Table 9-23.

Return to the Summary Table.

Table 9-23. ILIM_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	X	Reserved
13-12	CAP_CHRG_CH2	R/W	X	These bits set the capacitive charging mode during the inrush period after turn on. When CAP_CHRG_CH2 = 00, these are bits are programmed as the overcurrent protection threshold during the INRUSH_DURATION_CH2 period. The channel will immediately turn off if the threshold is reached. When CAP_CHRG_CH2 = 10, these bits are programmed as the current limit regulation threshold. The channel will turn on into the current limit and will continue to regulate the current until the output is fully charged or there is a thermal shutdown event. Note: PWM and I2T is not enabled during the INRUSH_DURATION. 0h = No cap charging mode, IOCP value set by INRUSH_LIMIT_CH2 bits 1h = Not supported 2h = Current limit regulation mode, value set by INRUSH_LIMIT_CH2 bits 3h = Not supported
11	I2T_EN_CH2	R/W	X	Enables the I2T functionality for channel 2. I2T can be enabled before the channel is enabled or while it is enabled, but the I2T calculation will only start after the inrush period ends. 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH2	R/W	X	These bits determine the inrush period duration during which the INRUSH_LIMIT_CH2 level applies. 0h = 0ms 1h = 2ms 2h = 4ms 3h = 6ms 4h = 10ms 5h = 20ms 6h = 50ms 7h = 100ms

Copyright © 2026 Texas Instruments Incorporated

Table 9-23. ILIM_CONFIG_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	INRUSH_LIMIT_CH2	R/W	X	These bits determine the inrush current limit on channel 2 for the different capacitive charging modes set by CAP_CHRG_CH2 bits. Note: If VBB > 19V, the device will limit the overcurrent threshold to 66A if the ILIMIT_SET_CH2 > 66A If no cap charging mode (CAP_CHRG_CH2 = 00) is used, the values are: 0x0 = 14.5A 0x1 = 18.2A 0x2 = 20.5A 0x3 = 24.2A 0x4 = 28.5A 0x5 = 30.6A 0x6 = 33.5A 0x7 = 44.3A 0x8 = 53.4A 0x9 = 66A 0xA = 76.2A Note: 0xB–0xF are not supported by design and shall never be selected. If current regulation mode (CAP_CHRG_CH2 = 10) is used, the values are: 0h = 2A 1h = 2.3A 2h = 2.7A 3h = 3.2A 4h = 3.7A 5h = 4.2A 6h = 4.6A 7h = 6.2A 8h = 7.6A 9h = 9.1A Ah = 10.6A Bh = 12.1A Ch = 13.5A Dh = 15.1A Eh = 16.7A Fh = 18.2A
3-0	ILIMIT_SET_CH2	R/W	X	These bits determine the overcurrent protection (I_{OCP}) threshold for channel 2 in steady state operation after the INRUSH_DURATION period expires. Note: If VBB > 19V, the device will limit the overcurrent threshold to 66A if the ILIMIT_SET_CH2 > 66A 0h = 14.5A 1h = 18.2A 2h = 20.5A 3h = 24.2A 4h = 28.5A 5h = 30.6A 6h = 33.5A 7h = 44.3A 8h = 53.4A 9h = 66A Ah = 76.2A

Copyright © 2026 Texas Instruments Incorporated

9.22 CH2_CONFIG Register (Offset = 18h) [Reset = XXXXh]

CH2_CONFIG is shown in Table 9-24.

Return to the Summary Table.

Table 9-24. CH2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH2	R/W	X	This bit determines if the VOUT VSNS ADC function for channel 2 is enabled. 0h = CH2 VOUT VSNS ADC functionality enabled 1h = CH2 VOUT VSNS ADC functionality is disabled
14	VDSSNS_DIS_CH2	R/W	X	This bit determines if the VDS_SNS ADC function for channel 2 is enabled. 0h = CH2 VDS_SNS ADC functionality enabled 1h = CH2 VDS_SNS ADC functionality is disabled
13	ISNS_DIS_CH2	R/W	X	This bit determines if the ISNS ADC function for channel 2 is enabled. 0h = CH2 ISNS ADC functionality enabled 1h = CH2 ISNS ADC functionality is disabled
12	OUT_DIS_MASK_CH2	R/W	X	If DI_OUT_DIS_FN = 1, this bit determines if channel 2 should turn off if OUT_DIS = 1 If DI_OUT_DIS_FN = 0, then this bit has no effect 0h = CH2 will turn OFF when OUT_DIS pin is high 1h = CH2 will ignore OUT_DIS pin when high, CH2 will follow CH2_ON in active state or CH2_LH_IN in limp home state
11	RESERVED	R/W	X	Reserved
10	ISNS_SCALE_CH2	R/W	X	This bit determines the voltage scaling of the channel 2 ISNS for the input to the ADC Note: If I2T is enabled (I2T_EN_CH2 = 1) and ISNS_SCALE_CH2 = 1, the 8x voltage scaling will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. If this is not intended then it is recommended to only use the 8x voltage scaling option when in OL_ON_EN_CH2 = 1 mode and with I2T disabled (I2T_EN_CH2 = 0). 0h = ADC input voltage scale equals 1x 1h = ADC input voltage scale equals 8x
9	OL_ON_EN_CH2	R/W	X	This bit determines if channel 2 should enter a mode with a higher RON and a lower KSNS value to more accurately detect lower output current. Note: It is recommended to only use OL_ON_EN_CH2 = 1 mode with I2T disabled (I2T_EN_CH2 = 0). If I2T is enabled (I2T_EN_CH2 = 1) and OL_ON_EN_CH2 = 1, the lower K_{SNS2} will be applied to the I2T algorithm which will provide different I2T trip thresholds and can cause the channel to turn off at a lower I2T threshold. Note: The device can only enter this mode if there are no existing faults on the channel and the output current is below $I_{ENTRY_OL_ON}$. 0h = KSNS1 ratio and RON = RON 1h = KSNS2 ratio and RON = RON_OL
8-7	OL_SVBB_BLANK_CH2	R/W	X	These bits determine the blanking time for open load or short to VBB faults in the OFF state for channel 2 0h = Blanking time is 0.4ms 1h = Blanking time is 1.0ms 2h = Blanking time is 2.0ms 3h = Blanking time is 4.0ms

Copyright © 2026 Texas Instruments Incorporated

Table 9-24. CH2_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	OL_PU_STR_CH2	R/W	X	These bits determine the pull-up current (I_pu) at the VOUT2 for the off-state open load detection circuitry. 0h = I_pu is 27µA 1h = I_pu is 62µA 2h = I_pu is 128µA 3h = I_pu is 270µA
4-3	OL_SVBB_EN_CH2	R/W	X	The bits are used to enable open load and short to supply detection in OFF state. Setting to 0x02h Turns on the pull up to see if there is an open load or short to supply in the off state with an output comparator. If detected set to 0x1h to turn on a pull down to see if there is a short to VBB in the off state. 0h = Disabled 1h = Turns-on an output pulldown to differentiate Short to supply from open load. 2h = Turns on a pull-up from VBB supply to output to detect if either an open load or short-to-battery exists. 3h = Output comparator enabled, use external switches and pull-up/pull-down to detect open load or short-to-supply.
2	LATCH_CH2	R/W	X	This bit determines if channel 2 should auto-retry or latch off after an overcurrent or thermal shutdown event has occurred. 0h = channel 2 will auto retry after tRETRY expires and THYS is reached 1h = channel 2 latches off until SW_STATE register is written to again
1-0	SLRT_CH2	R/W	X	These bits determine the turn on and turn off slew rates for channel 2. 0h = 0.13V/µs (Rising) and 0.15V/µs (Falling) 1h = 0.22V/µs (Rising) and 0.28V/µs (Falling) 2h = 0.13V/µs (Rising) and 0.3V/µs (Falling) 3h = 0.22V/µs (Rising) and 0.47V/µs (Falling)

Copyright © 2026 Texas Instruments Incorporated

9.23 ADC_RESULT_CH2_I Register (Offset = 19h) [Reset = E000h]

ADC_RESULT_CH2_I is shown in Table 9-25.

Return to the Summary Table.

Table 9-25. ADC_RESULT_CH2_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	ISNS_CH2_ONOFF_STAT	R	0h	The bit is set to 1 if the ADC conversion of ISNS is done while the channel is ON 0h = ISNS read is done while the status of the CH1 FET is OFF 1h = ISNS read is done while the status of the CH1 FET is ON
11	ISNS_SCALE_EFF_CH2	R	0h	The bit indicates the voltage scaling factor used for the conversion 0h = 1x ISNS2 voltage scaling 1h = 8x ISNS2 voltage scaling
10	ISNS_RDY_CH2	R	0h	Making sure the ADC conversion is new from the last time this was read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_I	R	0h	ADC result (10-bits) from the conversion of the current in CH2

Copyright © 2026 Texas Instruments Incorporated

9.24 ADC_RESULT_CH2_T Register (Offset = 1Ah) [Reset = F800h]

ADC_RESULT_CH2_T is shown in Table 9-26.

Return to the Summary Table.

Table 9-26. ADC_RESULT_CH2_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TSNS_RDY_CH2	R	0h	This bit indicates if a new ADC result for channel 2 TSNS conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_T	R	0h	10-bit ADC result from the conversion of channel 2 FET temperature (TSNS)

Copyright © 2026 Texas Instruments Incorporated

9.25 ADC_RESULT_CH2_V Register (Offset = 1Bh) [Reset = F800h]

ADC_RESULT_CH2_V is shown in Table 9-27.

Return to the Summary Table.

Table 9-27. ADC_RESULT_CH2_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VSNS_RDY_CH2	R	0h	This bit indicates if a new ADC result for channel 2 VOUT voltage (VSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_V	R	0h	10-bit ADC result from the conversion of channel 2 VOUT voltage (VSNS)

Copyright © 2026 Texas Instruments Incorporated

9.26 ADC_RESULT_CH2_VDS Register (Offset = 1Ch) [Reset = F800h]

ADC_RESULT_CH2_VDS is shown in Table 9-28.

Return to the Summary Table.

Table 9-28. ADC_RESULT_CH2_VDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VDSSNS_RDY_CH2	R	0h	This bit indicates if a new ADC result for channel 2 VDS voltage (VDSSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH2_VDS	R	0h	10-bit ADC result from the conversion of channel 2 VDS voltage (VDSSNS)

Copyright © 2026 Texas Instruments Incorporated

9.27 I2T_CONFIG_CH2 Register (Offset = 1Dh) [Reset = XXXXh]

I2T_CONFIG_CH2 is shown in Table 9-29.

Return to the Summary Table.

Table 9-29. I2T_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH2	R/W	X	These bits set the cool down time (or time to retry) after an I2T shutdown for channel 2. Note: If setting 0x0 is used, the channel will remain off after an I2T shutdown with no retry. To retry in this setting, change the bits to 0.8s, 2.0s, or 4.0s options to allow the device to retry after an I2T shutdown. 0h = channel off 1h = 0.8s 2h = 2.0s 3h = 4.0s
13	DCR_CH2	R/W	X	Sets the mode of I2T operation for channel 2. If DCR = 0: the device accumulates according to I2T_TRIP = I_{OUT2}^2 x t and decrements according to I2T_TRIP = (I_{OUT2}^2 - k x (NOM_CUR_CH2)^2) x t If DCR = 1: the device accumulates and decrements according to I2T_TRIP = (I_{OUT2}^2 - NOM_CUR_CH2^2) x t. 0h = I2t Mode DCR0 1h = I2t Mode DCR1
12-11	ACC_DCR0_CH2	R/W	X	Decrement factor of accumulated energy when DCR_CH2 = 0 for the following equation: I2T_TRIP = (I_{OUT2}^2 - k x (NOM_CUR_CH2)^2) x t 0h = Decrement factor k = 0.25 1h = Decrement factor k = 0.5 2h = Decrement factor k = 1 3h = Decrement factor k = 2
10-9	SWCL_DLY_TMR_CH2	R/W	X	2-bits to set delayed turn-off timer for Channel 2. Sets the time after which the channel shuts down when the current exceeds ISWCL. The default values loaded from NVM. 0h = 0.06ms 1h = 0.4ms 2h = 1.0ms 3h = 2.0ms
8-7	ISWCL_CH2	R/W	X	These bits set the delayed turn off current sense value ($I_{SWCL,700}$) for channel 2. Once the I_{OUT} current exceeds the $I_{SWCL,700}$ value, a timer starts and will turn off the channel if the current remains above the $I_{SWCL,700}$ threshold for a duration of SWCL_DLY_TMR_CH2. The threshold should be set below the current sense saturation value (I_{OUT_SAT} = K_{SNS1} * I_{SNS_SAT}). The current threshold below assume R_{SNS} = 700Ω. To calculate the new $I_{SWCL,700}$ thresholds based on a different R_{SNS} value, the following equation can be used: $I_{SWCL,ADJ}$ = ($I_{SWCL,700}$ * (700 / R_{SNS})) / ISNS_SCALE_CH2 Note: The ISWCL_CH2 value cannot be modified when the device is in the cool down time period. 0h = 27.3A 1h = 24.6A 2h = 22.4A 3h = 18.6A

Copyright © 2026 Texas Instruments Incorporated

Table 9-29. I2T_CONFIG_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-3	I2T_TRIP_CH2	R/W	X	These bits set the I2T trip value for Channel 2. Note: For reference the equations for the I2T trip value are below If DCR_CH2 = 0: $I2T_TRIP = I_{OUT2}^2 \times t$ If DCR_CH2 = 1: $I2T = (I_{OUT2}^2 - NOM_CUR_CH2^2) * t$ The below values assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $I2T_{ADJ} = (I2T_{700} * (700 / R_{SNS})^2) / ISNS_SCALE_CH2$ Note: The I2T_TRIP_CH2 value cannot be modified when the device is in the cool down time period. I2T settings with DCR = 0: 0h = 39A2s 1h = 59A2s 2h = 118A2s 3h = 177A2s 4h = 236A2s 5h = 295A2s 6h = 354A2s 7h = 413A2s 8h = 492A2s 9h = 570A2s Ah = 649A2s Bh = 747A2s Ch = 865A2s Dh = 983A2s Eh = 1180A2s Fh = 1573A2s I2T settings with DCR = 1: 0h = 17A2s 1h = 26A2s 2h = 52A2s 3h = 77A2s 4h = 103A2s 5h = 129A2s 6h = 155A2s 7h = 181A2s 8h = 215A2s 9h = 249A2s Ah = 284A2s Bh = 327A2s Ch = 378A2s Dh = 430A2s Eh = 516A2s Fh = 688A2s

Copyright © 2026 Texas Instruments Incorporated

Table 9-29. I2T_CONFIG_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	NOM_CUR_CH2	R/W	X	These bits set the nominal current value for channel 2 for the I2T function. If the I2T function is enabled for channel 2, above this value the device will enter the I2T accumulation mode. The nominal current values below assume R_{SNS} = 700Ω. To calculate the new I2T trip values based on a different R_{SNS} value, the following equation can be used: $NOM_CUR_CH2_{ADJ} = (NOM_CUR_CH2_{700} * (700 / R_{SNS})) / ISNS_SCALE_CH2$ Note: The NOM_CUR_CH2 value cannot be modified when the device is in the cool down time period. 0h = 5.6A 1h = 7A 2h = 8A 3h = 9A 4h = 10.5A 5h = 12.6A 6h = 16.8A 7h = 21A

Copyright © 2026 Texas Instruments Incorporated

9.28 EEPROM_PROG Register (Offset = 3Fh) [Reset = FFFCh]

EEPROM_PROG is shown in Table 9-30.

Return to the Summary Table.

Table 9-30. EEPROM_PROG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	3FFFh	Reserved
1	EEPROM_BUSY	R	0h	EEPROM programming status 0h = Device is not in EEPROM programming procedure 1h = Device is currently in EEPROM programming procedure
0	PROG_NVM	R	0h	EEPROM programming control status bit. This bit will self clear to 0 when the EEPROM programming is complete 1h = Device is programming EEPROM

Copyright © 2026 Texas Instruments Incorporated

9.29 TSNS_CAL_RESULT_CH1 Register (Offset = 50h) [Reset = XXXXh]

TSNS_CAL_RESULT_CH1 is shown in Table 9-31.

Return to the Summary Table.

Table 9-31. TSNS_CAL_RESULT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	X	Reserved
9-0	TSNS_CAL_RESULT_CH1	R/W	X	10-bit ADC result from production for channel 1 FET temperature (TSNS)

Copyright © 2026 Texas Instruments Incorporated

9.30 TSNS_CAL_RESULT_CH2 Register (Offset = 51h) [Reset = XXXXh]

TSNS_CAL_RESULT_CH2 is shown in Table 9-32.

Return to the Summary Table.

Table 9-32. TSNS_CAL_RESULT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	X	Reserved
9-0	TSNS_CAL_RESULT_CH2	R/W	X	10-bit ADC result from production for channel 2 FET temperature (TSNS)

Copyright © 2026 Texas Instruments Incorporated

9.31 CUST_REG_52 Register (Offset = 52h) [Reset = XXXXh]

CUST_REG_52 is shown in Table 9-33.

Return to the Summary Table.

Table 9-33. CUST_REG_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CUST_REG_52_BIT15	R/W	X	Customer programmable bit
14	CUST_REG_52_BIT14	R/W	X	Customer programmable bit
13	CUST_REG_52_BIT13	R/W	X	Customer programmable bit
12	CUST_REG_52_BIT12	R/W	X	Customer programmable bit
11	CUST_REG_52_BIT11	R/W	X	Customer programmable bit
10	CUST_REG_52_BIT10	R/W	X	Customer programmable bit
9	CUST_REG_52_BIT9	R/W	X	Customer programmable bit
8	CUST_REG_52_BIT8	R/W	X	Customer programmable bit
7	CUST_REG_52_BIT7	R/W	X	Customer programmable bit
6	CUST_REG_52_BIT6	R/W	X	Customer programmable bit
5	CUST_REG_52_BIT5	R/W	X	Customer programmable bit
4	CUST_REG_52_BIT4	R/W	X	Customer programmable bit
3	CUST_REG_52_BIT3	R/W	X	Customer programmable bit
2	CUST_REG_52_BIT2	R/W	X	Customer programmable bit
1	CUST_REG_52_BIT1	R/W	X	Customer programmable bit
0	CUST_REG_52_BIT0	R/W	X	Customer programmable bit

Copyright © 2026 Texas Instruments Incorporated

9.32 CUST_REG_53 Register (Offset = 53h) [Reset = XXXXh]

CUST_REG_53 is shown in Table 9-34.

Return to the Summary Table.

Table 9-34. CUST_REG_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CUST_REG_53_BIT15	R/W	X	Customer programmable bit
14	CUST_REG_53_BIT14	R/W	X	Customer programmable bit
13	CUST_REG_53_BIT13	R/W	X	Customer programmable bit
12	CUST_REG_53_BIT12	R/W	X	Customer programmable bit
11	CUST_REG_53_BIT11	R/W	X	Customer programmable bit
10	CUST_REG_53_BIT10	R/W	X	Customer programmable bit
9	CUST_REG_53_BIT9	R/W	X	Customer programmable bit
8	CUST_REG_53_BIT8	R/W	X	Customer programmable bit
7	CUST_REG_53_BIT7	R/W	X	Customer programmable bit
6	CUST_REG_53_BIT6	R/W	X	Customer programmable bit
5	CUST_REG_53_BIT5	R/W	X	Customer programmable bit
4	CUST_REG_53_BIT4	R/W	X	Customer programmable bit
3	CUST_REG_53_BIT3	R/W	X	Customer programmable bit
2	CUST_REG_53_BIT2	R/W	X	Customer programmable bit
1	CUST_REG_53_BIT1	R/W	X	Customer programmable bit
0	CUST_REG_53_BIT0	R/W	X	Customer programmable bit

Copyright © 2026 Texas Instruments Incorporated

9.33 CUST_REG_54 Register (Offset = 54h) [Reset = XXXXh]

CUST_REG_54 is shown in Table 9-35.

Return to the Summary Table.

Table 9-35. CUST_REG_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CUST_REG_54_BIT15	R/W	X	Customer programmable bit
14	CUST_REG_54_BIT14	R/W	X	Customer programmable bit
13	CUST_REG_54_BIT13	R/W	X	Customer programmable bit
12	CUST_REG_54_BIT12	R/W	X	Customer programmable bit
11	CUST_REG_54_BIT11	R/W	X	Customer programmable bit
10	CUST_REG_54_BIT10	R/W	X	Customer programmable bit
9	CUST_REG_54_BIT9	R/W	X	Customer programmable bit
8	CUST_REG_54_BIT8	R/W	X	Customer programmable bit
7	CUST_REG_54_BIT7	R/W	X	Customer programmable bit
6	CUST_REG_54_BIT6	R/W	X	Customer programmable bit
5	CUST_REG_54_BIT5	R/W	X	Customer programmable bit
4	CUST_REG_54_BIT4	R/W	X	Customer programmable bit
3	CUST_REG_54_BIT3	R/W	X	Customer programmable bit
2	CUST_REG_54_BIT2	R/W	X	Customer programmable bit
1	CUST_REG_54_BIT1	R/W	X	Customer programmable bit
0	CUST_REG_54_BIT0	R/W	X	Customer programmable bit

Copyright © 2026 Texas Instruments Incorporated

9.34 CUST_REG_55 Register (Offset = 55h) [Reset = XXXXh]

CUST_REG_55 is shown in Table 9-36.

Return to the Summary Table.

Table 9-36. CUST_REG_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CUST_REG_55_BIT15	R/W	X	Customer programmable bit
14	CUST_REG_55_BIT14	R/W	X	Customer programmable bit
13	CUST_REG_55_BIT13	R/W	X	Customer programmable bit
12	CUST_REG_55_BIT12	R/W	X	Customer programmable bit
11	CUST_REG_55_BIT11	R/W	X	Customer programmable bit
10	CUST_REG_55_BIT10	R/W	X	Customer programmable bit
9	CUST_REG_55_BIT9	R/W	X	Customer programmable bit
8	CUST_REG_55_BIT8	R/W	X	Customer programmable bit
7	CUST_REG_55_BIT7	R/W	X	Customer programmable bit
6	CUST_REG_55_BIT6	R/W	X	Customer programmable bit
5	CUST_REG_55_BIT5	R/W	X	Customer programmable bit
4	CUST_REG_55_BIT4	R/W	X	Customer programmable bit
3	CUST_REG_55_BIT3	R/W	X	Customer programmable bit
2	CUST_REG_55_BIT2	R/W	X	Customer programmable bit
1	CUST_REG_55_BIT1	R/W	X	Customer programmable bit
0	CUST_REG_55_BIT0	R/W	X	Customer programmable bit

Copyright © 2026 Texas Instruments Incorporated

9.35 CUST_REG_56 Register (Offset = 56h) [Reset = XXXXh]

CUST_REG_56 is shown in Table 9-37.

Return to the Summary Table.

Table 9-37. CUST_REG_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CUST_REG_56_BIT15	R/W	X	Customer programmable bit
14	CUST_REG_56_BIT14	R/W	X	Customer programmable bit
13	CUST_REG_56_BIT13	R/W	X	Customer programmable bit
12	CUST_REG_56_BIT12	R/W	X	Customer programmable bit
11	CUST_REG_56_BIT11	R/W	X	Customer programmable bit
10	CUST_REG_56_BIT10	R/W	X	Customer programmable bit
9	CUST_REG_56_BIT9	R/W	X	Customer programmable bit
8	CUST_REG_56_BIT8	R/W	X	Customer programmable bit
7	CUST_REG_56_BIT7	R/W	X	Customer programmable bit
6	CUST_REG_56_BIT6	R/W	X	Customer programmable bit
5	CUST_REG_56_BIT5	R/W	X	Customer programmable bit
4	CUST_REG_56_BIT4	R/W	X	Customer programmable bit
3	CUST_REG_56_BIT3	R/W	X	Customer programmable bit
2	CUST_REG_56_BIT2	R/W	X	Customer programmable bit
1	CUST_REG_56_BIT1	R/W	X	Customer programmable bit
0	CUST_REG_56_BIT0	R/W	X	Customer programmable bit

Copyright © 2026 Texas Instruments Incorporated

9.36 CUST_REG_57 Register (Offset = 57h) [Reset = XXXXh]

CUST_REG_57 is shown in Table 9-38.

Return to the Summary Table.

Table 9-38. CUST_REG_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CUST_REG_57_BIT15	R/W	X	Customer programmable bit
14	CUST_REG_57_BIT14	R/W	X	Customer programmable bit
13	CUST_REG_57_BIT13	R/W	X	Customer programmable bit
12	CUST_REG_57_BIT12	R/W	X	Customer programmable bit
11	CUST_REG_57_BIT11	R/W	X	Customer programmable bit
10	CUST_REG_57_BIT10	R/W	X	Customer programmable bit
9	CUST_REG_57_BIT9	R/W	X	Customer programmable bit
8	CUST_REG_57_BIT8	R/W	X	Customer programmable bit
7	CUST_REG_57_BIT7	R/W	X	Customer programmable bit
6	CUST_REG_57_BIT6	R/W	X	Customer programmable bit
5	CUST_REG_57_BIT5	R/W	X	Customer programmable bit
4	CUST_REG_57_BIT4	R/W	X	Customer programmable bit
3	CUST_REG_57_BIT3	R/W	X	Customer programmable bit
2	CUST_REG_57_BIT2	R/W	X	Customer programmable bit
1	CUST_REG_57_BIT1	R/W	X	Customer programmable bit
0	CUST_REG_57_BIT0	R/W	X	Customer programmable bit

Copyright © 2026 Texas Instruments Incorporated

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

Figure 10-1 and Figure 10-2 shows the schematic of a typical application of the TPS2HCS05A-Q1 and TPS2HCS05B-Q1, respectively. It includes all standard external components. This section of the datasheet describes the considerations in implementing commonly required application functionality. The circuit assumes no reverse polarity protection on the input supply, so additional components for protection are required.

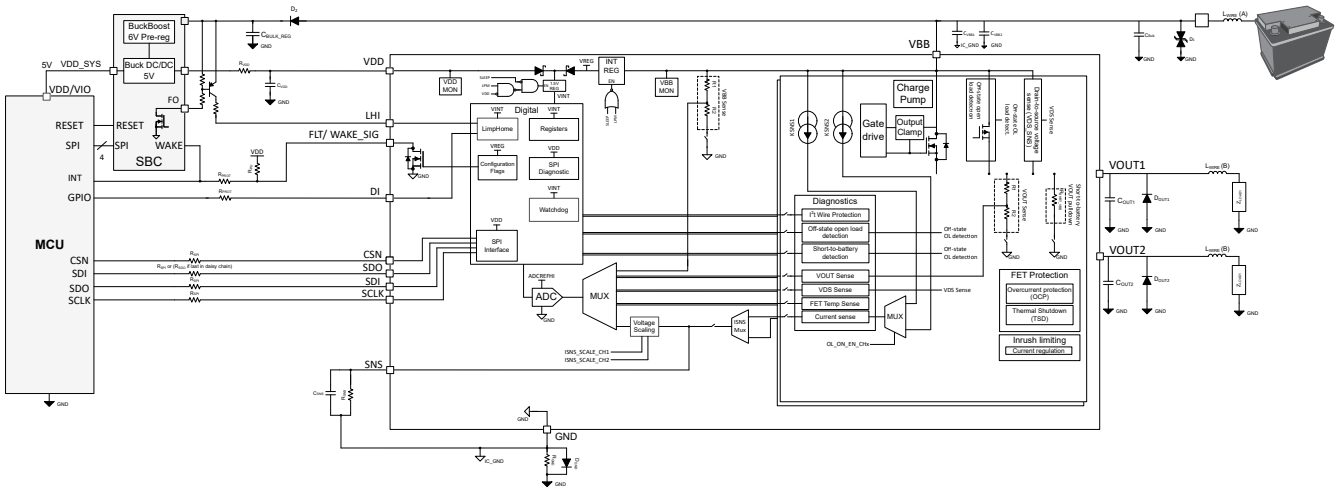


Figure 10-1. System Diagram - TPS2HCS05A-Q1

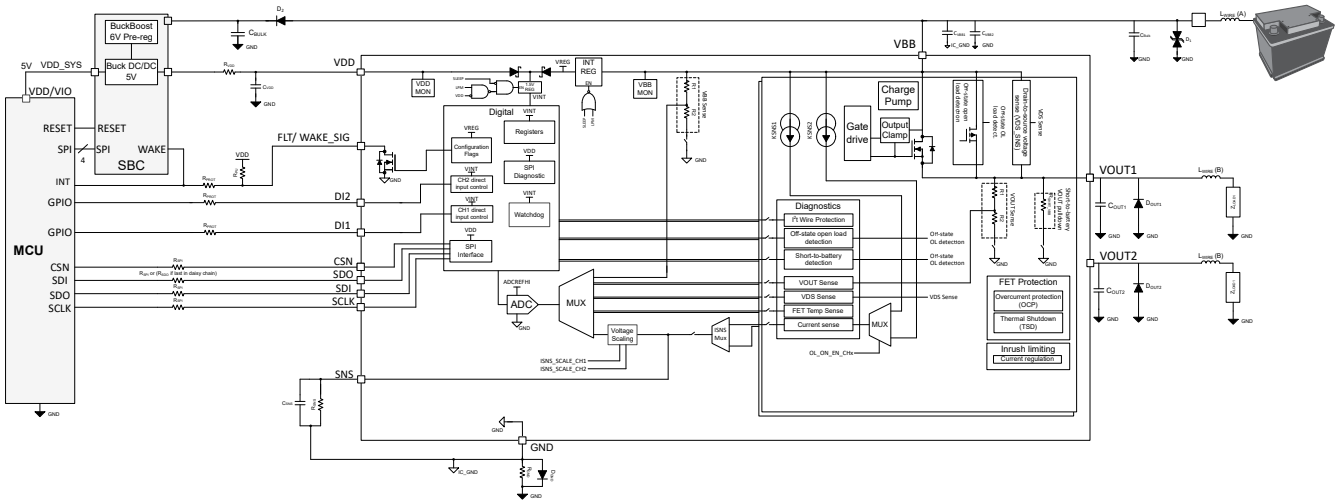


Figure 10-2. System Diagram - TPS2HCS05B-Q1

Table 10-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{SPI}	22Ω	(Optional) For EMI or other transient limits on the SPI pins.
R_{SDO}	100Ω	(Optional) For EMI or other transient limits on the SPI pins.
R_{PROT}	10kΩ	Protect microcontroller and device GPIO pins
R_{SNS}	0.2-1.5kΩ	Translate the sense current into sense voltage for internal ADC input
C_{SNS}	1 - 4.7nF	Low-pass filter for the ADC input.
D_1	±36V	To suppress voltage transients (one for the module)
D_{GND}	BAS21 / Schottky Diode	To limit the voltage drop across R_{GND} during normal operation of the device. A low forward voltage diode is recommended and a Schottky diode is suggested when the VDD is 3.3V. (**Note:** Recommended VDD operation is 5V for lower Iq)
R_{GND}	4.7kΩ	Maintain ground potential during negative output voltage excursions
R_{VDD}	10Ω	Limit the rate of rise / fall in VDD supply input- to the IC.
C_{VDD}	470nF	VDD supply voltage stability to system ground.
C_{VBB1}	1 – 4.7nF to IC_GND	(Optional) For improved emissions.
C_{VBB2}	20µF to Module GND	Stabilize the input supply and filter out low-frequency noise.
C_{OUTx}	100nF	Filtering of voltage transients (for example, ESD, ISO7637-2).
C_{BULK}	200µF - 1.2mF to Module GND	(Optional) To stabilize the input supply during Short-to-Ground Events. Bulk Capacitance can be consist of A.) a large single capacitor or B.) multiple smaller capacitors shared across all eFuses sharing a common input supply.
L_{WIRE}	0.5µH to 5µH	Parasitic inductance of wire harness between A.) Output of Battery and Input of the eFuse and B.) eFuse output and downstream load.
D_{OUTx}	Free-Wheeling Diode	**Note:** For protection against reverse polarity, a diode is required between the Battery and the eFuse to prevent excessive reverse current from flowing through the eFuse Power FET.

To establish the highest level of reliability and best transient response during high-current fault or short-circuit events, specific component selection is required. For robust protection performance, especially in high-current applications, designers must use an input TVS diode and a minimum input capacitance of 20uF to stabilize the input voltage and suppress high-frequency transients. Additionally, the inclusion of an output Schottky diode is essential to provide a freewheeling path for inductive load current and to minimize voltage overshoot during rapid current transitions. The use of these external components is mandatory to minimize channel crosstalk and establish stable and predictable device behavior across the full operating range. When implemented with the recommended external components as shown in the system diagram, the device meets the requirements of the AEC-Q100-012 standard for short-circuit reliability characterization.

During severe short-circuit or overcurrent events on one channel, strong transients can induce crosstalk affecting adjacent channels. High input-side inductance can cause rapid ringing and significant dips in the VBB supply voltage, potentially dropping below $V_{BB_UV_WRN_F}$ threshold or causing VBB fluctuations that trigger unintended overcurrent protection or UVLO events on the victim channel. When this occurs, the victim channel undergoes a temporary shutdown and execute a retry after a 2ms interval. While the risk of crosstalk is significantly reduced when using the recommended external components as shown in the system diagram, it can still be observed during high-current operations, specifically when a victim channel is operating above ILIMIT_SET_CHx setting of 0x05 (15A load) while an aggressor channel is operating at ILIMIT_SET_CHx settings of 9h and Ah. Utilizing the recommended components is critical to dampening transients, stabilizing the VBB rail, and pushing the onset of crosstalk to higher current thresholds.

10.2 Typical Application

This application example demonstrates how the TPS2HCS05A-Q1 device can be used to power ECU loads with large input capacitance. This is just one example of the many applications where this device can fit.

Copyright © 2026 Texas Instruments Incorporated

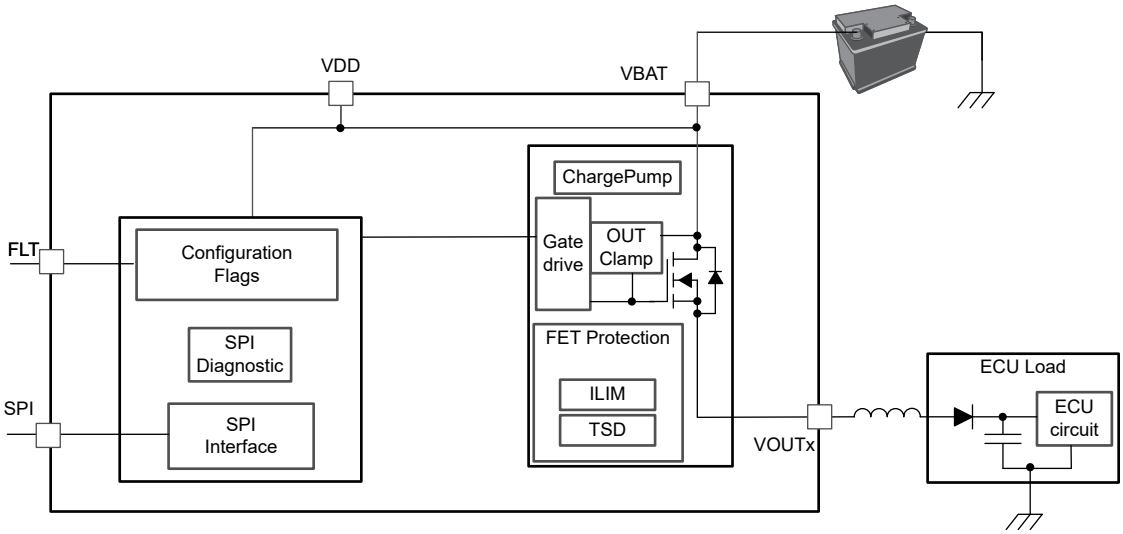


Figure 10-3. Block Diagram for Powering an ECU Load with Input Capacitance

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-2.

Table 10-2. Design Parameters

DESIGN PARAMETER	VALUES
V_{BB} range	8V to 18V
Input Capacitance of the ECU load	2mF
Time to charge	6ms
Ambient temperature	85°C

10.2.2 Detailed Design Procedure

10.2.2.1 Thermal Considerations

During cap-charging, the output voltage ramps up from zero toward the supply voltage while the FET regulates the current flowing into the load capacitor. Since the voltage across the FET stays large for most of this ramp, the power it dissipates during charging is much higher than what it sees during normal, steady-state conduction. This surge in power causes the junction temperature of the FET to rise quickly, and this rise is limited by how well the device can spread and dissipate heat, as well as by the maximum temperature the silicon can safely tolerate before the device trips into thermal shutdown.

This leads to a basic trade-off in selecting the charging current. A lower charging current reduces the power dissipated and keeps the temperature rise in check, allowing a larger capacitor to be charged safely, but it takes longer to fully charge the capacitor. A higher charging current charges the capacitor faster, but increases the power dissipation and heating in the FET, which raises the risk of hitting thermal shutdown if the capacitance is large or the ambient temperature is already high.

The total energy that must be absorbed during this charging event depends on the capacitor size and the supply voltage, and nearly all of this energy is dissipated inside the FET, since the device is operating in a resistive, voltage-dropping mode rather than simply switching on into a load. Because this is a short, one-time thermal event rather than a continuous heating condition, designers must evaluate it using the device's short-duration thermal response rather than relying only on steady-state thermal ratings, since the component can tolerate much more power for a brief pulse than it can on a sustained basis.

Copyright © 2026 Texas Instruments Incorporated

10.2.2.2 Configuring the Capacitive Charging Mode

The configuration parameters for the two channels are in the ILIM_CONFIG_CHx registers. The device offers a constant current charging mode designed for cases where there is a significant load current during charging phase. The current limit regulation value is set by the INRUSH_LIMIT_CHx bits ([7:4]) in the ILIM_CONFIG_CHx registers. The INRUSH_DURATION_CHx bits must be set such that the worst-case expected capacitive charge time is below the programmed inrush duration. The recommended choice of bit settings for each application case is listed in the table below.

Table 10-3. Setting Capacitive Charging Mode Parameters

Bit Field in the ILIM_CONFIG_CHx Register	Settings
CAP_CHRG_CHx	0x02h
INRUSH_DURATION_CHx	0x05h
INRUSH_LIMIT_CHx	0x05h

10.2.3 Application Curves

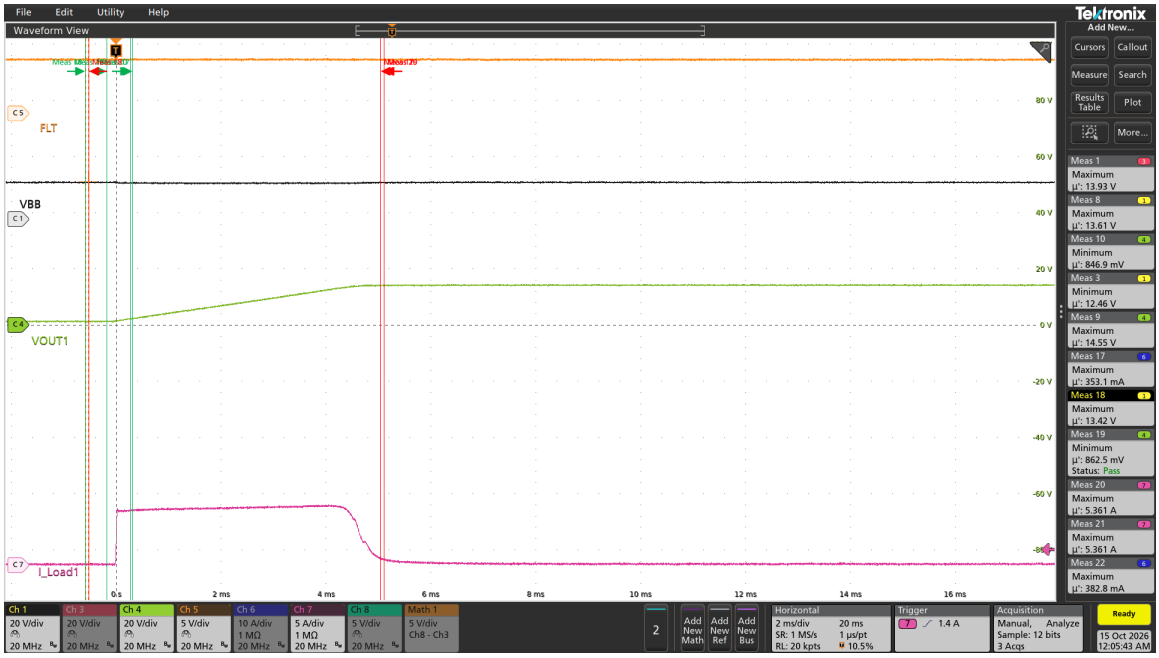


Figure 10-4. ICL_REG - Current Limit Regulation, VBB = 13.5V, INRUSH_DURATION = 0x5 (20ms), INRUSH_LIMIT_CHx = 0x5 (4.2A)

Copyright © 2026 Texas Instruments Incorporated

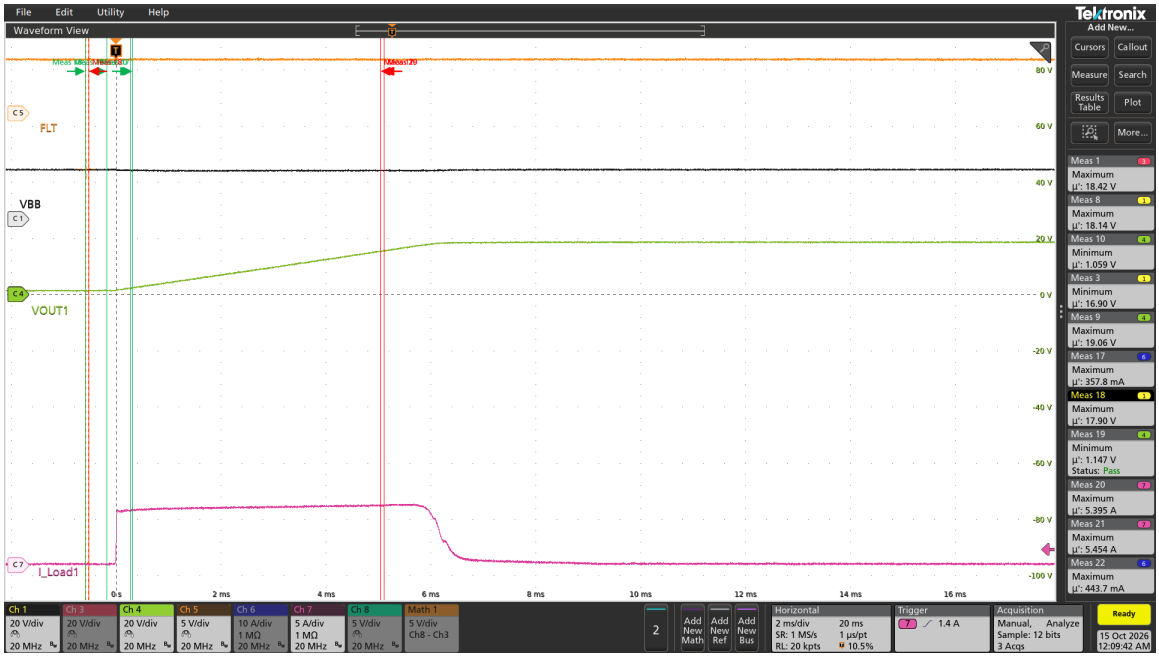


Figure 10-5. ICL_REG - Current Limit Regulation, VBB = 18V, INRUSH_DURATION = 0x5 (20ms), INRUSH_LIMIT_CHx = 0x5 (4.2A)

10.3 Power Supply Recommendations

The device is designed to operate in a 12V automotive system. The device works with two power supply inputs – a typically 12V battery input and a low voltage supply input (5V or 3.3V) typically generated with a DC-DC converter (recommended to reduce quiescent current draw from the battery) or LDO external to the IC from the battery.

The nominal supply voltage range is from 6V to 18V as measured at the V_{BB} pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in Section 6.5. The device is also designed to withstand voltage transients beyond this range like load dump. When operating outside of the nominal voltage range but within the operating voltage range, the device exhibits normal functional behavior.

A reliable, low-impedance connection between the IC GND pin and the system/module ground must be maintained at all times for proper device operation. Operation with a disconnected or high-impedance GND path is outside the recommended operating conditions and is not supported.

If the IC GND connection is lost, the GND pin can float toward the VBB potential, resulting in unpredictable device behavior. Depending on VDD level, this can include unintended output channel activation, elevated quiescent current ($I_{Q,VBB}$), or invalid SPI communication. Device behavior under this condition is not specified and must not be relied upon.

Table 10-4. Operating Voltage Range

V_{BB} VOLTAGE RANGE	NOTE
3V to 6V	Extended lower 12V automotive battery operation such as cold crank and start-stop. Device is fully functional and protected but some parametrics, such as RON, current sense accuracy, overcurrent thresholds and timing parameters, can deviate from specifications. Check the individual specifications in the *Electrical Characteristics* to confirm the voltage range it is applicable for. To establish appropriate OCP triggering accuracy, it is recommended to operate the device with a VBB voltage greater than 6V. Operating in the from 3V to 6V range can result in degraded OCP threshold precision.
6V to 18V	Nominal supply voltage, all parametric specifications apply. The device is short circuit protected up to 18V in MANUAL_LPM, AUTO_LPM, and OL_ON_EN = 1 modes.

Copyright © 2026 Texas Instruments Incorporated

Table 10-4. Operating Voltage Range (continued)

V_{BB} VOLTAGE RANGE	NOTE
18V to 24V	Extended upper 12V automotive battery operation such as double battery. Device is fully functional and protected but some parametrics such as RON, current sense accuracy, overcurrent thresholds, and timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for. The device is short circuit protected up to 125°C.
24V to 35V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

10.4 Layout

10.4.1 Layout Guidelines

To achieve peak thermal performance, connect the exposed pad to a large copper pour. On the top PCB layer, the pour can extend beyond the package dimensions as shown in the layout examples below. In addition to this, it is recommended to have a VBB plane on one or more internal PCB layers or on the bottom layer. Vias must connect these planes to the top VBB pour.

TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

The R_{SNS} and C_{SNS} components must be placed close to the SNS pin. If a ground network is used for reverse battery protection, the R_{SNS} and C_{SNS} must connect from the SNS pin to the IC_GND net for accurate current sense measurements by the internal ADC.

If used in the design, C_{VBB1}, must be placed as close as possible to the VBB and GND pin of the device. If a ground network is used for reverse battery protection, the C_{VBB1} capacitor must connect from the VBB net to the IC_GND net.

10.4.2 Layout Example

Figure 10-6 and Figure 10-7 below show example PCB layouts with and without a GND network, respectively. TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

Copyright © 2026 Texas Instruments Incorporated

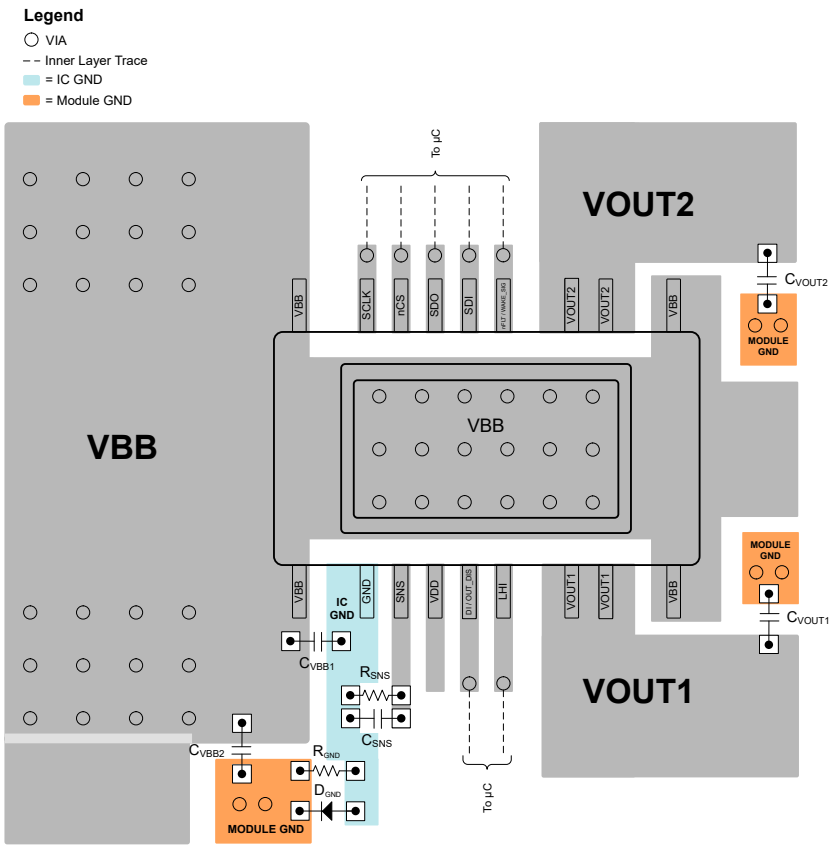


Figure 10-6. Layout Example with Ground Network

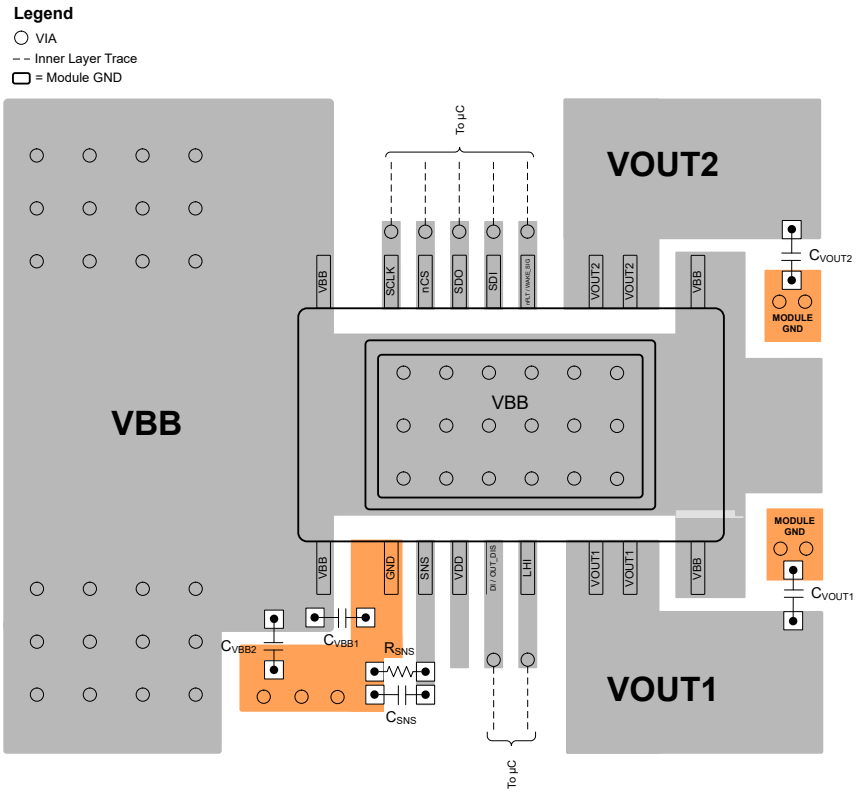


Figure 10-7. Layout Example without Ground Network

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS2HCS05AQPWPRQ1	Active	Preproduction	HTSSOP (PWC) | 18	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

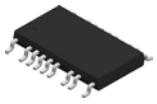
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

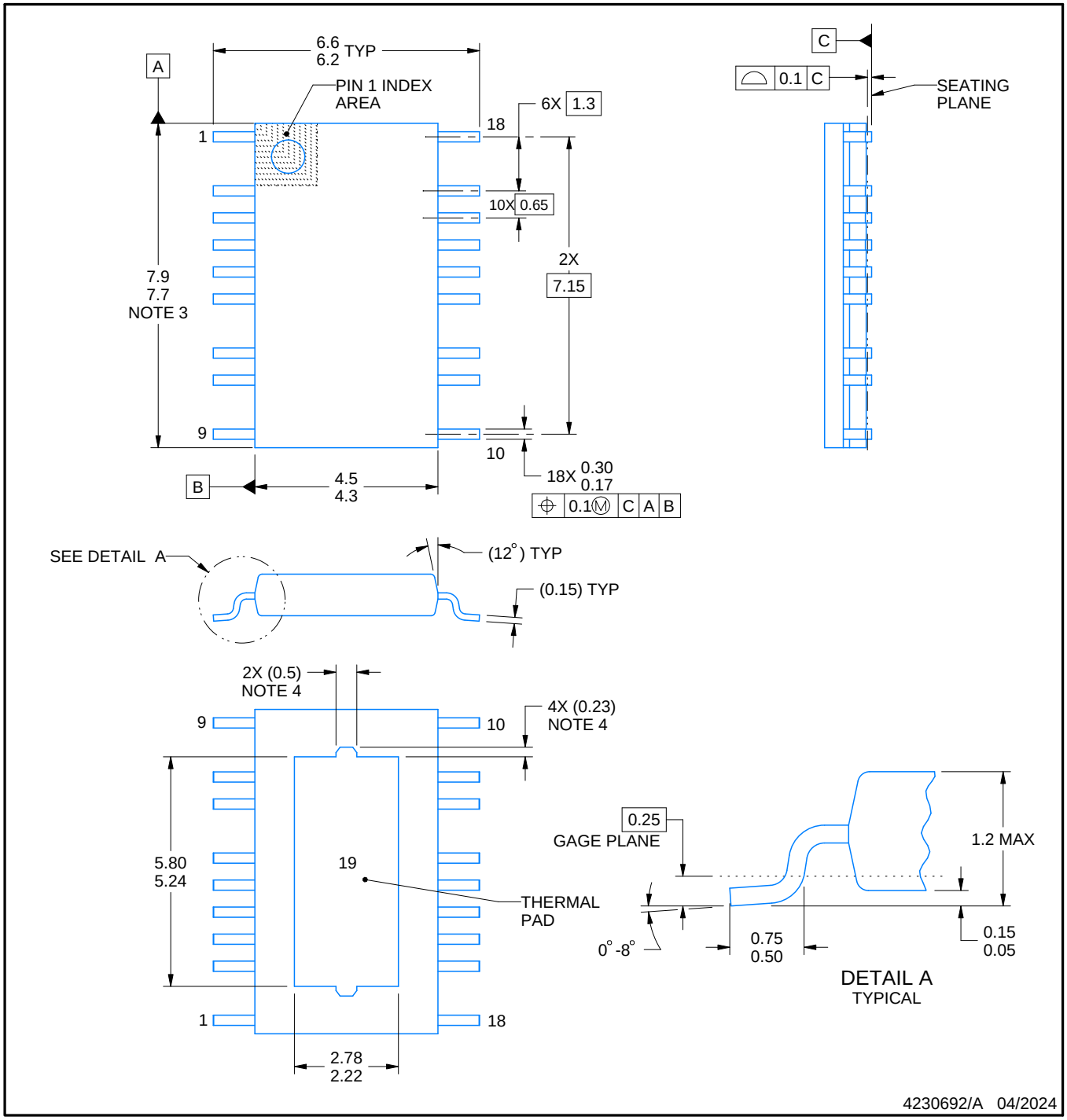
PACKAGE OUTLINE

PWC0018A



PowerPAD™ TSSOP - 1.2 mm max height

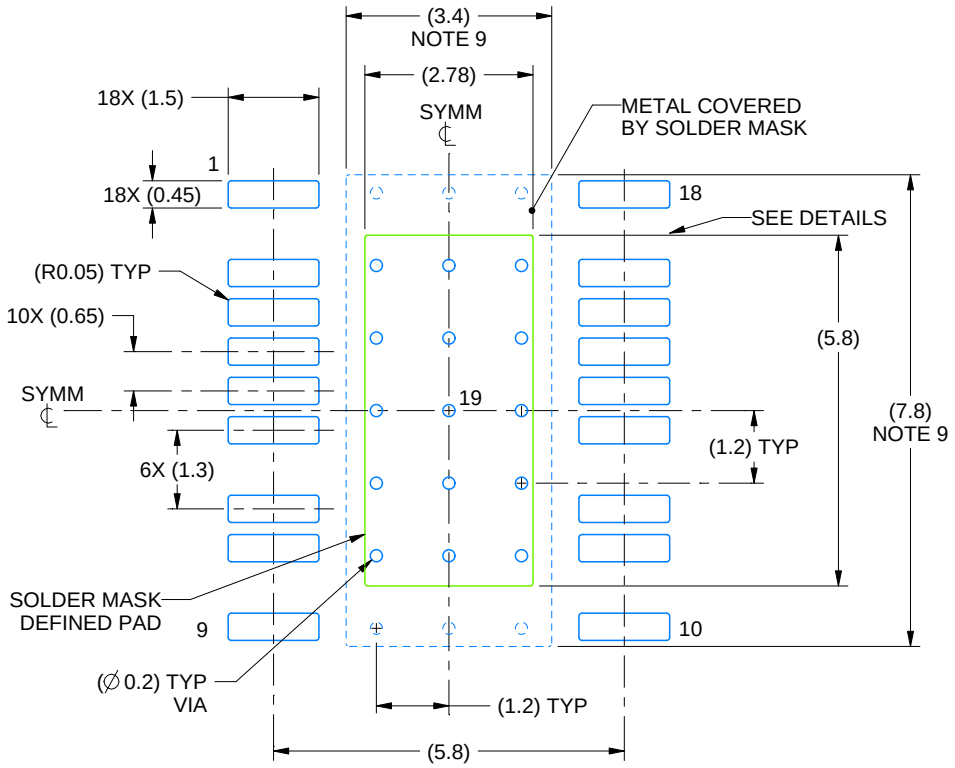
SMALL OUTLINE PACKAGE



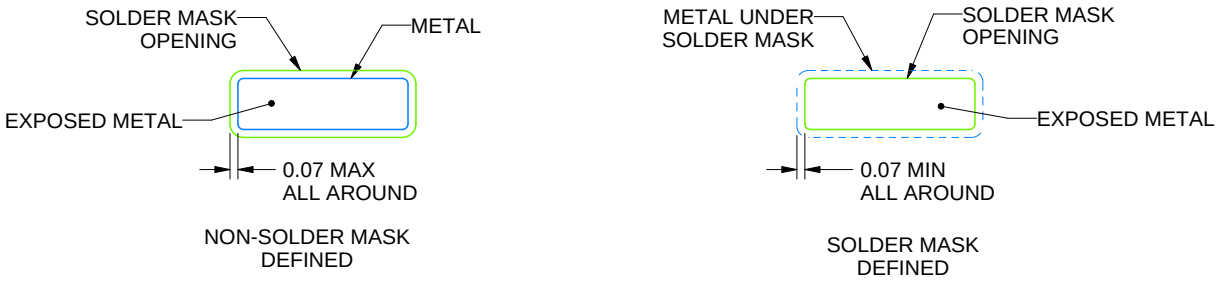
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

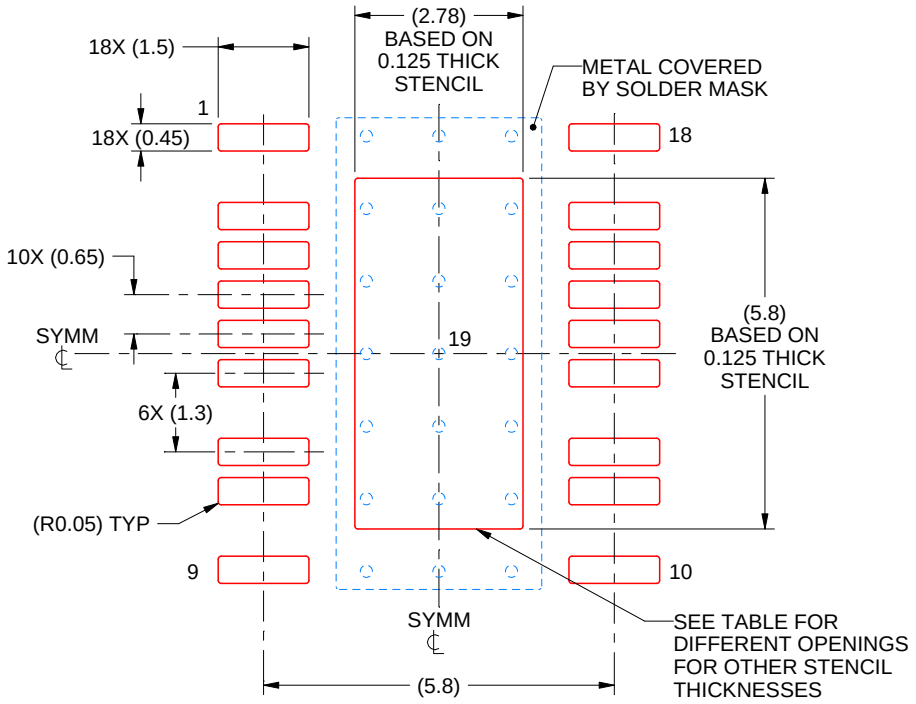


SOLDER MASK DETAILS

4230692/A 04/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.11 X 6.48
0.125	2.78 X 5.80 (SHOWN)
0.15	2.54 X 5.29
0.175	2.35 X 4.90

4230692/A 04/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025