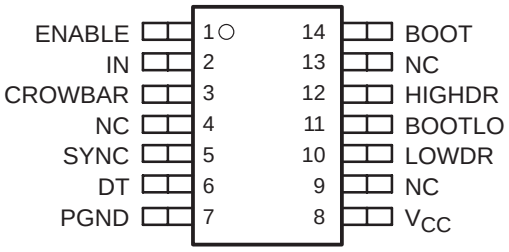
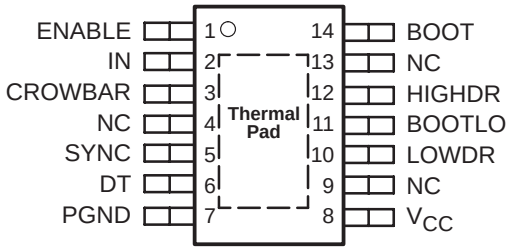
- **Floating Bootstrap or Ground-Reference High-Side Driver**
- **Adaptive Dead-Time Control**
- **50-ns Max Rise/Fall Times With 3.3-nF Load**
- **2.4-A Typical Output Current**
- **4.5-V to 15-V Supply Voltage Range**
- **TTL-Compatible Inputs**
- **Internal Schottky Bootstrap Diode**
- **SYNC Control for Synchronous or Nonsynchronous Operation**
- **CROWBAR for OVP, Protects Against Faulted High-Side Power FETs**
- **Low Supply Current....3 mA Typical**
- **Ideal for High-Current Single or Multiphase Power Supplies**
- **−40°C to 125°C Operating Virtual Junction Temperature Range**
- **Available in SOIC and TSSOP PowerPAD Packages**

D PACKAGE
(TOP VIEW)



PWP PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TPS2834 and TPS2835 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using switching controllers that do not include on-chip MOSFET drivers. The drivers are designed to deliver minimum 2-A peak currents into large capacitive loads. The high-side driver can be configured as ground-reference or as floating-bootstrap. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions, and provides high efficiency for the buck regulator. The TPS2834 and TPS2835 have additional control functions: ENABLE, SYNC, and CROWBAR. Both high-side and low-side drivers are off when ENABLE is low. The driver is configured as a nonsynchronous-buck driver disabling the low-side driver when SYNC is low. The CROWBAR function turns on the low-side power FET, overriding the IN signal, for overvoltage protection against faulted high-side power FETs.

The TPS2834 has a noninverting input, while the TPS2835 has an inverting input. These drivers are available in 14-terminal SOIC and thermally enhanced TSSOP PowerPAD™ packages and operate over a junction temperature range of −40°C to 125°C.

Related Synchronous MOSFET Drivers

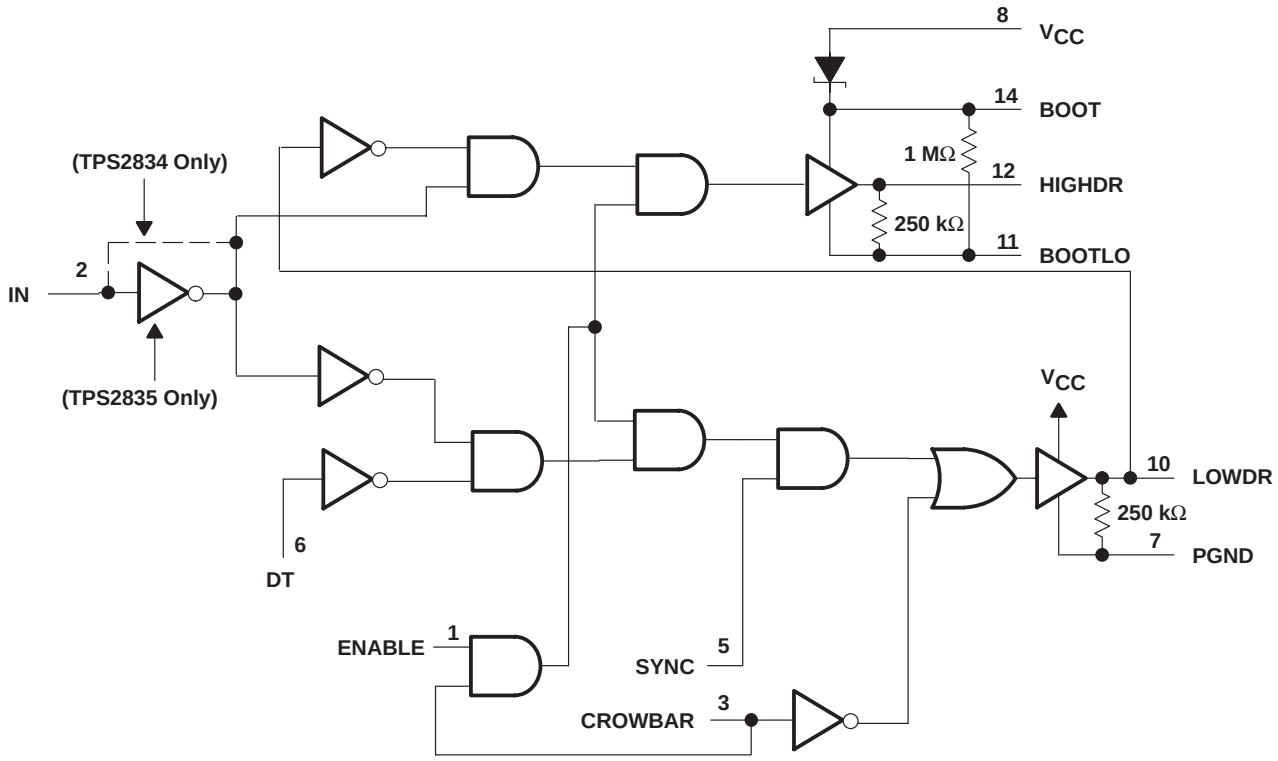
DEVICE NAME	ADDITIONAL FEATURES	INPUTS	
TPS2830	ENABLE, SYNC, and CROWBAR	CMOS	Noninverted
TPS2831			Inverted
TPS2832	W/O ENABLE, SYNC, and CROWBAR	CMOS	Noninverted
TPS2833			Inverted
TPS2836	W/O ENABLE, SYNC, and CROWBAR	TTL	Noninverted
TPS2837			Inverted

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES	
	SOIC (D)	TSSOP (PWP)
− 40°C to 125°C	TPS2834D TPS2835D	TPS2834PWP TPS2835PWP

The D and PWP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2834DR)

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOT	14	I	Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 μF and 1 μF.
BOOTLO	11	O	This terminal connects to the junction of the high-side and low-side MOSFETs.
CROWBAR	3	I	CROWBAR can to be driven by an external OVP circuit to protect against a short across the high-side MOSFET. If CROWBAR is driven low, the low-side driver will be turned on and the high-side driver will be turned off, independent of the status of all other control terminals.
DT	6	I	Dead-time control terminal. Connect DT to the junction of the high-side and low-side MOSFETs.
ENABLE	1	I	If ENABLE is low, both drivers are off.
HIGHDR	12	O	Output drive for the high-side power MOSFET
IN	2	I	Input signal to the MOSFET drivers (noninverting input for the TPS2834; inverting input for the TPS2835).
LOWDR	10	O	Output drive for the low-side power MOSFET
NC	4, 9, 13		No internal connection
PGND	7		Power ground. Connect to the FET power ground.
SYNC	5	I	Synchronous rectifier enable terminal. If SYNC is low, the low-side driver is always off; If SYNC is high, the low-side driver provides gate drive to the low-side MOSFET.
V_{CC}	8	I	Input supply. Recommended that a 1-μF capacitor be connected from V_{CC} to PGND.

detailed description

low-side driver

The low-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

high-side driver

The high-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

dead-time (DT) control

Dead-time control prevents shoot-through current from flowing through the main power FETs during switching transitions by controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (Vdrain) is low; the TTL-compatible DT terminal connects to the junction of the power FETs.

ENABLE

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low. ENABLE is a TTL-compatible digital terminal.

IN

The IN terminal is a TTL-compatible digital terminal that is the input control signal for the drivers. The TPS2834 has a noninverting input; the TPS2835 has an inverting input.

detailed description (continued)

SYNC

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off. SYNC is a TTL-compatible digital terminal.

CROWBAR

The CROWBAR terminal overrides the normal operation of the driver. When CROWBAR is low, the low-side FET turns on to act as a clamp, protecting the output voltage of the dc/dc converter against overvoltages due to a short across the high-side FET. V_{IN} should be fused to protect the low-side FET. CROWBAR is a TTL-compatible digital terminal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 16 V
Input voltage range: BOOT to PGND (high-side driver ON) . . . . . −0.3 V to 30 V
BOOTLO to PGND . . . . . −0.3 V to 16 V
BOOT to BOOTLO . . . . . −0.3 V to 16 V
ENABLE, SYNC, and CROWBAR . . . . . −0.3 V to 16 V
IN . . . . . −0.3 V to 16 V
DT . . . . . −0.3 V to 30 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to PGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP with solder‡	2668	26.68 mW/°C	1467	1067
PWP without solder‡	1024	10.24 mW/°C	563	409
D	749	7.49 mW/°C	412	300

JUNCTION-CASE THERMAL RESISTANCE TABLE

PWP	Junction-case thermal resistance	2.07 °C/W

‡ Test Board Conditions:
1. Thickness: 0.062″
2. 3″ × 3″ (for packages <27 mm long)
3. 4″ × 4″ (for packages >27 mm long)
4. 2-oz copper traces located on the top of the board (0.071 mm thick)
5. Copper areas located on the top and bottom of the PCB for soldering
6. Power and ground planes, 1-oz copper (0.036 mm thick)
7. Thermal vias, 0.33 mm diameter, 1.5 mm pitch
8. Thermal isolation of power plane

For more information, refer to TI technical brief literature number SLMA002.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		15	V
Input voltage	BOOT to PGND	4.5		28	V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range			4.5		15	V
V_{CC}	Quiescent current	$V_{(ENABLE)}$ = LOW,	V_{CC} =15 V			100	µA
		$V_{(ENABLE)}$ = HIGH,	V_{CC} =15 V		300	400	µA
		$V_{(ENABLE)}$ = HIGH, $f_{(SWX)}$ = 200 kHz, $C_{(HIGHDR)}$ = 50 pF, See Note 2	V_{CC} =12 V, BOOTLO grounded, $C_{(LOWDR)}$ = 50 pF,		3		mA

NOTE 2: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

output drivers

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current	High-side sink (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$ = 4 V	0.7	1.1		A
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$ = 5 V	1.1	1.5		
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ = 10.5 V	2	2.4		
	High-side source (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$ = 0.5V	1.2	1.4		A
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$ = 1.5 V	1.3	1.6		
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ = 1.5 V	2.3	2.7		
	Low-side sink (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	V_{CC} = 4.5 V, $V_{(LOWDR)}$ = 4 V	1.3	1.8		A
			V_{CC} = 6.5 V, $V_{(LOWDR)}$ = 5 V	2	2.5		
			V_{CC} = 12 V, $V_{(LOWDR)}$ = 10.5 V	3	3.5		
	Low-side source (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	V_{CC} = 4.5 V, $V_{LOWDR))}$ = 0.5V	1.4	1.7		A
			V_{CC} = 6.5 V, $V_{(LOWDR))}$ = 1.5 V	2	2.4		
			V_{CC} = 12 V, $V_{(LOWDR0)}$ = 1.5 V	2.5	3		
Output resistance	High-side sink (see Note 3)		$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$= 0.5 V			5	Ω
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$ = 0.5 V			5	
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ = 0.5 V			5	
	High-side source (see Note 3)		$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$ = 4 V			75	Ω
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$= 6 V			75	
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ =11.5 V			75	
	Low-side sink (see Note 3)		$V_{(DRV)}$ = 4.5 V, $V_{(LOWDR)}$= 0.5 V			9	Ω
			$V_{(DRV)}$ = 6.5 V, $V_{(LOWDR)}$ = 0.5 V			7.5	
			$V_{(DRV)}$ = 12 V, $V_{(LOWDR)}$ = 0.5 V			6	
	Low-side source (see Note 3)		$V_{(DRV)}$ = 4.5 V, $V_{(LOWDR)}$ = 4 V			75	Ω
			$V_{(DRV)}$ = 6.5 V, $V_{(LOWDR)}$= 6 V			75	
			$V_{(DRV)}$ = 12 V, $V_{(LOWDR)}$ = 11.5 V			75	

NOTES: 2: Ensured by design, not production tested.

3. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $r_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

dead-time control

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	LOWDR	Over the V_{CC} range (see Note 2)	$0.7V_{CC}$			V
V_{IL}	Low-level input voltage					1	
V_{IH}	High-level input voltage	DT	Over the V_{CC} range	2			V
V_{IL}	Low-level input voltage					1	V

NOTE 2: Ensured by design, not production tested.

digital control terminals (IN, CROWBAR, SYNC, ENABLE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Over the V_{CC} range	2			V
V_{IL}	Low-level input voltage				1	V

switching characteristics over recommended operating virtual junction temperature range, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rise time	HIGHDR output (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			60	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			50	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			50	
	LOWDR output (see Note 2)	V_{CC} = 4.5 V			40	ns
		V_{CC} = 6.5 V			30	
		V_{CC} = 12 V			30	
Fall time	HIGHDR output (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			50	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			40	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			40	
	LOWDR output (see Note 2)	V_{CC} = 4.5 V			40	ns
		V_{CC} = 6.5 V			30	
		V_{CC} = 12 V			30	
Propagation delay time	HIGHDR going low (excluding dead time) (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			95	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			80	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			70	
	LOWDR going high (excluding dead time) (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			80	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			70	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			60	
Propagation delay time	LOWDR going low (excluding dead time) (see Note 2)	V_{CC} = 4.5 V			80	ns
		V_{CC} = 6.5 V			70	
		V_{CC} = 12 V			60	
Driver nonoverlap time	DT to LOWDR and LOWDR to HIGHDR (see Note 2)	V_{CC} = 4.5 V	40		170	ns
		V_{CC} = 6.5 V	25		135	
		V_{CC} = 12 V	15		85	

NOTE 2: Ensured by design, not production tested.

TYPICAL CHARACTERISTICS

RISE TIME
vs
SUPPLY VOLTAGE

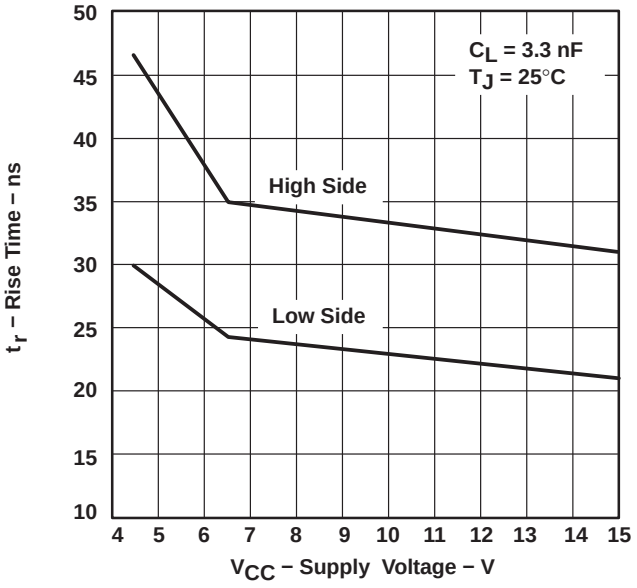


Figure 1

FALL TIME
vs
SUPPLY VOLTAGE

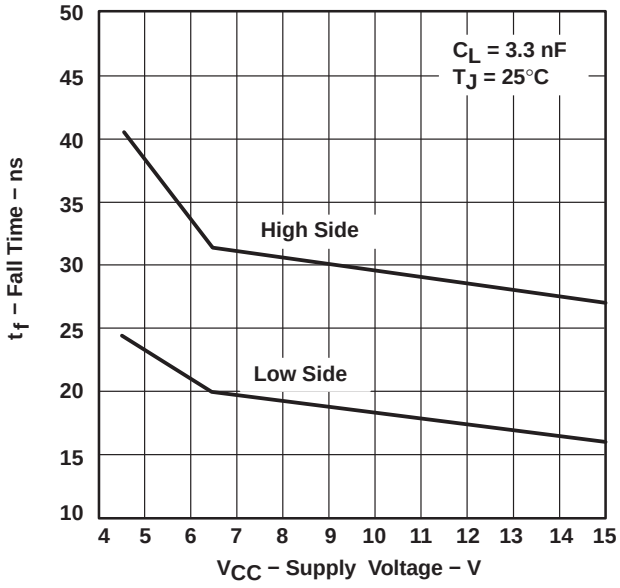


Figure 2

RISE TIME
vs
JUNCTION TEMPERATURE

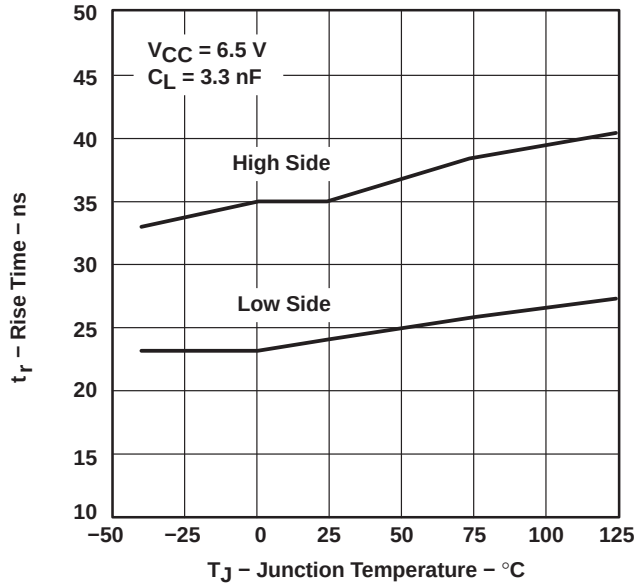


Figure 3

FALL TIME
vs
JUNCTION TEMPERATURE

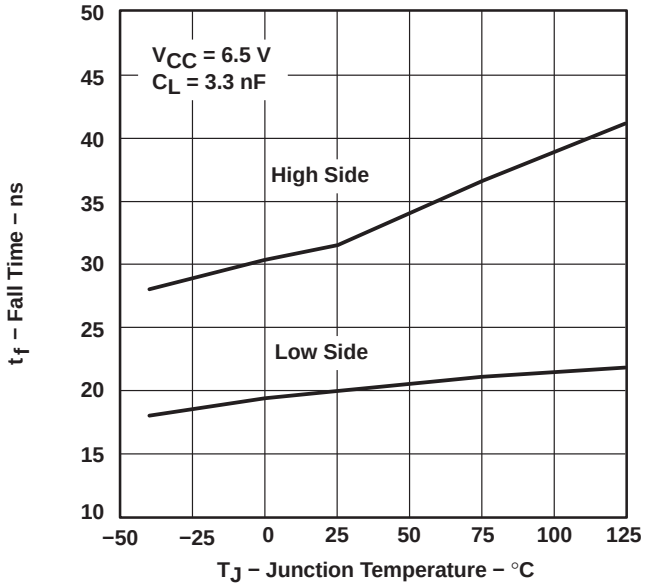


Figure 4

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, LOW TO HIGH LEVEL

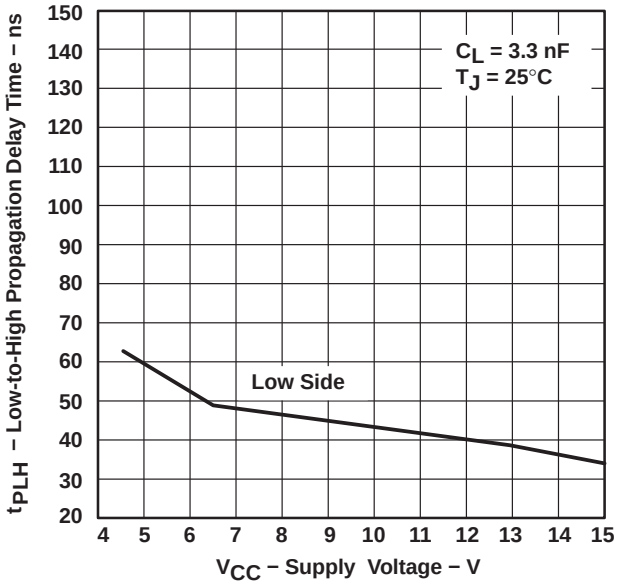


Figure 5

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, HIGH TO LOW LEVEL

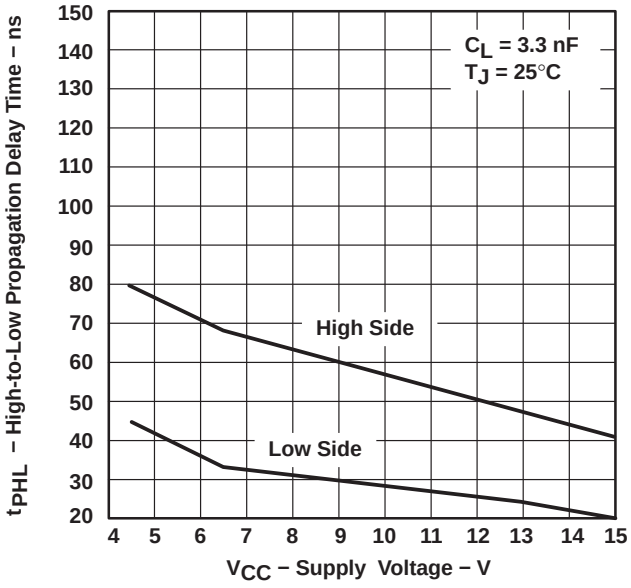


Figure 6

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

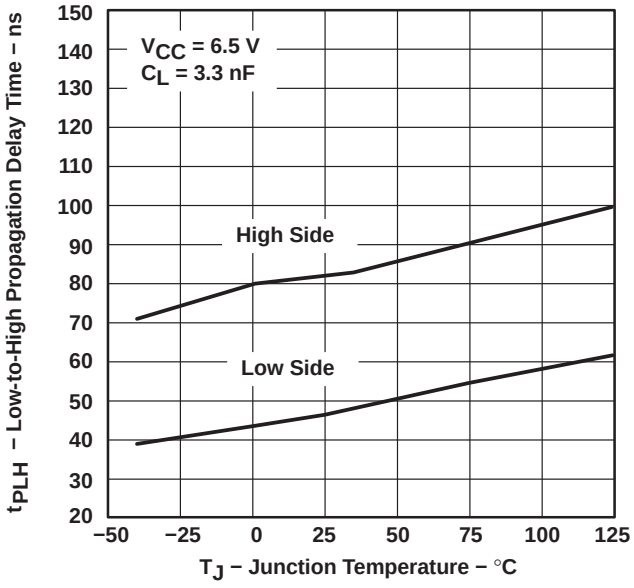


Figure 7

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

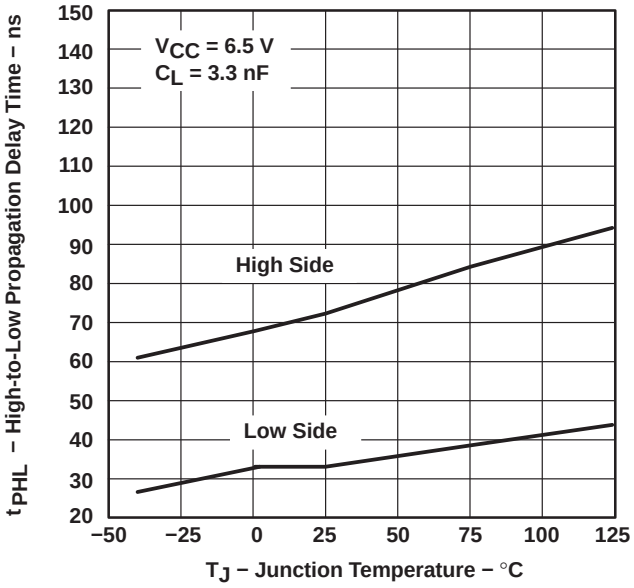


Figure 8

TYPICAL CHARACTERISTICS

DRIVER-OUTPUT RISE TIME
vs
LOAD CAPACITANCE

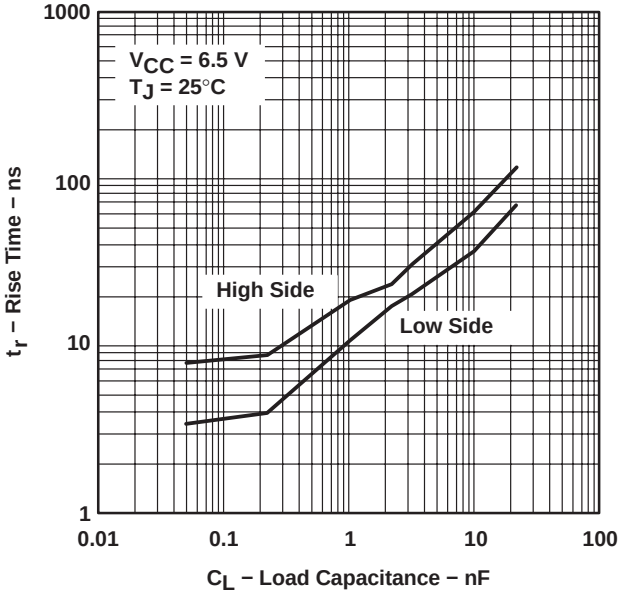


Figure 9

DRIVER-OUTPUT FALL TIME
vs
LOAD CAPACITANCE

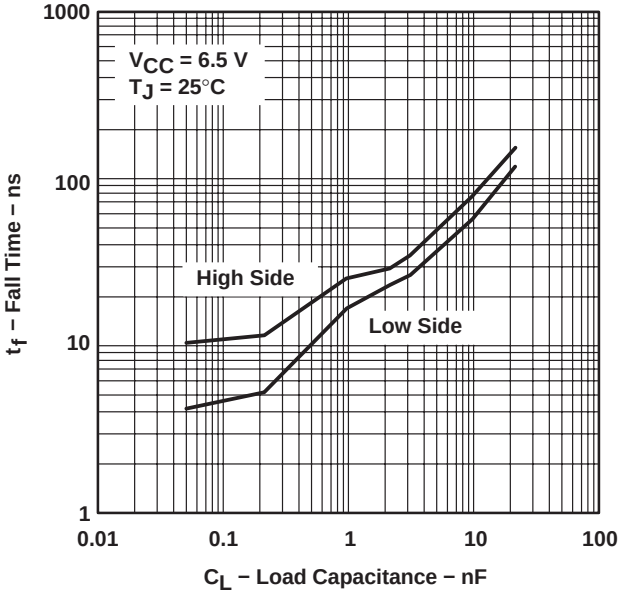


Figure 10

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

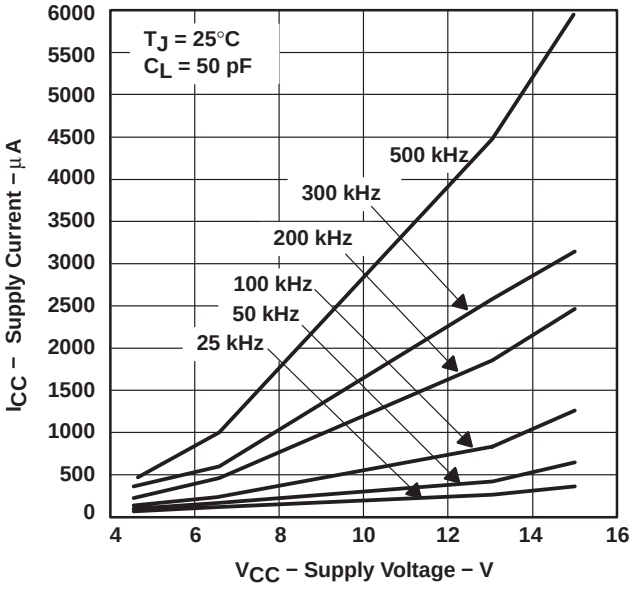


Figure 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

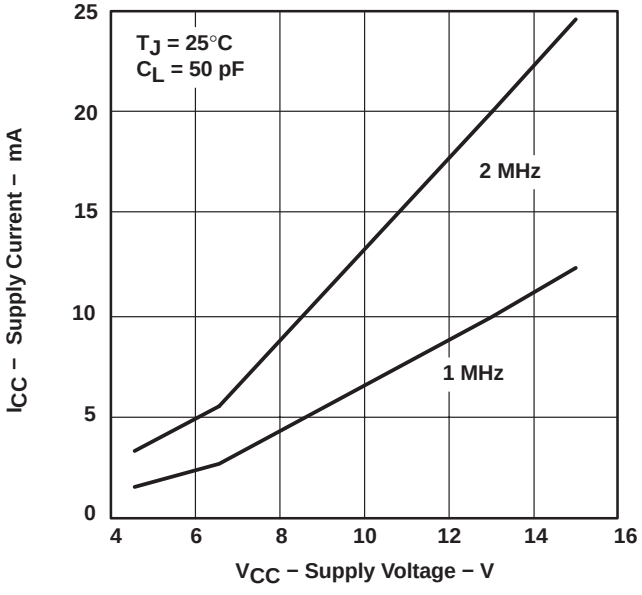


Figure 12

TYPICAL CHARACTERISTICS

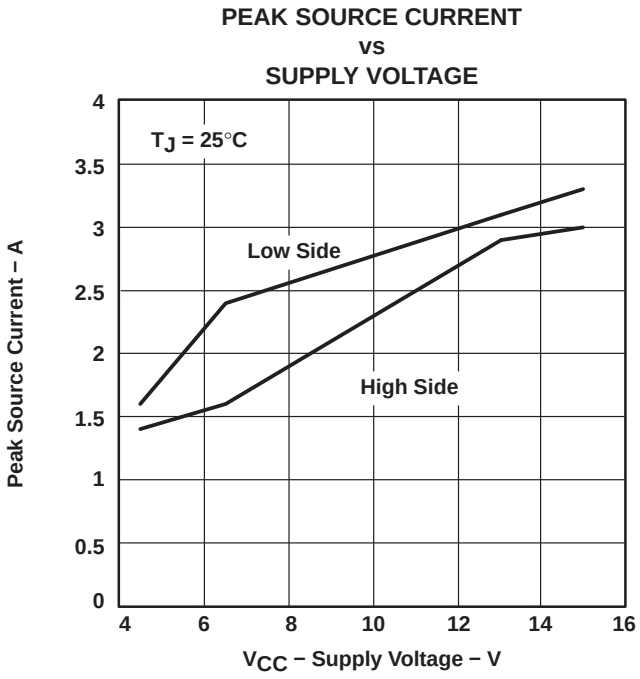


Figure 13

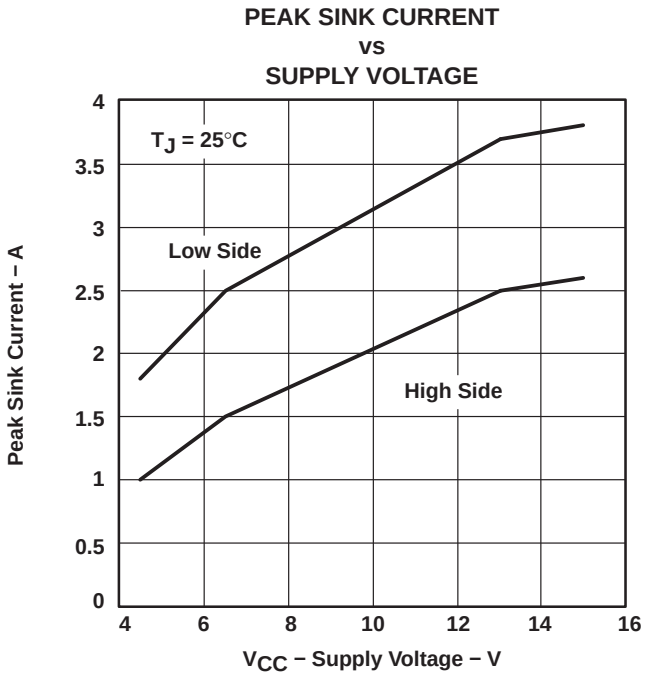


Figure 14

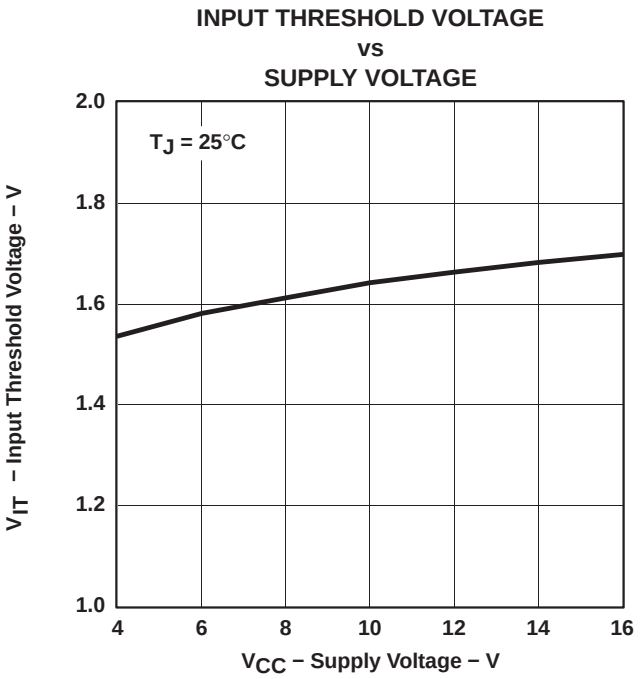


Figure 15

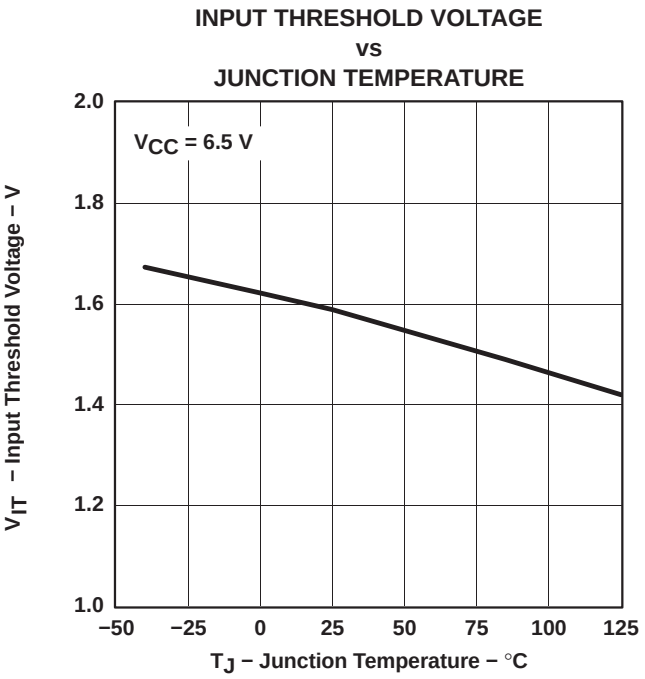


Figure 16

APPLICATION INFORMATION

Figure 17 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2835 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3 A continuous load. The converter achieves an efficiency of 94% for V_{IN} = 5 V, I_{load}=1 A, and 93% for V_{IN} = 5 V, I_{load} = 3 A.

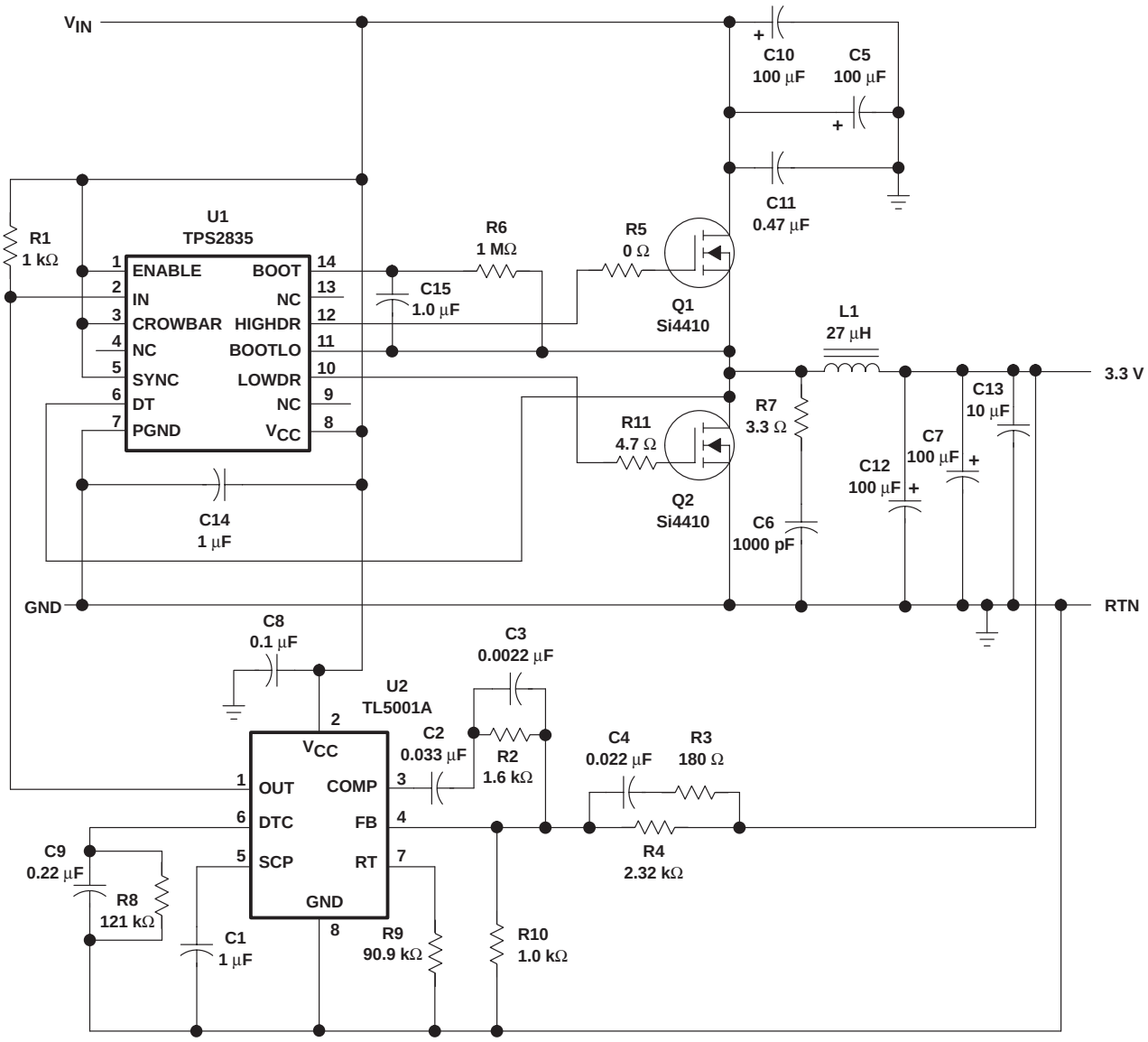


Figure 17. 3.3-V 3-A Synchronous-Buck Converter Circuit

APPLICATION INFORMATION

Great care should be taken when laying out the PC board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A). This node is very sensitive to noise pickup and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have other EMI problems and the power supply will be relatively free of noise.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2834D	NRND	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2834
TPS2834D.A	NRND	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2834
TPS2834DR	NRND	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2834
TPS2834DR.A	NRND	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2834
TPS2834PWP	NRND	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2834
TPS2834PWP.A	NRND	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2834
TPS2834PWPR	NRND	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2834
TPS2834PWPR.A	NRND	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2834
TPS2835D	NRND	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2835
TPS2835D.A	NRND	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2835
TPS2835PWP	NRND	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2835
TPS2835PWP.A	NRND	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2835

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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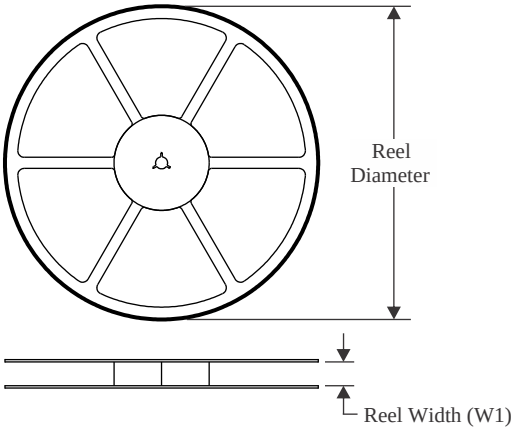
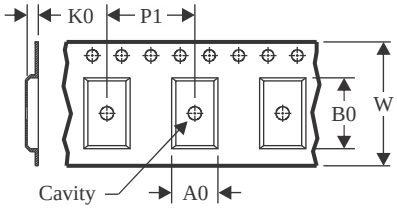
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

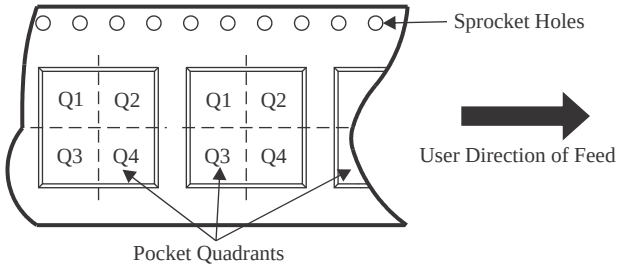


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

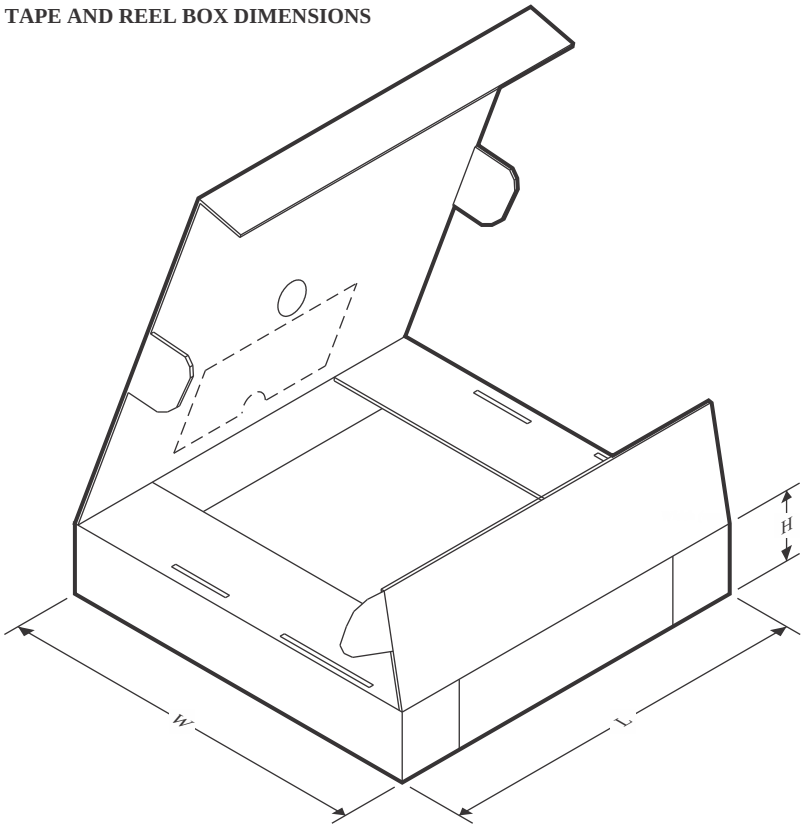
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2834DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TPS2834PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

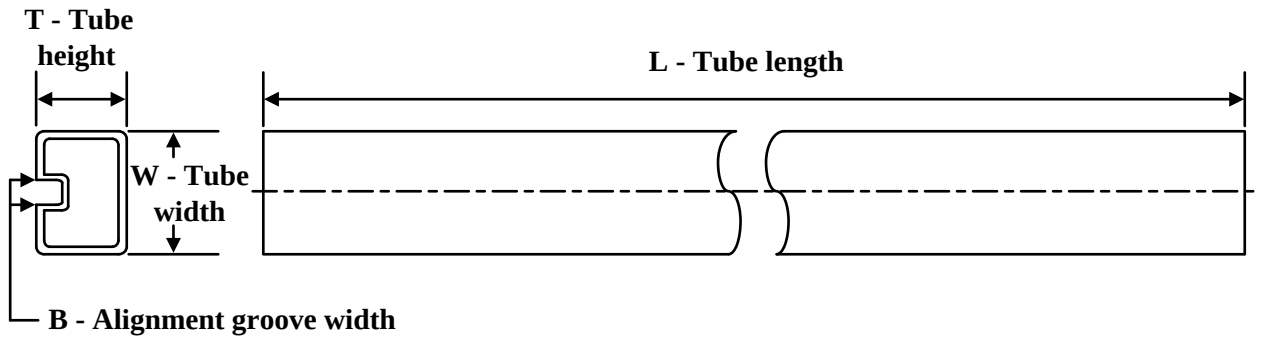
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

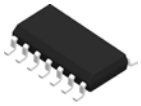
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2834DR	SOIC	D	14	2500	350.0	350.0	43.0
TPS2834PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2834D	D	SOIC	14	50	505.46	6.76	3810	4
TPS2834D.A	D	SOIC	14	50	505.46	6.76	3810	4
TPS2834PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2834PWP.A	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2835D	D	SOIC	14	50	505.46	6.76	3810	4
TPS2835D.A	D	SOIC	14	50	505.46	6.76	3810	4
TPS2835PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2835PWP.A	PWP	HTSSOP	14	90	530	10.2	3600	3.5

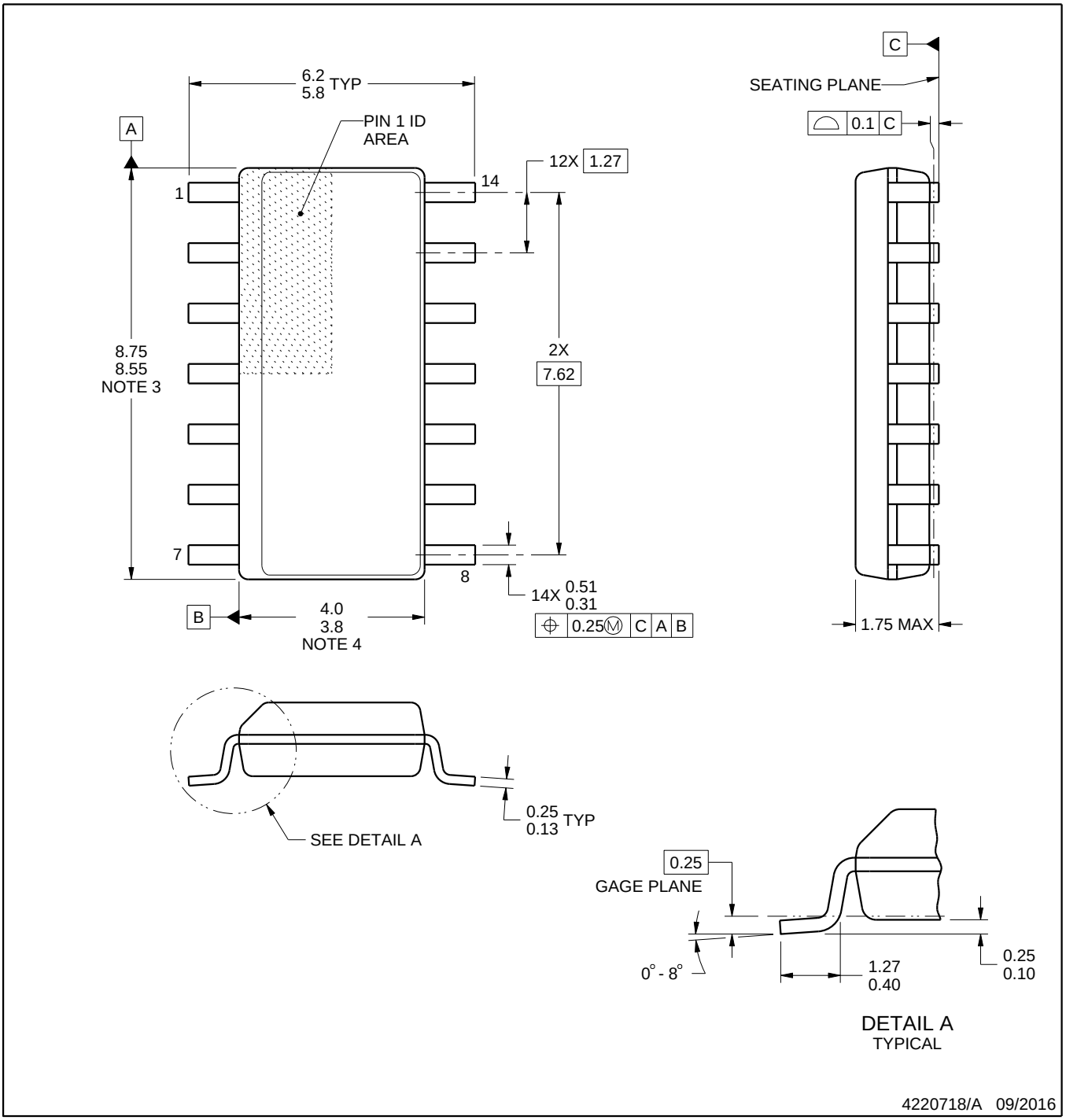


PACKAGE OUTLINE

D0014A

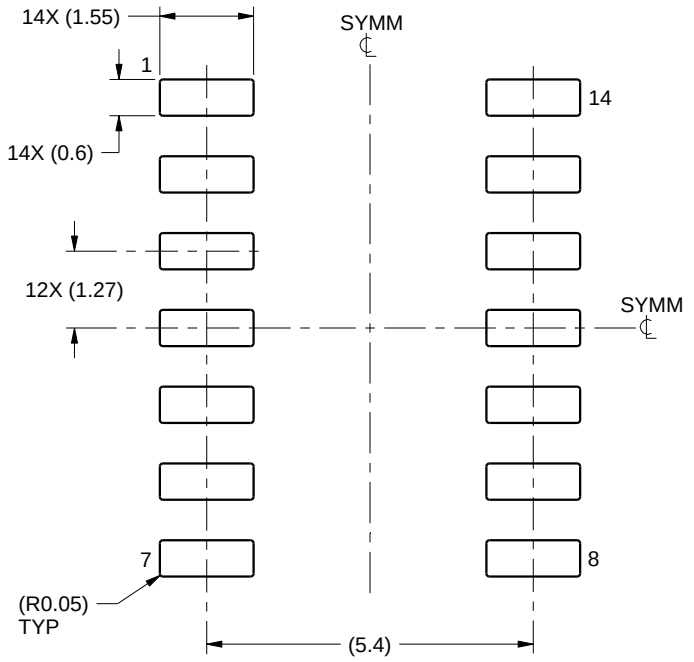
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

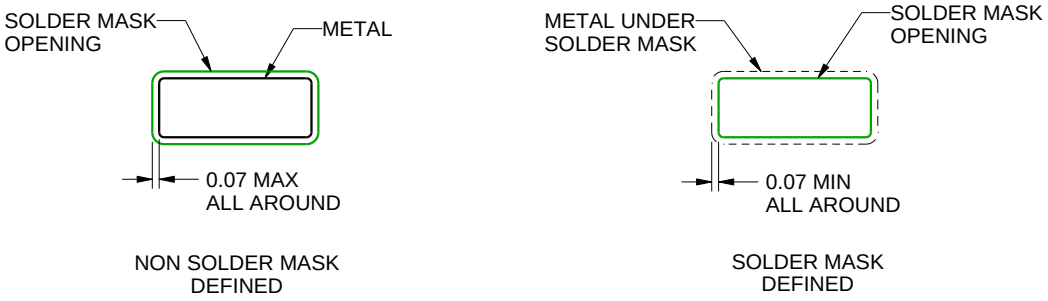


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

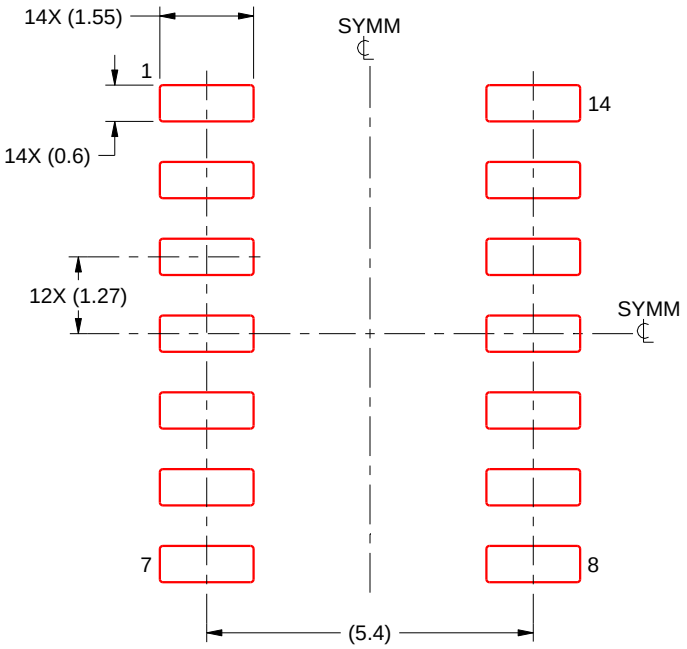
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

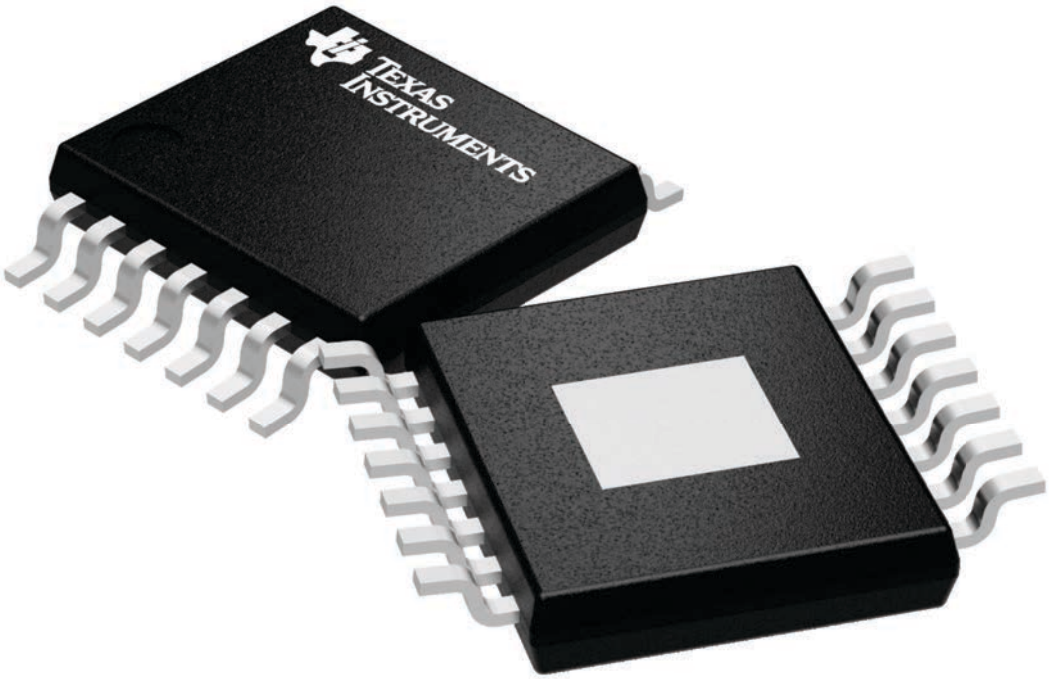
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



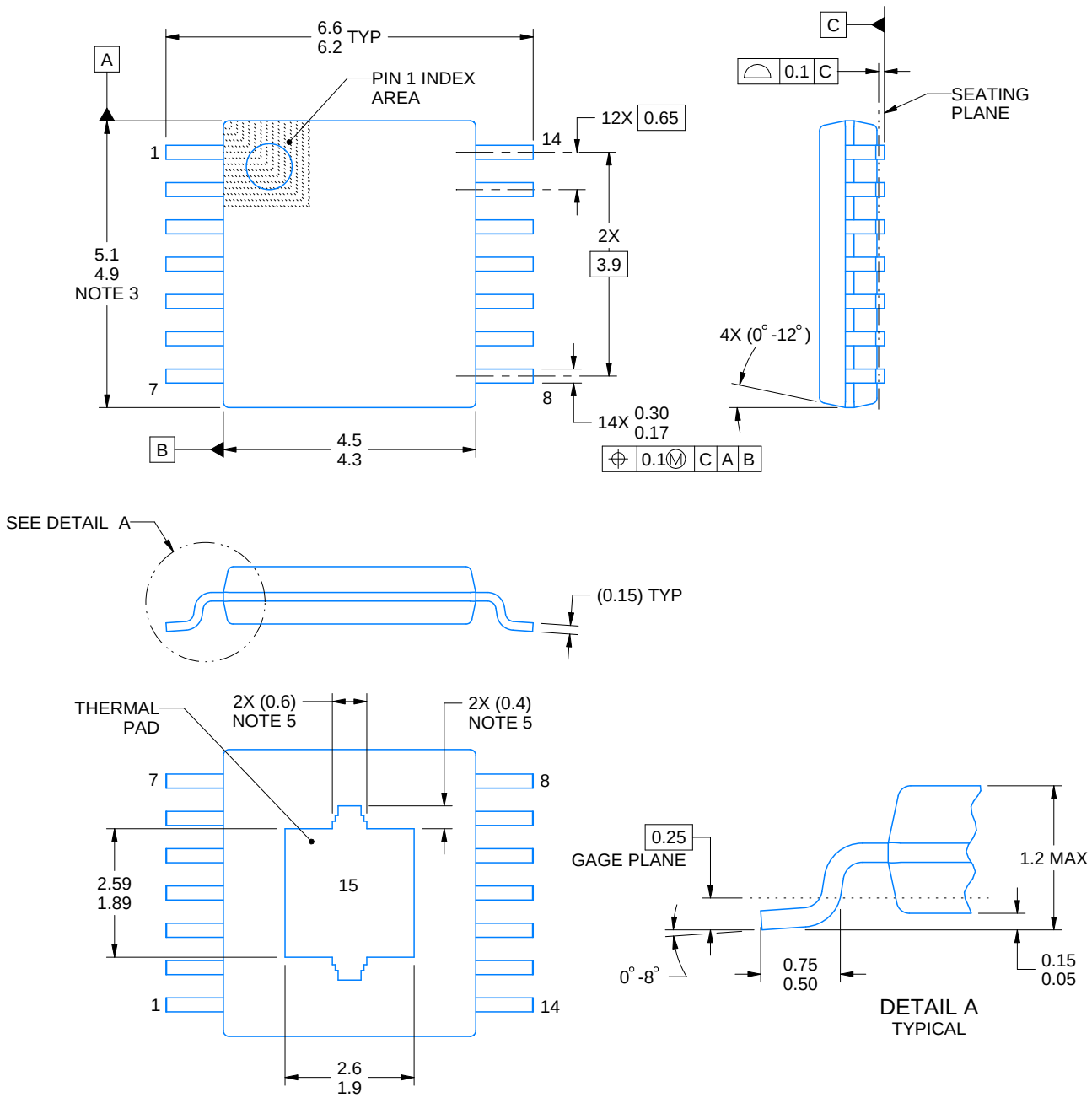
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

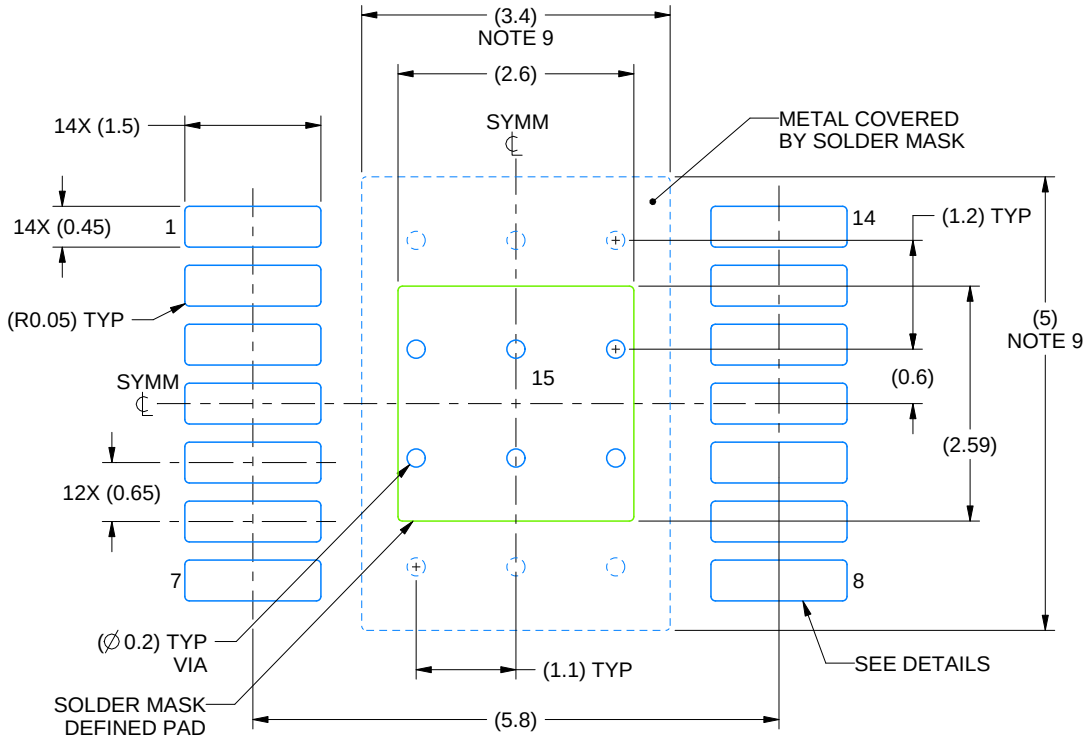
SMALL OUTLINE PACKAGE



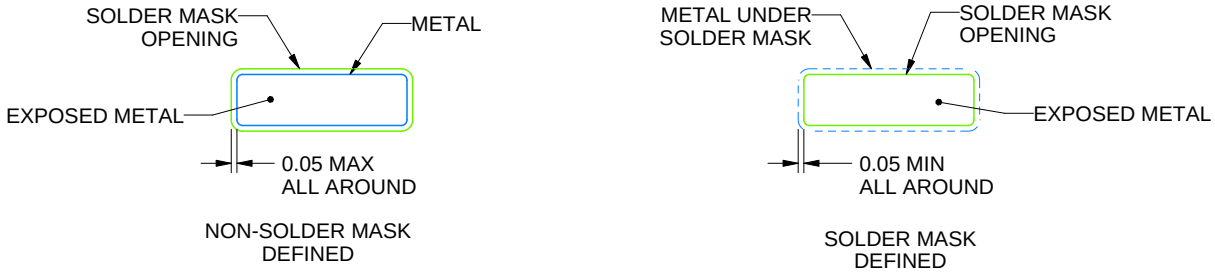
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

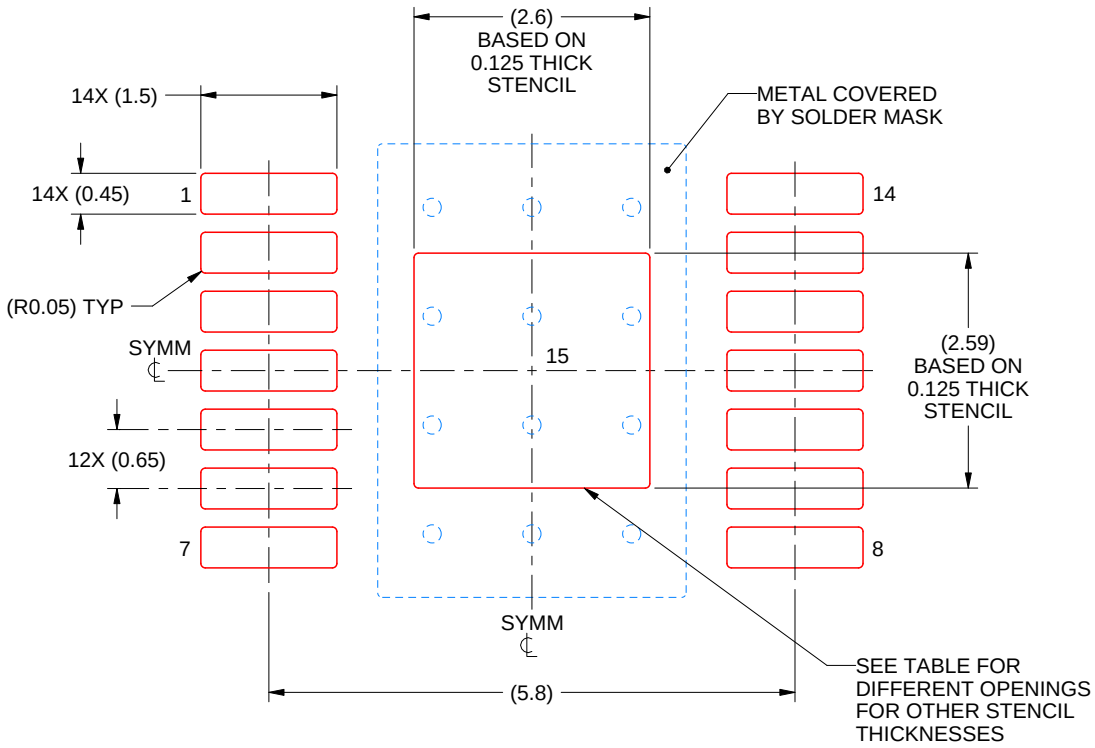


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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