TPS25924x 12-V eFuse with Over Voltage Protection and Blocking FET Control

1 Features

- $V_{OPERATING}$ = 4.5 V to 13.8 V, V_{ABSMAX} = 20 V
- Integrated 28-mΩ Pass MOSFET
- Fixed 15-V Over Voltage Clamp
- 1-A to 5-A Adjustable I_{LIMIT}
- ±8% I_{LIMIT} Accuracy at 3.7 A
- Reverse Current Blocking Support
- Programmable OUT Slew Rate, UVLO
- Built-in Thermal Shutdown
- UL 2367 Recognized – File No. E339631*
  - *RILIM ≤ 130 kΩ (5 A maximum)
- Safe During Single Point Failure Test (UL60950)
- Small Foot Print – 10L (3 mm x 3 mm) VSON

2 Applications

- Adapter Powered Devices
- HDD and SSD Drives
- Set Top Boxes
- Servers / AUX Supplies
- Fan Control
- PCI/PCIe Cards

3 Description

The TPS25924x family of eFuses is a highly integrated circuit protection and power management solution in a tiny package. The devices use few external components and provide multiple protection modes. They are a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current, and reverse current.

Current limit level can be set with a single external resistor. Over voltage events are limited by internal clamping circuits to a safe fixed maximum, with no external components required.

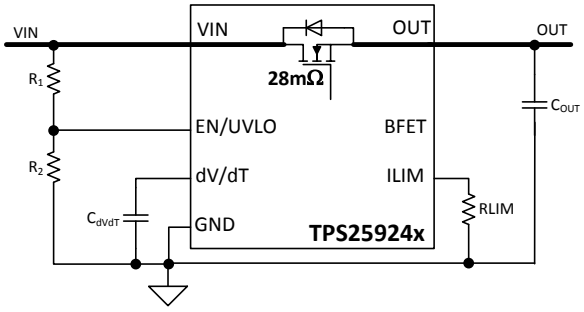
Applications with particular voltage ramp requirements can set dV/dT with a single capacitor to ensure proper output ramp rates. Many systems, such as SSDs, must not allow holdup capacitance energy to dump back through the FET body diode onto a drooping or shorted input bus. The BFET pin is for such systems. An external NFET can be connected “Back to Back (B2B)” with the TPS25924x output and the gate driven by BFET to prevent current flow from load to source (see Figure 43).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS259241	VSON (10)	3.00 mm × 3.00 mm
TPS259240		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



Transient: Output Short Circuit

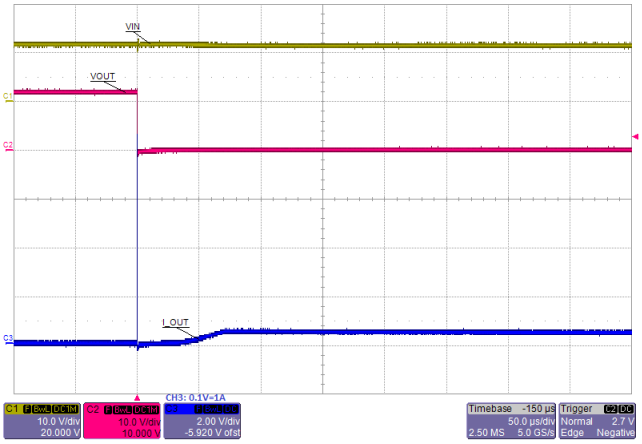


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 5
7.5 Electrical Characteristics ... 5
7.6 Timing Requirements ... 6
7.7 Typical Characteristics ... 7
8 Detailed Description ... 13
8.1 Overview ... 13
8.2 Functional Block Diagram ... 13
8.3 Feature Description ... 13
8.4 Device Functional Modes ... 16
9 Application and Implementation ... 17
9.1 Application Information ... 17
9.2 Typical Applications ... 17
10 Power Supply Recommendations ... 23
10.1 Transient Protection ... 23
10.2 Output Short-Circuit Measurements ... 24
11 Layout ... 25
11.1 Layout Guidelines ... 25
11.2 Layout Example ... 25
12 Device and Documentation Support ... 26
12.1 Device Support ... 26
12.2 Documentation Support ... 26
12.3 Related Links ... 26
12.4 Receiving Notification of Documentation Updates ... 26
12.5 Community Resources ... 26
12.6 Trademarks ... 26
12.7 Electrostatic Discharge Caution ... 26
12.8 Glossary ... 27
13 Mechanical, Packaging, and Orderable Information ... 27

4 Revision History

Changes from Revision A (August 2015) to Revision B **Page**

- Added section: *Controlled Power Down using TPS25924x* ... 22

Changes from Original (August 2015) to Revision A **Page**

- Changed from Product Preview to Production Data ... 1

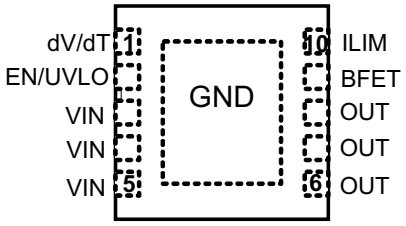
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5 Device Comparison Table

PART NUMBER	UV	OV CLAMP	FAULT RESPONSE	STATUS
TPS259241	4.3 V	15 V	Auto Retry	Active
TPS259240	4.3 V	15 V	Latched	Active

6 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BFET	9	O	Connect this pin to the gate of a blocking NFET. See the *Feature Description* section. This pin can be left floating if it is not used
dV/dT	1	O	Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turnon
EN/UVLO	2	I	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET and pulls BFET to GND. When pulled high, it enables the device and BFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider
GND	Thermal Pad	—	GND
ILIM	10	O	A resistor from this pin to GND sets the overload and short circuit limit
OUT	6-8	O	Output of the device
VIN	3-5	I	Input supply voltage

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
VIN	Supply voltage(1)	–0.3	20	V
VIN (10-ms transient)			22	
OUT	Output voltage	–0.3	VIN + 0.3	V
OUT (transient < 1 µs)			–1.2	V
ILIM	Voltage	–0.3	7	V
EN/UVLO		–0.3	7	
dV/dT		–0.3	7	
BFET		–0.3	30	
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VIN	Input voltage	4.5	12	13.8	V
BFET		0		VIN+6	
dV/dT, EN/UVLO		0		6	
ILIM		0		3	
I_{OUT}	Continuous output current	0		5	A
ILIM	Resistance	10	100	162	kΩ
OUT	External capacitance	0.1	1	1000	µF
dV/dT			1	1000	nF
T_J	Operating junction temperature	–40	25	125	°C
T_A	Operating Ambient temperature	–40	25	85	°C

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7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)(1)

THERMAL METRIC		TPS25924x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

–40°C ≤ T_J ≤ +125°C, VIN = 12 V, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN (INPUT SUPPLY)						
V_{UVR}	UVLO threshold, rising		4.15	4.3	4.45	V
V_{UVhyst}	UVLO hysteresis(1)			5%		
IQ_{ON}	Supply current	Enabled: EN/UVLO = 2 V	0.3	0.42	0.55	mA
IQ_{OFF}		EN/UVLO = 0 V		0.13	0.225	mA
V_{OVC}	Over-voltage clamp	VIN > 16.5 V, I_{OUT} = 10 mA	13.8	15	16.5	V
EN/UVLO (ENABLE/UVLO INPUT)						
V_{ENR}	EN threshold voltage, rising		1.37	1.4	1.44	V
V_{ENF}	EN threshold voltage, falling		1.32	1.35	1.39	V
I_{EN}	EN Input leakage current	0 V ≤ V_{EN} ≤ 5 V	–100	0	100	nA
dV/dT (OUTPUT RAMP CONTROL)						
I_{dVdT}	dV/dT charging current(1)	V_{dVdT} = 0 V		220		nA
R_{dVdT_disch}	dV/dT discharging resistance	EN/UVLO = 0 V, I_{dVdT} = 10 mA sinking	50	73	100	Ω
$V_{dVdTmax}$	dV/dT max capacitor voltage(1)			5.5		V
$GAIN_{dVdT}$	dV/dT to OUT gain(1)	ΔV_{dVdT}		4.85		V/V
ILIM (CURRENT LIMIT PROGRAMMING)						
I_{ILIM}	ILIM bias current(1)			10		µA
I_{OL}	Overload current limit(2)	R_{ILIM} = 10 kΩ, $V_{VIN-OUT}$ = 1 V		1.02		A
		R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 1 V	1.79	2.10	2.42	
		R_{ILIM} = 100 kΩ, $V_{VIN-OUT}$ = 1 V	3.46	3.75	4.03	
		R_{ILIM} = 150 kΩ, $V_{VIN-OUT}$ = 1 V	4.5	5.1	5.7	
$I_{OL-R-Short}$		R_{ILIM} = 0 Ω, shorted resistor current limit (single point failure test: UL60950)(1)		0.84		A
$I_{OL-R-Open}$		R_{ILIM} = OPEN, open resistor current limit (single point failure test: UL60950)(1)		0.73		A
I_{SCL}	Short-circuit current limit(2)	R_{ILIM} = 10 kΩ, $V_{VIN-OUT}$ = 12 V		1		A
		R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 12 V	1.66	1.98	2.37	
		R_{ILIM} = 100 kΩ, $V_{VIN-OUT}$ = 12 V	2.90	3.32	3.85	
		R_{ILIM} = 150 kΩ, $V_{VIN-OUT}$ = 12 V	3.7	4.5	5.5	
$RATIO_{FASTRIP}$	Fast-trip comparator level w.r.t. overload current limit(1)	$I_{FASTRIP}$: I_{OL}		160%		
$V_{OpenILIM}$	ILIM open resistor detect threshold(1)	V_{ILIM} rising, R_{ILIM} = OPEN		3.1		V

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(2) Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ +125°C, VIN = 12 V, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT (PASS FET OUTPUT)						
$R_{DS(on)}$	FET ON resistance	T_J = 25°C	21	28	37	mΩ
		T_J = 125°C		39	48	
$I_{OUT-OFF-LKG}$	OUT bias current in off state	$V_{EN/UVLO}$ = 0 V, V_{OUT} = 0 V (sourcing)	–5	0	1.2	µA
$I_{OUT-OFF-SINK}$		$V_{EN/UVLO}$ = 0 V, V_{OUT} = 300 mV (sinking)	10	15	20	
BFET (BLOCKING FET GATE DRIVER)						
I_{BFET}	BFET charging current(1)	V_{BFET} = V_{OUT}		2		µA
$V_{BFETmax}$	BFET clamp voltage(1)			V_{VIN} + 6.4		V
$R_{BFETdisch}$	BFET discharging resistance to GND	$V_{EN/UVLO}$ = 0 V, I_{BFET} = 100 mA	15	26	36	Ω
TSD (THERMAL SHUT DOWN)						
T_{SHDN}	TSD threshold, rising(1)			150		°C
$T_{SHDNhyst}$	TSD hysteresis(1)			10		°C
	Thermal fault: latched or auto-retry	TPS259240		Latched		
		TPS259241		Auto-retry		

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON}	Turnon delay(1)	EN/UVLO → H to I_{VIN} = 100 mA, 1-A resistive load at OUT		220		µs
t_{OFFdly}	Turnoff delay(1)	EN/UVLO↓ to BFET↓, C_{BFET} = 0		0.4		µs
dV/dT (OUTPUT RAMP CONTROL)						
t_{dVdT}	Output ramp time	EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 0	0.7	1	1.3	ms
		EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 1 nF(1)		12		
ILIM (CURRENT LIMIT PROGRAMMING)						
$t_{FastOffDly}$	Fast-Trip comparator delay(1)	I_{OUT} > $I_{FASTRIP}$ to I_{OUT}= 0 (Switch off)		300		ns
BFET (BLOCKING FET GATE DRIVER)						
$t_{BFET-ON}$	BFET Turnon duration(1)	EN/UVLO → H to V_{BFET} = 12 V, C_{BFET} = 1 nF		4.2		ms
		EN/UVLO → H to VB_{FET} = 12 V, C_{BFET} = 10 nF		42		
$t_{BFET-OFF}$	BFET Turnoff duration(1)	EN/UVLO → L to $_{VBFET}$ = 1 V, C_{BFET} = 1 nF		0.4		µs
		EN/UVLO → L to V_{BFET} = 1 V, C_{BFET} = 10 nF		1.4		
THERMAL SHUTDOWN (TSD)						
t_{TSDdly}	Retry delay after TSD recovery, T_J < [T_{SHDN} - 10°C](1)	TPS259241 only		100		µs

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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7.7 Typical Characteristics

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

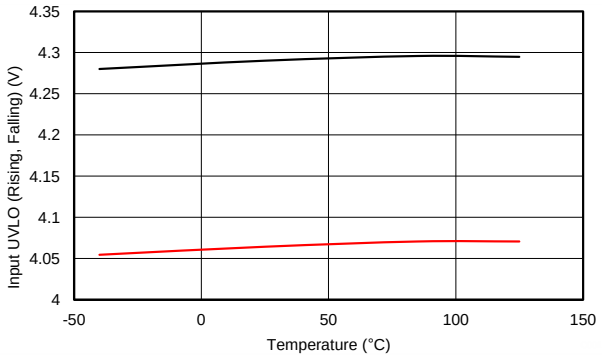


Figure 1. Input UVLO vs Temperature

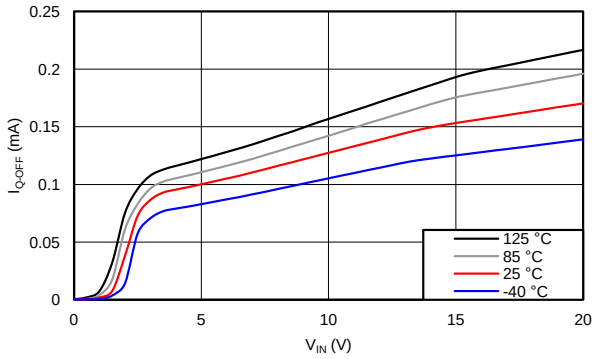


Figure 2. I_{Q-OFF} vs V_{IN}

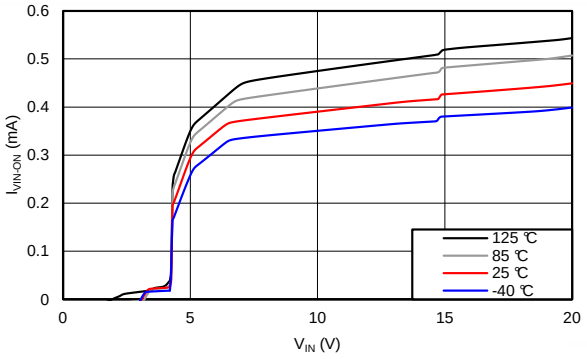


Figure 3. I_{VIN-ON} vs V_{IN}

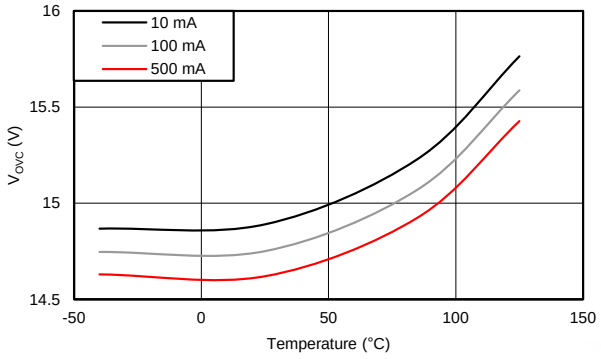


Figure 4. V_{OVC} vs Temperature Across I_{OUT}

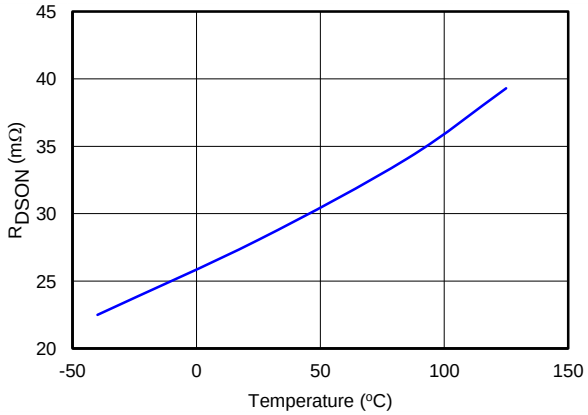


Figure 5. R_{DSON} vs Temperature

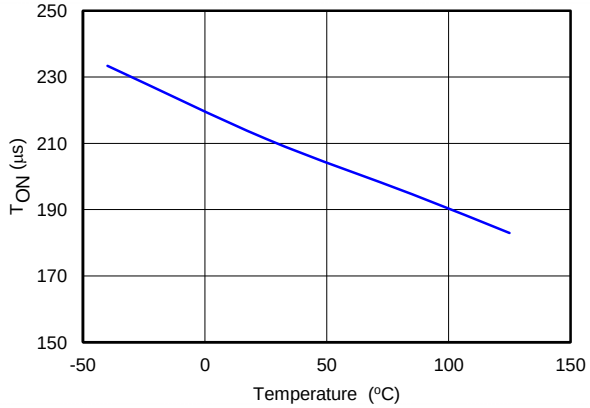


Figure 6. T_{ON} vs Temperature

Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

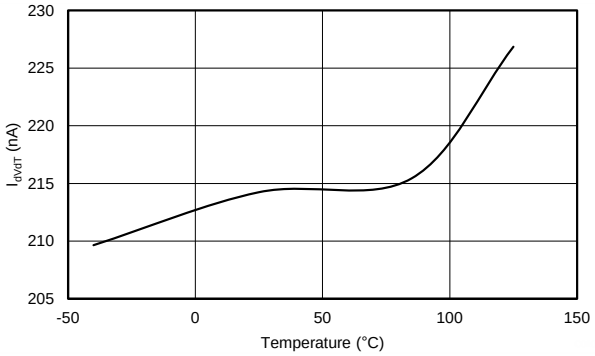


Figure 7. I_{dVdT} vs Temperature

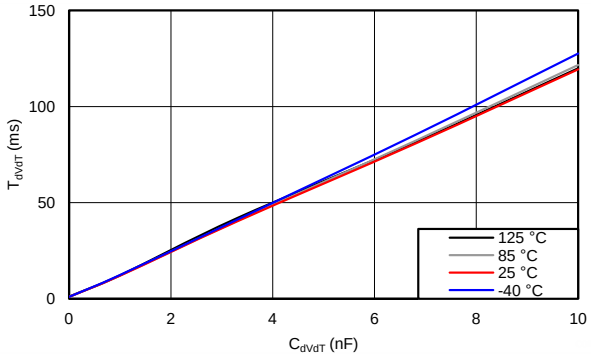


Figure 8. T_{dVdT} vs C_{dVdT}

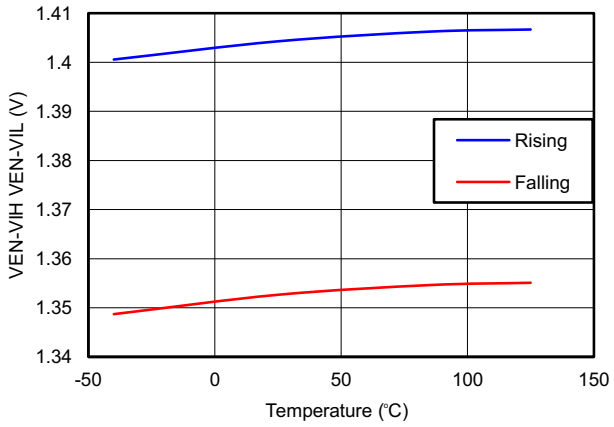


Figure 9. V_{EN-VIH}, V_{EN-VIL} vs Temperature

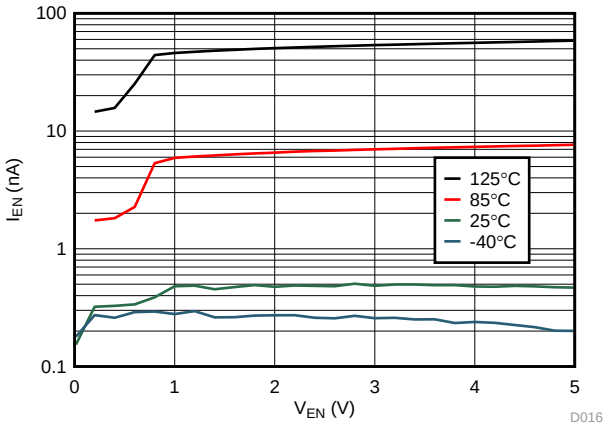
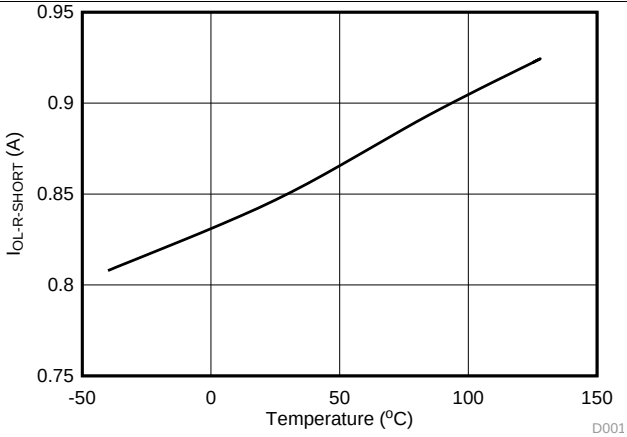
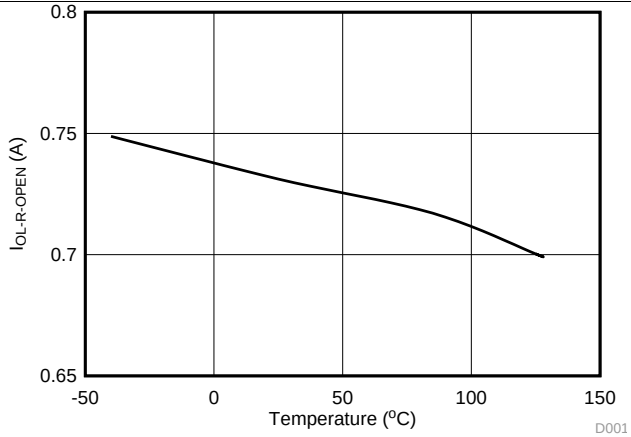


Figure 10. I_{EN} (Leakage Current) vs V_{EN}



R_{ILIM} = 0 Ω

Figure 11. $I_{OL-R-Short}$ vs Temperature



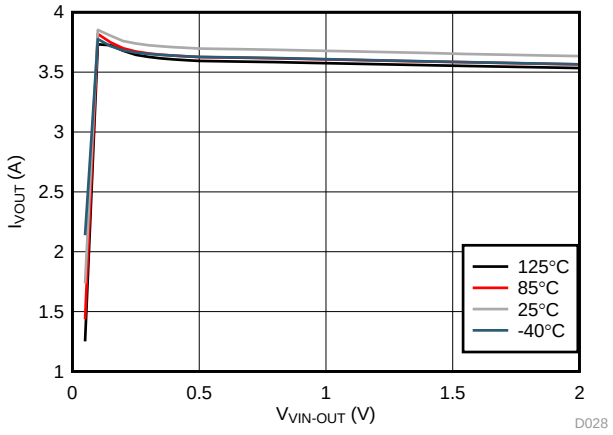
R_{ILIM} = OPEN

Figure 12. $I_{OL-R-Open}$ vs Temperature

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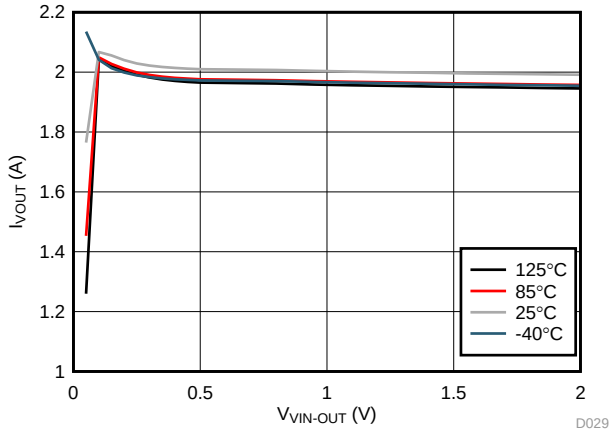
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)



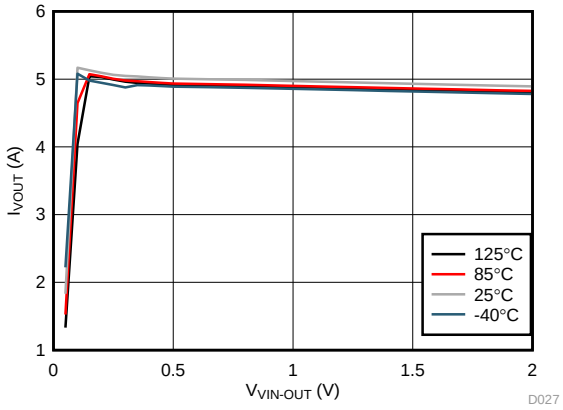
R_{ILIM} = 100 kΩ

Figure 13. I_{VOUT} vs $V_{VIN-OUT}$



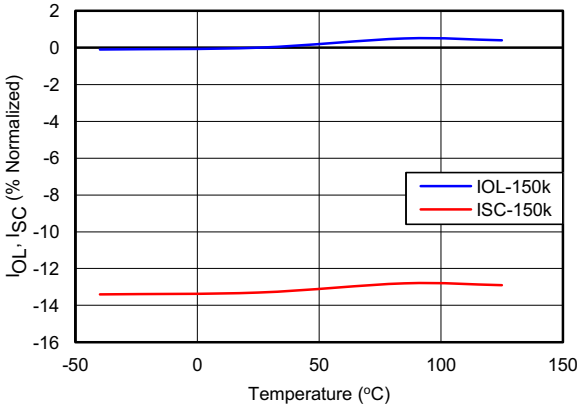
R_{ILIM} = 45.3 kΩ

Figure 14. I_{VOUT} vs $V_{VIN-OUT}$



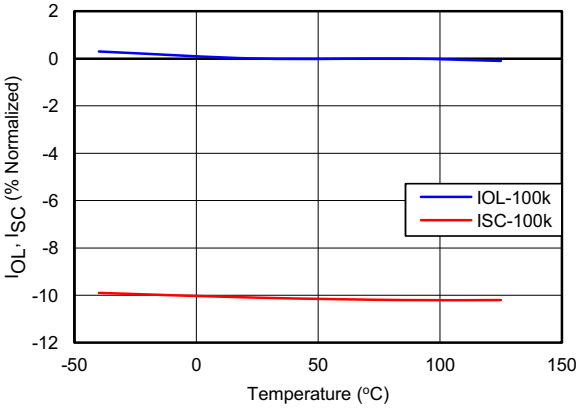
R_{ILIM} = 150 kΩ

Figure 15. I_{VOUT} vs $V_{VIN-OUT}$



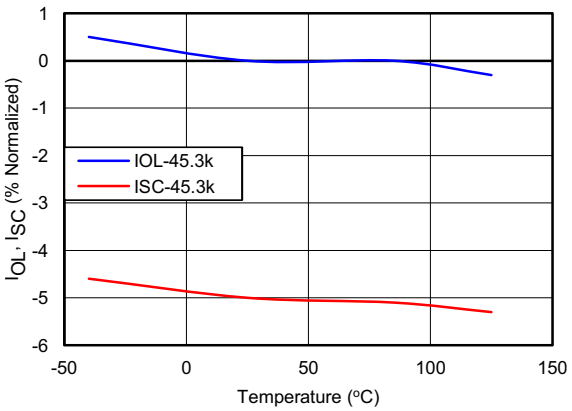
R_{ILIM} = 150 kΩ

Figure 16. I_{OL}, I_{SC} vs Temperature



R_{ILIM} = 100 kΩ

Figure 17. I_{OL}, I_{SC} vs Temperature



R_{ILIM} = 45.3 kΩ

Figure 18. I_{OL}, I_{SC} vs Temperature

Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

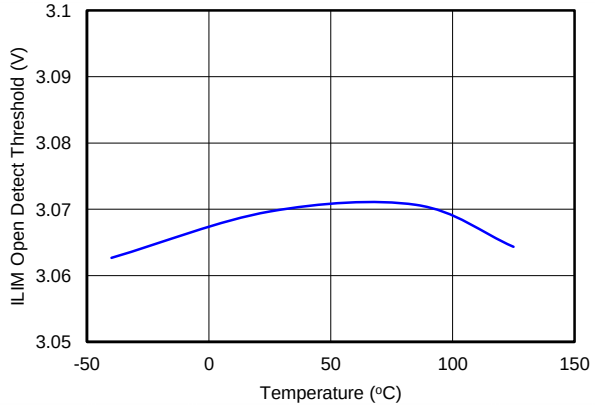


Figure 19. $V_{OpenILIM}$ vs Temperature

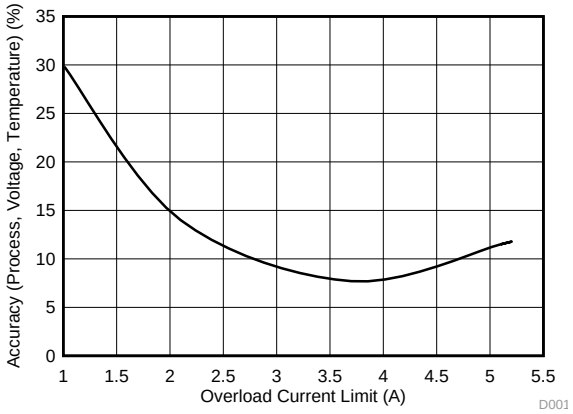


Figure 20. Accuracy vs Overload Current Limit

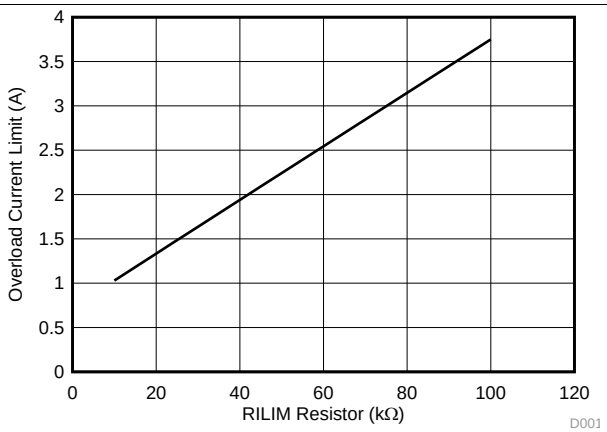


Figure 21. Overload Current Limit vs RILIM Resistor

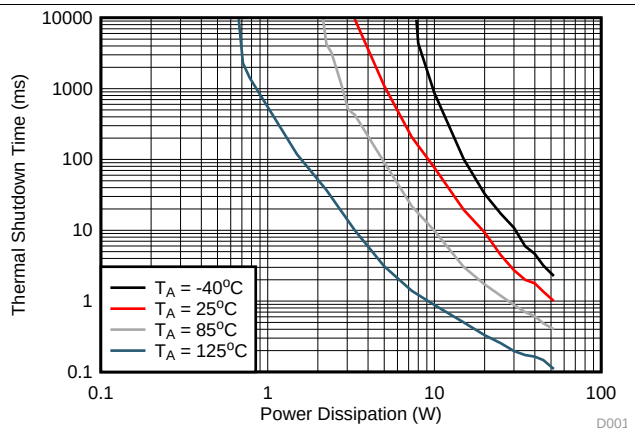


Figure 22. Thermal Shutdown Time vs Power Dissipation

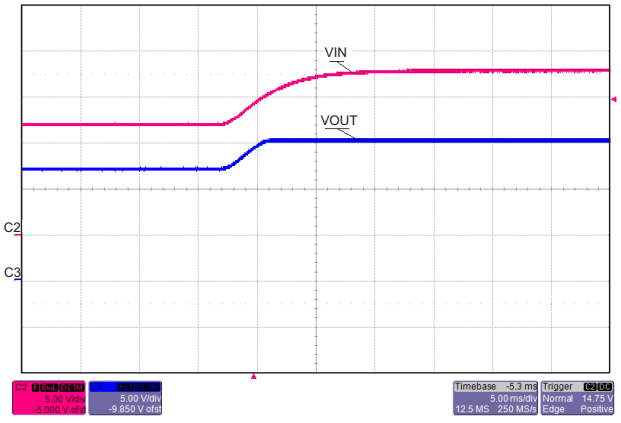
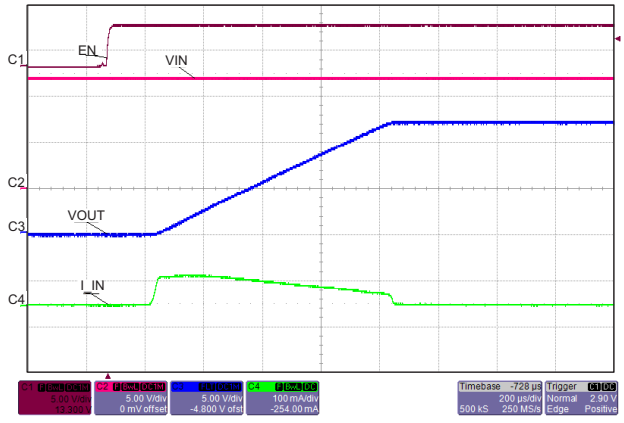


Figure 23. Transient: Over-Voltage Clamp



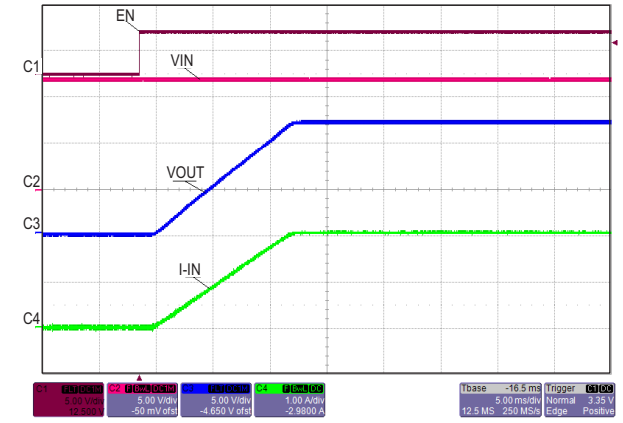
C_{dVdT} = OPEN, C_{OUT} = 4.7 µF

Figure 24. Transient: Output Ramp

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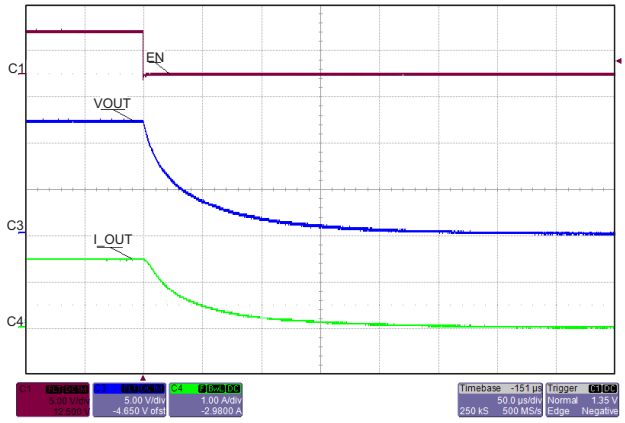
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)



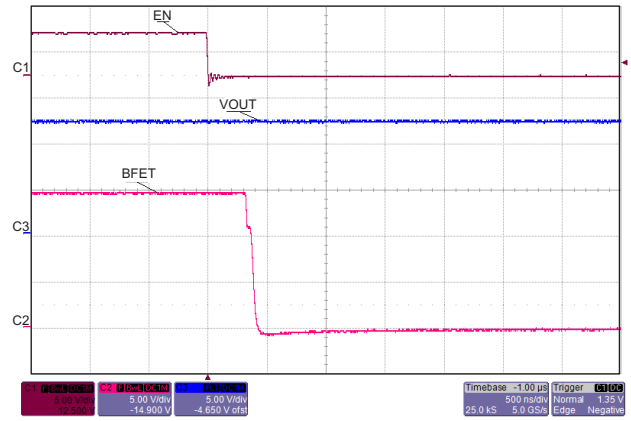
C_{dVdT} = 1nF, C_{OUT} = 10 µF, R_{OUT} = 5.7Ω

Figure 25. Transient: Output Ramp



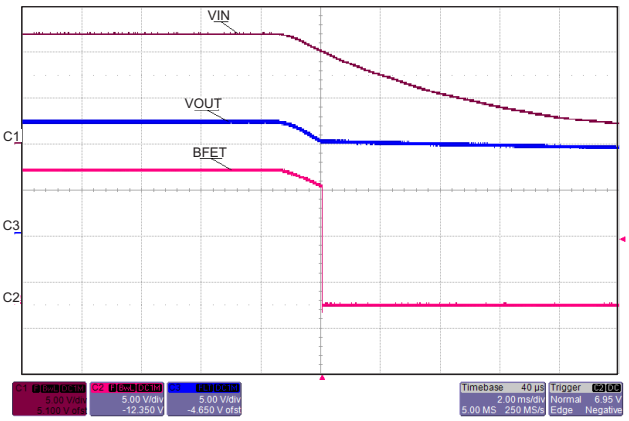
EN ↓

Figure 26. Transient: Turnoff Delay



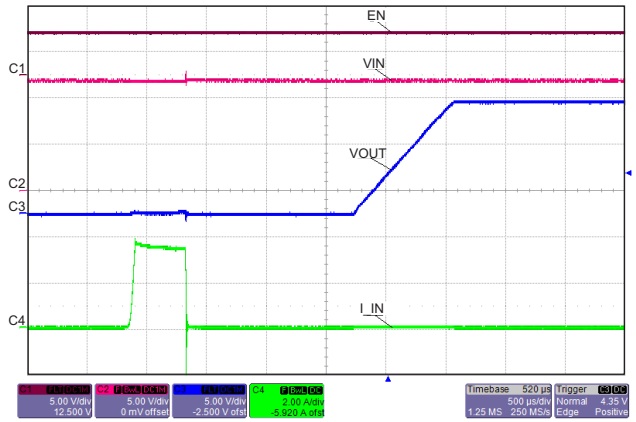
EN ↓

Figure 27. Turnoff Delay to BFET



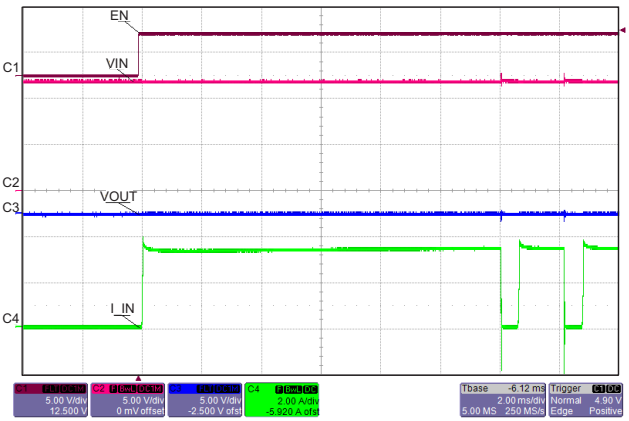
VIN↓

Figure 28. Turnoff Delay to BFET



TPS259241

Figure 29. Transient: Recovery From Short Circuit / Over Current

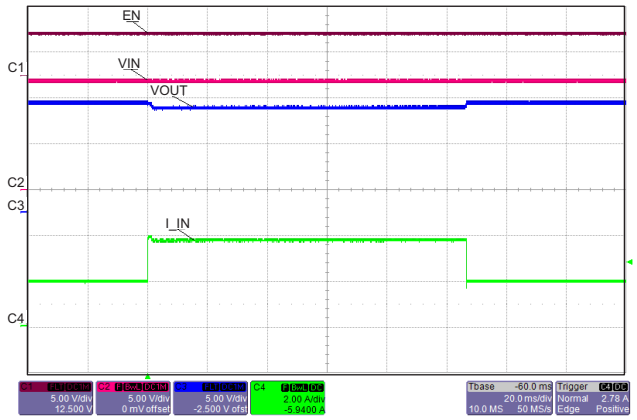


TPS259241

Figure 30. Transient: Wake Up to Short Circuit

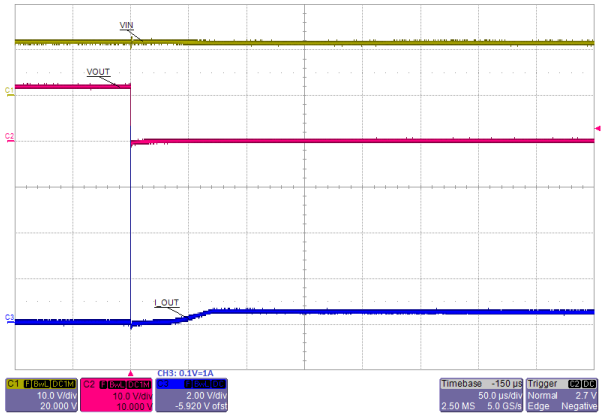
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)



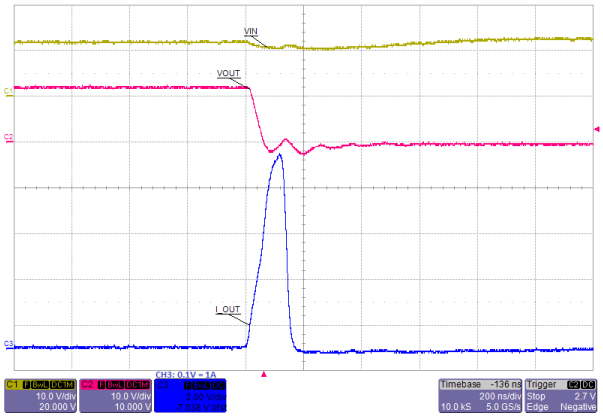
I_{LOAD} Stepped From 50% to 120%, back to 50%

Figure 31. Transient: Overload Current Limit



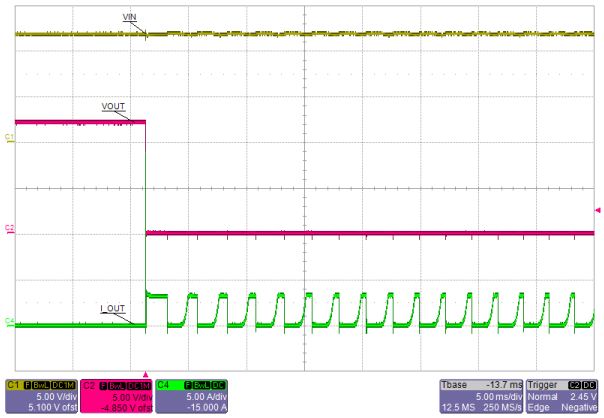
R_{ILIM} = 150 kΩ

Figure 32. Transient: Output Short Circuit



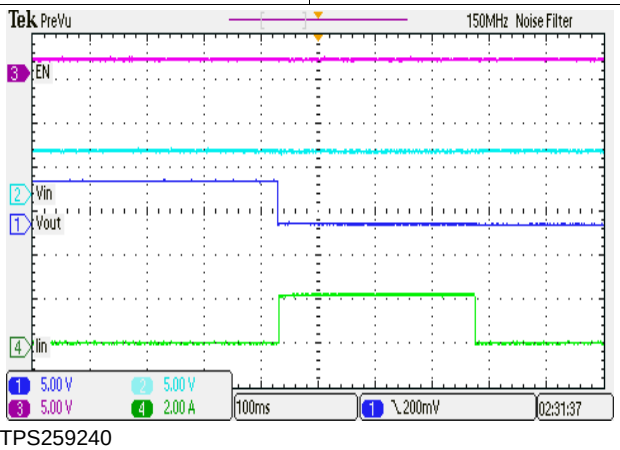
R_{ILIM} = 150 kΩ

Figure 33. Short Circuit (Zoom): Fast-Trip Comparator



TPS259241

Figure 34. Transient: Thermal Fault Auto-Retry



TPS259240

Figure 35. Transient: Thermal Fault Latched

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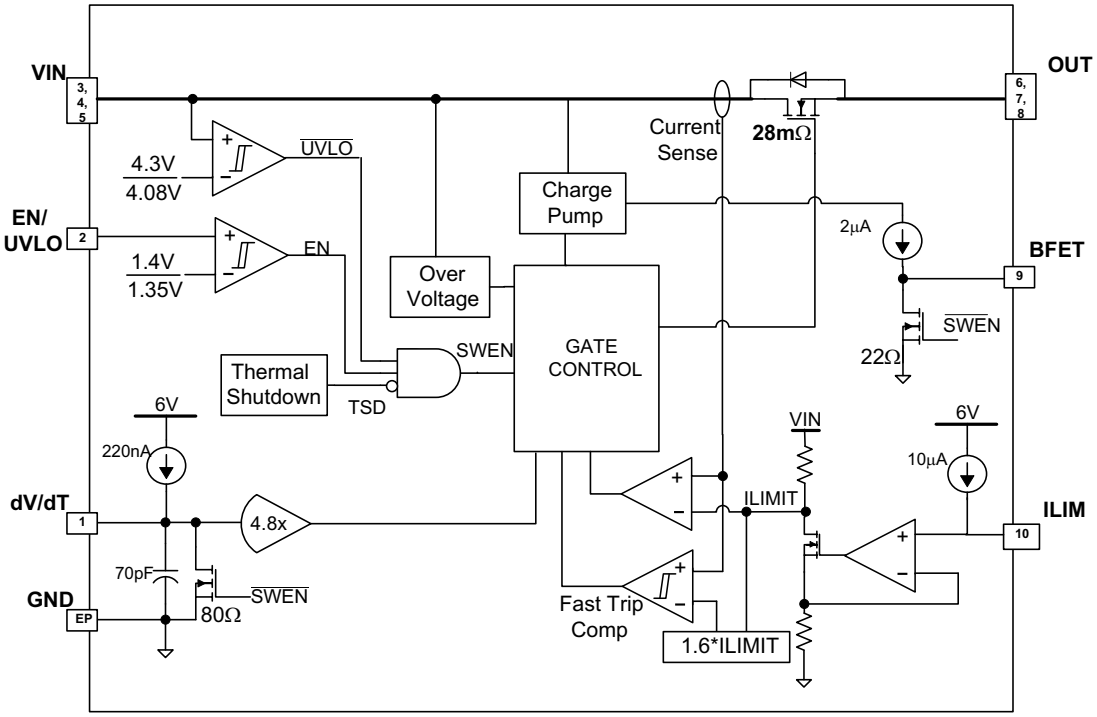
8 Detailed Description

8.1 Overview

The TPS25924x is an e-fuse with integrated power switch that is used to manage current, voltage and start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device starts conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (below V_{ENF}), internal MOSFET is turned off. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN}, typically 150°C, the thermal shutdown circuitry shuts down the internal MOSFET thereby disconnecting the load from the supply. In TPS259240, the output remains disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259241 device remains off during a cooling period until device temperature falls below T_{SHDN} – 10°C, after which it attempts to restart. This ON and OFF cycle continues until fault is cleared.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 GND

This is the most negative voltage in the circuit and is used as a reference for all voltage measurements unless otherwise specified.

Feature Description (continued)

8.3.2 VIN

Input voltage to the TPS25924x. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V to 13.8 V for TPS25924x. The device can continuously sustain a voltage of 20 V on VIN pin. However, above the recommended maximum bus voltage, the device will be in over-voltage protection (OVP) mode, limiting the output voltage to V_{OVC}. The power dissipation in OVP mode is P_{D_OVP} = (V_{VIN} – V_{OVC}) x I_{OUT}, which can potentially heat up the device and cause thermal shutdown.

8.3.3 dV/dT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{dVdT}) on the output. Equation governing slew rate at start-up is shown in Equation 1:

$$\frac{dV_{OUT}}{dt} = \frac{I_{dVdT} \times GAIN_{dVdT}}{C_{dVdT} + C_{INT}}$$

where

- I_{dVdT} = 220 nA (Typical)
- C_{INT} = 70 pF (Typical)
- $GAIN_{dVdT}$ = 4.85

$$\frac{dV_{OUT}}{dT} = \text{Desired output slew rate} \quad (1)$$

The total ramp time (T_{dVdT}) for 0 to VIN can be calculated using Equation 2:

$$T_{dVdT} = 10^6 \times V_{IN} \times (C_{dVdT} + 70\ pF) \quad (2)$$

For details on how to select an appropriate charging time/rate, refer to the applications section *Setting Output Voltage Ramp Time (T_{dVdT})*.

8.3.4 BFET

Connect this pin to an external NFET that can be used to disconnect input supply from rest of the system in the event of power failure at VIN. The BFET pin is controlled by either input UVLO (V_{UVR}) event or EN/UVLO (see Table 1). BFET can source charging current of 2 µA (TYP) and sink (discharge) current from the gate of the external FET via a 26-Ω internal discharge resistor to initiate fast turnoff, typically <1 µs. Due to 2 µA charging current, it is recommended to use >10 MΩ impedance when probing the BFET node.

Table 1. BFET

EN/UVLO > V_{ENR}	VIN>V_{UVR}	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

8.3.5 EN/UVLO

As an input pin, it controls both the ON and OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin turns off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the TPS259240 by toggling this pin (H→L).

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1 us typical) for quick detection of power failure. When used with a resistor divider from supply to EN/UVLO to GND, power-fail detection on EN/UVLO helps in quick turnoff of the BFET driver, thereby stopping the flow of reverse current (see typical application diagram, Figure 43). For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

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8.3.6 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM}. After start-up event and during normal operation, current limit is set to I_{OL} (over-load current limit) as shown in Equation 3.

$$I_{OL} = \left(0.7 + 3 \times 10^{-5} \times R_{ILIM}\right) \quad (3)$$

When power dissipation in the internal MOSFET [$P_D = (V_{VIN} – V_{OUT}) \times I_{OUT}$] exceeds 10 W, there is a 2% – 12% thermal foldback in the current limit value so that I_{OL} drops to I_{SC}. In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature. See Figure 36.

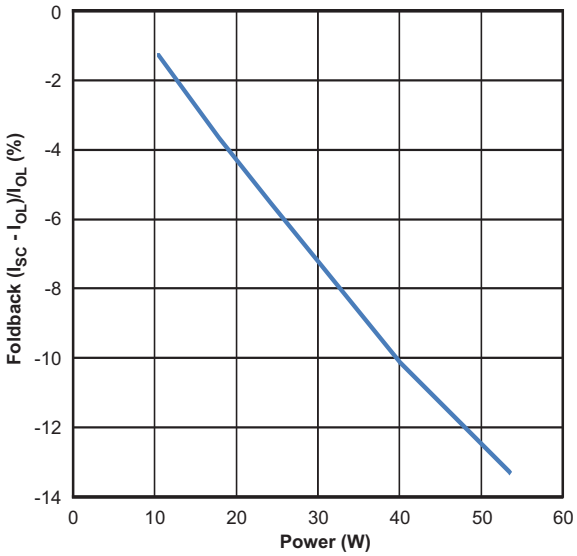


Figure 36. Thermal Foldback in Current Limit

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the TPS25924x incorporates a fast-trip comparator, which shuts down the pass device very quickly when $I_{OUT} > I_{FASTRIP}$, and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over-load current limit ($I_{FASTRIP} = 1.6 \times I_{OL}$). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to I_{OL} (see Figure 37 and Figure 38).

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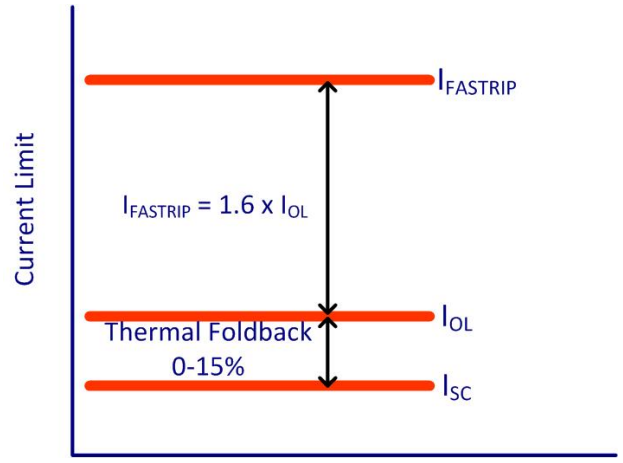


Figure 37. Fast-Trip Current

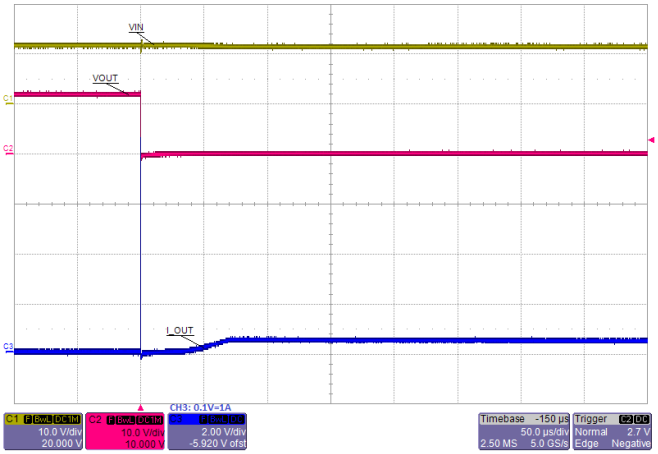


Figure 38. Fast-Trip and Current Limit Amplifier Response for Short Circuit

8.4 Device Functional Modes

The TPS25924x is a hot-swap controller with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When V_{VIN} exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET and also start charging the gate of external blocking FET (if connected) via the BFET pin. As VIN rises, the internal MOSFET of the device and external FET (if connected) starts conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (that is, below V_{ENF}), the internal MOSFET is turned off and BFET pin is discharged, thereby, blocking the flow of current from VIN to OUT. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

Having successfully completed its start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN}, typically 150°C, the thermal shutdown circuitry shuts down the internal MOSFET thereby disconnecting the load from the supply. In the TPS259240, the output remains disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259241 device remains off during a cooling period until device temperature falls below T_{SHDN} – 10°C, after which it attempts to restart. This ON and OFF cycle continues until fault is cleared.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS25924x is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select component values for the device. Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS2592xx Design Calculator* (SLUC570) is available on web folder. This section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Simple 3.7-A eFuse Protection for Set Top Boxes

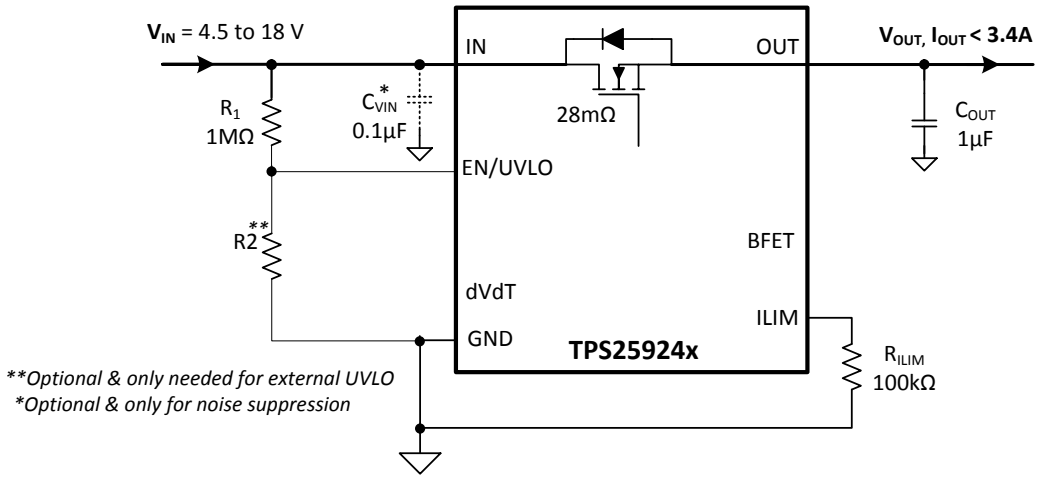


Figure 39. Typical Application Schematic: Simple 3.7-A e-Fuse for STBs

9.2.1.1 Design Requirements

Table 2 shows the design parameters for this application.

Table 2. Design Parameters

DESIGN PARAMETER		EXAMPLE VALUE
V_{IN}	Input voltage	12 V
$V_{(UV)}$	Undervoltage lockout set point	Default: V_{UVR} = 4.3 V
$V_{(OV)}$	Overvoltage protection set point	Default: V_{OVC} = 15 V
$R_{L(SU)}$	Load at start-up	4 Ω
$I_{OL} = I_{ILIM}$	Current limit	3.7 A
C_{OUT}	Load capacitance	1 µF
T_A	Maximum ambient temperature	85°C

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9.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25924x.

9.2.1.2.1 Step by Step Design Procedure

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

9.2.1.2.2 Programming the Current-Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4.

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} \quad (4)$$

For $I_{OL} = I_{ILIM}$ = 3.7 A, from Equation 4, R_{ILIM} = 100 kΩ, choose closest standard value resistor with 1% tolerance.

9.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving Equation 5.

$$V_{(UV)} = \frac{R_1 + R_2}{R_2} \times V_{ENR} \quad (5)$$

Where V_{ENR} = 1.4 V is enable voltage rising threshold.

Since R_1 and R_2 leak the current from input supply (VIN), these resistors must be selected based on the acceptable leakage current from input power supply (VIN). The current drawnby R_1 and R_2 from the power supply {$I_{R12} = V_{IN}/(R_1 + R_2)$}.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R12} must be chosen to be 20x greater than the leakage current expected.

For default UVLO of V_{UVR} = 4.3 V, select R_2 = OPEN, and R_1 = 1 MΩ. Since EN/UVLO pin is rated only to 7 V, it cannot be connected directly to V_{IN}= 12 V. It has to be connected through R_1 = 1 MΩ only, so that the pull-up current for EN/UVLO pin is limited to < 20 µA.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, V_{UVR}. This is calculated using Equation 6.

$$V_{(PFAIL)} = 0.96 \times V_{UVR} \quad (6)$$

Where V_{UVR} is 4.3 V, Power fail threshold set is 4.1 V.

9.2.1.2.4 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device must be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor C_{dVdT} needed is calculated considering the two possible cases:

9.2.1.2.4.1 Case 1: Start-Up without Load: Only Output Capacitance C_{OUT} Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using Equation 8.

For TPS25924x, the inrush current is determined as shown in Equation 7:

$$I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{T_{dVdT}} \quad (7)$$

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Power dissipation during start-up is given by Equation 8:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (8)$$

Equation 8 assumes that load does not draw any current until the output voltage has reached its final value.

9.2.1.2.4.2 Case 2: Start-Up with Load: Output Capacitance C_{OUT} and Load Draws Current During Start-Up

When load draws current during the turnon sequence, there is additional power dissipated. Considering a resistive load during start-up ($R_{L(SU)}$), load current ramps up proportionally with increase in output voltage during T_{dVdT} time. The average power dissipation in the internal FET during charging time due to resistive load is given by Equation 9:

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (9)$$

Total power dissipated in the device during startup is given by Equation 10:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

Total current during startup is given by Equation 11:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (11)$$

If $I_{(STARTUP)} > I_{OL}$, the device limits the current to I_{OL} and the current limited charging time is determined by Equation 12:

$$T_{dVdT(Current\text{-}Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{OL}}{I_{(INRUSH)}} - 1 + LN\left(\frac{I_{(INRUSH)}}{I_{OL} - \frac{V_{(IN)}}{R_{L(SU)}}}\right)\right] \quad (12)$$

The power dissipation, with and without load, for selected start-up time must not exceed the shutdown limits as shown in Figure 40:

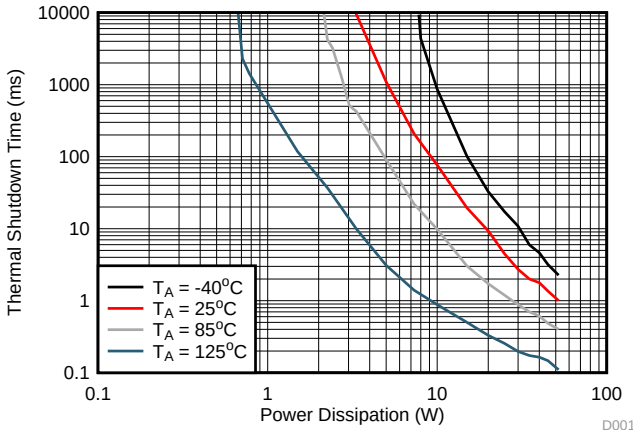


Figure 40. Thermal Shutdown Limit Plot

For the design example under discussion, select ramp-up capacitor C_{dVdT} = OPEN. Then, using Equation 2, we get Equation 13:

$$T_{dVdT} = 10^6 \times 12 \times (0 + 70\ pF) = 840\ \mu s \quad (13)$$

The inrush current drawn by the load capacitance (C_{OUT}) during ramp-up using Equation 7 is given by Equation 14:

$$I_{(INRUSH)} = 1\ \mu F \times \frac{12}{840\ \mu s} = 15\ mA \quad (14)$$

The inrush Power dissipation is calculated, using Equation 8 as shown in Equation 15:

$$P_{D(INRUSH)} = 0.5 \times 12 \times 15\ m = 90\ mW \quad (15)$$

For 90 mW of power loss, the thermal shut down time of the device must not be less than the ramp-up time T_{dVdT} to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 40 at T_A = 85°C, for 90 mW of power, the shutdown time is infinite. So it is safe to use 0.79 ms as start-up time without any load on output.

Considering the start-up with load 4 Ω, the additional power dissipation, when load is present during start up is calculated by Equation 16, using Equation 9:

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6\ W \quad (16)$$

The total device power dissipation during start up, using Equation 10 is given by Equation 17:

$$P_{D(STARTUP)} = 6 + 90\ m = 6.09\ W \quad (17)$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 6.09 W is more than 10 ms. So it is well within acceptable limits to not use an external capacitor ($C_{dV/dT}$) with start-up load of 4 Ω.

If, due to large C_{OUT}, there is a need to decrease the power loss during start-up, it can be done with increase of C_{dVdT} capacitor.

9.2.1.2.5 Support Component Selection—C_{VIN}

C_{VIN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for C_{VIN}.

9.2.1.3 Application Curves

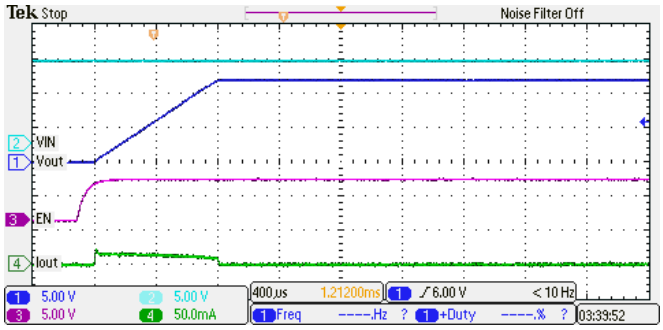


Figure 41. Output Ramp without Load on Output

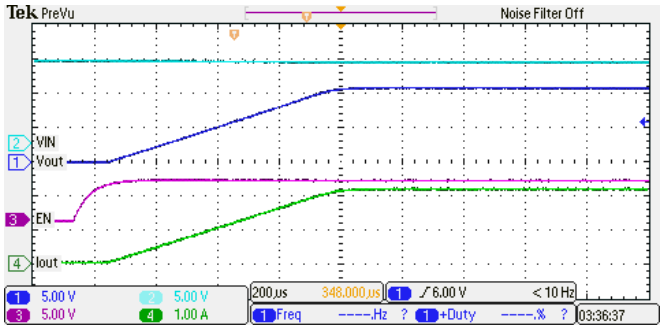


Figure 42. Output Ramp with 4-Ω Load at Start Up

9.2.2 Inrush and Reverse Current Protection for Hold-Up Capacitor Application (for example, SSD)

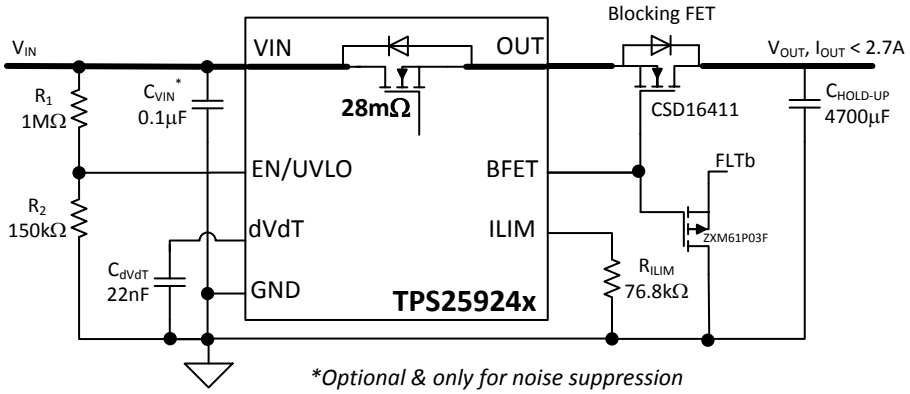


Figure 43. Inrush and Reverse Current Protection for Hold-Up Capacitor Application (for example, SSD) (TPS25924x UVLO is used as power fail comparator)

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9.2.2.1 Design Requirements

The design parameters for this design example are shown in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER		EXAMPLE VALUE
V_{IN}	Input voltage	12 V
$V_{(UV)}$	Undervoltage lockout set point	10.8 V
$V_{(OV)}$	Overvoltage protection set point	Default: V_{OVC} = 15 V
$R_{L(SU)}$	Load at start-up	1000 Ω
I_{OL}= I_{ILIM}	Current limit	3 A
C_{OUT}	Load capacitance	4700 µF
T_A	Maximum ambient temperature	85°C

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Programming the Current-Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4.

For I_{OL} = I_{ILIM} = 3 A, from Equation 4, R_{ILIM} = 76.8 kΩ. Choose closest standard value resistor with 1% tolerance.

9.2.2.2.2 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving Equation 5.

For UVLO of $V_{(UV)}$ = 10.8 V, select R_2 = 150 kΩ, and R_1 = 1 MΩ.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, $V_{(UV)}$. This is calculated using Equation 6.

Where $V_{(UV)}$ = 10.73 V, Power fail threshold set is $V_{(PFAIL)}$ = 10.35 V.

9.2.2.2.3 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device must be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

For the design example under discussion, select ramp-up capacitor C_{dVdT} = 22 nF. Then, using Equation 2 we get Equation 18:

$$T_{dVdT} = 10^6 \times 12 \times (22\ nF + 70\ pF) = 265\ ms \quad (18)$$

The inrush current drawn by the load capacitance (C_{OUT}) during ramp-up using Equation 7 is given by Equation 19:

$$I_{(INRUSH)} = 4700\ \mu F \times \frac{12}{265\ ms} = 213\ mA \quad (19)$$

The inrush Power dissipation is calculated, using Equation 8 is given by Equation 20:

$$P_{D(INRUSH)} = 0.5 \times 12 \times 213\ m = 1278\ mW \quad (20)$$

Considering the start-up with load 1000 Ω, the additional power dissipation, when load is present during start up is calculated, using Equation 9 is given by Equation 21:

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 1000} = 24\ mW \quad (21)$$

The total device power dissipation during start up is given by Equation 22:

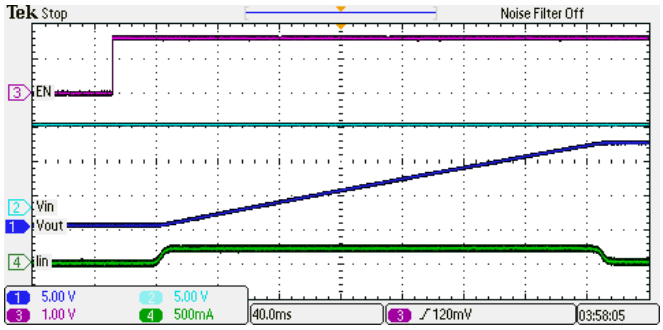
$$P_{D(STARTUP)} = 1278 + 24 = 1302\ mW \quad (22)$$

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From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 1.3 W is more than 300 ms. So the device starts safely.

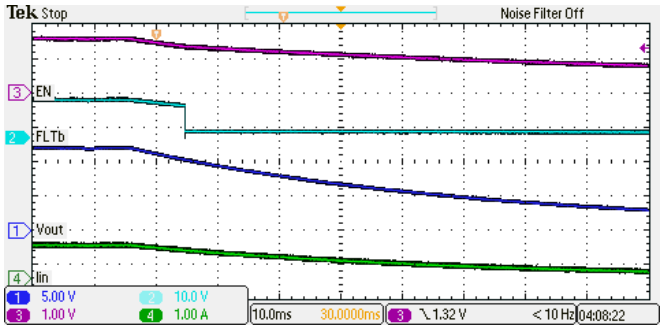
If CdVdT = 4.7 nF was used, the device must have tried to charge the 4700-µF output cap with inrush current of 986 mA in 57.24 ms, dissipating power of 5.94 W. This is outside the safe starting condition of the device, and must have led the device to enter thermal shutdown during start-up.

9.2.2.3 Application Curves



C_{OUT} = $C_{HOLD-UP}$ = 4700 µF C_{dVdT} = 22 nF

Figure 44. Output Ramp Up

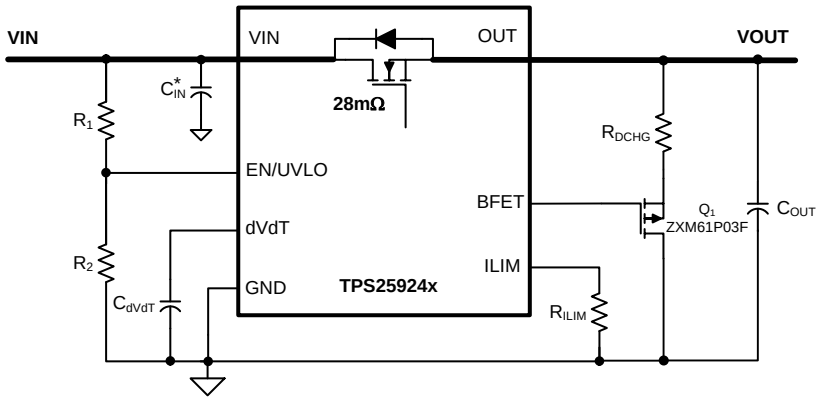


C_{OUT} = $C_{HOLD-UP}$ = 4700 µF $V_{(PFAIL)}$ = 10.35 V R_{LOAD} = 12 Ω

Figure 45. Hold-up Power When VIN Fails

9.2.3 Controlled Power Down using TPS25924x

When the device is disabled, the output voltage is left floating and power down profile is entirely dictated by the load. In some applications, this can lead to undesired activity as the load is not powered down to a defined state. Controlled output discharge can ensure the load is turned off completely and not in an undefined operational state. The BFET pin in TPS25924x family of eFuses facilitates Quick Output Discharge (QOD) function as illustrated in Figure 46. When the device is/gets disabled, the BFET pin pulls low which enables the external P-MOSFET Q1 for discharge feature to function. The output voltage discharge rate is dictated by the output capacitor C_{OUT}, the discharge resistance R_{DCHG} and the load.



*Optional & only for noise suppression

Figure 46. Circuit Implementation with Quick Output Discharge Function

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10 Power Supply Recommendations

The device is designed for supply voltage range of 4.5 V ≤ V_{IN} ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

10.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with Equation 23:

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (23)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 47.

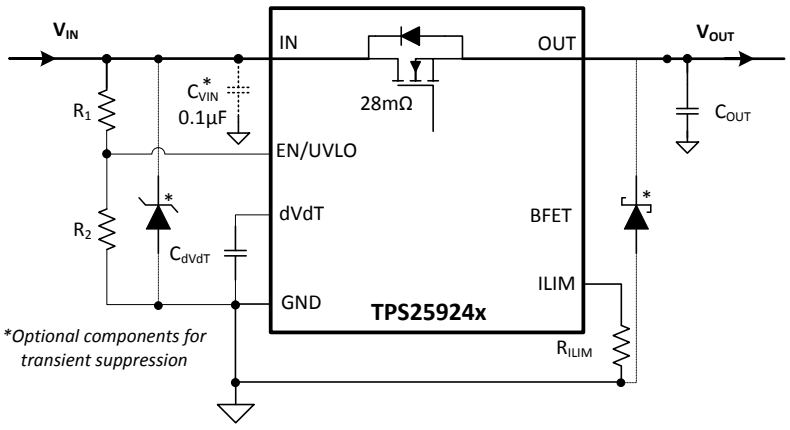


Figure 47. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

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11 Layout

11.1 Layout Guidelines

- For all applications, a 0.01-µF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 48 for a PCB layout example.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- Locate all support components: R_{ILIM}, C_{dVdT} and resistors for EN/UVLO, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILIM} and C_{dVdT} components to the device must be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

11.2 Layout Example

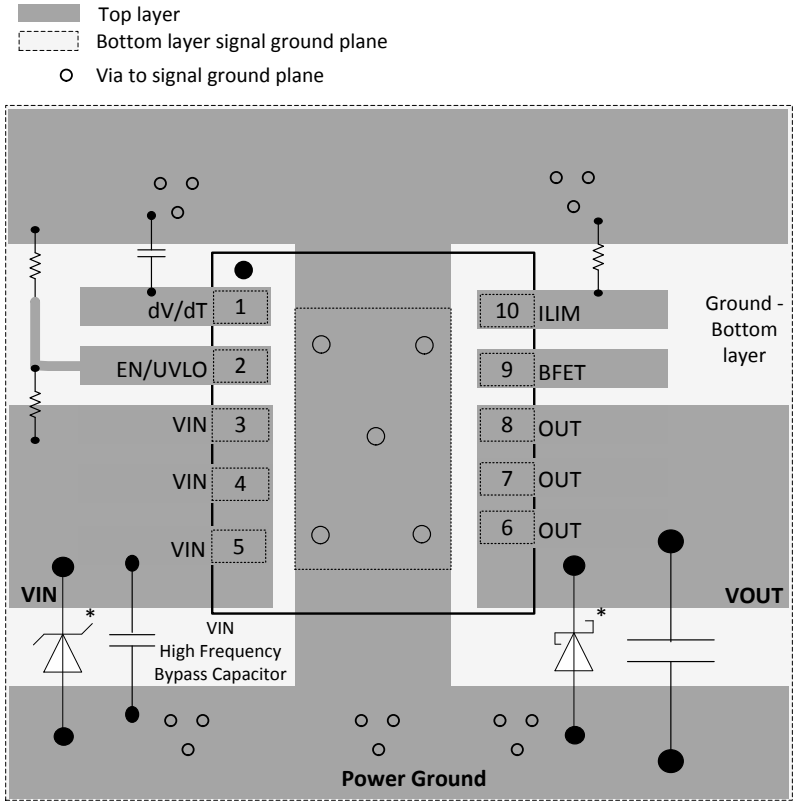


Figure 48. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *TPS2592xx Design Calculator*
- *TPS259230-41EVM User's Guide*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS259241	Click here	Click here	Click here	Click here	Click here
TPS259240	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

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All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259240DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259241DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

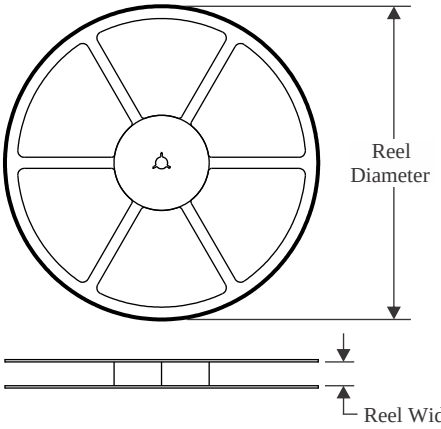
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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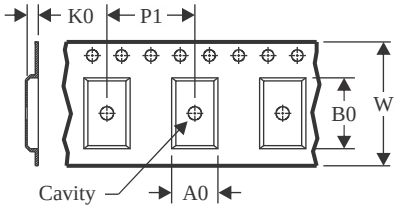
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

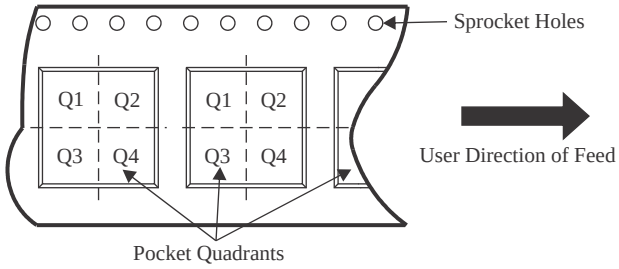


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

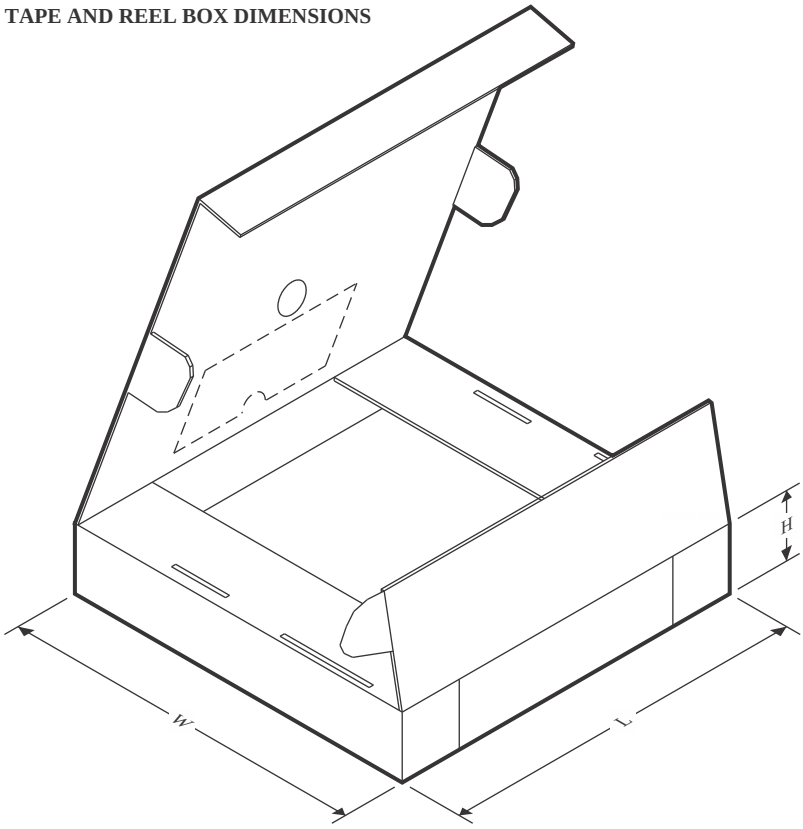
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259240DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS259240DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259240DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259240DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259240DRCR	VSON	DRC	10	3000	353.0	353.0	32.0
TPS259240DRCR	VSON	DRC	10	3000	335.0	335.0	25.0
TPS259240DRCRG4	VSON	DRC	10	3000	367.0	367.0	35.0
TPS259240DRCT	VSON	DRC	10	250	182.0	182.0	20.0
TPS259241DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS259241DRCRG4	VSON	DRC	10	3000	346.0	346.0	33.0
TPS259241DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

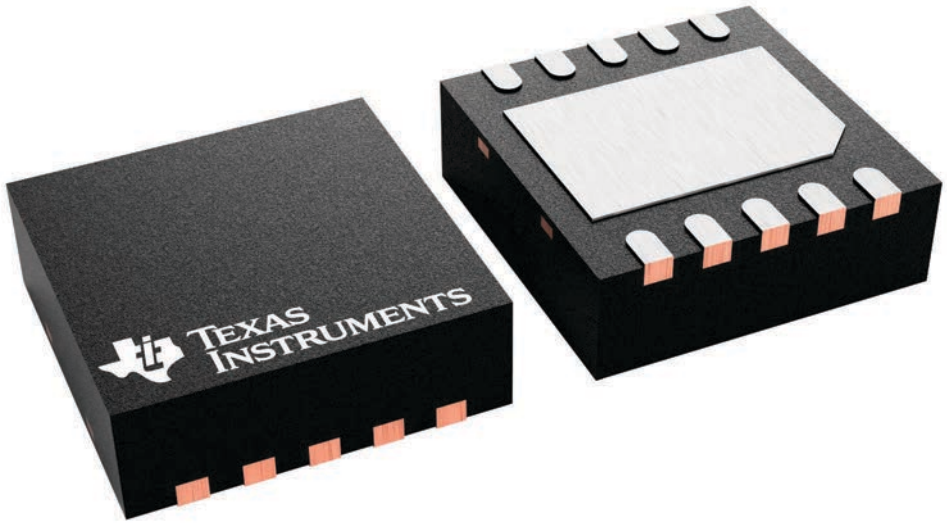
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



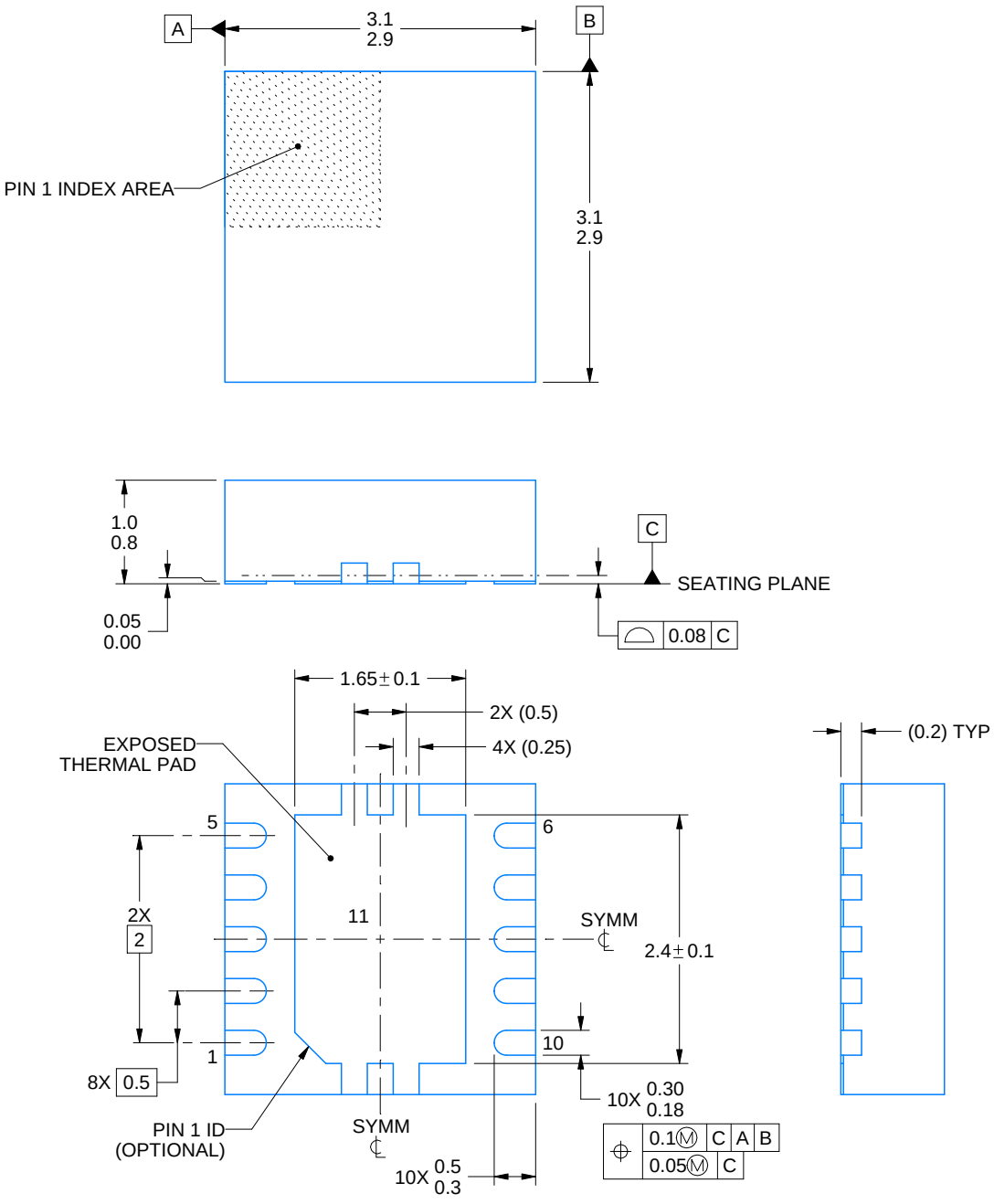
4226193/A

DRC0010J

PACKAGE OUTLINE

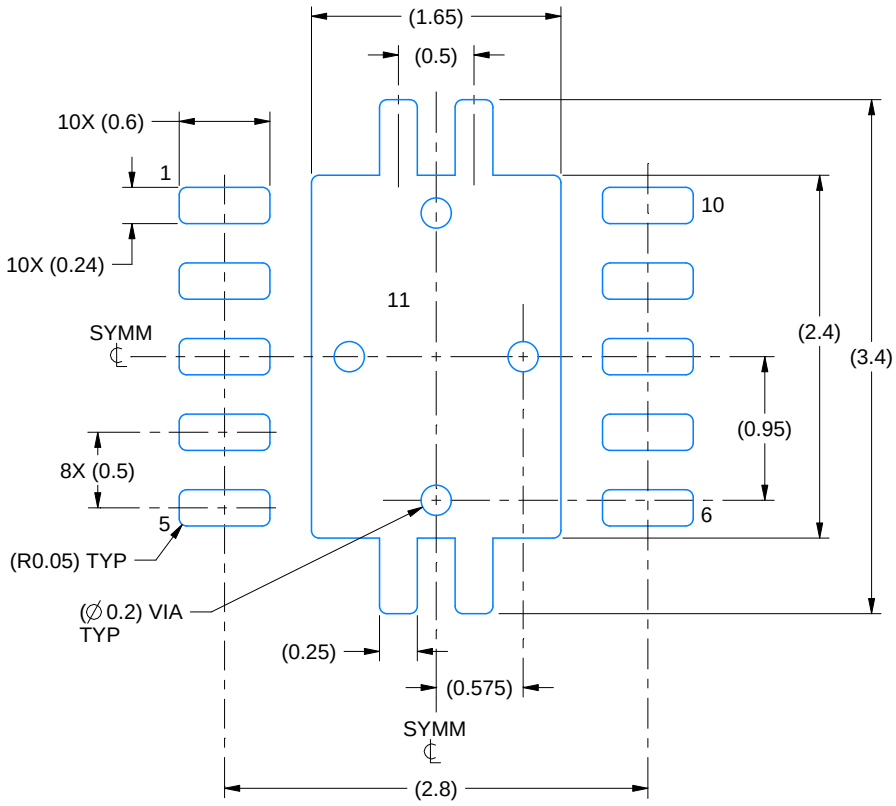
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

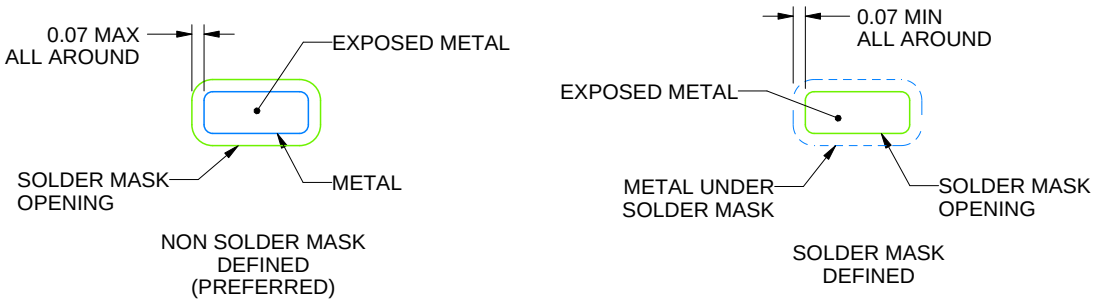


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

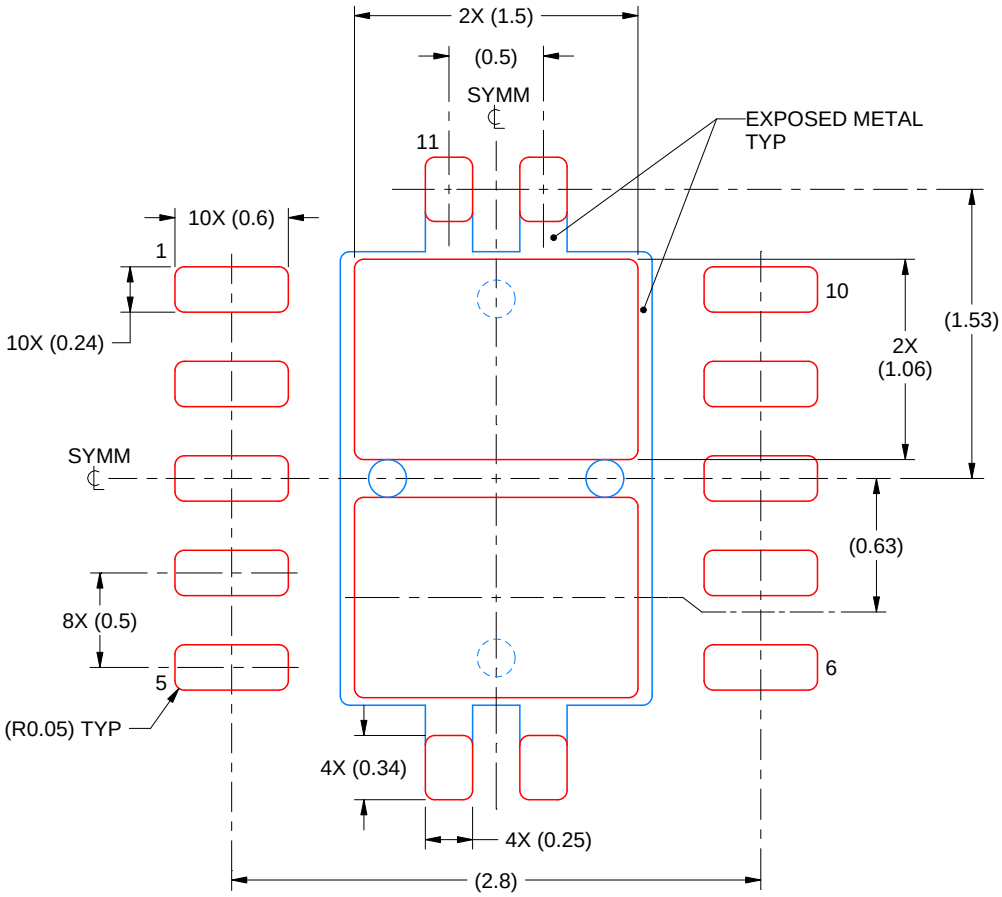
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025