# 2.5-V to 18-V High-Efficiency Hot-Swap Controller

**Check for Samples: TPS24700, TPS24701**

## FEATURES

- **2.5-V to 18-V Operation**
- **Accurate Current Limiting for Starup**
- **Accurate 25-mV Current Sense Threshold**
- **Timed Overcurrent Breaker**
- **Power-Good Output**
- **Fast Breaker for Short-Circuit Protection**
- **Latch Off (TPS24700) and Retry Versions (TPS24701)**
- **Programmable UV Threshold**
- **Drop-In Upgrade for LTC4211 – No Layout Changes**
- **Small MSOP-8 Package**

## APPLICATIONS

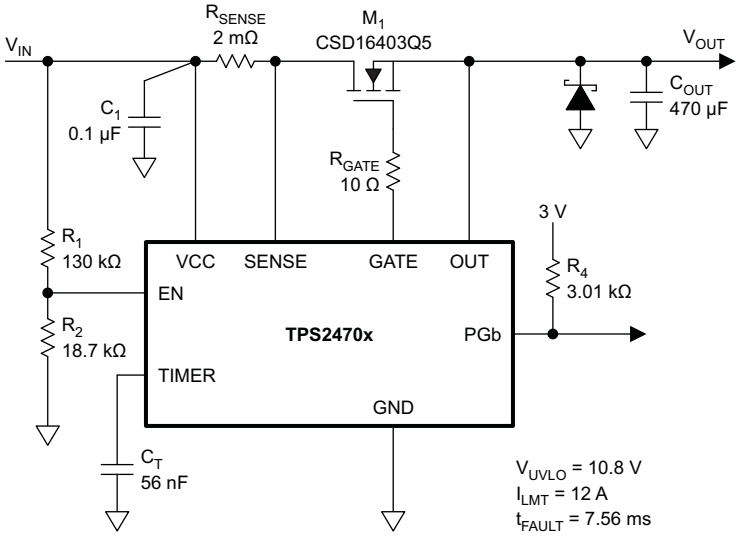
- **Server Backplanes**
- **Storage Area Networks (SAN)**
- **Medical Systems**
- **Plug-In Modules**
- **Base Stations**
- **Consumer Electronics**

## DESCRIPTION

The TPS24700/1 is an easy-to-use, 2.5 V to 18 V, hot-swap controller that drives an external N-channel MOSFET. The programmable current limit and fault time protect the supply and load from excessive current at startup. After startup, currents above the user-selected limit are allowed to flow until programmed timeout – except in extreme overload events when load is immediately disconnected from source. The low, 25-mV current sense threshold is highly accurate and allows use of smaller, more-efficient sense resistors, yielding lower power loss and smaller footprint. A power-good output is provided for status monitoring and downstream load control.

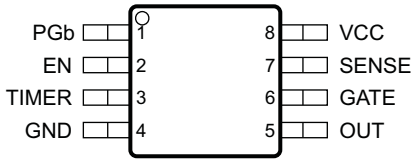
TPS24700/1 replaces the LTC4211 in existing designs with no PCB board changes and only minor external component changes – yielding a more accurate, efficient solution.

### TYPICAL APPLICATION OF TPS24700/1 (12 V AT 10 A)




### PINOUT

**DGK Package**
**(Top View)**




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DEVICE INFORMATION

| $T_A$ | PACKAGE | PART NUMBER(1) | FUNCTION | MARKING |
|---|---|---|---|---|
| –40ºC to 85ºC | MSOP-8 | TPS24700 | Latched | 24700 |
| | | TPS24701 | Retry | 24701 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, all voltages referred to GND (unless otherwise noted)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| Input voltage range | EN, GATE, OUT, PGb(1), SENSE, VCC | | –0.3 to 30 | V |
| | SENSE to VCC | | –0.3 to 0.3 | |
| | TIMER | | –0.3 to 5 | |
| Sink current | PGb | | 5 | mA |
| ESD rating | Human-body model | All pins except PGb | 2 | kV |
| | | PGb | 0.5 | |
| | Charged-device model | | 0.5 | |
| Temperature | Maximum junction, $T_J$ | | Internally limited | °C |

(1) Do not apply voltages directly to these pins.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS24700/01 | UNIT |
|---|---|---|---|
| | | MSOP (8) PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 57.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 110.5 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 60.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 24 | °C/W |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 14.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | SENSE, VCC | 2.5 | | 18 | V |
| | EN, PGb, OUT | 0 | | 18 | |
| Sink current | PGb | 0 | | 2 | mA |
| External capacitance | TIMER | 1 | | | nF |
| | GATE (1) | | | 1 | µF |
| Operating junction temperature range, $T_J$ | | –40 | | 125 | °C |

(1) External capacitance tied to GATE should be in series with a resistor no less than 1 kΩ.

## ELECTRICAL CHARACTERISTICS

–40°C ≤ $T_J$ ≤ 125°C, $V_{CC}$ = 12 V, and $V_{EN}$ = 3 V.
All voltages referenced to GND, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **VCC** | | | | | |
| UVLO threshold, rising | | 2.2 | 2.32 | 2.45 | V |
| UVLO threshold, falling | | 2.1 | 2.22 | 2.35 | V |
| UVLO hysteresis (1) | | | 0.1 | | V |
| Supply current | Enabled — $I_{OUT}$ + $I_{VCC}$ + $I_{SENSE}$ | | 1 | 1.4 | mA |
| | Disabled — EN = 0 V, $I_{OUT}$ + $I_{VCC}$ + $I_{SENSE}$ | | 0.45 | | mA |
| **EN** | | | | | |
| Threshold voltage, falling | | 1.2 | 1.3 | 1.4 | V |
| Hysteresis (1) | | | 50 | | mV |
| Input leakage current | 0 V ≤ $V_{EN}$ ≤ 30 V | –1 | 0 | 1 | µA |
| Turnoff time | EN ↓ to $V_{GATE}$ < 1 V, $C_{GATE}$ = 33 nF | 20 | 60 | 150 | µs |
| Deglitch time | EN ↑ | 8 | 14 | 18 | µs |
| Disable delay | EN ↓ to GATE ↓, $C_{GATE}$ = 0, $t_{pff50–90}$, See Figure 1 | 0.1 | 0.4 | 1 | µs |
| **PGb** | | | | | |
| Threshold | $V_{(SENSE–OUT)}$ rising, PGb going high | 140 | 240 | 340 | mV |
| Hysteresis (1) | Measured $V_{(SENSE–OUT)}$ falling, PGb going low | | 70 | | |
| Output low voltage | Sinking 2 mA | | 0.11 | 0.25 | V |
| Input leakage current | $V_{PGb}$ = 0 V, 30 V | –1 | 0 | 1 | µA |
| Delay (deglitch) time | Rising or falling edge | 2 | 3.4 | 6 | ms |
| **TIMER** | | | | | |
| Sourcing current | $V_{TIMER}$ = 0 V | 8 | 10 | 12 | µA |
| Sinking current | $V_{TIMER}$ = 2 V | 8 | 10 | 12 | µA |
| | $V_{EN}$ = 0 V, $V_{TIMER}$ = 2 V | 2 | 4.5 | 7 | mA |
| Upper threshold voltage | | 1.3 | 1.35 | 1.4 | V |
| Lower threshold voltage | | 0.33 | 0.35 | 0.37 | V |
| Timer activation voltage | Raise GATE until $I_{TIMER}$ sinking, measure $V_{(GATE–VCC)}$, $V_{CC}$ = 12 V | 5 | 5.9 | 7 | V |
| Bleed-down resistance | $V_{TIMER}$ = 2 V | 70 | 104 | 130 | kΩ |
| **OUT** | | | | | |
| Input bias current | $V_{OUT}$ = 12 V | | 16 | 30 | µA |
| **GATE** | | | | | |
| Output voltage | $V_{OUT}$ = 12 V | 23.5 | 25.8 | 28 | V |
| Clamp voltage | Inject 10 µA into GATE, measure $V_{(GATE–VCC)}$ | 12 | 13.9 | 15.5 | V |
| Sourcing current | $V_{GATE}$ = 12 V | 20 | 30 | 40 | µA |

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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## ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ $T_J$ ≤ 125°C, $V_{CC}$ = 12 V, and $V_{EN}$ = 3 V.

All voltages referenced to GND, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Sinking current | Fast turnoff, $V_{GATE}$ = 14 V | 0.5 | 1 | 1.4 | A |
| | Sustained, $V_{GATE}$ = 4 V to 23 V | 6 | 11 | 20 | mA |
| | In inrush current limit, $V_{GATE}$ = 4 V–23 V | 20 | 30 | 40 | µA |
| Pulldown resistance | Thermal shutdown | 14 | 20 | 26 | kΩ |
| Turnon delay | $V_{CC}$ rising to GATE sourcing, $t_{prr50-50}$, See Figure 2 | | 100 | 250 | µs |
| **SENSE** | | | | | |
| Input bias current | $V_{SENSE}$ = 12 V, sinking current | | 30 | 40 | µA |
| Current limit threshold | $V_{OUT}$ = 12 V | 22.5 | 25 | 27.5 | mV |
| Fast-trip threshold | | 52 | 60 | 68 | mV |
| Fast-turnoff duration | | 8 | 13.5 | 18 | µs |
| Fast-turnoff delay | $V_{(VCC–VSENSE)}$ = 80 mV, $C_{GATE}$ = 0 pF, $t_{prf50–50}$, See Figure 3 | | 200 | | ns |
| **OTSD** | | | | | |
| Threshold, rising | | 130 | 140 | | °C |
| Hysteresis(1) | | | 10 | | °C |

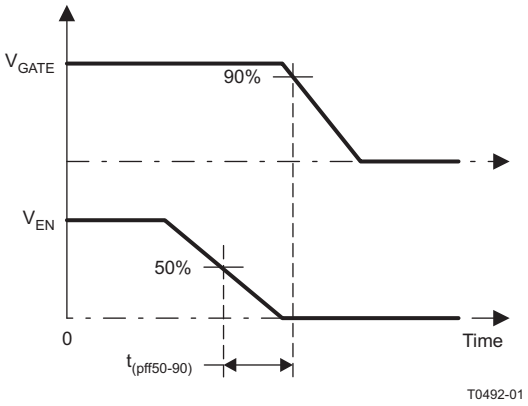



**Figure 1. $t_{pff50–90}$ Timing Definition**

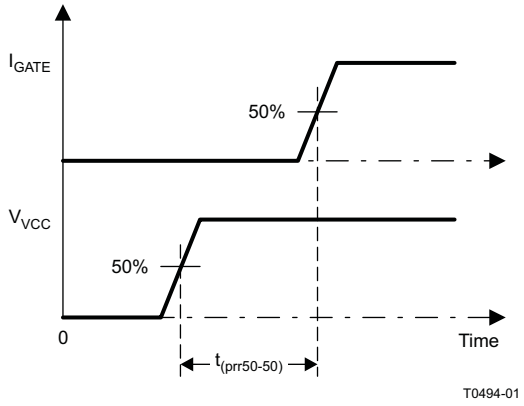



**Figure 2. $t_{prr50–50}$ Timing Definition**

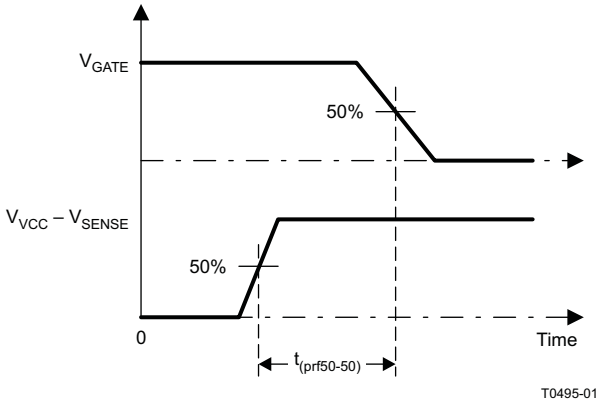



**Figure 3. $t_{prf50–50}$ Timing Definition**


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## FUNCTIONAL BLOCK DIAGRAM

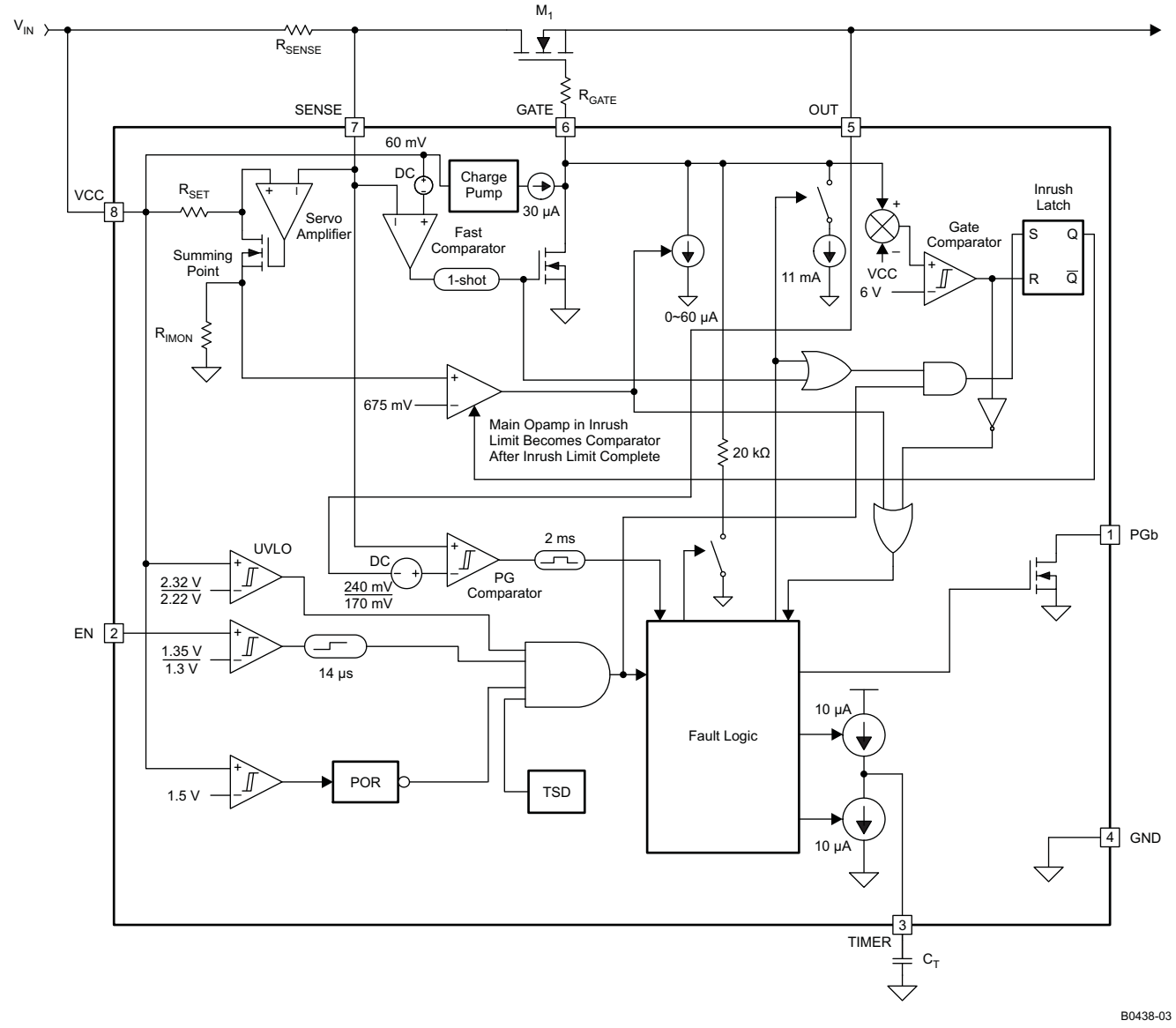



**Figure 4. Block Diagram of the TPS24700/1**

### PIN FUNCTIONS

| NAME | TPS24700/1 | I/O | DESCRIPTION |
|---|---|---|---|
| EN | 2 | I | Active-high enable input. Logic input. Connects to resistor divider |
| GATE | 6 | O | Gate driver output for external MOSFET |
| GND | 4 | – | Ground |
| OUT | 5 | I | Output voltage sensor for monitoring MOSFET power |
| PGb | 1 | O | Active-low, open-drain power good indicator. Status is determined by the voltage across the MOSFET. |
| SENSE | 7 | I | Current sensing input for resistor shunt from VCC to SENSE |
| TIMER | 3 | I/O | A capacitor connected from this pin to GND provides a fault timing function. |
| VCC | 8 | I | Input-voltage sense and power supply |

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## DETAILED PIN DESCRIPTIONS

The following description relies on the typical application diagram shown on the front page of this data sheet, as well as the functional block diagram of Figure 4.

**EN:** Applying a voltage of 1.35 V or more to this pin enables the gate driver. The addition of an external resistor divider allows the EN pin to serve as an undervoltage monitor. Cycling EN low and then back high resets a TPS24700 that has latched off due to a fault condition. This pin should not be left floating.

**GATE:** This pin provides gate drive to the external MOSFET. A charge pump sources 30 µA to enhance the external MOSFET. A 13.9-V clamp between GATE and VCC limits the gate-to-source voltage, because $V_{VCC}$ is very close to $V_{OUT}$ in normal operation. During start-up, a transconductance amplifier regulates the gate voltage of M1 to provide inrush current limiting. The TIMER pin charges timer capacitor $C_T$ during the inrush. Inrush current limiting continues until the $V_{(GATE–VCC)}$ exceeds the Timer Activation Voltage (6 V for $V_{VCC}$ = 12 V). Then the TPS24700/1 enters into circuit-breaker mode. The Timer Activation Voltage is defined as a threshold voltage. When $V_{(GATE-VCC)}$ exceeds this threshold voltage, the inrush operation is finished and the TIMER stops sourcing current and begins sinking current. In the circuit-breaker mode, the current flowing in $R_{SENSE}$ is compared with the current-limit threshold derived from Equation 1. If the current flowing in $R_{SENSE}$ exceeds the current limit threshold, then MOSFET M1 is turned off. The GATE pin is disabled by the following three mechanisms:

1. GATE is pulled down by an 11-mA current source when
   – The fault timer expires during an overload current fault ($V_{SENSE}$ > 25 mV)
   – $V_{EN}$ is below its falling threshold
   – $V_{VCC}$ drops below the UVLO threshold
2. GATE is pulled down by a 1-A current source for 13.5 µs when a hard output short circuit occurs and $V_{(VCC–SENSE)}$ is greater than 60 mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the external MOSFET remains off.
3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

GATE remains low in latch mode (TPS24700) and attempts a restart periodically in retry mode (TPS24701).

If used, any capacitor connecting GATE and GND should not exceed 1 µF and it should be connected in series with a resistor of no less than 1 kΩ. No external resistor should be directly connected from GATE to GND or from GATE to OUT.

**GND:** This pin is connected to system ground.

**OUT:** This pin allows the controller to measure the drain-to-source voltage across the external MOSFET M1. The power-good indicator (PGb) relies on this information. The OUT pin should be protected from negative voltage transients by a clamping diode or sufficient capacitors. A Schottky diode of 3 A / 40 V in an SMC package is recommended as a clamping diode for high-power applications. The OUT pin should be bypassed to GND with a low-impedance ceramic capacitor in the range of 10 nF to 1 µF.

**PGb:** This active-low, open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PGb pulls low after the drain-to-source voltage of the FET has fallen below 170 mV and a 3.4-ms deglitch delay has elapsed. It goes open-drain when VDS exceeds 240 mV. PGb assumes high-impedance status after a 3.4-ms deglitch delay once $V_{DS}$ of M1 rises up, resulting from GATE being pulled to GND at any of the following conditions:

- An overload current fault occurs ($V_{SENSE}$ > 25 mV).
- A hard output short circuit occurs, leading to $V_{(VCC–SENSE)}$ greater than 60 mV, i.e., the fast-trip shutdown threshold has been exceeded.
- $V_{EN}$ is below its falling threshold.
- $V_{VCC}$ drops below the UVLO threshold.
- Die temperature exceeds the OTSD threshold.

**SENSE:** This pin connects to the negative terminal of $R_{SENSE}$. It provides a means of sensing the voltage across this resistor, as well as a way to monitor the drain-to-source voltage across the external FET. The current limit $I_{LIM}$ is set by Equation 1.

$$I_{LIM} = \frac{25\ mV}{R_{SENSE}} \quad (1)$$


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A fast-trip shutdown occurs when $V_{(VCC–VSENSE)}$ exceeds 60 mV.

**TIMER:** A capacitor $C_T$ connected from the TIMER pin to GND determines the overload fault timing. TIMER sources 10 µA when an overload is present, and discharges $C_T$ at 10 µA otherwise. M1 is turned off when $V_{TIMER}$ reaches 1.35 V. In an application implementing auto-retry after a fault, this capacitor also determines the period before the external MOSFET is re-enabled. A minimum timing capacitance of 1 nF is recommended to ensure proper operation of the fault timer. The value of $C_T$ can be calculated from the desired fault time $t_{FLT}$, using Equation 2.

$$C_T = \frac{10\ \mu A}{1.35\ V} \times t_{FLT} \quad (2)$$

The latch mode (TPS24700) or the retry mode (TPS24701) occurs if the load current exceeds the current limit threshold or the fast-trip shutdown threshold. While in latch mode, the TIMER pin continues to charge and discharge the attached capacitor periodically. In retry mode, the external MOSFET is disabled for sixteen cycles of TIMER charging and discharging. The TIMER pin is pulled to GND by a 2-mA current source at the end of the $16^{th}$ cycle of charging and discharging. The external MOSFET is then re-enabled. The TIMER pin capacitor, $C_T$, can also be discharged to GND during latch mode or retry mode by a 2-mA current source whenever any of the following occurs:

- $V_{EN}$ is below its falling threshold.
- $V_{VCC}$ drops below the UVLO threshold.

**VCC:** This pin performs three functions. First, it provides biasing power to the integrated circuit. Second, it serves as an input to the power-on reset (POR) and undervoltage lockout (UVLO) functions. The VCC trace from the integrated circuit should connect directly to the positive terminal of $R_{SENSE}$ to minimize the voltage sensing error. Bypass capacitor $C_1$, shown in the typical application diagram on the front page, should be connected to the positive terminal of $R_{SENSE}$. A capacitance of at least 10 nF is recommended.

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## TYPICAL CHARACTERISTICS

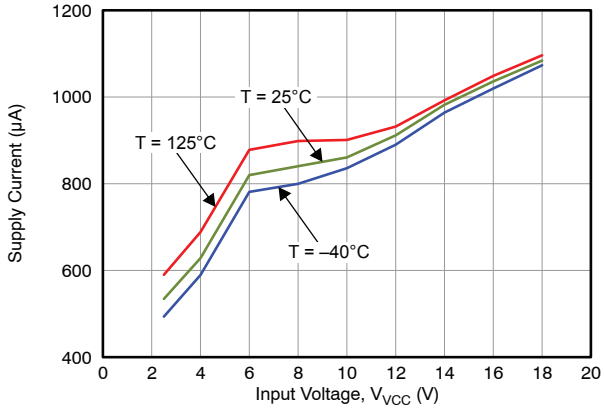



**Figure 5. Supply Current vs Input Voltage at Normal Operation (EN = High)**

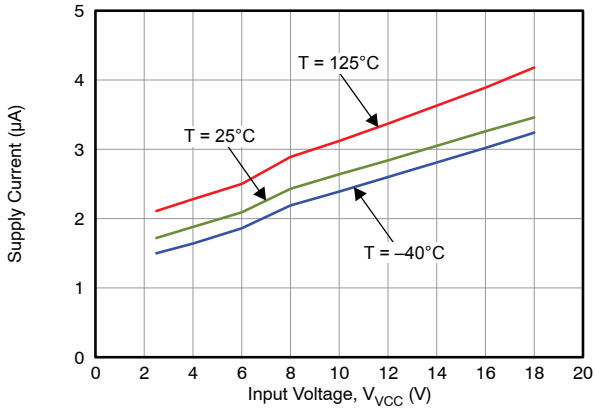



**Figure 6. Supply Current vs Input Voltage at Shutdown (EN = 0 V)**

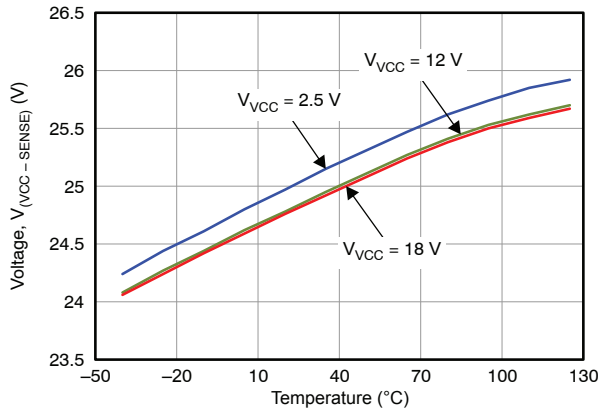



**Figure 7. Voltage Across $R_{SENSE}$ in Inrush Current Limiting vs Temperature**

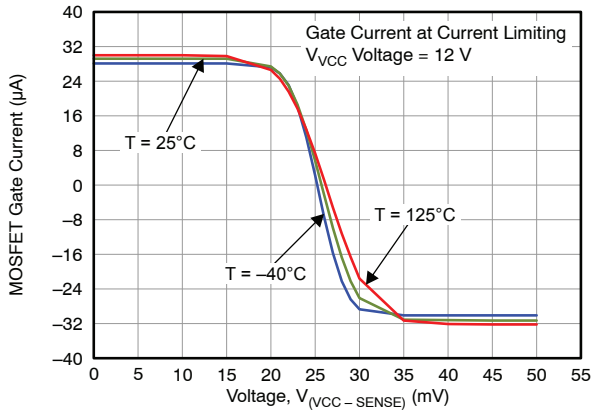



**Figure 8. Gate Current vs Voltage Across $R_{SENSE}$ During Inrush Current Limiting**

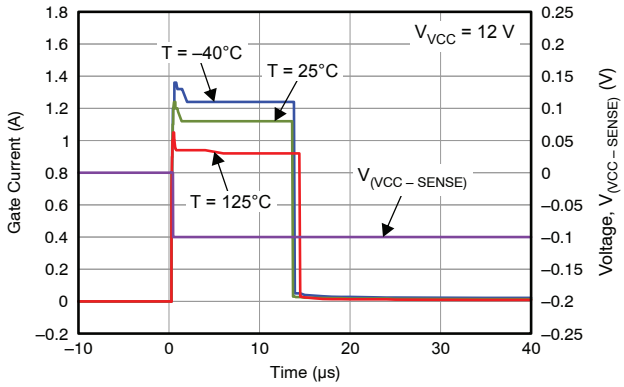



**Figure 9. Gate Current During Fast Trip, $V_{VCC} = V_{GATE} = 12$ V**

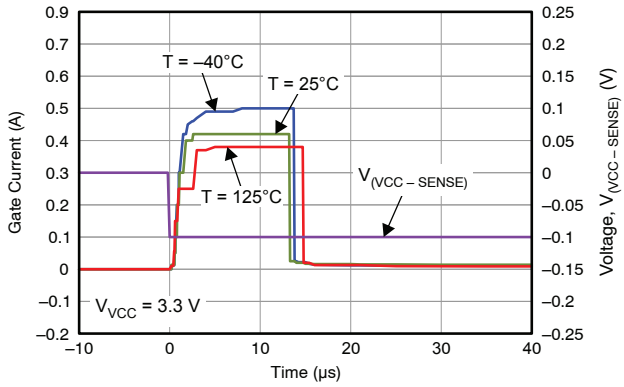



**Figure 10. Gate Current During Fast Trip, $V_{VCC} = V_{GATE} = 3.3$ V**


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## TYPICAL CHARACTERISTICS (continued)

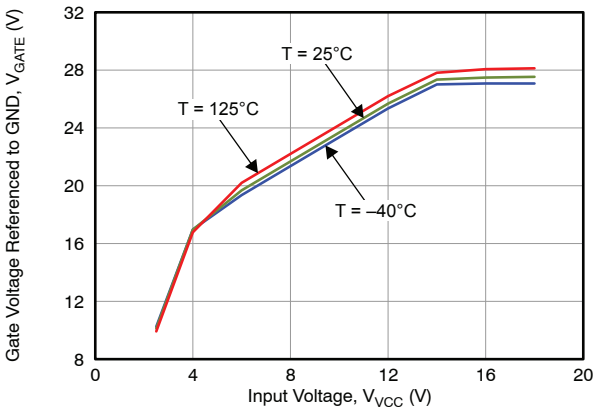



**Figure 11. Gate Voltage With Zero Gate Current vs $V_{VCC}$**

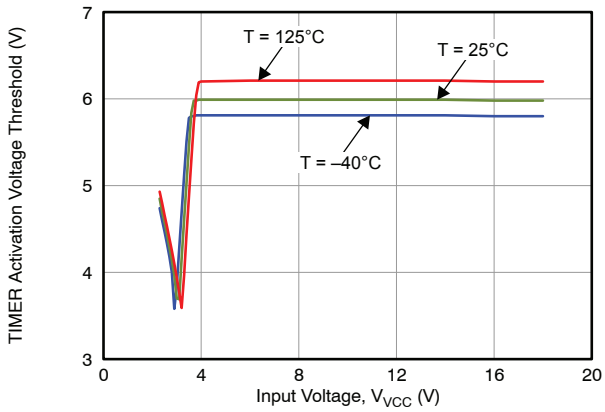



**Figure 12. TIMER Activation Voltage Threshold vs $V_{VCC}$ at Various Temperatures**

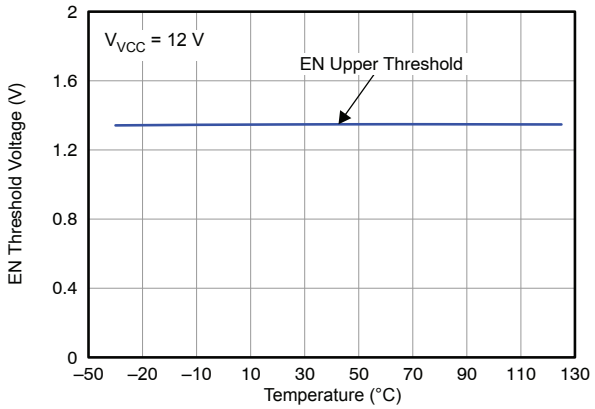



**Figure 13. EN Threshold Voltage vs Temperature**

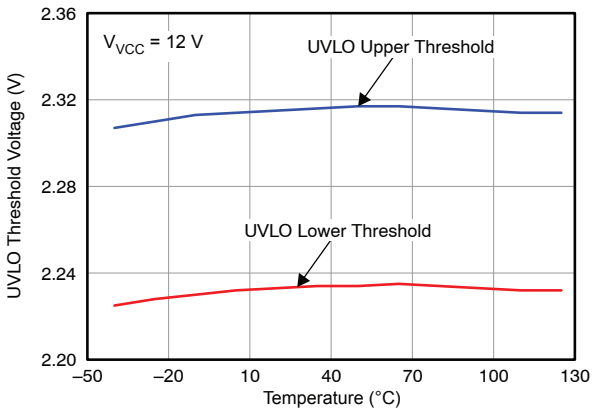



**Figure 14. UVLO Threshold Voltages vs Temperature**

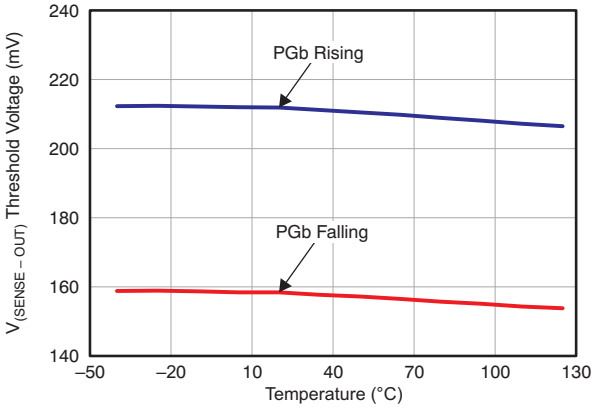



**Figure 15. Threshold of $V_{DS}$ vs Temperature, PGb Rising and Falling**

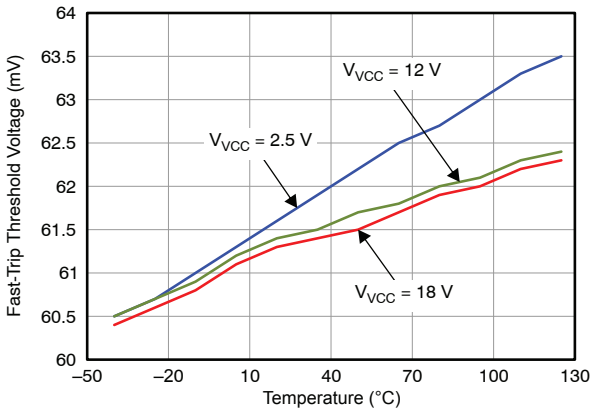



**Figure 16. Fast-Trip Threshold vs Temperature**

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## TYPICAL CHARACTERISTICS (continued)

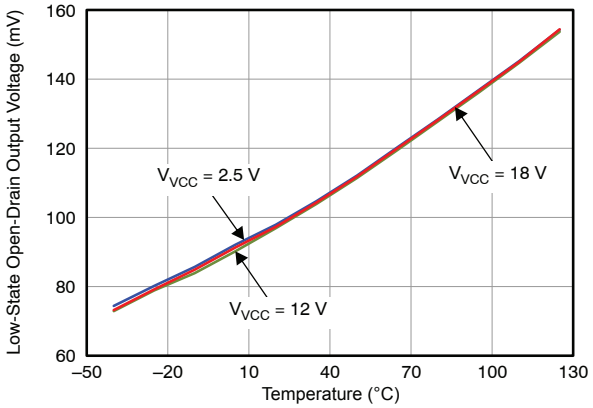



**Figure 17. PGb Open-Drain Output Voltage in Low State**

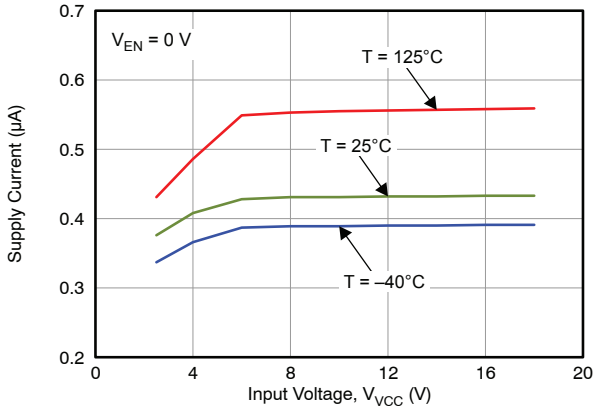



**Figure 18. Supply Current vs $V_{VCC}$ and Temperature When EN Pulled Low**

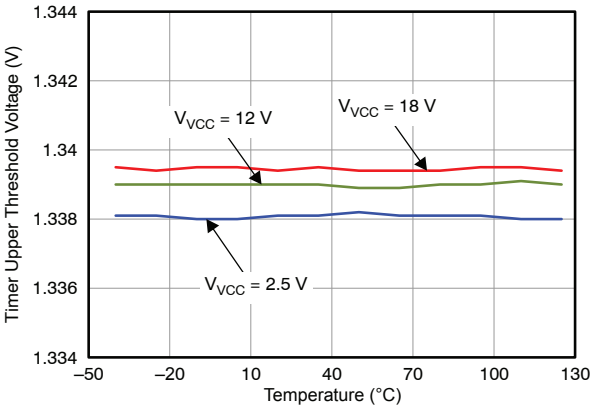



**Figure 19. Timer Upper Threshold vs $V_{VCC}$ and Temperature**

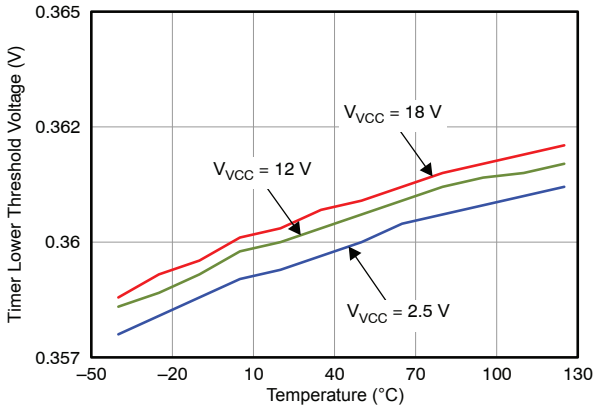



**Figure 20. Timer Lower Threshold vs $V_{VCC}$ and Temperature**

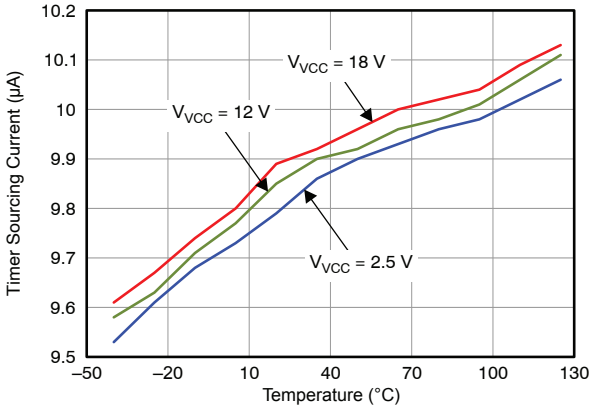



**Figure 21. Timer Sourcing Current vs $V_{VCC}$ and Temperature**

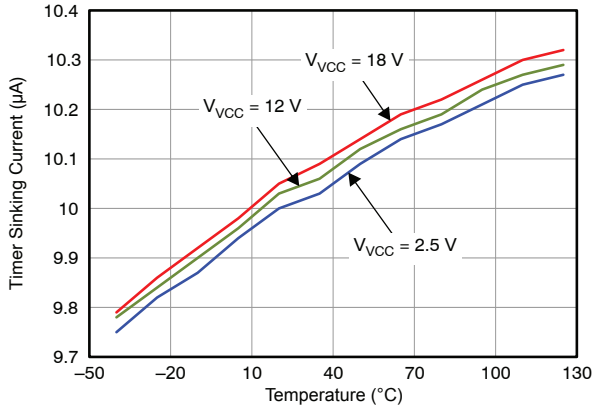



**Figure 22. Timer Sinking Current vs $V_{VCC}$ and Temperature**


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# SYSTEM OPERATION

## INTRODUCTION

The TPS24700/1 provides all the features needed for a positive hot-swap controller. These features include:

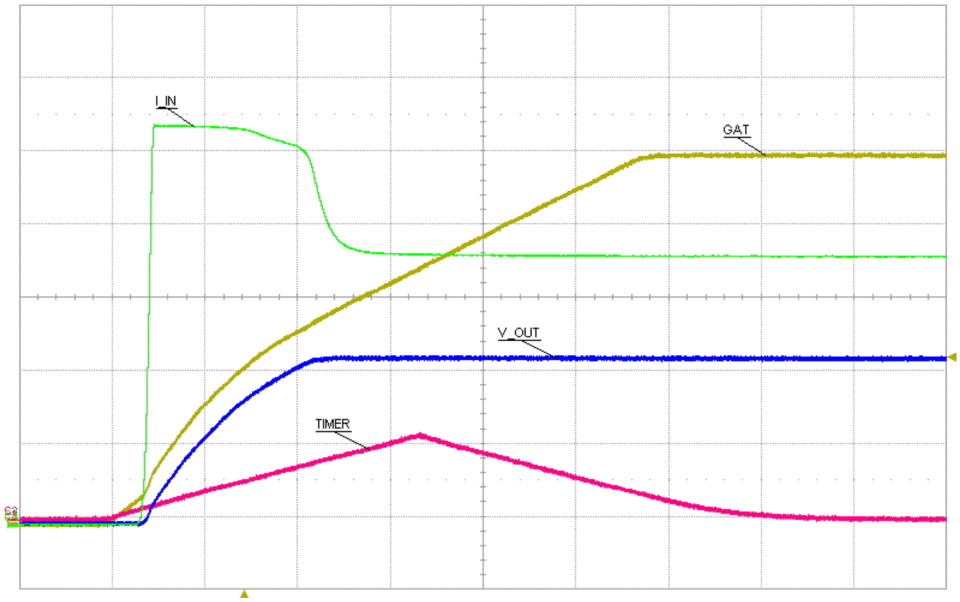
- Undervoltage lockout
- Adjustable (system-level) enable
- Turn-on inrush limiting
- High-side gate drive for an external N-channel MOSFET
- Adjustable overload timeout — also called an electronic circuit breaker
- Charge-complete indicator for downstream converter coordination
- A choice of latch (TPS24700) or automatic restart mode (TPS24701)

The typical application circuit, shown on the front page of this datasheet, and oscilloscope plots, shown in Figure 23 through Figure 24 and Figure 26 through Figure 28, demonstrate many of the functions described previously.

## BOARD PLUG IN

Figure 23 illustrates the inrush current that flows when a hot-swap board under the control of the TPS24700/1 is plugged into an input power bus. Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. The TPS24700/1 is held inactive for a short period while internal voltages stabilize. In this short period, GATE and TIMER are held low and PGb is held open-drain. When the voltage on the internal VCC rail exceeds approximately 1.5 V, the power-on reset (POR) circuit initializes the TPS24700/1 and a start-up cycle is ready to take place.

GATE, TIMER, and PGb are released after the internal voltages have stabilized and the external EN (enable) threshold has been exceeded. The part begins sourcing current from the GATE pin to turn on MOSFET M1. The TPS24700/1 monitors the drain current passing through MOSFET M1 by measuring the voltage $V_{(VCC - SENSE)}$. Based on the measurement, the TPS24700/1 limits the drain current in the MOSFET to be no more than the current limit $I_{LIM}$, so as to alleviate the charging impact of the downstream bulk storage capacitors.




I_IN: Input Current, 2 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_OUT: Voltage on OUT Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

C001

**Figure 23. Inrush Mode at Hot-Swap Circuit Insertion**

## INRUSH OPERATION

When the TPS2470/1 activates MOSFET M1, a current flows into the downstream bulk storage capacitors. When this current exceeds the limit threshold set by Equation 1, the gate of the MOSFET is regulated by a feedback loop to make the MOSFET current stay at a current level no more than the current limit threshold. This limits the inrush current charging capacitance. The TIMER pin begins to charge the timing capacitor $C_T$ with a current of approximately 10 µA. The TIMER pin continues to charge $C_T$ until $V_{(GATE–VCC)}$ reaches the timer activation voltage (6 V for $V_{VCC}$ = 12 V). The TIMER then begins to discharge $C_T$ with a current of approximately 10 µA. This indicates that the inrush mode is finished. If the TIMER exceeds its upper threshold of 1.35 V before $V_{(GATE–VCC)}$ reaches the timer activation voltage, the GATE pin is pulled to GND and the hot-swap circuit enters either latch mode (TPS24700) or auto-retry mode (TPS24701).

The current limit feature is disabled once the inrush operation is finished and the hot-swap circuit becomes a circuit breaker. The TPS24700/1 turns off the MOSFET, M1, after a fault timer period once the load exceeds the current limit threshold.

## CIRCUIT BREAKER AND FAST TRIP

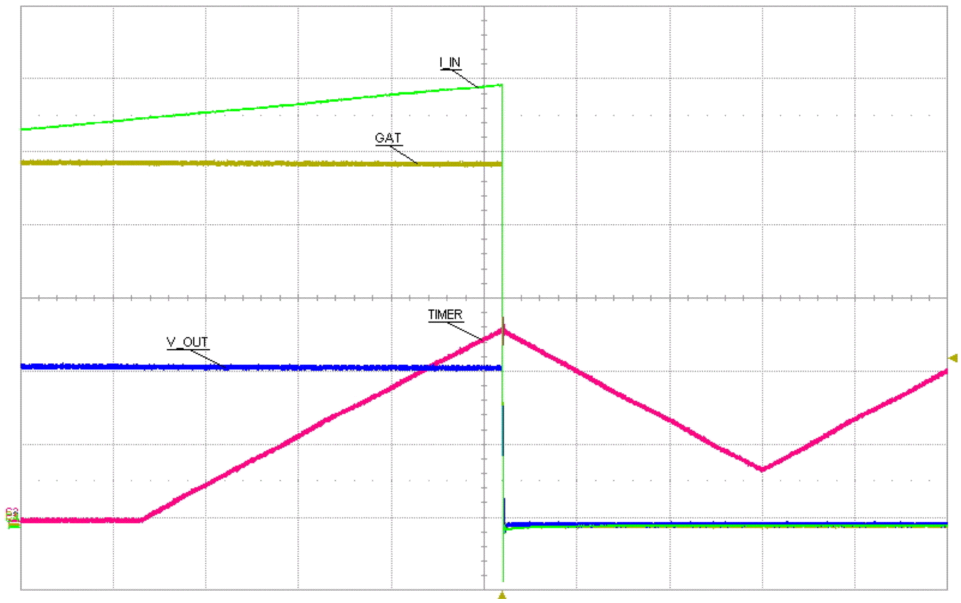
The TPS24700/1 monitors load current by sensing the voltage across $R_{SENSE}$. The TPS24700/1 incorporates two distinct thresholds: a current-limit threshold and a fast-trip threshold.

Figure 24 shows the behavior of the TPS24700/1 when a fault in the output load causes the current passing through $R_{SENSE}$ to increase to a value above the current limit but less than the fast-trip threshold. When the current exceeds the current-limit threshold, a current of approximately 10 µA begins to charge timing capacitor $C_T$. If the voltage on $C_T$ reaches 1.35 V, then the external MOSFET is turned off. The TPS24700 latches off and the TPS24701 commences a restart cycle. Overload between the current limit and the fast-trip threshold is permitted for this period. This shutdown scheme is sometimes called an electronic circuit breaker.

The fast-trip threshold protects the system against a severe overload or a dead short circuit. When the voltage across the sense resistor $R_{SENSE}$ exceeds the 60-mV fast-trip threshold, the GATE pin immediately pulls the external MOSFET gate to ground with approximately 1 A of current. This extremely rapid shutdown may generate disruptive transients in the system, in which case a low-value resistor inserted between the GATE pin and the MOSFET gate can be used to moderate the turnoff current. The fast-trip circuit holds the MOSFET off for only a few microseconds, after which the TPS24700/1 turns back on slowly, allowing the current-limit feedback loop to take over the gate control of M1. Then the hot-swap circuit goes into either latch mode (TPS24700) or auto-retry mode (TPS24701). Figure 26 and Figure 27 illustrate the behavior of the system when the current exceeds the fast-trip threshold.

The functions of circuit breaker and fast-trip turnoff are shown in Figure 24 through Figure 27.

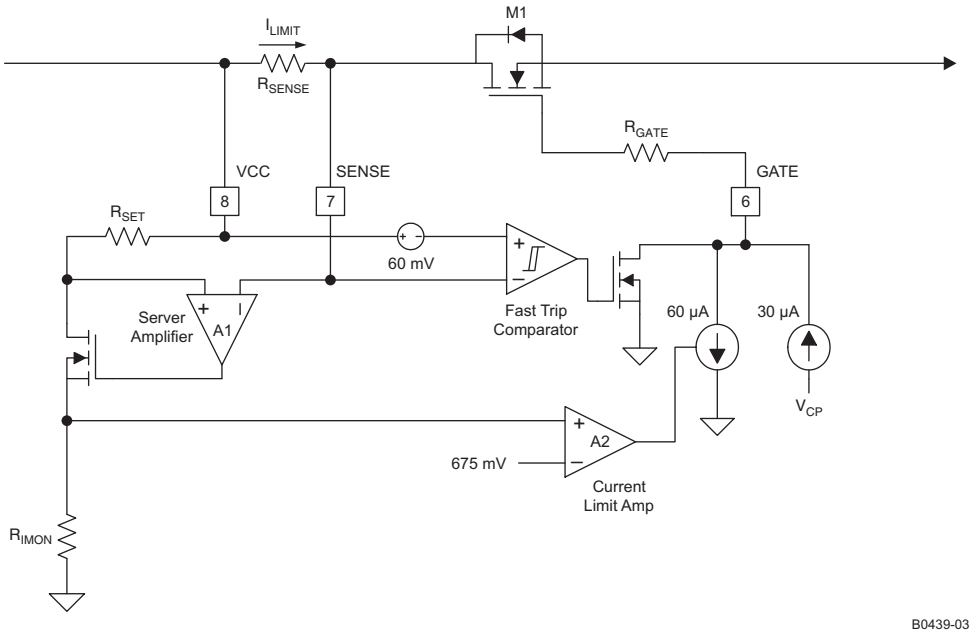

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I_IN: Input Current, 2 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_OUT: Voltage on OUT Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

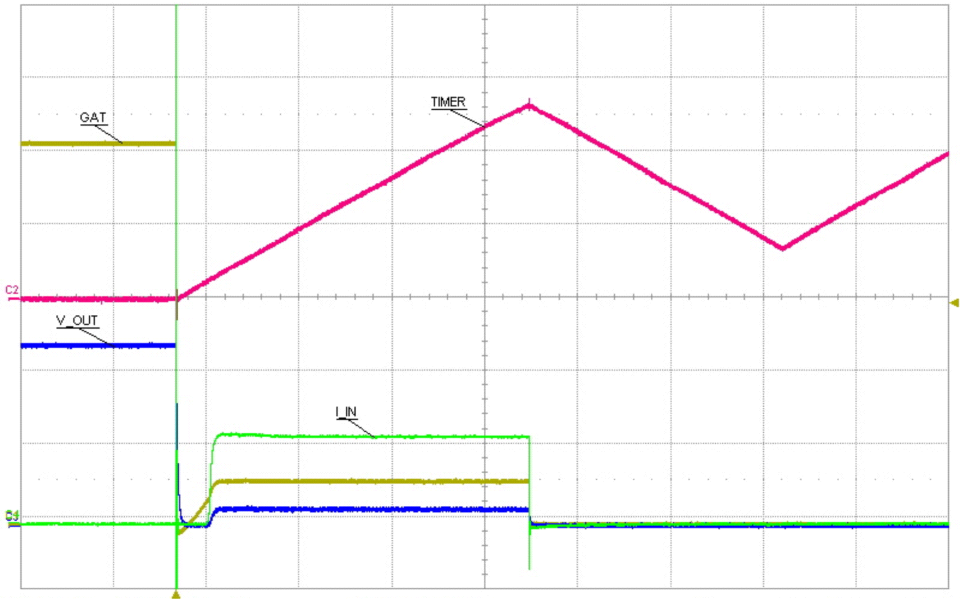
C003

**Figure 24. Circuit-Breaker Mode During Overload Condition**




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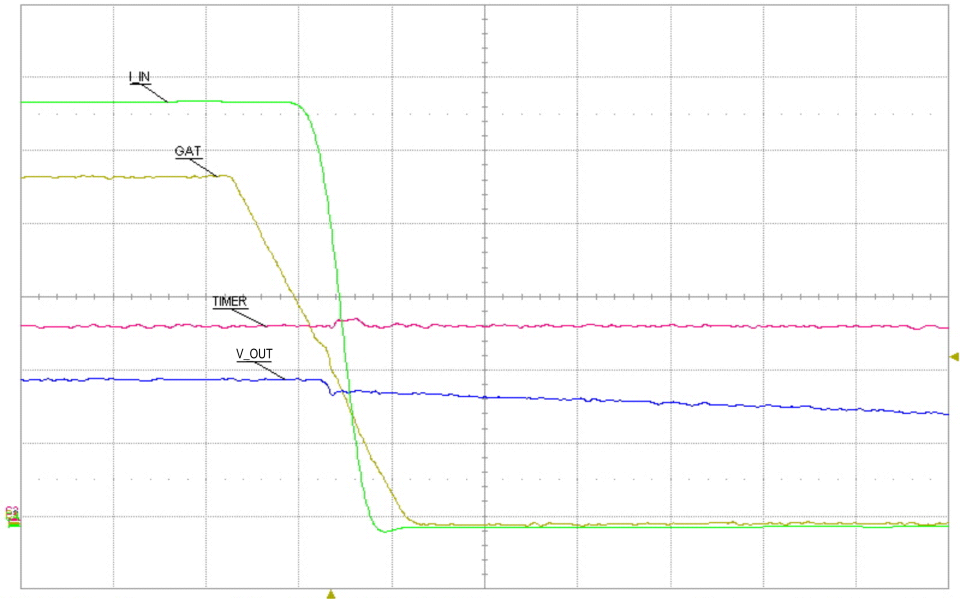
**Figure 25. Partial Diagram of the TPS24700/1 With Selected External Components**




I_IN: Input Current, 1 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_OUT: Voltage on OUT Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

C004

**Figure 26. Current Limit During Output Load Short-Circuit Condition (Overview)**




I_IN: Input Current, 5 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_OUT: Voltage on OUT Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 10 µs/div

C005

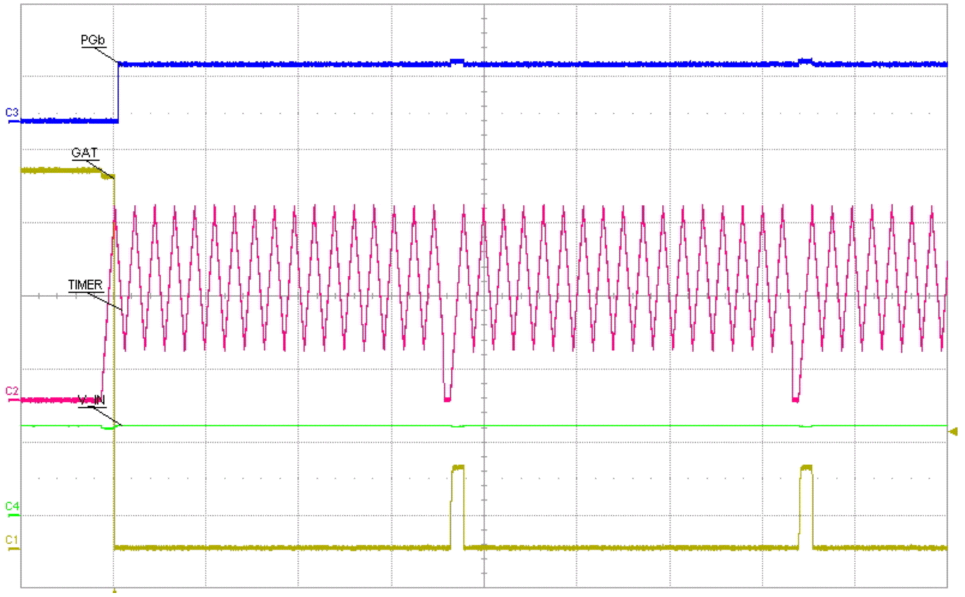
**Figure 27. Current Limit During Output-Load Short-Circuit Condition (Onset)**

## AUTOMATIC RESTART

The TPS24701 automatically initiates a restart after a fault has caused it to turn off the external MOSFET M1.


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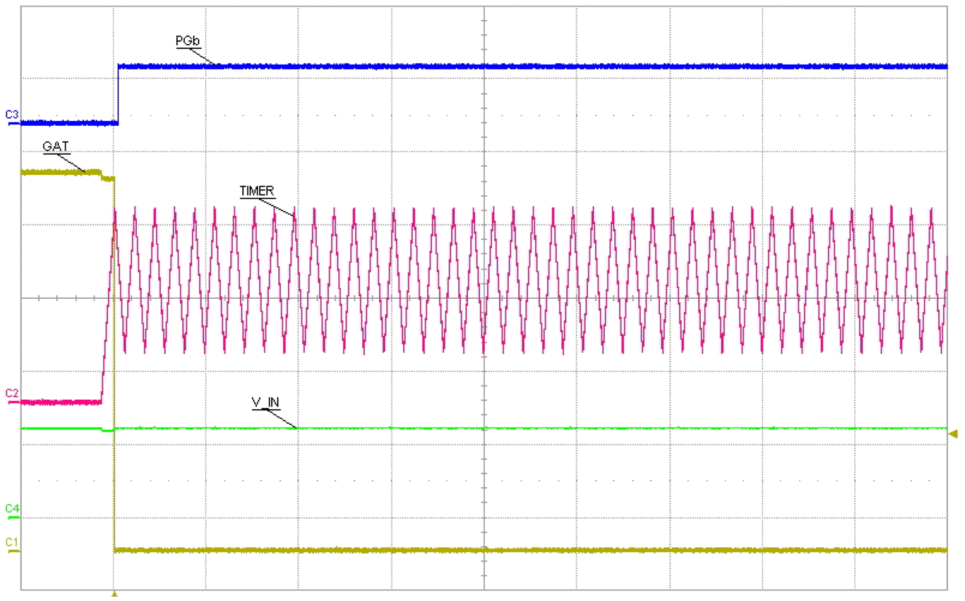
Internal control circuits use $C_T$ to count 16 cycles before re-enabling M1 as shown in Figure 28. This sequence repeats if the fault persists. The timer has a 1 : 1 charge-to-discharge current ratio. For the very first cycle, the TIMER pin starts from 0 V and rises to the upper threshold of 1.35 V and subsequently falls to 0.35 V before restarting. For the following 16 cycles, 0.35 V is used as the lower threshold. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.




V_IN: Input Voltage, 10 V/div
GAT: Voltage on GATE Pin, 5 V/div
PGb: Voltage on PGb Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 50 ms/div

C006

**Figure 28. Auto-Restart Cycle Timing**




V_IN: Input Voltage, 10 V/div
GAT: Voltage on GATE Pin, 5 V/div
PGb: Voltage on PGb Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 50 ms/div

C007

**Figure 29. Latch After Overload Fault**

## PGb AND TIMER OPERATIONS

The open-drain PGb output provides a deglitched end-of-inrush indication based on the voltage across M1. PGb is useful for preventing a downstream dc/dc converter from starting while its input capacitor $C_{OUT}$ is still charging. PGb goes active-low about 3.4 ms after $C_{OUT}$ is charged. This delay allows M1 to fully turn on and any transients in the power circuits to end before the converter starts up. This type of sequencing prevents the downstream converter from demanding full current before the current-limit engine allows the MOSFET to conduct the full current set by the current limit $I_{LIM}$. Failure to observe this precaution may prevent the system from starting. The pullup resistor shown on the PGb pin in the typical application diagram (front page) is illustrative only; the actual connection to the converter depends on the application. The PGb pin may indicate that inrush has ended before the MOSFET is fully enhanced, but the downstream capacitor will have been charged to substantially its full operating voltage. Care should be taken to ensure that the MOSFET on-resistance is sufficiently small to ensure that the voltage drop across this transistor is less than the minimum power-good threshold of 140 mV. After the hot-swap circuit successfully starts up, the PGb pin can return to a high-impedance status whenever the drain-to-source voltage of MOSFET M1 exceeds its upper threshold of 340 mV, which presents the downstream converters a warning flag. This flag may occur as a result of overload fault, output short fault, high die temperature, or the GATE shutdown by UVLO and EN.

The fault-timer defines an allowed period during which the load current can exceed the programmed current limit (but not the fast-trip threshold). The fault timer starts when a current of approximately 10 µA begins to flow into the external capacitor, $C_T$, and ends when the voltage of $C_T$ reaches TIMER upper threshold, i.e., 1.35 V. The fault-timer state requires an external capacitor $C_T$ connected between the TIMER pin and GND pin. The length of the fault timer is the charging time of $C_T$ from 0 V to its upper threshold of 1.35 V. The fault timer begins to count under any of the following three conditions:

- In the inrush mode, TIMER begins to source current to the timer capacitor, $C_T$, when MOSFET M1 is enabled. TIMER begins to sink current from the timer capacitor, $C_T$ when $V_{(GATE–VCC)}$ exceeds the timer activation voltage (see the *Inrush Operation* section). If $V_{(GATE–VCC)}$ does not reach the timer activation voltage before TIMER reaches 1.35 V, then the TPS24700/1 disables the external MOSFET M1. After the MOSFET turns off, the timer goes into either latch mode (TPS24700) or retry mode (TPS24701).


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- In an overload fault, TIMER begins to source current to the timer capacitor, $C_T$, when the load current exceeds the programmed current limits. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, $C_T$, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode (TPS24700) or retry mode (TPS24701).
- In output short-circuit fault, TIMER begins to source current to the timer capacitor, $C_T$, when the load current exceeds the current-limit threshold following a fast-trip shutdown of M1. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, $C_T$, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode (TPS24700) or retry mode (TPS24701).

If the fault current drops below the current limit falling threshold within the fault timer period, $V_{TIMER}$ decreases and the pass MOSFET, M1, remains enabled.

The behaviors of TIMER are different in the latch mode (TPS24700) and retry mode (TPS24701). If the timer capacitor reaches the upper threshold of 1.35 V, then:

- In latch mode, the TIMER pin continues to charge and discharge the attached capacitor periodically until TPS24700 is disabled by UVLO or EN as shown in Figure 29.
- In retry mode, TIMER charges and discharges $C_T$ between the lower threshold of 0.35 V and the upper threshold of 1.35 V for sixteen cycles before the TPS24701 attempts to restart. The TIMER pin is pulled to GND at the end of the $16^{th}$ cycle of charging and discharging and then ramps from 0 V to 1.35 V for the initial half-cycle in which the GATE pin sources current. This periodic pattern is stopped once the overload fault is removed or the TPS24701 is disabled by UVLO or EN.

## OVERTEMPERATURE SHUTDOWN

The TPS24700/1 includes a built-in overtemperature shutdown circuit designed to disable the gate driver if the die temperature exceeds approximately 140°C. An overtemperature condition also causes the PGb pin to go to the high-impedance state. Normal operation resumes once the die temperature has fallen approximately 10°C.

## START-UP OF HOT-SWAP CIRCUIT BY VCC OR EN

The connection and disconnection between a load and the input power bus are controlled by turning on and turning off the MOSFET, M1.

The TPS24700/1 has two ways to turn on MOSFET M1:

- Increasing $V_{VCC}$ above the UVLO upper threshold while EN is already higher than its upper threshold sources current to the GATE pin. After an inrush period, the TPS24700/1 fully turns on MOSFET M1.
- Increasing EN above its upper threshold while $V_{VCC}$ is already higher than the UVLO upper threshold sources current to the GATE pin. After an inrush period, TPS24700/1 fully turns on MOSFET M1.

The EN pin can be used to start up the TPS24700/1 at a selected input voltage $V_{VCC}$.

To isolate the load from the input power bus, the GATE pin sinks current and pulls the gate of MOSFET M1 low. The MOSFET can be disabled by any of the following conditions: UVLO, EN, load current above current limit threshold, hard short at load, or OTSD. Three separate mechanisms pull down the GATE pin:

1. GATE is pulled down by an 11-mA current source when any of the following occurs.
   - The fault timer expires during an overload current fault ($V_{SENSE}$ > 25 mV).
   - $V_{EN}$ is below its falling threshold.
   - $V_{VCC}$ drops below the UVLO falling threshold.
2. GATE is pulled down by a 1-A current source for 13.5 µs when a hard output short circuit occurs and $V_{(VCC–SENSE)}$ is greater than 60 mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the external MOSFET remains off.
3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

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## DESIGN EXAMPLE: CURRENT-LIMITED START-UP

This design example assumes a 12-V system voltage with an operating tolerance of ±2 V. The rated load current is 10 A, corresponding to a dc load of 1.2 Ω. If the current exceeds 12 A, then the controller should shut down and then attempt to restart. Ambient temperatures may range from 20°C to 50°C. The load has a minimum input capacitance of 470 µF. Figure 30 shows a simplified system block diagram of the proposed application.

This design procedure seeks to control the junction temperature of MOSFET M1 under both static and transient conditions by proper selection of package, cooling, $r_{DS(on)}$, current limit, fault timeout, and power limit. The design procedure further assumes that a unit running at full load and maximum ambient temperature experiences a brief input power interruption sufficient to discharge $C_{OUT}$, but short enough to keep M1 from cooling. A full $C_{OUT}$ recharge then takes place. Adjust this procedure to fit your application and design criteria.

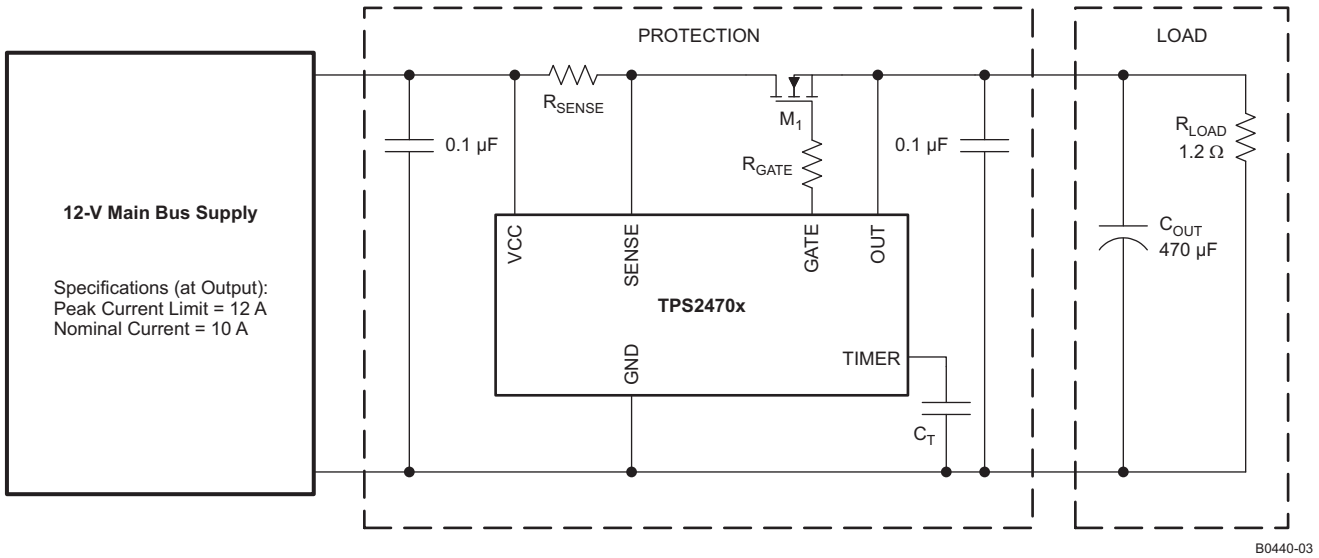



**Figure 30. Simplified Block Diagram of the System Constructed in the Design Example**

### STEP 1. Choose $R_{SENSE}$

From the TPS24700/1 electrical specifications, the typical current-limit threshold voltage, $V_{(VCC–SENSE)}$, is 25 mV. A resistance of 2 mΩ is selected for the peak current limit of 12 A, while dissipating only 200 mW at the rated 10-A current (see Equation 3). This represents a 0.17% power loss.

$$R_{SENSE} = \frac{V_{(VCC-SENSE)}}{I_{LIM}},$$

therefore,

$$R_{SENSE} = \frac{25\ mV}{12\ A} \approx 2\ m\Omega \quad (3)$$

### STEP 2. Choose MOSFET M1

The next design step is to select M1. The TPS24700/1 is designed to use an N-channel MOSFET with a gate-to-source voltage rating of 20 V.

Devices with lower gate-to-source voltage ratings can be used if a Zener diode is connected to limit the maximum gate-to-source voltage across the transistor.

The next factor to consider is the drain-to-source voltage rating, $V_{DS(MAX)}$, of the MOSFET. Although the MOSFET only sees 12 V dc, it may experience much higher transient voltages during extreme conditions, such as the abrupt shutoff that occurs during a fast trip. A TVS may be required to limit inductive transients under such conditions. A transistor with a $V_{DS(MAX)}$ rating of at least twice nominal input power supply voltage is recommended regardless of whether a TVS is used or not.


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Next select the on resistance of the transistor, $r_{DS(on)}$. The maximum on-resistance must not generate a voltage greater then the minimum power-good threshold voltage of 140 mV. Assuming a current limit of 12 A, a maximum $r_{DS(on)}$ of 11.67 mΩ is required. Also consider the effect of $r_{DS(on)}$ upon the maximum operating temperature $T_{J(MAX)}$ of the MOSFET. Equation 4 computes the value of $r_{DS(on)(MAX)}$ at a junction temperature of $T_{J(MAX)}$. Most manufacturers list $r_{DS(on)(MAX)}$ at 25°C and provide a derating curve from which values at other temperatures can be derived. Compute the maximum allowable on-resistance, $r_{DS(on)(MAX)}$, using Equation 4.

$$r_{DS(on)(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{I_{MAX}^2 \times R_{\theta JA}},$$

therefore,

$$r_{DS(on)(MAX)} = \frac{150°C - 50°C}{(12\ A)^2 \times 51°C/W} = 13.6\ m\Omega \quad (4)$$

Taking these factors into consideration, the TI CSD16403Q5 was selected for this example. This transistor has a $V_{GS(MAX)}$ rating of 16 V, a $V_{DS(MAX)}$ rating of 25 V, and a maximum $r_{DS(on)}$ of 2.8 mΩ at room temperature. During normal circuit operation, the MOSFET can have up to 10 A flowing through it. The power dissipation of the MOSFET equates to 0.24 W and a 9.6°C rise in junction temperature. This is well within the data sheet limits for the MOSFET. The power dissipated during a fault (e.g., output short) is far larger than the steady-state power. The power handling capability of the MOSFET must be checked during fault conditions.

**STEP 3. Choose Output Voltage Rising Time, $t_{ON}$, $C_T$**

The maximum output voltage rise time, $t_{ON}$, set by the timer capacitor $C_T$ must suffice to fully charge the load capacitance $C_{OUT}$ without triggering the fault circuitry. Equation 5 defines $t_{ON}$, where $V_{CC(MAX)}$ is the maximum input power bus voltage value and $I_{LIM}$ is the current limit value.

$$t_{ON} = \frac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} \quad \text{if} \quad P_{LIM} > I_{LIM} \times V_{VCC(MAX)}$$

therefore,

$$t_{ON} = \frac{470\ \mu F \times 12\ V}{12\ A} = 0.47\ ms \quad (5)$$

The next step is to determine the minimum fault-timer period. In Equation 5, the output rise time, $t_{ON}$, is the amount of time it takes to charge the output capacitor up to the final output voltage. However, the fault timer uses the difference between the input voltage and the gate voltage to determine if the TPS24700/1 is still in inrush limit. The fault timer continues to run until $V_{GATE}$ rises 6 V above the input voltage (for $V_{VCC}$ = 12 V). Some additional time must be added to the total time to account for this additional gate voltage rising. The minimum fault time can be calculated using Equation 6,

$$t_{FLT} = t_{ON} + \frac{6\ V \times C_{ISS}}{I_{GATE}},$$

therefore,

$$t_{FLT} = 0.47\ ms + \frac{6\ V \times 2040\ pF}{20\ \mu A} = 1.08\ ms \quad (6)$$

where $C_{ISS}$ is the MOSFET input capacitance and $I_{GATE}$ is the minimum gate sourcing current of TPS24700, or 20 µA. Using the example parameters in Equation 6 and the CSD16403Q5 data sheet leads to a minimum fault time of 1.08 ms. This time is derived considering the tolerances of $C_{OUT}$, $C_{ISS}$, $I_{LIM}$, $I_{GATE}$, $C_{OUT}$, and $V_{VCC}$. The fault timer must be set to a value higher than 1.08 ms to avoid turning off during start-up, but lower than any maximum fault time limit determined by the device SOA curve.

There is a maximum time limit set by the SOA curve of the MOSFET. Referring to Figure 31, which shows the

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CSD16403Q5 SOA curve at $T_J$ = 25°C, the MOSFET can tolerate 12 A with 12 V across it for approximately 20 ms. If the junction temperature $T_J$ is other than 25°C, then the pulse time should be scaled by a factor of (150°C – $T_J$) / (150°C – 25°C). Therefore, the fault timer should be set between 1.08 ms and 20 ms. For this example, we will select 7 ms to allow for variation of system parameters such as temperature, load, component tolerance, and input voltage. The timing capacitor is calculated in Equation 2 as 52 nF. Selecting the next-highest standard value, 56 nF, yields a 7.56-ms fault time (see Equation 7).

$$C_T = \frac{10\ \mu A}{1.35\ V} \times t_{FLT},$$

therefore,

$$C_T = \frac{10\ \mu A}{1.35\ V} \times 7\ ms = 52\ nF \tag{7}$$

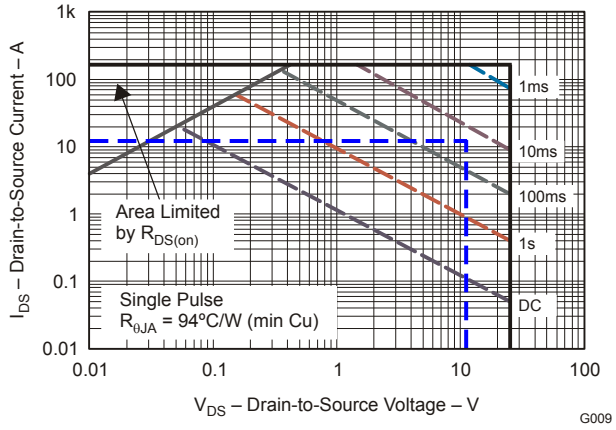



**Figure 31. CSD16403Q5 SOA Curve**

### STEP 4. Calculate the Retry-Mode Duty Ratio

In retry mode, the TPS24701 is on for one charging cycle and off for 16 charge/discharge cycles, as can be seen in Figure 28. The first $C_T$ charging cycle is from 0 V to 1.35 V, which gives 7.56 ms. The first $C_T$ discharging cycle is from 1.35 V to 0.35 V, which gives 5.6 ms. Therefore, the total time is 7.56 ms + 33 × 5.6 ms = 192.36 ms. As a result, the retry mode duty ratio is 7.56 ms/192.36 ms = 3.93%.

### STEP 5. Select R1 and R2 for UV

Next, select the values of the UV resistors, $R_1$ and $R_2$, as shown in the application diagram on the front page. From the TPS24700/1 electrical specifications, $V_{ENTHRESH}$ = 1.35 V. The $V_{UV}$ is the undervoltage trip voltage, which for this example equals 10.8 V.

$$V_{ENTHRESH} = \frac{R_2}{R_1 + R_2} \times V_{VCC} \tag{8}$$

Assume $R_1$ is 130 kΩ and use Equation 8 to solve for the $R_2$ value of 18.7 kΩ.

### STEP 6. Choose $R_{GATE}$, $R_4$ and $C_1$

In the application diagram on the front page, the gate resistor, $R_{GATE}$, is intended to suppress high-frequency oscillations. A resistor of 10 Ω serves for most applications, but if M1 has a $C_{ISS}$ below 200 pF, then 33 Ω is recommended. Applications with larger MOSFETs and very short wiring may not require $R_{GATE}$. $R_4$ is required only if PGb is used; this resistor serves as a pullup for the open-drain output driver. The current sunk by PGb pin should not exceed 2 mA. $C_1$ is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended.

## ALTERNATIVE DESIGN EXAMPLE: GATE CAPACITOR (dV/dt) CONTROL IN INRUSH MODE


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The TPS24700/1 can be used in applications that expect a constant inrush current. This current is controlled by a capacitor connected from the GATE terminal to GND. A resistor of 1 kΩ placed in series with this capacitor prevents it from slowing a fast-turnoff event. In this mode of operation, M1 operates as a source follower, and the slew rate of the output voltage approximately equals the slew rate of the gate voltage (see Figure 32).

To implement a constant-inrush-current circuit, choose the time to charge, $\Delta t$, using Equation 9,

$$\Delta t = \frac{C_{OUT} \times V_{VCC}}{I_{CHG}} \tag{9}$$

where $C_{OUT}$ is the output capacitance, $V_{VCC}$ is the input voltage, and $I_{CHG}$ is the desired $C_{OUT}$ charge current.

To select the gate capacitance use Equation 10.

$$C_{GATE} = \left( I_{GATE} \times \frac{\Delta t}{V_{VCC}} \right) - C_{ISS} \tag{10}$$

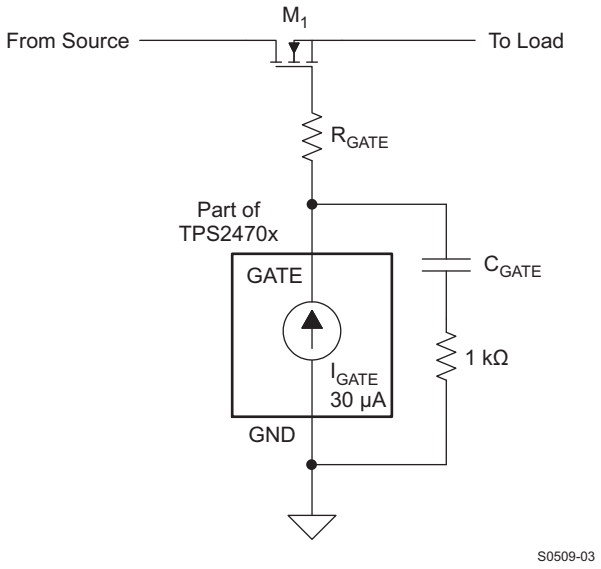



**Figure 32. Gate Capacitor (dV/dt) Control Inrush Mode**

## ADDITIONAL DESIGN CONSIDERATIONS

### Use of PGb

Use the PGb pin to control and coordinate a downstream dc/dc converter. If this is not done, then a long time delay is needed to allow $C_{OUT}$ to fully charge before the converter starts. An undesirable latch-up condition can be created between the TPS24700/1 output characteristic and the dc/dc converter input characteristic if the converter starts while $C_{OUT}$ is still charging; the PGb pin is one way to avoid this.

### Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current-limit event. The OUT pin ratings can be satisfied by connecting a diode from OUT to GND. The diode should be selected to control the negative voltage at the full short-circuit current. Schottky diodes are generally recommended for this application.

### Gate Clamp Diode

The TPS24700/1 has a relatively well-regulated gate voltage of 12 V to 15.5 V with a supply voltage $V_{VCC}$ higher than 4 V. A small clamp Zener from gate to source of M1 is recommended. A series resistance of several hundred ohms or a series silicon diode is recommended to prevent the output capacitance from discharging through the gate driver to ground.

### High-Gate-Capacitance Applications

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Gate voltage overstress and abnormally large fault current spikes can be caused by large gate capacitance. An external gate clamp Zener diode is recommended to assist the internal Zener if the total gate capacitance of M1 exceeds about 4000 pF. When gate capacitor dV/dt control is used, a 1-kΩ resistor in series with $C_G$ is recommended. If the series R-C combination is used for MOSFETs with $C_{ISS}$ less than 3000 pF, then a Zener is not necessary.

### Bypass Capacitors

It is a good practice to provide low-impedance ceramic capacitor bypassing of the VCC and OUT pins. Values in the range of 10 nF to 1 µF are recommended. Some system topologies are insensitive to the values of these capacitors; however, some are not and require minimization of the value of the bypass capacitor. Input capacitance on a plug-in board may cause a large inrush current as the capacitor charges through the low-impedance power bus when inserted. This stresses the connector contacts and causes a brief voltage sag on the input bus. Small amounts of capacitance (e.g., 10 nF to 0.1 µF) are often tolerable in these systems.

### Output Short-Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

### Layout Considerations

TPS24700/1 applications require careful attention to layout to ensure proper performance and to minimize susceptibility to transients and noise. In general, all traces should be as short as possible, but the following list deserves first consideration:

- Decoupling capacitors on VCC pin should have minimal trace lengths to the pin and to GND.
- Traces to VCC and SENSE must be short and run side-by-side to maximize common-mode rejection. Kelvin connections should be used at the points of contact with $R_{SENSE}$. (see Figure 33).
- Power path connections should be as short as possible and sized to carry at least twice the full load current, more if possible.
- The device dissipates low power, so soldering the thermal pad to the board is not a requirement. However, doing so improves thermal performance and reduces susceptibility to noise.
- Protection devices such as snubbers, TVS, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, the protection Schottky diode shown in the application diagram on the front page of the data sheet should be physically close to the OUT pin.


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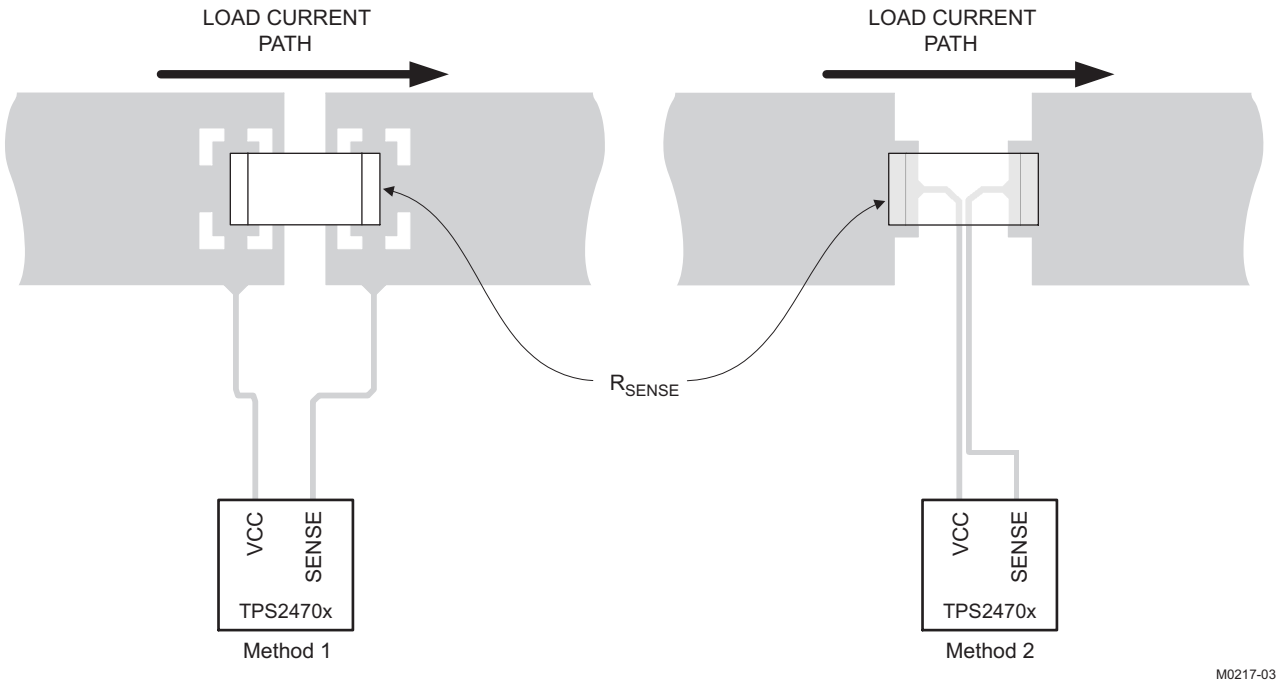



**Figure 33. Recommended $R_{SENSE}$ Layout**

## REVISION HISTORY

| Changes from Revision Original (April 2011) to Revision A | Page |
|---|---|
| • Revised voltage values shown in the block diagram | 5 |

| Changes from Revision A (April 2011) to Revision B | Page |
|---|---|
| • Changed in DETAILED PIN DESCRIPTIONS - **PGb:** from 140mV / 340mV to 170mV / 240 mV | 6 |


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS24700DGK | Active | Production | VSSOP (DGK) \| 8 | 80 \| TUBE | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | 24700 |
| TPS24700DGK.A | Active | Production | VSSOP (DGK) \| 8 | 80 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 24700 |
| TPS24700DGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | 24700 |
| TPS24700DGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 24700 |
| TPS24701DGK | Active | Production | VSSOP (DGK) \| 8 | 80 \| TUBE | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | 24701 |
| TPS24701DGK.A | Active | Production | VSSOP (DGK) \| 8 | 80 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 24701 |
| TPS24701DGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | 24701 |
| TPS24701DGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 24701 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

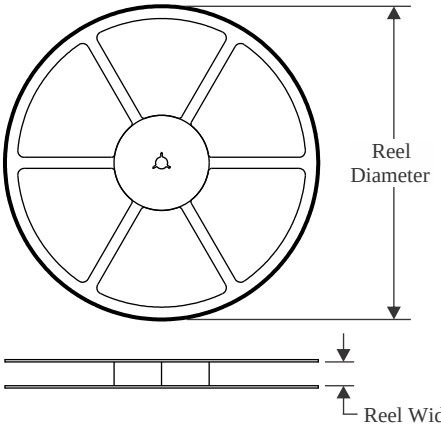
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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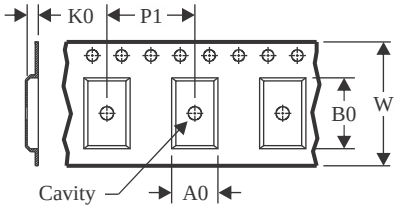
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

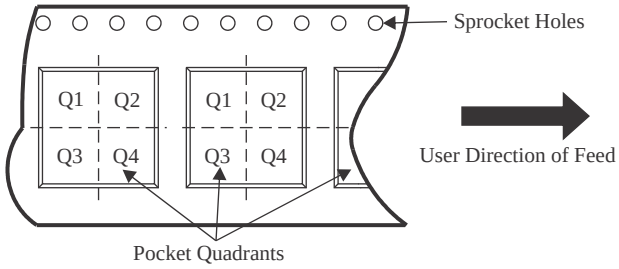



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

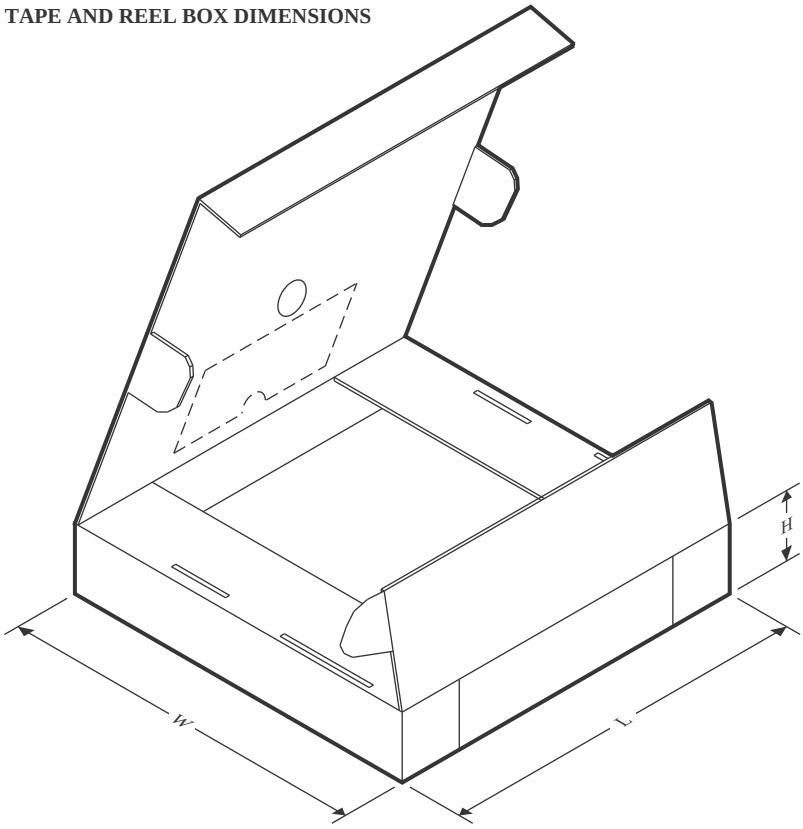
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS24700DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS24700DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS24701DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS24701DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

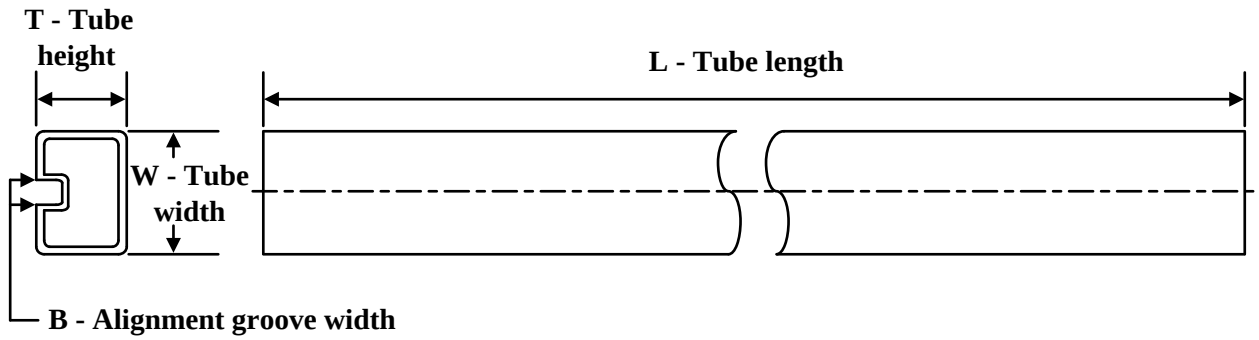
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS24700DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS24700DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TPS24701DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TPS24701DGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |

## TUBE




*All dimensions are nominal

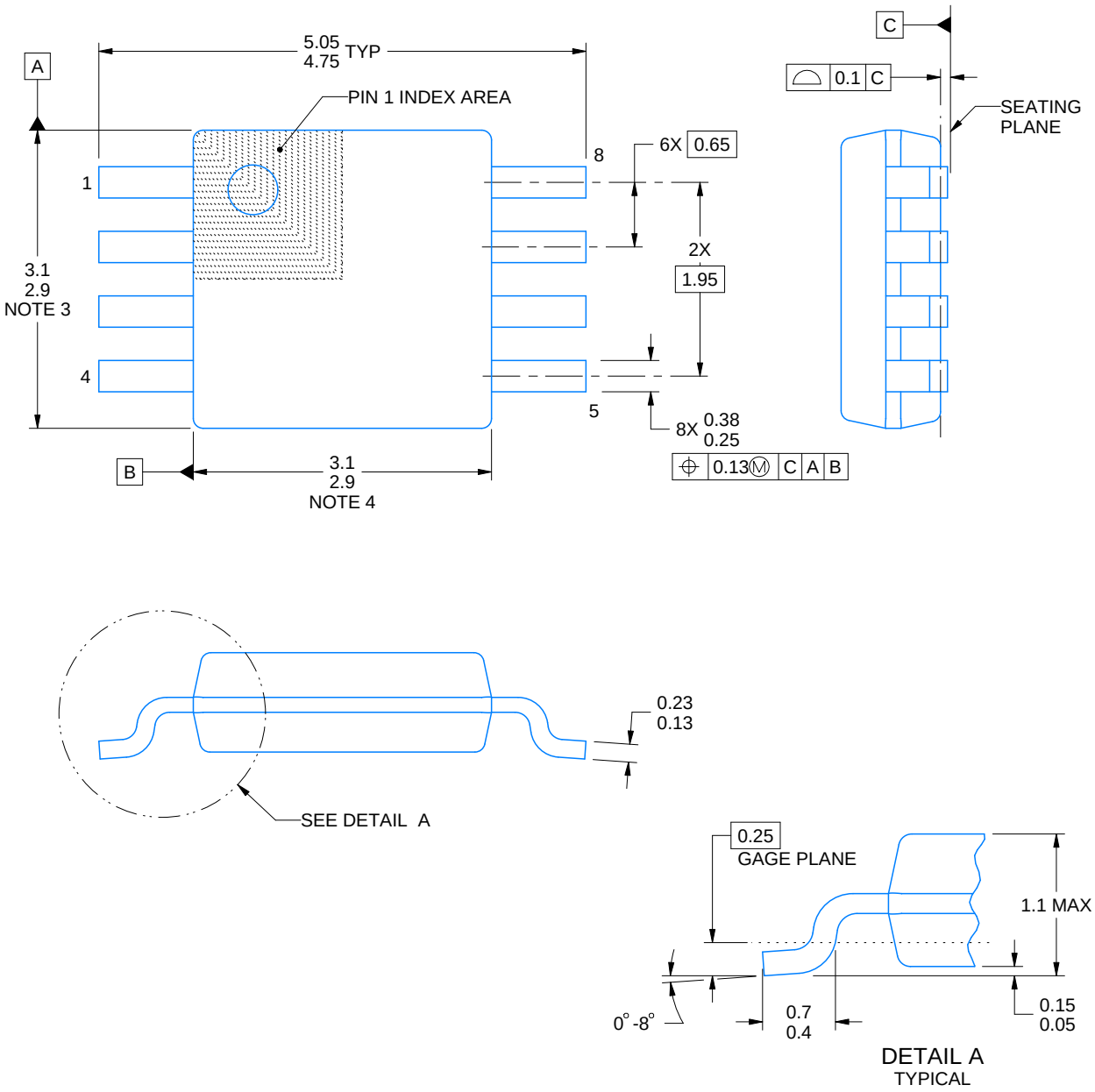
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS24700DGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS24700DGK | DGK | VSSOP | 8 | 80 | 274 | 6.2 | 2540 | 2.5 |
| TPS24700DGK.A | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS24700DGK.A | DGK | VSSOP | 8 | 80 | 274 | 6.2 | 2540 | 2.5 |
| TPS24701DGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS24701DGK | DGK | VSSOP | 8 | 80 | 274 | 6.2 | 2540 | 2.5 |
| TPS24701DGK.A | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS24701DGK.A | DGK | VSSOP | 8 | 80 | 274 | 6.2 | 2540 | 2.5 |

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

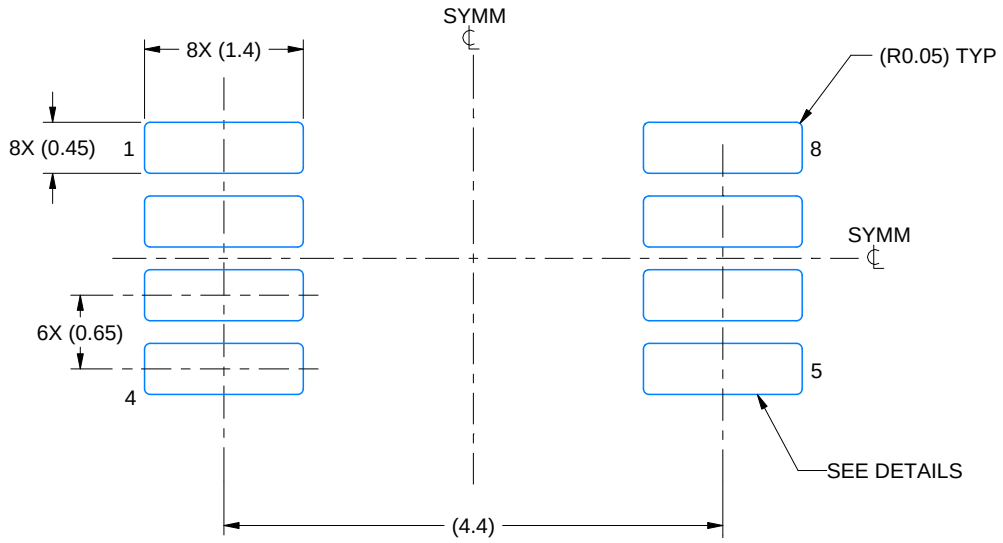
SMALL OUTLINE PACKAGE



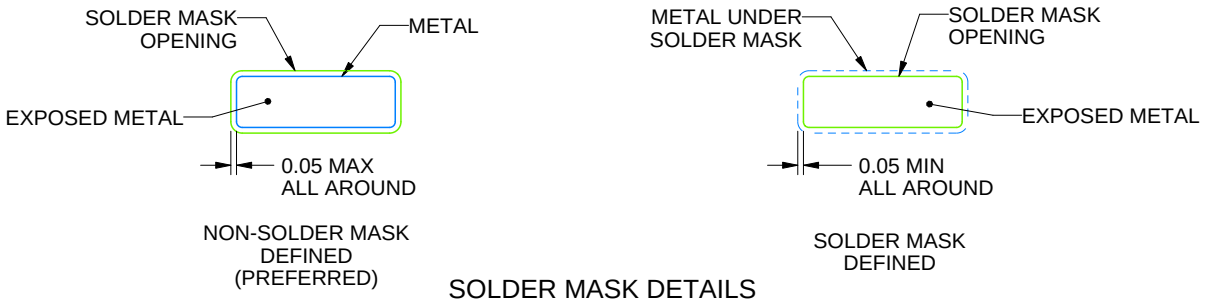

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

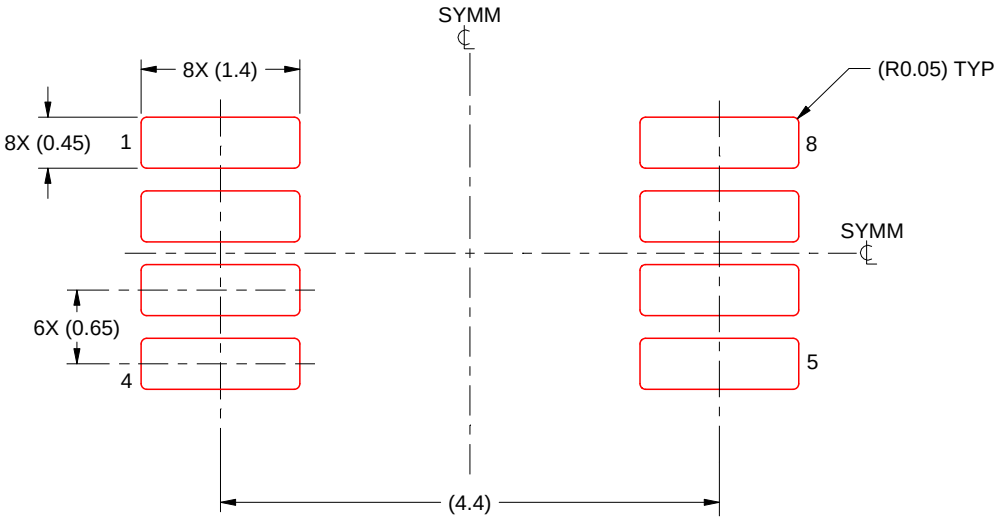



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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