

TPS22919-Q1 5.5 V, 1.5 A, 90-mΩ Self-Protected Load Switch

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified:
 - Device temperature grade 1: -40°C to 125°C ambient operating temperature range
- Input operating voltage range (V_{IN}): 1.6 V to 5.5 V
- Maximum continuous current (I_{MAX}): 1.5 A
- On-Resistance (R_{ON}):
 - 5-V V_{IN} : 89 mΩ (typical)
 - 3.6-V V_{IN} : 90 mΩ (typical)
 - 1.8-V V_{IN} : 105 mΩ (typical)
- Output short protection (I_{SC}): 3 A (typical)
- Low power consumption:
 - ON state (I_{Q}): 8 μA (typical)
 - OFF state (I_{SD}): 2 nA (typical)
- Smart ON pin pull down (R_{PD}):
 - $\text{ON} \geq V_{\text{IH}}$ (I_{ON}): 100 nA (maximum)
 - $\text{ON} \leq V_{\text{IL}}$ (R_{PD}): 530 kΩ (typical)
- Slow Turn ON timing to limit inrush current (t_{ON}):
 - 5.0 V Turn ON time (t_{ON}): 1.95 ms at 3.2 mV/μs
 - 3.6 V Turn ON time (t_{ON}): 1.75 ms at 2.7 mV/μs
 - 1.8 V Turn ON time (t_{ON}): 1.5 ms at 1.8 mV/μs
- Adjustable output discharge and fall time:
 - Internal QOD resistance = 24 Ω (typical)

2 Applications

- [Infotainment and cluster head unit](#)
- [Automotive cluster display](#)
- [ADAS Surround view system ECU](#)
- [Body control module and gateway](#)

3 Description

The TPS22919-Q1 device is a small, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.6 V to 5.5 V and can support a maximum continuous current of 1.5 A.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven High ($>V_{\text{IH}}$), the Smart Pull Down will be disconnected to prevent unnecessary power loss.

The TPS22919-Q1 load switch is also self-protected, meaning that it protects against short circuit events on the output of the device. It also has thermal shutdown protection to prevent any damage from overheating.

TPS22919-Q1 is available in a standard SC-70 package characterized for operation over a junction temperature range of -40°C to 125°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22919-Q1	SC-70 (6)	2.1 mm x 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application

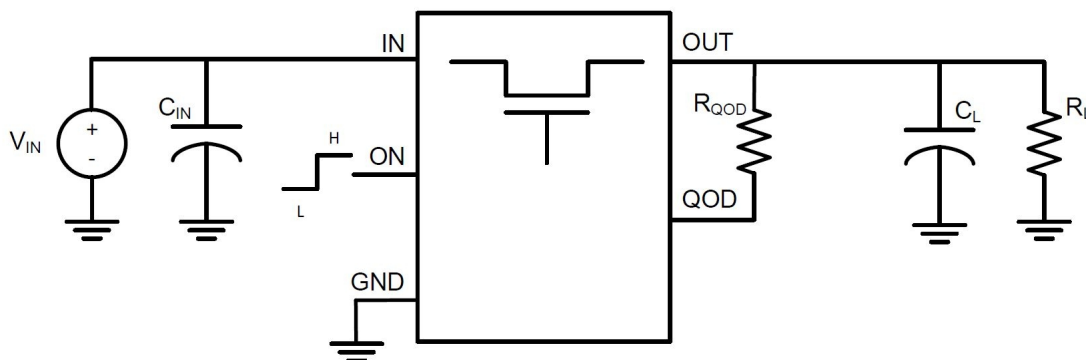


Table of Contents

1 Features	1	8.2 Functional Block Diagram	12
2 Applications	1	8.3 Feature Description	13
3 Description	1	8.4 Device Functional Modes	14
4 Revision History	2	9 Application and Implementation	15
5 Pin Configuration and Functions	3	9.1 Application Information	15
6 Specifications	4	9.2 Typical Application	15
6.1 Absolute Maximum Ratings	4	10 Power Supply Recommendations	17
6.2 ESD Ratings	4	11 Layout	18
6.3 Recommended Operating Conditions	4	11.1 Layout Guidelines	18
6.4 Thermal Information	4	11.2 Layout Example	18
6.5 Electrical Characteristics	4	11.3 Thermal Considerations	18
6.6 Switching Characteristics	5	12 Device and Documentation Support	19
6.7 Typical Characteristics	7	12.1 Trademarks	19
7 Parameter Measurement Information	11	12.2 Electrostatic Discharge Caution	19
7.1 Test Circuit and Timing Waveforms Diagrams	11	12.3 Glossary	19
8 Detailed Description	12	13 Mechanical, Packaging, and Orderable Information	19
8.1 Overview	12		

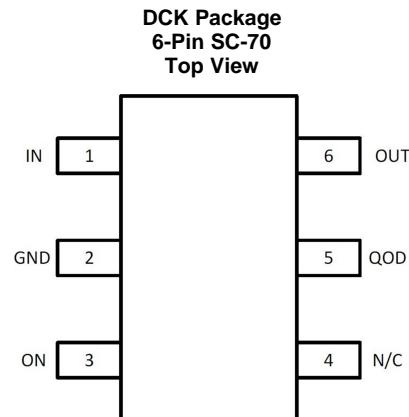
4 Revision History

Changes from Original (January 2020) to Revision A

Page

- Changed document status from *Advanced Information* to *Production Data* **1**

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input.
2	GND	—	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	NC	—	No connect pin, leave floating.
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. <ul style="list-style-type: none"> Placing an external resistor between VOUT and QOD Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) Disabling QOD by leaving pin floating See the Fall Time (t_{FALL}) and Quick Output Discharge (QOD) section for more information.
6	VOUT	O	Switch output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Maximum Input Voltage Range	-0.3	6	V
V _{OUT}	Maximum Output Voltage Range	-0.3	6	V
V _{ON}	Maximum ON Pin Voltage Range	-0.3	6	V
V _{QOD}	Maximum QOD Pin Voltage Range	-0.3	6	V
I _{MAX}	Maximum Continuous Current		1.5	A
I _{PLS}	Maximum Pulsed Current (2 ms, 2% Duty Cycle)		2.5	A
T _J	Junction temperature	Internally Limited		°C
T _{STG}	Storage temperature	-65	150	°C
T _{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Input Voltage Range	1.6		5.5	V
V _{OUT}	Output Voltage Range	0		5.5	V
V _{IH}	ON Pin High Voltage Range	1		5.5	V
V _{IL}	ON Pin Low Voltage Range	0		0.35	V
T _A	Ambient Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22919-Q1	UNIT
		DCK (SC-70)	
		PINS	
R _{θJA}	Junction-to-ambient thermal resistance	214.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	147.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	75.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	58.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	75.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Typical values at V_{IN} = 3.6V unless otherwise specified

PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
Input Supply (VIN)						

Electrical Characteristics (continued)

Typical values at $V_{IN} = 3.6V$ unless otherwise specified

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT	
$I_{Q, VIN}$	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, $V_{OUT} = \text{Open}$	25°C	8	15		μA	
			-40°C to 125°C			20	μA	
$I_{SD, VIN}$	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, $V_{OUT} = \text{GND}$	25°C	2	20		nA	
			-40°C to 125°C			800	nA	
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	$I_{OUT} = -200 \text{ mA}$	$V_{IN} = 5 \text{ V}$	25°C	89	125	m Ω	
				-40°C to 85°C			150	m Ω
				-40°C to 105°C			175	m Ω
				-40°C to 125°C			200	m Ω
			$V_{IN} = 3.6 \text{ V}$	25°C	90	150	m Ω	
				-40°C to 85°C			200	m Ω
				-40°C to 105°C			225	m Ω
				-40°C to 125°C			250	m Ω
			$V_{IN} = 1.8 \text{ V}$	25°C	105	300	m Ω	
				-40°C to 85°C			330	m Ω
				-40°C to 105°C			340	m Ω
				-40°C to 125°C			350	m Ω
Output Short Protection (ISC)								
I_{SC}	Short Circuit Current Limit	$V_{OUT} \leq V_{IN} - 1.5 \text{ V}$	-40°C to 125°C	3			A	
		$V_{OUT} \leq V_{SC}$	-40°C to 125°C	30	500	900	mA	
V_{SC}	Output Short Detection Threshold	$V_{IN} - V_{OUT}$	-40°C to 105°C	0.3	0.36	0.46	V	
			-40°C to 125°C	0.22	0.36	0.57	V	
t_{SC}	Output Short Reponse Time	$V_{IN} = 1.6V$ to $5.5V$, $10m\Omega$ short applied	-40°C to 125°C	2			μs	
T_{SD}	Thermal Shutdown		Rising	180			°C	
			Falling	145			°C	
Enable Pin (ON)								
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$	-40°C to 125°C			100	nA	
$R_{PD, ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$	-40°C to 125°C			530	k Ω	
Quick-output Discharge (QOD)								
$R_{PD, QOD}$	QOD Pin Internal Discharge Resistance	$V_{ON} \leq V_{IL}$	-40°C to 125°C			24	Ω	

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of $C_L = 0.1 \mu F$, $R_L = 100 \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	$V_{IN} = 5.0 \text{ V}$	1950		μs
		$V_{IN} = 3.6 \text{ V}$	1750		μs
		$V_{IN} = 1.8 \text{ V}$	1500		μs
t_R	Output Rise Time	$V_{IN} = 5.0 \text{ V}$	1280		μs
		$V_{IN} = 3.6 \text{ V}$	1100		μs
		$V_{IN} = 1.8 \text{ V}$	750		μs
SR_{ON}	Turn ON Slew Rate	$V_{IN} = 5.0 \text{ V}$	3.2		mV/ μs
		$V_{IN} = 3.6 \text{ V}$	2.7		mV/ μs
		$V_{IN} = 1.8 \text{ V}$	1.8		mV/ μs
t_{OFF}	Turn OFF Time	$V_{IN} = 1.8 \text{ V}$ to $5.0V$	$R_L = 100\Omega$, $C_L = 0.1\mu F$	6	μs

Switching Characteristics (continued)

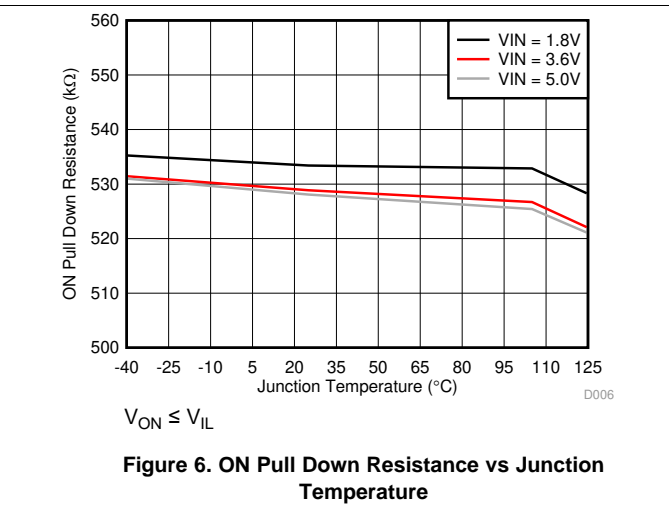
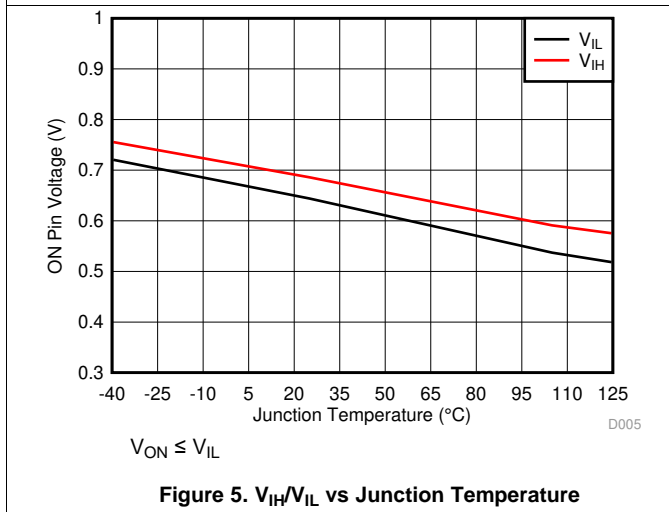
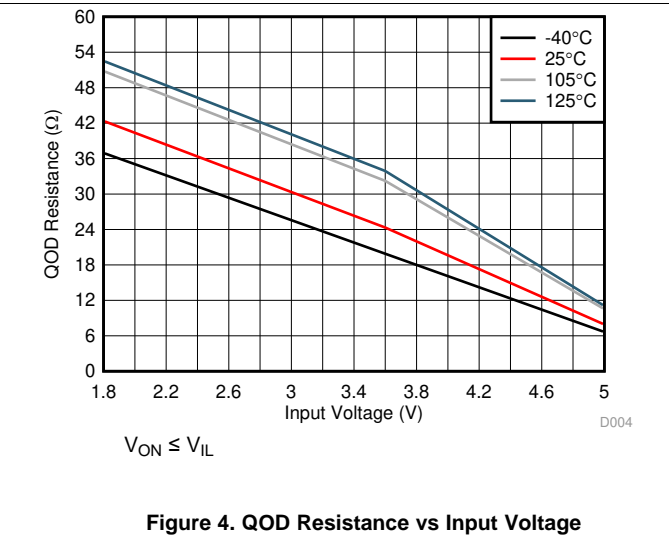
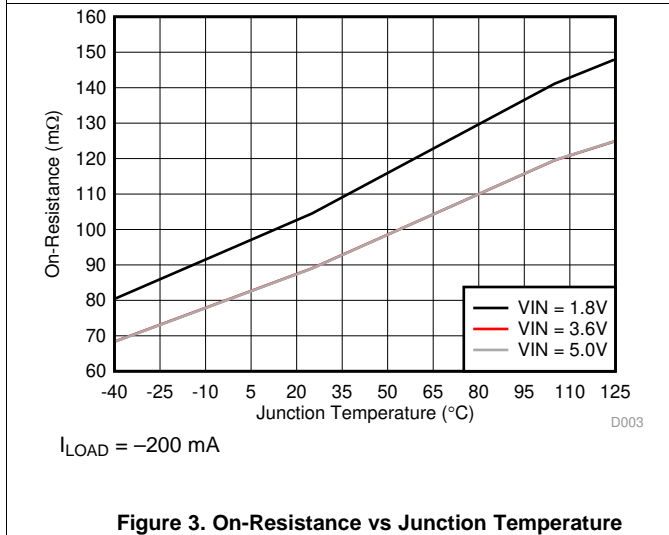
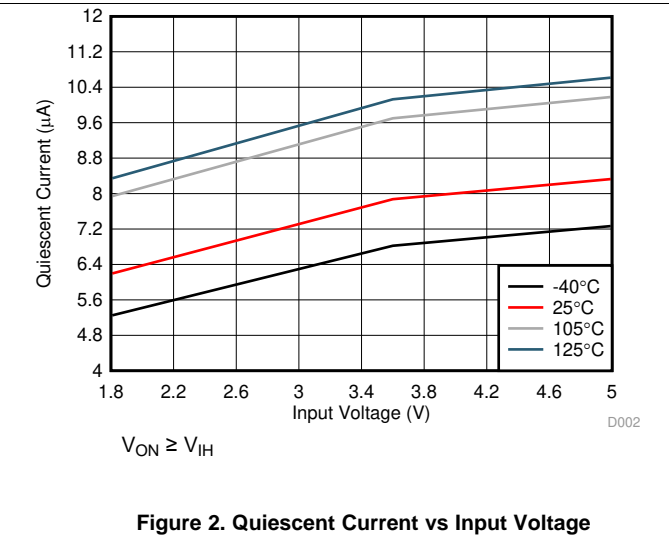
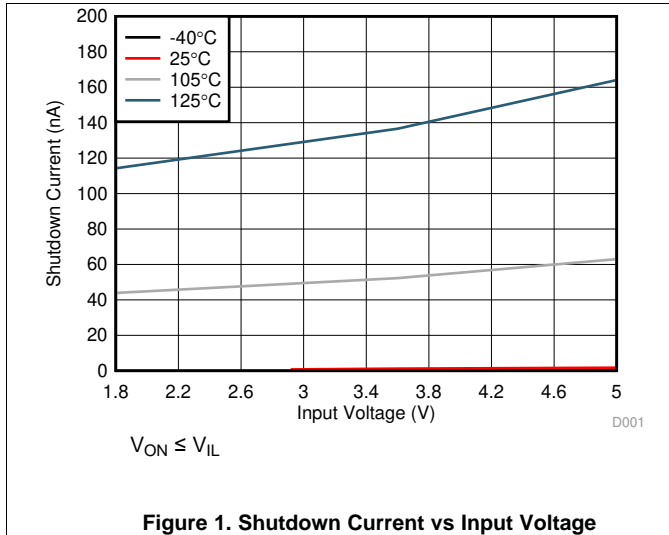
Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of $C_L = 0.1 \mu\text{F}$, $R_L = 100 \Omega$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{FALL}	Output Fall Time (1)	$R_L = 100\Omega$	$C_L = 0.1\mu\text{F}$, $R_{\text{QOD}} = \text{Short}$		10		μs
		$R_L = \text{Open}$ (2)	$C_L = 10\mu\text{F}$, $R_{\text{QOD}} = \text{Short}$		0.4		ms
			$C_L = 10\mu\text{F}$, $R_{\text{QOD}} = 100 \Omega$		3.5		ms
			$C_L = 100\mu\text{F}$, $R_{\text{QOD}} = \text{Short}$		4		ms

(1) Output may not discharge completely if QOD is not connected to VOUT

(2) See the *Timing Application* section for information on how R_L and C_L affect Fall Time.

6.7 Typical Characteristics



Typical Characteristics (continued)

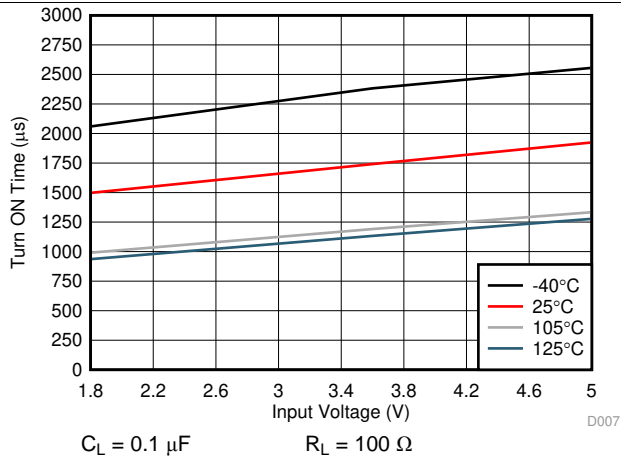


Figure 7. Turn ON Time vs Input Voltage

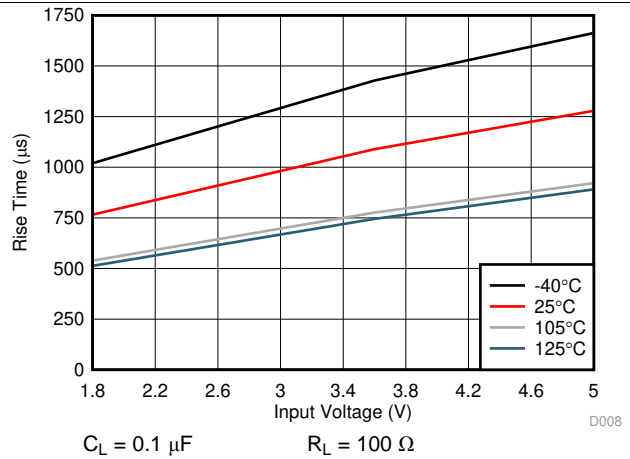


Figure 8. Rise Time vs Input Voltage

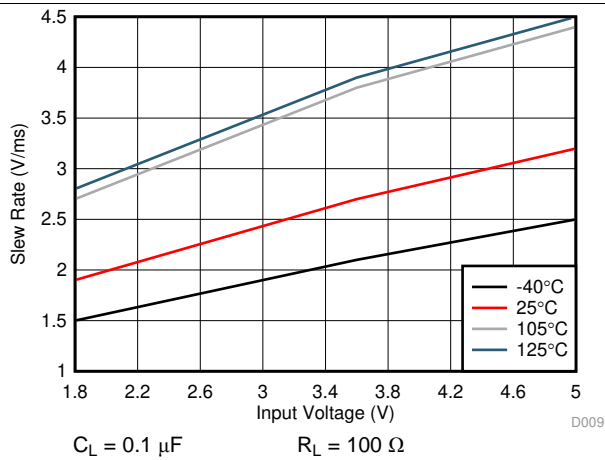


Figure 9. Output Slew Rate vs Input Voltage

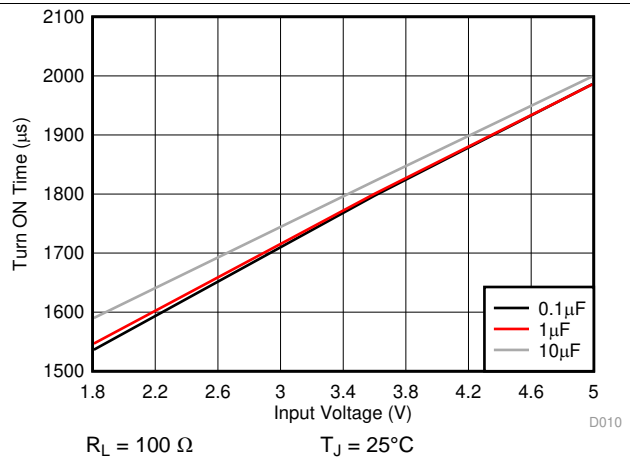


Figure 10. Turn ON Time vs Input Voltage Across Load Capacitance

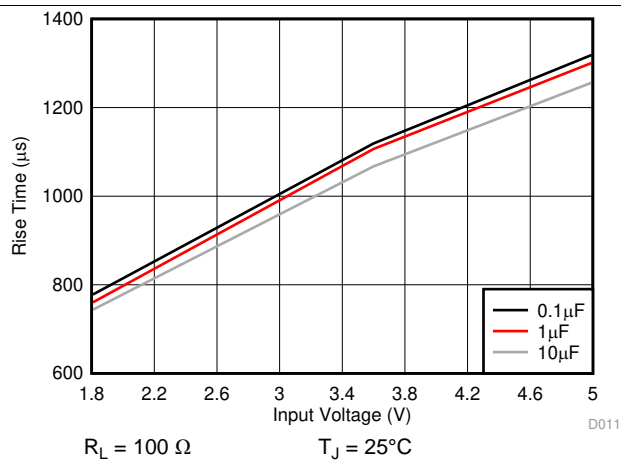


Figure 11. Rise Time vs Input Voltage Across Load Capacitance

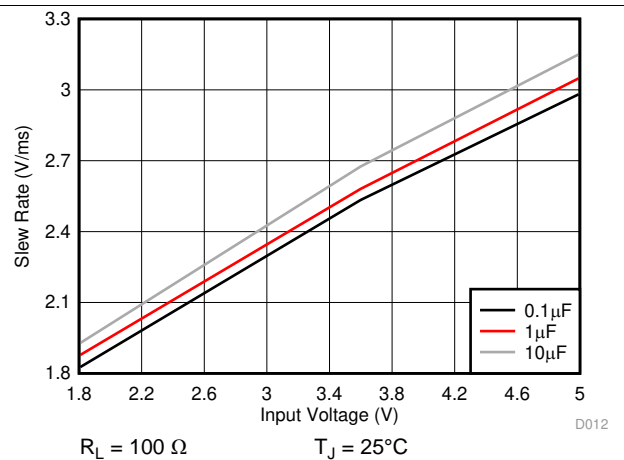


Figure 12. Slew Rate vs Input Voltage Across Load Capacitance

Typical Characteristics (continued)

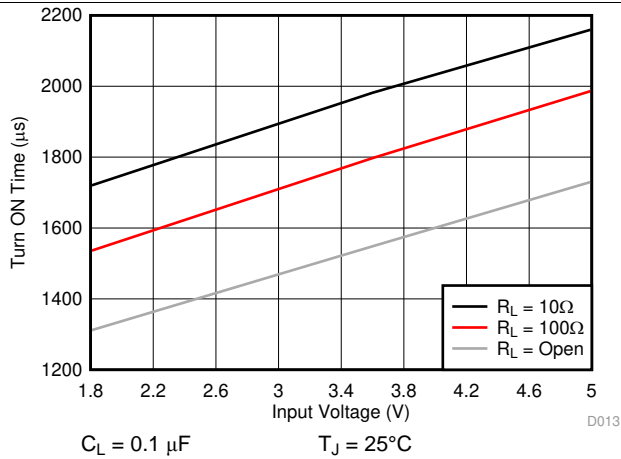


Figure 13. Turn ON Time vs Input Voltage Across Load Resistance

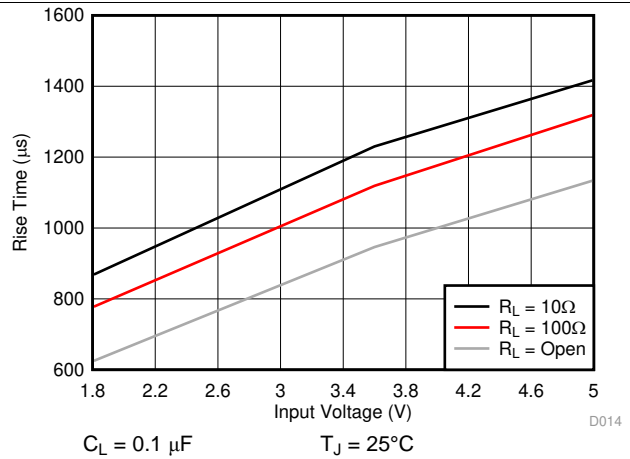


Figure 14. Rise Time vs Input Voltage Across Load Resistance

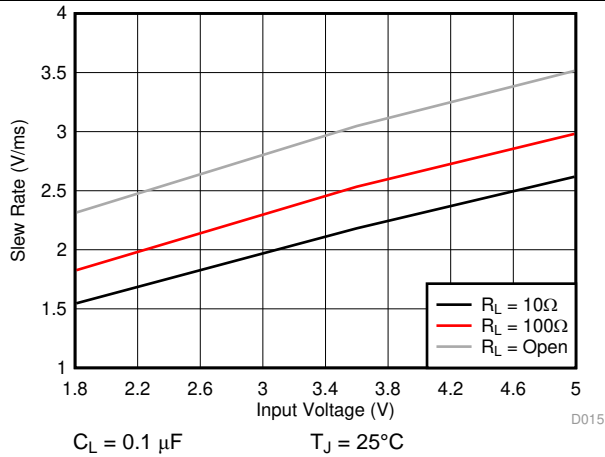


Figure 15. Output Slew Rate vs Input Voltage Across Load Resistance

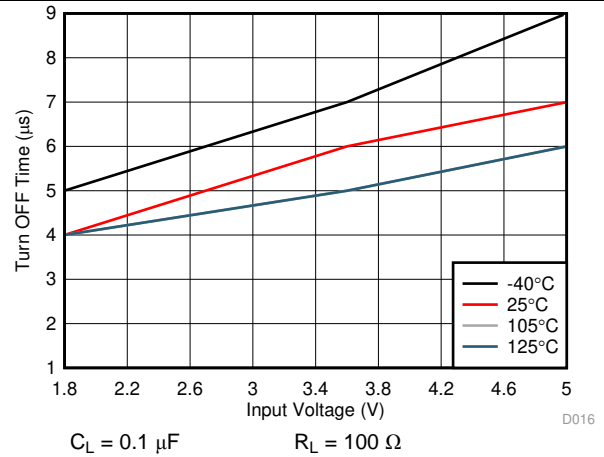


Figure 16. Turn OFF Time vs Input Voltage

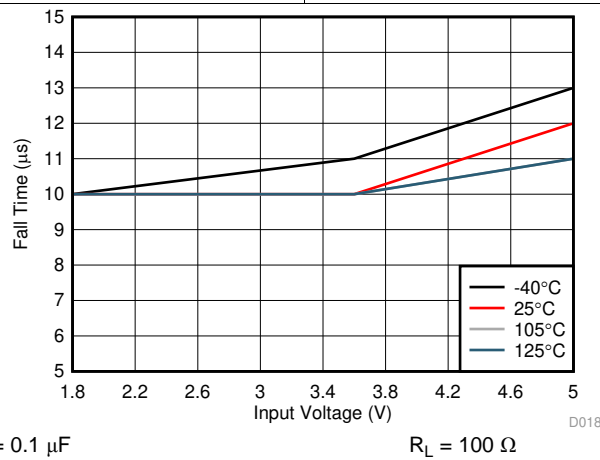
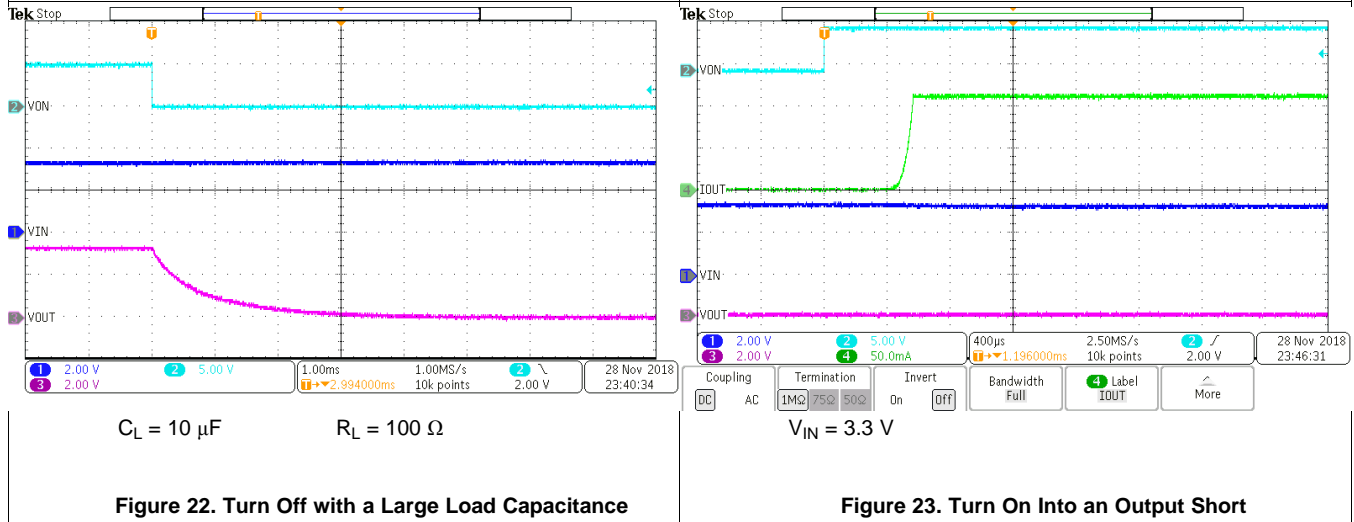
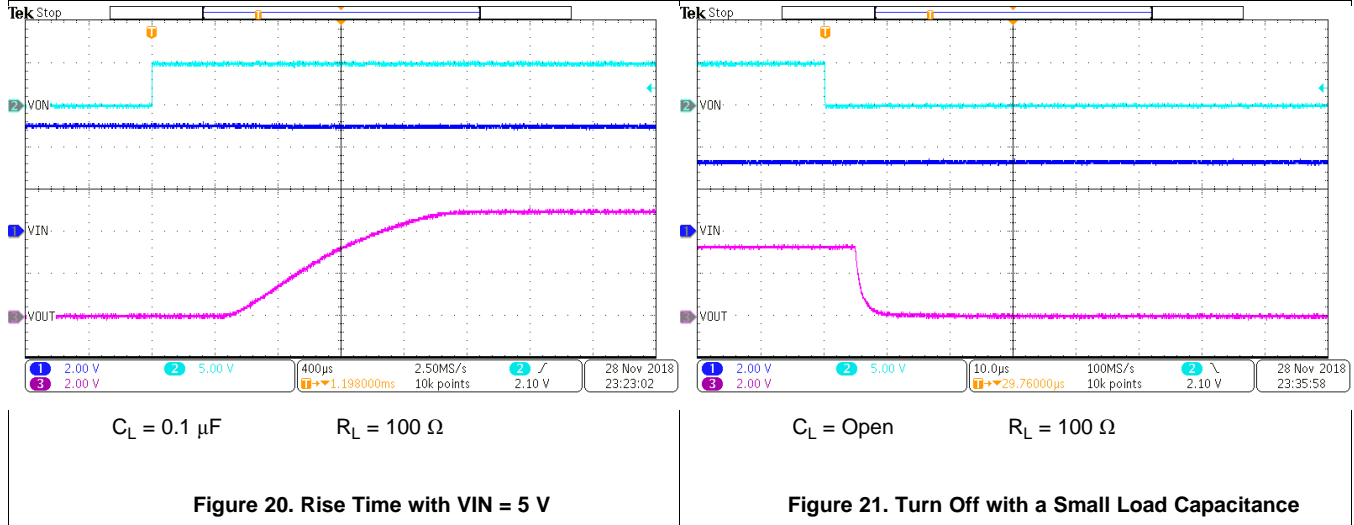
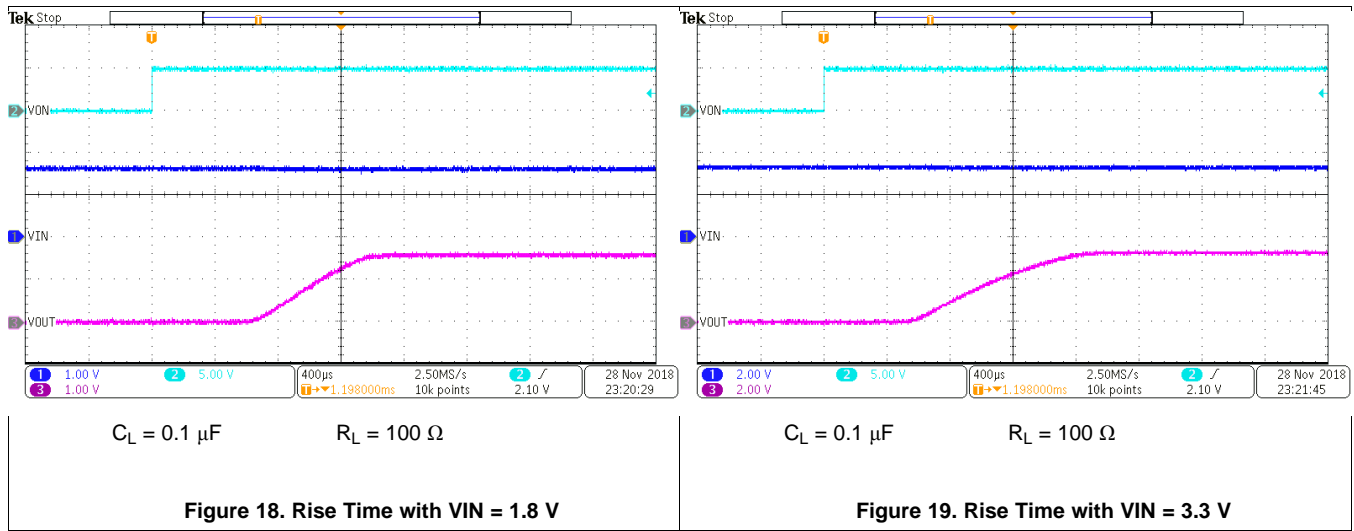
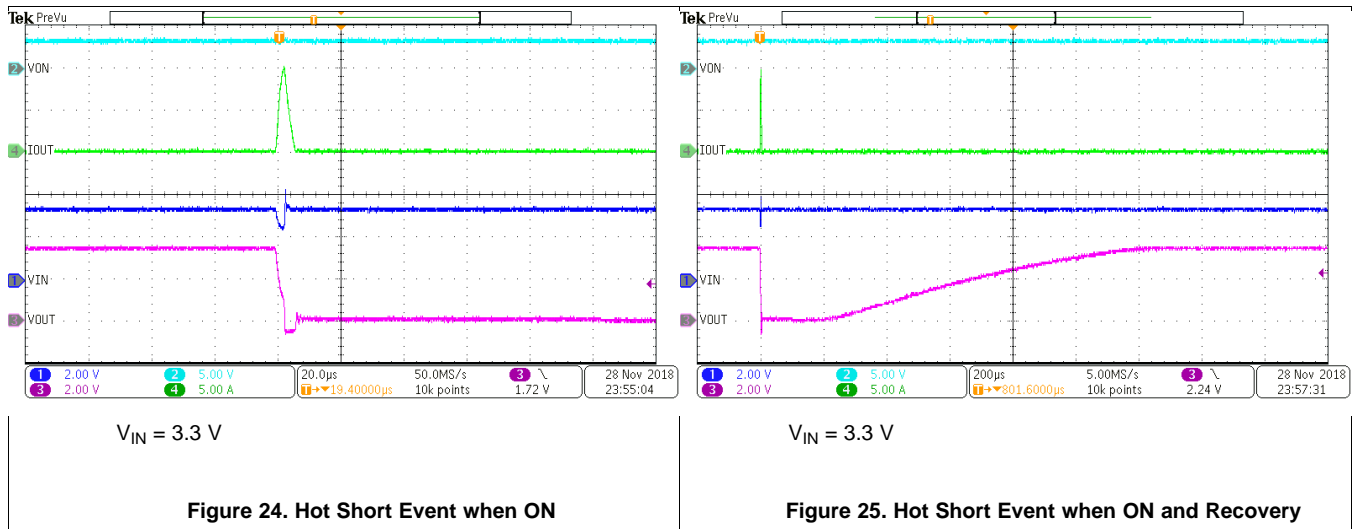


Figure 17. Fall Time vs Input Voltage

Typical Characteristics (continued)

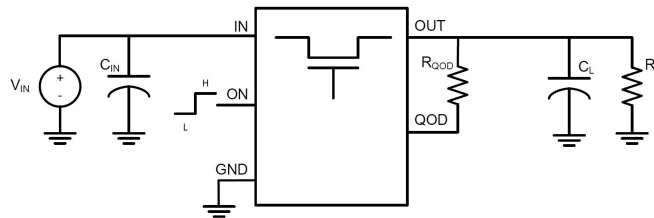


Typical Characteristics (continued)



7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams



- (1) Rise and fall times of the control signal are 100 ns
- (2) Turn-off times and fall times are dependent on the time constant at the load. For the TPS22919-Q1 devices, the internal pull-down resistance QOD is enabled when the switch is disabled. The time constant is $(R_{QOD} + R_{PD,QOD} \parallel R_L) \times C_L$.

Figure 26. Test Circuit

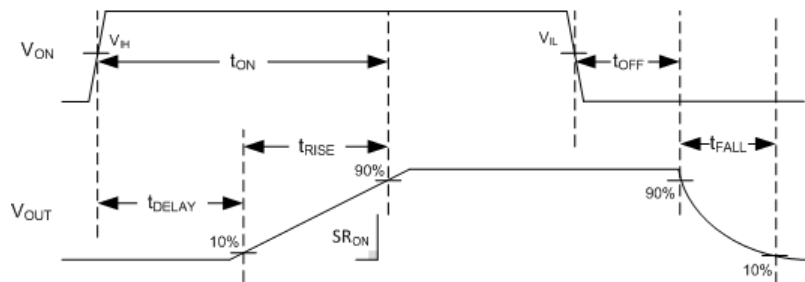


Figure 27. Timing Waveforms

8 Detailed Description

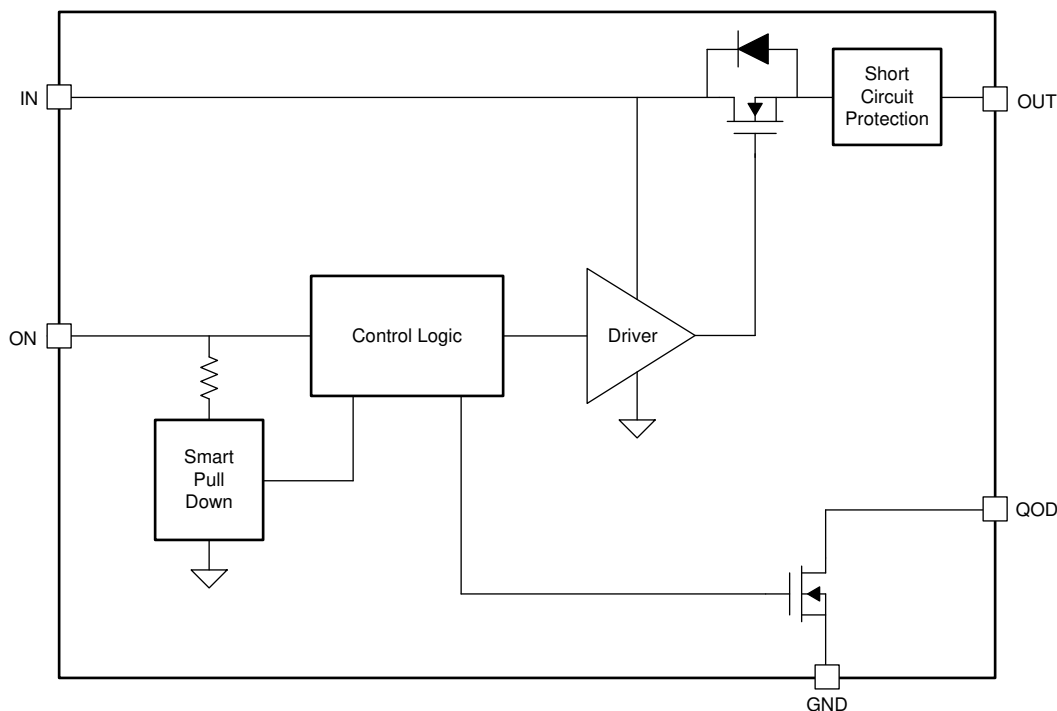
8.1 Overview

The TPS22919-Q1 device is a 5.5-V, 1.5-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The TPS22919-Q1 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22919-Q1 load switch is also self-protected, meaning that it will protect itself from short circuit events on the output of the device. It also has thermal shutdown to prevent any damage from overheating.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pull Down is used to keep the ON pin from floating until the system sequencing is complete. Once the ON pin is deliberately driven high ($\geq V_{IH}$), the Smart Pull Down is disconnected to prevent unnecessary power loss. See [Table 1](#) when the ON Pin Smart Pull Down is active.

Table 1. Smart-ON Pull Down

VON	Pull Down
$\leq V_{IL}$	Connected
$\geq V_{IH}$	Disconnected

8.3.2 Output Short Circuit Protection (I_{SC})

The device will limit current to the output in case of output shorts. When a short occurs, the large VIN to VOUT voltage drop causes the switch to limit the output current (I_{SC}) within (t_{SC}). When the output is below the hard short threshold (V_{SC}), a lower limit is used to minimize the power dissipation while the fault is present. The device will continue to limit the current until it reaches its thermal shutdown temperature. At this time, the device will turn off until its temperature has lowered by the thermal hysteresis (35°C typical) before turning on again.

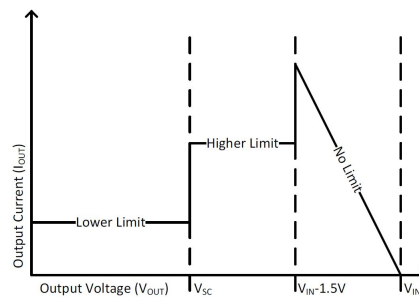


Figure 28. Output Short Circuit Current Limit

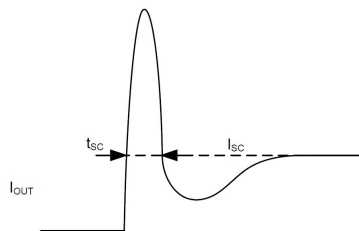


Figure 29. Output Short Circuit Response

8.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22919-Q1 device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance QOD ($R_{PD,QOD}$).
- QOD pin connected to VOUT pin using an external resistor R_{QOD} . After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, [Equation 1](#) can be used:

$$R_{DIS} = R_{PD,QOD} + R_{QOD}$$

where:

- R_{DIS} is the total output discharge resistance (Ω)

- $R_{PD,QOD}$ is the internal pulldown resistance (Ω)
- R_{QOD} is the external resistance placed between the VOUT and QOD pins (Ω) (1)
- QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality, and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_L). To calculate the approximate fall time of V_{OUT} use [Equation 2](#).

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L$$

where:

- t_{FALL} is the output fall time from 90% to 10% (μs)
- R_{DIS} is the total QOD + R_{QOD} Resistance (Ω)
- R_L is the output load resistance (Ω)
- C_L is the output load capacitance (μF) (2)

8.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN} . Past a certain V_{IN} level, the strength of the R_{PD} will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the [Setting Fall Time for Shutdown Power Sequencing](#) section.

8.4 Device Functional Modes

[Table 2](#) describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919-Q1 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD, QOD} + R_{QOD}$)
L	QOD pin tied to VOUT directly	GND ($R_{PD, QOD}$)
L	QOD pin left open	Floating
H	N/A	VIN

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22919-Q1 devices can be used to power downstream modules.

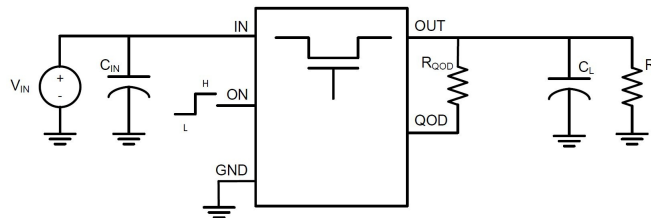


Figure 30. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in [Table 3](#) as the design parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	3.6 V
Load current resistance (R_L)	1 k Ω
Load capacitance (C_L)	47 μ F
Minimum fall time (t_F)	40 ms
Maximum inrush current (I_{RUSH})	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use Equation 3 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$(\text{Slew Rate}) = I_{\text{RUSH}} \div C_L$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_L = capacitance on VOUT (μF)
- Slew Rate = Output Slew Rate during turn on ($\text{mV}/\mu\text{s}$) (3)

Based on Equation 3, the required slew rate to limit the inrush current to 150 mA is $3.2 \text{ mV}/\mu\text{s}$. The TPS22919-Q1 has a slew rate of $2.3 \text{ mV}/\mu\text{s}$, so the inrush current will be below 150 mA.

9.2.2.2 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22919-Q1 device, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using Equation 2:

$$t_{\text{FALL}} = 2.2 \times (R_{\text{DIS}} \parallel R_L) \times C_L \tag{4}$$

$$R_{\text{DIS}} = 630 \Omega \tag{5}$$

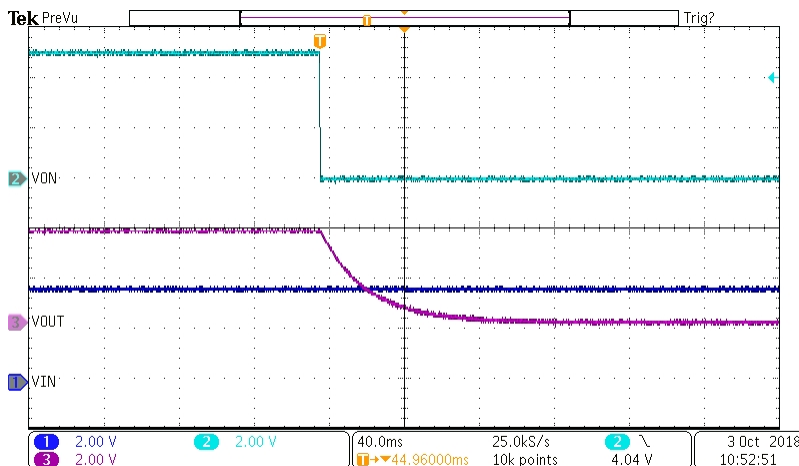
Equation 1 can then be used to calculate the R_{QOD} resistance needed to achieve a particular discharge value:

$$R_{\text{DIS}} = \text{QOD} + R_{\text{QOD}} \tag{6}$$

$$R_{\text{QOD}} = 600 \Omega \tag{7}$$

To ensure a fall time greater than, choose an R_{QOD} value greater than 600Ω .

9.2.2.3 Application Curves



A.

$$C_L = 47 \mu\text{F}$$

Figure 31. Fall Time ($R_{\text{QOD}} = 1 \text{ k}\Omega$)

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 μ F is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

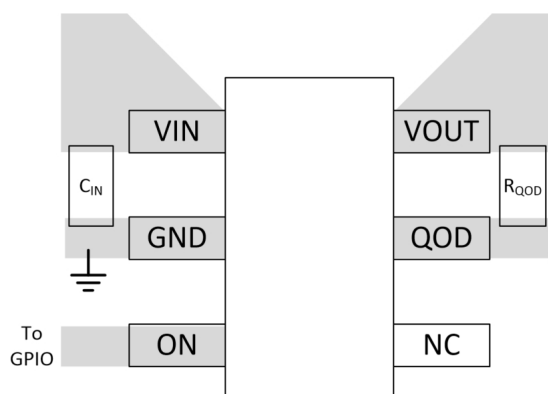


Figure 32. Recommended Board Layout

11.3 Thermal Considerations

It is recommended to keep the maximum IC junction temperature restricted to 150°C under normal operating conditions to prevent the TPS22919-Q1 from entering thermal shutdown. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use [Equation 8](#):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (150°C for the TPS22919-Q1 device)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the Thermal Parameters table. This parameter is highly dependent upon board layout.

(8)

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22919QDCKRQ1	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1H2
TPS22919QDCKRQ1.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1H2

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS22919-Q1 :

- Catalog : [TPS22919](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

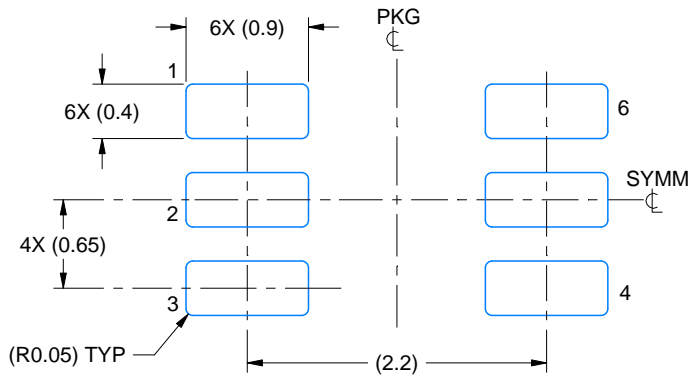
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22919QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

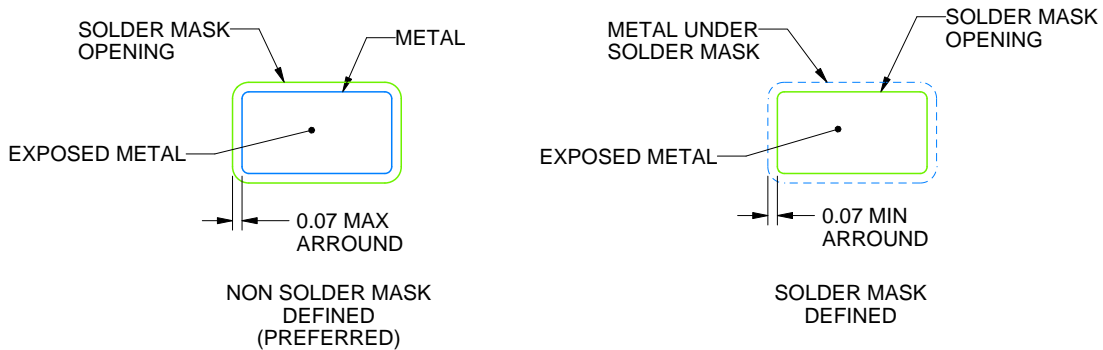


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22919QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

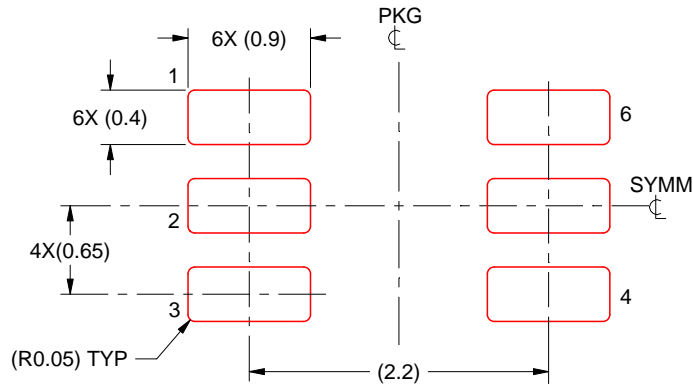


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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