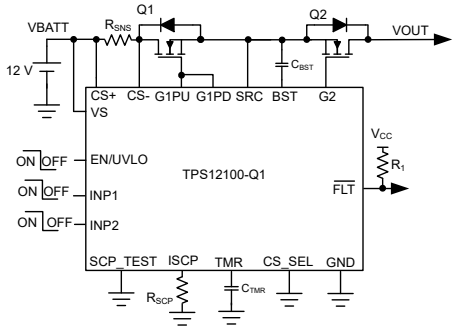
TPS1210-Q1 45V, Automotive Low I_Q, Back-to-Back MOSFET Smart High Side Driver With Short-Circuit Protection and Diagnostics

1 Features

- AEC-Q100 automotive qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 3.5V to 40V input range (45V absolute maximum)
- Reverse input protection down to –40V
- Integrated 11V charge pump
- Low quiescent current, 35µA in operation
- Low 1.5µA shutdown current (EN/UVLO = Low)
- Two strong gate drivers (2A src/sink) for back-to-back MOSFET driving with separate control inputs (INP1, INP2)
  - Variants with active high (TPS12100-Q1) and active low (TPS12101-Q1) inputs
- Adjustable short-circuit protection (ISCP) using external Rsense or MOSFET VDS sensing with adjustable delay (TMR)
- High or low-side current sense configuration (CS_SEL)
- Fault indication ($\overline{FLT}$) during short-circuit fault, charge pump under voltage, input undervoltage, and short-circuit comparator diagnosis (SCP_TEST)
- Adjustable input undervoltage lockout (UVLO)

2 Applications

- Automotive 12V BMS
- DC/DC converter



BMS Breaker With High Side Current Sense

3 Description

The TPS1210x-Q1 family is a 45V, low I_Q, smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5V–40V, the device is designed for 12V system designs. The device can withstand and protect the loads from negative supply voltages down to –40V.

The device has two strong (2A) GATE drivers with separate control inputs (INP1, INP2) to drive back-to-back MOSFETs in common source configuration. TPS12100-Q1 has active high control inputs and TPS12101-Q1 has active low control inputs.

The device provides adjustable short-circuit protection. Auto-retry and latch-off fault behavior can be configured. Current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. The device also features diagnosis of the internal short circuit comparator using external control on SCP_TEST input.

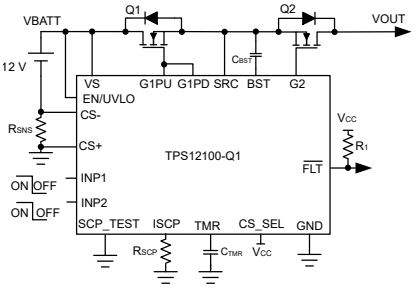
Low Quiescent current 35µA (typical) in operation enables always ON system designs. Quiescent current reduces to 1.5µA (typical) with EN/UVLO low.

The TPS1210x-Q1 is available in a 19-pin VSSOP package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS12100-Q1, TPS12101-Q1(3)	DGX (VSSOP, 19)	5.1mm × 3.0mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product preview.



BMS Breaker With Low Side Current Sense

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison

	TPS12100-Q1	TPS12101-Q1
Input controls (INP1, INP2)	Active High logic	Active Low logic

5 Pin Configuration and Functions

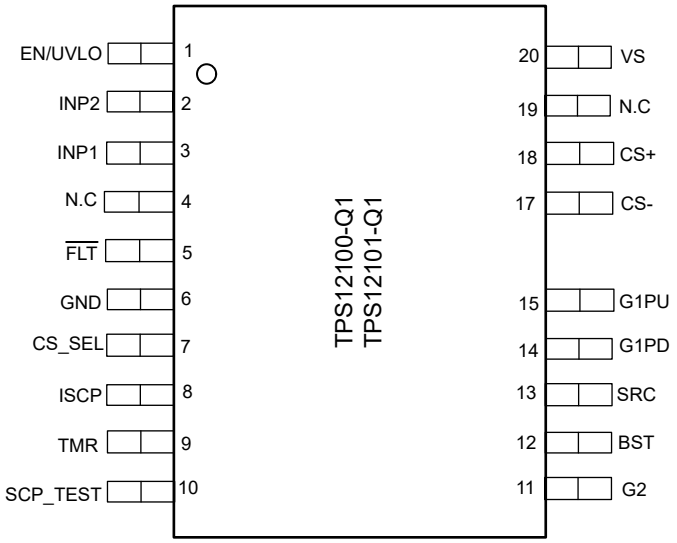


Figure 5-1. DGX Package, 19-Pin VSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN/UVLO	1	I	EN/UVLO Input. A voltage on this pin above 1.21V enables normal operation. Forcing this pin below 0.3V shuts down the device reducing quiescent current to approximately 1.6µA (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pull down of 100nA pulls EN/UVLO low and keeps the device in shutdown state.
INP2	2	I	Input Signal for external charge FET control. In TPS12100-Q1 drive INP2 high to drive G2 high. Drive INP2 low to pull G2 low. INP2 has an internal weak 100nA pulldown to GND to keep G2 pulled low to SRC when INP2 is left floating. In TPS12101-Q1 drive INP2 low to drive G2 high. Drive INP2 high to pull G2 low. INP2 has an internal weak pulldown of 100nA to GND to keep G2 high when INP2 is left floating.
INP1	3	I	Input Signal for external charge FET control. In TPS12100-Q1 drive INP1 high to drive G1PU high. Drive INP1 low to pull G1PD low. INP1 has an internal weak pulldown of 100nA to GND to keep G1PD pulled to SRC when INP1 is left floating. In TPS12101-Q1, drive INP1 low to drive G1PU high. Drive INP1 high to pull G1PD low. INP1 has an internal weak pull down of 100nA to GND to keep G1PU high when INP1 is left floating.
N.C	4	—	No connect.
$\overline{FLT}$	5	O	Open Drain Fault Output. This pin asserts low during short-circuit fault, charge pump UVLO, input UVLO and during SCP comparator diagnosis. If $\overline{FLT}$ feature is not desired then connect it to GND.

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Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	6	G	Connect GND to system ground.
CS_SEL	7	I	Current sense select input. Connect this pin to ground to activate high side current sense. Drive this pin to >2V to activate low side current sensing. CS_SEL has an internal weak pull down of 100nA to GND.
ISCP	8	I	Short-circuit detection setting. A resistor across ISCP to GND sets the short circuit current comparator threshold. If short-circuit protection feature is not desired then connect CS+, CS– , VS pins together and connect ISCP, TMR pins to GND.
TMR	9	I	Fault Timer Input. A capacitor across TMR pin to GND sets the delay time for short-circuit fault turn-off. Leave this pin open for fastest response setting. If short-circuit protection feature is not desired then connect CS+, CS–, VS pins together and connect ISCP, TMR pins to GND.
SCP_TEST	10	I	Internal short-circuit comparator (SCP) diagnosis input. When SCP_TEST is driven low to high with INP1 pulled high, the internal SCP comparator operation is checked. $\overline{FLT}$ goes low and G1PD gets pulled to SRC if SCP comparator is functional. Connect SCP_TEST pin to GND if this feature is not desired. SCP_TEST has an internal weak pulldown of 100nA to GND.
G2	11	O	Charging FET gate drive output. This pin has 1.69A peak source and 2A sink capacity. Leave the G2 pin floating if the G2 drive functionality is unused.
BST	12	O	High Side Bootstrapped Supply. An external capacitor with a minimum value of > $Q_{g(tot)}$ of the external FET must be connected between this pin and SRC.
SRC	13	O	Source connection of the external FET.
G1PD	14	O	High Current Gate Driver Pull-Down. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
G1PU	15	O	High Current Gate Driver Pull-Up. This pin pulls up to BST. Connect this pin to G1PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on.
CS-	17	I	Current sense negative input.
CS+	18	I	Current sense positive input.
N.C	19	—	No connect.
VS	20	P	Supply pin of the controller.

(1) I = input, O = output, I/O = input and output, P = power, G = ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	VS, CS+, CS– to GND	–40	45	V
	SRC to GND	–40	45	
	G1PU, G1PD, G2, BST to SRC	–0.3	19	
	ISCP, TMR, SCP_TEST to GND	–0.3	5.5	
	EN/UVLO, INP1, INP2, CS_SEL, $V_{(VS)}$ > 0 V	–1	45	
	EN/UVLO, INP1, INP2, CS_SEL, $V_{(VS)}$ ≤ 0 V	$V_{(VS)}$	(40 + $V_{(VS)}$)	
	CS+ to CS–	–1	45	V
	$\overline{FLT}$ to GND	–1	20	V
Sink current	$I_{(\overline{FLT})}$		10	mA
	$I_{(CS+)}$, $I_{(CS–)}$, 1msec	–100	100	mA
Output Pins	G1PU, G1PD, G2, BST to GND	–40	60	V
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, VS, SCP_TEST, G2)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	VS to GND	3.5		40	V
	Minimum voltage on VS pin for Short Circuit Protection	4			
	EN/UVLO, INP1, INP2 to GND	0		40	
Output Pins	$\overline{FLT}$ to GND	0		15	V
External Capacitor	VS, SRC to GND	22			nF
	BST to SRC	0.1			µF
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

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6.4 Thermal Information

THERMAL METRIC(1)		TPS1210-Q1 DGX 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40 °C to +125°C. $V_{(VS)}$ = 12 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VS	Operating input voltage		3.5		40	V
$V_{(S_PORR)}$	Input supply POR threshold, rising		1.85	2.55	3.3	V
$V_{(S_PORF)}$	Input supply POR threshold, falling		1.71	2.33	3.05	V
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		35	45	µA
	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V, –40°C ≤ T_J ≤ +85°C			44	µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		0.86	3.3	µA
$I_{(REV)}$	$I_{(VS)}$ leakage current during Reverse Polarity	$V_{(VS)}$ = – 40 V	11	13	23	µA
ENABLE, UNDERVOLTAGE LOCKOUT (EN/UVLO), SHORT CIRCUIT COMPARATOR TEST (SCP_TEST) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.176	1.23	1.287	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.09	1.138	1.184	V
$V_{(ENR)}$	Enable threshold voltage for low Iq shutdown, rising				1	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3			V
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)}$ = 12 V		170	310	nA
$V_{(SCP_TEST_H)}$	SCP test mode rising threshold				2	V
$V_{(SCP_TEST_L)}$	SCP test mode falling threshold		0.8			V
$I_{(SCP_TEST)}$	SCP_TEST input leakage current			90	700	nA
CHARGE PUMP (BST–SRC)						
$I_{(BST)}$	Charge Pump Supply current	$V_{(BST-SRC)}$ = 10 V, $V_{(EN/UVLO)}$ = 2 V	190	345	466	µA
$V_{(BST_UVLOR)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising	$V_{(EN/UVLO)}$ = 2 V	8.1	9	9.9	V
$V_{(BST_UVLOF)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, falling	$V_{(EN/UVLO)}$ = 2 V	7.31	8.2	8.9	V
$V_{(BST–SRC_ON)}$	Charge Pump Turn ON voltage	$V_{(EN/UVLO)}$ = 2 V	9.3	10.3	11.4	V
$V_{(BST–SRC_OFF)}$	Charge Pump Turn OFF voltage	$V_{(EN/UVLO)}$ = 2 V	10.4	11.6	12.8	V
$V_{(BST–SRC)}$	Charge Pump Voltage at $V_{(VS)}$ = 3.5 V	$V_{(EN/UVLO)}$ = 2 V	9.1	10.5	11.6	V
$I_{(SRC)}$	SRC pin leakage current	$V_{(EN/UVLO)}$ = 2 V, $V_{(INP1)}$ = $V_{(INP2)}$ = 0 V		0.4		µA
GATE DRIVER OUTPUTS (G1PU, G1PD, G2)						
$V_{(G1_GOOD)}$	G1 Good rising threshold		5.5	7	8.3	V
$I_{(G1PU)}$	Peak Source Current			1.69		A
$I_{(G1PD)}$	Peak Sink Current			2		A

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6.5 Electrical Characteristics (continued)

T_J = –40 °C to +125°C. $V_{(VS)}$ = 12 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(G2)}$	G2 Peak Source Current			1.69		A
$I_{(G2)}$	G2 Peak Sink Current			2		A
SHORT CIRCUIT PROTECTION (ISCP)						
I_{SCP}	SCP Input Bias current		8.4	10	12.33	µA
$V_{(SCP)}$	SCP threshold	$R_{(ISCP)}$ = 140.5 kΩ		300		mV
		$R_{(ISCP)}$ = 28 kΩ	60	75	90.5	mV
		$R_{(ISCP)}$ = 10.5 kΩ	32	40	48.9	mV
		$R_{(ISCP)}$ = 500 Ω	15	20	25	mV
		$R_{(ISCP)}$ = Open			757	mV
$V_{(SCP)}$	SCP threshold with external bias voltage on ISCP pin	$V_{(ISCP)}$ = 1.405 V	283	300	316	mV
		$V_{(ISCP)}$ = 280 mV	68.7	75	82.5	mV
		$V_{(ISCP)}$ = 105 mV	34.5	40	46.5	mV
DELAY TIMER (TMR)						
$I_{(TMR_SRC_CB)}$	TMR source current		67	87	104	µA
$I_{(TMR_SRC_FLT)}$	TMR source current		1.4	2.73	3.8	µA
$I_{(TMR_SNK)}$	TMR sink current		2.17	2.8	3.4	µA
$V_{(TMR_SC)}$			0.93	1.1	1.2	V
$V_{(TMR_LOW)}$			0.15	0.21	0.25	V
$N_{(A\text{-}R\ Count)}$				32		
INPUT CONTROLS (INP1, INP2), CURRENT SENSE SELECT (CS_SEL) & FAULT FLAG ($\overline{FLT}$)						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance		53	83	107	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 20 V			410	nA
$V_{(INP1_H)}$, $V_{(INP2_H)}$					2	V
$V_{(INP1_L)}$, $V_{(INP2_L)}$			0.8			V
$I_{(INP1)}$, $I_{(INP2)}$	INP Input leakage current			98	206	nA
$V_{(CS_SEL_H)}$	CS_SEL threshold for low side sensing				2	V
$V_{(CS_SEL_L)}$	CS_SEL threshold for high side sensing		0.8			V

6.6 Switching Characteristics

T_J = –40 °C to +125°C. $V_{(VS)}$ = 12 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{G1PU(INP_H)}$	INP1 Turn ON propogation Delay	INP1 ↑ to G1PU ↑, C_L = 47 nF	0.19		1.53	µs
$t_{G2(INP2_H)}$	INP2 Turn ON propogation Delay	INP2 ↑ to G2 ↑, C_L = 47 nF	2.7	4.5	6.7	µs
$t_{G1PD(INP_L)}$	INP1Turn OFF propogation Delay	INP1 ↓ to G1PD ↓, C_L = 47 nF		0.29	0.85	µs
$t_{G2(INP2_L)}$	INP2 Turn OFF propogation Delay	INP2 ↓ to G2 ↓, C_L = 47 nF	2.7	4.4	6.79	µs
$t_{PD(EN_OFF)}$	EN Turn OFF Propogation Delay	EN ↓ to G1PD ↓, C_L = 47 nF	2.2	4.6	6	µs
$t_{PD(UVLO_OFF)}$	UVLO Turn OFF Propogation Delay	UVLO ↓ to G1PD ↓ and $\overline{FLT}$ ↓, C_L = 47 nF	2.8	4.2	6	µs
t_{SC}	Hard Short-circuit protection propogation delay	$V_{(CS+-CS-)}$↑ $V_{(SCP)}$ to G1PD ↓, CL = 47 nF, $C_{(TMR)}$ = Open			4	µs
t_{SC_PUS}	Short-circuit protection propogation delay during power up with output short circuit	C_{TMR} = Open			10	µs

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6.6 Switching Characteristics (continued)

T_J = –40 °C to +125°C. $V_{(VS)}$ = 12 V, $V_{(BST-SRC)}$ = 11 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{ISCP}	ISCP Pulse current frequency			1.18		kHz

6.7 Typical Characteristics

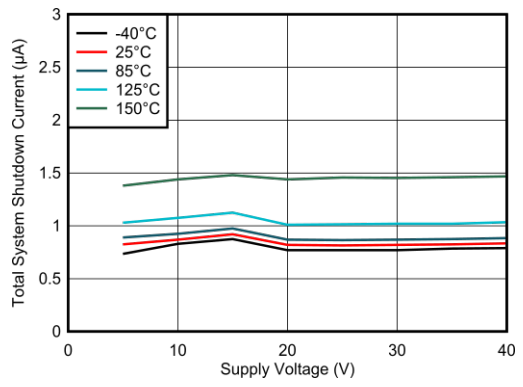


Figure 6-1. Shutdown Supply Current vs Supply Voltage

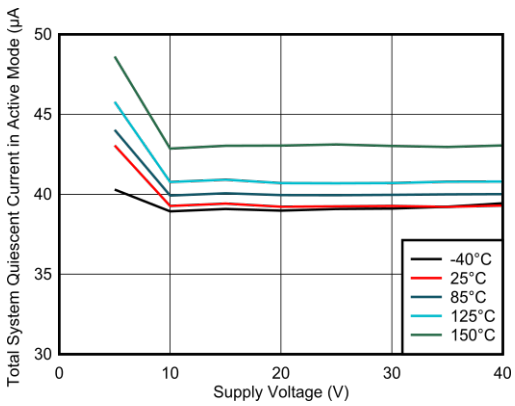


Figure 6-2. Operating Quiescent Current in Active Mode vs Supply Voltage

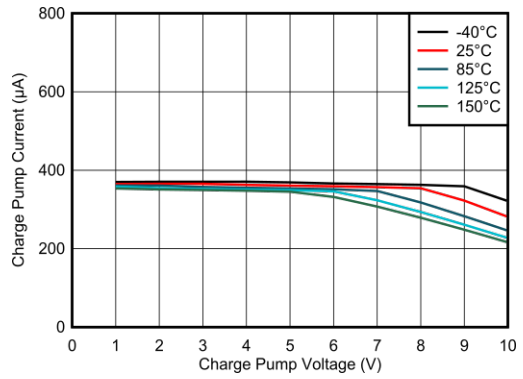
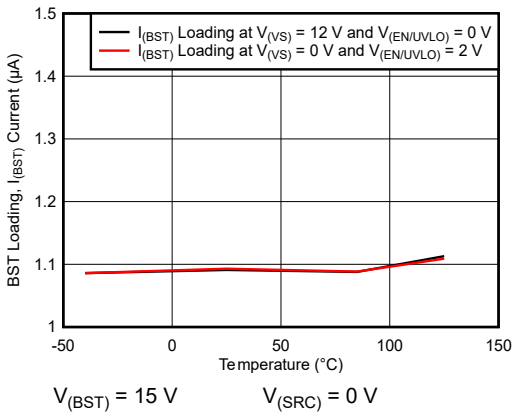


Figure 6-3. Charge Pump Current vs Charge Pump Voltage



$V_{(BST)}$ = 15 V $V_{(SRC)}$ = 0 V

Figure 6-4. BST Loading Current ($I_{(BST)}$) vs Temperature

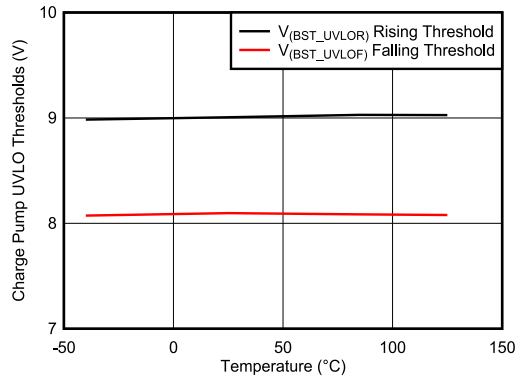


Figure 6-5. Charge Pump UVLO Thresholds vs Temperature

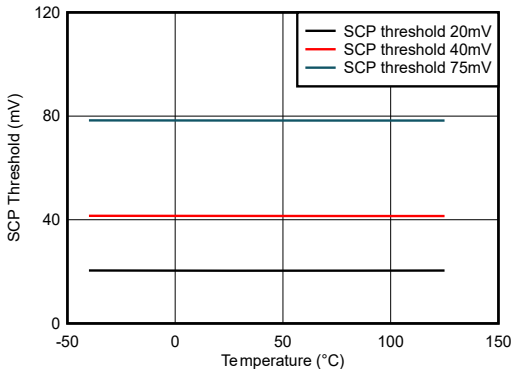


Figure 6-6. Short-Circuit Threshold ($V_{(SCP)}$) vs Temperature

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6.7 Typical Characteristics (continued)

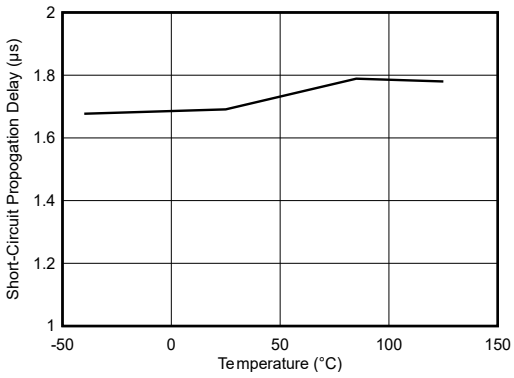


Figure 6-7. Short Circuit Protection Response Time (t_{SC}) vs Temperature

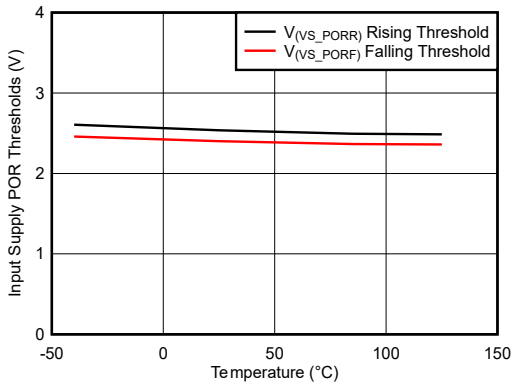


Figure 6-8. Input Supply POR Thresholds vs Temperature

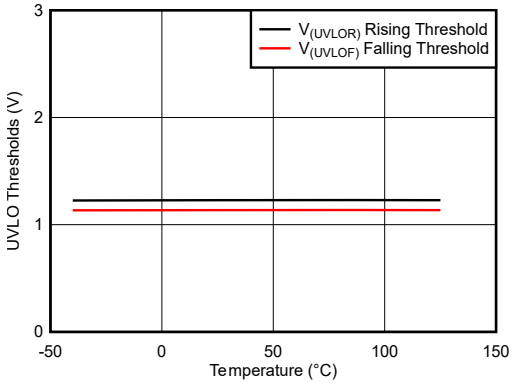


Figure 6-9. Input Supply UVLO Thresholds vs Temperature

7 Parameter Measurement Information

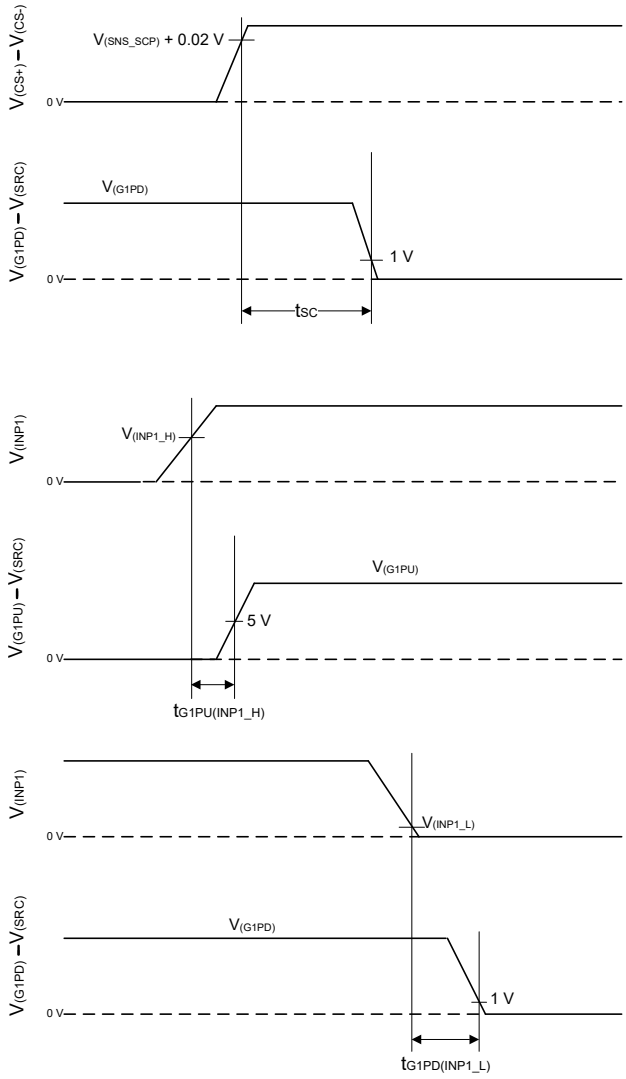


Figure 7-1. Timing Waveforms

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8 Detailed Description

8.1 Overview

The TPS1210x-Q1 family is a 45-V, low IQ, smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V – 40 V, the device is designed for 12-V, system designs. The device can withstand and protect the loads from negative supply voltages down to –40 V.

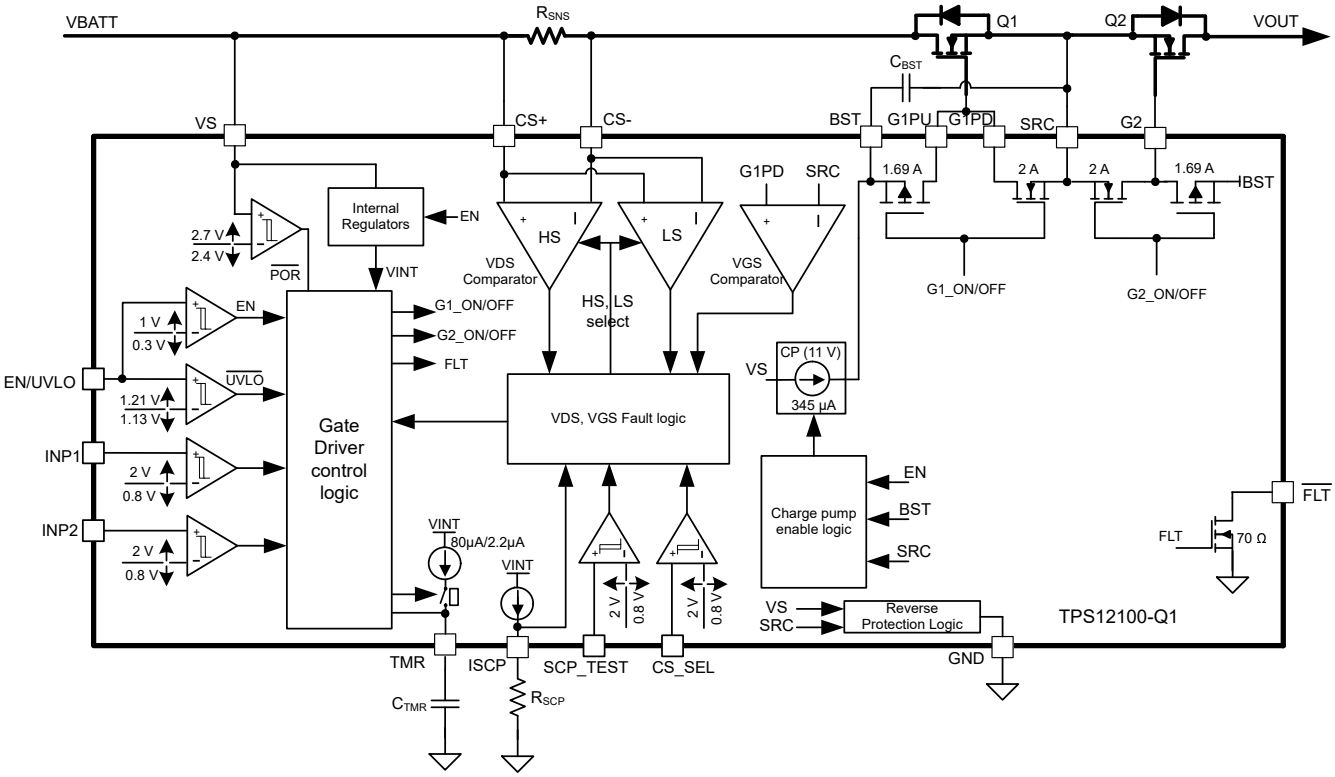
The device has two strong (2-A) GATE drivers with separate control inputs (INP1, INP2) to drive back-to-back MOSFETs in common source configuration. Strong GATE driving enables power switching using parallel FETs in high current system designs. TPS12100-Q1 has active high control inputs and TPS12101-Q1 has active low control inputs.

The device provides configurable short-circuit protection using ISCP and TMR pins for adjusting the threshold and response time respectively. Auto-retry and latch-off fault behavior can be configured. With TPS1210x-Q1, current sensing an be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. Diagnosis of the integrated short circuit comparator is possible using external control on SCP_TEST input.

The device indicates fault ($\overline{FLT}$) on open drain output during short circuit, charge pump undervoltage, and input undervoltage conditions.

Low Quiescent Current of 35 µA in operation enables always ON system designs. Quiescent current reduces to 1.5 µA (typical) with EN/UVLO low.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Charge Pump and Gate Driver Output (VS, G1PU, G1PD, G2, BST, SRC)

Figure 8-1 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses two strong 1.69-A/2-A peak source/sink gate drivers enabling paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 11-V, 345-µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the gate driver (BST and SRC).

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST_UVLOR)}$, the GATE driver section is activated. The device has a 1-V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET Q_G and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches 11.8 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 10 V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 11.8 V and 10 V as shown in the Figure 8-2.

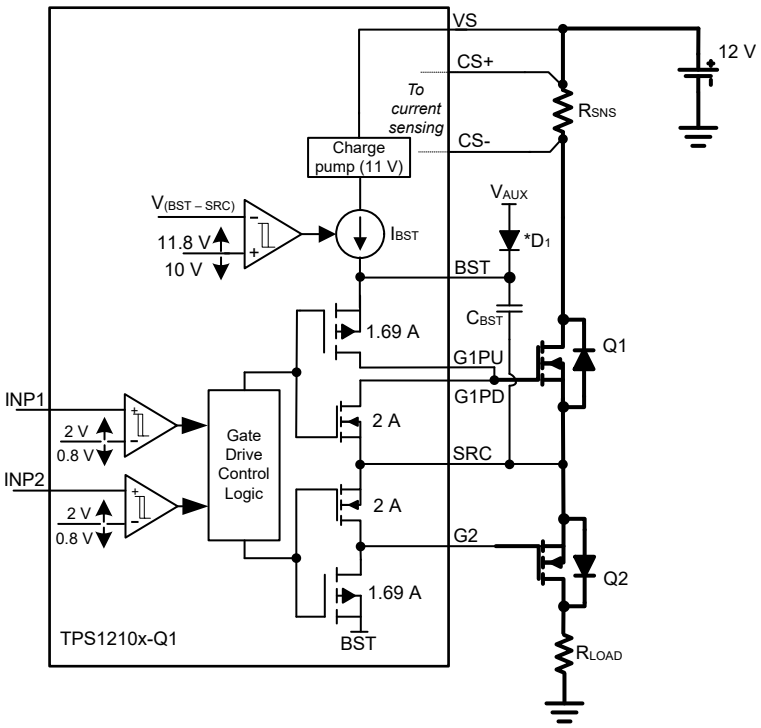


Figure 8-1. Gate Drivers

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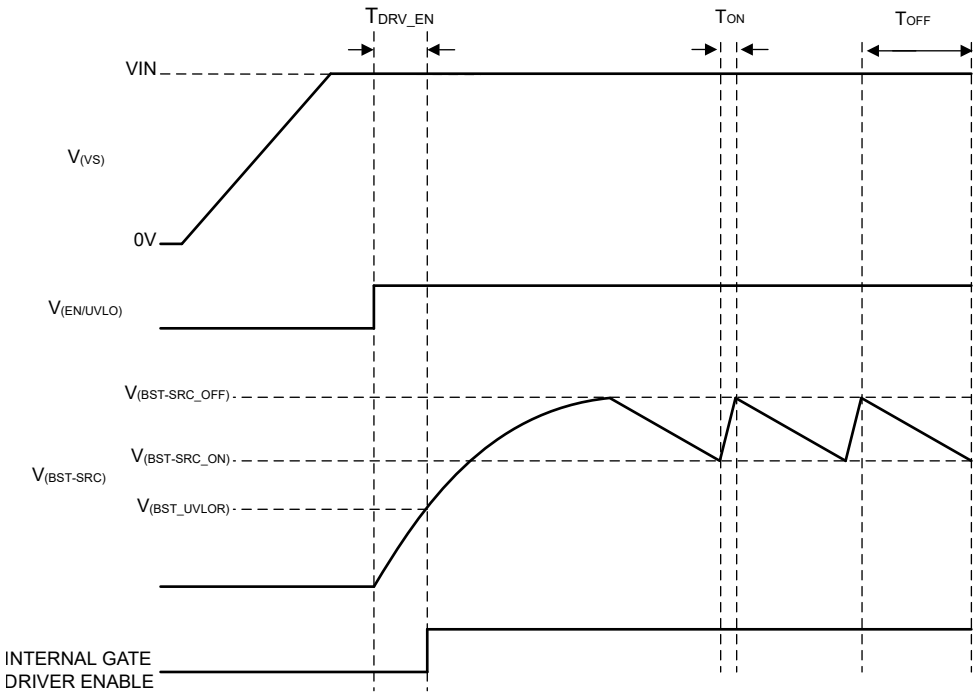


Figure 8-2. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay:

$$T_{DRV_EN} = \frac{C_{BST} \times V_{(BST_UVLOR)}}{345\ \mu A} \quad (1)$$

Where,

C_{BST} is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST_UVLOR)}$ = 9.5 V (maximum).

If T_{DRV_EN} must be reduced then pre-bias BST terminal externally using an external V_{AUX} supply through a low leakage diode D_1 as shown in . With this connection, T_{DRV_EN} reduces to 400 µs. TPS12100-Q1 application circuit with external supply to BST is shown in Figure 8-3.

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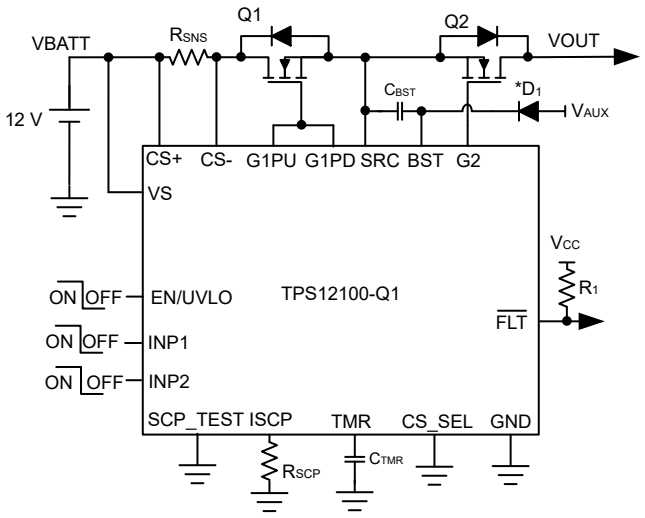


Figure 8-3. TPS12100-Q1 Application Circuit With External Supply to BST

Note

V_{AUX} can be supplied by external regulated supply ranging between 8 V and 18 V.

8.3.2 Capacitive Load Driving Using FET Gate (G1PU, G1PD) Slew Rate Control

For limiting inrush current during turn-ON of the external FET (Q1) with capacitive loads, use R_1, R_2, C_1 as shown in Figure 8-4. The R_1 and C_1 components slow down the voltage ramp rate at the gate of Q1 FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

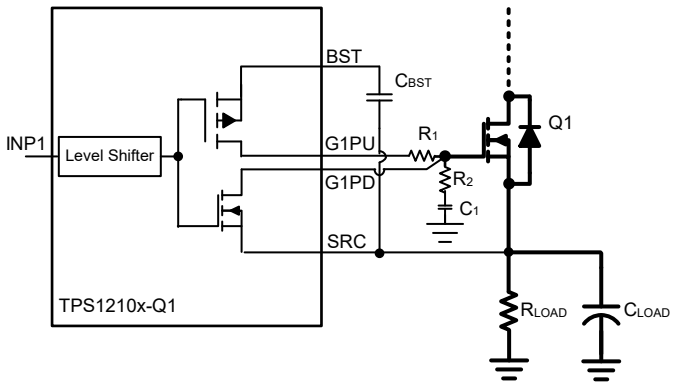


Figure 8-4. Inrush Current Limiting Using G1 Gate Drive

Use the Equation 2 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \quad (2)$$

$$C_1 = \frac{0.63 \times V_{(BST\ -\ SRC)} \times C_{LOAD}}{R_1 \times I_{INRUSH}} \quad (3)$$

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Where,

C_{LOAD} is the load capacitance.

VBATT is the input voltage and T_{charge} is the charge time.

$V_{(BST-SRC)}$ is the charge pump voltage (11 V),

Use a damping resistor R_2 (approximately 10 Ω) in series with C_1. Equation 3 can be used to compute required C_1 value for a target inrush current. A 100-kΩ resistor for R_1 can be a good starting point for calculations.

Connecting G1PD pin of TPS1210x-Q1 directly to the gate of the Q1 FET ensures fast turn-OFF without any impact of R_1 and C_1 components.

C_1 results in an additional loading on C_{BST} to charge during turn-ON. Use below equation to calculate the required C_{BST} value:

$$C_{BST} = \frac{Q_{g(total)}}{\Delta V_{BST}} + 10 \times C_1 \quad (4)$$

Where,

$Q_{g(total)}$ is the total gate charge of the FET,

ΔV_{BST} (1 V typical) is the ripple voltage across BST to SRC pins.

8.3.3 Short-Circuit Protection

The TPS1210x-Q1 feature adjustable short-circuit protection. The threshold and response time can be adjusted using R_{SCP} resistor and C_{TMR} capacitor respectively. The device senses the voltage across CS+ and CS– pins.

These pins can be connected across an external high and low side current sense resistor (R_{SNS}) or across the FET drain and source terminals for FET RDSON sensing as shown in Figure 8-5, Figure 8-6 and Figure 8-7 respectively.

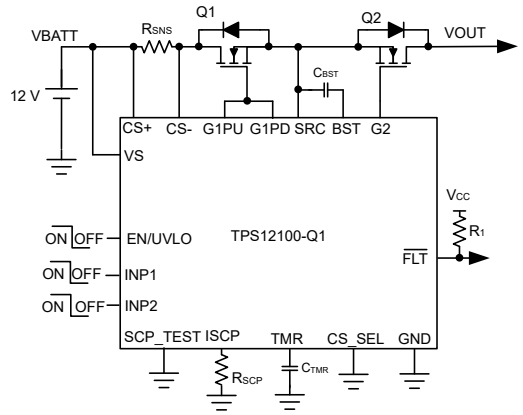


Figure 8-5. TPS12100-Q1 Application Circuit With External Sense Resistor RSNS based High Side Current Sensing

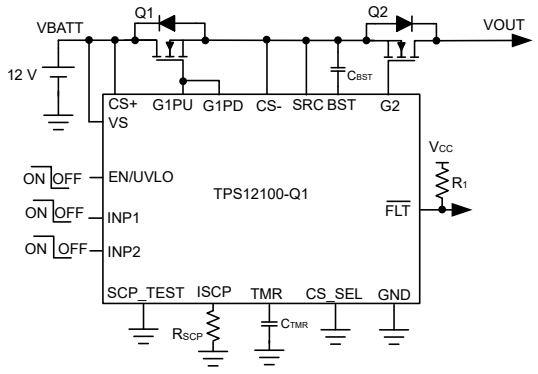


Figure 8-6. TPS12100-Q1 Application Circuit With MOSFET RDSON based Current Sensing

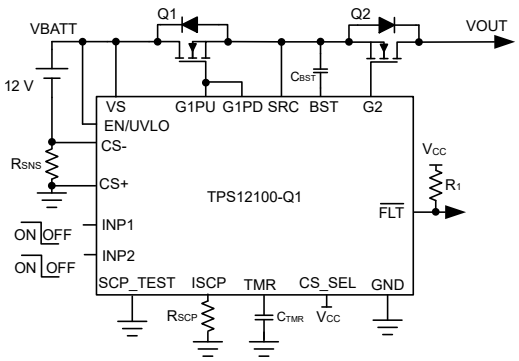


Figure 8-7. TPS12100-Q1 Application Circuit with External Sense Resistor RSNS based Low Side Current Sensing

Set the short-circuit detection threshold using an external R_{SCP} resistor across ISCP and GND pins. Use Equation 5 to calculate the required R_{SCP} value:

$$R_{SCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS} - 19\ mV\right)}{2\ \mu A} \quad (5)$$

Where,

R_{SNS} is the current sense resistor value or the FET R_{DSON} value.

I_{SC} is the desired short-circuit current level.

The short-circuit protection response is fastest with no C_{TMR} cap connected across TMR and GND pins.

With the device powered ON and EN/UVLO, INP1 pulled high, During Q1 turn-ON, first VGS of external FET Q1 (G1 gate drive) is sensed by monitoring the voltage across G1PD to SRC. Once G1PD to SRC voltage raises above $V_{(G1_GOOD)}$ threshold which ensures that the external FET is enhanced, then the SCP comparator output is monitored. If the sensed voltage across CS+ and CS– exceeds the short-circuit set point ($V_{(SCP)}$), G1PD pulls low to SRC and $\overline{FLT}$ asserts low. Subsequent events can be set either to be auto-retry or latch off as described in following sections.

VGS of external FET (Q1) is only monitored when CS_SEL is pulled low. VGS of external FET (Q1) is not monitored for low side current sensing.

Note

Short-circuit threshold can also be set by connecting external bias voltage on ISCP pin via buffer instead of R_{SCP} resistor enabling system design with improved SCP threshold accuracy as mentioned in electrical characteristics table. The external bias voltage to be forced on ISCP pin can be calculated by below eqaution:

$V_{(SCP_BIAS)}$ in mV = I_{SC} x R_{SNS} x 5 - 95mV

8.3.3.1 Short-Circuit Protection With Auto-Retry

The C_{TMR} programs the short-circuit protection delay (t_{SC}) and auto-retry time (t_{RETRY}). After the voltage across CS+ and CS– exceeds the set point, the C_{TMR} starts charging with 80-µA pullup current.

After C_{TMR} charges to $V_{(TMR_SC)}$, G1PD pulls low to SRC and $\overline{FLT}$ asserts low providing warning on impending FET turn-OFF. Post this event, the auto-retry behavior starts. The C_{TMR} capacitor starts discharging with 2.5-uA

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pulldown current. After the voltage reaches $V_{(TMR_LOW)}$ level, the capacitor starts charging with 2.2-uA pullup. After 32 charging-discharging cycles of C_{TMR} the FET turns ON back and $\overline{FLT}$ de-asserts.

The device retry time (t_{RETRY}) is based on C_{TMR} for the first time as per Equation 7.

Use Equation 6 to calculate the C_{TMR} capacitor to be connected across TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{SC}}{1.1} \quad (6)$$

Where,

I_{TMR} is internal pullup current of 80 µA.

t_{SC} is the desired short-circuit response time.

Leave TMR floating for fastest short-circuit response time.

$$t_{RETRY} = 22.7 \times 10^{6} \times C_{TMR} \quad (7)$$

If the short-circuit pulse duration is below t_{SC} then the FET remains ON and C_{TMR} gets discharged using internal pulldown switch.

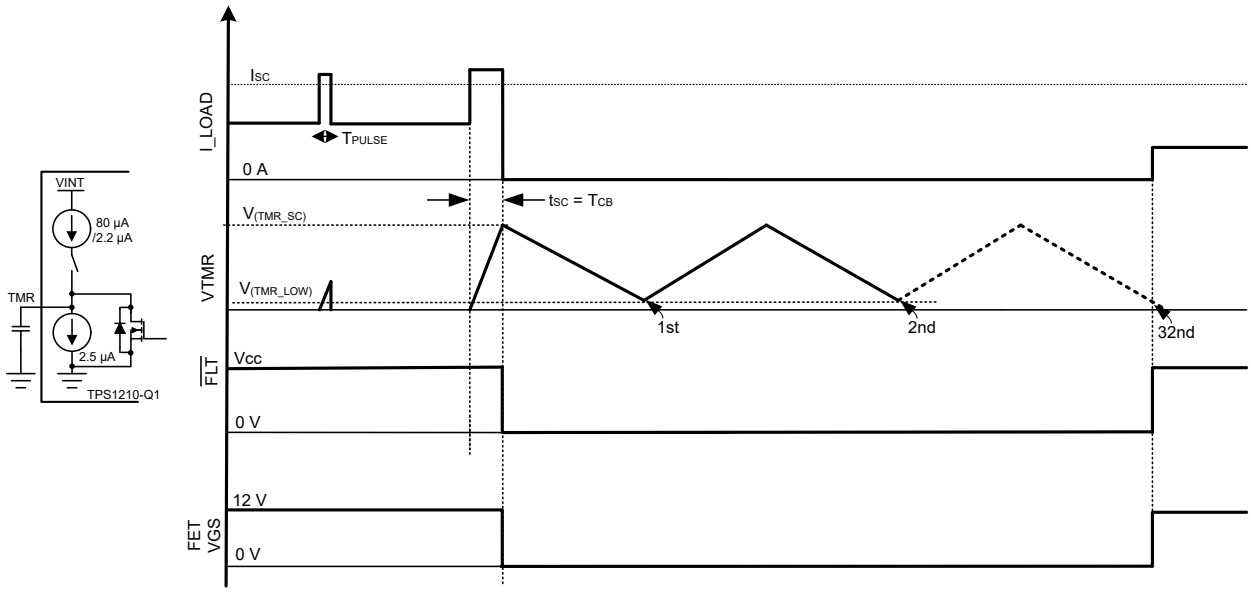


Figure 8-8. Short-Circuit Protection With Auto-Retry

8.3.3.2 Short-Circuit Protection With Latch-Off

Connect an approximately 100-kΩ resistor across C_{TMR} as shown in Figure 8-9. With this resistor, during the charging cycle, the voltage across C_{TMR} gets clamped to a level below $V_{(TMR_SC)}$ resulting in a latch-off behavior and $\overline{FLT}$ asserts low at same time.

Use Equation 8 to calculate C_{TMR} capacitor to be connected between TMR and GND for R_{TMR} = 100 kΩ.

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$$C_{TMR} = \frac{t_{SC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.1}{R_{TMR} \times 80\ \mu A}}\right)} \quad (8)$$

Where,

I_{TMR} is internal pullup current of 80 µA.

t_{SC} is the desired short-circuit response time.

Toggle INP or EN/UVLO (below $V_{(ENF)}$) or power cycle VS below $V_{(VS_PORF)}$ to reset the latch. At low edge, the timer counter is reset and C_{TMR} is discharged. G1PU pulls up to BST when INP is pulled high.

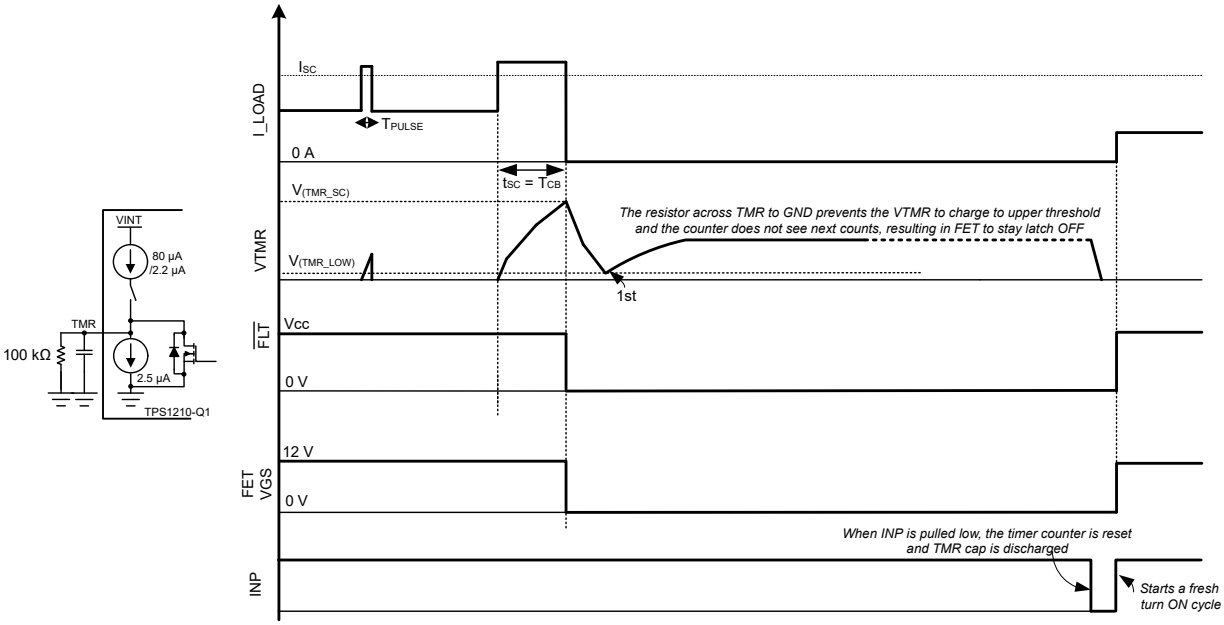


Figure 8-9. Short-Circuit Protection With Latch-Off

8.3.4 Undervoltage Protection (UVLO)

TPS1210x-Q1 has an accurate undervoltage protection (< ±2%) using EN/UVLO pin providing robust protection. Connect a resistor ladder as shown in Figure 8-10 for undervoltage protection threshold programming.

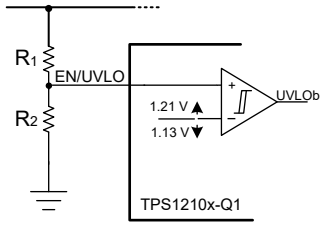


Figure 8-10. Programming Undervoltage Protection

8.3.5 Reverse Polarity Protection

The TPS1210x-Q1 devices features integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Reverse polarity faults occur during installation and maintenance

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of the end equipments. The device is tolerant to reverse polarity voltages down to –45 V both on input and on the output.

On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems the output negative voltage level is limited by the output side TVS or a diode.

8.3.6 Short-Circuit Protection Diagnosis (SCP_TEST)

In the safety critical designs, the short-circuit protection (SCP) feature and the diagnosis are important.

The TPS1210x-Q1 features the diagnosis of the internal short-circuit protection. When SCP_TEST is driven low to high, then a voltage is applied internally across the SCP comparator inputs to simulate a short-circuit event. The comparator output controls the gate drive (G1PU/G1PD) and also the $\overline{FLT}$. If the gate drive goes low (with initially being high) and $\overline{FLT}$ also goes low, then this action indicates that the SCP is good otherwise is to be treated as the SCP feature is not functional.

If the SCP_TEST feature is not used, then connect SCP_TEST pin to GND.

8.3.7 TPS1210x-Q1 as a Simple Gate Driver

Figure 8-11 shows application schematics of TPS1210x-Q1 as a simple gate driver in load connect-disconnect switch driving back-to-back FETs topology. The short-ciruit protection feature is disabled.

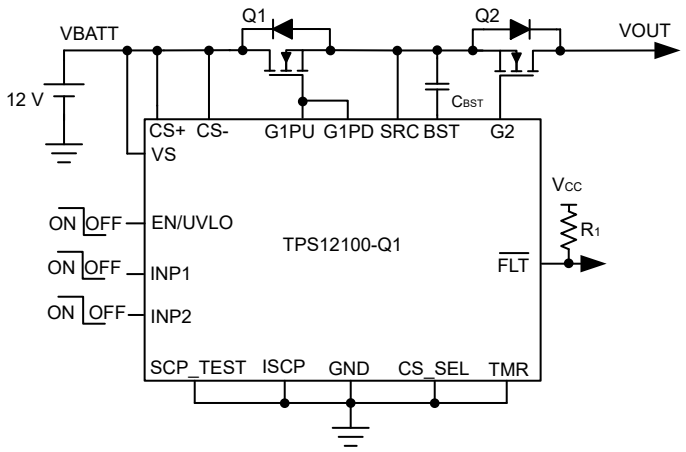


Figure 8-11. TPS12100-Q1 Application Circuit for Simple Gate Driver

8.4 Device Functional Modes

The TPS1210x-Q1 has two modes of operation. Active mode and low IQ shutdown mode.

If the EN/UVLO pin voltage is greater than $V_{(ENR)}$ rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers, all the protection and diagnostic features are enabled.

If the EN/UVLO voltage is pulled below $V_{(ENF)}$ falling threshold, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The gate drive and external FETs turn OFF. The TPS1210x-Q1 consumes low IQ of 1.5 µA (typical) in this mode.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS1210x-Q1 family is a 45-V, low IQ, smart high side driver with protection and diagnostics. The TPS1210x-Q1 device architecture is design to drive and control back-to-back N-Channel MOSFETs independently in common source configuration with separate control inputs (INP1, INP2), which makes TPS1210x-Q1 an excellent choice to realize circuit breaker in battery management system (BMS). The strong (2-A) GATE drivers enable switching parallel MOSFETs in high current applications such as circuit breaker in powertrain (DC/DC converter), driving loads in power distribution unit, circuit breaker in 12-V BMS, and so forth.

The TPS1210x-Q1 device provides configurable short-circuit protection using ISCP and TMR pins for adjusting the threshold and response time respectively. Auto-retry and latch-off fault behavior can be configured. By using CS+ and CS– pins, current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. The device also features diagnosis of the internal short circuit comparator using external control on SCP_TEST input.

The following design procedure can be used to select the supporting component values based on the application requirement.

9.2 Typical Application: Circuit Breaker in Battery Management System (BMS) using Low Side Current Sense

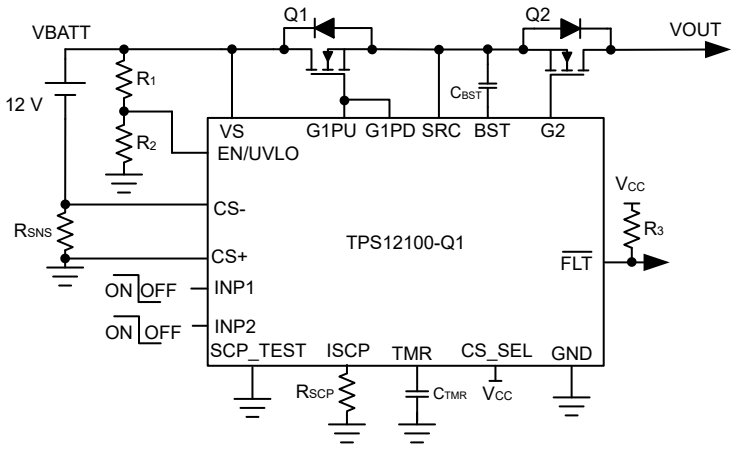


Figure 9-1. Typical Application Schematic: BMS Circuit Breaker With Low Side Current Sense

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9.2.1 Design Requirements

The following table shows the design parameters for this application example.

Table 9-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	12 V
Undervoltage lockout set point, VIN_{UVLO}	6.5 V
Maximum load current, I_{OUT}	25 A
Short-circuit protection threshold, I_{SC}	40 A
Short-circuit protection delay (t_{SC})	1 ms
Fault response	Auto-retry
Current sensing	Low-side

9.2.2 Detailed Design Procedure

Selection of Current Sense Resistor, R_{SNS}

The recommended range of the overcurrent protection threshold voltage, $V_{(SCP)}$, extends from 30 mV to 300 mV. Values near the low threshold of 30 mV can be affected by the system noise. Values near the upper threshold of 300 mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 40 mV is selected as the short-circuit protection threshold voltage. Use the following equation to calculate the current sense resistor, R_{SNS}.

$$R_{SNS} = \frac{V_{(SCP)}}{I_{SC}} \quad (9)$$

The next smaller available sense resistor 1 mΩ, 1% is chosen.

To improve signal to noise ratio or for better short-circuit protection accuracy, higher short-circuit protection threshold voltage, $V_{(SCP)}$ can be selected.

Programming the Short-Circuit Protection Threshold – R_{SCP} Selection

The R_{SCP} sets the short-circuit protection threshold. Use the following equation to calculate the value.

$$R_{SCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS} - 19\ \text{mV}\right)}{2\ \mu\text{A}} \quad (10)$$

To set 30-A as short-circuit protection threshold, R_{SCP} value is calculated to be 5.5 kΩ.

Choose the closest available standard value: 5.3 kΩ, 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor (R_{SNS}) and tweak the values during test in the real system. The RC filter components should not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

Programming the Short-Circuit Protection Delay – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This short-circuit protection delay, t_{SC} can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. Use the following equation to calculate the value of C_{TMR} to set 1 ms for t_{SC}.

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$$C_{TMR} = \frac{80\,\mu \times t_{SC}}{1.1} = 72.72\ \text{nF} \quad (11)$$

Choose closest available standard value: 82 nF, 10%.

Selection of MOSFETs, Q_1 and Q_2

For selecting the MOSFET Q_1 and Q_2 important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON-resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 35 V as the maximum application voltage, MOSFETs with V_{DS} voltage rating of 40 V is designed for this application.

The maximum V_{GS} TPS1210-Q1 can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred.

Based on the design requirements, BUK7S1R0-40H is selected and the ratings are:

- 40-V $V_{DS(MAX)}$ and 20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 0.88-mΩ typical at 10-V V_{GS}
- Maximum MOSFET $Q_{g(total)}$ is 137 nC

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 345 µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two BUK7S1R0-40H MOSFETs.

$$C_{BST} = \frac{Q_{g(total)}}{1\ \text{V}} = 274\ \text{nF} \quad (12)$$

Choose closest available standard value: 330 nF, 10 %.

Setting the Undervoltage Lockout

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider network of R_1 and R_2 connected between VS, EN/UVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 13.

$$V_{(UVLOR)} = \frac{R_2}{(R_1 + R_2)} \times VIN_{UVLO} \quad (13)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_1 and R_2. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{12})$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

From the device electrical specifications, $V_{(UVLOR)}$ = 1.21 V. From the design requirements, VIN_{UVLO} is 6.5 V. To solve the equation, first choose the value of R_1 = 470 kΩ and use Equation 13 to solve for R_2 = 107.5 kΩ. Choose the closest standard 1% resistor values: R_1 = 470 kΩ, and R_2 = 105 kΩ.

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9.2.3 Application Curves

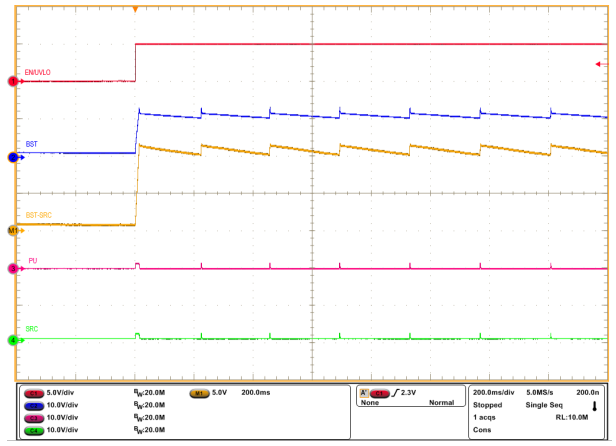


Figure 9-2. Start-Up Profile of Bootstrap Voltage with INP1=INP2 = GND and C_{BST} = 470 nF

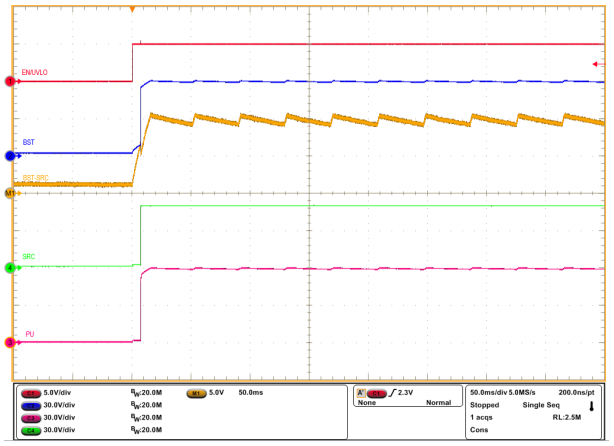


Figure 9-3. Start-Up Profile of Bootstrap Voltage with INP1=INP2 = HIGH and C_{BST} = 470 nF

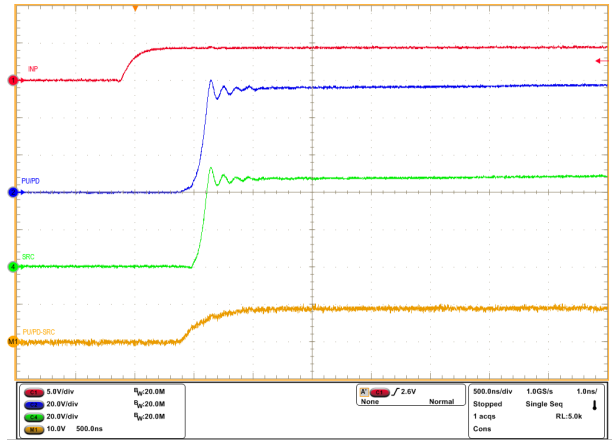


Figure 9-4. Turn-ON Response of TPS12100-Q1 for INP1 -> LOW to HIGH and C_{BST} = 470 nF

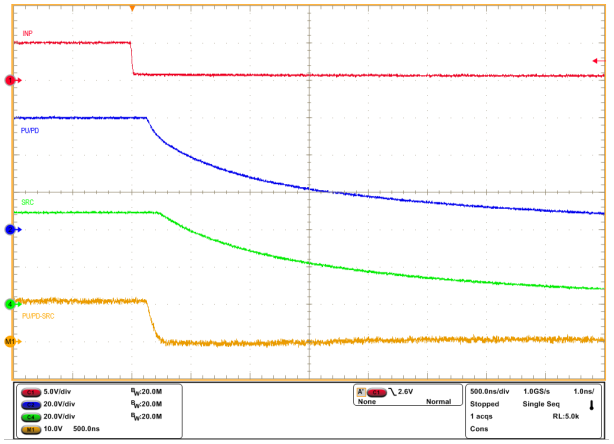


Figure 9-5. Turn-OFF Response of TPS12100-Q1 for INP1 -> HIGH to LOW and C_{BST} = 470 nF

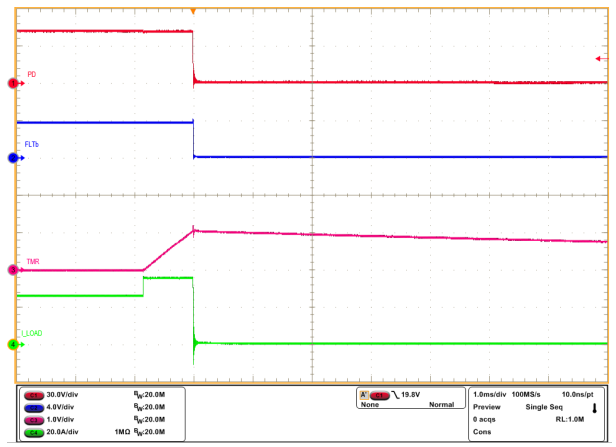


Figure 9-6. Overcurrent Response of TPS12100-Q1 for a Load Step from 25 A to 35 A with 30-A Overcurrent Protection Setting

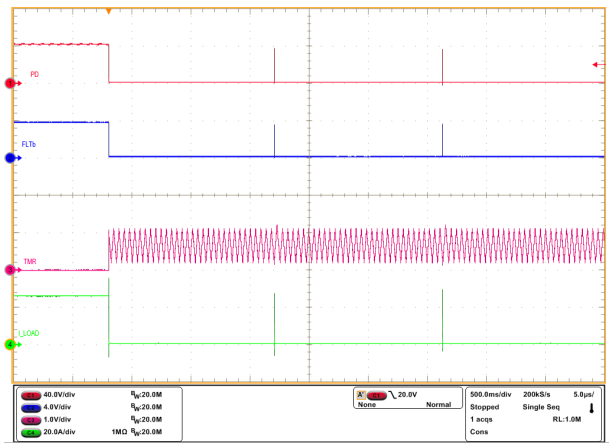


Figure 9-7. Auto-Retry Response of TPS12100-Q1 for an Overcurrent Fault

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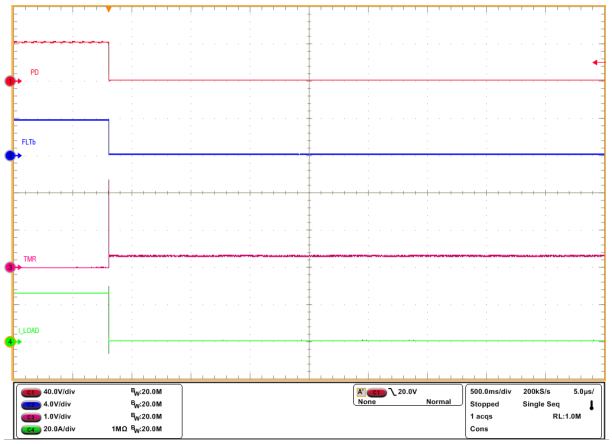


Figure 9-8. Latch-Off Response of TPS12100-Q1 for an Overcurrent Fault

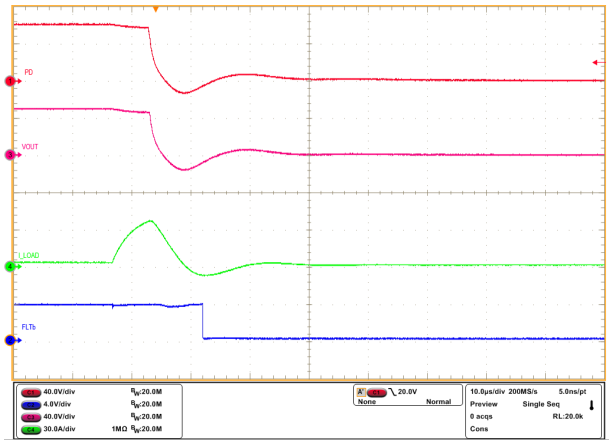


Figure 9-9. Output Short-Circuit Response of TPS12100-Q1 Device

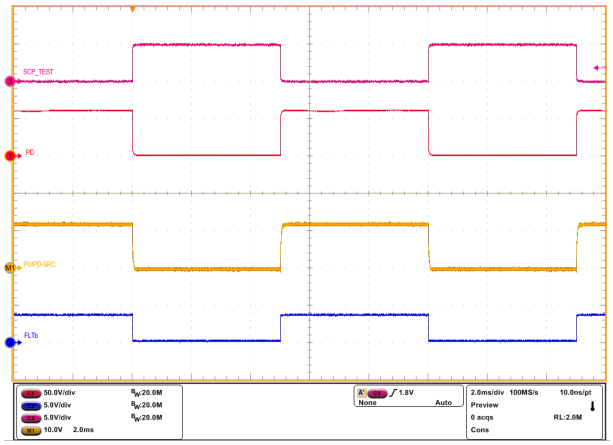


Figure 9-10. Short-Circuit Protection Diagnosis Test Response of TPS12100-Q1

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9.3 Power Supply Recommendations

When the external MOSFETs turn-OFF during the conditions such as INP1 control, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS1210-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS_PORR)}$ level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a R_{VS} – C_{VS} filter between the input supply line and VS pin to filter out the supply noise. TI recommends R_{VS} value around 100Ω.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor (R_{SNS}) and tweak the values during test in the real system. The RC filter components must not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

The following figure shows the circuit implementation with optional protection components.

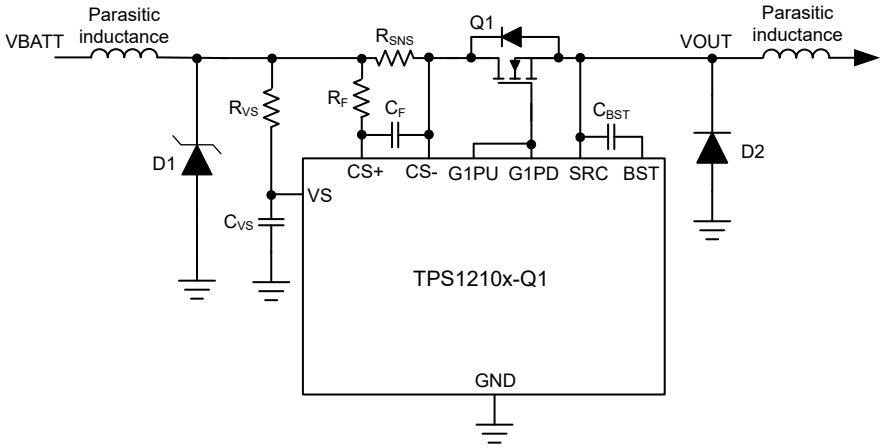


Figure 9-11. Circuit Implementation With Optional Protection Components For TPS1210-Q1

9.4 Layout

9.4.1 Layout Guidelines

- Place the sense resistor (R_{SNS}) close to the TPS1210x-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- Choose a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND for all the applications. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- Make the high-current path from the board input to the load, and the return path, parallel and close to each other to minimize loop inductance.
- Place the external MOSFETs close to the controller GATE drive pins (G1PU/PD and G2) such that the GATE of the MOSFETs are close to the controller GATE drive pins and forms a shorter GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- Place the external boot-strap capacitor close to BST and SRC pins to form very short loop.
- Connect the ground connections for the various components around the TPS1210x-Q1 directly to each other, and to the TPS1210x-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

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9.4.2 Layout Example

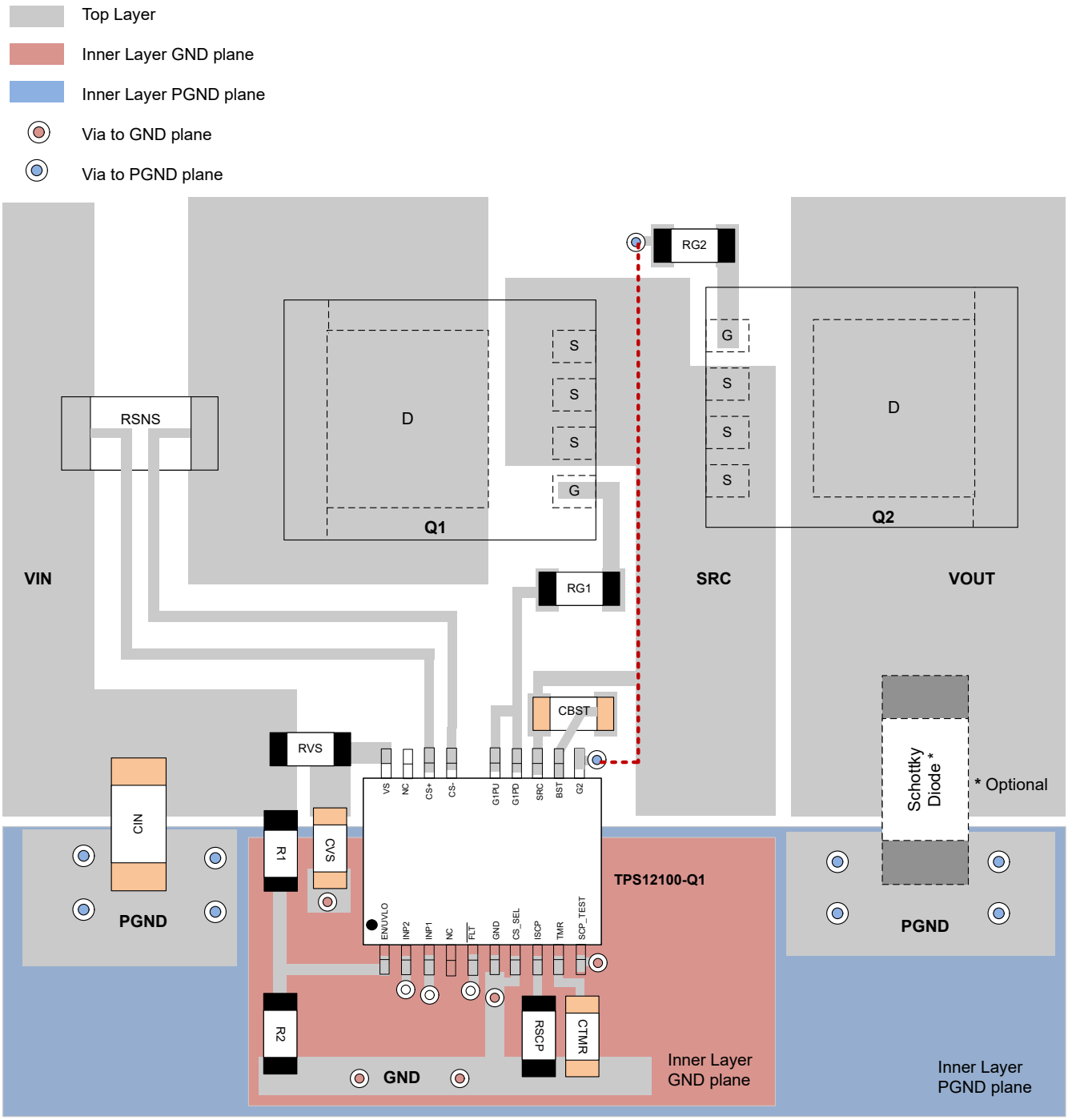


Figure 9-12. Typical PCB Layout Example for TPS1210-Q1 With B2B MOSFETs

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (December 2024)	Page
• Changed the document status From: *Advance Information* To: *Production Data*	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS12100QDGXRQ1	Active	Preproduction	VSSOP (DGX) | 19	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS12100QDGXRQ1.A	Active	Preproduction	VSSOP (DGX) | 19	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS12100QDGXRQ1	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1210
TPS12100QDGXRQ1.A	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1210

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

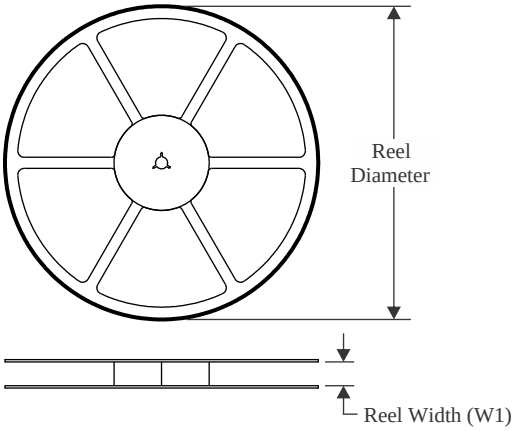
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

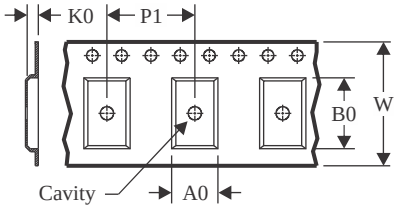
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

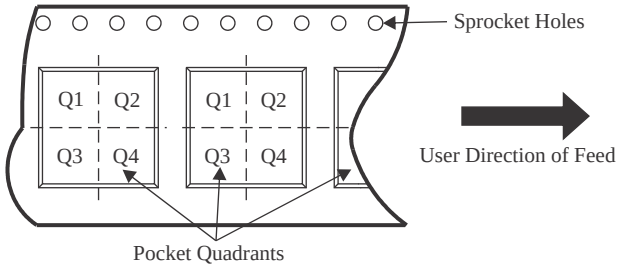


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

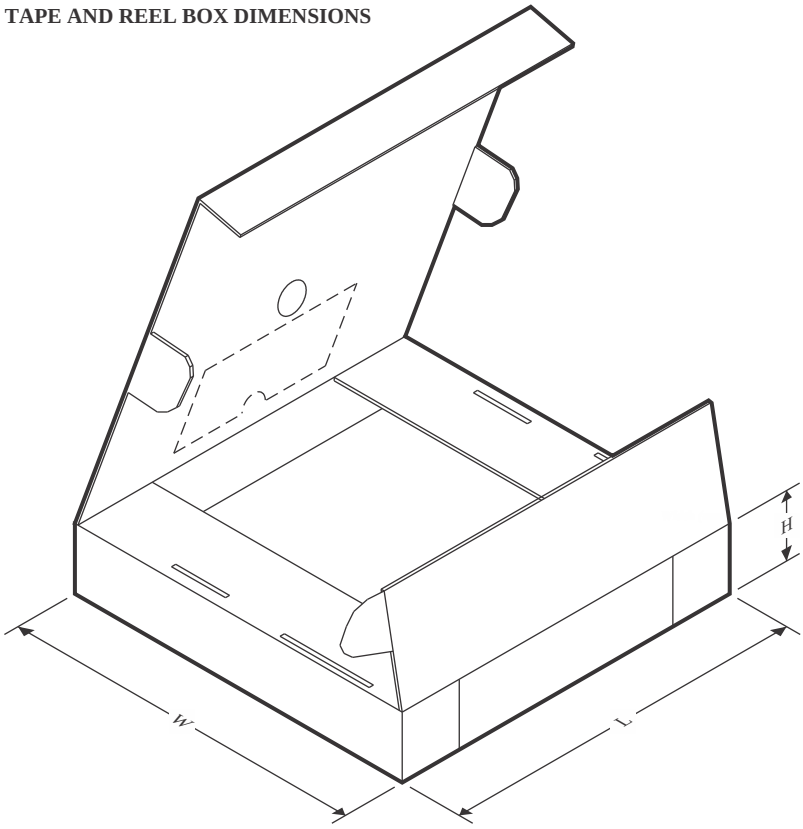
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS12100QDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

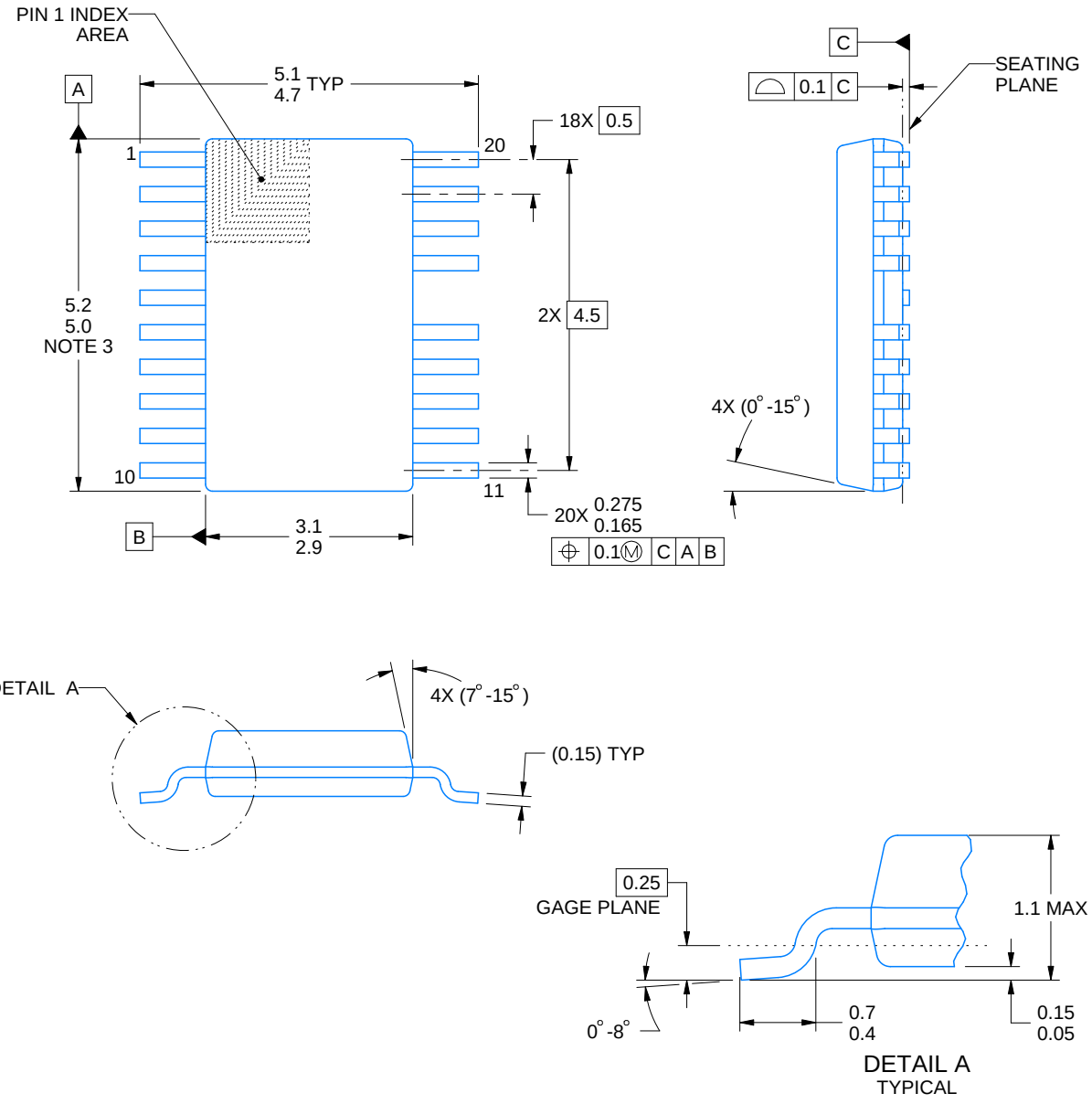
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS12100QDGXRQ1	VSSOP	DGX	19	5000	353.0	353.0	32.0

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

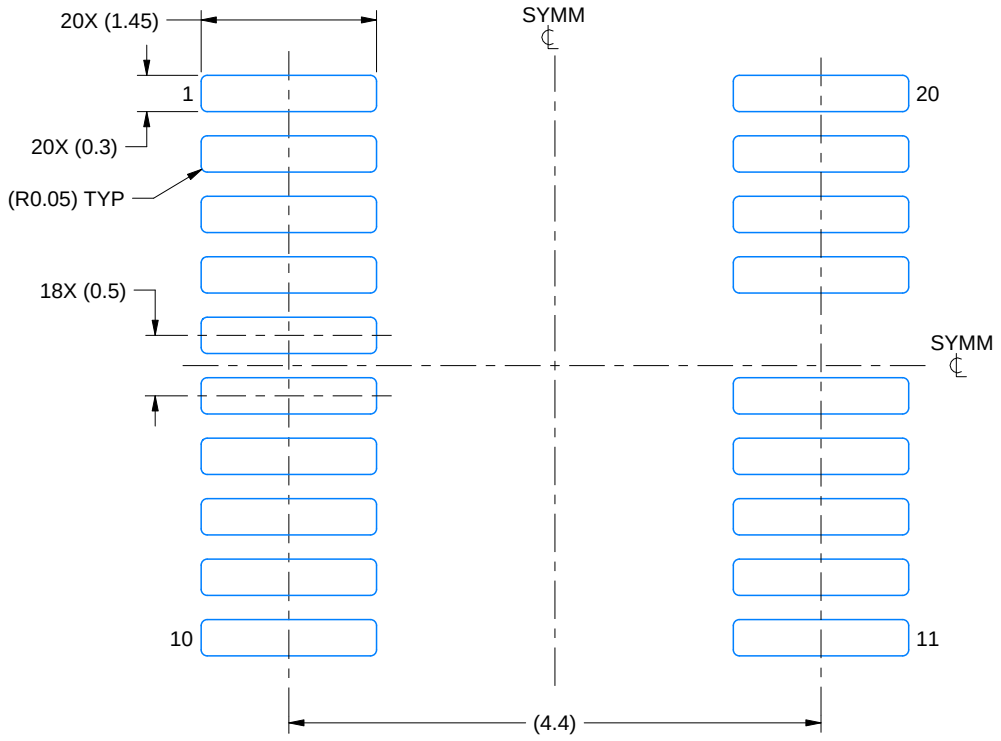
SMALL OUTLINE PACKAGE



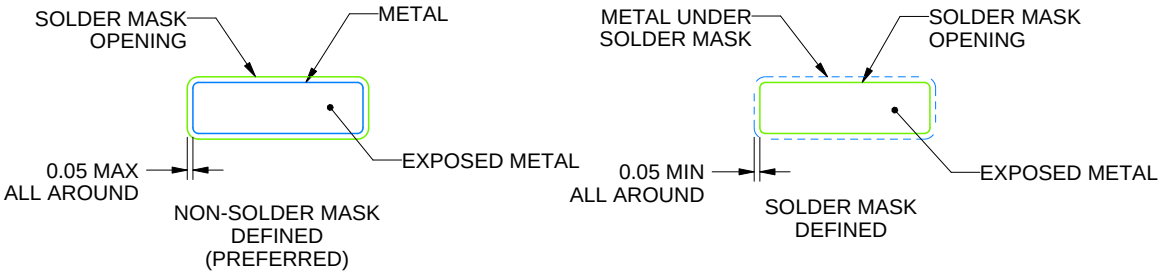
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

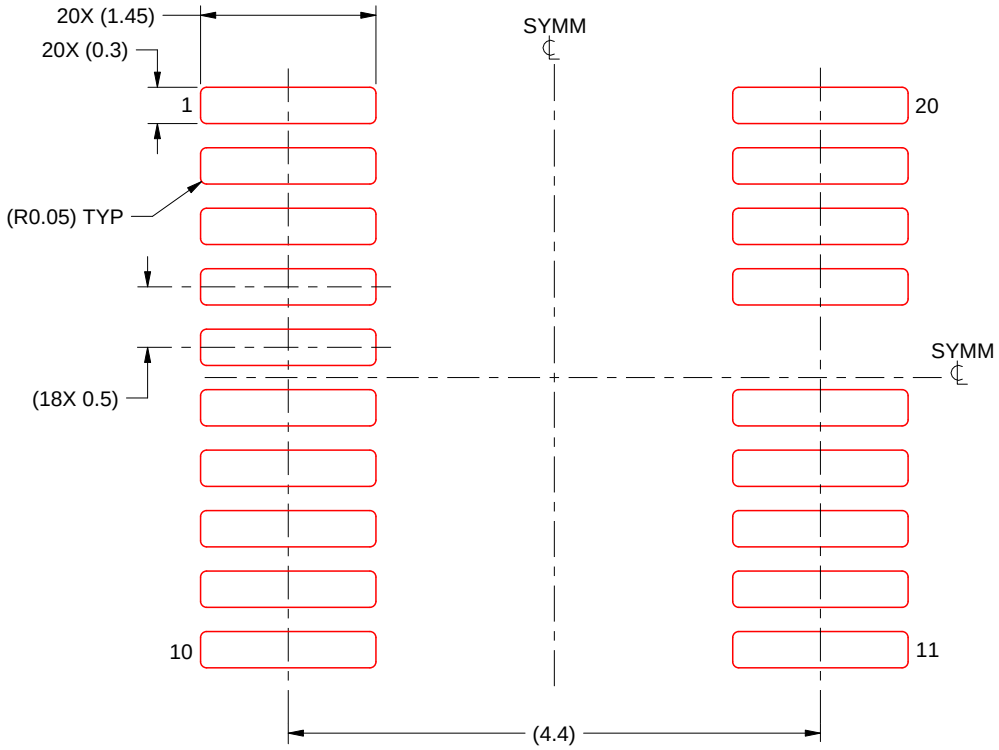


SOLDER MASK DETAILS

4226944/A 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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