TPLD1202 Programmable Logic Device With I²C/SPI and 10-GPIO

1 Features

- Operating characteristics
  - Extended temperature range: -40°C to 125°C
  - Wide supply voltage range: 1.71V to 5.5V
- Configurable macro-cells
  - 2-, 3-, and 4-bit lookup tables
  - D-type flip-flops and latches with and without reset/set option
  - 8-bit shift register
  - 16-bit pattern generator
  - 8-state state machine
  - Counters and delay generators
  - PWM generators
  - Watchdog timer
  - Programmable deglitch filter or edge detector
  - Multi-channel sampling analog comparator
  - Voltage reference and Analog temperature sensor
  - Oscillators
- Flexible digital I/O features
  - All digital signals can be routed to any GPIO
  - Digital input modes: digital in with and without Schmitt-trigger, low-voltage digital in
  - Digital output modes: push-pull, open-drain NMOS, tri-state
- Development tools
  - TPLD1202 evaluation module
  - TPLD programmer
  - InterConnect Studio
- In-line programming capable

2 Applications

- Factory automation and control
- Communications equipment
- Retail automation and payment
- Test and measurement
- Pro audio, video, and signage
- Personal electronics

3 Description

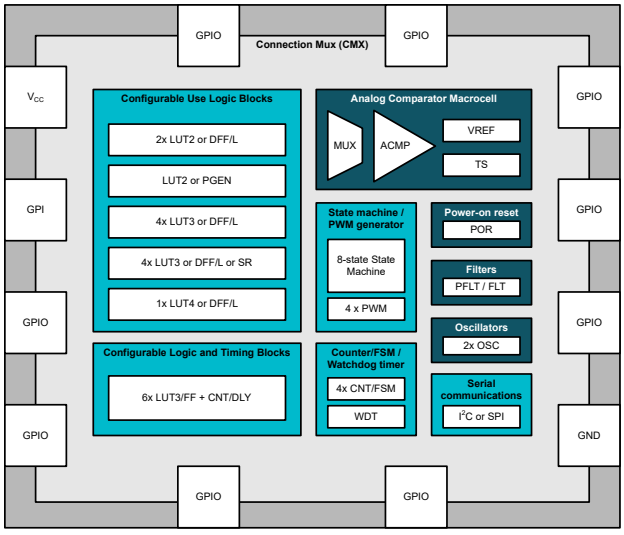
The TPLD1202 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks. TPLD provides a fully integrated, low power solution to implement common system functions, such as timing delays, voltage monitors, system resets, power sequencers, I/O expanders, and more. This device features configurable I/O structures that extends compatibility within mixed-signal environments, reducing the number of discrete components required.

System designers can create circuits and configure the macro-cells, I/O pins, and interconnections by temporarily emulating the non-volatile memory or by permanently programming the one-time programmable (OTP) through InterConnect Studio. The TPLD1202 is supported by a hardware and software ecosystem with application notes, reference designs, and design examples. Visit ti.com for more information and access to design tools.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPLD1202	DYY (SOT-23-THN, 14)	2.00mm × 4.20mm
	RWS (X2QFN, 12)	1.60mm × 1.60mm
	RWB (X2QFN, 12)	1.60mm × 1.60mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPLD1202 Simplified Block Diagram

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4 Pin Configuration and Functions

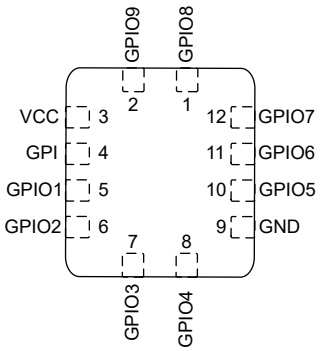


Figure 4-1. RWB Package, 12-Pin X2QFN, Top View

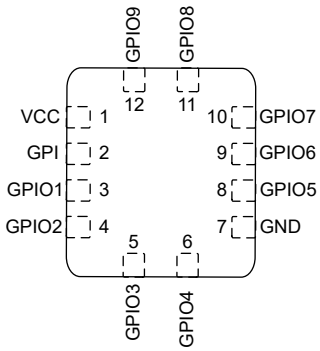


Figure 4-2. RWS Package, 12-Pin X2QFN, Top View

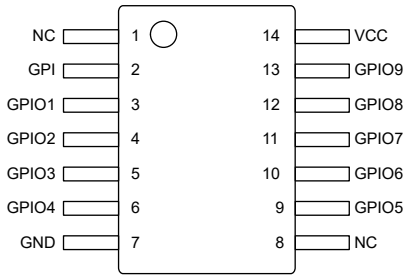


Figure 4-3. DYY Package, 14-Pin SOT-23-THN, Top View

Table 4-1. Pin Functions

PIN					DESCRIPTION			
NAME	RWB	RWS	DYY	TYPE (1)	Primary function	Secondary analog function (if any)	Secondary digital function (if any)	Secondary serial communications function (if any)
GPI	4	2	2	I	General-purpose input (3)		OSC0 Ext. CLK	I^2C address 3 / VPP
GPIO1	5	3	3	I/O	General-purpose I/O			SPI SCLK / I^2C SCL
GPIO2	6	4	4	I/O	General-purpose I/O			SPI SDI / I^2C SDA
GPIO3	7	5	5	I/O	General-purpose I/O with OE (4)			Interface select
GPIO4	8	6	6	I/O	General-purpose I/O with OE (4)	Ext. VREF IN		SPI SDO / I^2C address 4
GND	9	7	7	P	Ground			
GPIO5	10	8	9	I/O	General-purpose I/O	McACMP IN0		SPI nCS / I^2C address 5
GPIO6	11	9	10	I/O	General-purpose I/O	McACMP IN1		
GPIO7	12	10	11	I/O	General-purpose I/O	McACMP IN2		
GPIO8	1	11	12	I/O	General-purpose I/O with OE (4)	McACMP IN3	OSC1 Ext. CLK	I^2C address 6
GPIO9	2	12	13	I/O	General-purpose I/O with OE (4)			
VCC	3	1	14	P	Supply voltage			

Table 4-1. Pin Functions (continued)

PIN					DESCRIPTION			
NAME	RWB	RWS	DYY	TYPE (1)	Primary function	Secondary analog function (if any)	Secondary digital function (if any)	Secondary serial communications function (if any)
NC	—	—	1	—	Not internally connected (2)			
NC	—	—	8	—	Not internally connected (2)			

(1) P = power, I/O = input/output, I = Input
(2) Pins not internally connected must be grounded or left floating
(3) The general-purpose input (GPI) pin will sustain a high-voltage (VPP) during programming. Take special precaution with peripherals connected to this pin if performing in-system programming.
(4) The output enable (OE) connection is available through the connection mux and can be configured in InterConnect Studio.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage on V_{CC} relative to GND		-0.5	7	V
V_I	Input voltage		-0.5	V_{CC} + 0.5	V
V_O	Output voltage		-0.5	V_{CC} + 0.5	V
I_{IOK}	Input-output clamp current	V_{IO} < 0 or V_{IO} > V_{CC}	-50	50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	-50	50	mA
I_{DC}	Maximum average or DC current (through each pin)	Push-pull 1X		12	mA
		Push-pull 2X		17	
		Open-drain NMOS 1X		18	
		Open-drain NMOS 2X		28	
		Open-drain NMOS 4X		45	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC specification JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			1.71	5.5	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
V_{IH}	High-level input voltage	Logic input	1.71V to 5.5V	0.7 × V_{CC}		V
		Logic input with Schmitt trigger	1.71V to 5.5V	0.8 × V_{CC}		
		Low-voltage logic input	1.8V ± 0.09V	0.90		
			3.3V ± 0.3V	1.08		
			5V ± 0.5V	1.22		
V_{IL}	Low-level input voltage	Logic input	1.71V to 5.5V		0.3 × V_{CC}	V
		Logic input with Schmitt trigger	1.71V to 5.5V		0.2 × V_{CC}	
		Low-voltage logic input	1.8V ± 0.09V		0.47	
			3.3V ± 0.3V		0.52	
			5V ± 0.5V		0.57	
F_{IN_MAX}	Maximum input frequency	IN0 only	1.71V to 5.5V		250	kHz

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
$F_{(EXT\_OSC0)}$	External Oscillator Frequency	Logic input	1.71V to 5.5V		250	kHz
$F_{(EXT\_OSC1)}$	External Oscillator Frequency	Logic input	1.71V to 5.5V		25	MHz
T_A	Ambient temperature			–40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
RWB (X2QFN)	12	139.1	47.6	72.0	0.9	71.9	—	°C/W
DYY (SOT-23-THN)	14	137.3	65.9	58.1	3.8	57.9	—	°C/W
RWS (X2QFN)	12	139.1	47.6	72.0	0.9	71.9	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Supply and Power-on Reset								
V_{PORR}	Power-on reset voltage, V_{CC} rising		$V_I = V_{CC}$ or GND, $I_O = 0$		1.06		1.66	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		$V_I = V_{CC}$ or GND, $I_O = 0$		1.02		1.54	V
t_{SU}	Startup time		from V_{CC} rising past V_{PORR} to GPO becoming active			1.0		ms
V_{PP}	Programming voltage				7.5		8	V
t_{PP}	Programming time					50		ms
Digital IO								
V_{T+}	Positive-going input threshold voltage	Logic Input with Schmitt Trigger		1.8V ± 0.09V	0.94		1.27	V
				3.3V ± 0.3V	1.55		2.17	
				5V ± 0.5V	2.21		3.19	
V_{T-}	Negative-going input threshold voltage			1.8V ± 0.09V	0.58		0.94	V
				3.3V ± 0.3V	1.1		1.79	
				5V ± 0.5V	1.63		2.7	
V_{HYS}	Schmitt-Trigger hysteresis (V_{T+} - V_{T-})			1.8V ± 0.09V	0.25	0.36		V
				3.3V ± 0.3V	0.34	0.42		
				5V ± 0.5V	0.42	0.51		
V_{HYS}	IN0 hysteresis			1.71V to 5.5V			0.6	V

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Push-pull 1X	I_{OH} = -100µA	1.8V ± 0.09V	1.68			V
		Push-pull 2X			1.69			
		Push-pull 1X	I_{OH} = -3mA	3.3V ± 0.3V	2.47			
		Push-pull 2X			2.63			
		Push-pull 1X	I_{OH} = -5mA	5V ± 0.5V	3.84			
		Push-pull 2X			4.02			
V_{OH}	High-level output voltage	SPI SDO	I_{OH} = -2mA	1.71V to 5.5V	0.8 × V_{CC}			V
V_{OL}	Low-level output voltage	Push-pull 1X	I_{OL} = 100µA	1.8V ± 0.09V			0.01	V
		Push-pull 2X					0.01	
		Open-drain NMOS 1X					0.01	
		Open-drain NMOS 2X					0.01	
		Push-pull 1X	I_{OL} = 3mA	3.3V ± 0.3V			0.1	
		Push-pull 2X					0.1	
		Open-drain NMOS 1X					0.1	
		Open-drain NMOS 2X					0.1	
		Push-pull 1X	I_{OL} = 5mA	5V ± 0.5V			0.14	
		Push-pull 2X					0.14	
		Open-drain NMOS 1X					0.14	
		Open-drain NMOS 2X					0.14	
V_{OL}	Low-level output voltage	I^2C SCL, SDA pins (Open-drain NMOS 4X)	I_{OL} = 3mA	V_{CC} > 2V			0.4	V
		I^2C SCL, SDA pins (Open-drain NMOS 4X)	I_{OL} = 2mA	V_{CC} ≤ 2V			0.2 × V_{CC}	
		SPI SDO pin	I_{OL} = 2mA	1.71V to 5.5V			0.2 × V_{CC}	
I_{OL}	Low-level output current	I^2C SCL, SDA pins (Standard mode, Fast mode)	V_{OL} = 0.4V	1.71V to 5.5V	3			mA
		I^2C SCL, SDA pins (Fast mode Plus)	V_{OL} = 0.4V		20			
I_I	Input leakage current	All pins	V_I = V_{CC}	1.71V to 5.5V			±1	µA
			V_I = GND				±1	
I_{OZ}	Off-state (high-Z state) output current		V_O = 0 to 5.5V	1.71V to 5.5V			±1	µA
F_{OUT}	Max output frequency (1)	All IOs Push-pull 1X or Push-pull 2X	C_L = 15pF	1.8V ± 0.09V			8	MHz
				3.3V ± 0.3V			8	MHz
				5V ± 0.5V			8	MHz
$R_{pu(int)}$	Internal pull-up resistance					1		MΩ
						100		kΩ
						10		kΩ
$R_{pd(int)}$	Internal pull-down resistance					1		MΩ
						100		kΩ
						10		kΩ
C_I	Input pin capacitance	each input pin	V_I = V_{CC} or GND	1.71V to 5.5V		1.2		pF

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Input pin capacitance	I^2C SCL pin SPI SDI, SCK, nCS pins	$V_I = V_{CC}$ or GND	1.71V to 5.5V		4.1		pF
C_{IO}	Input-output pin capacitance	each I/O pin	$V_{IO} = V_{CC}$ or GND	1.71V to 5.5V		2.5		pF
C_{IO}	Input-output pin capacitance	I^2C SDA pin	$V_{IO} = V_{CC}$ or GND	1.71V to 5.5V		4.1		pF
Analog Comparator - Multi-channel Analog Comparator								
t_{start}	Start time	ACMP power on delay	1-channel, Bandgap force on, OSC1 force on	1.71V to 5.5V		100		µs
			1-channel, Bandgap auto on, OSC1 auto on	1.71V to 5.5V		190		µs
			OSC0 2kHz	1.71V to 5.5V		3.2		ms
			OSC0 10kHz	1.71V to 5.5V		640		µs
V_{AI}	Input voltage	Positive input		1.71V to 5.5V	0		V_{CC}	V
		Negative input			0		2.016	
V_{offset}	Input offset voltage	T_A = 25°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 1504mV	1.71V to 5.5V	-12.2		12.2	mV
		–40°C < T_A ≤ 125°C			-16.6		12.5	
		T_A = 25°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 2016mV	2.3V to 5.5V	-13.3		13.3	
		–40°C < T_A ≤ 125°C			-15.9		14.1	
dV_{IO}/dT	Input offset voltage drift	–40°C < T_A ≤ 125°C	V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 1504mV	1.71V to 5.5V		-9.7		µV/°C
			V_{HYS} = 0mV, Gain = 1, VREF = 32mV to 2016mV	2.3V to 5.5V		-9.7		
I_B	Input bias current						1	µA
C_{ID}	Input capacitance, differential					0.23		pF
C_{IM}	Input capacitance, common mode					1.20		pF

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
PROP	Propagation delay, response time	Low to High	1 channel, Gain = 1, Vref = 32mV to 1504mV, Overdrive = 32mV	1.71V to 5.5V			7.8	µs
		High to Low					4.9	
		Low to High	1 channel, Gain = 1, Vref = 32mV to 2016mV, Overdrive = 32mV	2.3V to 5.5V			7.8	
		High to Low					4.9	
		Low to High	Multi-channel, Gain = 1, Vref = 32mV to 1504mV, Overdrive = 32mV	1.71V to 5.5V			t_{SAMP_CLK} * CH	
		High to Low					t_{SAMP_CLK} * CH	
		Low to High	1 channel, Gain = 1, Vref = 32mV to 2016mV, Overdrive = 32mV	2.3V to 5.5V			t_{SAMP_CLK} * CH	
		High to Low					t_{SAMP_CLK} * CH	
Analog Comparator - Hysteresis								
V_{HYS}	Built-in hysteresis	–40°C < T_A ≤ 125°C	V_{HYS} = 64 mV	1.71V to 5.5V	61.7	62.7	65.9	mV
			V_{HYS} = 128 mV		123.4	126.7	132.2	
			V_{HYS} = 192 mV		185.4	190.3	197.9	
Analog Comparator - Input Gain								
R_{sin}	Series input resistance		Gain = 0.5	1.71V to 5.5V		1		MΩ
			Gain = 0.33			0.75		
			Gain = 0.25			1		
G_{err}	Gain error		Gain = 0.5	1.71V to 5.5V	-1.1		1.3	%
			Gain = 0.33		-1.8		1.8	
			Gain = 0.25		-1.8		1.7	
Voltage Reference								
VREF	Internal VREF error	T_A = 25°C	VREF = 32mV to 512mV	1.71V to 5.5V	-1.90	-0.3	1.90	%
		–40°C < T_A ≤ 125°C			-4.35		3.65	
		T_A = 25°C	VREF = 544mV to 1024mV		-1.50	-0.4	1.46	
		–40°C < T_A ≤ 125°C			-3.45		2.89	
		T_A = 25°C	VREF = 1056mV to 1504mV		-1.50	-0.4	1.48	
		–40°C < T_A ≤ 125°C			-3.44		2.90	
		T_A = 25°C	VREF = 1536mV to 2016mV	2.3 V to 5.5 V	-1.47	-0.7	1.42	
		–40°C < T_A ≤ 125°C			-3.07		6.28	
Analog Temperature Sensor								
T_{ERR}	Temperature sensor accuracy		10°C to 45°C	1.71V to 5.5V	-4.3		7.5	°C
			-40°C to 85°C		-10.6		11.1	
			-40°C to 105°C		-10.6		12.4	
			-40°C to 125°C		-10.6		14.2	

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
T_{OUT}	Temperature sensor output	-40°C	1.71V to 5.5V	1.193	1.242	1.289	V
		-30°C		1.151	1.197	1.236	
		-20°C		1.109	1.152	1.184	
		-10°C		1.067	1.107	1.133	
		0°C		1.025	1.061	1.084	
		10°C		0.983	1.016	1.035	
		20°C		0.940	0.972	0.989	
		25°C		0.917	0.949	0.966	
		30°C		0.895	0.927	0.943	
		40°C		0.850	0.883	0.899	
		50°C		0.803	0.840	0.857	
		60°C		0.756	0.796	0.815	
		70°C		0.709	0.753	0.774	
		80°C		0.661	0.709	0.734	
		85°C		0.638	0.687	0.714	
		90°C		0.614	0.665	0.694	
		100°C		0.566	0.621	0.654	
		110°C		0.519	0.578	0.615	
		120°C		0.472	0.534	0.576	
		125°C		0.449	0.512	0.556	

(1) Open drain switching performance will be limited by pull-up resistors used

5.6 Supply Current Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Standby												
I_{CC}	Standby	Inputs = 0V, Outputs = open, I_O = 0, BG forced off, OSC powered off, ACMP powered off		0.19			0.22			0.22		µA
I_{CC}	Standby, Bandgap enabled	Bandgap force on		2.40			2.42			2.44		µA
I_{CC}	Standby, Prebias enabled	Prebias force on		0.20			0.24			0.26		µA
Oscillator												
I_{CC}	OSC0 enabled: 2kHz or 10kHz	Predivide = 1		0.51			0.53			0.53		µA
		Predivide = 2		0.51			0.52			0.52		
		Predivide = 4		0.50			0.50			0.51		
		Predivide = 8		0.50			0.50			0.51		
I_{CC}	OSC1 enabled: 25MHz	Predivide = 1		254.4			256.9			258.5		µA
		Predivide = 2		218.2			220.0			221.3		
		Predivide = 4		198.9			200.3			201.6		
		Predivide = 8		187.6			189.3			190.0		

5.6 Supply Current Characteristics (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	OSC1 enabled: 25MHz	Normal startup, OSC output idle		2.41			2.16			2.41		µA
I_{CC}	OSC1 enabled: 25MHz	Fast startup enabled, OSC output idle		8.09			8.05			8.13		µA
Analog Comparator - Multi-channel Analog Comparator												
I_{CC}	Multi-channel sampling analog comparator (McACMP)	1 ch, External VREF (32mV), IN+ = 0V		0.94			0.90			0.94		µA
		1 ch, External VREF (32mV), IN+ = VCC		0.93			0.93			0.97		
		4 ch continuous sampling, External VREF (32mV), IN+ = 0V, OSC = 10kHz		0.90			0.97			0.99		
Voltage Reference												
I_{CC}	Voltage reference (VREF)	Internal VREF (32mV to 2016mV)		5.27			5.34			5.34		µA
Analog Temperature Sensor												
I_{CC}	Analog temperature sensor (TS)	Temperature sensor enabled		3.38			3.37			3.37		µA

5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Digital IO									
t_{pd}	Delay	Digital input	Push-pull output	Rising	1.8V ± 0.09V		33.5		ns
				Falling			31.2		
				Rising	3.3V ± 0.3V		19.9		
				Falling			16.5		
				Rising	5V ± 0.5V		12.3		
				Falling			18.3		
t_{pd}	Delay	Digital input with Schmitt trigger	Push-pull output	Rising	1.8V ± 0.09V		31.5		ns
				Falling			32.9		
				Rising	3.3V ± 0.3V		19.1		
				Falling			21.5		
				Rising	5V ± 0.5V		16.5		
				Falling			17.3		
t_{pd}	Delay	Low-voltage digital input	Push-pull output	Rising	1.8V ± 0.09V		25.5		ns
				Falling			30.5		
				Rising	3.3V ± 0.3V		16.1		
				Falling			18.1		
				Rising	5V ± 0.5V		11.4		
				Falling			15.9		

5.7 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Delay		Digital input	Open-drain NMOS output	Rising	1.8V ± 0.09V		—		ns
					Falling			31.2		
					Rising	3.3V ± 0.3V		—		
					Falling			20.8		
					Rising	5V ± 0.5V		—		
					Falling			21.2		
t_{pd}	Delay	Output enable from pin	OE	Push-pull output	Hi-Z to 1	1.8V ± 0.09V		38.8		ns
						3.3V ± 0.3V		26.7		
						5V ± 0.5V		21.1		
					Hi-Z to 0	1.8V ± 0.09V		35.7		ns
						3.3V ± 0.3V		23.1		
						5V ± 0.5V		18.4		
Configurable Use Logic										
t_{pd}	Delay	2-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		0.9		ns
					Falling			1.1		
					Rising	3.3V ± 0.3V		0.9		
					Falling			1.1		
					Rising	5V ± 0.5V		0.9		
					Falling			1.1		
t_{pd}	Delay	3-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		0.9		ns
					Falling			1.0		
					Rising	3.3V ± 0.3V		0.9		
					Falling			1.0		
					Rising	5V ± 0.5V		0.9		
					Falling			1.0		
t_{pd}	Delay	4-bit LUT	IN	OUT	Rising	1.8V ± 0.09V		1.0		ns
					Falling			1.3		
					Rising	3.3V ± 0.3V		0.9		
					Falling			1.7		
					Rising	5V ± 0.5V		4.9		
					Falling			1.7		
t_{pd}	Delay	DFF/Latch	CLK	Q	Rising	1.8V ± 0.09V		2.2		ns
					Falling			2.1		
					Rising	3.3V ± 0.3V		2.2		
					Falling			2.1		
					Rising	5V ± 0.5V		2.2		
					Falling			2.1		
t_{pd}	Delay	DFF/Latch	nRST/nSET	Q	Rising	1.8V ± 0.09V		2.3		ns
					Falling			2.2		
					Rising	3.3V ± 0.3V		2.1		
					Falling			2.3		
					Rising	5V ± 0.5V		2.1		
					Falling			2.2		

5.7 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Delay	Pattern generator	CLK	OUT	Rising	1.8V ± 0.09V		1.8		ns
					Falling			1.9		
					Rising	3.3V ± 0.3V		1.8		
					Falling			2.1		
					Rising	5V ± 0.5V		2.0		
					Falling			2.1		
Counter/Delay										
t_{pd}	Delay	Shift register	CLK	OUT	Rising	1.8V ± 0.09V		2.4		ns
					Falling			2.2		
					Rising	3.3V ± 0.3V		2.3		
					Falling			2.5		
					Rising	5V ± 0.5V		2.2		
					Falling			2.2		
t_{pd}	Delay	Shift register	nRST	OUT	Rising	1.8V ± 0.09V		2.5		ns
					Falling			2.6		
					Rising	3.3V ± 0.3V		2.3		
					Falling			2.3		
					Rising	5V ± 0.5V		2.2		
					Falling			2.5		
t_{pd}	Delay	Counter - Delay mode	Rising edge of IN	Rising edge of OUT	Falling edge triggered	1.8V ± 0.09V		3.3		ns
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			3.0		
			Rising edge of IN	Rising edge of OUT	Falling edge triggered	3.3V ± 0.3V		3.3		
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			3.0		
			Rising edge of IN	Rising edge of OUT	Falling edge triggered	5V ± 0.5V		3.3		
			Falling edge of IN	Falling edge of OUT	Rising edge triggered			3.0		
t_{pw}	Pulse width	Counter - Edge detect mode	Rising edge of OUT	Falling edge of OUT	Rising edge detect	1.8V ± 0.09V		23.3		ns
						3.3V ± 0.3V		21.6		
						5V ± 0.5V		21.9		
					Falling edge detect	1.8V ± 0.09V		21.3		
						3.3V ± 0.3V		21.1		
						5V ± 0.5V		21.2		
					Both edge detect	1.8V ± 0.09V		21.6		
						3.3V ± 0.3V		21.2		
						5V ± 0.5V		21.3		
State Machine										
t_{st_pw}	State transition pulse width					1.8V ± 0.09V	15.0	26	75.0	ns
						3.3V ± 0.3V	15.0	25	75.0	
						5V ± 0.5V	15.0	25	75.0	

5.7 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{st_dly}	State transition delay				1.8V ± 0.09V	25.0	63.3	155.0	ns
					3.3V ± 0.3V	25.0	51.3	140.0	
					5V ± 0.5V	25.0	52.4	135.0	
Oscillator									
f_{err}	Oscillator frequency error			OSC0 2kHz	1.8V ± 0.09V	-5.9		3.9	%
					3.3V ± 0.3V	-6.0		3.8	
					5V ± 0.5V	-6.0		3.6	
				OSC0 10kHz	1.8V ± 0.09V	-5.9		3.9	%
					3.3V ± 0.3V	-6.0		3.8	
					5V ± 0.5V	-6.0		3.6	
				OSC1 25MHz	1.8V ± 0.09V	-6.6		4.5	%
					3.3V ± 0.3V	-6.5		4.6	
					5V ± 0.5V	-6.5		4.6	
t_{d_osc}	Oscillator startup delay			OSC0 2kHz	1.8V ± 0.09V		0.9		µs
					3.3V ± 0.3V		1.0		
					5V ± 0.5V		1.0		
				OSC0 10kHz	1.8V ± 0.09V		0.9		µs
					3.3V ± 0.3V		1.0		
					5V ± 0.5V		1.0		
				OSC1 25MHz	1.8V ± 0.09V		3.2		µs
					3.3V ± 0.3V		3.1		
					5V ± 0.5V		3.0		
				OSC1 25MHz, fast startup enabled	1.8V ± 0.09V		0.4		µs
					3.3V ± 0.3V		0.4		
					5V ± 0.5V		0.4		
t_{d_bg}	Bandgap startup delay			Bandgap auto on	1.8V ± 0.09V		103.3		µs
					3.3V ± 0.3V		89.5		
					5V ± 0.5V		90.1		
t_{set_osc}	Oscillator startup settling time			OSC0 2kHz	1.8V ± 0.09V		99.0		µs
					3.3V ± 0.3V		100.0		
					5V ± 0.5V		105.0		
				OSC0 10kHz	1.8V ± 0.09V		99.0		µs
					3.3V ± 0.3V		100.0		
					5V ± 0.5V		105.0		
				OSC1 25MHz	1.8V ± 0.09V		4.2		µs
					3.3V ± 0.3V		3.6		
					5V ± 0.5V		2.6		
t_{d_err}	Delay error			OSC (Forced power on)	1.71V to 5.5V	0		1	CLK cycle
Programmable Filter									

5.7 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pflt_pw}	Pulse width	Programmable filter - Edge detect mode	Rising edge of OUT	Falling edge of OUT	1 cell	1.8V ± 0.09V		152.6		ns
						3.3V ± 0.3V		152.0		
						5V ± 0.5V		152.2		
					2 cells	1.8V ± 0.09V		250.6		ns
						3.3V ± 0.3V		250.4		
						5V ± 0.5V		249.9		
					3 cells	1.8V ± 0.09V		348.4		ns
						3.3V ± 0.3V		347.8		
						5V ± 0.5V		347.3		
					4 cells	1.8V ± 0.09V		444.9		ns
						3.3V ± 0.3V		444.5		
						5V ± 0.5V		444.5		
t_{pflt_pd}	Delay	Programmable filter - Edge detect mode			Any cells	1.8V ± 0.09V		67.4		ns
						3.3V ± 0.3V		67.3		
						5V ± 0.5V		67.2		
t_{pflt_d}	Delay	Programmable filter - Both edge delay mode	Rising/Falling edge of IN	Rising/Falling edge of OUT	1 cell	1.8V ± 0.09V		171.3		ns
						3.3V ± 0.3V		171.1		
						5V ± 0.5V		170.7		
					2 cells	1.8V ± 0.09V		269.4		ns
						3.3V ± 0.3V		269.2		
						5V ± 0.5V		268.5		
					3 cells	1.8V ± 0.09V		366.8		ns
						3.3V ± 0.3V		366.6		
						5V ± 0.5V		366.1		
					4 cells	1.8V ± 0.09V		464.0		ns
						3.3V ± 0.3V		463.9		
						5V ± 0.5V		463.4		

5.8 I²C Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			STANDARD MODE (Sm)		FAST MODE (Fm)		FAST MODE PLUS (Fm+)		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	0	1000	kHz
t_{sch}	I²C clock high time		4		0.6		0.26		µs
t_{scl}	I²C clock low time		4.7		1.3		0.5		µs
t_{sp}	I²C spike time			50		50		50	ns
t_{sds}	I²C serial-data setup time		250		100		50		ns
t_{sdh}	I²C serial-data hold time		0		0		0		ns
t_{icr}	I²C input rise time			1000	20	300		120	ns
t_{icf}	I²C input fall time			300	20 × (V_{CC} / 5.5 V)	300	20 × (V_{CC} / 5.5 V)	120	ns

5.8 I²C Bus Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			STANDARD MODE (Sm)		FAST MODE (Fm)		FAST MODE PLUS (Fm+)		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ocf}	I²C output fall time	10-pF to 400-pF bus (Sm/Fm) 10-pF to 550-pF bus (Fm+)		300		300		120	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		0.5		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		0.26		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		0.26		µs
t_{sps}	I²C stop condition setup		4		0.6		0.26		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45		0.9		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45		0.9		0.45	µs
C_b	I²C bus capacitive load			400		400		550	pF

5.9 SPI Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK, SPI clock frequency			4	MHz
t_{SCLK}	SCLK, SPI clock period	250			ns
t_R	SDI, nCS, and SCLK signals rise time			40	ns
t_F	SDI, nCS, and SCLK signals fall time			40	ns
t_{SCLKH}	SCLK High time	125			ns
t_{SCLKL}	SCLK Low time	125			ns
t_{NCS_SU}	nCS setup time before rising edge of SCLK	100			ns
t_{NCS_HOLD}	nCS hold time after falling edge of SCLK	100			ns
t_{NCS_DIS}	nCS disable time	50			ns
t_{SDI_SU}	SDI setup time before rising edge of SCLK	50			ns
t_{SDI_HOLD}	SDI hold time after rising edge of SCLK	50			ns
t_{SDO_VALID}	Time from falling edge of SCLK to next SDO data			80	ns
t_{SDOR}	SDO rise time			40	ns
t_{SDOF}	SDO fall time			40	ns

5.10 Typical Characteristics

T_A = 25°C

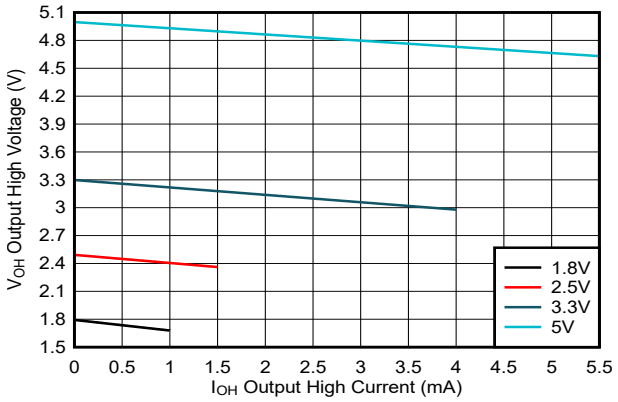


Figure 5-1. Typical 1X Push-Pull Output Voltage in the High State (V_{OH})

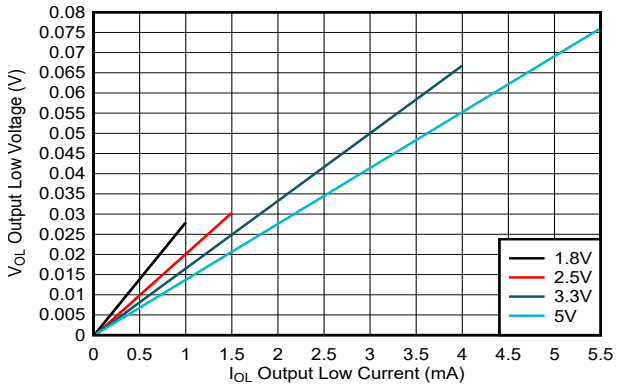


Figure 5-2. Typical 1X Push-Pull Output Voltage in the Low State (V_{OL})

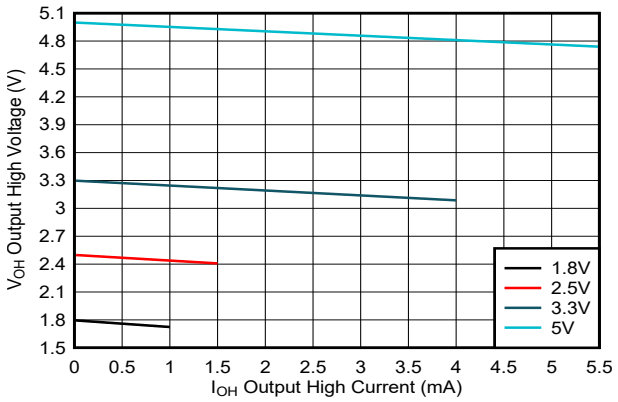


Figure 5-3. Typical 2X Push-Pull Output Voltage in the High State (V_{OH})

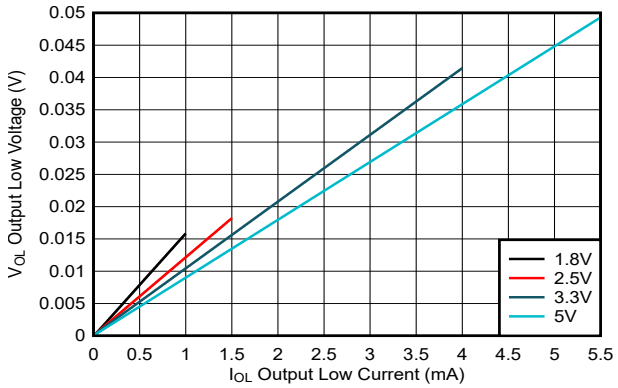


Figure 5-4. Typical 2X Push-Pull Output Voltage in the Low State (V_{OL})

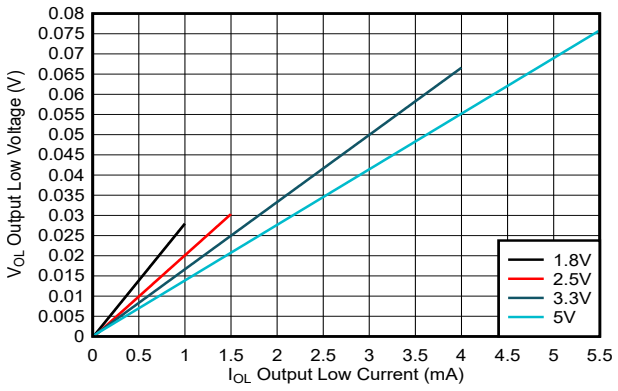


Figure 5-5. Typical 1X Open-Drain NMOS Output Voltage in the Low State (V_{OL})

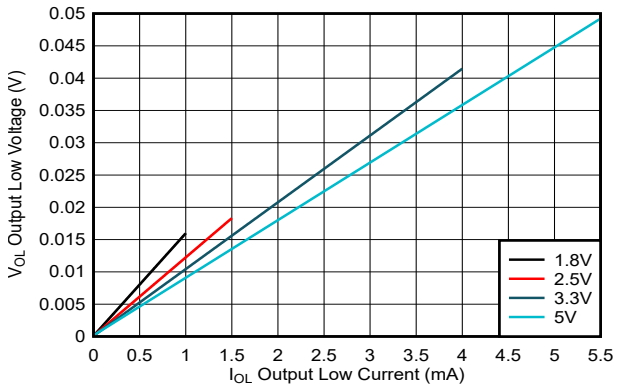


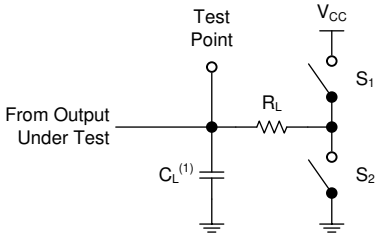
Figure 5-6. Typical 2X Open-Drain NMOS Output Voltage in the Low State (V_{OL})

6 Parameter Measurement Information

Phase relationships between waveforms are selected arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 5ns.

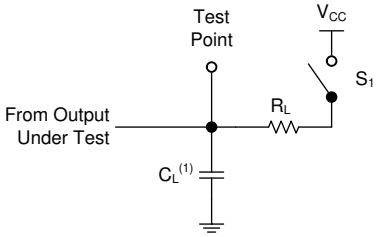
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



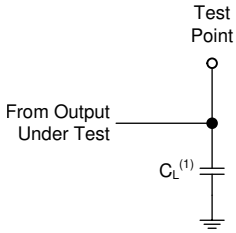
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-2. Load Circuit for Open-Drain Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-3. Load Circuit for Push-Pull Outputs

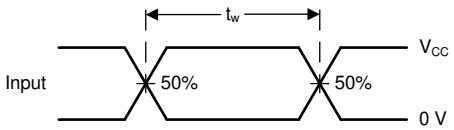


Figure 6-4. Voltage Waveforms, Pulse Duration

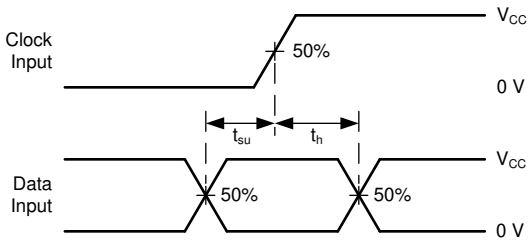
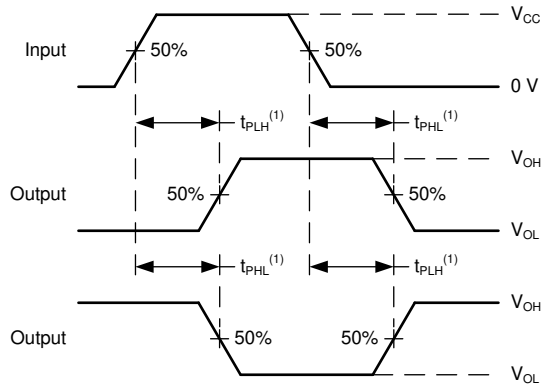
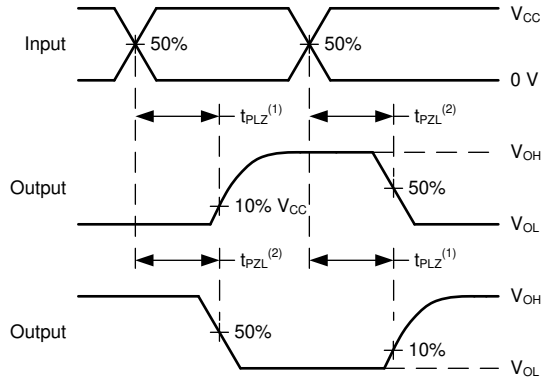


Figure 6-5. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-6. Voltage Waveforms Propagation Delays



(1) The greater between t_{PLZ} and t_{PZL} is the same as t_{pd}.

Figure 6-8. Voltage Waveforms Propagation Delays

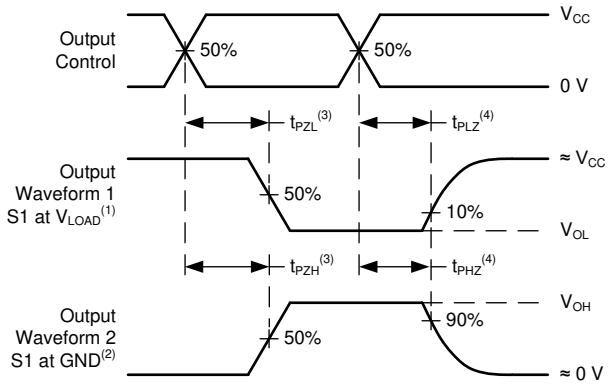
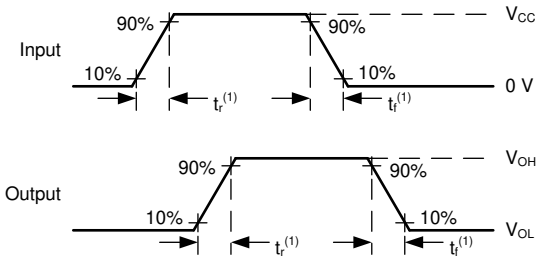
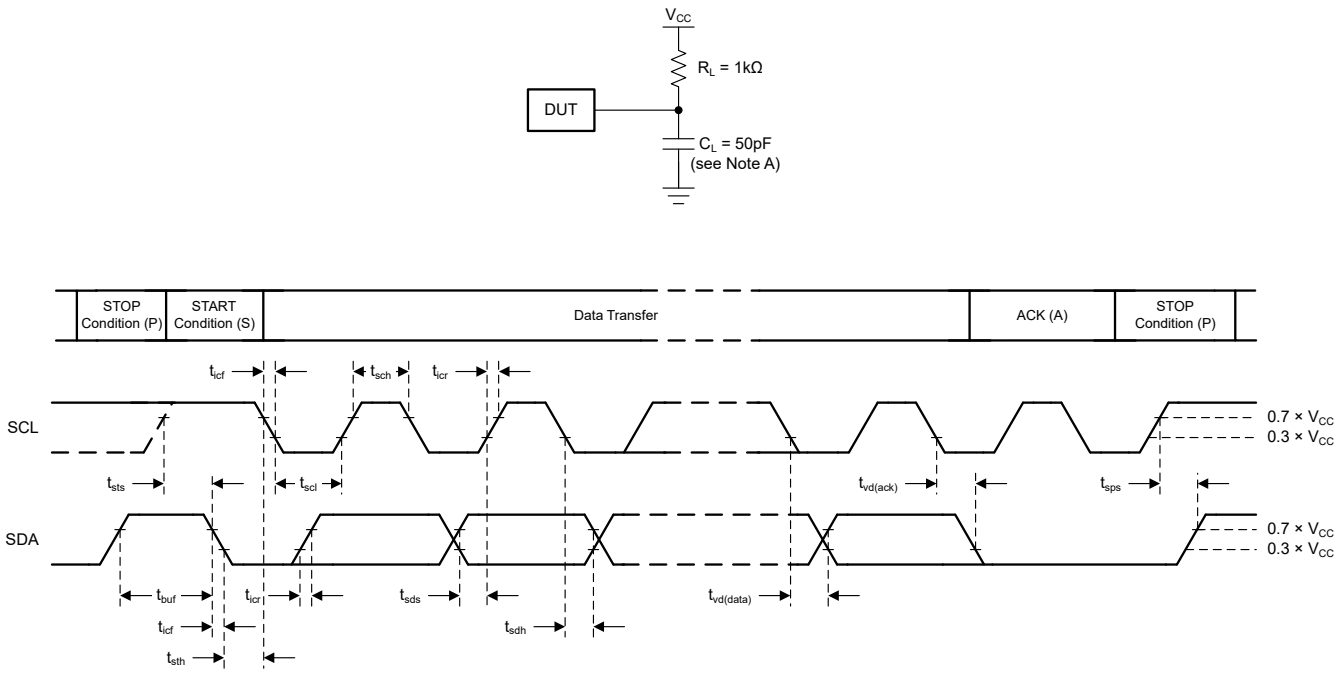


Figure 6-7. Voltage Waveforms Propagation Delays



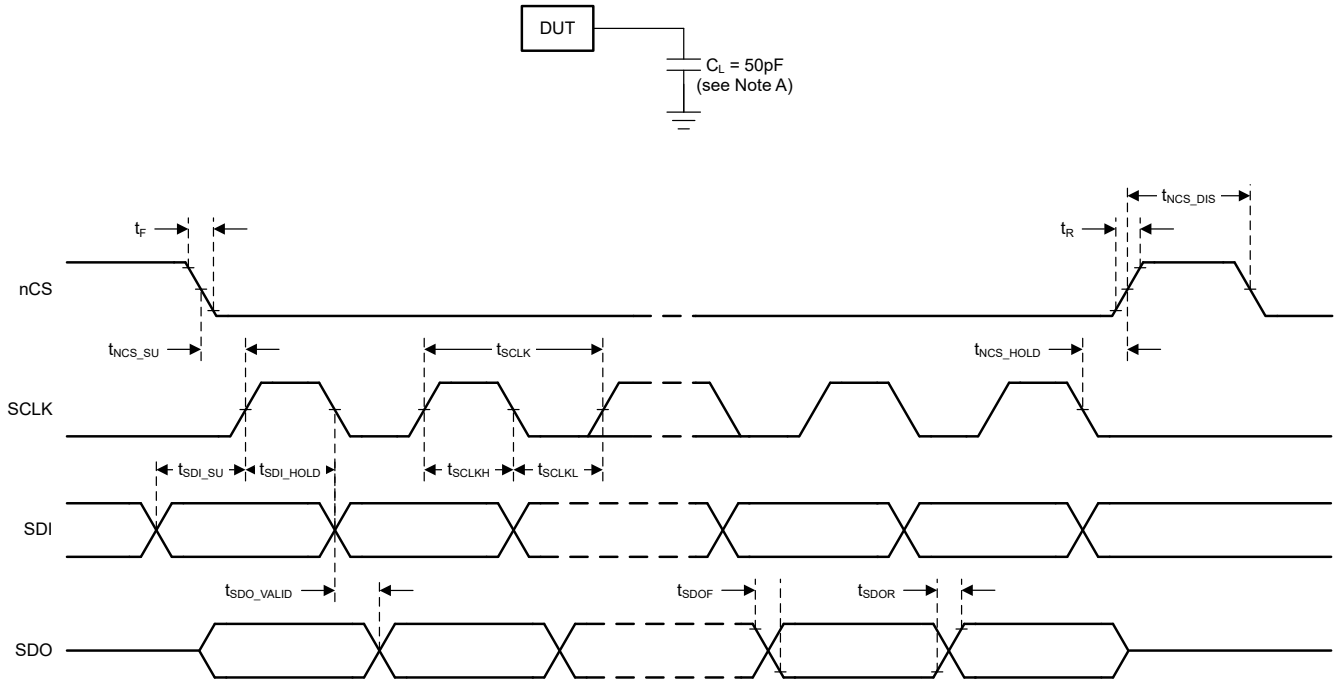
(1) The greater between t_r and t_f is the same as t_t.

Figure 6-9. Voltage Waveforms, Input and Output Transition Times



A. C_L include probe and jig capacitance.

Figure 6-10. I²C Interface Load Circuit and Voltage Waveforms



A. C_L include probe and jig capacitance.

Figure 6-11. SPI Interface Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The TPLD1202 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic , and analog blocks to provide an integrated, compact, low power solution to implement common system functions.

The TPLD1202 has one GPI and nine GPIOs that can be configured as a digital input, digital output, digital input or output, or analog input or output.

The TPLD1202 has a system of interconnects, further referred to as the connection mux, to configure the routing of internal macro-cells and I/O pins. Each connection mux input is hardwired to a specific digital macro-cell output, such as digital I/O, lookup tables, and analog comparator outputs. The connection mux allows each of the digital inputs to only connect to one output so that bus contention does not occur.

The TPLD1202 features the following macro-cells:

- Configurable use logic blocks
  - Two selectable 2-input lookup tables (LUT) or D flip-flop (DFF)/latch
  - One selectable 2-input LUT or Pattern generator (PGEN)
  - Four selectable 3-input LUTs or DFF/latch
  - Four selectable 3-input LUTs or DFF/latch or shift register
  - One selectable 4-input LUT or DFF/latch
- Configurable logic and timing blocks
  - Six 3-input LUT or DFF/latch and/or 8-bit counter (CNT)/delay generator (DLY)
- One programmable deglitch filter (PFLT) or edge detector (EDET)
- One 8-state state machine (SM) or four PWM generators
- Three 8-bit CNT/DLY/finite state machine (FSM)
- One 8-bit CNT/DLY/FSM or watchdog timer (WDT)
- One multi-channel analog comparator (McACMP) with integrated sampling engine
- Voltage reference (VREF)
- Analog temperature sensor (TS)
- Two oscillators (OSC)
  - One selectable 2kHz or 10kHz
  - One fixed 25MHz
- One serial communications macro-cell selectable I^2C or SPI

The InterConnect Studio software environment enables a simple drag-and-drop interface to build custom circuit designs and configure the macro-cells, I/O pins, and interconnections. In addition to circuit creation, InterConnect Studio has the ability to simulate digital and analog functionality to verify designs and provide a typical power consumption estimate. Once circuit designs are finalized, InterConnect Studio can temporarily emulate the design in the non-volatile memory or permanently program the one-time programmable (OTP). The OTP can be locked to prevent readback of its contents.

7.2 Functional Block Diagram

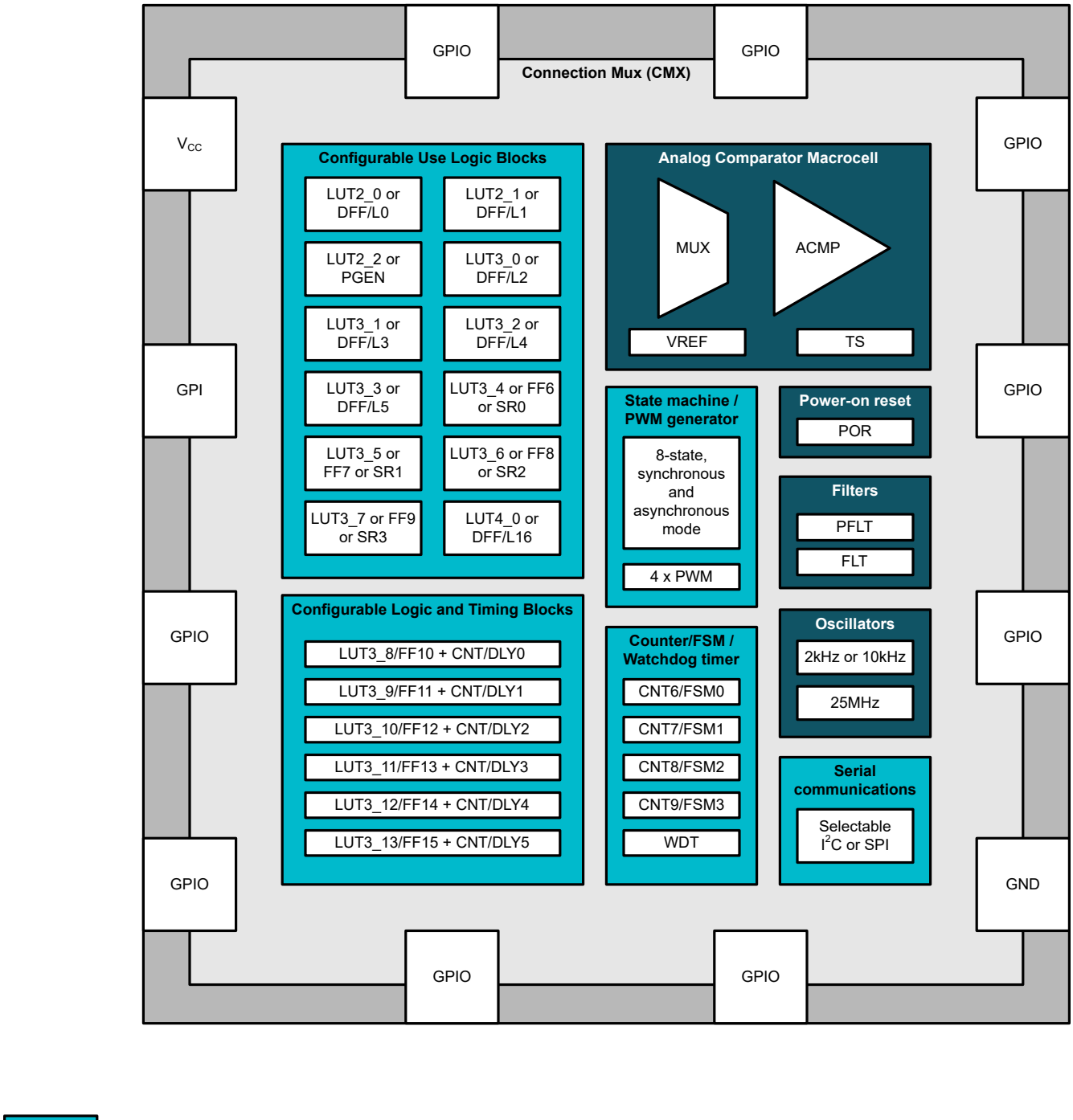


Figure 7-1. TPLD1202 Block Diagram

7.3 Feature Description

7.3.1 I/O Pins

TPLD1202 has one input and nine multifunctional I/O pins. GPIO pins can function as either a user defined input, output, or a special function.

7.3.1.1 Input Modes

The following options are available when configuring pins as an input:

- Digital input without Schmitt-trigger
- Digital input with Schmitt-trigger
- Low-voltage digital input

The low-voltage digital input has lower V_{IH}/V_{IL} specifications than the digital input without Schmitt trigger. This allows for up-translation from any voltage domain lower than V_{CC} that meets the low-voltage digital input V_{IH} and V_{IL} specifications.

In addition to digital input options, several IOs can serve a special function. Two IOs can be used as an external oscillator input.

- IN0: OSC0 external clock
- IO8: OSC1 external clock

Several IOs can also be configured to serve as analog inputs to the internal analog comparator.

- IO5: McACMP IN0
- IO6: McACMP IN1
- IO7: McACMP IN2
- IO8: McACMP IN3
- IO4: External VREF IN

7.3.1.2 Output Modes

The following options are available with programmable drive strength when configuring pins as an output:

- Push-pull output
- Open-drain NMOS output

7.3.1.3 Pull-Up or Pull-Down Resistors

All I/O pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10kΩ, 100kΩ and 1MΩ. The internal resistors can be configured as either pull-up or pull-down. When designing in InterConnect Studio, any pin left unused in a design are configured with a 1MΩ pull-down by default. Furthermore, following a power-on event, all ports are in a Hi-Z state until the power-on reset sequence has completed.

Table 7-1. Pin Configuration Options

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IN0	Pin not used	—	—	Pull-Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down Pull-Up	10k 100k 1M

Table 7-1. Pin Configuration Options (continued)

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IO1, IO2	Pin not used	—	—	Pull-Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
	Digital output	1	Push-pull (1X, 2X) Open-drain NMOS (1X, 4X)	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
IO3, IO4, IO8	Pin not used	—	—	Pull-Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
	Digital output	1	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X) 3-state output (1X, 2X)	Pull-Down Pull-Up	10k 100k 1M
	Digital input/output	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input Analog input	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
		1	Push-pull (1X, 2X) Open-drain NMOS (1X, 2X)		
	Analog input/output	—	Analog input/output	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
IO5, IO6, IO7	Pin not used	—	—	Pull-Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
	Digital output	1	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X)	Pull-Down Pull-Up	10k 100k 1M
	Analog input/output	—	Analog input/output	Floating	—
				Pull-Down Pull-Up	10k 100k 1M

Table 7-1. Pin Configuration Options (continued)

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IO9	Pin not used	—	—	Pull-Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
	Digital output	1	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X) 3-state output (1X, 2X)	Pull-Down Pull-Up	10k 100k 1M
	Digital input/output	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down Pull-Up	10k 100k 1M
		1	Push-pull (1X, 2X) Open-drain NMOS (1X, 2X)		

Note

When using an IO with output-enable (OE) controlled from the CMX configured as a Digital output with 3-state output, TI recommends configuring the input mode to 0b11 (Analog IO or Reserved).

7.3.2 Connection Mux

The connection mux is used to create the internal routing for internal functions of the device once programmed. The registers are programmed from the one-time programmable memory (OTP).

The output of each functional macro-cell within the TPLD1202 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low,” based on the design that is created. Once the 2048 register bits within the TPLD1202 are programmed a fully custom circuit is created.

The connection mux has 53 inputs and 113 outputs. Each of the 53 inputs to the connection mux is hard-wired to a particular source macro-cell, including I/O pins, LUTs, analog comparators, other digital resources and V_{CC} and GND. The input to a digital macro-cell uses a 6-bit register to select one of these 53 input lines.

Table 7-2. Connection Mux Input Table

Connection Mux Input	Connection Mux Input Signal	Mux Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	IN0 OUT	0	0	0	0	0	1
2	IO1 DIN / VIRTUAL IN0	0	0	0	0	1	0
3	IO2 DIN / VIRTUAL IN1	0	0	0	0	1	1
4	IO3 DIN / VIRTUAL IN2	0	0	0	1	0	0
5	IO4 DIN / VIRTUAL IN3	0	0	0	1	0	1
6	IO5 DIN / VIRTUAL IN4	0	0	0	1	1	0
7	IO6 DIN / VIRTUAL IN5	0	0	0	1	1	1
8	IO7 DIN / VIRTUAL IN6	0	0	1	0	0	0
9	IO8 DIN	0	0	1	0	0	1
10	IO9 DIN / VIRTUAL IN7	0	0	1	0	1	0
11	LUT2_0 / DFF OUT	0	0	1	0	1	1
12	LUT2_1 / DFF OUT	0	0	1	1	0	0

Table 7-2. Connection Mux Input Table (continued)

Connection Mux Input	Connection Mux Input Signal	Mux Decode					
		5	4	3	2	1	0
13	LUT2_2 / PGEN OUT	0	0	1	1	0	1
14	LUT3_0 / DFF OUT	0	0	1	1	1	0
15	LUT3_1 / DFF OUT	0	0	1	1	1	1
16	LUT3_2 / DFF OUT	0	1	0	0	0	0
17	LUT3_3 / DFF OUT	0	1	0	0	0	1
18	LUT3_4 / DFF / SR OUT	0	1	0	0	1	0
19	LUT3_5 / DFF / SR OUT	0	1	0	0	1	1
20	LUT3_6 / DFF / SR OUT	0	1	0	1	0	0
21	LUT3_7 / DFF / SR OUT	0	1	0	1	0	1
22	LUT3_8 / LDC (CNT0) OUT	0	1	0	1	1	0
23	LUT3_9 / LDC (CNT1) OUT	0	1	0	1	1	1
24	LUT3_10 / LDC (CNT2) OUT	0	1	1	0	0	0
25	LUT3_11 / LDC (CNT3) OUT	0	1	1	0	0	1
26	LUT3_12 / LDC (CNT4) OUT	0	1	1	0	1	0
27	LUT3_13 / LDC (CNT5) OUT	0	1	1	0	1	1
28	LUT4_0 / DFF OUT	0	1	1	1	0	0
29	PFLT OUT	0	1	1	1	0	1
30	FLT / EDET OUT	0	1	1	1	1	0
31	SM OUT0 or PWM GEN3 OUTP	0	1	1	1	1	1
32	SM OUT1 or PWM GEN3 OUTN	1	0	0	0	0	0
33	SM OUT2 or PWM GEN2 OUTP	1	0	0	0	0	1
34	SM OUT3 or PWM GEN2 OUTN	1	0	0	0	1	0
35	SM OUT4 or PWM GEN1 OUTP	1	0	0	0	1	1
36	SM OUT5 or PWM GEN1 OUTN	1	0	0	1	0	0
37	SM OUT6 or PWM GEN0 OUTP	1	0	0	1	0	1
38	SM OUT7 or PWM GEN0 OUTN	1	0	0	1	1	0
39	McACMP OUT0	1	0	0	1	1	1
40	McACMP OUT1	1	0	1	0	0	0
41	McACMP OUT2	1	0	1	0	0	1
42	McACMP OUT3	1	0	1	0	1	0
43	McACMP DATA RDY	1	0	1	0	1	1
44	OSC0 OUT0	1	0	1	1	0	0
45	OSC0 OUT1	1	0	1	1	0	1
46	OSC1 OUT	1	0	1	1	1	0
47	CNT6/FSM0 OUT	1	0	1	1	1	1
48	CNT7/FSM1 OUT	1	1	0	0	0	0
49	CNT8/FSM2 OUT	1	1	0	0	0	1
50	CNT9/FSM3 or WDT OUT	1	1	0	0	1	0
51	POR OUT	1	1	0	0	1	1
52	Reserved(1)	1	1	0	1	0	0
...	...	...	...	...	...	...	...
62	Reserved(1)	1	1	1	1	1	0

Table 7-2. Connection Mux Input Table (continued)

Connection Mux Input	Connection Mux Input Signal	Mux Decode					
		5	4	3	2	1	0
63	V_{CC}	1	1	1	1	1	1

(1) Reserved options internally connect to VCC.

Table 7-3. Connection Mux Output Table

Connection Mux Output	Connection Mux Output Signal
0	IO1 DOUT
1	IO2 DOUT
2	IO3 DOUT
3	IO3 OE
4	IO4 DOUT
5	IO4 OE
6	IO5 DOUT
7	IO6 DOUT
8	IO7 DOUT
9	IO8 DOUT
10	IO8 OE
11	IO9 DOUT
12	IO9 OE
13	LUT2_0 IN0 / DFF CLK IN
14	LUT2_0 IN1 / DFF D IN
15	LUT2_1 IN0 / DFF CLK IN
16	LUT2_1 IN1 / DFF D IN
17	LUT2_2 IN0 / PGEN CLK IN
18	LUT2_2 IN1 / PGEN RST IN
19	LUT3_0 IN0 / DFF CLK IN
20	LUT3_0 IN1 / DFF D IN
21	LUT3_0 IN2 / DFF RST/SET IN
22	LUT3_1 IN0 / DFF CLK IN
23	LUT3_1 IN1 / DFF D IN
24	LUT3_1 IN2 / DFF RST/SET IN
25	LUT3_2 IN0 / DFF CLK IN
26	LUT3_2 IN1 / DFF D IN
27	LUT3_2 IN2 / DFF RST/SET IN
28	LUT3_3 IN0 / DFF CLK IN
29	LUT3_3 IN1 / DFF D IN
30	LUT3_3 IN2 / DFF RST/SET IN
31	LUT3_4 IN0 / DFF / SR CLK IN
32	LUT3_4 IN1 / DFF / SR D IN
33	LUT3_4 IN2 / DFF / SR RST/SET IN

Table 7-3. Connection Mux Output Table (continued)

Connection Mux Output	Connection Mux Output Signal
34	LUT3_5 IN0 / DFF / SR CLK IN
35	LUT3_5 IN1 / DFF / SR D IN
36	LUT3_5 IN2 / DFF / SR RST/SET IN
37	LUT3_6 IN0 / DFF / SR CLK IN
38	LUT3_6 IN1 / DFF / SR D IN
39	LUT3_6 IN2 / DFF / SR RST/SET IN
40	LUT3_7 IN0 / DFF / SR CLK IN
41	LUT3_7 IN1 / DFF / SR D IN
42	LUT3_7 IN2 / DFF / SR RST/SET IN
43	LUT3_8 IN0 / DFF CLK IN OR LDC (CNT0) IN0
44	LUT3_8 IN1 / DFF D IN OR LDC (CNT0) IN1
45	LUT3_8 IN2 / DFF RST IN OR LDC (CNT0) IN2
46	LUT3_9 IN0 / DFF CLK IN OR LDC (CNT1) IN0
47	LUT3_9 IN1 / DFF D IN OR LDC (CNT1) IN1
48	LUT3_9 IN2 / DFF RST IN OR LDC (CNT1) IN2
49	LUT3_10 IN0 / DFF CLK IN OR LDC (CNT2) IN0
50	LUT3_10 IN1 / DFF D IN OR LDC (CNT2) IN1
51	LUT3_10 IN2 / DFF RST IN OR LDC (CNT2) IN2
52	LUT3_11 IN0 / DFF CLK IN OR LDC (CNT3) IN0
53	LUT3_11 IN1 / DFF D IN OR LDC (CNT3) IN1
54	LUT3_11 IN2 / DFF RST IN OR LDC (CNT3) IN2
55	LUT3_12 IN0 / DFF CLK IN OR LDC (CNT4) IN0
56	LUT3_12 IN1 / DFF D IN OR LDC (CNT4) IN1
57	LUT3_12 IN2 / DFF RST IN OR LDC (CNT4) IN2
58	LUT3_13 IN0 / DFF CLK IN OR LDC (CNT5) IN0
59	LUT3_13 IN1 / DFF D IN OR LDC (CNT5) IN1
60	LUT3_13 IN2 / DFF RST IN OR LDC (CNT5) IN2
61	LUT4_0 IN0 / DFF CLK IN
62	LUT4_0 IN1 / DFF D IN
63	LUT4_0 IN2 / DFF RST/SET IN
64	LUT4_0 IN3
65	PFLT IN
66	FLT / EDET IN
67	SM ST0 EN0
68	SM ST0 EN1
69	SM ST1 EN0
70	SM ST1 EN1
71	SM ST2 EN0

Table 7-3. Connection Mux Output Table (continued)

Connection Mux Output	Connection Mux Output Signal
72	SM ST2 EN1
73	SM ST3 EN0
74	SM ST3 EN1
75	SM ST4 EN0 / PWM GEN3 PWR UP
76	SM ST4 EN1
77	SM ST5 EN0 / PWM GEN2 PWR UP
78	SM ST5 EN1
79	SM ST6 EN0 / PWM GEN1 PWR UP
80	SM ST6 EN1
81	SM ST7 EN0 / PWM GEN0 PWR UP
82	SM ST7 EN1
83	SM CLK
84	SM nRST
85	McACMP ENABLE
86	McACMP nRST
87	OSC0 PWR DOWN
88	OSC1 PWR DOWN
89	CNT6/FSM0 IN
90	CNT6/FSM0 FSM UP
91	CNT6/FSM0 FSM KEEP
92	CNT6/FSM0 Ext. CLK
93	CNT7/FSM1 IN
94	CNT7/FSM1 FSM UP
95	CNT7/FSM1 FSM KEEP
96	CNT7/FSM1 Ext. CLK
97	CNT8/FSM2 IN
98	CNT8/FSM2 FSM UP
99	CNT8/FSM2 FSM KEEP
100	CNT8/FSM2 Ext. CLK
101	CNT9/FSM3 IN / WDT IN
102	CNT9/FSM3 FSM UP / WDT EN
103	CNT9/FSM3 FSM KEEP
104	CNT9/FSM3 Ext. CLK
105	VIR_OUT0
106	VIR_OUT1
107	VIR_OUT2
108	VIR_OUT3
109	VIR_OUT4
110	VIR_OUT5
111	VIR_OUT6
112	VIR_OUT7

7.3.3 Configurable Use Logic blocks

Combinational logic is supported via Lookup Tables (LUTs) within the TPLD1202. Inputs and outputs for the combination function macro-cells are configured from the connection mux with specific logic functions being defined by the state of OTP bits.

The TPLD1202 has twelve configurable use logic blocks (macro-cells) that can serve as a combinational or sequential logic function. In each case, they can serve as a LUT or as another logic or timing function. See the list below for the functions that can be implemented in these logic blocks:

- Two selectable 2-input LUT or D flip-flop or latch (DFF/L)
- One selectable 2-input LUT or pattern generator (PGEN)
- Four selectable 3-input LUT or D flip-flop or latch with reset/set
- Four selectable 3-input LUT or D flip-flop or Shift register (SR)
- One selectable 4-input LUT or D flip-flop or latch with reset/set

7.3.3.1 2-Bit LUT or D Flip-Flop/Latch macro-cell

This configurable use logic block serves as either a 2-bit LUT or as a D flip-flop or latch.

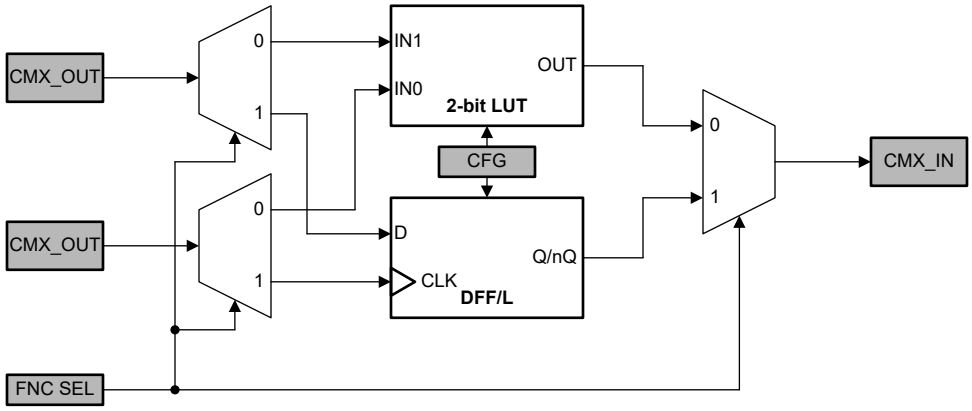


Figure 7-2. 2-bit LUT or DFF/Latch Block Diagram

7.3.3.1.1 2-Bit LUT

When used to implement LUT functions, the 2-bit LUT take in two input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 2-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses a 4-bit register to define the output function.

Table 7-4 shows the truth tables for the 2-bit LUT.

Table 7-4. 2-bit LUT Truth Table

IN1	IN0	OUT
0	0	
0	1	
1	0	
1	1	

7.3.3.1.2 D Flip-Flop/Latch

When used to implement a sequential logic element, the two input signals from the connection mux go to the data (D) and clock (CLK) inputs of the flip-flop or latch, with the output going back to the connection mux. This macro-cell has initial state parameters as well as clock and output polarity parameters that can be configured.

The operation of the D flip-flop/latch follows the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLK) or inverted (nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q does not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q does not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is Low).
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-5 and Table 7-6 show the truth tables for the D flip-flop and D latch, respectively.

Table 7-5. D Flip-Flop Truth Table

CLKPOL	CLK	D	Q	nQ
0	↓	0	Q_0	nQ_0
	↑	0	0	1
	↓	1	Q_0	nQ_0
	↑	1	1	0
1	↓	0	0	1
	↑	0	Q_0	nQ_0
	↓	1	1	0
	↑	1	Q_0	nQ_0

Table 7-6. D Latch Truth Table

CLKPOL	CLK	D	Q	nQ
0	0	0	0	1
	1	0	Q_0	nQ_0
	0	1	1	0
	1	1	Q_0	nQ_0
1	0	0	Q_0	nQ_0
	1	0	0	1
	0	1	Q_0	nQ_0
	1	1	1	0

7.3.3.2 2-Bit LUT or Pattern Generator macro-cell

This configurable use logic block serves as either a 2-bit LUT or as a Pattern generator.

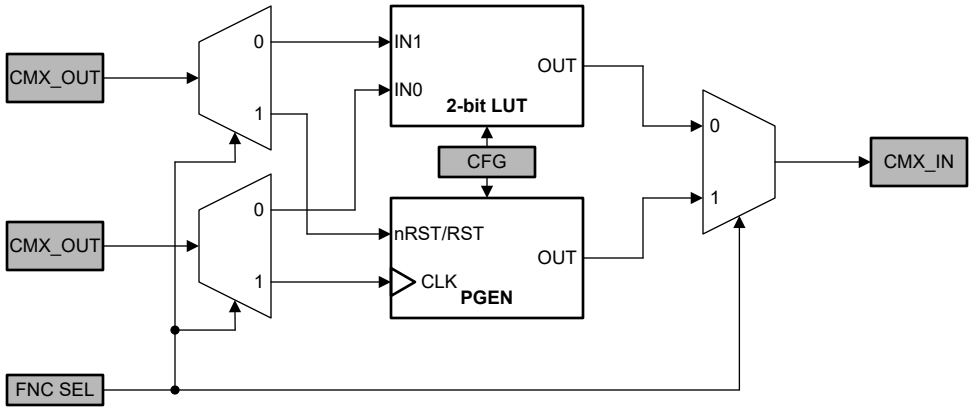


Figure 7-3. 2-bit LUT or Pattern Generator Block Diagram

7.3.3.2.1 2-Bit LUT

When used to implement LUT functions, the 2-bit LUT take in two input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 2-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses a 4-bit register to define the output function.

Table 7-7 shows the truth tables for the 2-bit LUT.

Table 7-7. 2-bit LUT Truth Table

IN1	IN0	OUT
0	0	
0	1	
1	0	
1	1	

7.3.3.2.2 Pattern Generator

When configured as a Pattern generator, the two input signals from the connect mux go to the reset (nRST/RST) and clock (CLK) inputs of the pattern generator, with the output going back to the connection mux. This macro-cell has pattern size, bit pattern, and reset signal polarity parameters that can be configured to generate up to a 16-bit pattern that is clocked out continually on the rising edge of the CLK input as long as the macro-cell is not in reset. While in reset, the macro-cell continually outputs the first bit of the programmed bit pattern.

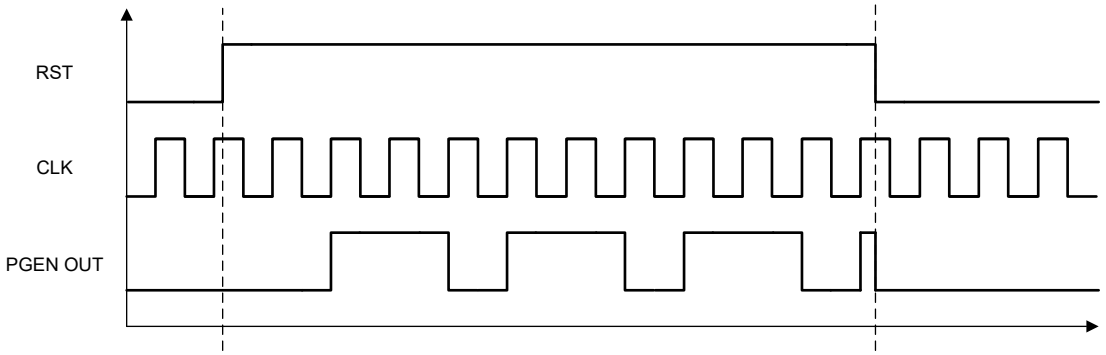


Figure 7-4. Pattern Generator Output Timing Diagram Example (SIZE = 3, PATTERN = 011, Low level RST)

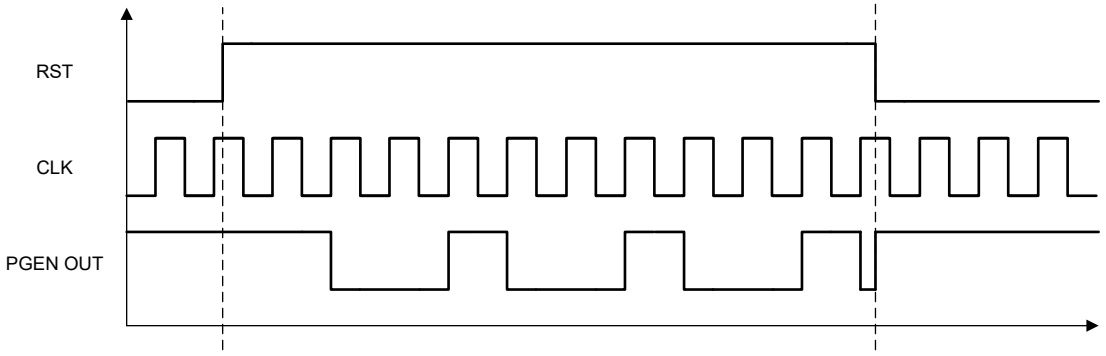


Figure 7-5. Pattern Generator Output Timing Diagram Example (SIZE = 3, PATTERN = 100, Low level RST)

The output pattern can be updated in-system using the User Registers. It is recommended to put the pattern generator in a reset state when updating the pattern registers to verify glitch-free loading of the data.

7.3.3.3 3-Bit LUT or D Flip-Flop/Latch With Reset/Set Macro-Cell

This configurable use logic block serves as either a 3-bit LUT or as a D flip-flop or latch with a reset or set.

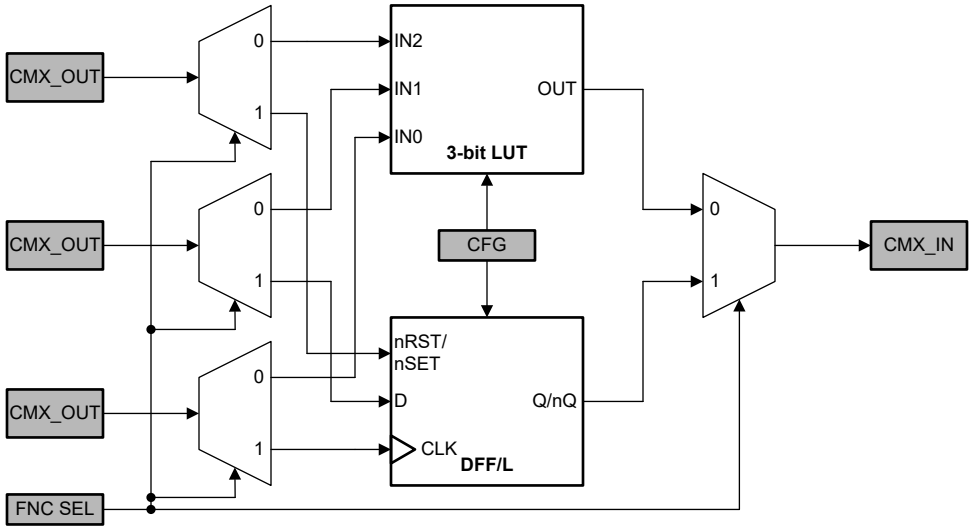


Figure 7-6. 3-bit LUT or DFF/Latch with nRST/nSET Block Diagram

7.3.3.3.1 3-bit LUT

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses an 8-bit register to define the output function.

Table 7-8 shows truth tables for the 3-bit LUT.

Table 7-8. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

7.3.3.3.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has user-configurable initial state, clock polarity, reset/set polarity, output stage select, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLK) or inverted (nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q does not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q does not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is Low).
- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- These DFF/Latches have the option to further isolate the output from the input with the use of a second DFF/Latch sampling on the falling edge of CLK, or rising edge of nCLK, by enabling the "Dual Stage DFF" option.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-9 and Table 7-10 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

Table 7-9. D Flip-Flop with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	Q_0	nQ_0
			↑	0	0	1
			↓	1	Q_0	nQ_0
			↑	1	1	0

Table 7-9. D Flip-Flop with nRST/nSET Truth Table (continued)

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	0	1
			↑	0	Q_0	nQ_0
			↓	1	1	0
			↑	1	Q_0	nQ_0

Table 7-10. D Latch with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		0	0	0	1
			1	0	Q_0	nQ_0
			0	1	1	0
			1	1	Q_0	nQ_0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		0	0	Q_0	nQ_0
			1	0	0	1
			0	1	Q_0	nQ_0
			1	1	1	0

7.3.3.4 3-Bit LUT or D Flip-Flop/Latch or Shift Register macro-cell

This configurable use logic block can serve as either a 3-bit LUT or as a D flip-flop or latch with a reset or set or an 8-bit Shift register.

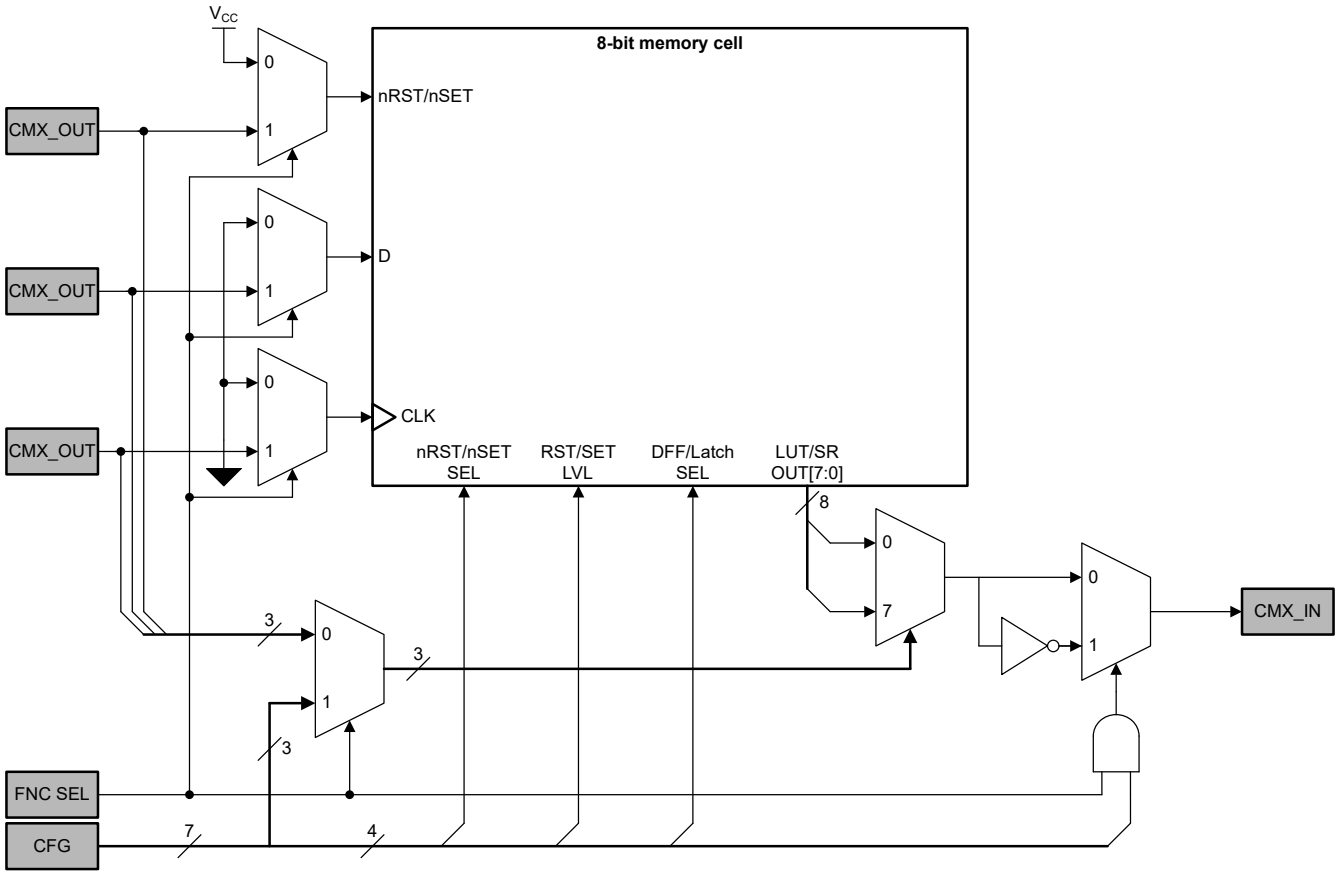


Figure 7-7. 3-bit LUT or DFF/Latch with nRST/nSET or 8-bit SISO Shift Register Block Diagram

7.3.3.4.1 3-bit LUT

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses an 8-bit register to define the output function.

Table 7-11 shows truth tables for the 3-bit LUT.

Table 7-11. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

7.3.3.4.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back

to the connection mux. This macro-cell has user-configurable initial state, reset/set polarity, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-12 and Table 7-13 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

Table 7-12. D Flip-Flop with nRST/nSET truth table

nRST	nSET	CLK	D	Q	nQ
0	—	X	X	0	1
—	0	X	X	1	0
1	1	↓	0	Q_0	nQ_0
		↑	0	0	1
		↓	1	Q_0	nQ_0
		↑	1	1	0

Table 7-13. D Latch with nRST/nSET truth table

nRST	nSET	CLK	D	Q	nQ
0	—	X	X	0	1
—	0	X	X	1	0
1	1	0	0	0	1
		1	0	Q_0	nQ_0
		0	1	1	0
		1	1	Q_0	nQ_0

7.3.3.4.3 8-bit Shift Register

When used to implement a shift register, users can configure the initial state, reset/set polarity, output polarity, and register length. The register length can be set to a minimum of 2 and a maximum of 8.

Figure 7-8 shows an example of how the Shift register macro-cell operates.

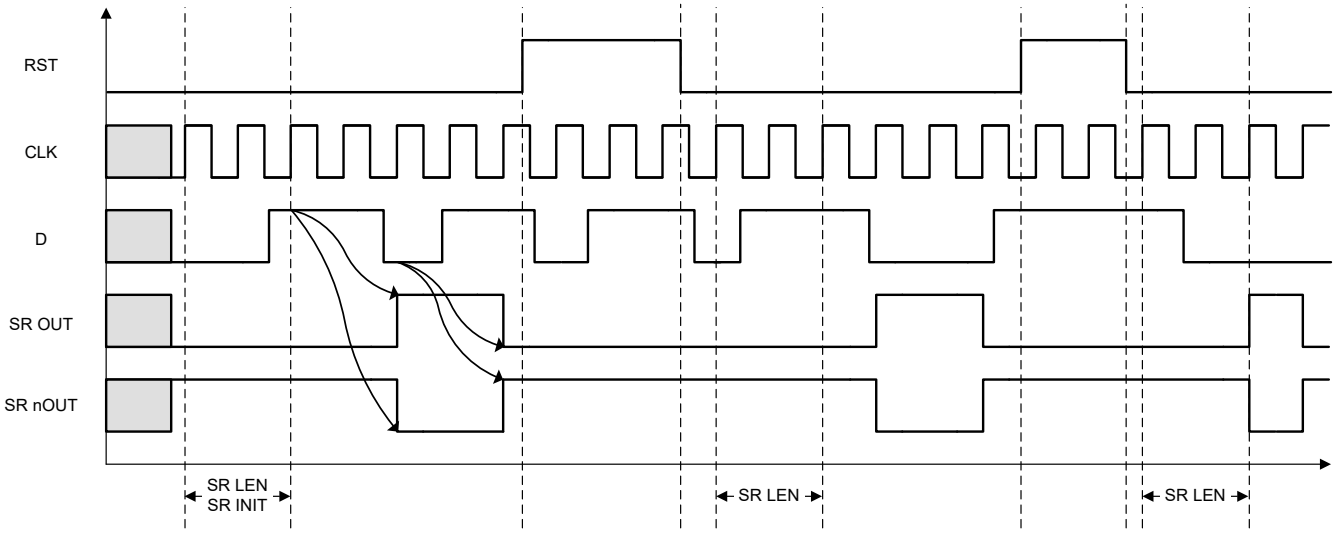


Figure 7-8. Shift Register Output Timing Diagram Example (INIT STATE = 00, REG LENGTH = 2, High level RST)

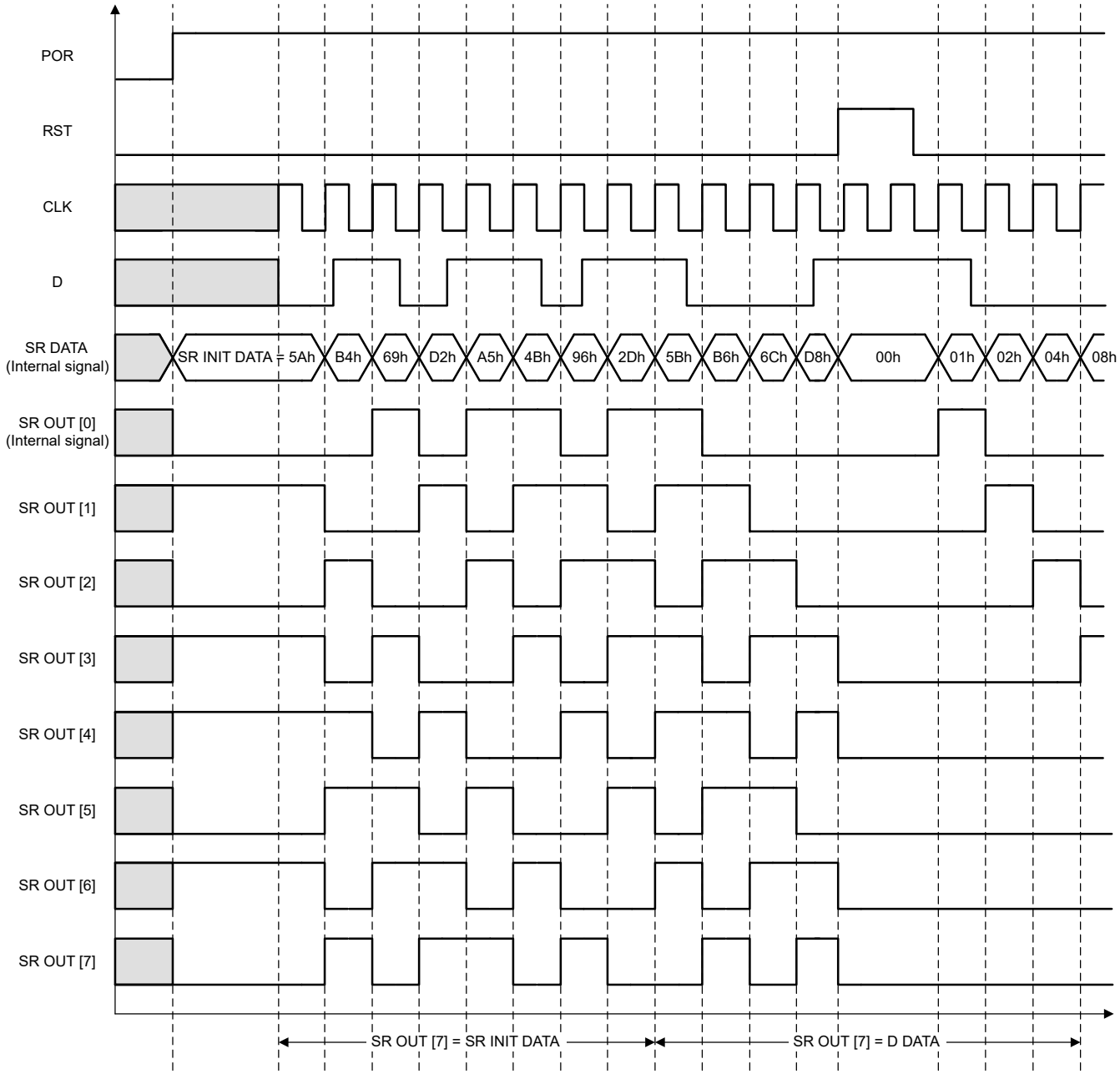


Figure 7-9. Shift Register Output Timing Diagram Example (INIT STATE = 5Ah, High level RST)

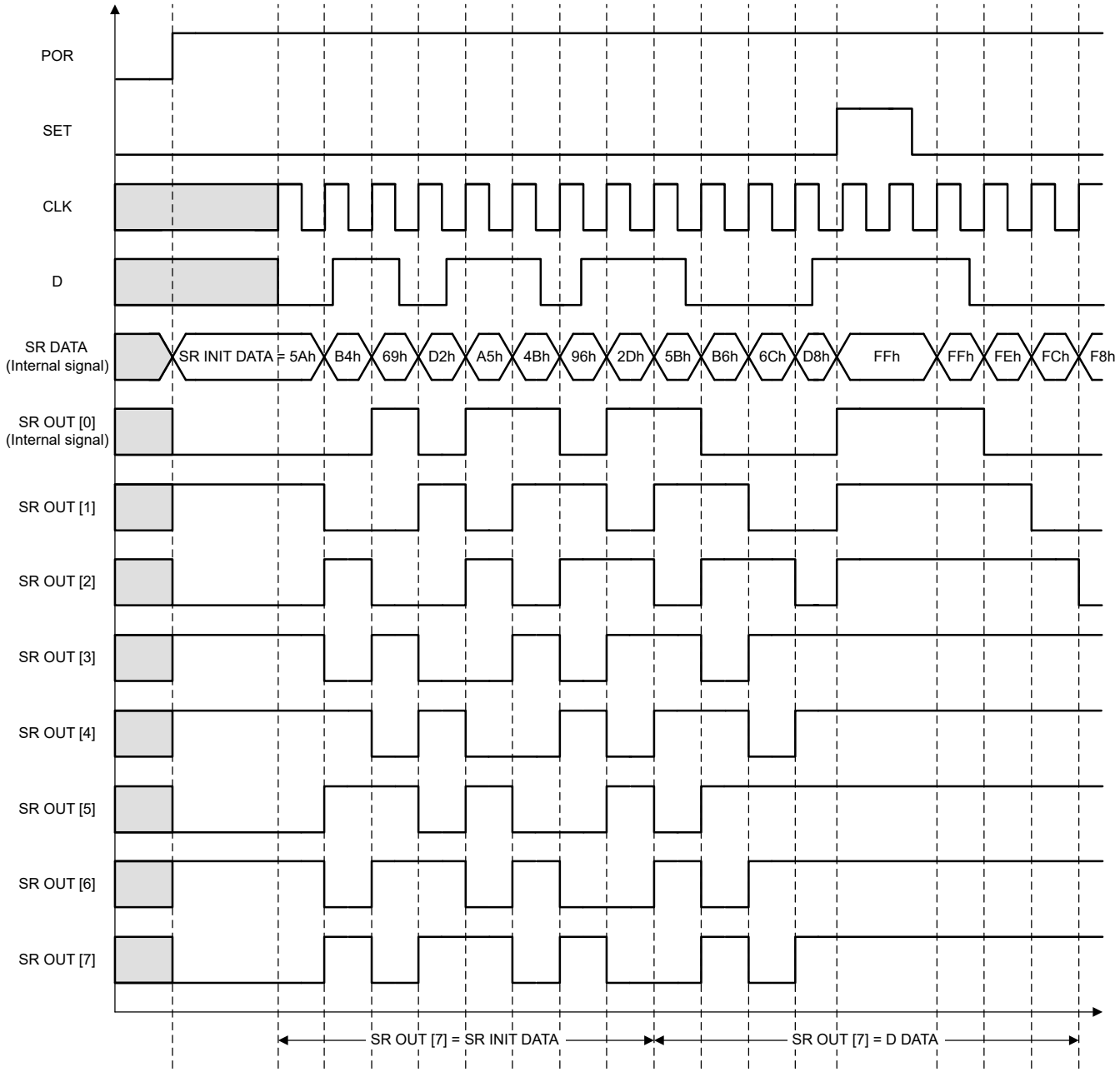


Figure 7-10. Shift Register Output Timing Diagram Example (INIT STATE = 5Ah, High level SET)

7.3.3.5 4-Bit LUT or D Flip-Flop/Latch with Reset/Set Macro-Cell

This configurable use logic block can serve as either a 4-bit LUT or as a D flip-flop or latch with a reset or set.

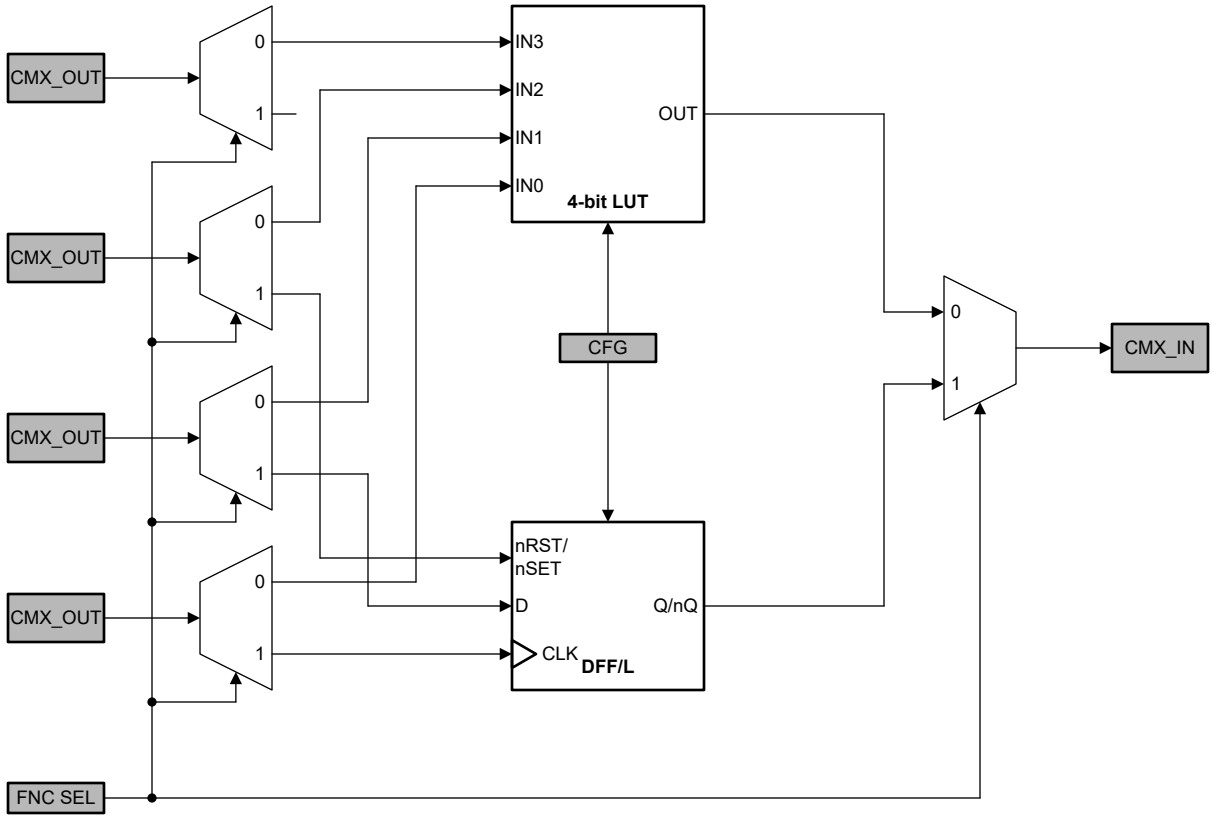


Figure 7-11. 4-bit LUT or DFF/Latch Block Diagram

7.3.3.5.1 4-bit LUT

When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection mux and produces a single output, which goes back into the connection mux. This LUT can be configured to any 4-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, this macro-cell uses a 16-bit register to define the output function.

Table 7-14 shows truth tables for the 4-bit LUT.

Table 7-14. 4-bit LUT Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

7.3.3.5.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has user-configurable initial state, clock polarity, reset/set polarity, output stage select, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLK) or inverted (nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q does not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q does not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is Low).
- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- These DFF/Latches have the option to further isolate the output from the input with the use of a second DFF/Latch sampling on the falling edge of CLK, or rising edge of nCLK, by enabling the "Dual Stage DFF" option.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-15 and Table 7-16 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

Table 7-15. D Flip-Flop with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	Q_0	nQ_0
			↑	0	0	1
			↓	1	Q_0	nQ_0
			↑	1	1	0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	0	1
			↑	0	Q_0	nQ_0
			↓	1	1	0
			↑	1	Q_0	nQ_0

Table 7-16. D Latch with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		0	0	0	1
			1	0	Q_0	nQ_0
			0	1	1	0
			1	1	Q_0	nQ_0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		0	0	Q_0	nQ_0
			1	0	0	1
			0	1	Q_0	nQ_0
			1	1	1	0

7.3.4 Configurable Logic and Timing Blocks

The TPLD1202 has six configurable logic and timing blocks (macro-cells) that can serve as a combinational or sequential logic function. The configurable logic and timing blocks can serve as a 3-bit LUT, D flip-flop with nRST/nSET, or an 8-bit Counter/Delay generator. These macro-cells also have the option to combine the previous functions, with a LUT/DFF output connected to the CNT/DLY input or a CNT/DLY output connected to any LUT/DFF input.

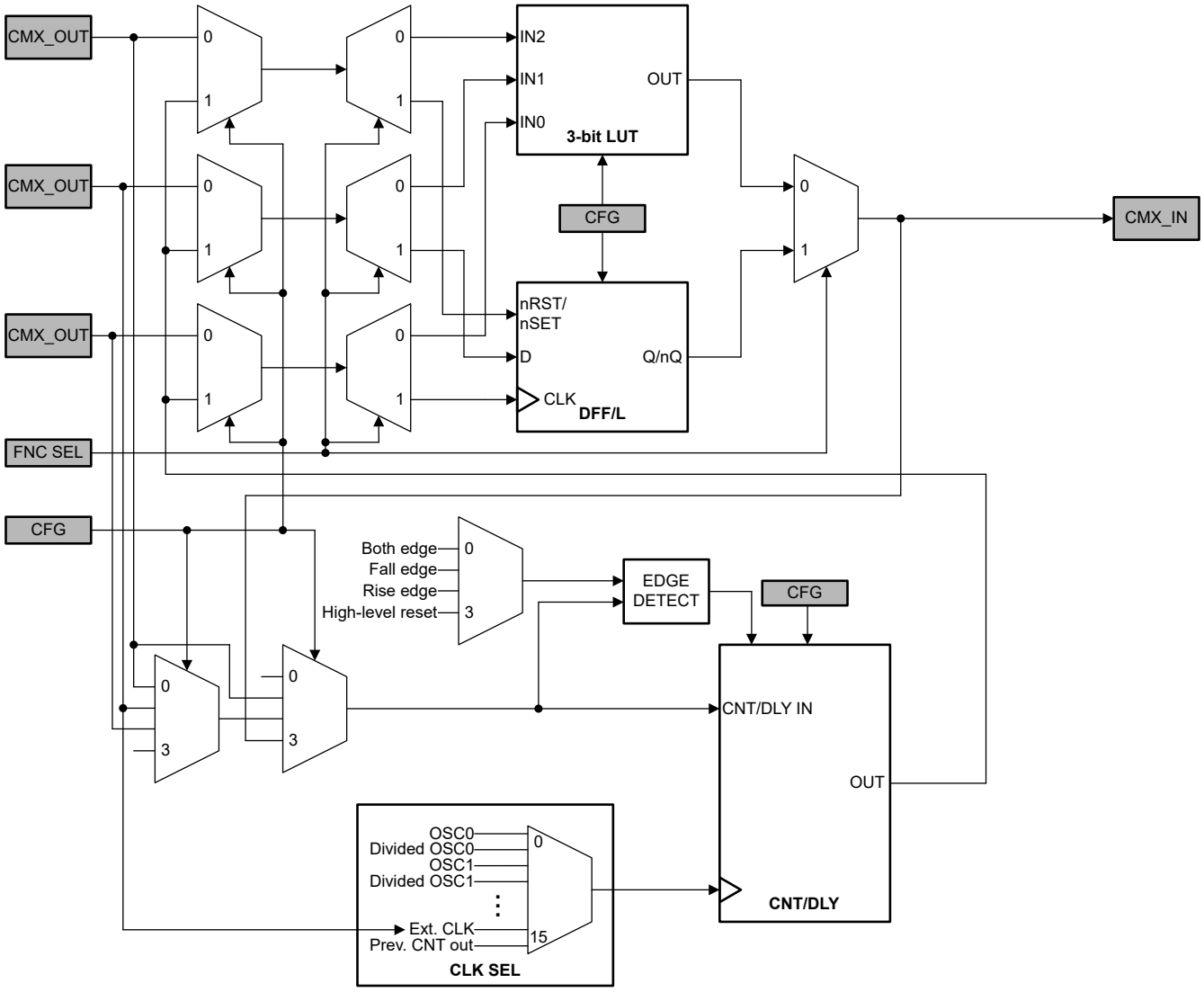


Figure 7-12. LUT/DFF + CNT/DLY Block Diagram

Table 7-17. LUT/DFF + CNT/DLY Connection Options

LDC_FS (1 bit)	LDC_CMX_IN_SEL (2 bits)	LDC_CMX_MODE (2 bits)	LDC IN0	LDC IN1	LDC IN2	LDC OUT
0	XX	00	LUT A	LUT B	LUT C	LUT OUT
1	XX	00	DFF CLK	DFF D	DFF RST	DFF OUT
X	XX	01	Unused	CNT Ext. CLK	CNT IN	CNT OUT
0	00	10	LUT A	LUT B	CNT IN	LUT OUT
0	01	10	LUT A	CNT IN	LUT C	LUT OUT
0	10	10	CNT IN	LUT B	LUT C	LUT OUT
1	00	10	DFF CLK	DFF D	CNT IN	DFF OUT
1	01	10	DFF CLK	CNT IN	DFF RST	DFF OUT
1	10	10	CNT IN	DFF D	DFF RST	DFF OUT
0	XX	11	LUT A	LUT B	LUT C	CNT OUT

Table 7-17. LUT/DFF + CNT/DLY Connection Options (continued)

LDC_FS (1 bit)	LDC_CMX_IN_SEL (2 bits)	LDC_CMX_MODE (2 bits)	LDC IN0	LDC IN1	LDC IN2	LDC OUT
1	XX	11	DFF CLK	DFF D	DFF RST	CNT OUT

7.3.4.1 3-bit LUT

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection mux and produce a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions (AND, NAND, OR, NOR, XOR, XNOR).

When programmed for a LUT function, each macro-cell uses an 8-bit register to define the output function.

Table 7-18 shows truth tables for the 3-bit LUT.

Table 7-18. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

7.3.4.2 D Flip-Flop/Latch with Reset/Set

When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has user-configurable initial state, clock polarity, reset/set polarity, output stage select, and output polarity parameters.

The operation of the D flip-flop/latch follows the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLK) or inverted (nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q does not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q does not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains the previous value (input D has no effect on the output, when CLK is Low).
- These DFF/Latches have an option for both an active-low and active-high reset/set:
  - nRST: If High, then the DFF/Latch is in normal operation. If Low, then Q is reset to 0.
  - RST: If Low, then the DFF/Latch is in normal operation. If High, then Q is reset to 0.
  - nSET: If High, then the DFF/Latch is in normal operation. If Low, then Q is set to 1.
  - SET: If Low, then the DFF/Latch is in normal operation. If High, then Q is set to 1.
- If reset/set is not desired, users can set the polarity to active-low and connect this input to V_{CC} or a constant High source.
- These DFF/Latches have the option to further isolate the output from the input with the use of a second DFF/Latch sampling on the falling edge of CLK, or rising edge of nCLK, by enabling the "Dual Stage DFF" option.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-19 and Table 7-20 show the truth tables for the D flip-flop and D latch with an active-low reset/set, respectively.

Table 7-19. D Flip-Flop with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	Q_0	nQ_0
			↑	0	0	1
			↓	1	Q_0	nQ_0
			↑	1	1	0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	0	1
			↑	0	Q_0	nQ_0
			↓	1	1	0
			↑	1	Q_0	nQ_0

Table 7-20. D Latch with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		0	0	0	1
			1	0	Q_0	nQ_0
			0	1	1	0
			1	1	Q_0	nQ_0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		0	0	Q_0	nQ_0
			1	0	0	1
			0	1	Q_0	nQ_0
			1	1	1	0

7.3.4.3 8-Bit Counters/Delay Generators (CNT/DLY)

The counters/delay generators are 8-bit, supporting counter data values from 1 to 255. For flexibility, the clock source for each of these macro-cells can be configured as the internal oscillator (OSC0 or OSC1), a divided clock derived from an oscillator (OSC0/8, /12, /24, /64, /512, /4096 or OSC1/4, /8, /64, /512), or an external clock source coming from the connection mux. There is also the option to chain from the output of the previous CNT/DLY macro-cell to implement longer counter/delay circuits. Note that the counter/delay macro-cell is rising edge triggered, that is the counter increments/decrements on rising clock edges.

As a counter/delay (CNT/DLY) macro-cell, users can select from the following modes: delay, one-shot, frequency detector, counter, edge detector, delayed edge detector.

7.3.4.3.1 Delay Mode

When configured as a Delay generator (DLY), this macro-cell delays the input based on counter DATA and CLK input frequency and postpones rising and/or falling edges. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which to delay is selected by the Edge select parameter and can be configured as:

- Rising: only delay on rising edges of IN.
- Falling: only delay on falling edges of IN.
- Both: delay on both rising and falling edges of IN.

For delay applications, TI recommends to use larger counter data values for less error. If an input pulse width is shorter than the specified delay time, the pulse is filtered out. This feature can be useful for deglitching.

If the on-chip oscillator is used, a delay error or offset is introduced depending on whether the OSC is set to "forced power on" or "auto power on". An additional 2 clock cycles are included in the delay calculation for clock synchronization.

The delay time is calculated by:

$$\mathrm{DELAY} = \left[\mathrm{DATA} + \left(t_{d\_er} \text{ or } t_{d\_os}\right) + 2\right] \div f_{CLK} \quad (1)$$

When the OSC is set to "auto power on" and DLY macro-cells are triggered subsequently before the previous output is present, the OSC continues to clock and the DLY begins on the next rising edge. Thus, the subsequent delays can be calculated as if the OSC are set to "forced power on".

Figure 7-13 shows an example of the Delay macro-cell operation set to both edge delay and data = 1.

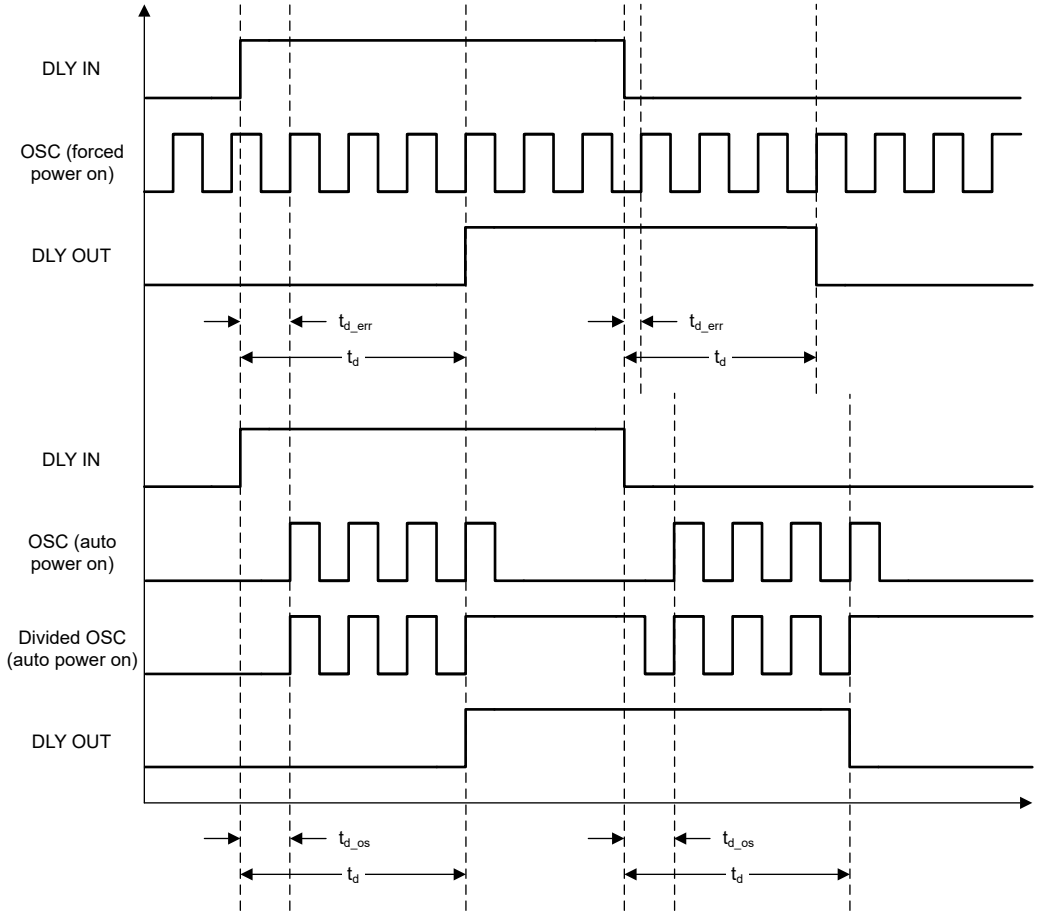


Figure 7-13. Delay Output Timing Example (Both Edge Delay and DATA = 1)

Figure 7-14 shows an example timing of Delay macro-cells with respect to the edge selected and data = 3.

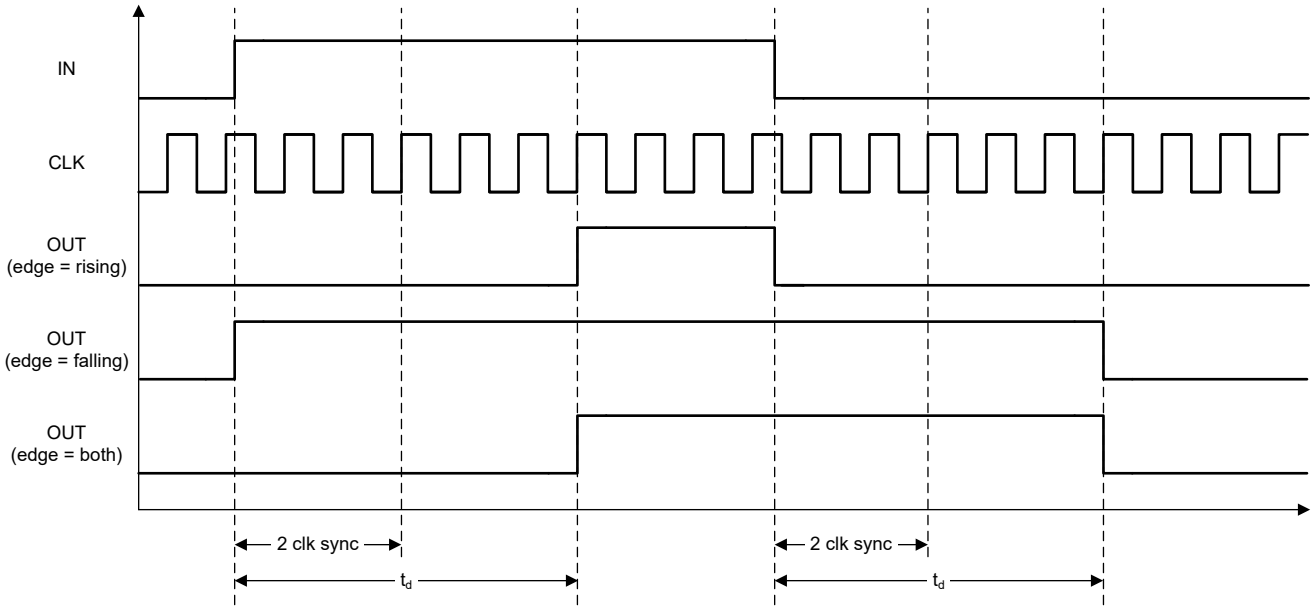


Figure 7-14. Delay Output Timing Example (DATA = 3)

7.3.4.3.2 Reset Counter Mode

When configured as a Counter (CNT) and a valid edge appears on the IN input, this macro-cells resets the internal counter to 0 and begins counting down from DATA on the next rising clock edge. Then, the macro-cell outputs a pulse for the duration of one CLK period when the count reaches 0 and wrap around to the value in DATA. The counter continually operates until another reset is received. The edge on which the Counter is reset is determined by the Edge select parameter and can be configured as:

- Rising: only rising edges of IN reset the counter.
- Falling: only falling edges of IN reset the counter.
- Both: both rising and falling edges of IN reset the counter.
- High Level Reset: the counter is reset to 0 whenever IN is High; after reset, the counter output stays Low until the next rising CLK edge, then operates normally.

The counter time is calculated by:

$$\text{COUNT} = [\text{DATA} + 1] \div f_{\text{CLK}} \quad (2)$$

After a reset, an additional 2 clock cycles is added for clock synchronization with an option to bypass. Note, bypassing the clock synchronization can result in the counter resetting to an unknown value.

Note

Counters are initialized with DATA = 0 after POR.

Figure 7-15 and Figure 7-16 show examples of Counter output timing diagrams with respect to the Edge select parameter with DATA = 1 and DATA = 3, respectively.

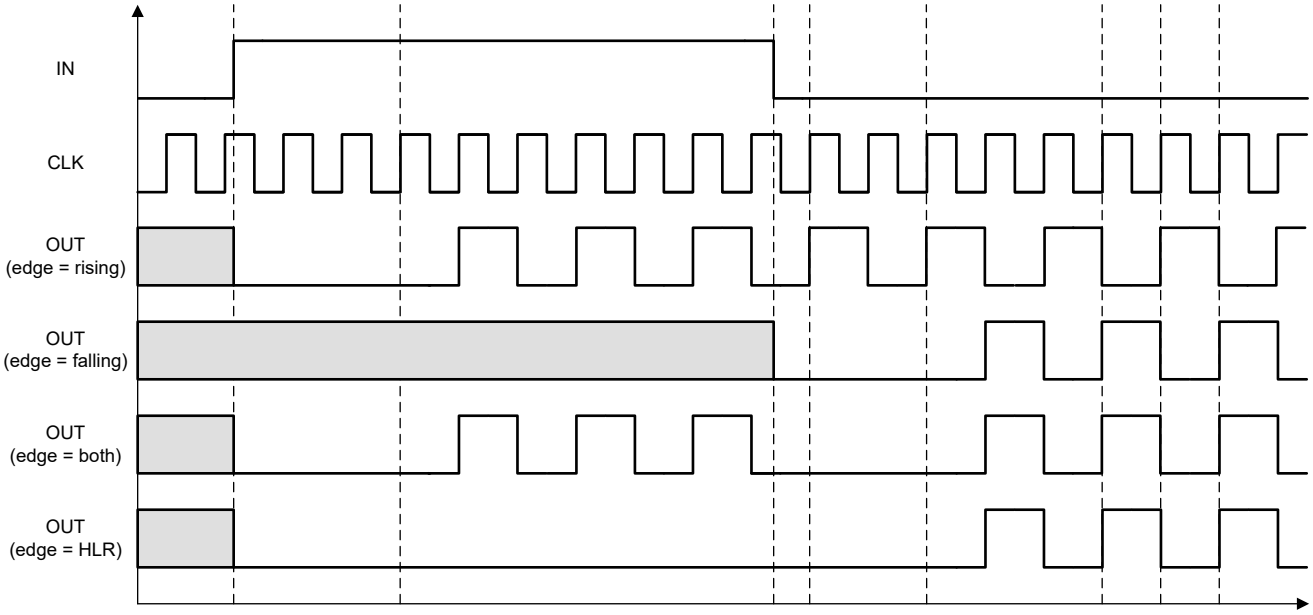


Figure 7-15. Counter Output Timing Example (DATA = 1)

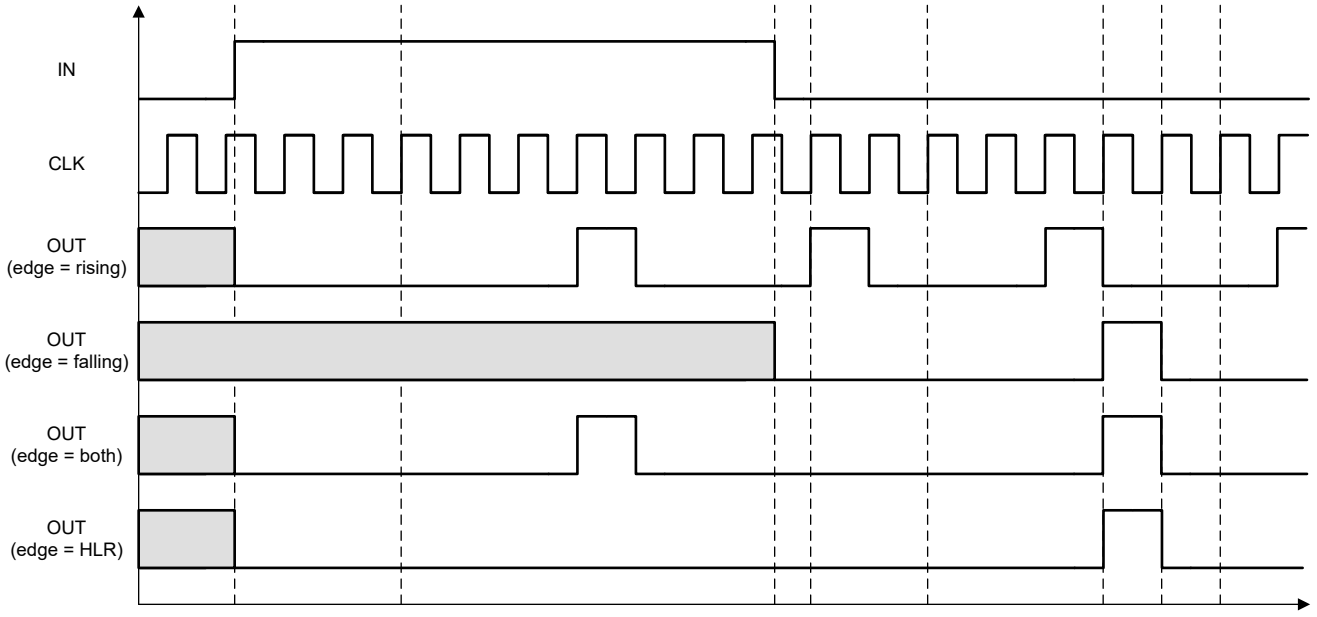


Figure 7-16. Counter Output Timing Example (DATA = 3)

Figure 7-17 shows an example of how the Counter macro-cell operates when the IN signal is shorter than the counter length (shown when edge select parameter is set to "both").

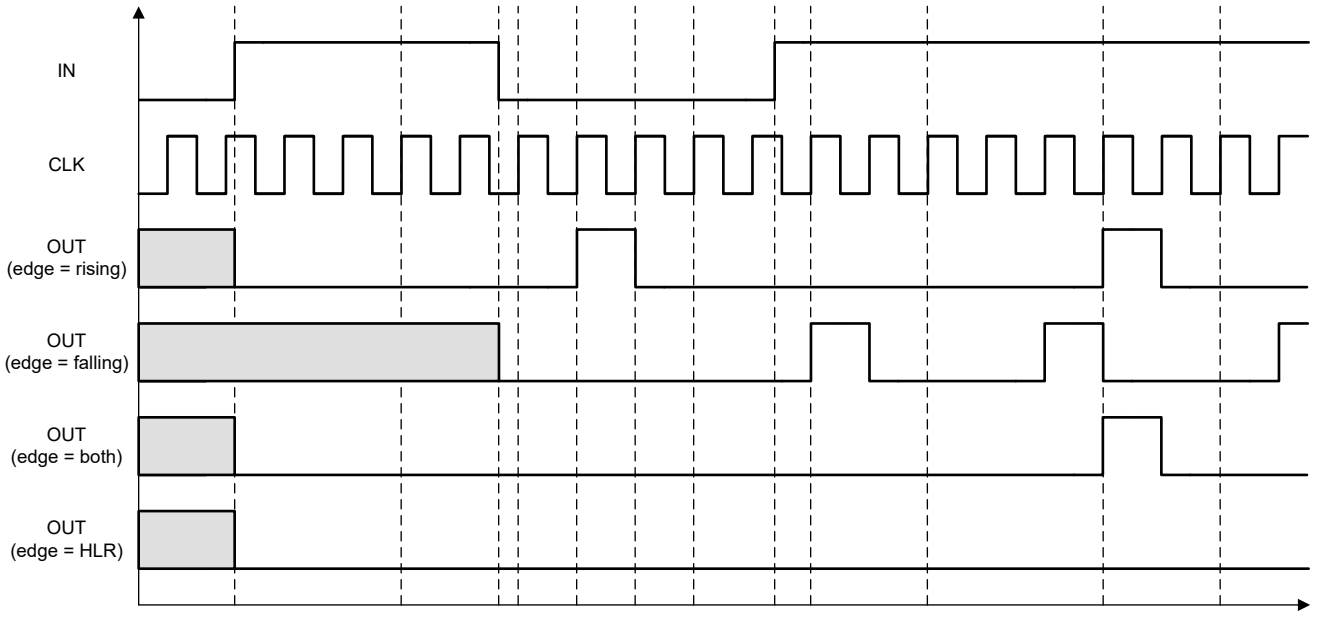


Figure 7-17. Counter Output Timing Example with RST < DATA (DATA = 3)

7.3.4.3.3 One-Shot Mode

When configured as a One-shot, this macro-cell generates a pulse that begins when a valid edge appears on the IN input, which triggers the counter to begin counting down from DATA following two CLK cycles, and the pulse ends once the counter reaches 0 and DATA is subsequently reloaded into the counter and waiting for the next trigger. Triggers received while the counter is decrementing are ignored. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which the One-shot is reset is determined by the Edge select parameter and can be configured as:

- **Rising**: only rising edges of IN reset the one-shot.

- **Falling**: only falling edges of IN reset the one-shot.
- **Both**: both rising and falling edges of IN reset the one-shot.

An additional 2 clock cycles are included in the one-shot pulse width calculation for clock synchronization.

$$\text{ONESHOT} = \left[\text{DATA} + \left(t_{d\_er} \text{ or } t_{d\_os}\right) + 1\right] \div f_{CLK} \quad (3)$$

Figure 7-18 shows an example of how the One-shot macro-cell operates with respect to the Edge select parameter.

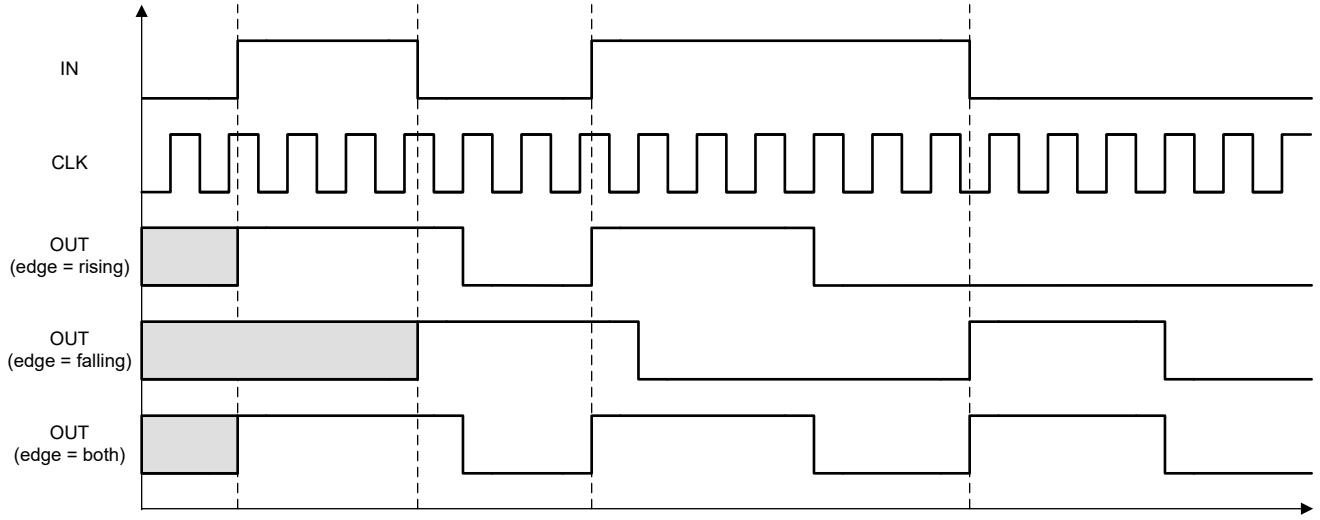


Figure 7-18. One-shot output timing example (DATA = 2)

7.3.4.3.4 Frequency Detector Mode

When configured as a Frequency detector (FDET), this macro-cell indicates whether the input signal is faster or slower than the period specified by DATA. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which the Frequency detector is reset is determined by the Edge select parameter and can be configured as:

- **Rising**: rising edges of IN trigger and reset the frequency detector.
- **Falling**: falling edges of IN trigger and reset the frequency detector.
- **Both**: rising edges of IN triggers the frequency detector to begin counting and falling edges of IN reset the frequency detector.

Upon receiving a trigger, an additional 2 clock cycles is used to synchronize IN and the counter with CLK, then the counter begins decrementing from DATA on the following rising edge of CLK. For proper operation of the FDET macro-cell, TI recommends using a minimum DATA of 3.

If the internal counter reaches 0, the FDET macro-cell outputs a Low signal, indicating the input frequency is slower than DATA. Otherwise, if the counter is interrupted with a reset before reaching 0, the FDET macro-cell outputs a High signal, indicating a faster signal on IN.

Figure 7-19 shows an example of how the FDET macro-cell operates with respect to the Edge select parameter.

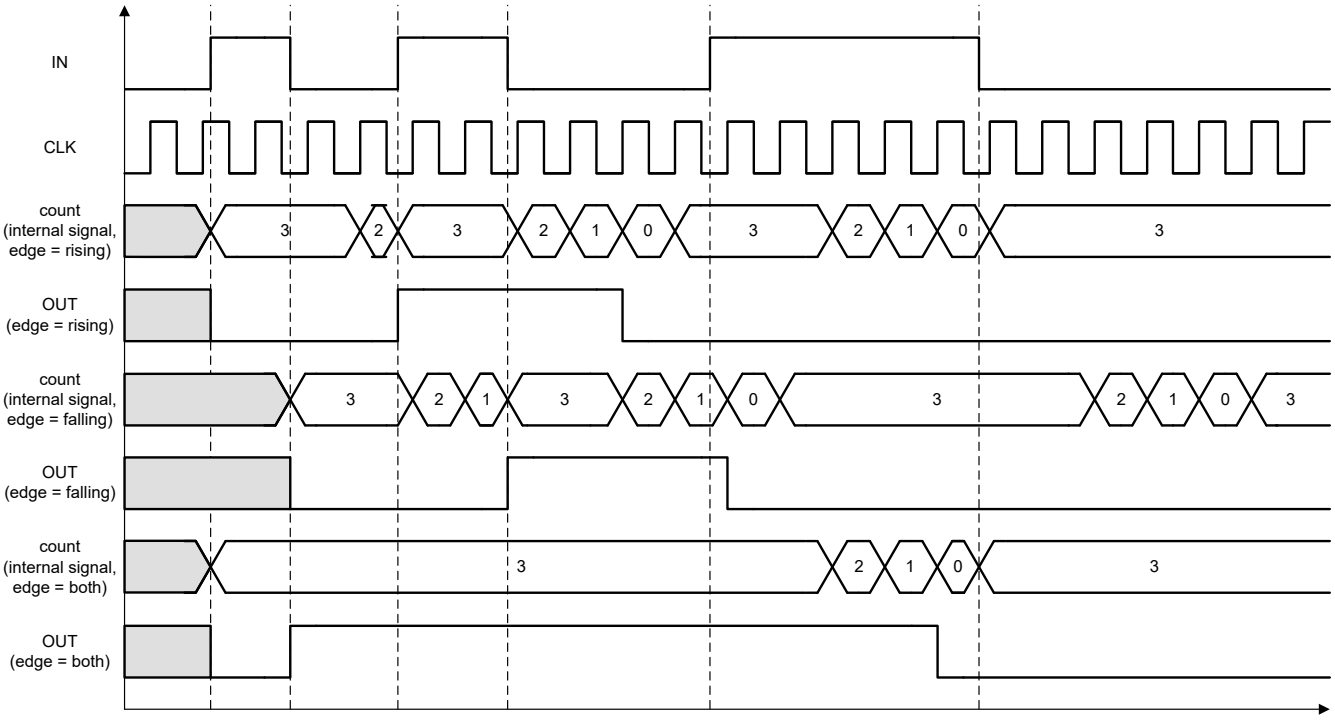


Figure 7-19. Frequency detector output timing example (DATA = 4)

7.3.4.3.5 Edge Detector Mode

When configured as an Edge detector (EDET), this macro-cell generates a pulse of approximately 20ns width when a valid edge is detected. The edge on which the Edge detector generates a pulse is determined by the Edge select parameter and can be configured as:

- **Rising**: only rising edges of IN generate a pulse.
- **Falling**: only falling edges of IN generate a pulse.
- **Both**: both rising and falling edges of IN generate a pulse.

Figure 7-20 shows an example of how the EDET macro-cell operates with respect to the Edge select parameter.

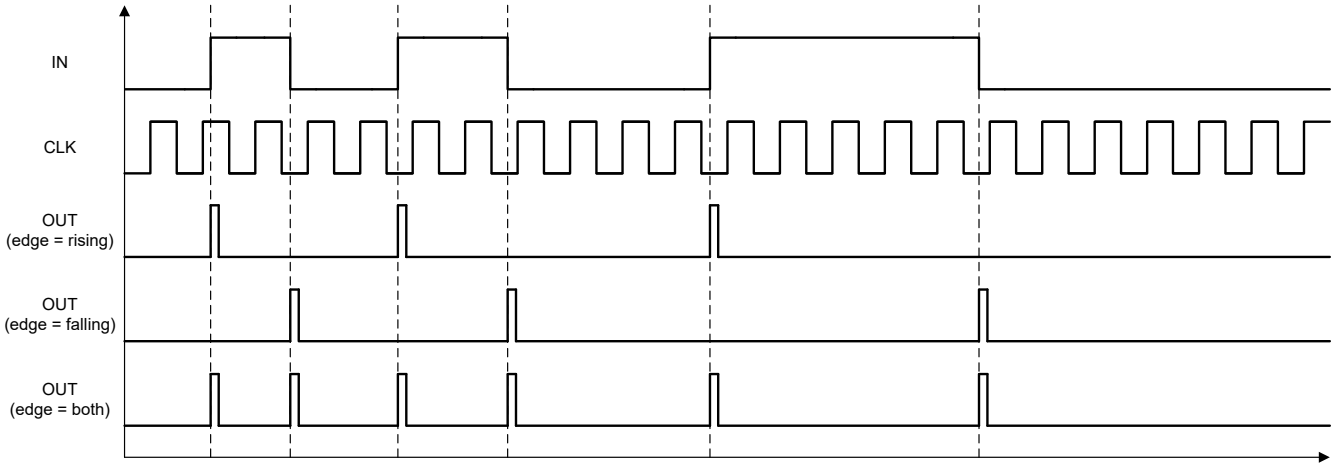


Figure 7-20. Edge Detector Output Timing Example

7.3.4.3.6 Delayed Edge Detector Mode

When configured as a Delayed edge detector (Delayed EDET), this macro-cell delays the input by the value in DATA and then generate a pulse of approximately 20ns width when the selected edge is detected on the delayed input. The initial output value of this macro-cell after device startup can also be configured to Bypass Initial, Initial Low, or Initial High. The edge on which to delay and then output an edge detect pulse is selected by the Edge select parameter and can be configured as:

- **Rising**: only delay on rising edges of IN.
- **Falling**: only delay on falling edges of IN.
- **Both**: delay on both rising and falling edges of IN.

Upon receiving a trigger, an additional 2 clock cycles is used to synchronize IN and the counter with CLK, then the counter begins decrementing from DATA on the following rising edge of CLK. If the counter is allowed to reach 0 and wrap around back to DATA, the Delayed EDET macro-cell outputs a pulse. Otherwise, if the counter is interrupted with a reset before reaching 0, the Delayed EDET macro-cell "filter out" the previous edge.

Figure 7-21 shows an example of how the Delayed EDET macro-cell operates with respect to the Edge select parameter.

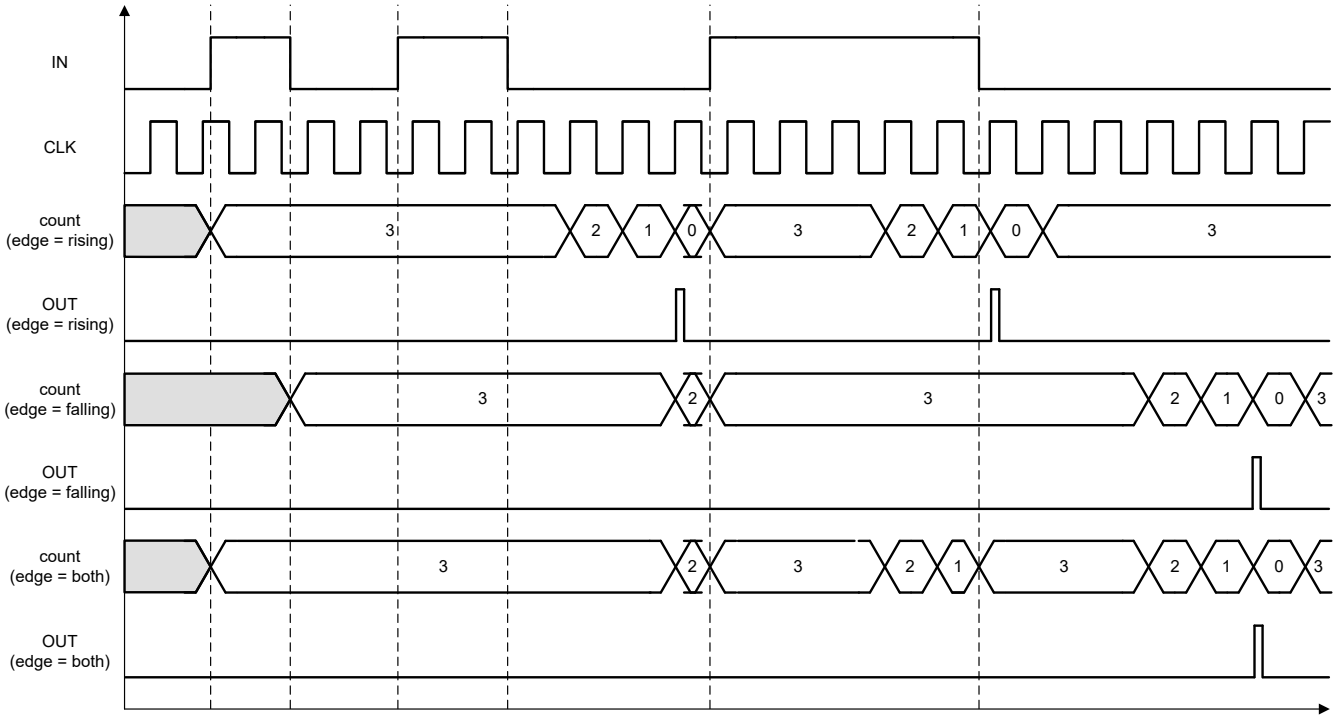


Figure 7-21. Delayed Edge Detector Output Timing Example (DATA = 3)

7.3.4.4 LUT/DFF + CNT modes

In addition to the discrete LUT, DFF/latch, or counters described previously, the configurable logic and timing blocks can be configured in two other modes:

- Mode 1: LUT/DFF into counter. The three inputs from the connection mux go into the LUT/DFF/LAT and the output of the first stage feed into the input of the counter. The output of the counter goes back into the connection mux.
- Mode 2: Counter into LUT/DFF. One input from the connection mux goes to the counter input and the output feeds into any one input of the LUT or the DFF/LAT. The output of the second stage goes back into the connection mux.

This feature enables more LUTs, DFFs/latches, and counters to be used in a design. However, within a single block, only the LUT or only the DFF/latch may be used. Further, in these modes, the external clock source from the connection mux for the counter is disabled, thus, only a frequency derived from the internal oscillator can be used.

7.3.5 Programmable Deglitch Filter or Edge Detector

The TPLD1202 has two macro-cells that can be configured as a Programmable filter (PFLT) or Edge detector (EDET). The PFLT macro-cell can be used to generate a delay (t_{pflt_d}) characterized by t_{pflt_pw} and t_{pflt_pd}. t_{pflt_pw} can be set to 125ns, 250ns, 375ns, or 500ns and t_{pflt_pd} is a fixed value. Furthermore, the output of the macro-cell can be configured to one of four options: rising edge detection, falling edge detection, both edge detection, or both edge delay. Lastly, the filter operates as a short low-pass filter and its output can be set as non-inverted or inverted.

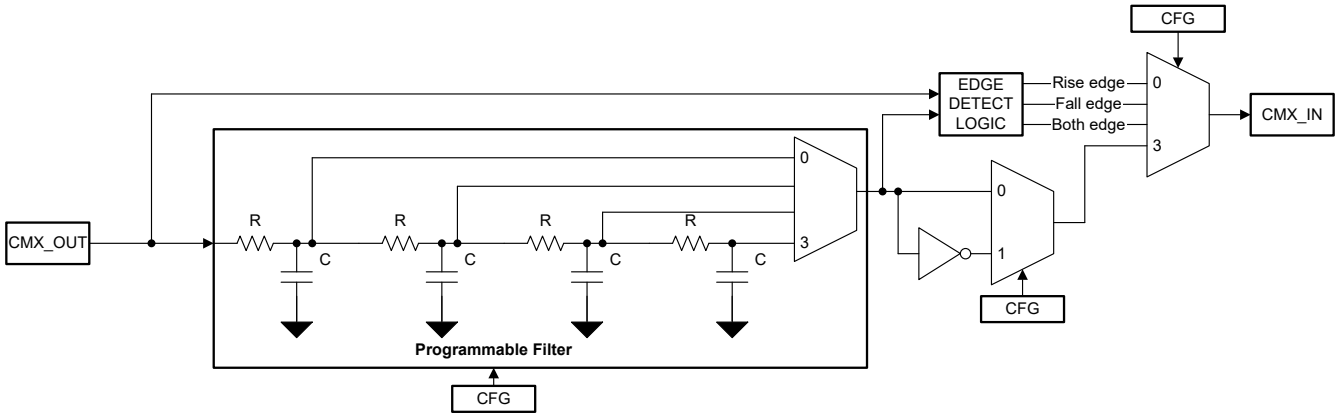


Figure 7-22. Programmable Filter/Edge Detector Block Diagram

Note

The input signal must be longer than the t_{pflt_d}, otherwise it filters out.

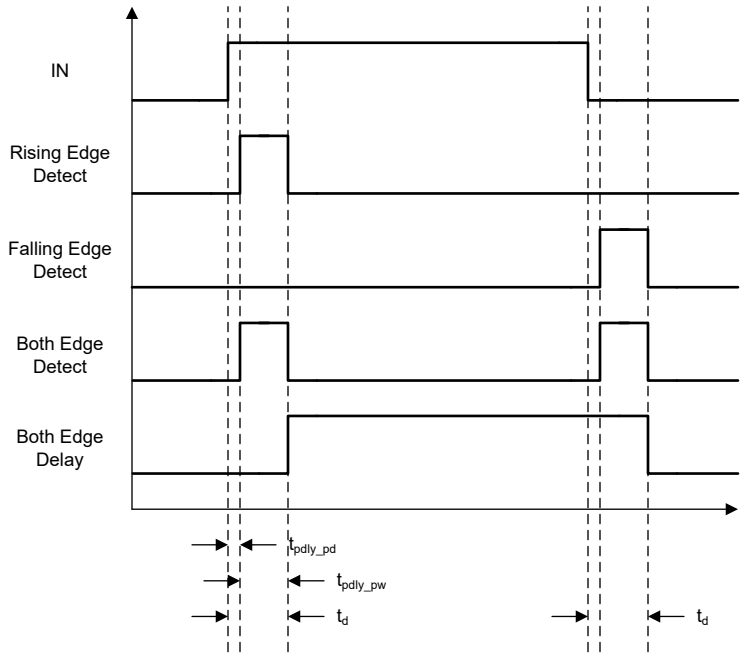


Figure 7-23. Delayed edge detector output timing diagram

7.3.6 Deglitch Filter or Edge Detector

The TPLD1202 has one macro-cell that can be configured as a Deglitch filter or an Edge detector.

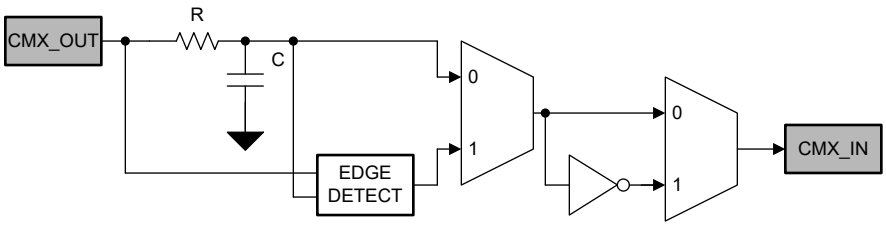


Figure 7-24. Deglitch Filter or Edge Detector Block Diagram

The Deglitch filter operates as short low-pass filter and the filter output can be set as non-inverted or inverted.

As an Edge detector, this macro-cell can be configured to output a short pulse that is triggered on the rising edge, the falling edge, both edges, or act as a filter and delay both edges. The edge detector output can be set as non-inverted or inverted.

7.3.7 State Machine (SM)

The TPLD1202 features a state machine macro-cell that can be operated synchronously or asynchronously with 16 state transition inputs, 1 clock input, 1 state machine reset input, and 8 outputs. This macro-cell can be configured to create a 2- to 8-state state machine, where the states, state transition conditions, state transition inputs, and state outputs are user-defined. Each state has a maximum of 2 transition conditions that can trigger a transition into that particular state, limited by the state transition inputs that are hardwired in the connection mux.

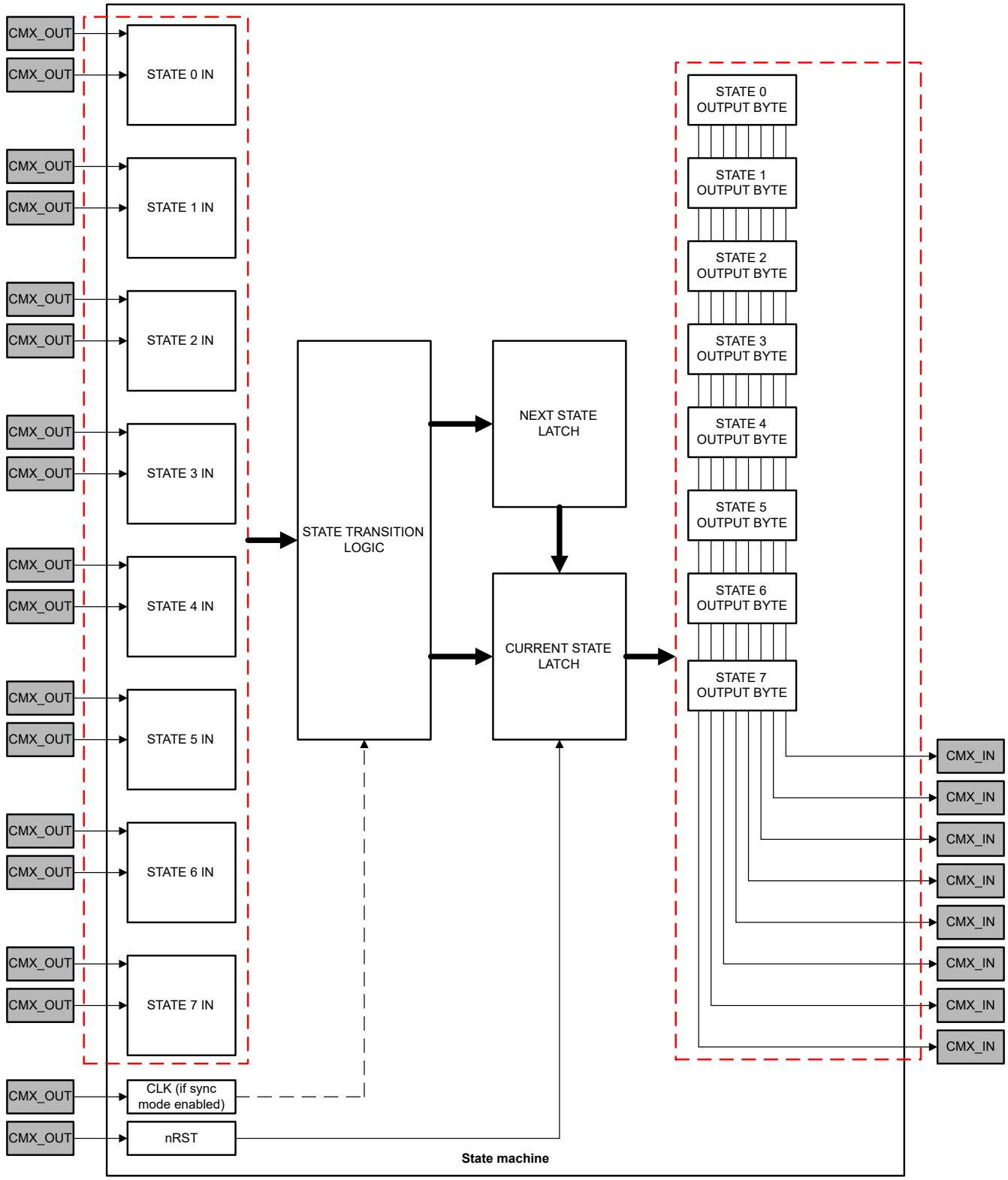


Figure 7-25. State Machine Block Diagram

7.3.7.1 State Machine Inputs

The state machine macro-cell has 18 inputs from the connection mux: 16 state transition inputs, 1 clock input, and 1 reset input.

Each of the 16 state transition inputs are active-high inputs, meaning a high-level input triggers a state transition given the timing considerations are met. Further, these 24 inputs are grouped such that each set of 2 inputs drives a transition into a particular state. For example, there are 2 inputs that drives a transition from any state into State 2. Thus, this limits the maximum number of transitions into a particular state to 2.

When operating the state machine in synchronous mode and a state transition condition is met, the state transition occurs on the next rising edge of the clock input. In asynchronous mode, when a state transition condition is met, the state transition occurs asynchronously and the clock input is unavailable/ignored.

There is also an active-low, asynchronous reset input which, when asserted, puts the state machine into the user-selected initial state and, when released, returns the state machine into normal operation from the initial state.

7.3.7.2 State Machine Outputs

The state machine macro-cell has 8 outputs into the connection mux. With a 1-byte RAM per state, users are able to set the behavior of the 8 outputs for each defined state, which could be seen as 8 parallel outputs that can be configured depending on the current state. Each of the 8 outputs are connection mux inputs that could be elsewhere in the design, such as an input into a LUT, D flip-flop, counter, or out to a GPO pin.

The state machine outputs can be updated in-system using the User Registers. For glitch-free operation, it is recommended to put the state machine in a reset while the state machine output bits are being modified.

7.3.7.3 Configuring the State Machine

The following can be configured for an operating state machine: states, initial state, state transitions, mode, clock polarity.

- **States:** Up to 8 states can be created and renamed, if desired.
- **Initial state:** One of the states creates can be selected as the initial state in which the state machine macro-cell resets to following an asynchronous reset.
- **State transitions:** Users can set the transition from one state into another to enable a state transition condition input, with a maximum of 2 transitions into a particular state. The state transition conditions are inputs from the connection mux and can be configured to come from any GPI or other macro-cell outputs.
- **Mode:** The state machine can be selected to operate in synchronous mode, in which state transition conditions are synchronously latched in with respect to the clock input, or asynchronous mode.
- **Clock sync:** In synchronous mode, this setting determines whether the state machine is rising edge triggered (sync disabled), that is state transition inputs and state transitions are latched in on the rising edge of the clock, or falling edge triggered (sync enabled).

The serial communication interface, if enabled, can be used to read the current state of an active state machine and reconfigure the state outputs. Any changes made to the state machine configuration through the serial communication interface only reflects after the next state transition or a reset event. Thus, to establish the desired behavior, best practice is to keep the state machine in reset while reconfiguring the macro-cell.

7.3.7.4 State Machine Timing Considerations

When the state machine macro-cell is in operation, especially when operating asynchronously, the state transition inputs timing requirement, delays in the I/O, other macro-cells used in the state transition input path, and the connection mux need to be taken into consideration to verify inputs are properly processed and state transitions are deterministic.

In synchronous mode, state transition trigger input needs to be asserted for at least 3 clock cycles. In asynchronous mode, the state transition trigger input needs to be asserted for at least the state transition pulse width, t_{st_pw}. If a state transition condition is met, the transition occurs after the state transition delay, t_{st_dly}.

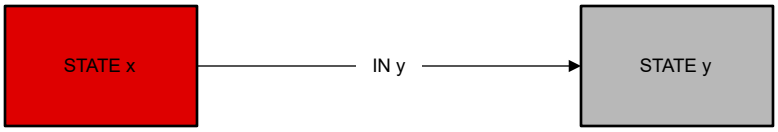


Figure 7-26. State Transitions

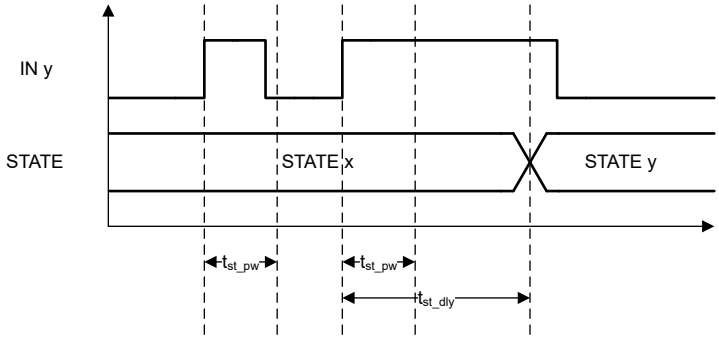


Figure 7-27. State Transition Trigger Requirements Timing Example

When two or more state transition input triggers exist within the state transition pulse width, t_{st_pw}, the next state is indeterminate. To avoid such cases, careful consideration must be taken in the timing of the state transition inputs.

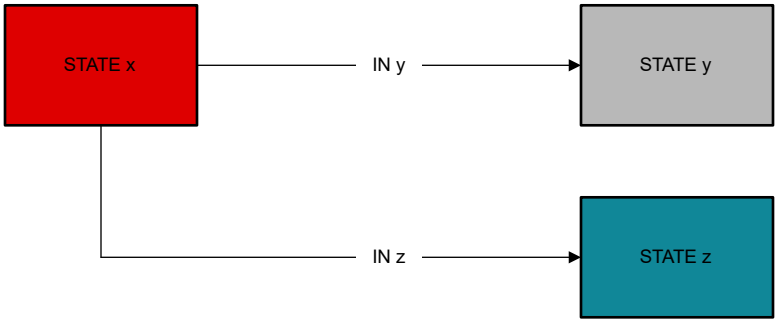


Figure 7-28. State Transitions With Competing Triggers

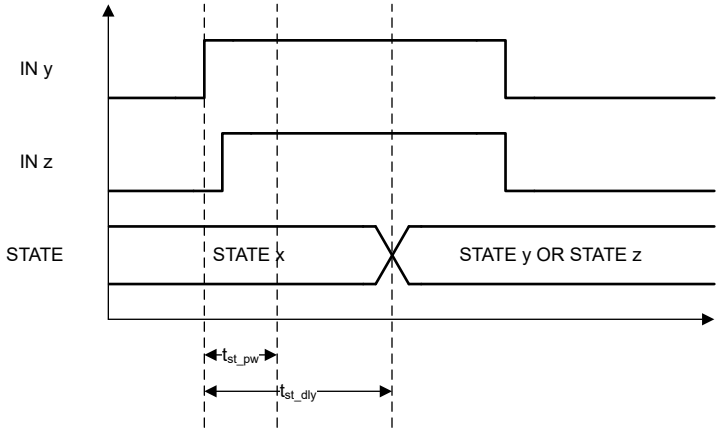


Figure 7-29. State Transition With Competing Triggers Considerations Timing Example

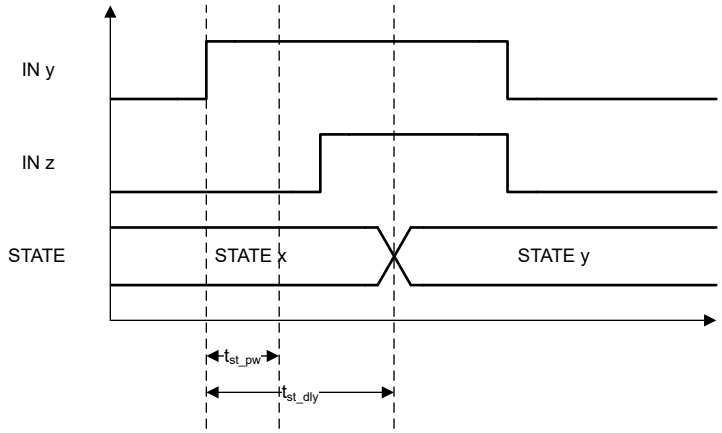


Figure 7-30. State Transition Considerations for Deterministic Transition Timing Example

For sequential state transitions or closed loop state transitions, where state transition input triggers are asserted that prompt the state machine to go into a next state, transitions into consecutive states occurs after the state transition delay, t_{st_dly}. Thus, the state machine remains in the current state for at least t_{st_dly}.

Figure 7-31. Sequential State Transition

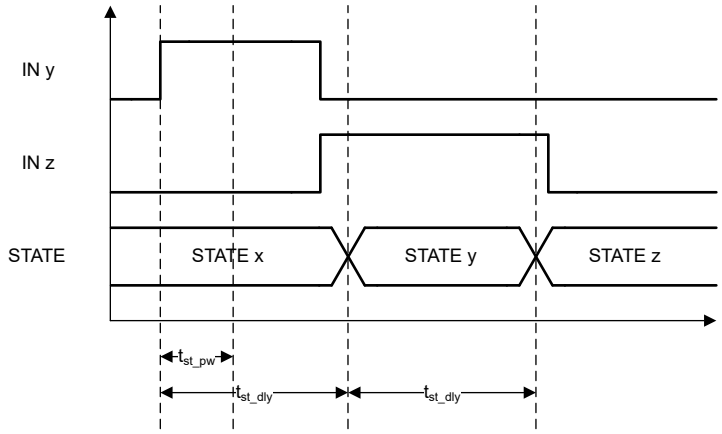


Figure 7-32. Sequential State Transition Timing Example

The closed loop state transition example shown only considers two states; however, the closed loop can be made with any number of states from two to the maximum of eight.

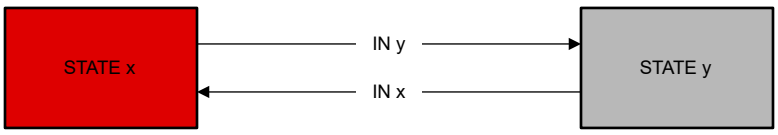


Figure 7-33. Closed loop state transition

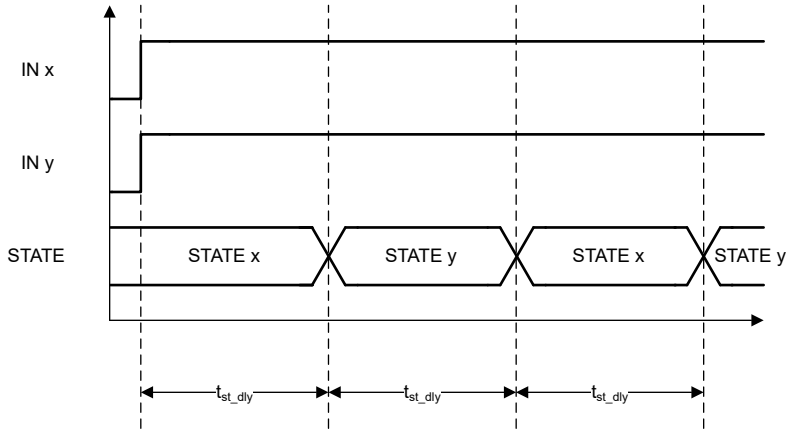


Figure 7-34. Closed Loop State Transition Timing Example

7.3.8 8-Bit Counters/Delay Generators/Finite State Machines

The TPLD1202 has 8-bit counters that can operate as a finite state machine (FSM) while in Reset counter mode. These 8-bit counter macro-cells have 4 inputs from the connection mux: counter input, FSM up/down, FSM keep, and external clock input; and 1 output into the connection mux: counter out. There is also an 8-bit parallel output of the current count value from this macro-cell that routes directly into the pulse-width modulation (PWM) generator macro-cells.

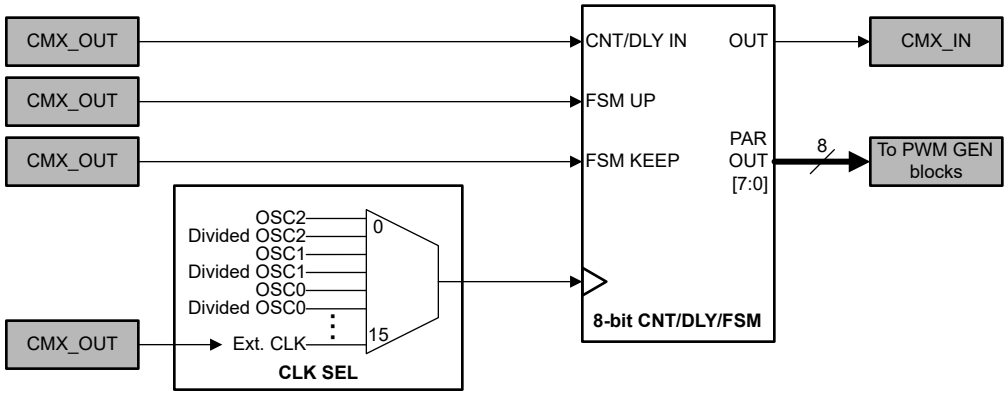


Figure 7-35. CNT/DLY/FSM block diagram

The following can be configured for an operating FSM: initial counter data and clock.

- Initial counter data: The value at which the counter will load upon reaching 0 can be set to any value between 1 and 255. The counter data can be updated in-system using the User Registers. It is recommended to put the counter in a reset state when updating the counter data registers to ensure glitch-free loading of the data.
- Edge select, the edge in which to asynchronously reset the counter to the inital counter data: Both, Rise, Fall, or High-level reset.
- Clock input: OSC0, a divided clock derived from OSC0 (/8, /64, /512, /4096, /32768, /262144), OSC1, a divided clock derived from OSC1 (/8, /64, /512), OSC2, a divided clock derived from OSC2 (/4), or an external clock.

The FSM UP input determines the direction of the counter/FSM, whether the count will decrement or increment with respect to the rising edge of the clock input. While FSM UP = Low, the counter will decrement (count downward) and reset to the inital counter data once 0 is reached; and while FSM UP = High, the counter will increment (count upward) and reset to the initial counter data once 255 is reached.

The FSM KEEP input will pause, or latch, the current count and ignore any FSM UP or clock input. The count reset input will still reset the counter, but will neither decrement nor increment. While FSM KEEP = Low, the counter will count as configured; and while FSM KEEP = High, the counter will pause.

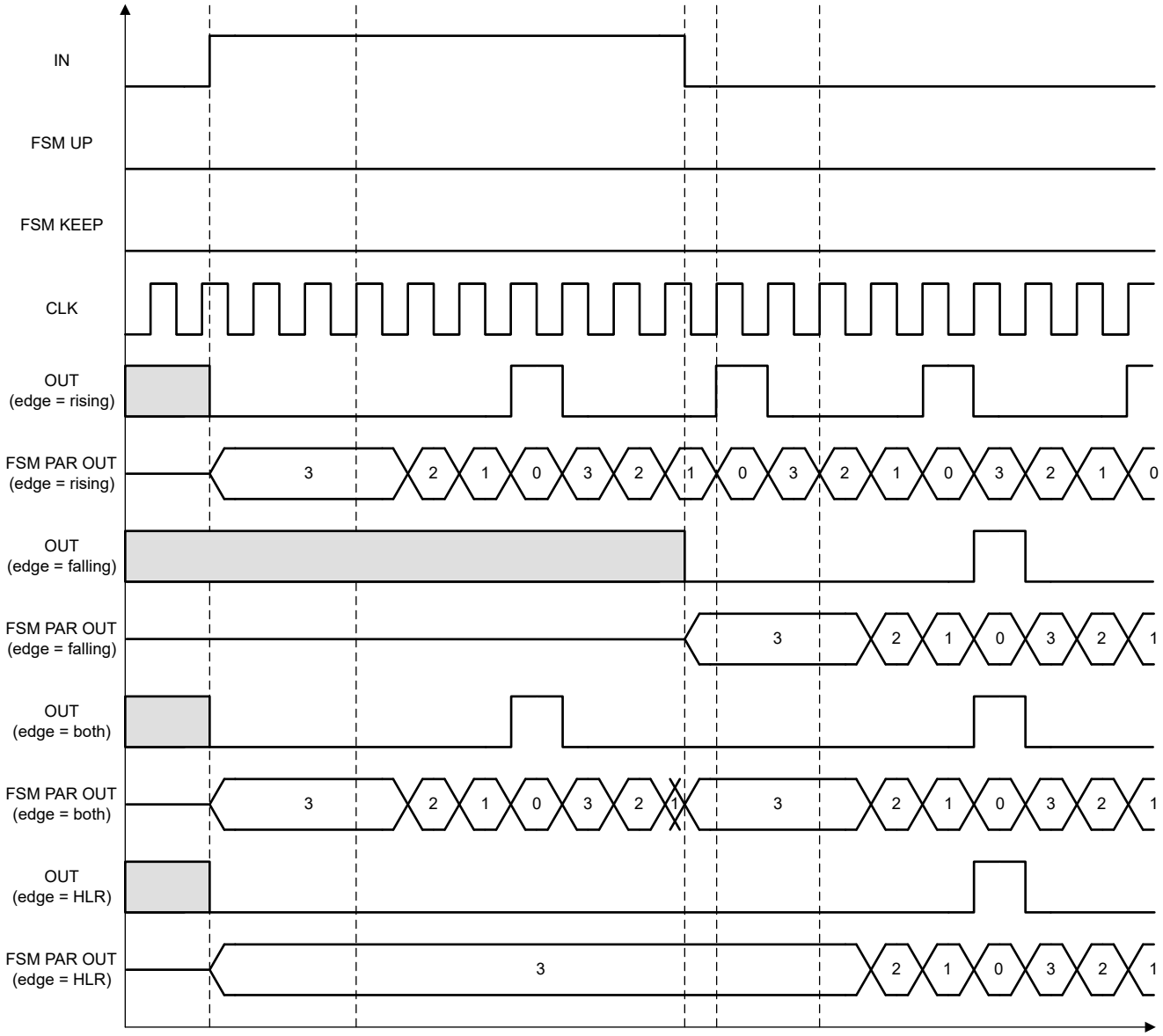


Figure 7-36. CNT/FSM timing example (DATA = 3)

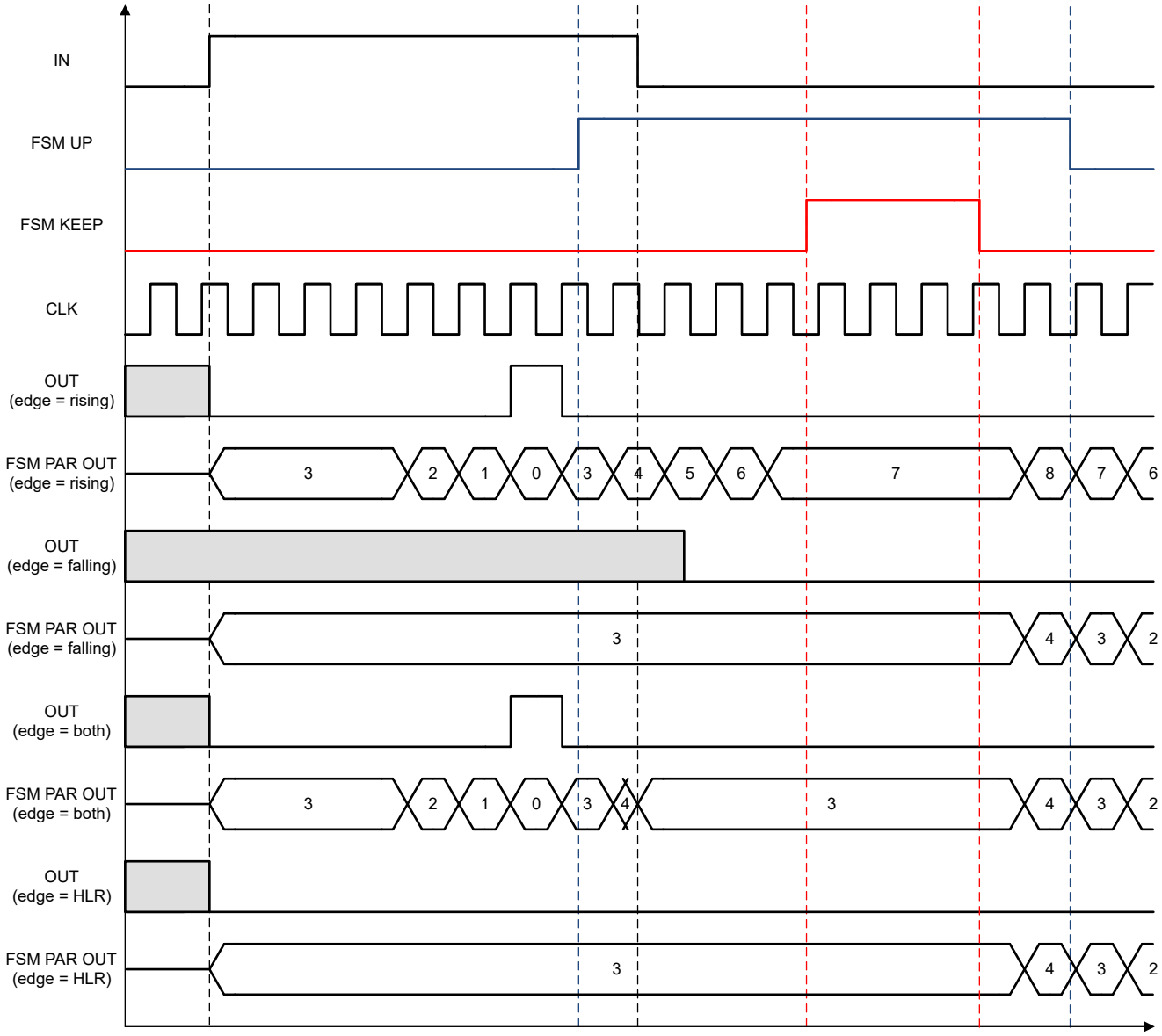


Figure 7-37. CNT/FSM with UP/KEEP timing example (DATA = 3)

7.3.9 PWM Generators

The pulse-width modulation (PWM) generator outputs a square wave with a duty cycle proportional to the counter value from the selected FSM. These PWM generator macro-cells have one input from the connection mux to control the macro-cell power up; 1 input directly from FSM blocks; and 2 outputs into the connection mux.

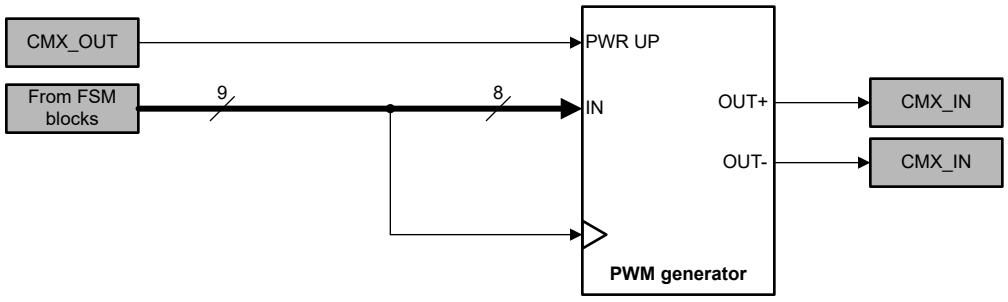


Figure 7-38. PWM Generator Block Diagram

The following can be configured for an operating PWM generator: input source, deadband time, output polarity, clock.

- Data input source (IN): Any of the four FSMs can be selected to provide the counter value.
- Deadband time (t_{db}): 0 CLKs (no deadband), 1 CLK, 2 CLKs, or 5 CLKs.
- Output polarity: the polarity of each output (OUT+ and OUT-) can be configured to non-inverted or inverted.

The duty cycle of the PWM signal calculated by:

$$\text{Duty cycle (\%)} = \left(\frac{\text{IN}}{256}\right) \times 100 \quad (4)$$

With a minimum duty cycle of 0% (or 0/256) and a maximum of 99.61% (or 255/256).

Note, upon startup of the PWM generator, the macro-cell requires 2 clock cycles for clock synchronization. If the selected deadband time is greater than the FSM counter data input, a constant low appears on the non-inverted OUT- output. Additionally, the PWM generator macro-cell can be powered down by sending a LOW signal to the PWM PWR UP input to prevent outputting in an idle state.

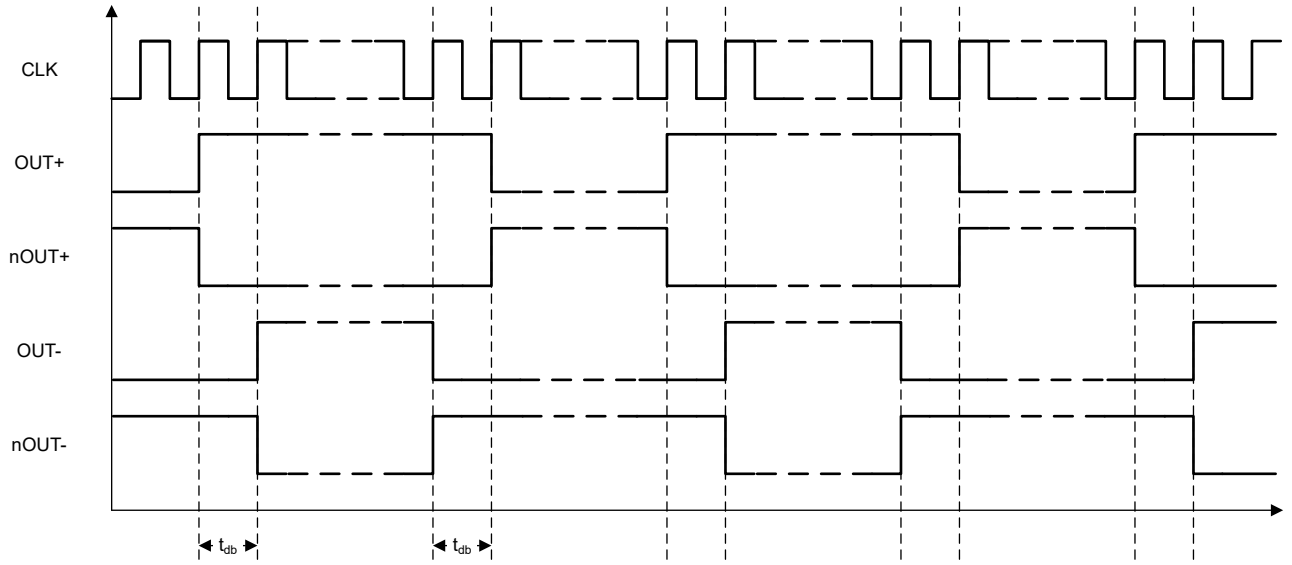


Figure 7-39. PWM Generator Timing Example

7.3.10 Watchdog Timer

The watchdog timer (WDT) macro-cell monitors the input into the macro-cell for any edge in the time frame defined by the t_{WD} time period. The WDT macro-cell has 2 inputs from the connection mux: 1 active-high enable and 1 watchdog input. There is also 1 clock input directly from the internal oscillators.

Figure 7-40. Watchdog Timer Block Diagram

The following can be configured for an operating WDT: the timeout period (t_{WD}), the output assert time (t_{WDO}), the clock source, an additional clock divider option, behavior of WDT while disabled.

- Timeout period (t_{WD}): The WDT operates on an 8-bit counter and, thus, supports count data values of 1 to 255.
- Output assert time (t_{WDO}): A separate 8-bit counter controls the output assertion time period, supporting count data values of 1 to 255.
- Clock source: OSC0, a divided clock derived from OSC0 (/8, /12, /24, /64, /512, /4096), OSC1, or a divided clock derived from OSC1 (/4, /8, /64, /512).
- Additional clock division: An additional clock divide by 100 can be toggled to further extend the timeout period.
- Behavior while disabled: Users can set the counter to reset to the specified count data when the WDT is disabled or to pause the counter and resume once the WDT is re-enabled.

When a timeout condition is reached, the WDT macro-cell outputs a Low pulse for the specified amount of time.

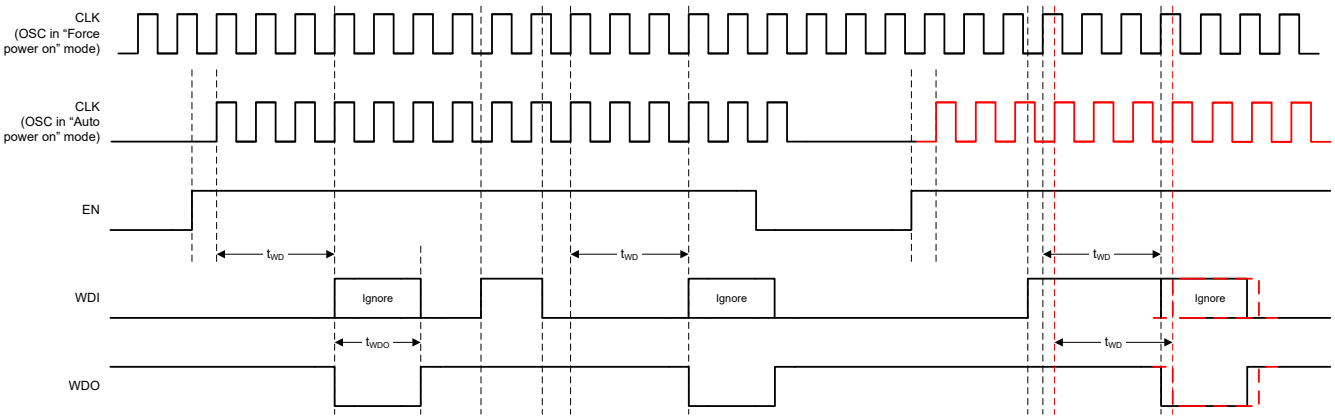


Figure 7-41. Watchdog Timer Output Timing Example (Reset Count When Disabled)

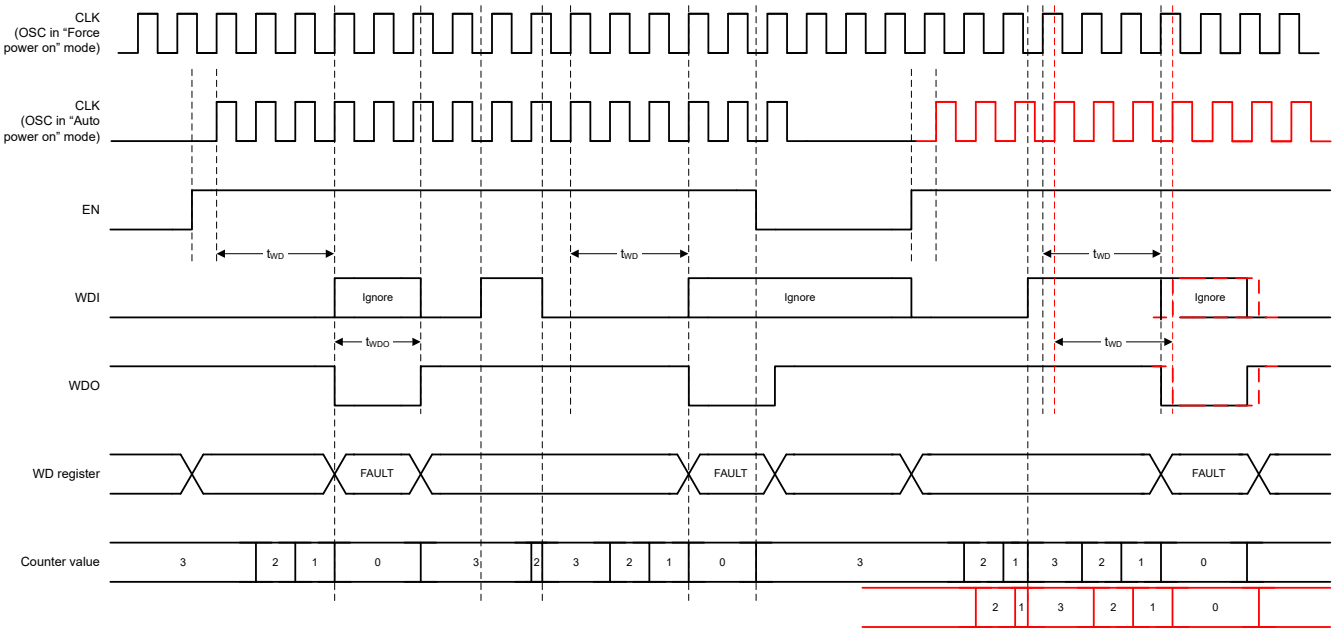


Figure 7-42. Watchdog Timer Output Timing Example With Count Data (Reset Count When Disabled)

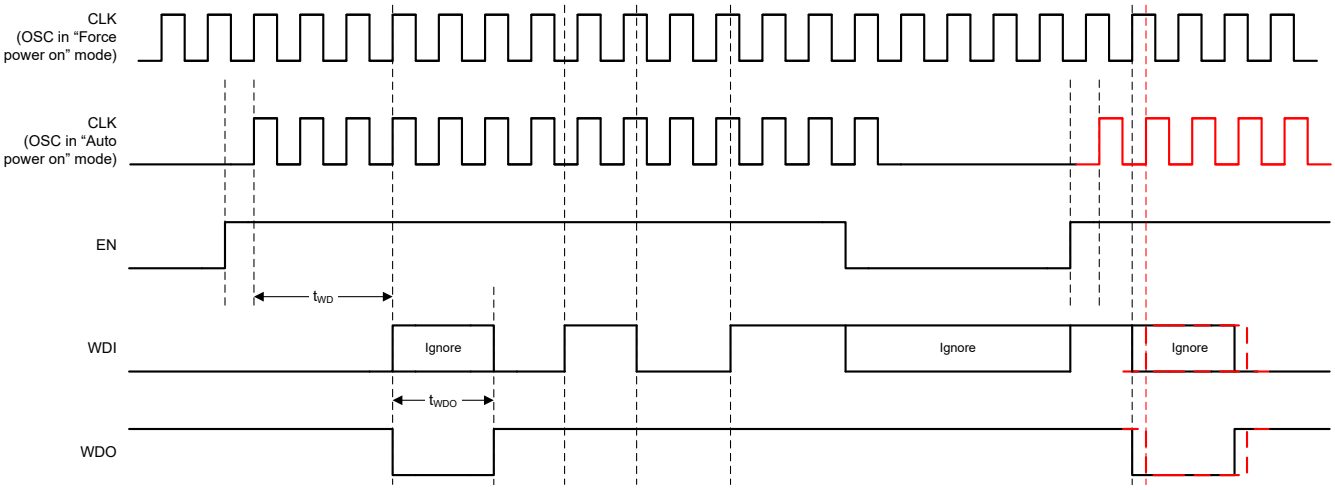


Figure 7-43. Watchdog Timer Output Timing Example (Pause Count When Disabled)

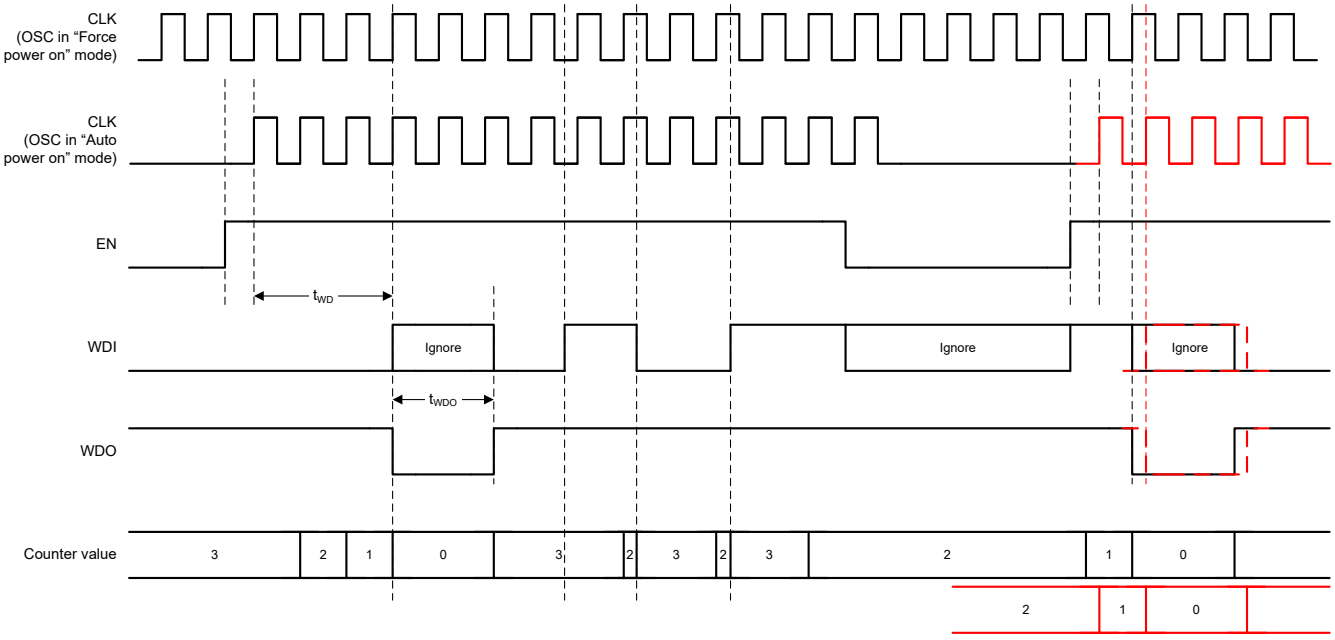


Figure 7-44. Watchdog Timer Output Timing Example With Count Data (Pause Count When Disabled)

7.3.11 Multi-channel Analog Comparator (McACMP)

The TPLD1202 has one Multi-channel Analog comparator (McACMP) macro-cell with an integrated sampling engine. The McACMP compares two voltages (IN+ and IN-) and outputs a digital signal (OUT) indicating which is larger, a High signal for IN+ and a Low for IN-.

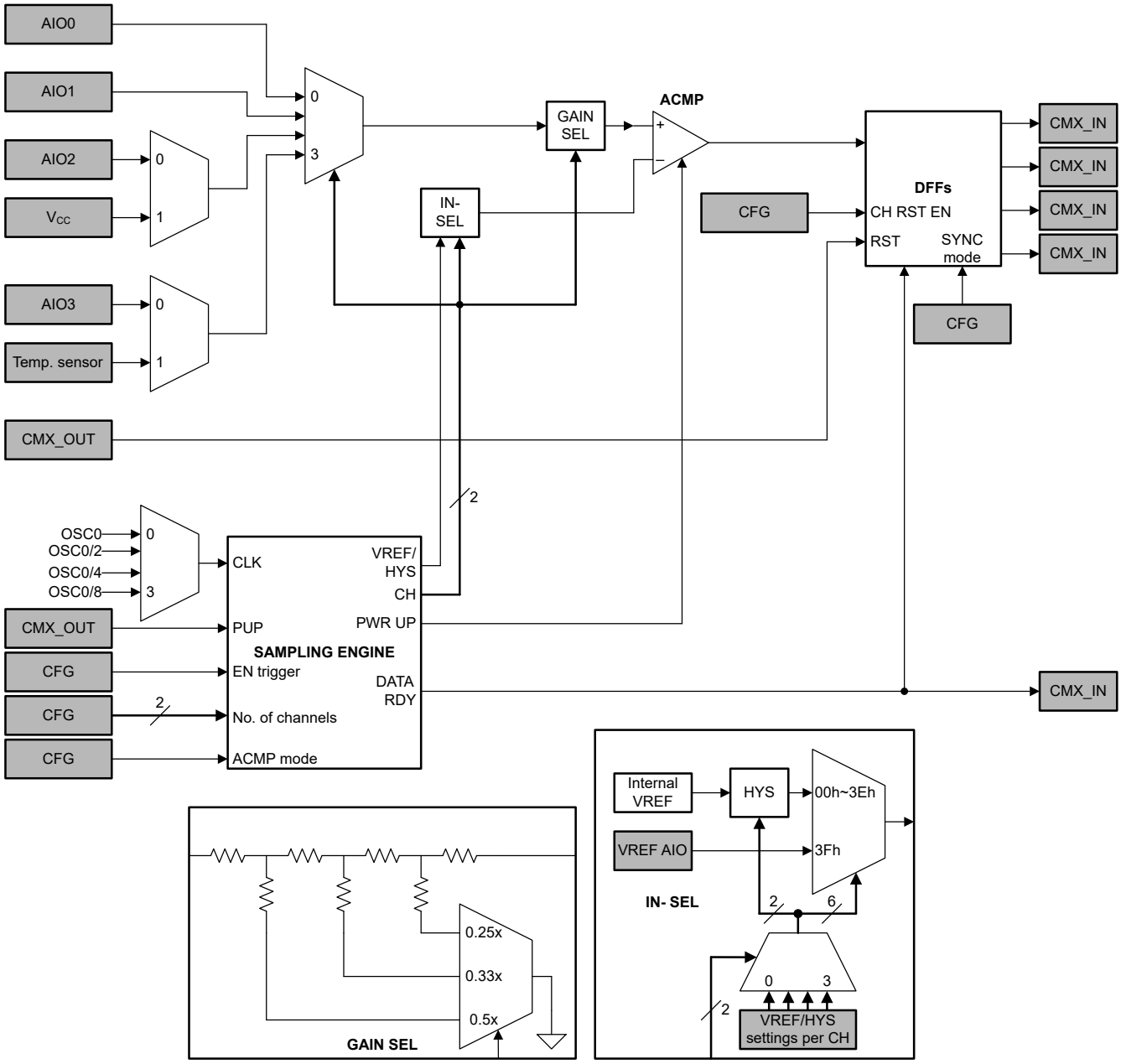


Figure 7-45. Multi-channel Analog Comparator Block Diagram

For the McACMP macro-cell to be used in a TPLD design, the power up (PUP) port needs to be connected to a logic high signal. By connecting the PUP signal coming from the connection mux, McACMP can be operated always on, always off, or switched on dynamically. When the McACMP is powered down, the output is Low.

- PUP = 1 => ACMP is powered up.
- PUP = 0 => ACMP is powered down.

Upon powerup, the McACMP's output remains Low, and then become valid t_{start} after the PUP input signal goes High.

The McACMP macro-cell has a positive input that can be connected to a variety of external sources with a selectable gain stage and voltage hysteresis before going into the analog comparator. The negative input is either created from an internal VREF or provided by way of an external source.

Table 7-21. McACMP Input Sources

Parameters	Primary source	Secondary source
IN+ source	McACMP IN0	
	McACMP IN1	
	McACMP IN2	V_{CC}
	McACMP IN3	Temp. sensor

IN+ gain: The McACMP positive input can be provided by a variety of external sources, and can also have a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connecting to the analog comparator.

IN- voltage range: 32mV to 2.016V through the internal VREF or up to 2.016V external source.

Hysteresis: If the internal VREF is used, corresponding McACMP channels have four selectable hysteresis options: 0mV, 32mV, 64mV, and 192mV.

- **0mV**: disables the input signal hysteresis.
- **64mV**: is a +32mV and -32mV hysteresis. For VREF = 1.024V, the trigger points are 1.056V and 0.992V.
- **128mV**: is a +64mV and -64mV hysteresis. For VREF = 1.024V, the trigger points are 1.088V and 0.960V.
- **192mV**: is a +96mV and -96mV hysteresis. For VREF = 1.024V, the trigger points are 1.120V and 0.928V.

If hysteresis is desired, the internal VREF must be used. Further, hysteresis values that otherwise extends beyond the range of the VREF is limited to the minimum and maximum values available in the device. For example, if IN- = 1.984V and VHYS = ±64mV, the lower trigger point is 1.920V and the upper trigger point is 2.016V.

When only one channel is selected, the McACMP disables the sampling engine and acts as a discrete analog comparator.

In multi-channel sampling mode, the TPLD1202 can be configured to sample up to 4 channels, each with its own selectable gain, voltage reference, and hysteresis (if the internal VREF is used). The sampling clock can be selected from the output of OSC0 with a given pre-divider and an additional divider at the McACMP. Other configurations that can be set are the output synchronicity, the trigger to begin a sample sequence, and an asynchronous reset option per channel.

When sampling in multi-channel mode, the McACMP samples the set channels in sequential order (channel 0 through channel n) and the edge of the clock on which samples are captured can be selected.

Clock: The McACMP sampling clock can be selected to be OSC0, OSC0/2, OSC0/4, or OSC0/8.

Enable trigger: Note that the Enable signal is a synchronous signal for the McACMP, thus the trigger pulse width needs to be at least one clock cycle wide.

- **Edge sensitive EN mode:** The McACMP begins one sampling sequence when a rising edge is detected at the PUP input and then enter an idle state.
- **Level sensitive EN mode:** The McACMP begins the sampling sequence when a high signal is detected at the PUP input and continuously sample as long as PUP is high, and once PUP goes low, the McACMP finishes the sampling sequence before entering an idle state.

Output synchronicity:

- **Simultaneous:** Sampled outputs are latched and then appear at the respective channel output after the last channel is sampled.
- **Staggered:** Sampled outputs appears at the respective channel output as they are sampled.

Sampling edge select:

- **Negative edge:** samples are captured on the negative or falling edge of the clock.
- **Positive edge:** samples are captured on the positive or rising edge of the clock.

Sequence restart/output latch reset: while the McACMP is running, a restart/reset signal can be asserted to restart the sampling sequence from channel 0. Channels can also independently be selected to have the output latch data cleared when this signal is asserted. If the reset input is held low, the McACMP will continuously sample channel 0 regardless of Enable trigger mode, until the reset is released.

There is also a data ready output that asserts a high signal for one clock of the base clock frequency once all channels configured have been sampled. For example, if the 1kHz (2kHz/2) sampling clock is selected, the data ready pulse width is 500µs.

7.3.12 Voltage Reference (VREF)

The TPLD1202 has a voltage reference (VREF) macro-cell to provide references to the analog comparators. This macro-cell provides a user selection of fixed voltage references from 32mV to 2.016V in 32mV increments or an externally supplied voltage reference from the External VREF AIO can be provided. The External VREF option is shared between all comparators.

When operating on a V_{CC} less than 2.3V, the maximum VREF option is reduced to V_{CC} - 0.3V; thus, the maximum VREF when operating at 1.8V supply is 1.504V.

The VREF selection per comparator can be updated in-system using the User Registers. For glitch-free measurements, TI recommends disabling/powering down all analog comparators when changing the VREF. If the analog comparator is not disabled while the VREF selection is being updated, the analog comparator can take up to 10µs for valid data to be output.

Table 7-22. VREF Selection Table

Bit Enumeration	VREF output
000000	32mV
000001	64mV
000010	96mV
000011	128mV
000100	160mV
000101	192mV
000110	224mV
000111	256mV
001000	288mV
001001	320mV
001010	352mV
001011	384mV
001100	416mV
001101	448mV
001110	480mV
001111	512mV
010000	544mV
010001	576mV
010010	608mV
010011	640mV
010100	672mV
010101	704mV
010110	736mV
010111	768mV
011000	800mV
011001	832mV

Table 7-22. VREF Selection Table (continued)

Bit Enumeration	VREF output
011010	864mV
011011	896mV
011100	928mV
011101	960mV
011110	992mV
011111	1024mV
100000	1056mV
100001	1088mV
100010	1120mV
100011	1152mV
100100	1184mV
100101	1216mV
100110	1248mV
100111	1280mV
101000	1312mV
101001	1344mV
101010	1376mV
101011	1408mV
101100	1440mV
101101	1472mV
101110	1504mV
101111	1536mV
110000	1568mV
110001	1600mV
110010	1632mV
110011	1664mV
110100	1696mV
110101	1728mV
110110	1760mV
110111	1792mV
111000	1824mV
111001	1856mV
111010	1888mV
111011	1920mV
111100	1952mV
111101	1984mV
111110	2016mV
111111	Ext. VREF AIO

Table 7-23. VREF Range

V_{CC}	VREF Range
1.71V - 2.3V	32mV - 1.504V
2.3V - 5.5V	32mV - 2.016V

7.3.13 Analog Temperature Sensor (TS)

The TPLD1202 has an Analog temperature sensor (TS) macro-cell that operates from -40°C to +125°C. The linear transfer function has a slope of -0.0044V/°C (typical) and an output voltage of 1.061V (typical) at 0°C.

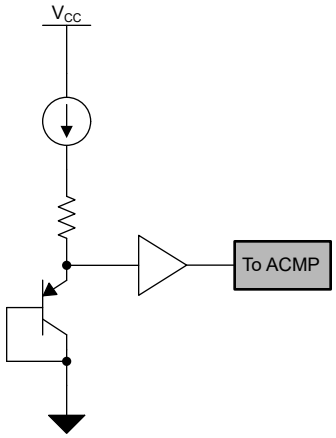


Figure 7-46. Analog temperature sensor block diagram

The formula to convert from temperature (T, in Celsius) to sensor output (V_{out}, in volts) is:

$$V_{out} = [-0.0044 \times T] + 1.061 \quad (5)$$

7.3.14 Oscillators

The TPLD1202 has two internal oscillators, OSC0 is selectable between 2kHz and 10kHz and OSC1 is fixed at 25MHz. The user can also bypass in the internal oscillators and the operating frequency can come from an IO

7.3.14.1 2kHz or 10kHz Selectable Frequency Oscillator

The TPLD1202 has one internal oscillator, selectable to operate at 2kHz or at 10kHz. The user can select one of these operating frequencies for the OSC macro-cell, or the internal oscillator can be bypassed and the operating frequency can come from an external clock.

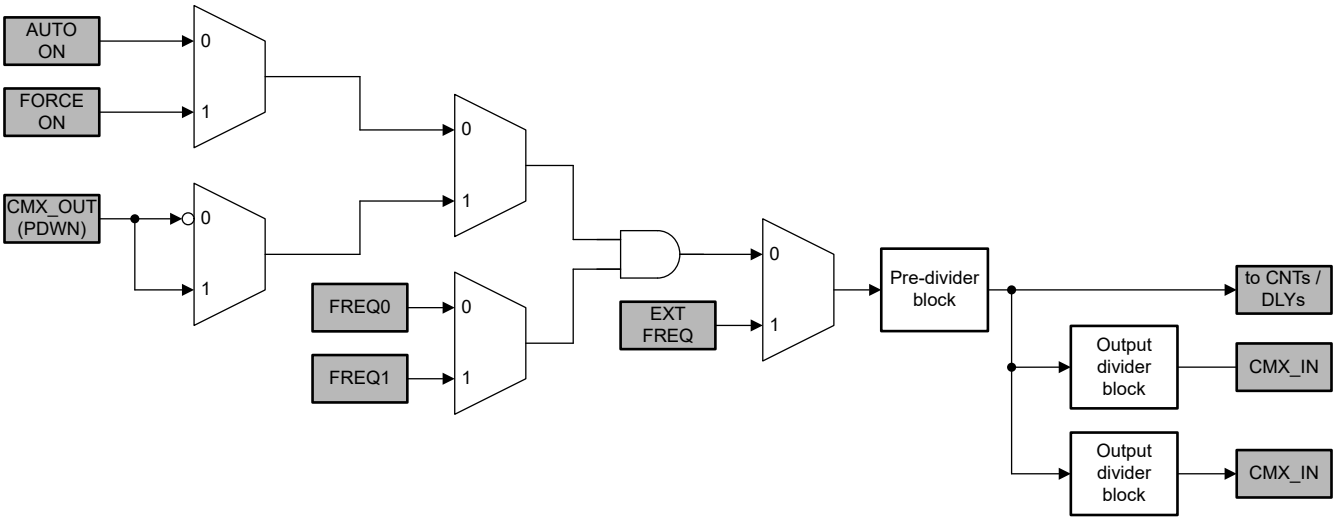


Figure 7-47. Selectable Frequency Oscillator Block Diagram

Following the operating clock input, there are two divider stages that allow users the flexibility of various clock frequencies for use throughout the device.

The first stage divider allows the selection of up to four options from the operating oscillator frequency as listed in Oscillator Pre-dividers. The output of the first divider stage is routed directly to the counter/delay generator macro-cell CLK inputs, where a separate second divider stage is available.

The output of the first divider stage is also routed into a second divider stage within the oscillator macro-cell. The oscillator macro-cell has two separate second stage dividers, allowing for the output of two separate clocks (OUT0 and OUT1) into the connection mux. See Oscillator Output Dividers.

Table 7-24. Frequency Options and Limits

Frequency Option	MIN	TYP	MAX
FREQ0	1.908kHz	2kHz	2.102kHz
FREQ1	9.44kHz	10kHz	10.6kHz
EXT FREQ	-	-	10MHz

Table 7-25. Oscillator Pre-dividers

Pre-Divider Option	Magnitude
P0	1
P1	2
P2	4
P3	8

Table 7-26. Oscillator Output Dividers

Output Divider Options	Magnitude
OD0	1
OD1	2
OD2	3
OD3	4
OD4	8
OD5	12
OD6	24
OD7	64

7.3.14.2 25MHz Fixed Frequency Oscillator

The TPLD1202 has one internal oscillator operating at 25MHz. The user can use the oscillator at this operating frequency for the OSC macro-cell, or the internal oscillator can be bypassed and the operating frequency can come from an external clock.

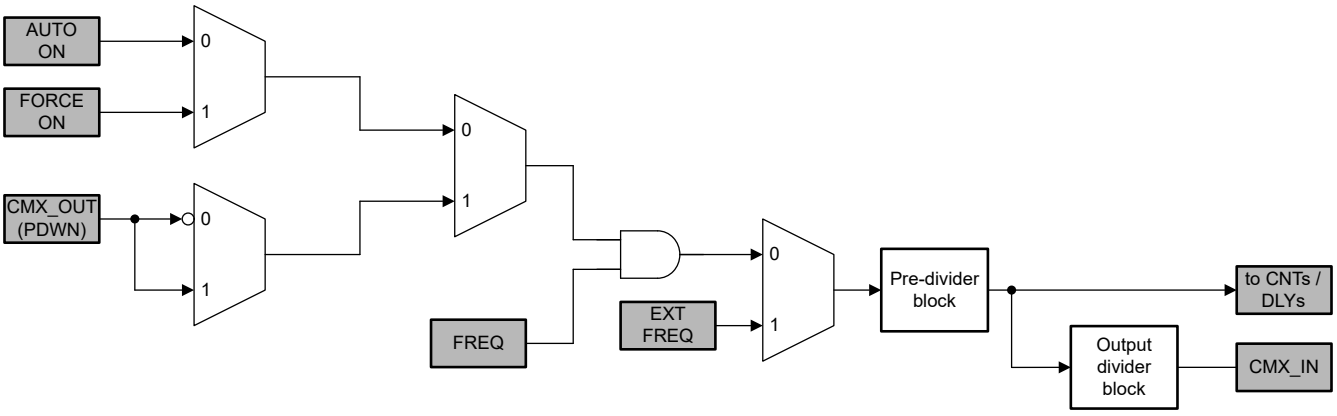


Figure 7-48. Fixed frequency oscillator block diagram

Following the operating clock input, there are two divider stages that allow users the flexibility of various clock frequencies for use throughout the device.

The first stage divider allows the selection of up to four options from the operating oscillator frequency as listed in Table 7-28. The output of the first divider stage is routed directly to the counter/delay generator macro-cell CLK inputs, where a separate second divider stage is available.

The output of the first divider stage is also routed into a second divider stage within the oscillator macro-cell. The oscillator macro-cell has a separate second stage divider, with an output (OUT0) into the connection mux. See Table 7-29.

Table 7-27. Frequency Options and Limits

Frequency Option	MIN	TYP	MAX
FREQ	23.5MHz	25MHz	26.225MHz
EXT	-	-	25MHz

Table 7-28. Oscillator Pre-dividers

Pre-Divider Option	Magnitude
P0	1
P1	2
P2	4
P3	8

Table 7-29. Oscillator Output Dividers

Output Divider Options	Magnitude
OD0	1
OD1	2
OD2	3
OD3	4
OD4	8
OD5	12
OD6	24
OD7	64

7.3.14.3 Oscillator Power Modes

When using any of the device's internal oscillator, there are three power modes available for each oscillator:

- **Auto power on (CTRL_SRC = 0 and PWR_MODE = 0):** the internal oscillator is triggered when any macro-cell that requires the oscillator is running and then power off once the task is complete.
- **Force power on (CTRL_SRC = 0 and PWR_MODE = 1)**: the internal oscillator continuously runs as long as the device is powered on.
- **External power on/off (CTRL_SRC = 1, CTRL_SEL = 0, and PWR_MODE = 1)**: a High input into the PDWN input powers down the oscillator and a Low powers on the oscillator.

These power modes are only applicable when the internal oscillator is selected and is bypassed when an external clock (SRC_SEL = 1) is used.

7.3.15 Serial Communications

The TPLD1202 has a serial communications macro-cell for in-system updates to configuration registers via the user registers.

The user registers allow for reading of the Device ID, Program ID, current Counter COUNT, current Counter DATA, Watchdog Timer DATA, Watchdog Timer Status, Pattern Generator DATA, State Machine Status and

Output DATA, Voltage Reference Selections for the Analog Comparators, Virtual Inputs, and Virtual Outputs. See the User Registers register map for associated addresses.

By writing to the respective registers, the current Counter DATA, Watchdog Timer DATA, Pattern Generator DATA, State Machine Output DATA, Voltage Reference Selections, and Virtual Inputs can be updated in-system.

This macro-cell can configure the TPLD1202 as an I2C or SPI device.

7.3.15.1 I2C Mode

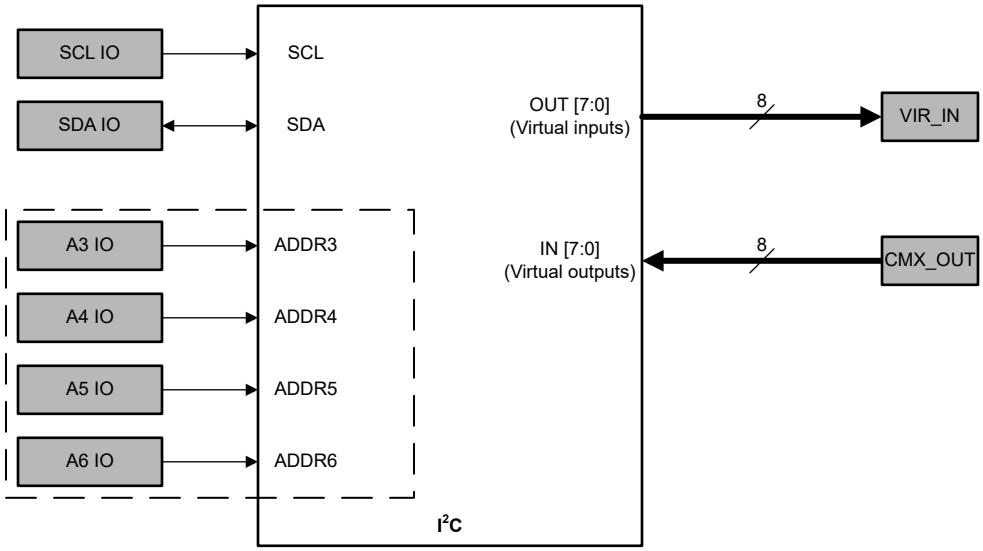


Figure 7-49. I2C Serial Communications GPIO Allocation

When configured to I2C, the following IOs are used by the macro-cell:

- IO1: SCL
- IO2: SDA
- IN0: HW defined ADDR 3, A3 (optional)
- IO4: HW defined ADDR 4, A4 (optional)
- IO5: HW defined ADDR 5, A5 (optional)
- IO8: HW defined ADDR 6, A6 (optional)

The TPLD1202 supports:

- Peripheral mode only
- Standard mode, Fast mode, and Fast mode plus
- Configurable 4-bit hardware address by IO or by OTP memory

The bidirectional I2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer only initiates when the bus is not busy.

The target device address of the TPLD is derived from the OTP and the most significant byte have an option to come from IOs, which the TPLD samples the IOs only at power up of the TPLD device, which allows use of the respective GPIO as a digital input within a circuit design. There is also an option to enable IO latching to continuously sample while powered on by setting the I2C_IO_LAT bit to logic 1.

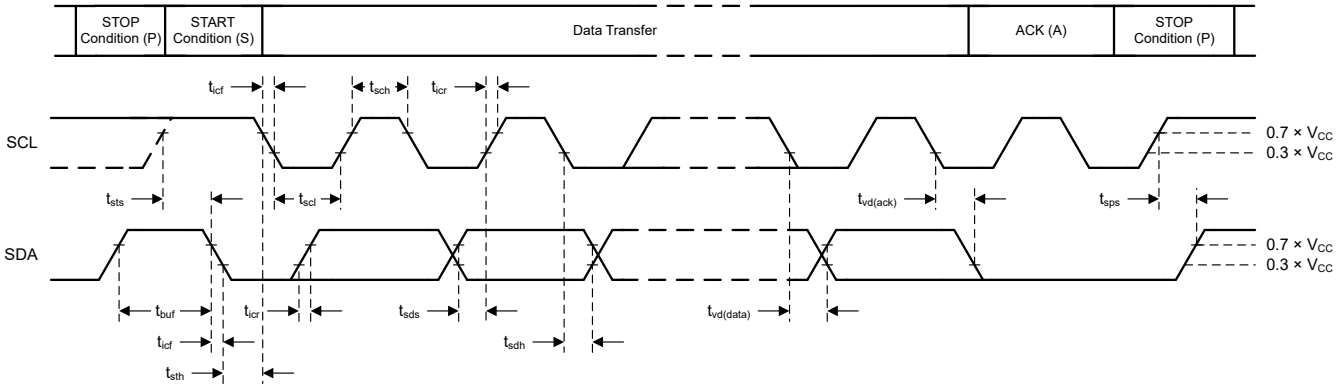


Figure 7-50. I²C Read/Write Timing Diagram

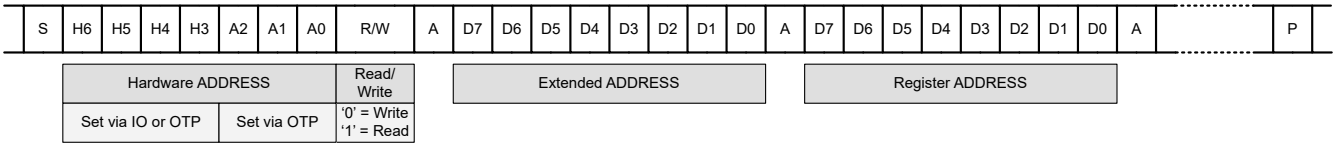


Figure 7-51. TPLD I²C Frame and Formatting

I²C communication with this device is initiated by a controller sending a START condition, a high-to-low transition on the SDA input/output, while the SCL input is high. After the START condition, the device hardware address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address input of the responder device must not be changed between the START and the STOP conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP).

A STOP condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller.

Any number of data bytes can be transferred from the transmitter to receiver between the START and the STOP conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a responder receiver is addressed, the responder receiver must generate an ACK after each byte is received. Similarly, the controller must generate a NACK after each byte that the controller receives from the responder transmitter. Setup and hold times must be met for proper operation.

A controller receiver signals an end of data to the responder transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the responder. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a STOP condition.

When writing or reading from the TPLD1202, there is an option to enable automatic address incrementing by writing a logic 0 to bit 0 of address 0x0FD. This can be disabled by writing a logic 1.

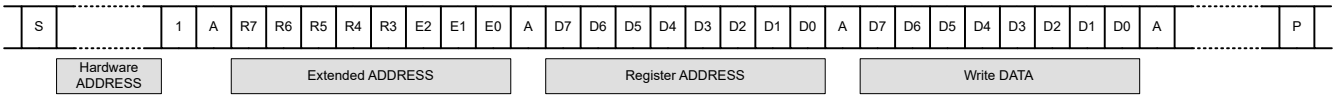


Figure 7-52. TPLD I²C Write Command Formatting

To transmit data or write to the TPLD1202, the bus controller must send the device hardware address and set the least significant bit (LSB) to a logic 0. The next two bytes set the register address and then the write data follows. There is no limitation on the number of data bytes sent in one write frame.

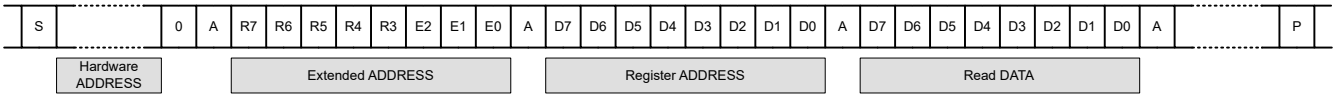


Figure 7-53. TPLD I²C Read Command Formatting

To read from the TPLD1202, the bus controller first must send the TPLD1202 hardware address with the LSB set to a logic 1. The byte that follows contains the data in the address previously written to, or the next address if address auto-increment is enabled.

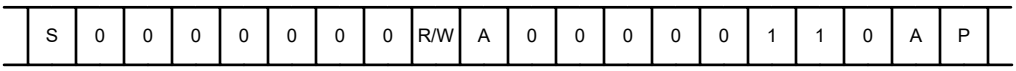


Figure 7-54. TPLD I²C Software Reset Command

The Software Reset call is a command sent from the controller on the I2C bus that instructs all devices that support the command to be reset to the power-up default state and listening for the Software Reset call can be enabled by setting the I2C_RST_EN bit to logic 1. For the Software Reset to function as expected, the I²C bus must be functional and no devices can be hanging the bus.

The software Reset call is defined as the following steps:

1. A START condition is sent by the I²C bus controller.
2. The address used is the reserved General Call I²C bus address '0000 000' with the R/W bit set to 0. The byte sent is 0x00.
3. Any devices supporting the General Call functionality ACK. If the R/W bit is set to 1 (read), the device NACK.
4. Once the General Call address is acknowledged, the controller sends only 1 byte of data equal to 0x06. If the data byte is any other value, the device does not acknowledge nor reset. If more than 1 byte is sent, no more bytes are acknowledged and the device ignores the I²C message considering it invalid.
5. After the 1 byte of data (0x06) is sent, the controller sends a STOP condition to end the Software Reset call sequence. A repeated START condition is ignored by the device and no reset can be performed.

Once the above steps are completed successfully, the device performs a reset, clearing all register values back to power-on defaults.

7.3.15.2 SPI Mode

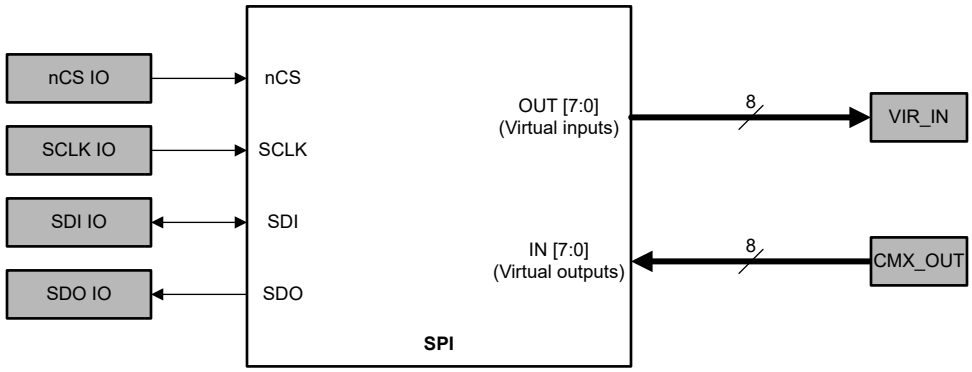


Figure 7-55. SPI Serial Communications GPIO Allocation

When configured to SPI, the following IOs are used by the macro-cell:

- IO5: nCS
- IO1: SCLK

- IO2: SDI
- IO4: SDO

The TPLD1202 supports:

- Peripheral mode only
- SPI mode 0, that is, SCLK is idle Low and SDI/SDO is valid on the rising edge of SCLK
- Up to 4MHz SCLK
- 8-bit data frame size

The SPI communication uses a standard SPI. Physically, the digital interface pins are nCS (Chip select not), SDI (Serial Data In), SDO (Serial Data Out), and SCLK (SPI Clock).

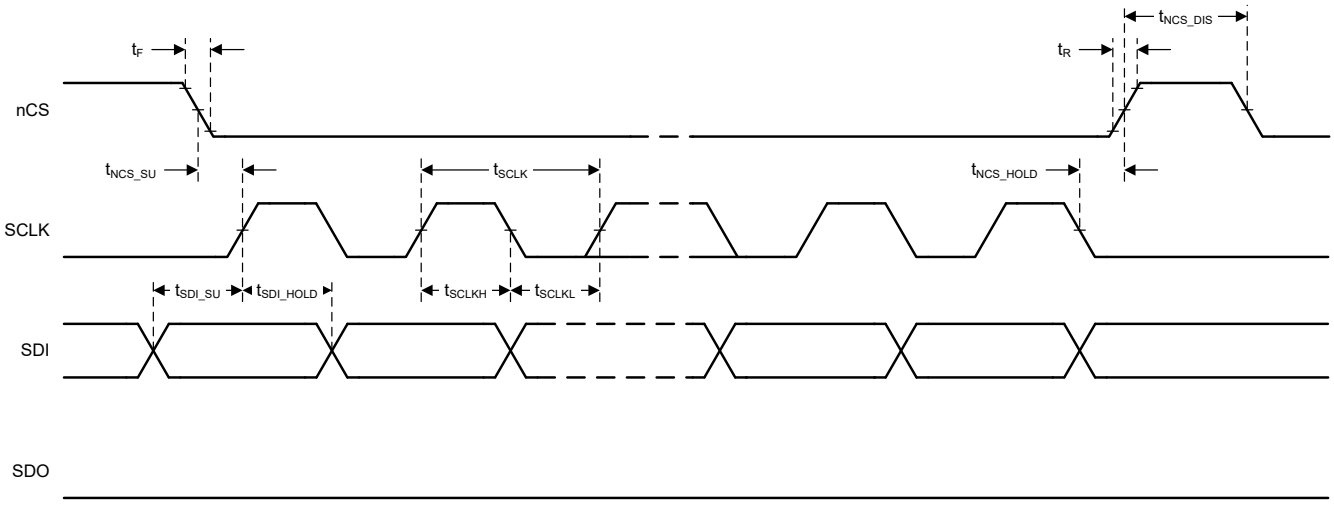


Figure 7-56. SPI Write Timing Diagram

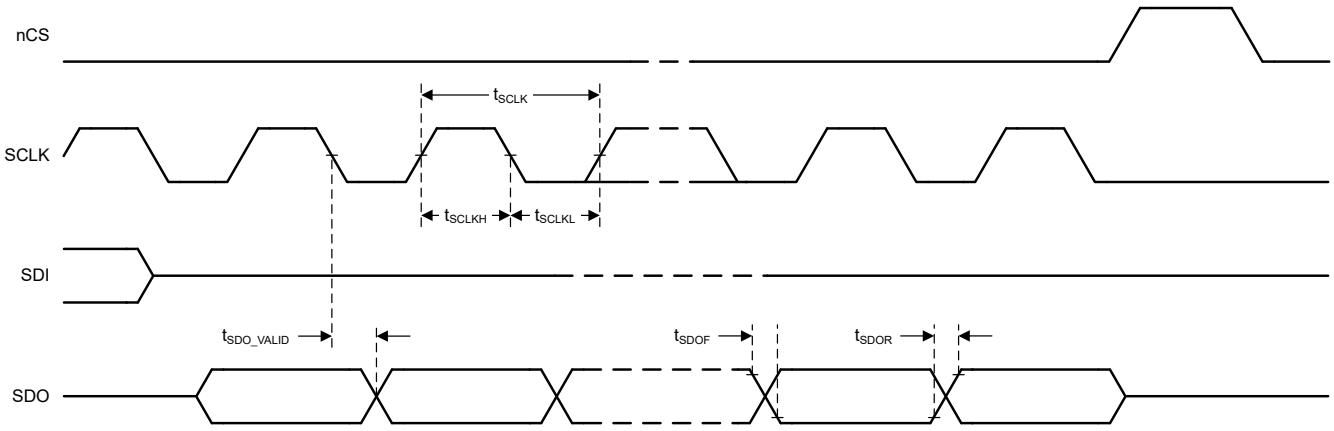


Figure 7-57. SPI Read Timing Diagram

The SPI module in TPLD1202 supports mode 0, thus input data on the SDI line is sampled on the rising edge of SCLK. The SPI output data on the SDO line is changed on the falling edge of SCLK.

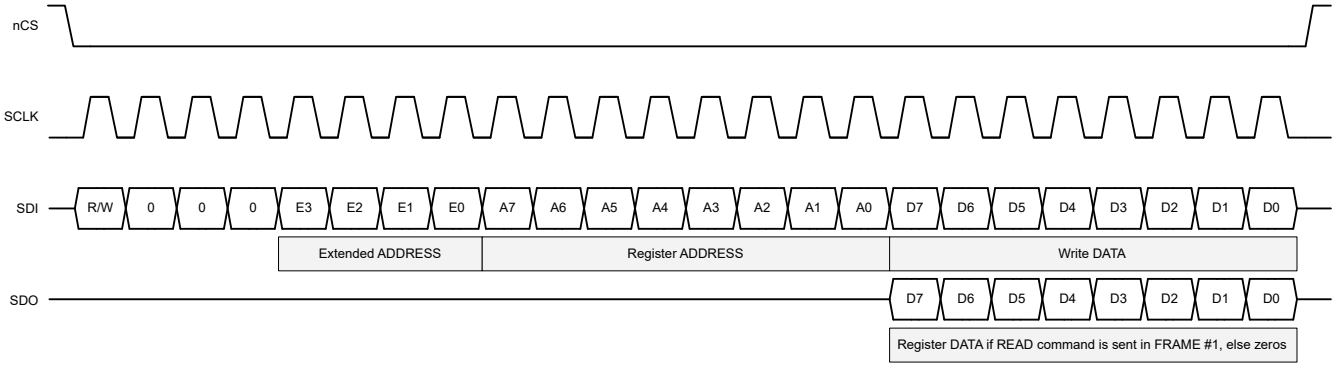


Figure 7-58. TPLD SPI Frame and Formatting

Each SPI transaction is consists of a 1-bit command, a 7-bit extended address, an 8-bit target register address, and an 8-bit data field. The data shifted out on the SDO line contains the data that is stored in the set address with the READ command (R/W = 0). Data bytes shifted out during a WRITE command (R/W = 1) is content of the registers prior to the new data being written.

7.3.15.3 Virtual I/Os

Within the TPLD, this macro-cell has 8 inputs and 8 outputs to allow for reading of up to 8 digital macro-cell outputs and provide up to 8 virtual inputs to be used within the device.

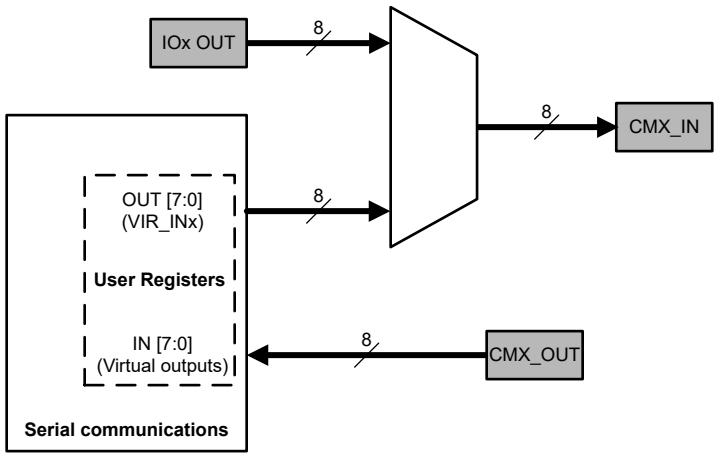


Figure 7-59. Serial Communications Block Diagram

The outputs of this macro-cell act as virtual inputs into the device. The routing of the signal into the Connection Mux is shared with the physical digital input pins, so if a virtual input is used, the digital input pin resource is no longer available and the Connection Mux input is sourced from the Virtual Input register. Table 7-30 shows the shared resource between the digital input pin and the virtual input.

Table 7-30. Digital IO and Virtual In Shared Resources

Virtual input	VIR_IN0	VIR_IN1	VIR_IN2	VIR_IN3	VIR_IN4	VIR_IN5	VIR_IN6	VIR_IN7
Digital input pin	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO9

Using the virtual inputs and virtual outputs, the TPLD can be configured for 8-bit serial-to-parallel GPIO expansion or parallel-to-serial buffering.

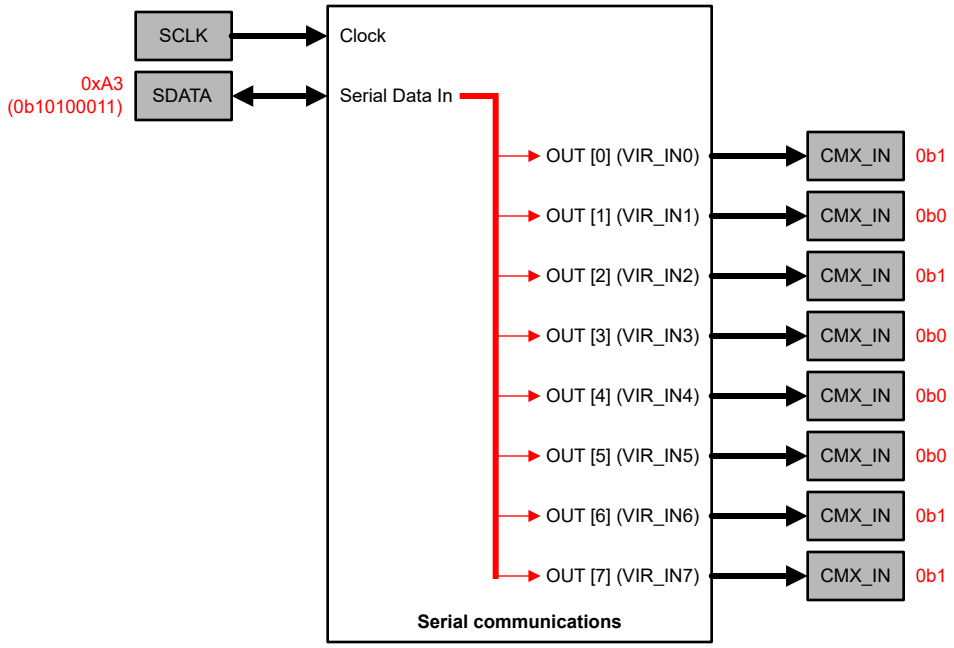


Figure 7-60. Serial Communications for Serial-to-Parallel I/O Expander Block Diagram

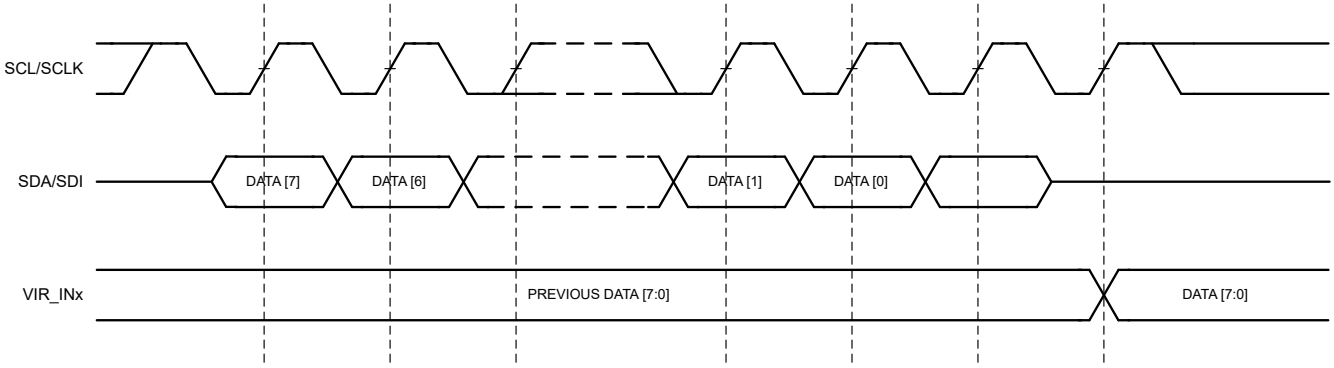


Figure 7-61. Serial Communications for Serial-to-Parallel I/O Expander Timing Example

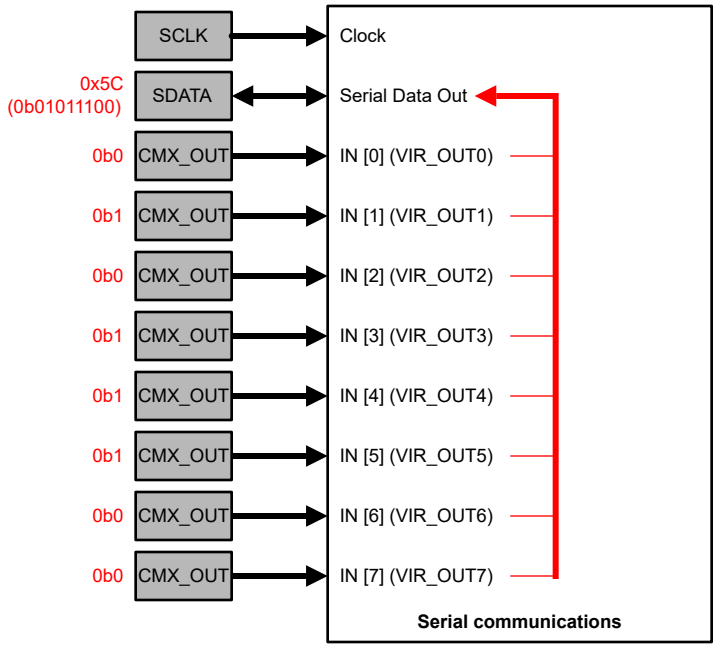


Figure 7-62. Serial Communications for Parallel-to-Serial Block Diagram

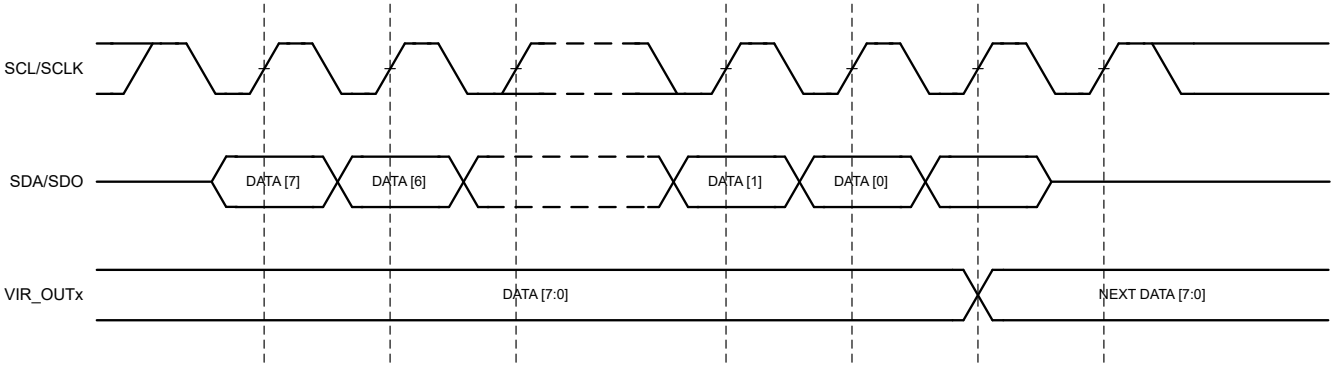


Figure 7-63. Serial Communications for Parallel-to-Serial Timing Example

7.4 Device Functional Modes

7.4.1 Power-On Reset

The TPLD1202 follows a power-on reset (POR) sequence to provide correct device initialization and operation of all macro-cells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{CC} power is ramping up, and also while the V_{CC} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macro-cells inside the device, and finally to the state of the I/O pins.

The POR macro-cell outputs a logic High signal when the device power-on reset sequence is complete, signaling the completion of the device start up. To start the sequence, all outputs are in a high-impedance state and the chip starts loading data from OTP. The reset signal releases for internal macro-cells and all the registers initialize to the configured states. Figure 7-64 shows how the POR system generates a sequence of signals that enable certain macro-cells.

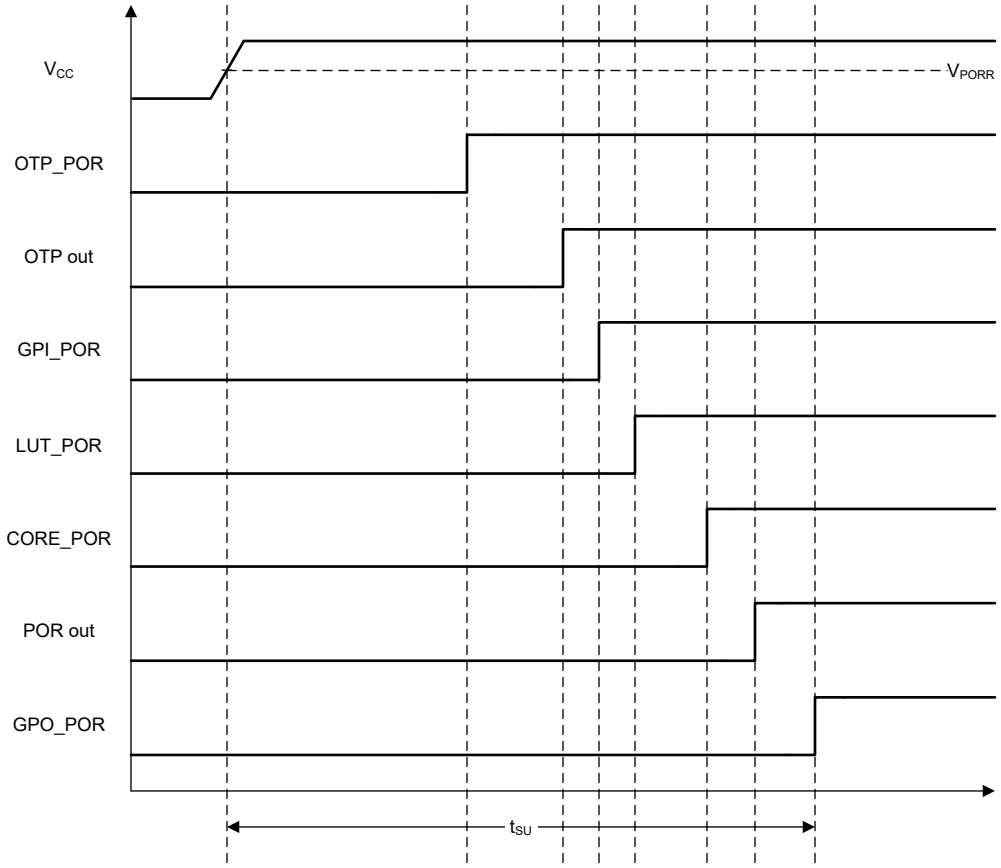


Figure 7-64. POR Sequence

As illustrated in Figure 7-64, after the V_{CC} has start ramping up and crosses the V_{PORR} threshold, that is when V_{CC} > V_{PORR}, macro-cells in the TPLD1202 power on and are forced into a reset state. All outputs are in Hi-Z and the device is initialized according to the following sequence:

- First, the on-device RAM is reset.
- Next the device (TPLD1202) reads the data from OTP, and transfers this information to RAM (registers) that serve to configure each macro-cell, and the connection mux which routes signals between macro-cells.
- The third stage resets and then enables the input pins (GPIOs configured as Inputs).
- After that, the LUTs are reset and become active. After LUTs the Delay cells, OSC, DFFs, Latches and Pipe Delay are initialized.
- After all macro-cells are initialized internal POR signal (POR macro-cell output) goes from Low to High.
- The last portion of the device to be initialized are the output pins (GPIOs configured as Outputs), which transition from high-impedance to active at this point.

Note

The output level of GPOs during the V_{CC} ramp up to time t_{SU} is unpredictable. TI recommends reading the state of outputs only after time t_{SU}.

GPIO quick charge: If enabled, during the POR sequence, a 2kΩ resistor is connected between the GPIO and GND to precondition the GPIO.

Initialization: All internal macro-cells have an initial low-level output by default, unless otherwise configured. During the power-on reset sequence, the reset signal is released for internal macro-cells and initialize according to the following sequence:

- Input pins, analog comparators, pull up/pull down resistors

- LUTs
- DFFs, Delays/Counters, pipe delay
- POR output to matrix
- Output pin corresponds to the internal logic

The POR signal going high indicates the mentioned power-up sequence is complete.

7.4.2 Power Supply Control Modes

The TPLD1202 has the option to control the power mode of the Bandgap Voltage and the Prebias Voltage. TI recommends keeping these bits to 000 (Auto on/off); however, if analog macro-cells (for example, oscillators, analog comparators) are not used, these settings can be used to power off the Bandgap and Prebias Voltages to further reduce the power consumption of the device.

Table 7-31. Bandgap Voltage Power Control Modes

Control code	Bit description
00X	Auto ON for: • Oscillators • Analog Comparators • Voltage Reference • Temperature Sensor • Any Counter/PWM Generator/Watchdog Timer/State Machine not using "External CLK from CMX"
01X	Force ON
1XX	Force OFF

Table 7-32. Prebias Voltage Power Control Modes

Control code	Bit description
000	Auto ON for: • Any active Serial Communications transaction
001	Auto ON for: • Any Pattern Generator/DFF/Shift Register • Any active Serial Communications transaction
010	Auto ON for: • Any Counter/PWM Generator/Watchdog Timer/State Machine including any using "External CLK from CMX" • Any active Serial Communications transaction
011	Force ON
100	Auto ON for: • Oscillators • Any active Serial Communications transaction
101	Auto ON for: • Oscillators • Any Pattern Generator/DFF/Shift Register • Any active Serial Communications transaction
110	Auto ON for: • Any Pattern Generator/DFF/Shift Register • Any Counter/PWM Generator/Watchdog Timer/State Machine including any using "External CLK from CMX" • Any active Serial Communications transaction

Table 7-32. Prebias Voltage Power Control Modes (continued)

Control code	Bit description
111	Force OFF

7.4.3 Protection Features

The TPLD1202 has some protection features including read/write protection for device configuration bits and CRC error detection on the internal OTP.

7.4.3.1 Device Read/Write Lock

The TPLD1202 implements lock features that enables device read-back protection for secure applications and prevents an accidental or unintended write to the TPLD1202 registers. There are three bits in the OTP that allows the user to define rules for reading and writing through the serial communications interface:

- **Configuration register (CFG) read (RD) lock**: the CFG RD lock, if set, blocks all read commands of the configuration registers through the serial communications interface and respond with 0's.
- **Configuration register (CFG) write (WR) lock**: the CFG WR lock, if set, blocks all write commands to the configuration registers through the serial communications interface.
- **User register (USER) lock**: the USER lock consists of two bits and, depending on bit setting, blocks write commands to the user register space through the serial communications interface to specific register addresses and any changes requested is denied (no changes are made to the configuration registers).

Table 7-33. User Register Lock Access Type Enumeration

Register	Lock bits						
	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b00	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b01	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b10	CFG RD lock = 0b0 CFG WR lock = 0b0 USER lock = 0b11	CFG RD lock = 0b1 CFG WR lock = 0b0 USER lock = 0bXX	CFG RD lock = 0b0 CFG WR lock = 0b1 USER lock = 0bXX	CFG RD lock = 0b1 CFG WR lock = 0b1 USER lock = 0bXX
Device ID (0x000 - 0x003)	R	R	R	R	R	R	R
Program ID (0x004 - 0x007)	R	R	R	R	R	R	R
Counter COUNT (0x010 - 0x01F)	R	R	R	R	—	R	—
Counter DATA (0x020 - 0x02F)	R/W	R/W	R	R	—	R/W	—
Watchdog Timer DATA (0x030 - 0x031)	R/W	R/W	R	R	—	R/W	—
Watchdog Timer Status (0x032)	R	R	R	R	—	R	—
Pattern Generator (0x040 - 0x041)	R/W	R/W	R	R	—	R/W	—
State Machine (0x050 - 0x05F)	R/W	R	R/W	R	—	R/W	—

Table 7-33. User Register Lock Access Type Enumeration (continued)

Register	Lock bits						
Voltage Reference select for Analog Comparator (0x070 - 0x07F)	R/W	R	R	R/W	—	R/W	—
Virtual Input (0x0E0)	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Virtual Output (0x0E1)	R	R	R	R	R	R	R
CRC Status (0x0FE)	R	R	R	R	R	R	R
Configuration Registers (0x200 - 0x3FF)	R/W	R/W	R/W	R/W	W	R	—

Any write commands that come to the device via the serial communications interface that are not blocked, based on the protection bits, changes the contents of the configuration register that mirror the OTP bits. These write commands do not change the OTP bits themselves, and a POR event restores the register bits to original programmed contents of the OTP.

7.4.3.2 OTP Cyclic Redundancy Check (CRC)

Cyclic Redundancy Checks (CRCs) is a common method of performing error checking on areas of OTP and verifying data integrity of this memory. OTP is used to configure the macro-cells and connection mux routing of the TPLD1202. The OTP is one-time programmable and holds the device configuration data. OTP memory is loaded during device power up and transferred to TPLD1202 connection mux.

To verify the bit integrity of the OTP memory before the stored configuration is loaded from OTP to device registers, as a safety measure, TPLD1202 implements a cyclic redundancy check (CRC) feature for the OTP to make sure that the data stored in the OTP is uncorrupted. At start-up, the OTP is read internally and checks for a valid CRC. If the CRC is not valid, this process is performed for a total of 7 more times. If still not valid after the 8th attempt, the device proceeds with loading the contents from OTP but sets the following status bits:

CRC_ERR_CNT bits:

The CRC_ERR_CNT bits in register 0x0FEh [7:5] indicate the number of failed CRC attempts before loading the OTP contents into the configuration of the device.

CRC_ERR_FLAG bit:

The CRC_ERR_FLAG bit in register 0x0FEh [0] indicates there are more than 8 CRC calculation failures in the loading of the OTP contents into the configuration of the device.

7.4.4 Programming

The TPLD1202 is programmed through a I^2C or SPI.

In the programmed case for the TPLD1202 device, the configuration choices made by the user are stored as bit settings in the OTP, and this information is transferred at startup time to connection mux registers that enable the configuration of the macro-cells and for setting the connections in the connection mux to route signals in the manner most appropriate for the user's application.

7.4.4.1 Selectable I²C/SPI Interface

In an unprogrammed TPLD1202 device, the Interface Select pin (IO3) is sampled at device power up to determine the interface the TPLD boots up with after t_{SU} (max).

When the pin is tied to GND (logic low) or left floating, the TPLD1202 is configured with I²C interface with the first four bits of the target address determined by the respective HW Addr IO and the next three bits default to 001b, or ADDR = [A6][A5][A4][A3][0][0][1].

When the pin is tied to VCC (logic high), the TPLD1202 is configured with SPI.

In a programmed device (one in which the OTP has been burned), this setting is overwritten by the selection stored in the OTP memory.

I2C_EN	SPI_EN	Interface enabled
0	0	Device is unprogrammed (blank)
0	1	SPI
1	0	I²C
1	1	Neither I2C nor SPI, pins are GPIOs

7.4.4.2 One-Time Programmable Memory (OTP) and Programming Procedure

The TPLD1202 contains one-time programmable (OTP) memory bits. These memory bits retain the set values in the absence of a power supply, are used to configure the TPLD device, and can be programmed a maximum of one time. The default values for all the configuration registers in the TPLD1202 are loaded from OTP after a POR event is issued.

Procedure to temporarily set up configuration registers:

1. After starting up the device with the desired serial communications protocol, read the DEVICE_ID from registers 0x000 and 0x001 to verify communication with the device is established
2. Then:
    a. For SPI, send the following four frames with at least 200µs between frames: 0x9000B9, 0x90003E, 0x9000AF, 0x900058
    b. For I²C, in four write transactions, send the following with at least 500µs between transactions:
        i. Transaction 1: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0xB9
        ii. Transaction 2: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0x3E
        iii. Transaction 3: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0xAF
        iv. Transaction 4: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0x58
3. After the final frame is sent, wait 1ms.
4. Verify the configuration mode has been entered correctly by reading 0x10 from register 0x400.
5. Write 0x02 to register 0x400.
6. Send configuration bits to 0x200 - 0x3FF.
7. Optionally, after sending configuration bits, read commands can be used to verify the correct data was written to the device.
8. Then:
    a. For SPI, send the following frame: 0x90004B
    b. For I²C, send the following write transaction: BYTE0 = ADDR, BYTE1 = 0x01, BYTE2 = 0x4B
9. Lastly, write 0x00 to register 0x400 for the configuration to take effect.
10. Device is now temporarily configured.

Note

When temporarily configuring the TPLD with the I^2C macro-cell enabled, the first four bits of the target address is set to 0000b and the next three bits comes from the configuration bits, or ADDR = [0][0][0][0][A2][A1][A0]. An OTP burn is necessary to change the first four bits, or MSB, of the target address.

To change the temporary configuration, TI recommends power cycling the device and repeating the procedure to temporarily set up the configuration registers.

Procedure to burn the OTP:

1. If the device has been temporarily configured, power cycle the device to clear configuration registers before continuing.
2. Follow steps 1 - 7 from the procedure to temporarily set up configuration registers.
3. Apply V_{PP} to the GPI pin.
4. Write 0x01 to register 0x401 to start the OTP programming.
5. Wait t_{PP} for the programming to be completed.
6. Remove V_{PP} from the GPI pin.
7. Device OTP is now burned.

7.4.4.3 Intel HEX File Format

InterConnect Studio generates the configuration bits in Intel HEX format. The .hex file can be parsed to extract the datastream to configure the TPLD device. The Intel HEX record, or line of text, structure is shown below.

Table 7-34. Record structure example

:	10	0200	00	000102030405060708090A0B0C0D0E0F	76
Start code	Byte count	Address	Record type	Data	Checksum

- **Start code:** one character, an ASCII colon (:).
- **Byte count:** two hex digits to indicate the number of bytes in the Data field.
- **Address:** four hex digits to represent the starting address offset of the first Data byte.
- **Record type:** two hex digits defining the meaning of the Data field. While Intel HEX has six standard record types, only two are used in the .hex file generation.
  - **Hex code 00:** indicates Data record type; the example record structure above results in a Byte count of 0x10 (16 bytes), starting Address of 0x0200, and Data (0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, and 0x0F).
  - **Hex code 01:** indicates an End of File record type; the Byte count is 0x00, the Address is typically 0x0000, and the Data field is omitted.
- **Data:** contains the sequence of *Byte count* bytes of data.
- **Checksum:** two hex digits computed by taking the summation of each byte preceding the Checksum and computing the two's complement of the sum's least significant byte. This value can be used to verify the record has no errors.

8 TPLD1202 Registers

The following section provides the registers accessible in the TPLD1202.

Note

Reads from and writes to the device are asynchronous; thus current counter data can change by the time the read occurs depending on the speed of the clock used for the counter and of the serial communications interface.

Note

When updating counter data, TI recommends putting the counter in reset. If counters are not kept in a reset state, updates to CNT0 to CNT5 do not take affect until the next reset; whereas updates to CNT6 to CNT9 take affect immediately.

After updating the counter data, two clocks are required to re-initialize the counter. If an External Clock option is used, provide the two clocks for proper operation of the counter.

8.1 TPLD1202_User Registers

Table 8-1 lists the memory-mapped registers for the TPLD1202_User registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. TPLD1202_USER Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	DEVICE_ID0	DEVICE_ID_MSB							
1h	DEVICE_ID1	DEVICE_ID_LSB							
2h	DEVICE_ID2	DEVICE_ID_RSVD							
3h	DEVICE_ID3	DEVICE_ID_REV							
4h	PROG_ID0	PROG_ID0							
5h	PROG_ID1	PROG_ID1							
6h	PROG_ID2	PROG_ID2							
7h	PROG_ID3	PROG_ID3							
10h	CNT0_COUNT	CNT0_COUNT							
11h	CNT1_COUNT	CNT1_COUNT							
12h	CNT2_COUNT	CNT2_COUNT							
13h	CNT3_COUNT	CNT3_COUNT							
14h	CNT4_COUNT	CNT4_COUNT							
15h	CNT5_COUNT	CNT5_COUNT							
16h	CNT6_COUNT	CNT6_COUNT							
17h	CNT7_COUNT	CNT7_COUNT							
18h	CNT8_COUNT	CNT8_COUNT							
19h	CNT9_COUNT	CNT9_COUNT							
20h	CNT0_DATA	CNT0_DATA							
21h	CNT1_DATA	CNT1_DATA							
22h	CNT2_DATA	CNT2_DATA							
23h	CNT3_DATA	CNT3_DATA							
24h	CNT4_DATA	CNT4_DATA							
25h	CNT5_DATA	CNT5_DATA							
26h	CNT6_DATA	CNT6_DATA							
27h	CNT7_DATA	CNT7_DATA							
28h	CNT8_DATA	CNT8_DATA							
29h	CNT9_DATA	CNT9_DATA							
30h	WDT_TIMEOUT_DATA	WATCHDOG_TIMEOUT_DATA							
31h	WDT_OUTPUT_DATA	WATCHDOG_OUTPUT_DATA							
32h	WDT_STATUS	RESERVED							WDT_STATUS
40h	PGEN_DATA_LSB	PGEN_DATA_LSB							
41h	PGEN_DATA_MSB	PGEN_DATA_MSB							
50h	STATE_MACHINE	RESERVED					CURRENT_STATE		
51h	STATE0_OUT	STATE0_OUT							
52h	STATE1_OUT	STATE1_OUT							
53h	STATE2_OUT	STATE2_OUT							
54h	STATE3_OUT	STATE3_OUT							
55h	STATE4_OUT	STATE4_OUT							
56h	STATE5_OUT	STATE5_OUT							
57h	STATE6_OUT	STATE6_OUT							
58h	STATE7_OUT	STATE7_OUT							
70h	VREF_McACMP0	RESERVED		VREF_McACMP0					
71h	VREF_McACMP1	RESERVED		VREF_McACMP1					
72h	VREF_McACMP2	RESERVED		VREF_McACMP2					
73h	VREF_McACMP3	RESERVED		VREF_McACMP3					
E0h	VIRTUAL_INPUT	VIRTUAL_IN							
E1h	VIRTUAL_OUTPUT	VIRTUAL_OUT							
FDh	SER_COMM_CFG	RESERVED							ADDR_INC
FEh	CRC_STATUS	ERR_CNT			RESERVED				ERR_FLAG

Table 8-1. TPLD1202_USER Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FFh	SER_COMM_WR_MASK	SER_COMM_WR_MASK							

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. TPLD1202_User Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 DEVICE_ID0 Register (Offset = 0h) [Reset = 12h]

DEVICE_ID0 is shown in Table 8-3.

Return to the Summary Table.

Table 8-3. DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_MSB	R	12h	

8.1.2 DEVICE_ID1 Register (Offset = 1h) [Reset = 02h]

DEVICE_ID1 is shown in Table 8-4.

Return to the Summary Table.

Table 8-4. DEVICE_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_LSB	R	2h	

8.1.3 DEVICE_ID2 Register (Offset = 2h) [Reset = 00h]

DEVICE_ID2 is shown in Table 8-5.

Return to the Summary Table.

Table 8-5. DEVICE_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_RSVD	R	0h	

8.1.4 DEVICE_ID3 Register (Offset = 3h) [Reset = 20h]

DEVICE_ID3 is shown in Table 8-6.

Return to the Summary Table.

Table 8-6. DEVICE_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_REV	R	20h	

8.1.5 PROG_ID0 Register (Offset = 4h) [Reset = X0h]

PROG_ID0 is shown in Table 8-7.

Return to the Summary Table.

Table 8-7. PROG_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PROG_ID0	R	Xh	

8.1.6 PROG_ID1 Register (Offset = 5h) [Reset = X0h]

PROG_ID1 is shown in Table 8-8.

Return to the Summary Table.

Table 8-8. PROG_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PROG_ID1	R	Xh	

8.1.7 PROG_ID2 Register (Offset = 6h) [Reset = X0h]

PROG_ID2 is shown in Table 8-9.

Return to the Summary Table.

Table 8-9. PROG_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PROG_ID2	R	Xh	

8.1.8 PROG_ID3 Register (Offset = 7h) [Reset = X0h]

PROG_ID3 is shown in Table 8-10.

Return to the Summary Table.

Table 8-10. PROG_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PROG_ID3	R	Xh	

8.1.9 CNT0_COUNT Register (Offset = 10h) [Reset = X0h]

CNT0_COUNT is shown in Table 8-11.

Return to the Summary Table.

Table 8-11. CNT0_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT0_COUNT	R	Xh	

8.1.10 CNT1_COUNT Register (Offset = 11h) [Reset = X0h]

CNT1_COUNT is shown in Table 8-12.

Return to the Summary Table.

Table 8-12. CNT1_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT1_COUNT	R	Xh	

8.1.11 CNT2_COUNT Register (Offset = 12h) [Reset = X0h]

CNT2_COUNT is shown in Table 8-13.

Return to the Summary Table.

Table 8-13. CNT2_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT2_COUNT	R	Xh	

8.1.12 CNT3_COUNT Register (Offset = 13h) [Reset = X0h]

CNT3_COUNT is shown in Table 8-14.

Return to the Summary Table.

Table 8-14. CNT3_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT3_COUNT	R	Xh	

8.1.13 CNT4_COUNT Register (Offset = 14h) [Reset = X0h]

CNT4_COUNT is shown in Table 8-15.

Return to the Summary Table.

Table 8-15. CNT4_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT4_COUNT	R	Xh	

8.1.14 CNT5_COUNT Register (Offset = 15h) [Reset = X0h]

CNT5_COUNT is shown in Table 8-16.

Return to the Summary Table.

Table 8-16. CNT5_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT5_COUNT	R	Xh	

8.1.15 CNT6_COUNT Register (Offset = 16h) [Reset = X0h]

CNT6_COUNT is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. CNT6_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT6_COUNT	R	Xh	

8.1.16 CNT7_COUNT Register (Offset = 17h) [Reset = X0h]

CNT7_COUNT is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. CNT7_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT7_COUNT	R	Xh	

8.1.17 CNT8_COUNT Register (Offset = 18h) [Reset = X0h]

CNT8_COUNT is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. CNT8_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT8_COUNT	R	Xh	

8.1.18 CNT9_COUNT Register (Offset = 19h) [Reset = X0h]

CNT9_COUNT is shown in Table 8-20.

Return to the Summary Table.

Table 8-20. CNT9_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT9_COUNT	R	Xh	

8.1.19 CNT0_DATA Register (Offset = 20h) [Reset = X0h]

CNT0_DATA is shown in Table 8-21.

Return to the Summary Table.

Table 8-21. CNT0_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT0_DATA	R/W	Xh	

8.1.20 CNT1_DATA Register (Offset = 21h) [Reset = X0h]

CNT1_DATA is shown in Table 8-22.

Return to the Summary Table.

Table 8-22. CNT1_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT1_DATA	R/W	Xh	

8.1.21 CNT2_DATA Register (Offset = 22h) [Reset = X0h]

CNT2_DATA is shown in Table 8-23.

Return to the Summary Table.

Table 8-23. CNT2_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT2_DATA	R/W	Xh	

8.1.22 CNT3_DATA Register (Offset = 23h) [Reset = X0h]

CNT3_DATA is shown in Table 8-24.

Return to the Summary Table.

Table 8-24. CNT3_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT3_DATA	R/W	Xh	

8.1.23 CNT4_DATA Register (Offset = 24h) [Reset = X0h]

CNT4_DATA is shown in Table 8-25.

Return to the Summary Table.

Table 8-25. CNT4_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT4_DATA	R/W	Xh	

8.1.24 CNT5_DATA Register (Offset = 25h) [Reset = X0h]

CNT5_DATA is shown in Table 8-26.

Return to the Summary Table.

Table 8-26. CNT5_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT5_DATA	R/W	Xh	

8.1.25 CNT6_DATA Register (Offset = 26h) [Reset = X0h]

CNT6_DATA is shown in Table 8-27.

Return to the Summary Table.

Table 8-27. CNT6_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT6_DATA	R/W	Xh	

8.1.26 CNT7_DATA Register (Offset = 27h) [Reset = X0h]

CNT7_DATA is shown in Table 8-28.

Return to the Summary Table.

Table 8-28. CNT7_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT7_DATA	R/W	Xh	

8.1.27 CNT8_DATA Register (Offset = 28h) [Reset = X0h]

CNT8_DATA is shown in Table 8-29.

Return to the Summary Table.

Table 8-29. CNT8_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT8_DATA	R/W	Xh	

8.1.28 CNT9_DATA Register (Offset = 29h) [Reset = X0h]

CNT9_DATA is shown in Table 8-30.

Return to the Summary Table.

Table 8-30. CNT9_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT9_DATA	R/W	Xh	

8.1.29 WDT_TIMEOUT_DATA Register (Offset = 30h) [Reset = X0h]

WDT_TIMEOUT_DATA is shown in Table 8-31.

Return to the Summary Table.

Table 8-31. WDT_TIMEOUT_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WATCHDOG_TIMEOUT_DATA	R/W	Xh	

8.1.30 WDT_OUTPUT_DATA Register (Offset = 31h) [Reset = X0h]

WDT_OUTPUT_DATA is shown in Table 8-32.

Return to the Summary Table.

Table 8-32. WDT_OUTPUT_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WATCHDOG_OUTPUT_DATA	R/W	Xh	

8.1.31 WDT_STATUS Register (Offset = 32h) [Reset = X0h]

WDT_STATUS is shown in Table 8-33.

Return to the Summary Table.

Table 8-33. WDT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	WDT_STATUS	R/W	Xh	Watchdog fault output

8.1.32 PGEN_DATA_LSB Register (Offset = 40h) [Reset = X0h]

PGEN_DATA_LSB is shown in Table 8-34.

Return to the Summary Table.

Table 8-34. PGEN_DATA_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_LSB	R/W	Xh	

8.1.33 PGEN_DATA_MSB Register (Offset = 41h) [Reset = X0h]

PGEN_DATA_MSB is shown in Table 8-35.

Return to the Summary Table.

Table 8-35. PGEN_DATA_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_MSB	R/W	Xh	

8.1.34 STATE_MACHINE Register (Offset = 50h) [Reset = X0h]

STATE_MACHINE is shown in Table 8-36.

Return to the Summary Table.

Table 8-36. STATE_MACHINE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0h	Reserved
2:0	CURRENT_STATE	R	Xh	

8.1.35 STATE0_OUT Register (Offset = 51h) [Reset = X0h]

STATE0_OUT is shown in Table 8-37.

Return to the Summary Table.

Table 8-37. STATE0_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE0_OUT	R/W	Xh	

8.1.36 STATE1_OUT Register (Offset = 52h) [Reset = X0h]

STATE1_OUT is shown in Table 8-38.

Return to the Summary Table.

Table 8-38. STATE1_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE1_OUT	R/W	Xh	

8.1.37 STATE2_OUT Register (Offset = 53h) [Reset = X0h]

STATE2_OUT is shown in Table 8-39.

Return to the Summary Table.

Table 8-39. STATE2_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE2_OUT	R/W	Xh	

8.1.38 STATE3_OUT Register (Offset = 54h) [Reset = X0h]

STATE3_OUT is shown in Table 8-40.

Return to the Summary Table.

Table 8-40. STATE3_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE3_OUT	R/W	Xh	

8.1.39 STATE4_OUT Register (Offset = 55h) [Reset = X0h]

STATE4_OUT is shown in Table 8-41.

Return to the Summary Table.

Table 8-41. STATE4_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE4_OUT	R/W	Xh	

8.1.40 STATE5_OUT Register (Offset = 56h) [Reset = X0h]

STATE5_OUT is shown in Table 8-42.

Return to the Summary Table.

Table 8-42. STATE5_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE5_OUT	R/W	Xh	

8.1.41 STATE6_OUT Register (Offset = 57h) [Reset = X0h]

STATE6_OUT is shown in Table 8-43.

Return to the Summary Table.

Table 8-43. STATE6_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE6_OUT	R/W	Xh	

8.1.42 STATE7_OUT Register (Offset = 58h) [Reset = X0h]

STATE7_OUT is shown in Table 8-44.

Return to the Summary Table.

Table 8-44. STATE7_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STATE7_OUT	R/W	Xh	

8.1.43 VREF_McACMP0 Register (Offset = 70h) [Reset = X0h]

VREF_McACMP0 is shown in Table 8-45.

Return to the Summary Table.

Table 8-45. VREF_McACMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP0	R/W	Xh	

8.1.44 VREF_McACMP1 Register (Offset = 71h) [Reset = X0h]

VREF_McACMP1 is shown in Table 8-46.

Return to the Summary Table.

Table 8-46. VREF_McACMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP1	R/W	Xh	

8.1.45 VREF_McACMP2 Register (Offset = 72h) [Reset = X0h]

VREF_McACMP2 is shown in Table 8-47.

Return to the Summary Table.

Table 8-47. VREF_McACMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP2	R/W	Xh	

8.1.46 VREF_McACMP3 Register (Offset = 73h) [Reset = X0h]

VREF_McACMP3 is shown in Table 8-48.

Return to the Summary Table.

Table 8-48. VREF_McACMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_McACMP3	R/W	Xh	

8.1.47 VIRTUAL_INPUT Register (Offset = E0h) [Reset = X0h]

VIRTUAL_INPUT is shown in Table 8-49.

Return to the Summary Table.

Table 8-49. VIRTUAL_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VIRTUAL_IN	R/W	Xh	

8.1.48 VIRTUAL_OUTPUT Register (Offset = E1h) [Reset = X0h]

VIRTUAL_OUTPUT is shown in Table 8-50.

Return to the Summary Table.

Table 8-50. VIRTUAL_OUTPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VIRTUAL_OUT	R	Xh	

8.1.49 SER_COMM_CFG Register (Offset = FDh) [Reset = X0h]

SER_COMM_CFG is shown in Table 8-51.

Return to the Summary Table.

Table 8-51. SER_COMM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	ADDR_INC	R/W	Xh	Address auto-incrementing disable select 0h = Enabled 1h = Disabled

8.1.50 CRC_STATUS Register (Offset = FEh) [Reset = X0h]

CRC_STATUS is shown in Table 8-52.

Return to the Summary Table.

Table 8-52. CRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	ERR_CNT	R	0h	
4:1	RESERVED	R	0h	Reserved
0	ERR_FLAG	R/W	Xh	

8.1.51 SER_COMM_WR_MASK Register (Offset = FFh) [Reset = X0h]

SER_COMM_WR_MASK is shown in Table 8-53.

Return to the Summary Table.

Table 8-53. SER_COMM_WR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SER_COMM_WR_MASK	R/W	Xh	

8.2 TPLD1202_Cfg_0 Registers

Table 8-54 lists the memory-mapped registers for the TPLD1202_Cfg_0 registers. All register offset addresses not listed in Table 8-54 should be considered as reserved locations and the register contents should not be modified.

Table 8-54. TPLD1202_CFG_0 Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
200h	CMX_0	RESERVED		IO1_DOUT_CMX					
201h	CMX_1	RESERVED		IO2_DOUT_CMX					
202h	CMX_2	RESERVED		IO3_DOUT_CMX					
203h	CMX_3	RESERVED		IO3_OE_CMX					
204h	CMX_4	RESERVED		IO4_DOUT_CMX					
205h	CMX_5	RESERVED		IO4_OE_CMX					
206h	CMX_6	RESERVED		IO5_DOUT_CMX					
207h	CMX_7	RESERVED		IO6_DOUT_CMX					
208h	CMX_8	RESERVED		IO7_DOUT_CMX					
209h	CMX_9	RESERVED		IO8_DOUT_CMX					
20Ah	CMX_10	RESERVED		IO8_OE_CMX					
20Bh	CMX_11	RESERVED		IO9_DOUT_CMX					
20Ch	CMX_12	RESERVED		IO9_OE_CMX					
20Dh	CMX_13	RESERVED		LUT2_0_IN0_/_DFF_CLK_IN_CMX					
20Eh	CMX_14	RESERVED		LUT2_0_IN1_/_DFF_D_IN_CMX					
20Fh	CMX_15	RESERVED		LUT2_1_IN0_/_DFF_CLK_IN_CMX					
210h	CMX_16	RESERVED		LUT2_1_IN1_/_DFF_D_IN_CMX					
211h	CMX_17	RESERVED		LUT2_2_IN0_/_PGEN_CLK_IN_CMX					
212h	CMX_18	RESERVED		LUT2_2_IN1_/_PGEN_RST_IN_CMX					
213h	CMX_19	RESERVED		LUT3_0_IN0_/_DFF_CLK_IN_CMX					
214h	CMX_20	RESERVED		LUT3_0_IN1_/_DFF_D_IN_CMX					
215h	CMX_21	RESERVED		LUT3_0_IN2_/_DFF_RST_IN_CMX					
216h	CMX_22	RESERVED		LUT3_1_IN0_/_DFF_CLK_IN_CMX					
217h	CMX_23	RESERVED		LUT3_1_IN1_/_DFF_D_IN_CMX					
218h	CMX_24	RESERVED		LUT3_1_IN2_/_DFF_RST_IN_CMX					
219h	CMX_25	RESERVED		LUT3_2_IN0_/_DFF_CLK_IN_CMX					
21Ah	CMX_26	RESERVED		LUT3_2_IN1_/_DFF_D_IN_CMX					
21Bh	CMX_27	RESERVED		LUT3_2_IN2_/_DFF_RST_IN_CMX					
21Ch	CMX_28	RESERVED		LUT3_3_IN0_/_DFF_CLK_IN_CMX					
21Dh	CMX_29	RESERVED		LUT3_3_IN1_/_DFF_D_IN_CMX					
21Eh	CMX_30	RESERVED		LUT3_3_IN2_/_DFF_RST_IN_CMX					
21Fh	CMX_31	RESERVED		LUT3_4_IN0_/_DFF/SR_CLK_IN_CMX					
220h	CMX_32	RESERVED		LUT3_4_IN1_/_DFF/SR_D_IN_CMX					
221h	CMX_33	RESERVED		LUT3_4_IN2_/_DFF/SR_RST_IN_CMX					
222h	CMX_34	RESERVED		LUT3_5_IN0_/_DFF/SR_CLK_IN_CMX					
223h	CMX_35	RESERVED		LUT3_5_IN1_/_DFF/SR_D_IN_CMX					
224h	CMX_36	RESERVED		LUT3_5_IN2_/_DFF/SR_RST_IN_CMX					
225h	CMX_37	RESERVED		LUT3_6_IN0_/_DFF/SR_CLK_IN_CMX					
226h	CMX_38	RESERVED		LUT3_6_IN1_/_DFF/SR_D_IN_CMX					
227h	CMX_39	RESERVED		LUT3_6_IN2_/_DFF/SR_RST_IN_CMX					
228h	CMX_40	RESERVED		LUT3_7_IN0_/_DFF/SR_CLK_IN_CMX					
229h	CMX_41	RESERVED		LUT3_7_IN1_/_DFF/SR_D_IN_CMX					
22Ah	CMX_42	RESERVED		LUT3_7_IN2_/_DFF/SR_RST_IN_CMX					
22Bh	CMX_43	RESERVED		LUT3_8_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX					
22Ch	CMX_44	RESERVED		LUT3_8_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX					
22Dh	CMX_45	RESERVED		LUT3_8_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX					
22Eh	CMX_46	RESERVED		LUT3_9_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX					
22Fh	CMX_47	RESERVED		LUT3_9_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX					
230h	CMX_48	RESERVED		LUT3_9_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX					

Table 8-54. TPLD1202_CFG_0 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
231h	CMX_49	RESERVED		LUT3_10_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX					
232h	CMX_50	RESERVED		LUT3_10_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX					
233h	CMX_51	RESERVED		LUT3_10_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX					
234h	CMX_52	RESERVED		LUT3_11_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX					
235h	CMX_53	RESERVED		LUT3_11_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX					
236h	CMX_54	RESERVED		LUT3_11_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX					
237h	CMX_55	RESERVED		LUT3_12_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX					
238h	CMX_56	RESERVED		LUT3_12_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX					
239h	CMX_57	RESERVED		LUT3_12_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX					
23Ah	CMX_58	RESERVED		LUT3_13_IN0_/_DFF_CLK_IN_OR_LDC_IN0_CMX					
23Bh	CMX_59	RESERVED		LUT3_13_IN1_/_DFF_D_IN_OR_LDC_IN1_CMX					
23Ch	CMX_60	RESERVED		LUT3_13_IN2_/_DFF_RST_IN_OR_LDC_IN2_CMX					
23Dh	CMX_61	RESERVED		LUT4_0_IN0_/_DFF_CLK_IN_CMX					
23Eh	CMX_62	RESERVED		LUT4_0_IN1_/_DFF_D_IN_CMX					
23Fh	CMX_63	RESERVED		LUT4_0_IN2_/_RST_IN_CMX					
240h	CMX_64	RESERVED		LUT4_0_IN3__CMX					
241h	CMX_65	RESERVED		PFLT_IN_CMX					
242h	CMX_66	RESERVED		FLT/EDET_IN_CMX					
243h	CMX_67	RESERVED		SM_ST0_EN0_CMX					
244h	CMX_68	RESERVED		SM_ST0_EN1_CMX					
245h	CMX_69	RESERVED		SM_ST1_EN0_CMX					
246h	CMX_70	RESERVED		SM_ST1_EN1_CMX					
247h	CMX_71	RESERVED		SM_ST2_EN0_CMX					
248h	CMX_72	RESERVED		SM_ST2_EN1_CMX					
249h	CMX_73	RESERVED		SM_ST3_EN0_CMX					
24Ah	CMX_74	RESERVED		SM_ST3_EN1_CMX					
24Bh	CMX_75	RESERVED		SM_ST4_EN0_/_PWM_GEN3_PUP_CMX					
24Ch	CMX_76	RESERVED		SM_ST4_EN1_CMX					
24Dh	CMX_77	RESERVED		SM_ST5_EN0_/_PWM_GEN2_PUP_CMX					
24Eh	CMX_78	RESERVED		SM_ST5_EN1_CMX					
24Fh	CMX_79	RESERVED		SM_ST6_EN0_/_PWM_GEN1_PUP_CMX					
250h	CMX_80	RESERVED		SM_ST6_EN1_CMX					
251h	CMX_81	RESERVED		SM_ST7_EN0_/_PWM_GEN0_PUP_CMX					
252h	CMX_82	RESERVED		SM_ST7_EN1_CMX					
253h	CMX_83	RESERVED		SM_CLK_IN_CMX					
254h	CMX_84	RESERVED		SM_RST_IN_CMX					
255h	CMX_85	RESERVED		McACMP_ENABLE_CMX					
256h	CMX_86	RESERVED		McACMP_RST_CMX					
257h	CMX_87	RESERVED		OSC0_PWR_DOWN_CMX					
258h	CMX_88	RESERVED		OSC1_PWR_DOWN_CMX					
259h	CMX_89	RESERVED		CNT6/FSM_IN_CMX					
25Ah	CMX_90	RESERVED		CNT6/FSM_UP_CMX					
25Bh	CMX_91	RESERVED		CNT6/FSM_KEEP_CMX					
25Ch	CMX_92	RESERVED		CNT6/FSM_CLK_IN_CMX					
25Dh	CMX_93	RESERVED		CNT7/FSM_IN_CMX					
25Eh	CMX_94	RESERVED		CNT7/FSM_UP_CMX					
25Fh	CMX_95	RESERVED		CNT7/FSM_KEEP_CMX					
260h	CMX_96	RESERVED		CNT7/FSM_CLK_IN_CMX					
261h	CMX_97	RESERVED		CNT8/FSM_IN_CMX					
262h	CMX_98	RESERVED		CNT8/FSM_UP_CMX					
263h	CMX_99	RESERVED		CNT8/FSM_KEEP_CMX					
264h	CMX_100	RESERVED		CNT8/FSM_CLK_IN_CMX					
265h	CMX_101	RESERVED		CNT9/FSM_IN_/_WDT_IN_CMX					
266h	CMX_102	RESERVED		CNT9/FSM_UP_/_WDT_EN_CMX					
267h	CMX_103	RESERVED		CNT9/FSM_KEEP_CMX					

Table 8-54. TPLD1202_CFG_0 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
268h	CMX_104	RESERVED		CNT9/FSM_CLK_IN_CMX					
269h	CMX_105	RESERVED		VIRTUAL_OUT0_CMX					
26Ah	CMX_106	RESERVED		VIRTUAL_OUT1_CMX					
26Bh	CMX_107	RESERVED		VIRTUAL_OUT2_CMX					
26Ch	CMX_108	RESERVED		VIRTUAL_OUT3_CMX					
26Dh	CMX_109	RESERVED		VIRTUAL_OUT4_CMX					
26Eh	CMX_110	RESERVED		VIRTUAL_OUT5_CMX					
26Fh	CMX_111	RESERVED		VIRTUAL_OUT6_CMX					
270h	CMX_112	RESERVED		VIRTUAL_OUT7_CMX					

Complex bit access types are encoded to fit into small table cells. Table 8-55 shows the codes that are used for access types in this section.

Table 8-55. TPLD1202_Cfg_0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 CMX_0 Register (Offset = 200h) [Reset = X0h]

CMX_0 is shown in Table 8-56.

Return to the Summary Table.

Table 8-56. CMX_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-56. CMX_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	IO1_DOUT_CMX	R/W	Xh	0h = GND 1h = IN0 DIN 2h = IO1 / V_IN0 DIN 3h = IO2 / V_IN1 DIN 4h = IO3 / V_IN2 DIN 5h = IO4 / V_IN3 DIN 6h = IO5 / V_IN4 DIN 7h = IO6 / V_IN5 DIN 8h = IO7 / V_IN6 DIN 9h = IO8 DIN Ah = IO9 / V_IN7 DIN Bh = LUT2_0 OUT Ch = LUT2_1 OUT Dh = LUT2_2 OUT Eh = LUT3_0 OUT Fh = LUT3_1 OUT 10h = LUT3_2 OUT 11h = LUT3_3 OUT 12h = LUT3_4 OUT 13h = LUT3_5 OUT 14h = LUT3_6 OUT 15h = LUT3_7 OUT 16h = LUT3_8 / LDC OUT 17h = LUT3_9 / LDC OUT 18h = LUT3_10 / LDC OUT 19h = LUT3_11 / LDC OUT 1Ah = LUT3_12 / LDC OUT 1Bh = LUT3_13 / LDC OUT 1Ch = LUT4_0 OUT 1Dh = PFLT OUT 1Eh = FLT / EDET OUT 1Fh = SM OUT0 / PWM GEN3 OUTP 20h = SM OUT1 / PWM GEN3 OUTN 21h = SM OUT2 / PWM GEN2 OUTP 22h = SM OUT3 / PWM GEN2 OUTN 23h = SM OUT4 / PWM GEN1 OUTP 24h = SM OUT5 / PWM GEN1 OUTN 25h = SM OUT6 / PWM GEN0 OUTP 26h = SM OUT7 / PWM GEN0 OUTN 27h = McACMP OUT0 28h = McACMP OUT1 29h = McACMP OUT2 2Ah = McACMP OUT3 2Bh = McACMP DATA RDY 2Ch = OSC0 OUT0 2Dh = OSC0 OUT1 2Eh = OSC1 OUT 2Fh = CNT6 OUT 30h = CNT7 OUT 31h = CNT8 OUT 32h = CNT9 OUT / WDT OUT 33h = POR OUT 34h = Reserved 35h = Reserved 36h = Reserved 37h = Reserved 38h = Reserved 39h = Reserved 3Ah = Reserved 3Bh = Reserved 3Ch = Reserved 3Dh = Reserved 3Eh = Reserved 3Fh = VCC

8.2.2 CMX_1 Register (Offset = 201h) [Reset = X0h]

CMX_1 is shown in Table 8-57.

Return to the Summary Table.

Table 8-57. CMX_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO2_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.3 CMX_2 Register (Offset = 202h) [Reset = X0h]

CMX_2 is shown in Table 8-58.

Return to the Summary Table.

Table 8-58. CMX_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO3_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.4 CMX_3 Register (Offset = 203h) [Reset = X0h]

CMX_3 is shown in Table 8-59.

Return to the Summary Table.

Table 8-59. CMX_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO3_OE_CMX	R/W	Xh	Same options as CMX_0

8.2.5 CMX_4 Register (Offset = 204h) [Reset = X0h]

CMX_4 is shown in Table 8-60.

Return to the Summary Table.

Table 8-60. CMX_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO4_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.6 CMX_5 Register (Offset = 205h) [Reset = X0h]

CMX_5 is shown in Table 8-61.

Return to the Summary Table.

Table 8-61. CMX_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO4_OE_CMX	R/W	Xh	Same options as CMX_0

8.2.7 CMX_6 Register (Offset = 206h) [Reset = X0h]

CMX_6 is shown in Table 8-62.

Return to the Summary Table.

Table 8-62. CMX_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO5_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.8 CMX_7 Register (Offset = 207h) [Reset = X0h]

CMX_7 is shown in Table 8-63.

Return to the Summary Table.

Table 8-63. CMX_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO6_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.9 CMX_8 Register (Offset = 208h) [Reset = X0h]

CMX_8 is shown in Table 8-64.

Return to the Summary Table.

Table 8-64. CMX_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO7_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.10 CMX_9 Register (Offset = 209h) [Reset = X0h]

CMX_9 is shown in Table 8-65.

Return to the Summary Table.

Table 8-65. CMX_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO8_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.11 CMX_10 Register (Offset = 20Ah) [Reset = X0h]

CMX_10 is shown in Table 8-66.

Return to the Summary Table.

Table 8-66. CMX_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO8_OE_CMX	R/W	Xh	Same options as CMX_0

8.2.12 CMX_11 Register (Offset = 20Bh) [Reset = X0h]

CMX_11 is shown in Table 8-67.

Return to the Summary Table.

Table 8-67. CMX_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO9_DOUT_CMX	R/W	Xh	Same options as CMX_0

8.2.13 CMX_12 Register (Offset = 20Ch) [Reset = X0h]

CMX_12 is shown in Table 8-68.

Return to the Summary Table.

Table 8-68. CMX_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	IO9_OE_CMX	R/W	Xh	Same options as CMX_0

8.2.14 CMX_13 Register (Offset = 20Dh) [Reset = X0h]

CMX_13 is shown in Table 8-69.

Return to the Summary Table.

Table 8-69. CMX_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT2_0_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.15 CMX_14 Register (Offset = 20Eh) [Reset = X0h]

CMX_14 is shown in Table 8-70.

Return to the Summary Table.

Table 8-70. CMX_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT2_0_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.16 CMX_15 Register (Offset = 20Fh) [Reset = X0h]

CMX_15 is shown in Table 8-71.

Return to the Summary Table.

Table 8-71. CMX_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT2_1_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.17 CMX_16 Register (Offset = 210h) [Reset = X0h]

CMX_16 is shown in Table 8-72.

Return to the Summary Table.

Table 8-72. CMX_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT2_1_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.18 CMX_17 Register (Offset = 211h) [Reset = X0h]

CMX_17 is shown in Table 8-73.

Return to the Summary Table.

Table 8-73. CMX_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-73. CMX_17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	LUT2_2_IN0_/ _PGEN_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.19 CMX_18 Register (Offset = 212h) [Reset = X0h]

CMX_18 is shown in Table 8-74.

Return to the Summary Table.

Table 8-74. CMX_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT2_2_IN1_/ _PGEN_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.20 CMX_19 Register (Offset = 213h) [Reset = X0h]

CMX_19 is shown in Table 8-75.

Return to the Summary Table.

Table 8-75. CMX_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_0_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.21 CMX_20 Register (Offset = 214h) [Reset = X0h]

CMX_20 is shown in Table 8-76.

Return to the Summary Table.

Table 8-76. CMX_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_0_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.22 CMX_21 Register (Offset = 215h) [Reset = X0h]

CMX_21 is shown in Table 8-77.

Return to the Summary Table.

Table 8-77. CMX_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_0_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.23 CMX_22 Register (Offset = 216h) [Reset = X0h]

CMX_22 is shown in Table 8-78.

Return to the Summary Table.

Table 8-78. CMX_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-78. CMX_22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	LUT3_1_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.24 CMX_23 Register (Offset = 217h) [Reset = X0h]

CMX_23 is shown in Table 8-79.

Return to the Summary Table.

Table 8-79. CMX_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_1_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.25 CMX_24 Register (Offset = 218h) [Reset = X0h]

CMX_24 is shown in Table 8-80.

Return to the Summary Table.

Table 8-80. CMX_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_1_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.26 CMX_25 Register (Offset = 219h) [Reset = X0h]

CMX_25 is shown in Table 8-81.

Return to the Summary Table.

Table 8-81. CMX_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_2_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.27 CMX_26 Register (Offset = 21Ah) [Reset = X0h]

CMX_26 is shown in Table 8-82.

Return to the Summary Table.

Table 8-82. CMX_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_2_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.28 CMX_27 Register (Offset = 21Bh) [Reset = X0h]

CMX_27 is shown in Table 8-83.

Return to the Summary Table.

Table 8-83. CMX_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-83. CMX_27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	LUT3_2_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.29 CMX_28 Register (Offset = 21Ch) [Reset = X0h]

CMX_28 is shown in Table 8-84.

Return to the Summary Table.

Table 8-84. CMX_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_3_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.30 CMX_29 Register (Offset = 21Dh) [Reset = X0h]

CMX_29 is shown in Table 8-85.

Return to the Summary Table.

Table 8-85. CMX_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_3_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.31 CMX_30 Register (Offset = 21Eh) [Reset = X0h]

CMX_30 is shown in Table 8-86.

Return to the Summary Table.

Table 8-86. CMX_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_3_IN2_/_DFF_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.32 CMX_31 Register (Offset = 21Fh) [Reset = X0h]

CMX_31 is shown in Table 8-87.

Return to the Summary Table.

Table 8-87. CMX_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_4_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.33 CMX_32 Register (Offset = 220h) [Reset = X0h]

CMX_32 is shown in Table 8-88.

Return to the Summary Table.

Table 8-88. CMX_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-88. CMX_32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	LUT3_4_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.34 CMX_33 Register (Offset = 221h) [Reset = X0h]

CMX_33 is shown in Table 8-89.

Return to the Summary Table.

Table 8-89. CMX_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_4_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.35 CMX_34 Register (Offset = 222h) [Reset = X0h]

CMX_34 is shown in Table 8-90.

Return to the Summary Table.

Table 8-90. CMX_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_5_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.36 CMX_35 Register (Offset = 223h) [Reset = X0h]

CMX_35 is shown in Table 8-91.

Return to the Summary Table.

Table 8-91. CMX_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_5_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.37 CMX_36 Register (Offset = 224h) [Reset = X0h]

CMX_36 is shown in Table 8-92.

Return to the Summary Table.

Table 8-92. CMX_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_5_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.38 CMX_37 Register (Offset = 225h) [Reset = X0h]

CMX_37 is shown in Table 8-93.

Return to the Summary Table.

Table 8-93. CMX_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_6_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.39 CMX_38 Register (Offset = 226h) [Reset = X0h]

CMX_38 is shown in Table 8-94.

Return to the Summary Table.

Table 8-94. CMX_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_6_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.40 CMX_39 Register (Offset = 227h) [Reset = X0h]

CMX_39 is shown in Table 8-95.

Return to the Summary Table.

Table 8-95. CMX_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_6_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.41 CMX_40 Register (Offset = 228h) [Reset = X0h]

CMX_40 is shown in Table 8-96.

Return to the Summary Table.

Table 8-96. CMX_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_7_IN0_/_DFF/ SR_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.42 CMX_41 Register (Offset = 229h) [Reset = X0h]

CMX_41 is shown in Table 8-97.

Return to the Summary Table.

Table 8-97. CMX_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_7_IN1_/_DFF/ SR_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.43 CMX_42 Register (Offset = 22Ah) [Reset = X0h]

CMX_42 is shown in Table 8-98.

Return to the Summary Table.

Table 8-98. CMX_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_7_IN2_/_DFF/ SR_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.44 CMX_43 Register (Offset = 22Bh) [Reset = X0h]

CMX_43 is shown in Table 8-99.

Return to the Summary Table.

Table 8-99. CMX_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_8_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

8.2.45 CMX_44 Register (Offset = 22Ch) [Reset = X0h]

CMX_44 is shown in Table 8-100.

Return to the Summary Table.

Table 8-100. CMX_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_8_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

8.2.46 CMX_45 Register (Offset = 22Dh) [Reset = X0h]

CMX_45 is shown in Table 8-101.

Return to the Summary Table.

Table 8-101. CMX_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_8_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

8.2.47 CMX_46 Register (Offset = 22Eh) [Reset = X0h]

CMX_46 is shown in Table 8-102.

Return to the Summary Table.

Table 8-102. CMX_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_9_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

8.2.48 CMX_47 Register (Offset = 22Fh) [Reset = X0h]

CMX_47 is shown in Table 8-103.

Return to the Summary Table.

Table 8-103. CMX_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_9_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

8.2.49 CMX_48 Register (Offset = 230h) [Reset = X0h]

CMX_48 is shown in Table 8-104.

Return to the Summary Table.

Table 8-104. CMX_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_9_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

8.2.50 CMX_49 Register (Offset = 231h) [Reset = X0h]

CMX_49 is shown in Table 8-105.

Return to the Summary Table.

Table 8-105. CMX_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_10_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

8.2.51 CMX_50 Register (Offset = 232h) [Reset = X0h]

CMX_50 is shown in Table 8-106.

Return to the Summary Table.

Table 8-106. CMX_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_10_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

8.2.52 CMX_51 Register (Offset = 233h) [Reset = X0h]

CMX_51 is shown in Table 8-107.

Return to the Summary Table.

Table 8-107. CMX_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-107. CMX_51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	LUT3_10_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

8.2.53 CMX_52 Register (Offset = 234h) [Reset = X0h]

CMX_52 is shown in Table 8-108.

Return to the Summary Table.

Table 8-108. CMX_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_11_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

8.2.54 CMX_53 Register (Offset = 235h) [Reset = X0h]

CMX_53 is shown in Table 8-109.

Return to the Summary Table.

Table 8-109. CMX_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_11_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

8.2.55 CMX_54 Register (Offset = 236h) [Reset = X0h]

CMX_54 is shown in Table 8-110.

Return to the Summary Table.

Table 8-110. CMX_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_11_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

8.2.56 CMX_55 Register (Offset = 237h) [Reset = X0h]

CMX_55 is shown in Table 8-111.

Return to the Summary Table.

Table 8-111. CMX_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_12_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

8.2.57 CMX_56 Register (Offset = 238h) [Reset = X0h]

CMX_56 is shown in Table 8-112.

Return to the Summary Table.

Table 8-112. CMX_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_12_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

8.2.58 CMX_57 Register (Offset = 239h) [Reset = X0h]

CMX_57 is shown in Table 8-113.

Return to the Summary Table.

Table 8-113. CMX_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_12_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

8.2.59 CMX_58 Register (Offset = 23Ah) [Reset = X0h]

CMX_58 is shown in Table 8-114.

Return to the Summary Table.

Table 8-114. CMX_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_13_IN0_/ _DFF_CLK_IN_OR_LDC_IN0_CMX	R/W	Xh	Same options as CMX_0

8.2.60 CMX_59 Register (Offset = 23Bh) [Reset = X0h]

CMX_59 is shown in Table 8-115.

Return to the Summary Table.

Table 8-115. CMX_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_13_IN1_/ _DFF_D_IN_OR_LDC_IN1_CMX	R/W	Xh	Same options as CMX_0

8.2.61 CMX_60 Register (Offset = 23Ch) [Reset = X0h]

CMX_60 is shown in Table 8-116.

Return to the Summary Table.

Table 8-116. CMX_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT3_13_IN2_/ _DFF_RST_IN_OR_LDC_IN2_CMX	R/W	Xh	Same options as CMX_0

8.2.62 CMX_61 Register (Offset = 23Dh) [Reset = X0h]

CMX_61 is shown in Table 8-117.

Return to the Summary Table.

Table 8-117. CMX_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT4_0_IN0_/_DFF_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.63 CMX_62 Register (Offset = 23Eh) [Reset = X0h]

CMX_62 is shown in Table 8-118.

Return to the Summary Table.

Table 8-118. CMX_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT4_0_IN1_/_DFF_D_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.64 CMX_63 Register (Offset = 23Fh) [Reset = X0h]

CMX_63 is shown in Table 8-119.

Return to the Summary Table.

Table 8-119. CMX_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT4_0_IN2_/_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.65 CMX_64 Register (Offset = 240h) [Reset = X0h]

CMX_64 is shown in Table 8-120.

Return to the Summary Table.

Table 8-120. CMX_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	LUT4_0_IN3__CMX	R/W	Xh	Same options as CMX_0

8.2.66 CMX_65 Register (Offset = 241h) [Reset = X0h]

CMX_65 is shown in Table 8-121.

Return to the Summary Table.

Table 8-121. CMX_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	PFLT_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.67 CMX_66 Register (Offset = 242h) [Reset = X0h]

CMX_66 is shown in Table 8-122.

Return to the Summary Table.

Table 8-122. CMX_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	FLT/EDET_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.68 CMX_67 Register (Offset = 243h) [Reset = X0h]

CMX_67 is shown in Table 8-123.

Return to the Summary Table.

Table 8-123. CMX_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST0_EN0_CMX	R/W	Xh	Same options as CMX_0

8.2.69 CMX_68 Register (Offset = 244h) [Reset = X0h]

CMX_68 is shown in Table 8-124.

Return to the Summary Table.

Table 8-124. CMX_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST0_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.70 CMX_69 Register (Offset = 245h) [Reset = X0h]

CMX_69 is shown in Table 8-125.

Return to the Summary Table.

Table 8-125. CMX_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST1_EN0_CMX	R/W	Xh	Same options as CMX_0

8.2.71 CMX_70 Register (Offset = 246h) [Reset = X0h]

CMX_70 is shown in Table 8-126.

Return to the Summary Table.

Table 8-126. CMX_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST1_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.72 CMX_71 Register (Offset = 247h) [Reset = X0h]

CMX_71 is shown in Table 8-127.

Return to the Summary Table.

Table 8-127. CMX_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST2_EN0_CMX	R/W	Xh	Same options as CMX_0

8.2.73 CMX_72 Register (Offset = 248h) [Reset = X0h]

CMX_72 is shown in Table 8-128.

Return to the Summary Table.

Table 8-128. CMX_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST2_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.74 CMX_73 Register (Offset = 249h) [Reset = X0h]

CMX_73 is shown in Table 8-129.

Return to the Summary Table.

Table 8-129. CMX_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST3_EN0_CMX	R/W	Xh	Same options as CMX_0

8.2.75 CMX_74 Register (Offset = 24Ah) [Reset = X0h]

CMX_74 is shown in Table 8-130.

Return to the Summary Table.

Table 8-130. CMX_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST3_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.76 CMX_75 Register (Offset = 24Bh) [Reset = X0h]

CMX_75 is shown in Table 8-131.

Return to the Summary Table.

Table 8-131. CMX_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST4_EN0_/ _PWM_GEN3_PUP_CMX	R/W	Xh	Same options as CMX_0

8.2.77 CMX_76 Register (Offset = 24Ch) [Reset = X0h]

CMX_76 is shown in Table 8-132.

Return to the Summary Table.

Table 8-132. CMX_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST4_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.78 CMX_77 Register (Offset = 24Dh) [Reset = X0h]

CMX_77 is shown in Table 8-133.

Return to the Summary Table.

Table 8-133. CMX_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST5_EN0_/ _PWM_GEN2_PUP_CMX	R/W	Xh	Same options as CMX_0

8.2.79 CMX_78 Register (Offset = 24Eh) [Reset = X0h]

CMX_78 is shown in Table 8-134.

Return to the Summary Table.

Table 8-134. CMX_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST5_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.80 CMX_79 Register (Offset = 24Fh) [Reset = X0h]

CMX_79 is shown in Table 8-135.

Return to the Summary Table.

Table 8-135. CMX_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST6_EN0_/ _PWM_GEN1_PUP_CMX	R/W	Xh	Same options as CMX_0

8.2.81 CMX_80 Register (Offset = 250h) [Reset = X0h]

CMX_80 is shown in Table 8-136.

Return to the Summary Table.

Table 8-136. CMX_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST6_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.82 CMX_81 Register (Offset = 251h) [Reset = X0h]

CMX_81 is shown in Table 8-137.

Return to the Summary Table.

Table 8-137. CMX_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST7_EN0_/ _PWM_GEN0_PUP_CMX	R/W	Xh	Same options as CMX_0

8.2.83 CMX_82 Register (Offset = 252h) [Reset = X0h]

CMX_82 is shown in Table 8-138.

Return to the Summary Table.

Table 8-138. CMX_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_ST7_EN1_CMX	R/W	Xh	Same options as CMX_0

8.2.84 CMX_83 Register (Offset = 253h) [Reset = X0h]

CMX_83 is shown in Table 8-139.

Return to the Summary Table.

Table 8-139. CMX_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.85 CMX_84 Register (Offset = 254h) [Reset = X0h]

CMX_84 is shown in Table 8-140.

Return to the Summary Table.

Table 8-140. CMX_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	SM_RST_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.86 CMX_85 Register (Offset = 255h) [Reset = X0h]

CMX_85 is shown in Table 8-141.

Return to the Summary Table.

Table 8-141. CMX_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	McACMP_ENABLE_CMX	R/W	Xh	Same options as CMX_0

8.2.87 CMX_86 Register (Offset = 256h) [Reset = X0h]

CMX_86 is shown in Table 8-142.

Return to the Summary Table.

Table 8-142. CMX_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	McACMP_RST_CMX	R/W	Xh	Same options as CMX_0

8.2.88 CMX_87 Register (Offset = 257h) [Reset = X0h]

CMX_87 is shown in Table 8-143.

Return to the Summary Table.

Table 8-143. CMX_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	OSC0_PWR_DOWN_CMX	R/W	Xh	Same options as CMX_0

8.2.89 CMX_88 Register (Offset = 258h) [Reset = X0h]

CMX_88 is shown in Table 8-144.

Return to the Summary Table.

Table 8-144. CMX_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	OSC1_PWR_DOWN_CMX	R/W	Xh	Same options as CMX_0

8.2.90 CMX_89 Register (Offset = 259h) [Reset = X0h]

CMX_89 is shown in Table 8-145.

Return to the Summary Table.

Table 8-145. CMX_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT6/FSM_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.91 CMX_90 Register (Offset = 25Ah) [Reset = X0h]

CMX_90 is shown in Table 8-146.

Return to the Summary Table.

Table 8-146. CMX_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT6/FSM_UP_CMX	R/W	Xh	Same options as CMX_0

8.2.92 CMX_91 Register (Offset = 25Bh) [Reset = X0h]

CMX_91 is shown in Table 8-147.

Return to the Summary Table.

Table 8-147. CMX_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-147. CMX_91 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	CNT6/FSM_KEEP_CMX	R/W	Xh	Same options as CMX_0

8.2.93 CMX_92 Register (Offset = 25Ch) [Reset = X0h]

CMX_92 is shown in Table 8-148.

Return to the Summary Table.

Table 8-148. CMX_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT6/FSM_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.94 CMX_93 Register (Offset = 25Dh) [Reset = X0h]

CMX_93 is shown in Table 8-149.

Return to the Summary Table.

Table 8-149. CMX_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT7/FSM_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.95 CMX_94 Register (Offset = 25Eh) [Reset = X0h]

CMX_94 is shown in Table 8-150.

Return to the Summary Table.

Table 8-150. CMX_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT7/FSM_UP_CMX	R/W	Xh	Same options as CMX_0

8.2.96 CMX_95 Register (Offset = 25Fh) [Reset = X0h]

CMX_95 is shown in Table 8-151.

Return to the Summary Table.

Table 8-151. CMX_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT7/FSM_KEEP_CMX	R/W	Xh	Same options as CMX_0

8.2.97 CMX_96 Register (Offset = 260h) [Reset = X0h]

CMX_96 is shown in Table 8-152.

Return to the Summary Table.

Table 8-152. CMX_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-152. CMX_96 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	CNT7/FSM_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.98 CMX_97 Register (Offset = 261h) [Reset = X0h]

CMX_97 is shown in Table 8-153.

Return to the Summary Table.

Table 8-153. CMX_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT8/FSM_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.99 CMX_98 Register (Offset = 262h) [Reset = X0h]

CMX_98 is shown in Table 8-154.

Return to the Summary Table.

Table 8-154. CMX_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT8/FSM_UP_CMX	R/W	Xh	Same options as CMX_0

8.2.100 CMX_99 Register (Offset = 263h) [Reset = X0h]

CMX_99 is shown in Table 8-155.

Return to the Summary Table.

Table 8-155. CMX_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT8/FSM_KEEP_CMX	R/W	Xh	Same options as CMX_0

8.2.101 CMX_100 Register (Offset = 264h) [Reset = X0h]

CMX_100 is shown in Table 8-156.

Return to the Summary Table.

Table 8-156. CMX_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT8/FSM_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.102 CMX_101 Register (Offset = 265h) [Reset = X0h]

CMX_101 is shown in Table 8-157.

Return to the Summary Table.

Table 8-157. CMX_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-157. CMX_101 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	CNT9/FSM_IN_/_WDT_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.103 CMX_102 Register (Offset = 266h) [Reset = X0h]

CMX_102 is shown in Table 8-158.

Return to the Summary Table.

Table 8-158. CMX_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT9/FSM_UP_/_WDT_EN_CMX	R/W	Xh	Same options as CMX_0

8.2.104 CMX_103 Register (Offset = 267h) [Reset = X0h]

CMX_103 is shown in Table 8-159.

Return to the Summary Table.

Table 8-159. CMX_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT9/FSM_KEEP_CMX	R/W	Xh	Same options as CMX_0

8.2.105 CMX_104 Register (Offset = 268h) [Reset = X0h]

CMX_104 is shown in Table 8-160.

Return to the Summary Table.

Table 8-160. CMX_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	CNT9/FSM_CLK_IN_CMX	R/W	Xh	Same options as CMX_0

8.2.106 CMX_105 Register (Offset = 269h) [Reset = X0h]

CMX_105 is shown in Table 8-161.

Return to the Summary Table.

Table 8-161. CMX_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VIRTUAL_OUT0_CMX	R/W	Xh	Same options as CMX_0

8.2.107 CMX_106 Register (Offset = 26Ah) [Reset = X0h]

CMX_106 is shown in Table 8-162.

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Table 8-162. CMX_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-162. CMX_106 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VIRTUAL_OUT1_CMX	R/W	Xh	Same options as CMX_0

8.2.108 CMX_107 Register (Offset = 26Bh) [Reset = X0h]

CMX_107 is shown in Table 8-163.

Return to the Summary Table.

Table 8-163. CMX_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VIRTUAL_OUT2_CMX	R/W	Xh	Same options as CMX_0

8.2.109 CMX_108 Register (Offset = 26Ch) [Reset = X0h]

CMX_108 is shown in Table 8-164.

Return to the Summary Table.

Table 8-164. CMX_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VIRTUAL_OUT3_CMX	R/W	Xh	Same options as CMX_0

8.2.110 CMX_109 Register (Offset = 26Dh) [Reset = X0h]

CMX_109 is shown in Table 8-165.

Return to the Summary Table.

Table 8-165. CMX_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VIRTUAL_OUT4_CMX	R/W	Xh	Same options as CMX_0

8.2.111 CMX_110 Register (Offset = 26Eh) [Reset = X0h]

CMX_110 is shown in Table 8-166.

Return to the Summary Table.

Table 8-166. CMX_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VIRTUAL_OUT5_CMX	R/W	Xh	Same options as CMX_0

8.2.112 CMX_111 Register (Offset = 26Fh) [Reset = X0h]

CMX_111 is shown in Table 8-167.

Return to the Summary Table.

Table 8-167. CMX_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-167. CMX_111 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VIRTUAL_OUT6_CMX	R/W	Xh	Same options as CMX_0

8.2.113 CMX_112 Register (Offset = 270h) [Reset = X0h]

CMX_112 is shown in Table 8-168.

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Table 8-168. CMX_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VIRTUAL_OUT7_CMX	R/W	Xh	Same options as CMX_0

8.3 TPLD1202_Cfg_1 Registers

Table 8-169 lists the memory-mapped registers for the TPLD1202_Cfg_1 registers. All register offset addresses not listed in Table 8-169 should be considered as reserved locations and the register contents should not be modified.

Table 8-169. TPLD1202_CFG_1 Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
300h	GPI_CFG	RESERVED	PULL_UP_EN	RES_SEL		RESERVED		IN_CTRL	
301h	GPIO1_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
302h	GPIO2_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
303h	GPIO3_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
304h	GPIO4_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
305h	GPIO5_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
306h	GPIO6_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
307h	GPIO7_CFG	OE	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
308h	GPIO8_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
309h	GPIO9_CFG	RESERVED	PULL_UP_EN	RES_SEL		OUT_CTRL		IN_CTRL	
320h	VIO_SEL_0	V_IN7	V_IN6	V_IN5	V_IN4	V_IN3	V_IN2	V_IN1	V_IN0
324h	LUT_FS_0	RESERVED					LUT2_2_FS	LUT2_1_FS	LUT2_0_FS
325h	LUT_FS_1	LUT3_7_FS	LUT3_6_FS	LUT3_5_FS	LUT3_4_FS	LUT3_3_FS	LUT3_2_FS	LUT3_1_FS	LUT3_0_FS
326h	LUT_FS_2	RESERVED							LUT4_0_FS
328h	LUT2_0_CFG	RESERVED				BIT3	BIT2	BIT1	BIT0
329h	LUT2_1_CFG	RESERVED				BIT3	BIT2	BIT1	BIT0
32Eh	LUT2_2_CFG0	RESERVED		PGEN_RST	RESERVED	BITS3_0			
32Fh	LUT2_2_CFG1	PGEN_DATA_LSB							
330h	LUT2_2_CFG2	PGEN_DATA_MSB							
334h	LUT3_0_CFG	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
335h	LUT3_1_CFG	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
336h	LUT3_2_CFG	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
337h	LUT3_3_CFG	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
338h	LUT3_4_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
339h	LUT3_4_CFG1	SR0_INIT							
33Ah	LUT3_5_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
33Bh	LUT3_5_CFG1	SR1_INIT							
33Ch	LUT3_6_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
33Dh	LUT3_6_CFG1	SR2_INIT							
33Eh	LUT3_7_CFG0	BIT7	BITS6_4			BIT3	BIT2	BIT1	BIT0
33Fh	LUT3_7_CFG1	SR3_INIT							
344h	LUT4_0_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
345h	LUT4_0_CFG1	LUT4_0_MSB							
354h	LUT3_8_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
355h	LUT3_8_CFG1	CNT_DATA							
356h	LUT3_8_CFG2	CLK_SEL				MODE_SEL			
357h	LUT3_8_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
358h	LUT3_8_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
359h	LUT3_9_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
35Ah	LUT3_9_CFG1	CNT_DATA							
35Bh	LUT3_9_CFG2	CLK_SEL				MODE_SEL			
35Ch	LUT3_9_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
35Dh	LUT3_9_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
35Eh	LUT3_10_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
35Fh	LUT3_10_CFG1	CNT_DATA							
360h	LUT3_10_CFG2	CLK_SEL				MODE_SEL			
361h	LUT3_10_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
362h	LUT3_10_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
363h	LUT3_11_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

Table 8-169. TPLD1202_CFG_1 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
364h	LUT3_11_CFG1	CNT_DATA							
365h	LUT3_11_CFG2	CLK_SEL				MODE_SEL			
366h	LUT3_11_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
367h	LUT3_11_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
368h	LUT3_12_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
369h	LUT3_12_CFG1	CNT_DATA							
36Ah	LUT3_12_CFG2	CLK_SEL				MODE_SEL			
36Bh	LUT3_12_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
36Ch	LUT3_12_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
36Dh	LUT3_13_CFG0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
36Eh	LUT3_13_CFG1	CNT_DATA							
36Fh	LUT3_13_CFG2	CLK_SEL				MODE_SEL			
370h	LUT3_13_CFG3	RESERVED		RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
371h	LUT3_13_CFG4	RESERVED			LDC_FS	LDC_CMX_IN_SEL		LDC_CMX_MODE	
37Eh	CNT6_FSM0_CFG0	CNT_DATA							
37Fh	CNT6_FSM0_CFG1	CLK_SEL				MODE_SEL			
380h	CNT6_FSM0_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
381h	CNT7_FSM1_CFG0	CNT_DATA							
382h	CNT7_FSM1_CFG1	CLK_SEL				MODE_SEL			
383h	CNT7_FSM1_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
384h	CNT8_FSM2_CFG0	CNT_DATA							
385h	CNT8_FSM2_CFG1	CLK_SEL				MODE_SEL			
386h	CNT8_FSM2_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
387h	CNT9_FSM3_CFG0	CNT_DATA							
388h	CNT9_FSM3_CFG1	CLK_SEL				MODE_SEL			
389h	CNT9_FSM3_CFG2	UP_SYNC	KEEP_SYNC	RST_SYNC	RESERVED	CNT_INIT		OUT_POL	DLY_EDET
38Ah	PWM_GEN0_CFG	PWM_EN	RESERVED			TDB_SEL		OUTP_POL	OUTN_POL
38Bh	PWM_GEN1_CFG	PWM_EN	RESERVED			TDB_SEL		OUTP_POL	OUTN_POL
38Ch	PWM_GEN2_CFG	PWM_EN	RESERVED			TDB_SEL		OUTP_POL	OUTN_POL
38Dh	PWM_GEN3_CFG	PWM_EN	RESERVED			TDB_SEL		OUTP_POL	OUTN_POL
38Eh	PWM_SRC_CFG	PWM3_DATA_SEL		PWM2_DATA_SEL		PWM1_DATA_SEL		PWM0_DATA_SEL	
38Fh	SM_CFG0	RESERVED	SM_S1_IN0			RESERVED	SM_S0_IN0		
390h	SM_CFG1	RESERVED	SM_S1_IN1			RESERVED	SM_S0_IN1		
391h	SM_CFG2	RESERVED							
392h	SM_CFG3	RESERVED	SM_S3_IN0			RESERVED	SM_S2_IN0		
393h	SM_CFG4	RESERVED	SM_S3_IN1			RESERVED	SM_S2_IN1		
394h	SM_CFG5	RESERVED							
395h	SM_CFG6	RESERVED	SM_S5_IN0			RESERVED	SM_S4_IN0		
396h	SM_CFG7	RESERVED	SM_S5_IN1			RESERVED	SM_S4_IN1		
397h	SM_CFG8	RESERVED							
398h	SM_CFG9	RESERVED	SM_S7_IN0			RESERVED	SM_S6_IN0		
399h	SM_CFG10	RESERVED	SM_S7_IN1			RESERVED	SM_S6_IN1		
39Ah	SM_CFG11	SM_SYNC_EN	RESERVED						
3A7h	SM_CFG12	SM_CLK_SEL				MODE_SEL	SM_INIT_STATE		
3A8h	SM_CFG13	S0_OUT_CFG							
3A9h	SM_CFG14	S1_OUT_CFG							
3AAh	SM_CFG15	S2_OUT_CFG							
3ABh	SM_CFG16	S3_OUT_CFG							
3ACh	SM_CFG17	S4_OUT_CFG							
3ADh	SM_CFG18	S5_OUT_CFG							
3AEh	SM_CFG19	S6_OUT_CFG							
3AFh	SM_CFG20	S7_OUT_CFG							
3B8h	WDT_CFG0	WDT_TIMEOUT_DATA							
3B9h	WDT_CFG1	WDT_OUT_DATA							
3BAh	WDT_CFG2	WDT_CLK_SEL				RESERVED	WDT_EN	WDT_100X_EN	WDT_EN_SEL

Table 8-169. TPLD1202_CFG_1 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3BBh	PFLT_CFG	RESERVED		PFLT_DLY_SEL		PFLT_POL	RESERVED	PFLT_EDGE_SEL	
3BDh	FLT_CFG	RESERVED				FLT_POL	RESERVED	FLT_EDGE_SEL	
3BEh	OSC0_CFG0	RESERVED	CTRL_SRC	CTRL_SEL	SRC_SEL	PDIV		FREQ_SEL	PWR_MODE
3BFh	OSC0_CFG1	OUT1_EN	OUT1_DIV			OUT0_EN	OUT0_DIV		
3C0h	OSC1_CFG0	SU_DLY	CTRL_SRC	CTRL_SEL	SRC_SEL	PDIV			PWR_MODE
3C1h	OSC1_CFG1	RESERVED				OUT_EN	OUT_DIV		
3C5h	OSC1_CG	OSC1_DIV3	OSC1_DIV512	OSC1_DIV64	OSC1_DIV24	OSC1_DIV12	OSC1_DIV8	OSC1_DIV4	OSC1_DIV2
3CFh	MCACMP_CFG0	TS_INP_EN	VCC_INP_EN	SYNC_EN	MCS_MODE	CH_EN		RESERVED	MCS_EN
3D0h	MCACMP_CFG1	RESERVED					EDGE_SEL	MCS_CLK_SEL	
3D1h	MCACMP_CH0_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3D2h	MCACMP_CH0_CFG1	RESERVED		VREF_SEL					
3D6h	MCACMP_CH1_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3D7h	MCACMP_CH1_CFG1	RESERVED		VREF_SEL					
3DBh	MCACMP_CH2_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3DCh	MCACMP_CH2_CFG1	RESERVED		VREF_SEL					
3E0h	MCACMP_CH3_CFG0	RESERVED	RST_EN	INP_SEL		GAIN_SEL		HYS_SEL	
3E1h	MCACMP_CH3_CFG1	RESERVED		VREF_SEL					
3F2h	SER_COMM_CFG0	I2C_ADDR_SRC_SEL				I2C_IO_LAT	I2C_RST_EN	I2C_EN	SPI_EN
3F3h	SER_COMM_CFG1	I2C_ADDR_MSB				I2C_ADDR_LSB			RESERVED
3F7h	MISC_CFG0	GPIO_QC	CFG_RD_LCK	CFG_WR_LCK	OTP_WR_LCK	USER_LCK		RESERVED	
3F8h	MISC_CFG1	RESERVED	VBG_CTRL			RESERVED	PREBIAS_CTRL		
3F9h	MISC_CFG2	RESERVED							RD_DATA_SYNC
3FAh	DEVICE_ID4	DEVICE_ID4							
3FBh	DEVICE_ID5	DEVICE_ID5							
3FCh	DEVICE_ID6	DEVICE_ID6							
3FDh	DEVICE_ID7	DEVICE_ID7							
3FEh	CRC_LSB	CRC_LSB							
3FFh	CRC_MSB	CRC_MSB							

Complex bit access types are encoded to fit into small table cells. Table 8-170 shows the codes that are used for access types in this section.

Table 8-170. TPLD1202_Cfg_1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 GPI_CFG Register (Offset = 300h) [Reset = XXh]

GPI_CFG is shown in Table 8-171.

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Table 8-171. GPI_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up

Table 8-171. GPI_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	RESERVED	R	0h	Reserved
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

8.3.2 GPIO1_CFG Register (Offset = 301h) [Reset = X0h]

GPIO1_CFG is shown in Table 8-172.

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Table 8-172. GPIO1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 4X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

8.3.3 GPIO2_CFG Register (Offset = 302h) [Reset = X0h]

GPIO2_CFG is shown in Table 8-173.

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Table 8-173. GPIO2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 4X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

8.3.4 GPIO3_CFG Register (Offset = 303h) [Reset = XXh]

GPIO3_CFG is shown in Table 8-174.

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Table 8-174. GPIO3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

8.3.5 GPIO4_CFG Register (Offset = 304h) [Reset = XXh]

GPIO4_CFG is shown in Table 8-175.

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Table 8-175. GPIO4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

8.3.6 GPIO5_CFG Register (Offset = 305h) [Reset = X0h]

GPIO5_CFG is shown in Table 8-176.

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Table 8-176. GPIO5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

8.3.7 GPIO6_CFG Register (Offset = 306h) [Reset = X0h]

GPIO6_CFG is shown in Table 8-177.

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Table 8-177. GPIO6_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

8.3.8 GPIO7_CFG Register (Offset = 307h) [Reset = X0h]

GPIO7_CFG is shown in Table 8-178.

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Table 8-178. GPIO7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0h	0h = Input 1h = Output
6	PULL_UP_EN	R/W	0h	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	0h	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

8.3.9 GPIO8_CFG Register (Offset = 308h) [Reset = XXh]

GPIO8_CFG is shown in Table 8-179.

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Table 8-179. GPIO8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X

Table 8-179. GPIO8_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Analog I/O

8.3.10 GPIO9_CFG Register (Offset = 309h) [Reset = XXh]

GPIO9_CFG is shown in Table 8-180.

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Table 8-180. GPIO9_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PULL_UP_EN	R/W	Xh	0h = Pull down 1h = Pull up
5:4	RES_SEL	R/W	Xh	0h = Floating 1h = 10k Ω 2h = 100k Ω 3h = 1M Ω
3:2	OUT_CTRL	R/W	Xh	0h = Push-pull 1X 1h = Push-pull 2X 2h = Open-drain NMOS 1X 3h = Open-drain NMOS 2X
1:0	IN_CTRL	R/W	Xh	0h = Digital input without Schmitt Trigger 1h = Digital input with Schmitt Trigger 2h = Low voltage digital input 3h = Reserved

8.3.11 VIO_SEL_0 Register (Offset = 320h) [Reset = X0h]

VIO_SEL_0 is shown in Table 8-181.

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Table 8-181. VIO_SEL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V_IN7	R/W	0h	0h = IO9 1h = V_IN7
6	V_IN6	R/W	0h	0h = IO7 1h = V_IN6
5	V_IN5	R/W	0h	0h = IO6 1h = V_IN5
4	V_IN4	R/W	0h	0h = IO5 1h = V_IN4
3	V_IN3	R/W	Xh	0h = IO4 1h = V_IN3
2	V_IN2	R/W	Xh	0h = IO3 1h = V_IN2
1	V_IN1	R/W	Xh	0h = IO2 1h = V_IN1
0	V_IN0	R/W	Xh	0h = IO1 1h = V_IN0

8.3.12 LUT_FS_0 Register (Offset = 324h) [Reset = 0Xh]

LUT_FS_0 is shown in Table 8-182.

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Table 8-182. LUT_FS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0h	Reserved

Table 8-182. LUT_FS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LUT2_2_FS	R/W	Xh	0h = LUT 1h = PGEN
1	LUT2_1_FS	R/W	Xh	0h = LUT 1h = DFF
0	LUT2_0_FS	R/W	Xh	0h = LUT 1h = DFF

8.3.13 LUT_FS_1 Register (Offset = 325h) [Reset = X0h]

LUT_FS_1 is shown in Table 8-183.

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Table 8-183. LUT_FS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LUT3_7_FS	R/W	0h	0h = LUT 1h = DFF / SR
6	LUT3_6_FS	R/W	0h	0h = LUT 1h = DFF / SR
5	LUT3_5_FS	R/W	0h	0h = LUT 1h = DFF / SR
4	LUT3_4_FS	R/W	0h	0h = LUT 1h = DFF / SR
3	LUT3_3_FS	R/W	Xh	0h = LUT 1h = DFF
2	LUT3_2_FS	R/W	Xh	0h = LUT 1h = DFF
1	LUT3_1_FS	R/W	Xh	0h = LUT 1h = DFF
0	LUT3_0_FS	R/W	Xh	0h = LUT 1h = DFF

8.3.14 LUT_FS_2 Register (Offset = 326h) [Reset = 0Xh]

LUT_FS_2 is shown in Table 8-184.

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Table 8-184. LUT_FS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	LUT4_0_FS	R/W	Xh	0h = LUT 1h = DFF

8.3.15 LUT2_0_CFG Register (Offset = 328h) [Reset = X0h]

LUT2_0_CFG is shown in Table 8-185.

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Table 8-185. LUT2_0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	BIT3	R/W	Xh	LUT2[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT2[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT2[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output

Table 8-185. LUT2_0_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BIT0	R/W	Xh	LUT2[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.16 LUT2_1_CFG Register (Offset = 329h) [Reset = X0h]

LUT2_1_CFG is shown in Table 8-186.

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Table 8-186. LUT2_1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	BIT3	R/W	Xh	LUT2[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT2[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT2[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT2[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.17 LUT2_2_CFG0 Register (Offset = 32Eh) [Reset = XXh]

LUT2_2_CFG0 is shown in Table 8-187.

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Table 8-187. LUT2_2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	PGEN_RST	R/W	Xh	OTP_SPARE or PGEN RST LVL 0h = Low 1h = High
4	RESERVED	R	0h	Reserved
3:0	BITS3_0	R/W	Xh	LUT2[3:0] or PGEN SIZE 0h = 1 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8 8h = 9 9h = 10 Ah = 11 Bh = 12 Ch = 13 Dh = 14 Eh = 15 Fh = 16

8.3.18 LUT2_2_CFG1 Register (Offset = 32Fh) [Reset = X0h]

LUT2_2_CFG1 is shown in Table 8-188.

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Table 8-188. LUT2_2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_LSB	R/W	Xh	PGEN_DATA[7:0]

8.3.19 LUT2_2_CFG2 Register (Offset = 330h) [Reset = X0h]

LUT2_2_CFG2 is shown in Table 8-189.

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Table 8-189. LUT2_2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PGEN_DATA_MSB	R/W	Xh	PGEN_DATA[15:8]

8.3.20 LUT3_0_CFG Register (Offset = 334h) [Reset = X0h]

LUT3_0_CFG is shown in Table 8-190.

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Table 8-190. LUT3_0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.21 LUT3_1_CFG Register (Offset = 335h) [Reset = X0h]

LUT3_1_CFG is shown in Table 8-191.

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Table 8-191. LUT3_1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock

Table 8-191. LUT3_1_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.22 LUT3_2_CFG Register (Offset = 336h) [Reset = X0h]

LUT3_2_CFG is shown in Table 8-192.

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Table 8-192. LUT3_2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.23 LUT3_3_CFG Register (Offset = 337h) [Reset = X0h]

LUT3_3_CFG is shown in Table 8-193.

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Table 8-193. LUT3_3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High

Table 8-193. LUT3_3_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.24 LUT3_4_CFG0 Register (Offset = 338h) [Reset = X0h]

LUT3_4_CFG0 is shown in Table 8-194.

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Table 8-194. LUT3_4_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.25 LUT3_4_CFG1 Register (Offset = 339h) [Reset = X0h]

LUT3_4_CFG1 is shown in Table 8-195.

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Table 8-195. LUT3_4_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SR0_INIT	R/W	Xh	DFF / SR INIT VAL

8.3.26 LUT3_5_CFG0 Register (Offset = 33Ah) [Reset = X0h]

LUT3_5_CFG0 is shown in Table 8-196.

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Table 8-196. LUT3_5_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8

Table 8-196. LUT3_5_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.27 LUT3_5_CFG1 Register (Offset = 33Bh) [Reset = X0h]

LUT3_5_CFG1 is shown in Table 8-197.

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Table 8-197. LUT3_5_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SR1_INIT	R/W	Xh	DFF / SR INIT VAL

8.3.28 LUT3_6_CFG0 Register (Offset = 33Ch) [Reset = X0h]

LUT3_6_CFG0 is shown in Table 8-198.

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Table 8-198. LUT3_6_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.29 LUT3_6_CFG1 Register (Offset = 33Dh) [Reset = X0h]

LUT3_6_CFG1 is shown in Table 8-199.

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Table 8-199. LUT3_6_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SR2_INIT	R/W	Xh	DFF / SR INIT VAL

8.3.30 LUT3_7_CFG0 Register (Offset = 33Eh) [Reset = X0h]

LUT3_7_CFG0 is shown in Table 8-200.

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Table 8-200. LUT3_7_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6:4	BITS6_4	R/W	0h	LUT3[6:4] or SR SIZE 0h = 1 (DFF) 1h = 2 2h = 3 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8
3	BIT3	R/W	Xh	LUT3[3] or DFF / SR RST LVL 0h = Low 1h = High
2	BIT2	R/W	Xh	LUT3[2] or DFF / SR RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
1	BIT1	R/W	Xh	LUT3[1] or DFF / SR OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.31 LUT3_7_CFG1 Register (Offset = 33Fh) [Reset = X0h]

LUT3_7_CFG1 is shown in Table 8-201.

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Table 8-201. LUT3_7_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SR3_INIT	R/W	Xh	DFF / SR INIT VAL

8.3.32 LUT4_0_CFG0 Register (Offset = 344h) [Reset = X0h]

LUT4_0_CFG0 is shown in Table 8-202.

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Table 8-202. LUT4_0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT4[7]
6	BIT6	R/W	0h	LUT4[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT4[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT4[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT4[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT4[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT4[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output

Table 8-202. LUT4_0_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BIT0	R/W	Xh	LUT4[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.33 LUT4_0_CFG1 Register (Offset = 345h) [Reset = X0h]

LUT4_0_CFG1 is shown in Table 8-203.

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Table 8-203. LUT4_0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LUT4_0_MSB	R/W	Xh	LUT4_0[15:8]

8.3.34 LUT3_8_CFG0 Register (Offset = 354h) [Reset = X0h]

LUT3_8_CFG0 is shown in Table 8-204.

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Table 8-204. LUT3_8_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.35 LUT3_8_CFG1 Register (Offset = 355h) [Reset = X0h]

LUT3_8_CFG1 is shown in Table 8-205.

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Table 8-205. LUT3_8_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.36 LUT3_8_CFG2 Register (Offset = 356h) [Reset = X0h]

LUT3_8_CFG2 is shown in Table 8-206.

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Table 8-206. LUT3_8_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.37 LUT3_8_CFG3 Register (Offset = 357h) [Reset = X0h]

LUT3_8_CFG3 is shown in Table 8-207.

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Table 8-207. LUT3_8_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.38 LUT3_8_CFG4 Register (Offset = 358h) [Reset = XXh]

LUT3_8_CFG4 is shown in Table 8-208.

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Table 8-208. LUT3_8_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF

Table 8-208. LUT3_8_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

8.3.39 LUT3_9_CFG0 Register (Offset = 359h) [Reset = X0h]

LUT3_9_CFG0 is shown in Table 8-209.

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Table 8-209. LUT3_9_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.40 LUT3_9_CFG1 Register (Offset = 35Ah) [Reset = X0h]

LUT3_9_CFG1 is shown in Table 8-210.

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Table 8-210. LUT3_9_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.41 LUT3_9_CFG2 Register (Offset = 35Bh) [Reset = X0h]

LUT3_9_CFG2 is shown in Table 8-211.

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Table 8-211. LUT3_9_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.42 LUT3_9_CFG3 Register (Offset = 35Ch) [Reset = X0h]

LUT3_9_CFG3 is shown in Table 8-212.

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Table 8-212. LUT3_9_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.43 LUT3_9_CFG4 Register (Offset = 35Dh) [Reset = XXh]

LUT3_9_CFG4 is shown in Table 8-213.

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Table 8-213. LUT3_9_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF

Table 8-213. LUT3_9_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

8.3.44 LUT3_10_CFG0 Register (Offset = 35Eh) [Reset = X0h]

LUT3_10_CFG0 is shown in Table 8-214.

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Table 8-214. LUT3_10_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.45 LUT3_10_CFG1 Register (Offset = 35Fh) [Reset = X0h]

LUT3_10_CFG1 is shown in Table 8-215.

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Table 8-215. LUT3_10_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.46 LUT3_10_CFG2 Register (Offset = 360h) [Reset = X0h]

LUT3_10_CFG2 is shown in Table 8-216.

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Table 8-216. LUT3_10_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.47 LUT3_10_CFG3 Register (Offset = 361h) [Reset = X0h]

LUT3_10_CFG3 is shown in Table 8-217.

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Table 8-217. LUT3_10_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.48 LUT3_10_CFG4 Register (Offset = 362h) [Reset = XXh]

LUT3_10_CFG4 is shown in Table 8-218.

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Table 8-218. LUT3_10_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF

Table 8-218. LUT3_10_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

8.3.49 LUT3_11_CFG0 Register (Offset = 363h) [Reset = X0h]

LUT3_11_CFG0 is shown in Table 8-219.

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Table 8-219. LUT3_11_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.50 LUT3_11_CFG1 Register (Offset = 364h) [Reset = X0h]

LUT3_11_CFG1 is shown in Table 8-220.

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Table 8-220. LUT3_11_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.51 LUT3_11_CFG2 Register (Offset = 365h) [Reset = X0h]

LUT3_11_CFG2 is shown in Table 8-221.

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Table 8-221. LUT3_11_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.52 LUT3_11_CFG3 Register (Offset = 366h) [Reset = X0h]

LUT3_11_CFG3 is shown in Table 8-222.

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Table 8-222. LUT3_11_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.53 LUT3_11_CFG4 Register (Offset = 367h) [Reset = XXh]

LUT3_11_CFG4 is shown in Table 8-223.

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Table 8-223. LUT3_11_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF

Table 8-223. LUT3_11_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

8.3.54 LUT3_12_CFG0 Register (Offset = 368h) [Reset = X0h]

LUT3_12_CFG0 is shown in Table 8-224.

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Table 8-224. LUT3_12_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.55 LUT3_12_CFG1 Register (Offset = 369h) [Reset = X0h]

LUT3_12_CFG1 is shown in Table 8-225.

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Table 8-225. LUT3_12_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.56 LUT3_12_CFG2 Register (Offset = 36Ah) [Reset = X0h]

LUT3_12_CFG2 is shown in Table 8-226.

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Table 8-226. LUT3_12_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.57 LUT3_12_CFG3 Register (Offset = 36Bh) [Reset = X0h]

LUT3_12_CFG3 is shown in Table 8-227.

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Table 8-227. LUT3_12_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.58 LUT3_12_CFG4 Register (Offset = 36Ch) [Reset = XXh]

LUT3_12_CFG4 is shown in Table 8-228.

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Table 8-228. LUT3_12_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF

Table 8-228. LUT3_12_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

8.3.59 LUT3_13_CFG0 Register (Offset = 36Dh) [Reset = X0h]

LUT3_13_CFG0 is shown in Table 8-229.

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Table 8-229. LUT3_13_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BIT7	R/W	0h	LUT3[7]
6	BIT6	R/W	0h	LUT3[6] or DFF NUM SEL 0h = 1-DFF 1h = 2-DFF
5	BIT5	R/W	0h	LUT3[5] or DFF RST LVL 0h = Low 1h = High
4	BIT4	R/W	0h	LUT3[4] or DFF RST / SET SEL 0h = Reset (CLRZ) 1h = Set (PREZ)
3	BIT3	R/W	Xh	LUT3[3] or DFF CLK POL 0h = Non-inverted clock 1h = Inverted clock
2	BIT2	R/W	Xh	LUT3[2] or DFF INIT VAL 0h = Low 1h = High
1	BIT1	R/W	Xh	LUT3[1] or DFF OUT POL 0h = Non-inverted output 1h = Inverted output
0	BIT0	R/W	Xh	LUT3[0] or DFF / LAT SEL 0h = DFF function 1h = LATCH function

8.3.60 LUT3_13_CFG1 Register (Offset = 36Eh) [Reset = X0h]

LUT3_13_CFG1 is shown in Table 8-230.

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Table 8-230. LUT3_13_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.61 LUT3_13_CFG2 Register (Offset = 36Fh) [Reset = X0h]

LUT3_13_CFG2 is shown in Table 8-231.

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Table 8-231. LUT3_13_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.62 LUT3_13_CFG3 Register (Offset = 370h) [Reset = X0h]

LUT3_13_CFG3 is shown in Table 8-232.

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Table 8-232. LUT3_13_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.63 LUT3_13_CFG4 Register (Offset = 371h) [Reset = XXh]

LUT3_13_CFG4 is shown in Table 8-233.

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Table 8-233. LUT3_13_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	LDC_FS	R/W	Xh	LUT3 / DFF function select 0h = LUT 1h = DFF

Table 8-233. LUT3_13_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LDC_CMX_IN_SEL	R/W	Xh	LUT3 / DFF input routing select 0h = CNT OUT to LUT IN2 / DFF RST IN 1h = CNT OUT to LUT IN1 / DFF D IN 2h = CNT OUT to LUT IN0 / DFF CLK IN 3h = Reserved
1:0	LDC_CMX_MODE	R/W	Xh	LUT3 / DFF + CNT mode select 0h = LUT / DFF only 1h = CNT only 2h = CNT OUT to LUT / DFF IN 3h = LUT / DFF OUT to CNT IN

8.3.64 CNT6_FSM0_CFG0 Register (Offset = 37Eh) [Reset = X0h]

CNT6_FSM0_CFG0 is shown in Table 8-234.

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Table 8-234. CNT6_FSM0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.65 CNT6_FSM0_CFG1 Register (Offset = 37Fh) [Reset = X0h]

CNT6_FSM0_CFG1 is shown in Table 8-235.

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Table 8-235. CNT6_FSM0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.66 CNT6_FSM0_CFG2 Register (Offset = 380h) [Reset = 0Xh]

CNT6_FSM0_CFG2 is shown in Table 8-236.

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Table 8-236. CNT6_FSM0_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.67 CNT7_FSM1_CFG0 Register (Offset = 381h) [Reset = X0h]

CNT7_FSM1_CFG0 is shown in Table 8-237.

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Table 8-237. CNT7_FSM1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.68 CNT7_FSM1_CFG1 Register (Offset = 382h) [Reset = X0h]

CNT7_FSM1_CFG1 is shown in Table 8-238.

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Table 8-238. CNT7_FSM1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved

Table 8-238. CNT7_FSM1_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.69 CNT7_FSM1_CFG2 Register (Offset = 383h) [Reset = 0Xh]

CNT7_FSM1_CFG2 is shown in Table 8-239.

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Table 8-239. CNT7_FSM1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.70 CNT8_FSM2_CFG0 Register (Offset = 384h) [Reset = X0h]

CNT8_FSM2_CFG0 is shown in Table 8-240.

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Table 8-240. CNT8_FSM2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.71 CNT8_FSM2_CFG1 Register (Offset = 385h) [Reset = X0h]

CNT8_FSM2_CFG1 is shown in Table 8-241.

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Table 8-241. CNT8_FSM2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.72 CNT8_FSM2_CFG2 Register (Offset = 386h) [Reset = 0Xh]

CNT8_FSM2_CFG2 is shown in Table 8-242.

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Table 8-242. CNT8_FSM2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.73 CNT9_FSM3_CFG0 Register (Offset = 387h) [Reset = X0h]

CNT9_FSM3_CFG0 is shown in Table 8-243.

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Table 8-243. CNT9_FSM3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CNT_DATA	R/W	Xh	CNT DATA

8.3.74 CNT9_FSM3_CFG1 Register (Offset = 388h) [Reset = X0h]

CNT9_FSM3_CFG1 is shown in Table 8-244.

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Table 8-244. CNT9_FSM3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK_SEL	R/W	0h	CNT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3:0	MODE_SEL	R/W	Xh	CNT MODE and EDGE SEL 0h = Delay / Both edge 1h = Delay / Falling edge 2h = Delay / Rising edge 3h = One-shot / Both edge 4h = One-shot / Falling edge 5h = One-shot / Rising edge 6h = Frequency detect / Both edge 7h = Frequency detect / Falling edge 8h = Frequency detect / Rising edge 9h = Edge detect / Both edge Ah = Edge detect / Falling edge Bh = Edge detect / Rising edge Ch = Counter / Both edge Dh = Counter / Falling edge Eh = Counter / Rising edge Fh = Counter / High-level reset

8.3.75 CNT9_FSM3_CFG2 Register (Offset = 389h) [Reset = 0Xh]

CNT9_FSM3_CFG2 is shown in Table 8-245.

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Table 8-245. CNT9_FSM3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UP_SYNC	R/W	0h	FSM UP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
6	KEEP_SYNC	R/W	0h	FSM KEEP SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
5	RST_SYNC	R/W	0h	CNT RST SYNC bypass option 0h = 2-DFF sync 1h = Bypass 2-DFF
4	RESERVED	R	0h	Reserved
3:2	CNT_INIT	R/W	Xh	CNT INIT VAL 0h = Bypass initial 1h = Initial Low 2h = Initial High 3h = Initial High (Reserved)
1	OUT_POL	R/W	Xh	CNT OUT POL 0h = Non-inverted 1h = Inverted

Table 8-245. CNT9_FSM3_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DLY_EDET	R/W	Xh	DLY EDGE DETECT option 0h = Delay function 1h = Enable edge detect on delay function

8.3.76 PWM_GEN0_CFG Register (Offset = 38Ah) [Reset = 0Xh]

PWM_GEN0_CFG is shown in Table 8-246.

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Table 8-246. PWM_GEN0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM_EN	R/W	0h	PWM EN 0h = Disabled 1h = Enabled
6:4	RESERVED	R	0h	Reserved
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

8.3.77 PWM_GEN1_CFG Register (Offset = 38Bh) [Reset = 0Xh]

PWM_GEN1_CFG is shown in Table 8-247.

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Table 8-247. PWM_GEN1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM_EN	R/W	0h	PWM EN 0h = Disabled 1h = Enabled
6:4	RESERVED	R	0h	Reserved
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

8.3.78 PWM_GEN2_CFG Register (Offset = 38Ch) [Reset = 0Xh]

PWM_GEN2_CFG is shown in Table 8-248.

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Table 8-248. PWM_GEN2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM_EN	R/W	0h	PWM EN 0h = Disabled 1h = Enabled
6:4	RESERVED	R	0h	Reserved

Table 8-248. PWM_GEN2_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

8.3.79 PWM_GEN3_CFG Register (Offset = 38Dh) [Reset = 0Xh]

PWM_GEN3_CFG is shown in Table 8-249.

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Table 8-249. PWM_GEN3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM_EN	R/W	0h	PWM EN 0h = Disabled 1h = Enabled
6:4	RESERVED	R	0h	Reserved
3:2	TDB_SEL	R/W	Xh	PWM Deadband time select 0h = 0 CLKs 1h = 1 CLK 2h = 2 CLKs 3h = 5 CLKs
1	OUTP_POL	R/W	Xh	PWM OUT1 POL 0h = Non-inverted output 1h = Inverted output
0	OUTN_POL	R/W	Xh	PWM OUT0 POL 0h = Non-inverted output 1h = Inverted output

8.3.80 PWM_SRC_CFG Register (Offset = 38Eh) [Reset = X0h]

PWM_SRC_CFG is shown in Table 8-250.

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Table 8-250. PWM_SRC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PWM3_DATA_SEL	R/W	0h	PWM3 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3
5:4	PWM2_DATA_SEL	R/W	0h	PWM2 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3
3:2	PWM1_DATA_SEL	R/W	Xh	PWM1 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3
1:0	PWM0_DATA_SEL	R/W	Xh	PWM0 DATA source select 0h = FSM0 1h = FSM1 2h = FSM2 3h = FSM3

8.3.81 SM_CFG0 Register (Offset = 38Fh) [Reset = XXh]

SM_CFG0 is shown in Table 8-251.

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Table 8-251. SM_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S1_IN0	R/W	Xh	STATE1 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S0_IN0	R/W	Xh	STATE0 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.82 SM_CFG1 Register (Offset = 390h) [Reset = XXh]

SM_CFG1 is shown in Table 8-252.

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Table 8-252. SM_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S1_IN1	R/W	Xh	STATE1 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S0_IN1	R/W	Xh	STATE0 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.83 SM_CFG2 Register (Offset = 391h) [Reset = 00h]

SM_CFG2 is shown in Table 8-253.

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Table 8-253. SM_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2:0	RESERVED	R	0h	Reserved

8.3.84 SM_CFG3 Register (Offset = 392h) [Reset = XXh]

SM_CFG3 is shown in Table 8-254.

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Table 8-254. SM_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S3_IN0	R/W	Xh	STATE3 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S2_IN0	R/W	Xh	STATE2 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.85 SM_CFG4 Register (Offset = 393h) [Reset = XXh]

SM_CFG4 is shown in Table 8-255.

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Table 8-255. SM_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S3_IN1	R/W	Xh	STATE3 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S2_IN1	R/W	Xh	STATE2 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.86 SM_CFG5 Register (Offset = 394h) [Reset = 00h]

SM_CFG5 is shown in Table 8-256.

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Table 8-256. SM_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2:0	RESERVED	R	0h	Reserved

8.3.87 SM_CFG6 Register (Offset = 395h) [Reset = XXh]

SM_CFG6 is shown in Table 8-257.

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Table 8-257. SM_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S5_IN0	R/W	Xh	STATE5 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S4_IN0	R/W	Xh	STATE4 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.88 SM_CFG7 Register (Offset = 396h) [Reset = XXh]

SM_CFG7 is shown in Table 8-258.

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Table 8-258. SM_CFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S5_IN1	R/W	Xh	STATE5 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S4_IN1	R/W	Xh	STATE4 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.89 SM_CFG8 Register (Offset = 397h) [Reset = 00h]

SM_CFG8 is shown in Table 8-259.

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Table 8-259. SM_CFG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2:0	RESERVED	R	0h	Reserved

8.3.90 SM_CFG9 Register (Offset = 398h) [Reset = XXh]

SM_CFG9 is shown in Table 8-260.

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Table 8-260. SM_CFG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S7_IN0	R/W	Xh	STATE7 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S6_IN0	R/W	Xh	STATE6 IN0 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.91 SM_CFG10 Register (Offset = 399h) [Reset = XXh]

SM_CFG10 is shown in Table 8-261.

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Table 8-261. SM_CFG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	SM_S7_IN1	R/W	Xh	STATE7 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7
3	RESERVED	R	0h	Reserved
2:0	SM_S6_IN1	R/W	Xh	STATE6 IN1 transition FROM select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.92 SM_CFG11 Register (Offset = 39Ah) [Reset = 00h]

SM_CFG11 is shown in Table 8-262.

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Table 8-262. SM_CFG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SM_SYNC_EN	R/W	0h	State machine synchronous mode clock sync enable 0h = Disabled 1h = Enabled
6:4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved

Table 8-262. SM_CFG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	R	0h	Reserved

8.3.93 SM_CFG12 Register (Offset = 3A7h) [Reset = X0h]

SM_CFG12 is shown in Table 8-263.

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Table 8-263. SM_CFG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SM_CLK_SEL	R/W	0h	State machine CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2.048kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Previous CNT out (CNT4) Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3	MODE_SEL	R/W	Xh	State machine synchronous mode select 0h = Asynchronous 1h = Synchronous
2:0	SM_INIT_STATE	R/W	Xh	State machine initial state select 0h = S0 1h = S1 2h = S2 3h = S3 4h = S4 5h = S5 6h = S6 7h = S7

8.3.94 SM_CFG13 Register (Offset = 3A8h) [Reset = X0h]

SM_CFG13 is shown in Table 8-264.

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Table 8-264. SM_CFG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S0_OUT_CFG	R/W	Xh	

8.3.95 SM_CFG14 Register (Offset = 3A9h) [Reset = X0h]

SM_CFG14 is shown in Table 8-265.

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Table 8-265. SM_CFG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S1_OUT_CFG	R/W	Xh	

8.3.96 SM_CFG15 Register (Offset = 3AAh) [Reset = X0h]

SM_CFG15 is shown in Table 8-266.

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Table 8-266. SM_CFG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S2_OUT_CFG	R/W	Xh	

8.3.97 SM_CFG16 Register (Offset = 3ABh) [Reset = X0h]

SM_CFG16 is shown in Table 8-267.

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Table 8-267. SM_CFG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S3_OUT_CFG	R/W	Xh	

8.3.98 SM_CFG17 Register (Offset = 3ACh) [Reset = X0h]

SM_CFG17 is shown in Table 8-268.

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Table 8-268. SM_CFG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S4_OUT_CFG	R/W	Xh	

8.3.99 SM_CFG18 Register (Offset = 3ADh) [Reset = X0h]

SM_CFG18 is shown in Table 8-269.

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Table 8-269. SM_CFG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S5_OUT_CFG	R/W	Xh	

8.3.100 SM_CFG19 Register (Offset = 3AEh) [Reset = X0h]

SM_CFG19 is shown in Table 8-270.

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Table 8-270. SM_CFG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S6_OUT_CFG	R/W	Xh	

8.3.101 SM_CFG20 Register (Offset = 3AFh) [Reset = X0h]

SM_CFG20 is shown in Table 8-271.

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Table 8-271. SM_CFG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	S7_OUT_CFG	R/W	Xh	

8.3.102 WDT_CFG0 Register (Offset = 3B8h) [Reset = X0h]

WDT_CFG0 is shown in Table 8-272.

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Table 8-272. WDT_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WDT_TIMEOUT_DATA	R/W	Xh	WDT Timeout Period Counter DATA

8.3.103 WDT_CFG1 Register (Offset = 3B9h) [Reset = X0h]

WDT_CFG1 is shown in Table 8-273.

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Table 8-273. WDT_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	WDT_OUT_DATA	R/W	Xh	WDT Output Period Counter DATA

8.3.104 WDT_CFG2 Register (Offset = 3BAh) [Reset = 0Xh]

WDT_CFG2 is shown in Table 8-274.

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Table 8-274. WDT_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	WDT_CLK_SEL	R/W	0h	WDT CLK SEL 0h = OSC1 (25MHz) 1h = OSC1 / 4 2h = OSC1 / 8 3h = OSC1 / 64 4h = OSC1 / 512 5h = OSC0 (2kHz or 10kHz) 6h = OSC0 / 8 7h = OSC0 / 12 8h = OSC0 / 24 9h = OSC0 / 64 Ah = OSC0 / 512 Bh = OSC0 / 4096 Ch = Reserved Dh = External CLK from CMX Eh = Reserved Fh = Reserved
3	RESERVED	R	0h	Reserved
2	WDT_EN	R/W	Xh	WDT EN 0h = Disabled 1h = Enabled
1	WDT_100X_EN	R/W	Xh	WDT 100X CLK multiplier EN 0h = Disabled 1h = Enabled
0	WDT_EN_SEL	R/W	Xh	WDT EN function select 0h = Reset CNT 1h = Pause CNT

8.3.105 PFLT_CFG Register (Offset = 3BBh) [Reset = XXh]

PFLT_CFG is shown in Table 8-275.

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Table 8-275. PFLT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-275. PFLT_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	PFLT_DLY_SEL	R/W	Xh	Programmable filter delay value select 0h = 125 ns 1h = 250 ns 2h = 375 ns 3h = 500 ns
3	PFLT_POL	R/W	Xh	Programmable filter output polarity select 0h = Non-inverted 1h = Inverted
2	RESERVED	R	0h	Reserved
1:0	PFLT_EDGE_SEL	R/W	Xh	Programmable filter edge select 0h = Rising edge 1h = Falling edge 2h = Both edge 3h = Filter

8.3.106 FLT_CFG Register (Offset = 3BDh) [Reset = 0Xh]

FLT_CFG is shown in Table 8-276.

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Table 8-276. FLT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	FLT_POL	R/W	Xh	Filter output polarity select 0h = Non-inverted 1h = Inverted
2	RESERVED	R	0h	Reserved
1:0	FLT_EDGE_SEL	R/W	Xh	Filter / Edge detect edge select 0h = Rising edge 1h = Falling edge 2h = Both edge 3h = Filter

8.3.107 OSC0_CFG0 Register (Offset = 3BEh) [Reset = XXh]

OSC0_CFG0 is shown in Table 8-277.

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Table 8-277. OSC0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	CTRL_SRC	R/W	Xh	OSC power control source select 0h = From register 1h = From CMX
5	CTRL_SEL	R/W	Xh	OSC power control polarity select 0h = Power down (High turns off OSC) 1h = Force on (High turns on OSC)
4	SRC_SEL	R/W	Xh	OSC frequency source select 0h = Internal OSC 1h = External clock (from IO7)
3:2	PDIV	R/W	Xh	OSC pre-divider select 0h = / 1 1h = / 2 2h = / 4 3h = / 8
1	FREQ_SEL	R/W	Xh	OSC frequency select 0h = 2 kHz 1h = 10 kHz
0	PWR_MODE	R/W	Xh	OSC power mode select 0h = Auto power on 1h = Force power on

8.3.108 OSC0_CFG1 Register (Offset = 3BFh) [Reset = X0h]

OSC0_CFG1 is shown in Table 8-278.

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Table 8-278. OSC0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT1_EN	R/W	0h	OSC OUT1 enable 0h = Disabled 1h = Enabled
6:4	OUT1_DIV	R/W	0h	OSC OUT1 secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64
3	OUT0_EN	R/W	Xh	OSC OUT0 enable 0h = Disabled 1h = Enabled
2:0	OUT0_DIV	R/W	Xh	OSC OUT0 secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64

8.3.109 OSC1_CFG0 Register (Offset = 3C0h) [Reset = X0h]

OSC1_CFG0 is shown in Table 8-279.

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Table 8-279. OSC1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SU_DLY	R/W	0h	OSC 100ns startup delay control 0h = Enabled 1h = Disabled
6	CTRL_SRC	R/W	0h	OSC power control source select 0h = From register 1h = From CMX
5	CTRL_SEL	R/W	0h	OSC power control polarity select 0h = Power down (High turns off OSC) 1h = Force on (High turns on OSC)
4	SRC_SEL	R/W	0h	OSC frequency source select 0h = Internal OSC 1h = External clock (from IN0)
3:1	PDIV	R/W	Xh	OSC pre-divider select 0h = / 1 1h = / 2 2h = / 4 3h = / 8 4h = / 12 5h = / 24 6h = / 48 7h = Reserved
0	PWR_MODE	R/W	Xh	OSC power mode select 0h = Auto power on 1h = Force power on

8.3.110 OSC1_CFG1 Register (Offset = 3C1h) [Reset = 0Xh]

OSC1_CFG1 is shown in Table 8-280.

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Table 8-280. OSC1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	OUT_EN	R/W	Xh	OSC OUT enable 0h = Disabled 1h = Enabled
2:0	OUT_DIV	R/W	Xh	OSC OUT secondary divider select 0h = / 1 1h = / 2 2h = / 3 3h = / 4 4h = / 8 5h = / 12 6h = / 24 7h = / 64

8.3.111 OSC1_CG Register (Offset = 3C5h) [Reset = X0h]

OSC1_CG is shown in Table 8-281.

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Table 8-281. OSC1_CG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OSC1_DIV3	R/W	0h	Disable /3, /12, and /24 dividers. 0h = Divider enabled 1h = Divider disabled
6	OSC1_DIV512	R/W	0h	Disable /512 divider. 0h = Divider enabled 1h = Divider disabled
5	OSC1_DIV64	R/W	0h	Disable /64 and /512 dividers. 0h = Divider enabled 1h = Divider disabled
4	OSC1_DIV24	R/W	0h	Disable /3, /12, and /24 dividers. 0h = Divider enabled 1h = Divider disabled
3	OSC1_DIV12	R/W	Xh	Disable /3 and /12 dividers. 0h = Divider enabled 1h = Divider disabled
2	OSC1_DIV8	R/W	Xh	Disable /8, /64, and /512 dividers. 0h = Divider enabled 1h = Divider disabled
1	OSC1_DIV4	R/W	Xh	Disable /4, /8, /64, and /512 dividers. 0h = Divider enabled 1h = Divider disabled
0	OSC1_DIV2	R/W	Xh	Disable /2, /4, /8, /64, and /512 dividers. 0h = Divider enabled 1h = Divider disabled

8.3.112 MCACMP_CFG0 Register (Offset = 3CFh) [Reset = 0Xh]

MCACMP_CFG0 is shown in Table 8-282.

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Table 8-282. MCACMP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TS_INP_EN	R/W	0h	Temperature sensor input to McACMP enable 0h = Disabled 1h = Enabled
6	VCC_INP_EN	R/W	0h	VCC input to McACMP enable 0h = Disabled 1h = Enabled
5	SYNC_EN	R/W	0h	McACMP output synchronicity select 0h = Asynchronous 1h = Synchronous
4	MCS_MODE	R/W	0h	McACMP trigger mode select 0h = Level sensitive EN mode 1h = Edge sensitive EN mode

Table 8-282. MCACMP_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	CH_EN	R/W	0h	Number of channels sampled select 0h = 1 channel 1h = 2 channels 2h = 3 channels 3h = 4 channels
1	RESERVED	R	0h	Reserved
0	MCS_EN	R/W	Xh	Sampling mode select 0h = Regular mode (single channel) 1h = Multi-channel mode

8.3.113 MCACMP_CFG1 Register (Offset = 3D0h) [Reset = 0Xh]

MCACMP_CFG1 is shown in Table 8-283.

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Table 8-283. MCACMP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:3	RESERVED	R	0h	Reserved
2	EDGE_SEL	R/W	Xh	McACMP sampling edge select 0h = Sample on negative edge of CLK 1h = Sample on positive edge of CLK
1:0	MCS_CLK_SEL	R/W	Xh	McACMP CLK select 0h = OSC0 (2kHz or 10kHz) 1h = OSC0 / 2 2h = OSC0 / 4 3h = OSC0 / 8

8.3.114 MCACMP_CH0_CFG0 Register (Offset = 3D1h) [Reset = XXh]

MCACMP_CH0_CFG0 is shown in Table 8-284.

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Table 8-284. MCACMP_CH0_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH0 RST EN select 0h = Disabled 1h = Enabled
5:4	INP_SEL	R/W	Xh	McACMP CH0 input source select 0h = AIO0 1h = AIO1 2h = AIO2 (or VCC) 3h = AIO3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH0 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH0 hysteresis select 0h = 0 mV 1h = 32 mV 2h = 64 mV 3h = 192 mV

8.3.115 MCACMP_CH0_CFG1 Register (Offset = 3D2h) [Reset = XXh]

MCACMP_CH0_CFG1 is shown in Table 8-285.

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Table 8-285. MCACMP_CH0_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_SEL	R/W	Xh	McACMP CH0 VREF select 0h = 32 mV 1h = 64 mV 2h = 96 mV 3h = 128 mV 4h = 160 mV 5h = 192 mV 6h = 224 mV 7h = 256 mV 8h = 288 mV 9h = 320 mV Ah = 352 mV Bh = 384 mV Ch = 416 mV Dh = 448 mV Eh = 480 mV Fh = 512 mV 10h = 544 mV 11h = 576 mV 12h = 608 mV 13h = 640 mV 14h = 672 mV 15h = 704 mV 16h = 736 mV 17h = 768 mV 18h = 800 mV 19h = 832 mV 1Ah = 864 mV 1Bh = 896 mV 1Ch = 928 mV 1Dh = 960 mV 1Eh = 992 mV 1Fh = 1.024 V 20h = 1.056 V 21h = 1.088 V 22h = 1.120 V 23h = 1.152 V 24h = 1.184 V 25h = 1.216 V 26h = 1.248 V 27h = 1.280 V 28h = 1.312 V 29h = 1.344 V 2Ah = 1.376 V 2Bh = 1.408 V 2Ch = 1.440 V 2Dh = 1.472 V 2Eh = 1.504 V 2Fh = 1.536 V 30h = 1.568 V 31h = 1.600 V 32h = 1.632 V 33h = 1.664 V 34h = 1.696 V 35h = 1.728 V 36h = 1.760 V 37h = 1.792 V 38h = 1.824 V 39h = 1.856 V 3Ah = 1.888 V 3Bh = 1.920 V 3Ch = 1.952 V 3Dh = 1.984 V 3Eh = 2.016 V 3Fh = External VREF

8.3.116 MCACMP_CH1_CFG0 Register (Offset = 3D6h) [Reset = XXh]

MCACMP_CH1_CFG0 is shown in Table 8-286.

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Table 8-286. MCACMP_CH1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH1 RST EN select 0h = Disabled 1h = Enabled

Table 8-286. MCACMP_CH1_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	INP_SEL	R/W	Xh	McACMP CH1 input source select 0h = AIO0 1h = AIO1 2h = AIO2 (or VCC) 3h = AIO3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH1 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH1 hysteresis select 0h = 0 mV 1h = 32 mV 2h = 64 mV 3h = 192 mV

8.3.117 MCACMP_CH1_CFG1 Register (Offset = 3D7h) [Reset = XXh]

MCACMP_CH1_CFG1 is shown in Table 8-287.

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Table 8-287. MCACMP_CH1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_SEL	R/W	Xh	McACMP CH1 VREF select (same options as CH0)

8.3.118 MCACMP_CH2_CFG0 Register (Offset = 3DBh) [Reset = XXh]

MCACMP_CH2_CFG0 is shown in Table 8-288.

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Table 8-288. MCACMP_CH2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH2 RST EN select 0h = Disabled 1h = Enabled
5:4	INP_SEL	R/W	Xh	McACMP CH2 input source select 0h = AIO0 1h = AIO1 2h = AIO2 (or VCC) 3h = AIO3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH2 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH2 hysteresis select 0h = 0 mV 1h = 32 mV 2h = 64 mV 3h = 192 mV

8.3.119 MCACMP_CH2_CFG1 Register (Offset = 3DCh) [Reset = XXh]

MCACMP_CH2_CFG1 is shown in Table 8-289.

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Table 8-289. MCACMP_CH2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved

Table 8-289. MCACMP_CH2_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	VREF_SEL	R/W	Xh	McACMP CH2 VREF select (same options as CH0)

8.3.120 MCACMP_CH3_CFG0 Register (Offset = 3E0h) [Reset = XXh]

MCACMP_CH3_CFG0 is shown in Table 8-290.

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Table 8-290. MCACMP_CH3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RST_EN	R/W	Xh	McACMP CH3 RST EN select 0h = Disabled 1h = Enabled
5:4	INP_SEL	R/W	Xh	McACMP CH3 input source seelct 0h = AIO0 1h = AIO1 2h = AIO2 (or VCC) 3h = AIO3 (or TS)
3:2	GAIN_SEL	R/W	Xh	McACMP CH3 gain select 0h = 1X 1h = 0.5X 2h = 0.33X 3h = 0.25X
1:0	HYS_SEL	R/W	Xh	McACMP CH3 hysteresis select 0h = 0 mV 1h = 32 mV 2h = 64 mV 3h = 192 mV

8.3.121 MCACMP_CH3_CFG1 Register (Offset = 3E1h) [Reset = XXh]

MCACMP_CH3_CFG1 is shown in Table 8-291.

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Table 8-291. MCACMP_CH3_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:0	VREF_SEL	R/W	Xh	McACMP CH3 VREF select (same options as CH0)

8.3.122 SER_COMM_CFG0 Register (Offset = 3F2h) [Reset = X0h]

SER_COMM_CFG0 is shown in Table 8-292.

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Table 8-292. SER_COMM_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I2C_ADDR_SRC_SEL	R/W	0h	I2C HW address source select (bitwise) 0h = OTP 1h = IO
3	I2C_IO_LAT	R/W	Xh	I2C HW addressing IO latching select 0h = Enabled 1h = Disabled
2	I2C_RST_EN	R/W	Xh	I2C Global Reset listening select 0h = Disabled 1h = Enabled
1	I2C_EN	R/W	Xh	I2C serial communications enable select 0h = Disabled 1h = Enabled
0	SPI_EN	R/W	Xh	SPI serial communications enable select 0h = Disabled 1h = Enabled

8.3.123 SER_COMM_CFG1 Register (Offset = 3F3h) [Reset = 00h]

SER_COMM_CFG1 is shown in Table 8-293.

Return to the Summary Table.

Table 8-293. SER_COMM_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I2C_ADDR_MSB	R/W	0h	I2C HW address
3:1	I2C_ADDR_LSB	R/W	0h	I2C HW address
0	RESERVED	R	0h	Reserved

8.3.124 MISC_CFG0 Register (Offset = 3F7h) [Reset = 00h]

MISC_CFG0 is shown in Table 8-294.

Return to the Summary Table.

Table 8-294. MISC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_QC	R/W	0h	GPIO quick charge control 0h = Disabled 1h = Enabled
6	CFG_RD_LCK	R/W	0h	CFG read lock control 0h = Disabled 1h = Enabled
5	CFG_WR_LCK	R/W	0h	CFG write lock control 0h = Disabled 1h = Enabled
4	OTP_WR_LCK	R/W	0h	OTP write lock control 0h = Disabled 1h = Enabled
3:2	USER_LCK	R/W	0h	USER read/write lock control 0h = R/W to all non-reserved, non-read-only registers 1h = R/W to only Counter DATA, Watchdog Timer DATA, and Pattern Generator registers 2h = R/W to only State Machine registers 3h = R/W to only Voltage Reference select registers
1:0	RESERVED	R	0h	Reserved

8.3.125 MISC_CFG1 Register (Offset = 3F8h) [Reset = 0Xh]

MISC_CFG1 is shown in Table 8-295.

Return to the Summary Table.

Table 8-295. MISC_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	VBG_CTRL	R/W	0h	Bandgap control
3	RESERVED	R	0h	Reserved
2:0	PREBIAS_CTRL	R/W	Xh	Prebias control 0h = Auto on for Serial Comms. only 1h = Auto on for Serial Comms., DFF, PGEN, and Shift Reg. 2h = Auto on for Serial Comms. and counters with ext. clock 3h = Force on 4h = Auto on for Serial Comms. and OSC1 5h = Auto on for Serial Comms., DFF, PGEN, Shift Reg., and OSC1 6h = Auto on for Serial Comms., PGEN, and counters with ext. clock 7h = Force off

8.3.126 MISC_CFG2 Register (Offset = 3F9h) [Reset = 0Xh]

MISC_CFG2 is shown in Table 8-296.

Return to the Summary Table.

Table 8-296. MISC_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	RD_DATA_SYNC	R/W	Xh	Read data sync control 0h = Enabled 1h = Disabled

8.3.127 DEVICE_ID4 Register (Offset = 3FAh) [Reset = X0h]

DEVICE_ID4 is shown in Table 8-297.

Return to the Summary Table.

Table 8-297. DEVICE_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID4	R	Xh	Device ID

8.3.128 DEVICE_ID5 Register (Offset = 3FBh) [Reset = X0h]

DEVICE_ID5 is shown in Table 8-298.

Return to the Summary Table.

Table 8-298. DEVICE_ID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID5	R	Xh	Device ID

8.3.129 DEVICE_ID6 Register (Offset = 3FCh) [Reset = X0h]

DEVICE_ID6 is shown in Table 8-299.

Return to the Summary Table.

Table 8-299. DEVICE_ID6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID6	R	Xh	Device ID

8.3.130 DEVICE_ID7 Register (Offset = 3FDh) [Reset = X0h]

DEVICE_ID7 is shown in Table 8-300.

Return to the Summary Table.

Table 8-300. DEVICE_ID7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID7	R	Xh	Device ID

8.3.131 CRC_LSB Register (Offset = 3FEh) [Reset = X0h]

CRC_LSB is shown in Table 8-301.

Return to the Summary Table.

Table 8-301. CRC_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC_LSB	R/W	Xh	CRC LSB for 2kb OTP

8.3.132 CRC_MSB Register (Offset = 3FFh) [Reset = X0h]

CRC_MSB is shown in Table 8-302.

Return to the Summary Table.

Table 8-302. CRC_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC_MSB	R/W	Xh	CRC MSB for 2kb OTP

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The configurable logic and timing blocks of TPLD1202 allow for the device to provide symmetric power-up and power-down signals for numerous components. In this application the device is configured to output the maximum amount of power- up and power-down sequencing signals based on a counter/delay macro-cell.

9.2 Typical Application

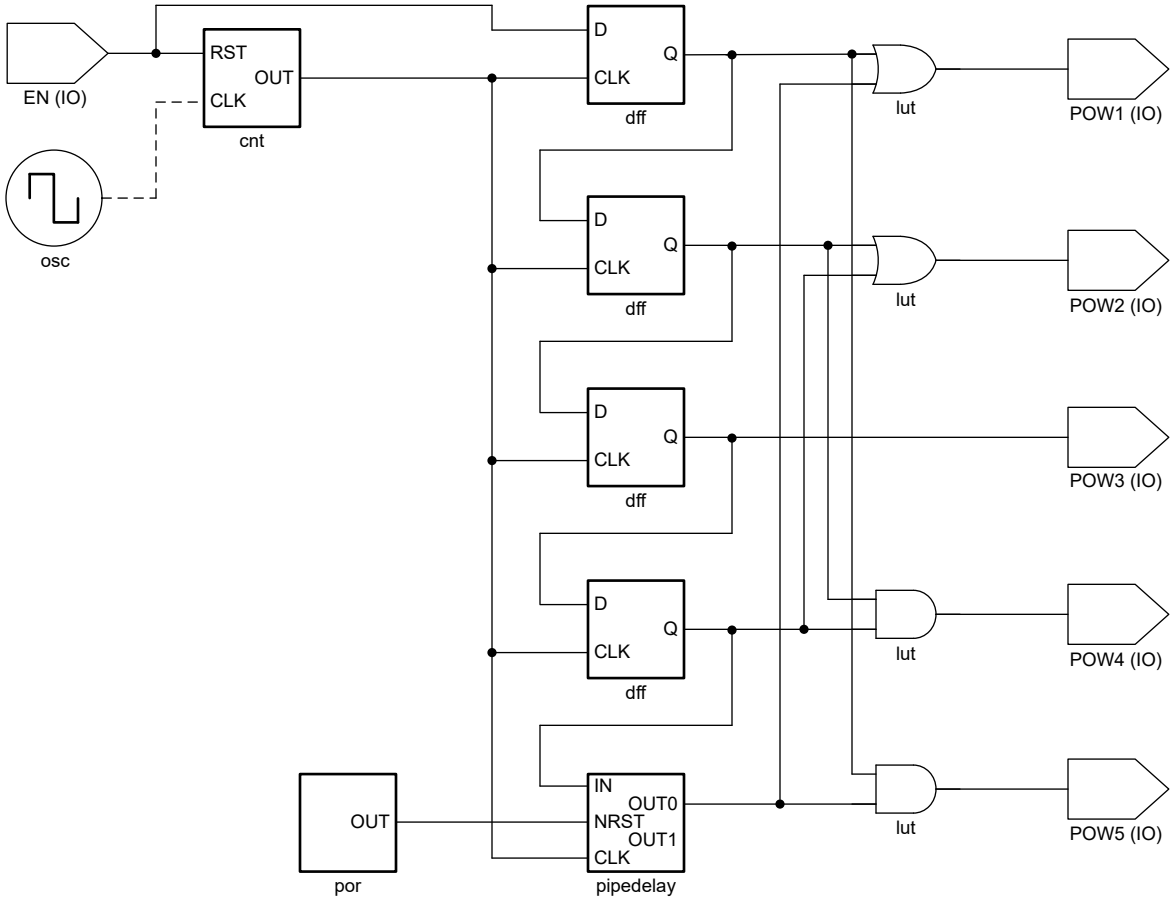


Figure 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the TPLD1202 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the TPLD1202 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The TPLD1202 can drive a load with a total capacitance less than or equal to 15pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 15pF.

The TPLD1202 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} andV_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ or $V_{t-(min)}$ to be considered a logic LOW, and $V_{IH(min)}$ or $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the unused inputs can be connected with a pull-up or pull-down resistor if the input is used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the TPLD1202 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The TPLD1202 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

The TPLD1202 can be used with no signal transition rate requirements because the device has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value provides the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*.The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the TPLD1202 to the receiving device.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

9.2.3 Application Curves

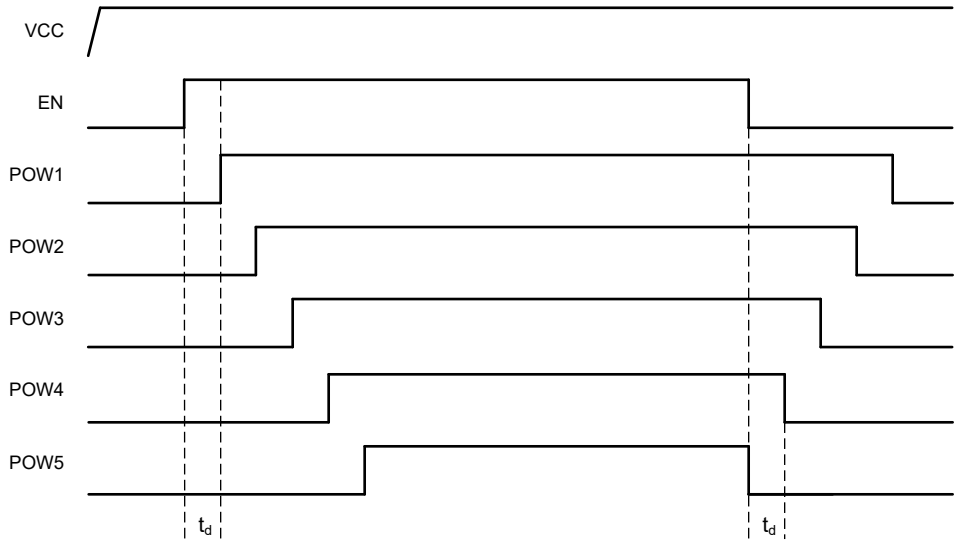


Figure 9-2. Application Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

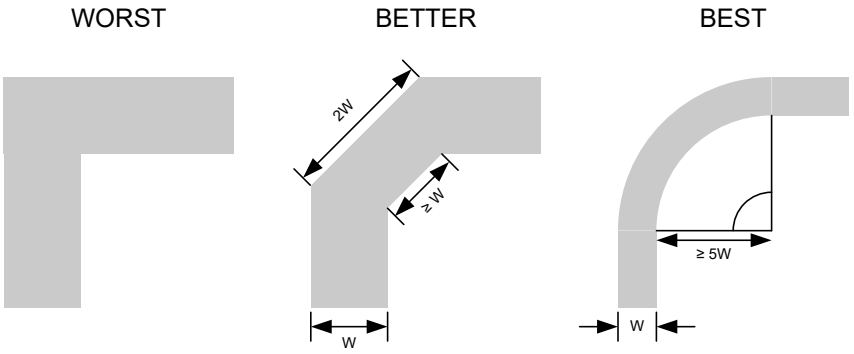


Figure 9-3. Example trace corners for improved signal integrity

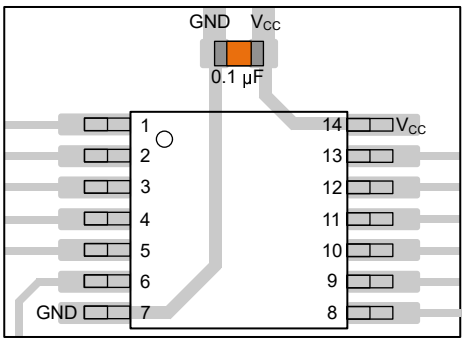


Figure 9-4. Example bypass capacitor placement for TSSOP and similar packages

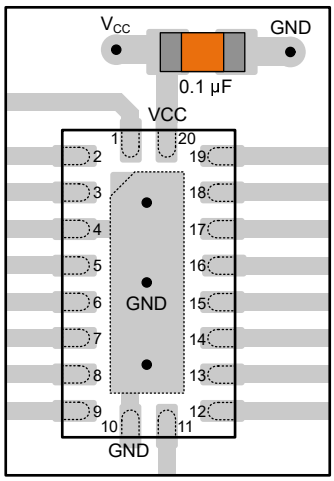


Figure 9-5. Example bypass capacitor placement for WQFN and similar packages

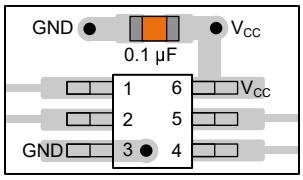


Figure 9-6. Example bypass capacitor placement for SOT, SC70 and similar packages

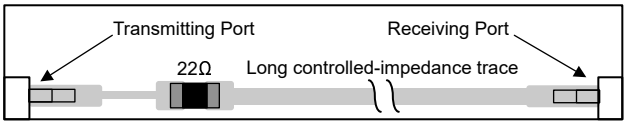


Figure 9-7. Example damping resistor placement for improved signal integrity

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2026) to Revision B (August 2026)	Page
• Changed the document status from *Advance Information* to *Production Data*	1
• First public release of datasheet	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPLD1202DYYR	Active	Preproduction	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPLD1202DYYR.A	Active	Preproduction	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPLD1202RWBR	Active	Preproduction	X2QFN (RWB) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPLD1202RWBR.A	Active	Preproduction	X2QFN (RWB) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPLD1202RWSR	Active	Preproduction	X2QFN (RWS) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPLD1202RWBR	Active	Production	X2QFN (RWB) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TO
TPLD1202RWSR	Active	Production	X2QFN (RWS) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	TP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPLD1202 :

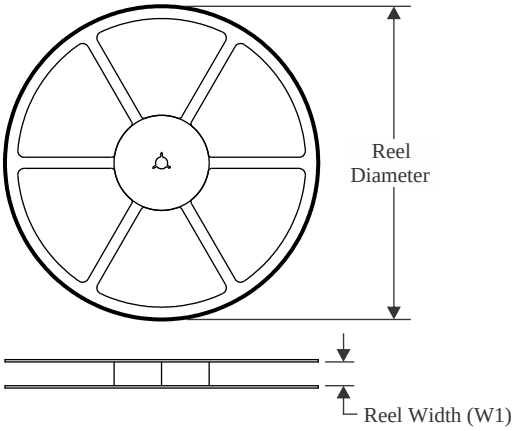
- Automotive : TPLD1202-Q1

NOTE: Qualified Version Definitions:

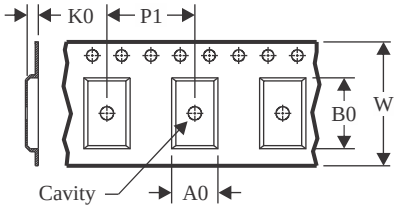
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

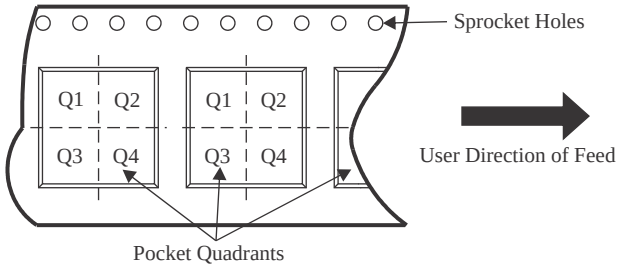


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

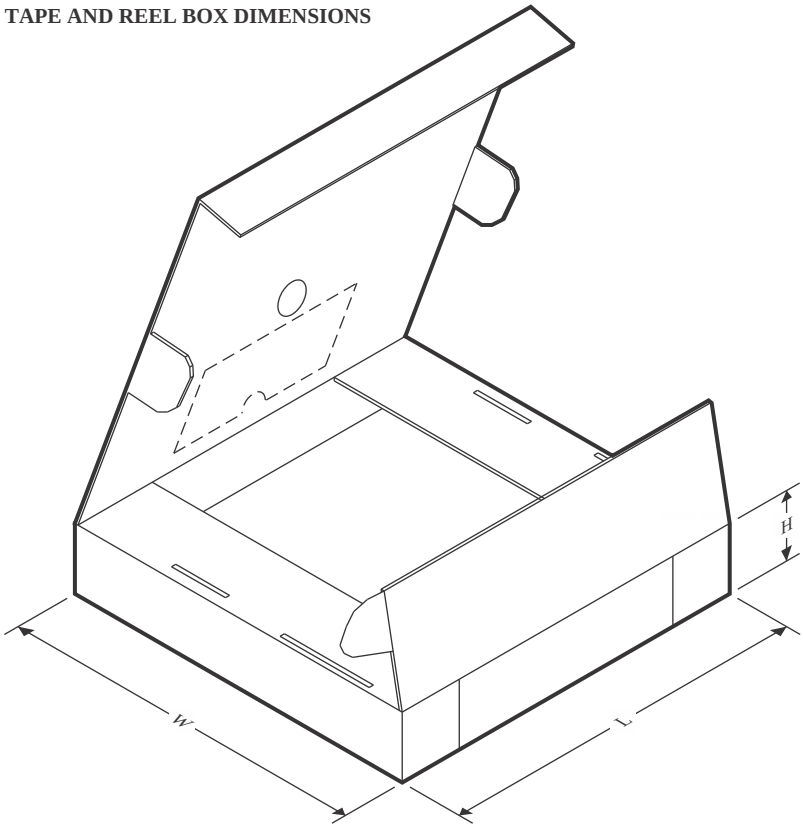
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPLD1202RWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q2
TPLD1202RWSR	X2QFN	RWS	12	3000	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

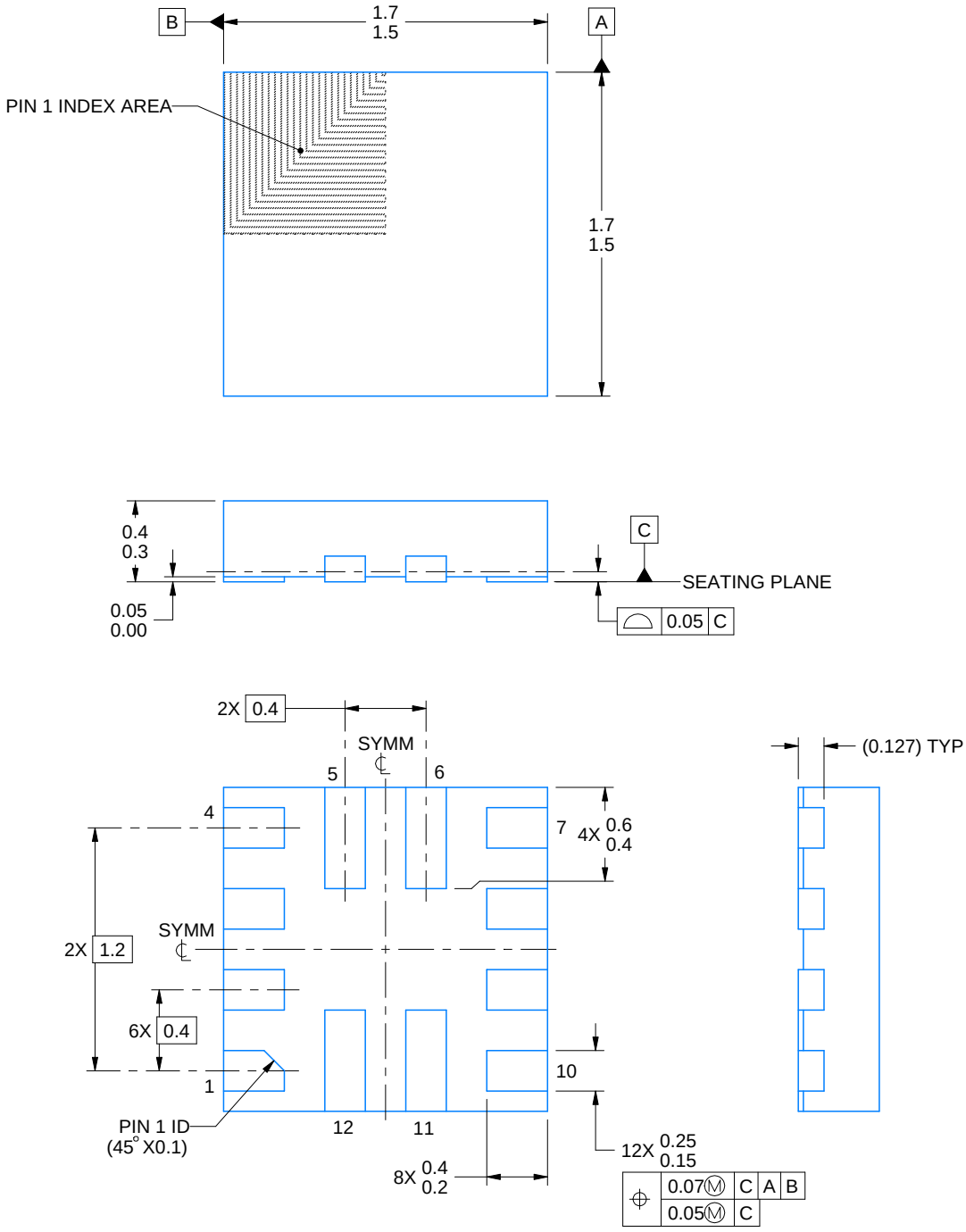
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPLD1202RWBR	X2QFN	RWB	12	3000	210.0	185.0	35.0
TPLD1202RWSR	X2QFN	RWS	12	3000	210.0	185.0	35.0

RWS0012A

PACKAGE OUTLINE

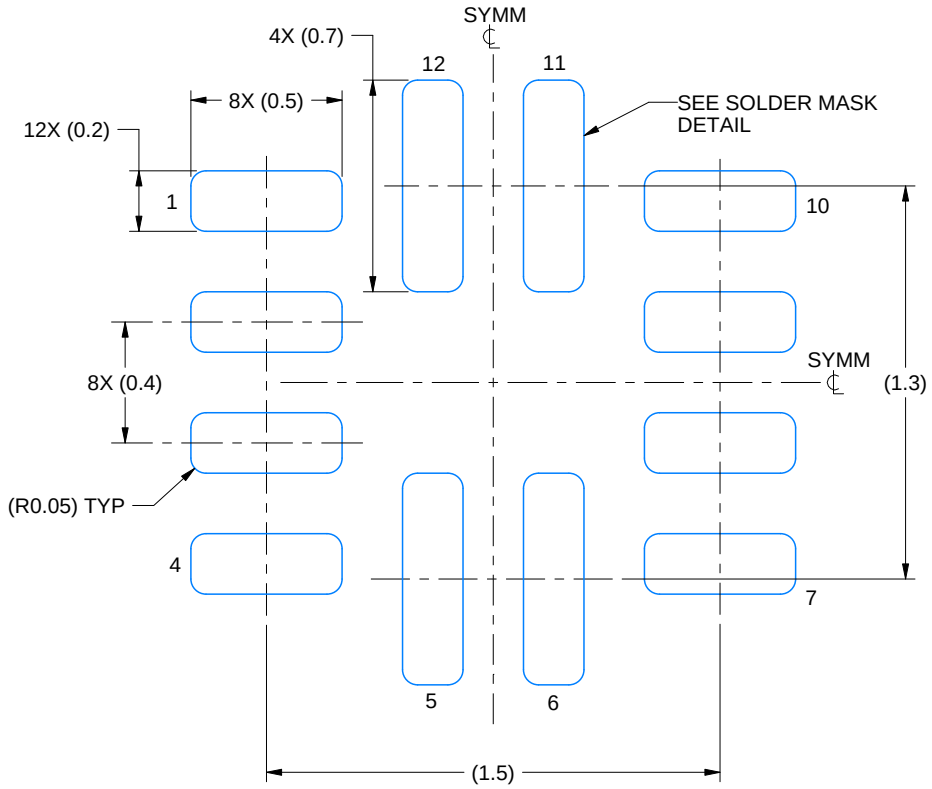
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

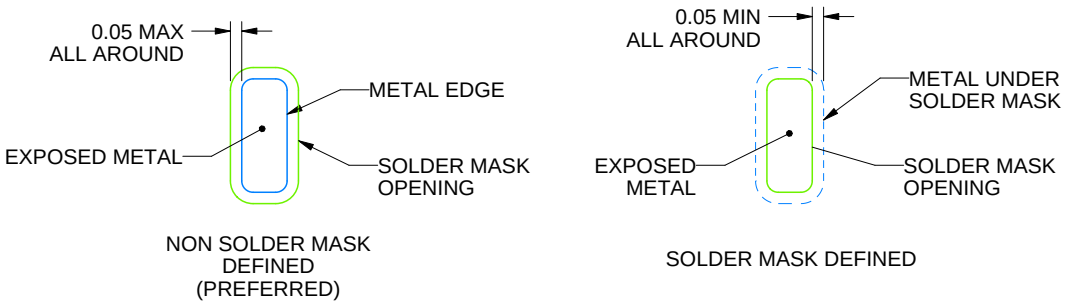


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

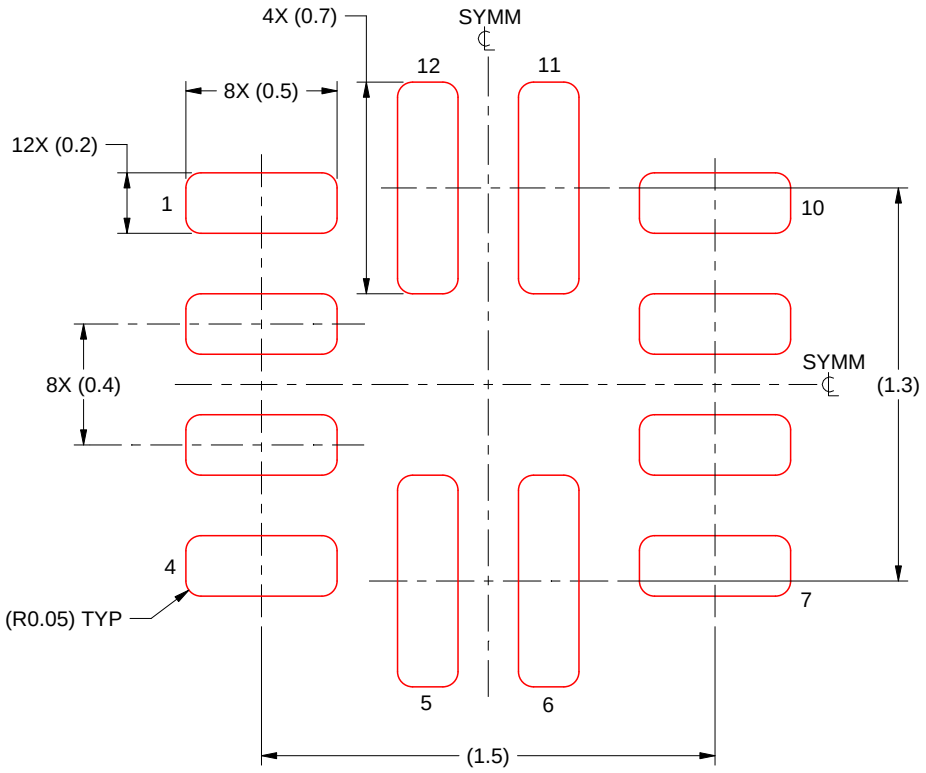


SOLDER MASK DETAILS

4231917/A 05/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 40X

4231917/A 05/2025

NOTES: (continued)

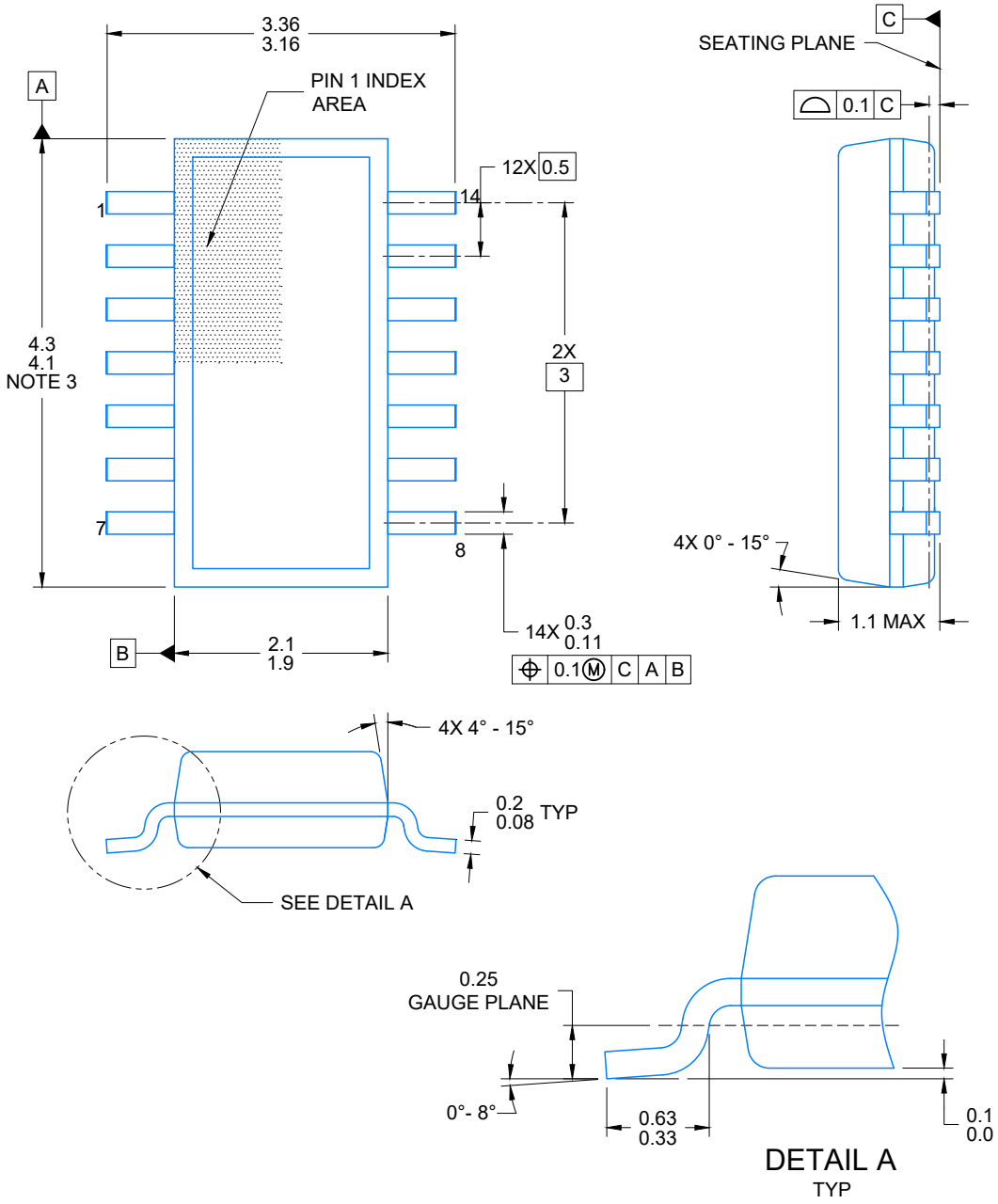
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0014A

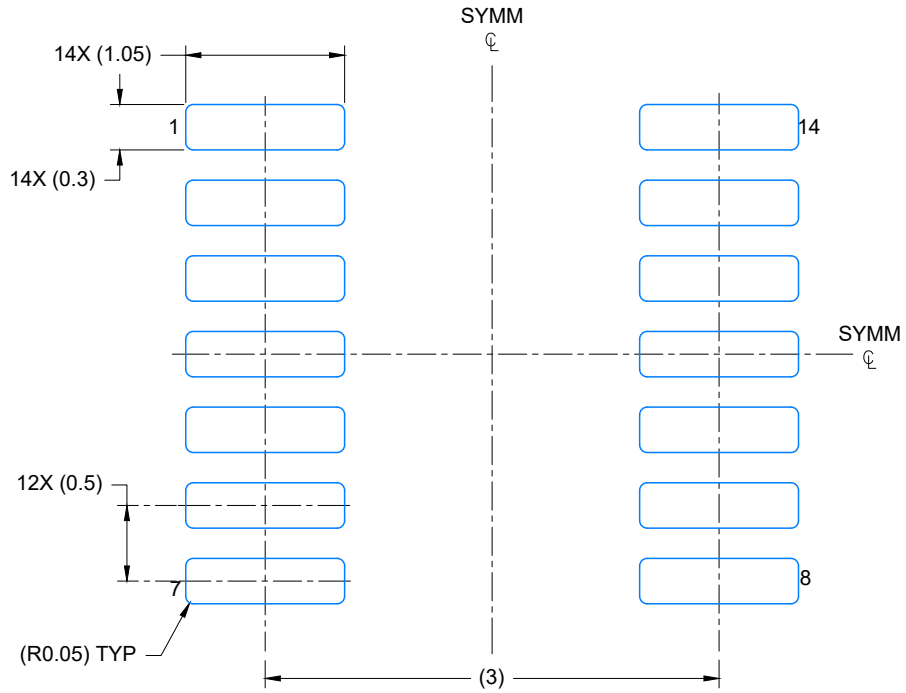
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

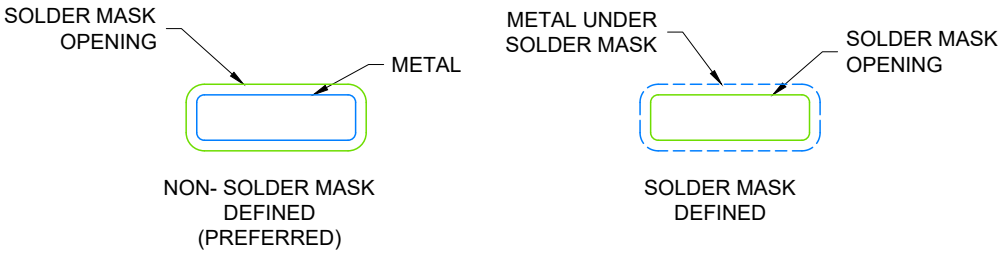


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

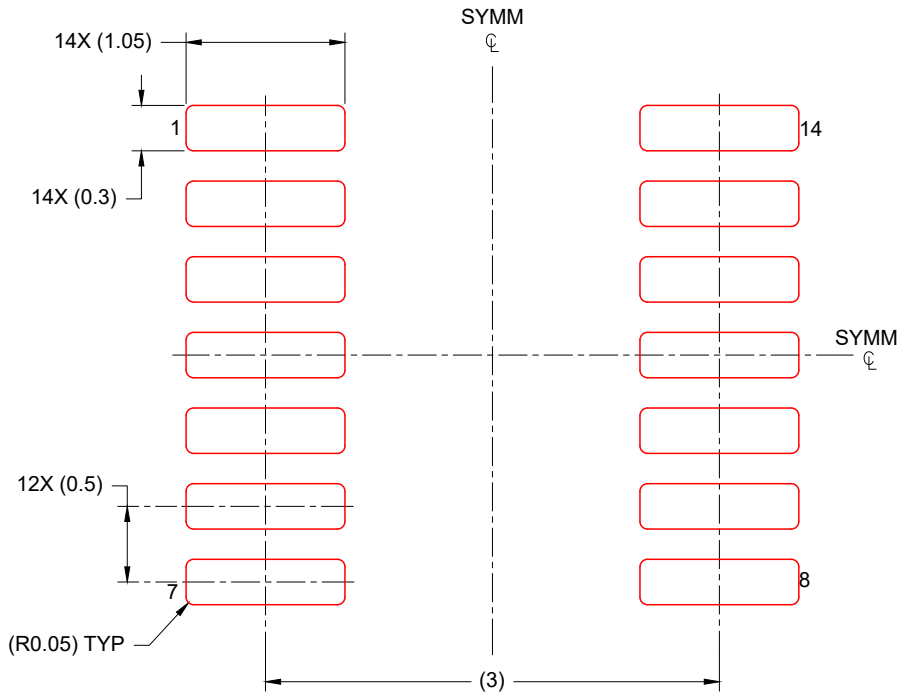


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

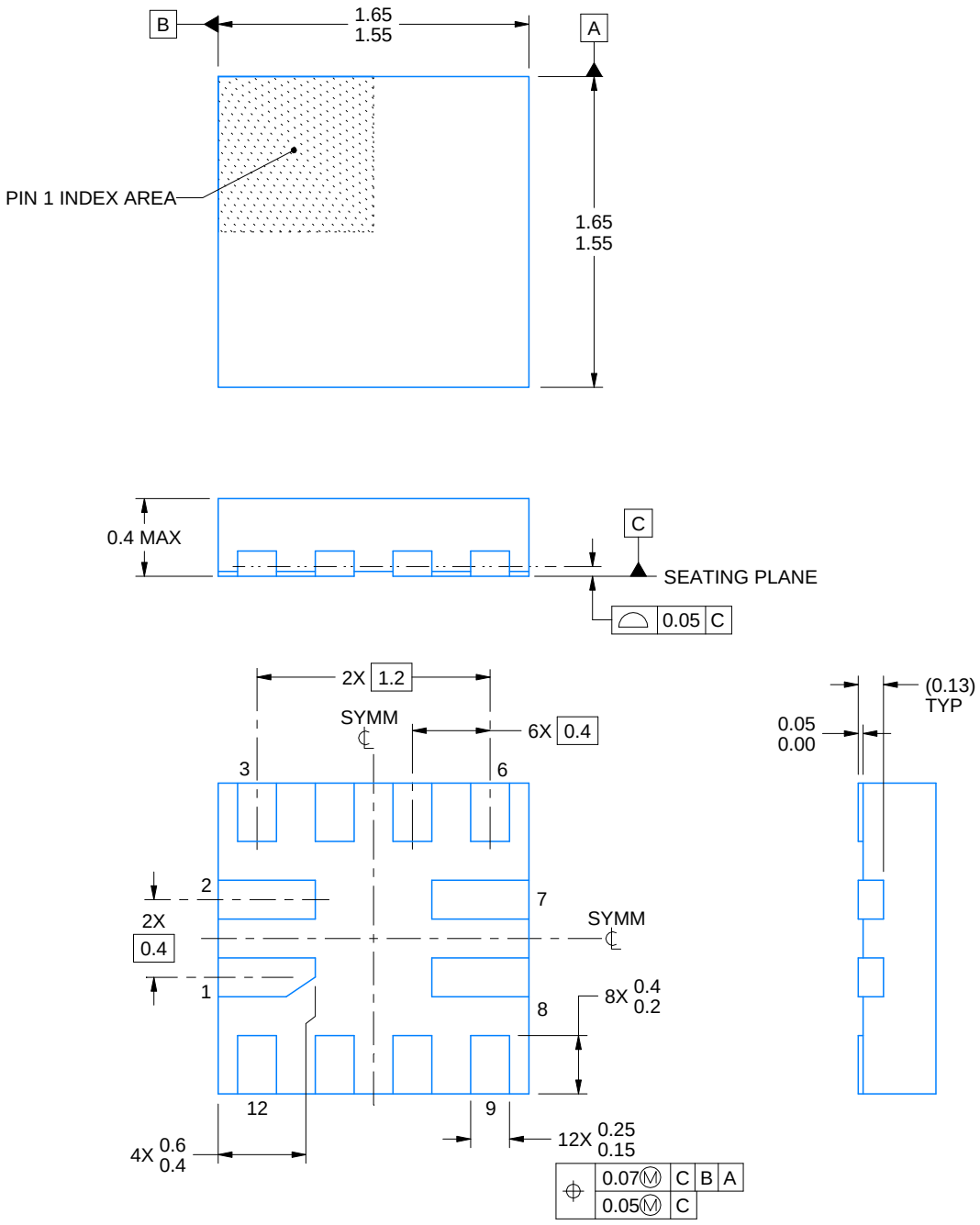
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RWB0012A

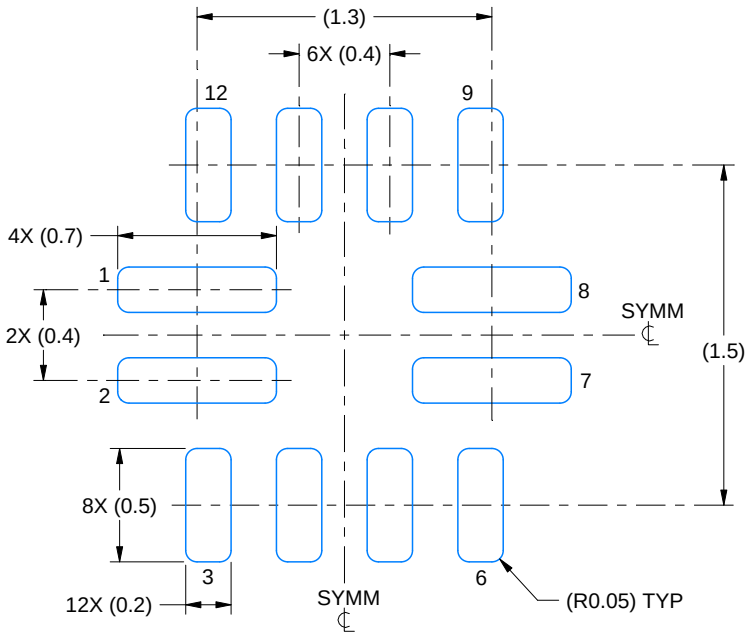
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

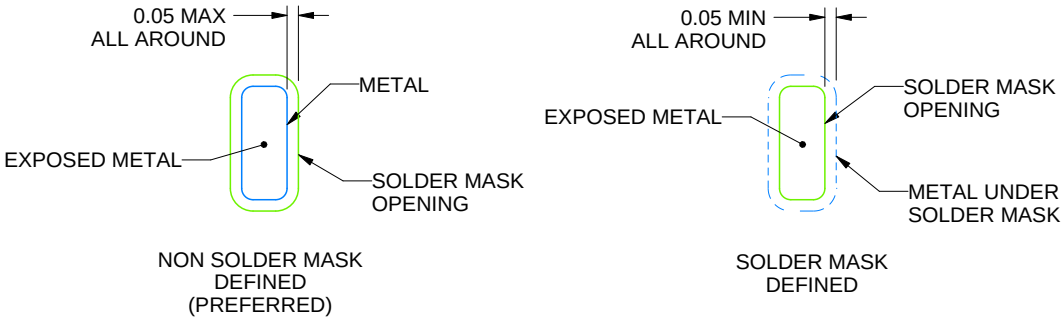


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

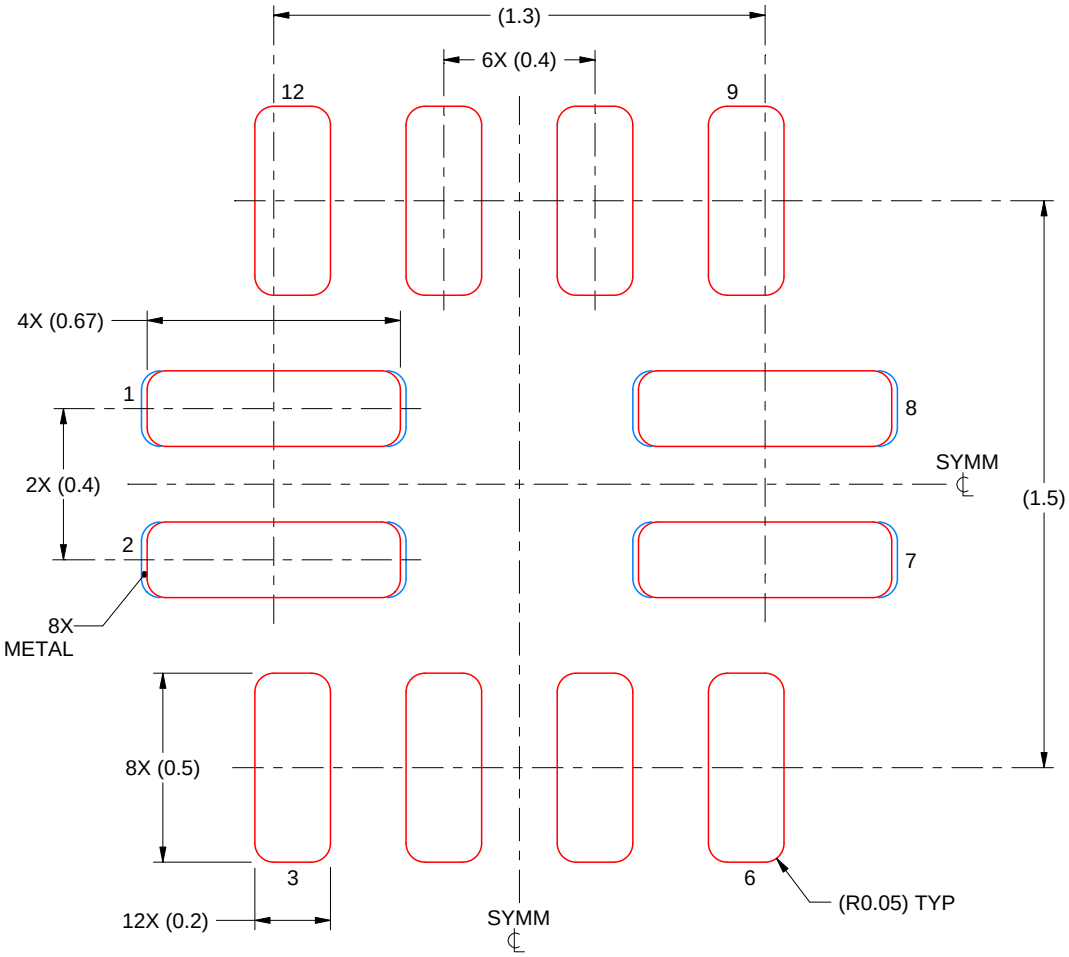
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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