

TPIC6B596 Power Logic 8-Bit Shift Register

1 Features

- Low $r_{DS(on)}$: 5Ω
- Avalanche energy: 30mJ
- Eight power DMOS-transistor outputs of 150-mA continuous current
- 500mA typical current-limiting capability
- Output clamp voltage: 50V
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption

2 Application

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls
- Automotive Relay or Solenoids Drivers

3 Description

The TPIC6B596 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium- current or high-voltage loads.

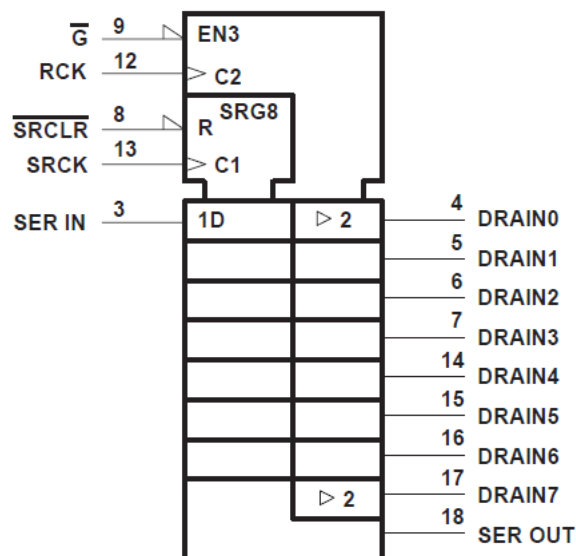
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift- register clear (SRCLR) is high. Write data and read data are valid only when RCK is low. When SRCLR is low, all registers in the device are cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS- transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50V and 150mA continuous sink- current capability. Each output provides a 500mA typical current limit at $T_C = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B596 is characterized for operation over the operating case temperature range of -40°C to 125°C .

Table 3-1. Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
TPIC6A595	PDIP(20)	25.4mm × 6.35mm
	SOIC(20)	12.80mm × 7.50mm



A. † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

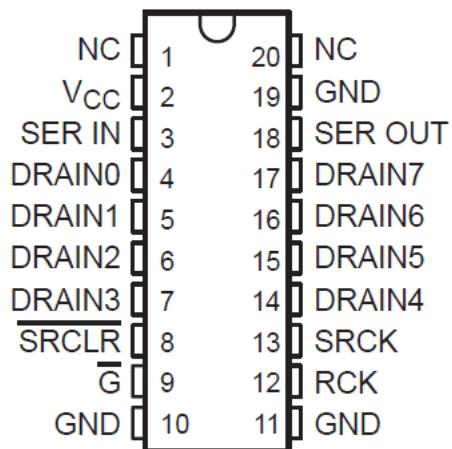
Logic Symbol



Table of Contents

1 Features	1	7.2 Functional Block Diagram.....	11
2 Application	1	7.3 Reference.....	12
3 Description	1	8 Device Functional Modes	13
4 Pin Configuration and Functions	3	8.1 Operating with $V_{CC} < 4.5V$	13
5 Specifications	4	8.2 Operating with $5.5V < V_{CC} \leq 7V$	13
5.1 Absolute Maximum Ratings	4	9 Device and Documentation Support	14
5.2 Dissipation Rating Table.....	4	9.1 Documentation Support.....	14
5.3 Recommended Operating Conditions.....	4	9.2 Receiving Notification of Documentation Updates....	14
5.4 Electrical Characteristics.....	5	9.3 Support Resources.....	14
5.5 Switching Characteristics	6	9.4 Trademarks.....	14
5.6 Thermal Resistance.....	6	9.5 Electrostatic Discharge Caution.....	14
5.7 Typical Characteristics.....	6	9.6 Glossary.....	14
6 Parameter Measurement Information	8	10 Revision History	14
7 Detailed Description	11	11 Mechanical, Packaging, and Orderable Information	14
7.1 Overview.....	11		

4 Pin Configuration and Functions



A. NC - No internal connection

Figure 4-1. DW or N Package (Top View)

Pin Function

PIN		I/O	DESCRIPTION
Name	NO.		
DRAIN0	4	O	Open-drain output
DRAIN1	5		
DRAIN2	6		
DRAIN3	7		
DRAIN4	14		
DRAIN5	15		
DRAIN6	16		
DRAIN7	17		
G	9	I	Output enable, active-low
GND	10, 11, 19	-	Power ground
NC	1, 20	-	No internal connection
RCK	12	I	Register clock
SERIN	3	I	Serial data input
SEROUT	18	O	Serial data output
SRCK	15	I	Shift register clock
SRCLR	3	I	Shift register clear, active-low
VCC	2	I	Power supply

5 Specifications

5.1 Absolute Maximum Ratings

over recommended operating case temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Logic supply voltage ⁽²⁾			7	V
V _I	Logic input voltage range		-0.3	7	V
V _{DS}	Power DMOS drain-to-source voltage ⁽³⁾			50	V
	Continuous source-to-drain diode anode current			500	mA
	Pulsed source-to-drain diode anode current ⁽⁴⁾			1	A
I _D	Pulsed drain current, each output, all outputs on ⁽⁴⁾	T _C = 25°C		500	mA
I _D	Continuous drain current, each output, all outputs on	T _C = 25°C		150	mA
I _{DM}	Peak drain current single output ⁽⁴⁾	T _C = 25°C		500	mA
E _{AS}	Single-pulse avalanche energy (see Figure 6-4)			30	mJ
I _{AS}	Avalanche current ⁽⁵⁾			500	mA
	Continuous total dissipation		See Section 5.2		
T _J	Operating virtual junction temperature range		-40	150	°C
T _C	Operating case temperature range		-40	125	°C
	Storage temperature range		-65	150	°C
	Lead temperature 1,6mm (1/16 inch) from case for 10 seconds			260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Each power DMOS source is internally connected to GND.
- (4) Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
- (5) DRAIN supply voltage = 15V, starting junction temperature (T_{JS}) = 25°C, L = 200mH, I_{AS} = 0.5A (see Figure 6-4).

5.2 Dissipation Rating Table

PACKAGE	T _C ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1389mW	11.1mW/°C	278mW
N	1050mW	10. mW/°C	263mW

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC}	Logic supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	0.85 V _{CC}		V
V _{IL}	Low-level input voltage		0.15 V _{CC}	V
	Pulsed drain output current, T _C = 25°C, V _{CC} = 5V ^{(1) (2)}	-500	500	mA
t _{su}	Setup time, SER IN high before SRCK (see Figure 6-2)	15		ns
t _h	Hold time, SER IN high after SRCK (see Figure 6-2)	15		ns
t _w	Pulse duration (see Figure 6-2)	40		ns
T _C	Operating case temperature	-40	125	°C

- (1) Pulse duration ≤ 100μs and duty cycle ≤ 2%.
- (2) Technique should limit T_J – T_C to 10°C maximum.

5.4 Electrical Characteristics

$V_{CC} = 5V$, $T_C = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{(BR)DSX}	Drain-to-source breakdown voltage	I _D = 1mA			50			V
V _{SD}	Source-to-drain diode forward voltage	I _F = 100mA			0.85		1	V
V _{OH}	High-level output voltage, SER OUT	I _{OH} = −20μA	V _{CC} = 4.5V		4.4	4.49		V
		I _{OH} = −4mA,	V _{CC} = 4.5V		4	4.2		
V _{OL}	Low-level output voltage, SER OUT	I _{OL} = 20μA,	V _{CC} = 4.5V			0.005	0.1	V
		I _{OL} = 4mA,	V _{CC} = 4.5V			0.3	0.5	
I _{IH}	High-level input current	V _{CC} = 5.5V, V _I = V _{CC}					1	μA
I _{IL}	Low-level input current	V _{CC} = 5.5V, V _I = 0					−1	μA
I _{CC}	Logic supply current	V _{CC} = 5.5V		All outputs off	20	100	μA	
				All outputs on	150	300		
I _{CC(FRQ)}	Logic supply current at frequency	f _{SRCK} = 5MHz, All outputs off,		C _L = 30pF, See Figure 6-2 and Figure 5-2	0.4	5	mA	
I _N	Nominal current	V _{DS(on)} = 0.5V, I _N = I _D , T _C = 85°C		See ^{(1) (2) (3)}	90		mA	
I _{DSX}	Off-state drain current	V _{DS} = 40V,	V _{CC} = 5.5V		0.1	5	μA	
		V _{DS} = 40V,	V _{CC} = 5.5V,	T _C = 125°C	0.15	8		
r _{DS(on)}	Static drain-source on-state resistance	I _D = 100mA,	V _{CC} = 4.5V		4.2	5.7	Ω	
		I _D = 100mA V _{CC} = 4.5V	T _C = 125°C, See Figure 5-3 and Figure 5-4 ^{(1) (2)}		6.8	9.5		
		I _D = 350mA,	V _{CC} = 4.5V		5.5	8		

- (1) Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.
- (2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
- (3) Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5V at $T_C = 85^\circ C$.

5.5 Switching Characteristics

 $V_{CC} = 5V$, $T_C = 25^\circ C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output from G	C _L = 30pF,	I _D = 100mA,	150		ns	
t _{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			90		ns	
t _r	Rise time, drain output	See Figure 6-1, Figure 6-2 and Figure 5-5		200		ns	
t _f	Fall time, drain output			200		ns	
t _{pd}	Propagation delay time, SRCK↓ to SEROUT	C _L = 30pF, See Figure 6-2	I _D = 100mA,	15		ns	
f _(SRCK)	Serial clock frequency	C _L = 30pF, See ⁽³⁾	I _D = 100mA,			10	MHz
t _a	Reverse-recovery-current rise time	I _F = 100mA,	di/dt = 20A/μs,	100		ns	
t _{rr}	Reverse-recovery time	See Figure 6-3 ⁽¹⁾ ⁽²⁾		300			

(1) Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.

(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

(3) This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK $\rightarrow$ SEROUT propagation delay and setup time plus some timing margin.

5.6 Thermal Resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		$^\circ C/W$
		N package			
				90	
				95	

5.7 Typical Characteristics

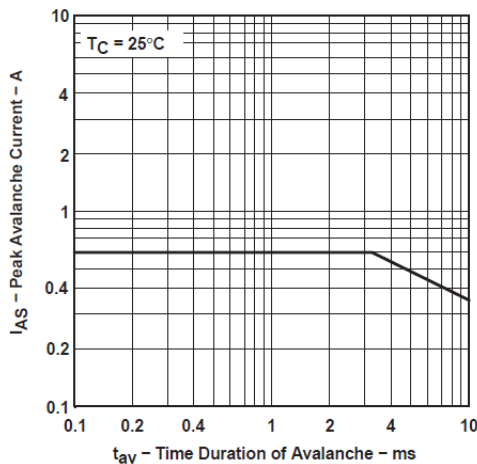


Figure 5-1. Peak Avalanche Current vs Time Duration of Avalanche

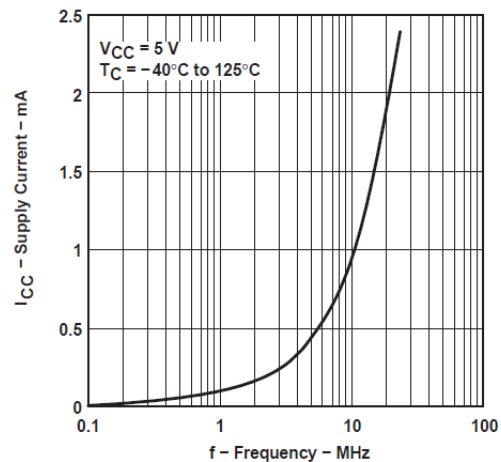


Figure 5-2. Supply Current vs Frequency

5.7 Typical Characteristics (continued)

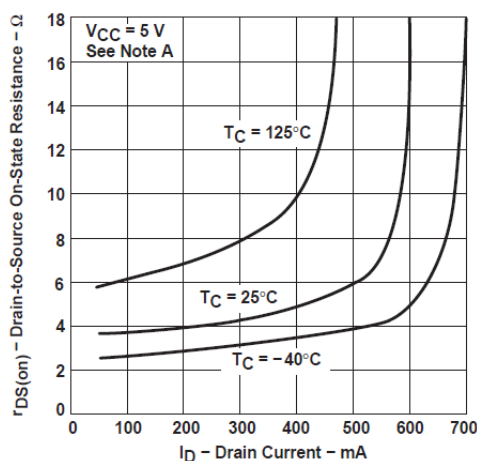


Figure 5-3. Drain-to-Source On-State Resistance vs Drain Current

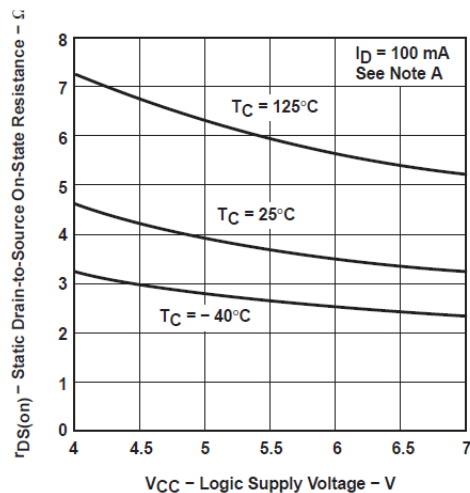
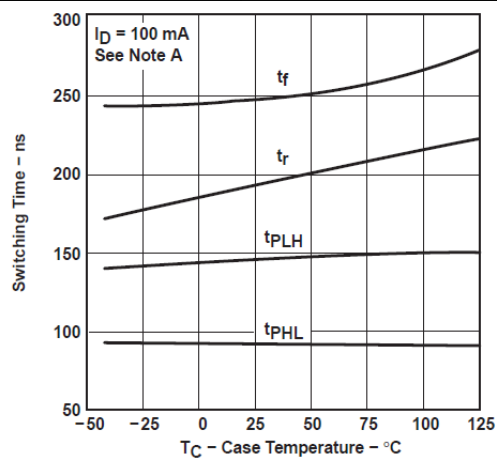


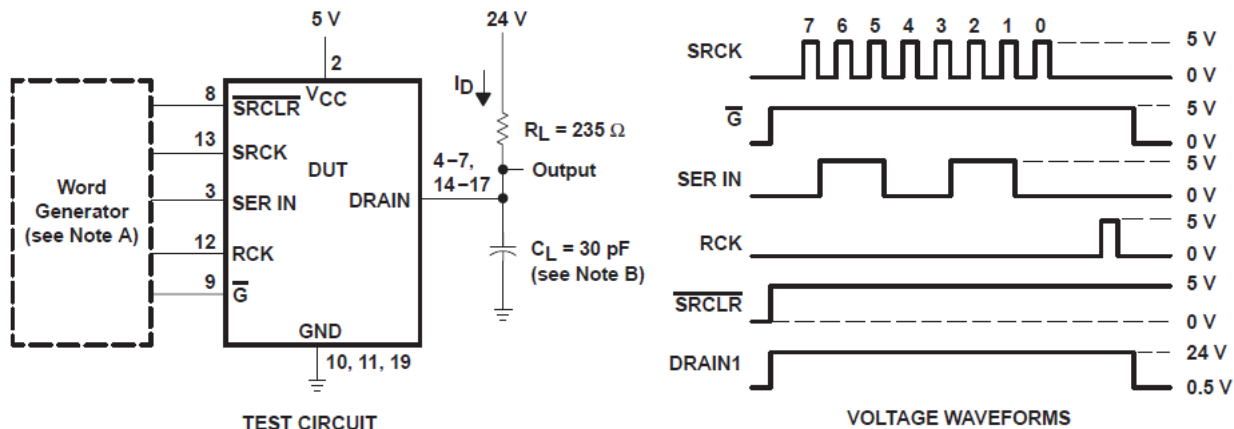
Figure 5-4. Static Drain-to-Source On-State Resistance vs Logic Supply Voltage



Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.

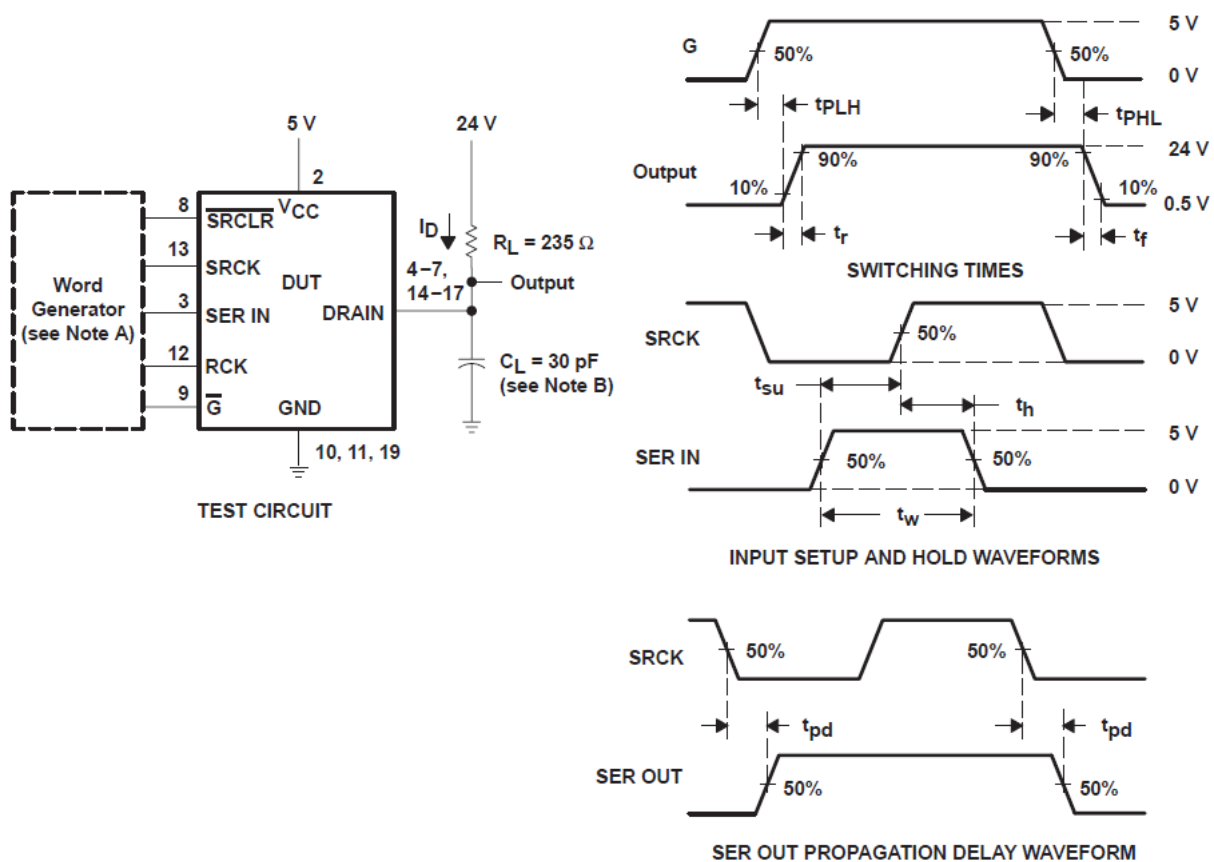
Figure 5-5. Switching Time vs Case Temperature

6 Parameter Measurement Information



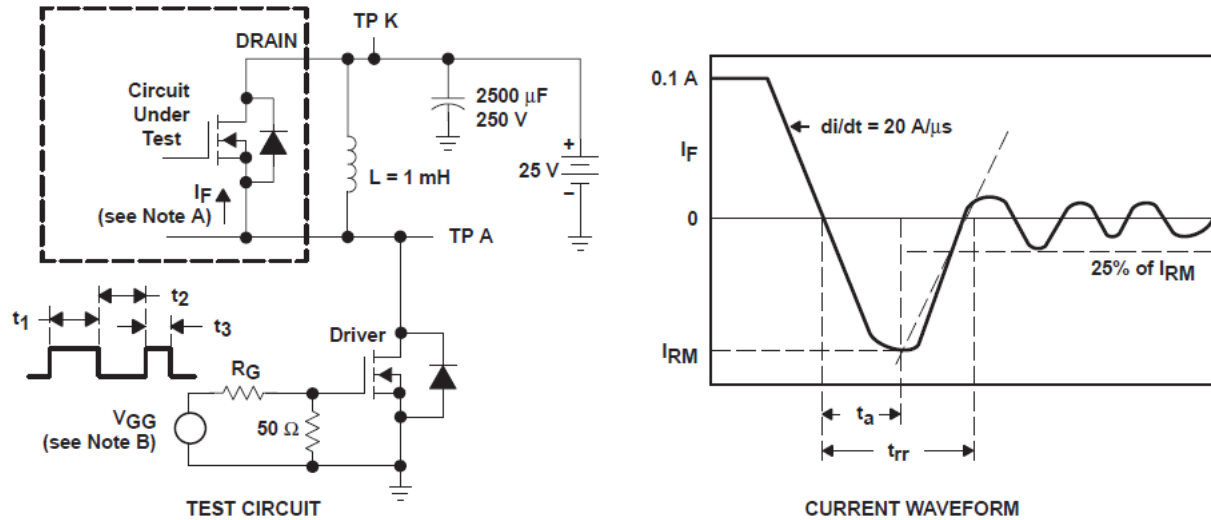
- A. The word generator has the following characteristics: $t_r \leq 10\text{ns}$, $t_f \leq 10\text{ns}$, $t_w = 300\text{ns}$, pulsed repetition rate (PRR) = 5kHz, $Z_O = 50\Omega$.
- B. C_L includes probe and jig capacitance.
- C. Write data and read data are valid only when RCK is low

Figure 6-1. Resistive-Load Test Circuit and Voltage Waveforms



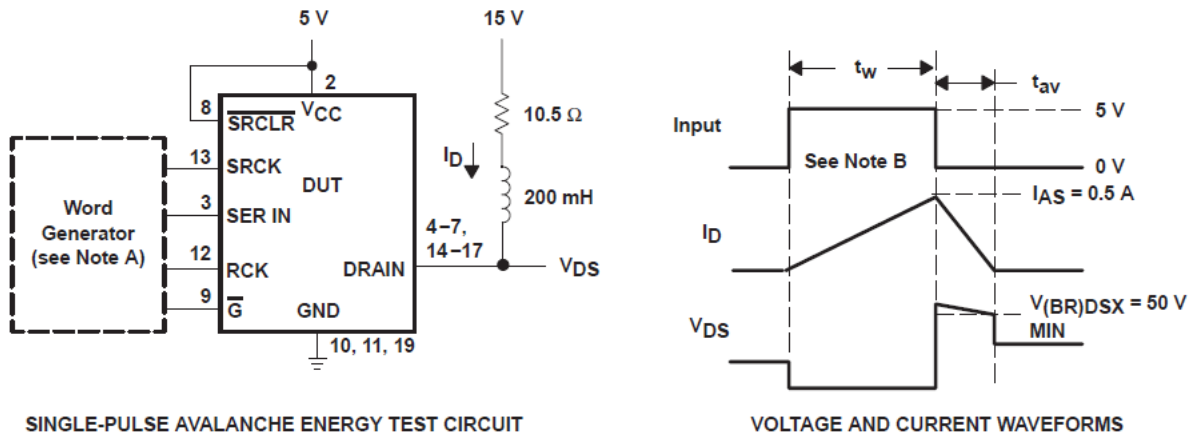
- A. The word generator has the following characteristics: $t_r \leq 10\text{ns}$, $t_f \leq 10\text{ns}$, $t_w = 300\text{ns}$, pulsed repetition rate (PRR) = 5kHz, $Z_O = 50\Omega$.
- B. C_L includes probe and jig capacitance

Figure 6-2. Test Circuit, Switching Times, and Voltage Waveforms



- A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
- B. The V_{GG} amplitude and R_G are adjusted for $di/dt = 20 \text{ A}/\mu\text{s}$. A V_{GG} double-pulse train is used to set $I_F = 0.1 \text{ A}$, where $t_1 = 10 \mu\text{s}$, $t_2 = 7 \mu\text{s}$, and $t_3 = 3 \mu\text{s}$.

Figure 6-3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



- A. The word generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_O = 50 \Omega$.
- B. Input pulse duration, t_w , is increased until peak current $I_{AS} = 0.5 \text{ A}$.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30 \text{ mJ}$.

Figure 6-4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

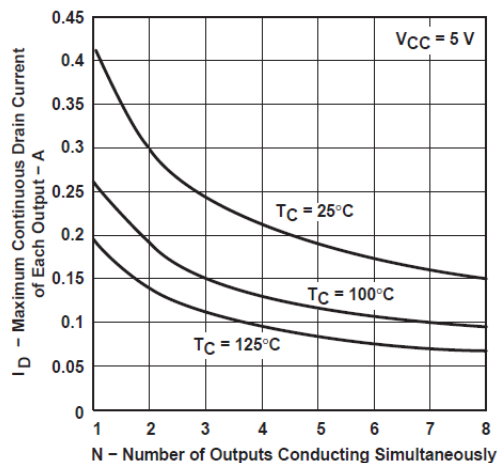


Figure 6-5. Maximum Continuous Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

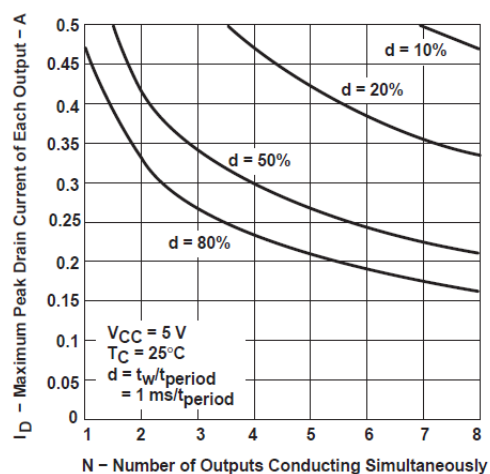


Figure 6-6. Maximum Peak Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

The TPIC6B596 device is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection, so it can also drive relays, solenoids, and other medium-current or high-voltage loads.

[Submit Document Feedback](#)

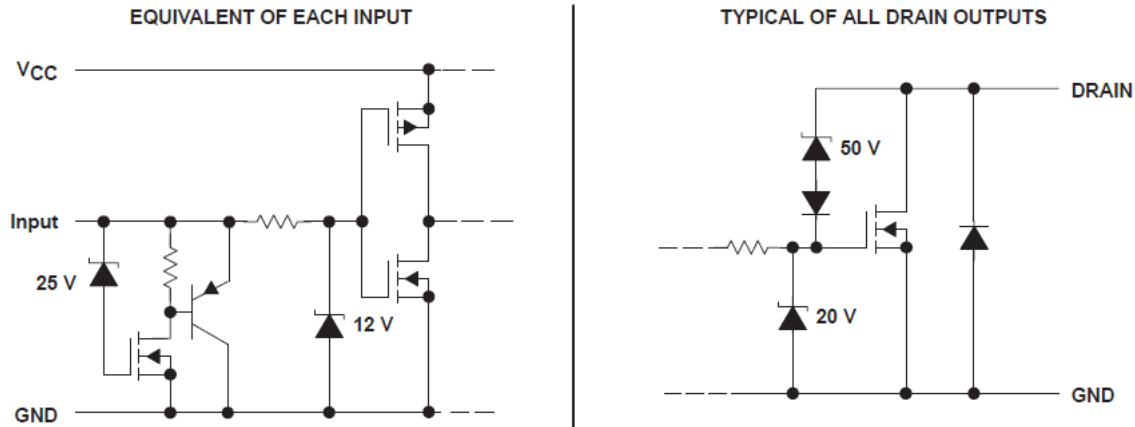


Figure 7-1. Functional Block Diagram (continued)

7.3 Reference

7.3.1 Reference

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. Write data and read data are valid only when RCK is low. The storage register transfers data to the output buffer when shift register clear (SRCLR) is high.

7.3.2 Clear Register

A logical low on ($\overline{\text{SRCLR}}$) clears all registers in the device. TI suggests clearing the device during power up or initialization.

7.3.3 Output Control

Holding the output enable ($\overline{\text{G}}$) high holds all data in the output buffers low, and all drain outputs are off. Holding ($\overline{\text{G}}$) low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are OFF. When data is high, the DMOS transistor outputs have sink-current capability. This pin can also be used for global PWM dimming.

7.3.4 Cascaded Application

The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. Connect the device (SER OUT) pin to the next device (SER IN) for daisy Chain.

7.3.5 Current Limit Function

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink current capability. Each output provides a 500-mA typical current limit at $T_C = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection.

8 Device Functional Modes

8.1 Operating with $V_{CC} < 4.5V$

This device works normally during $4.5V \leq V_{CC} \leq 5.5V$, when operation voltage is lower than 4.5V, correct behavior of the device, including communication interface and current capability, is not assured.

8.2 Operating with $5.5V < V_{CC} \leq 7V$

The device works normally in this voltage range, but reliability issues can occur if the device works for a long time in this voltage range.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2005) to Revision B (March 2024) Page

- Updated Applications section..... 1

Changes from Revision * (March 2000) to Revision A (May 2005) Page

- Changed $\overline{\text{SRCLR}}$ timing diagram in [Figure 6-1](#) 8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPIC6B596DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	
TPIC6B596DWG4	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-	
TPIC6B596DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6B596
TPIC6B596DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6B596
TPIC6B596DWRG4	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-	TPIC6B596
TPIC6B596N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6B596N
TPIC6B596N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6B596N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

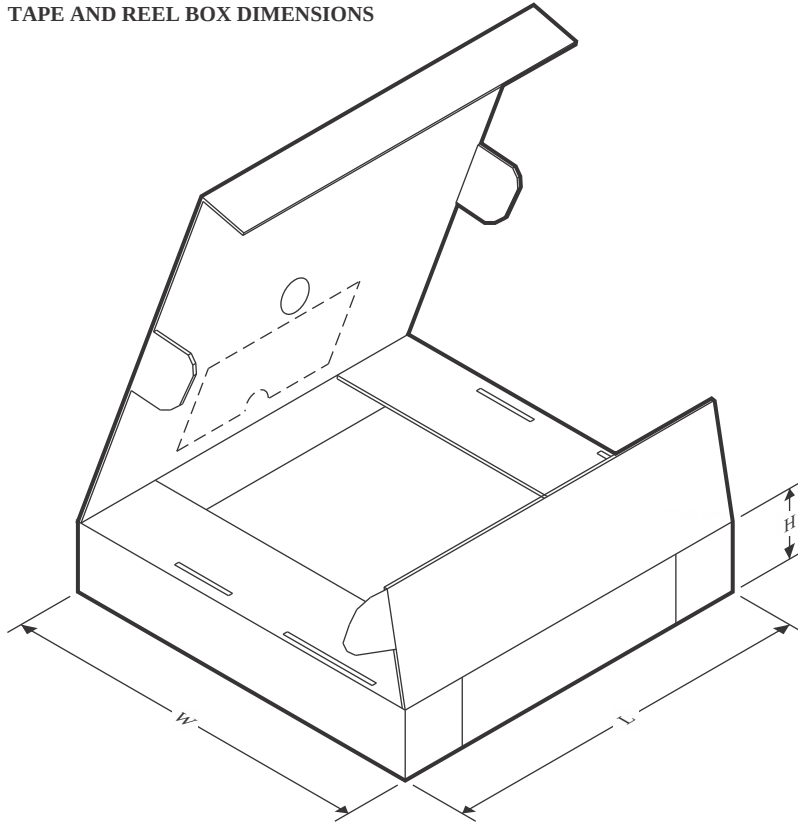
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6B596DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6B596DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

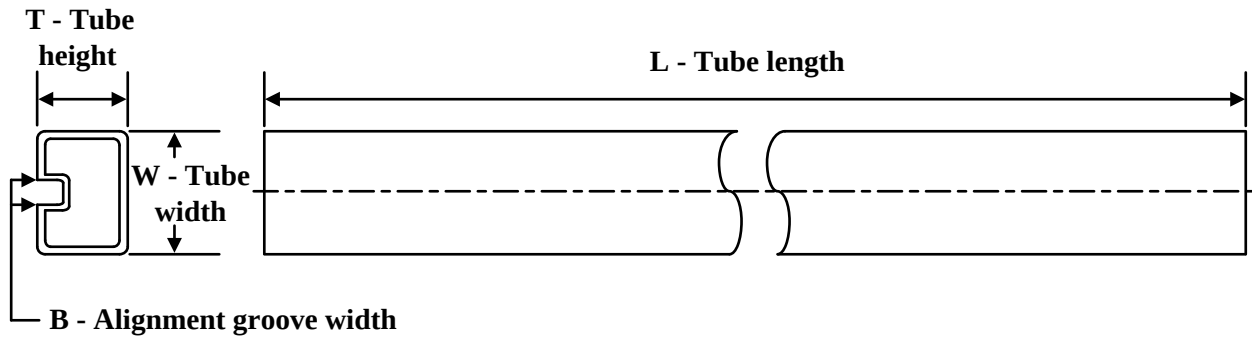
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6B596DWR	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6B596DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



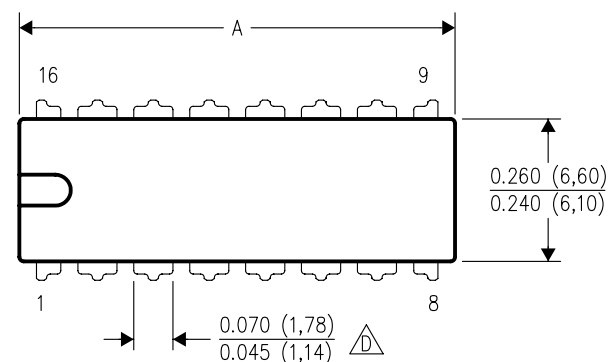
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPIC6B596N	N	PDIP	20	20	506	13.97	11230	4.32
TPIC6B596N.A	N	PDIP	20	20	506	13.97	11230	4.32

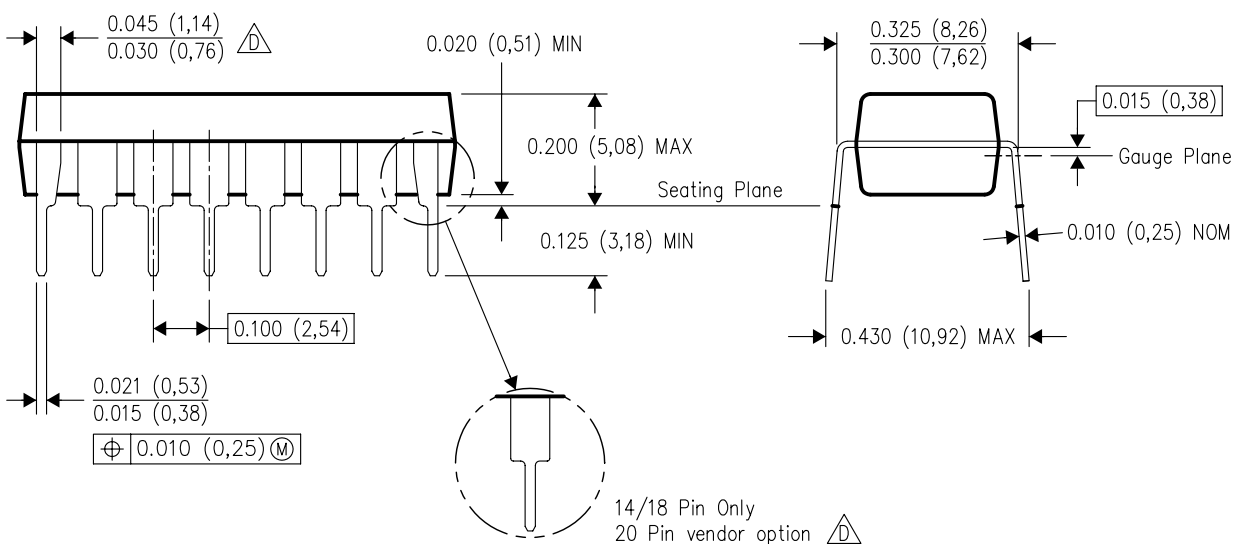
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



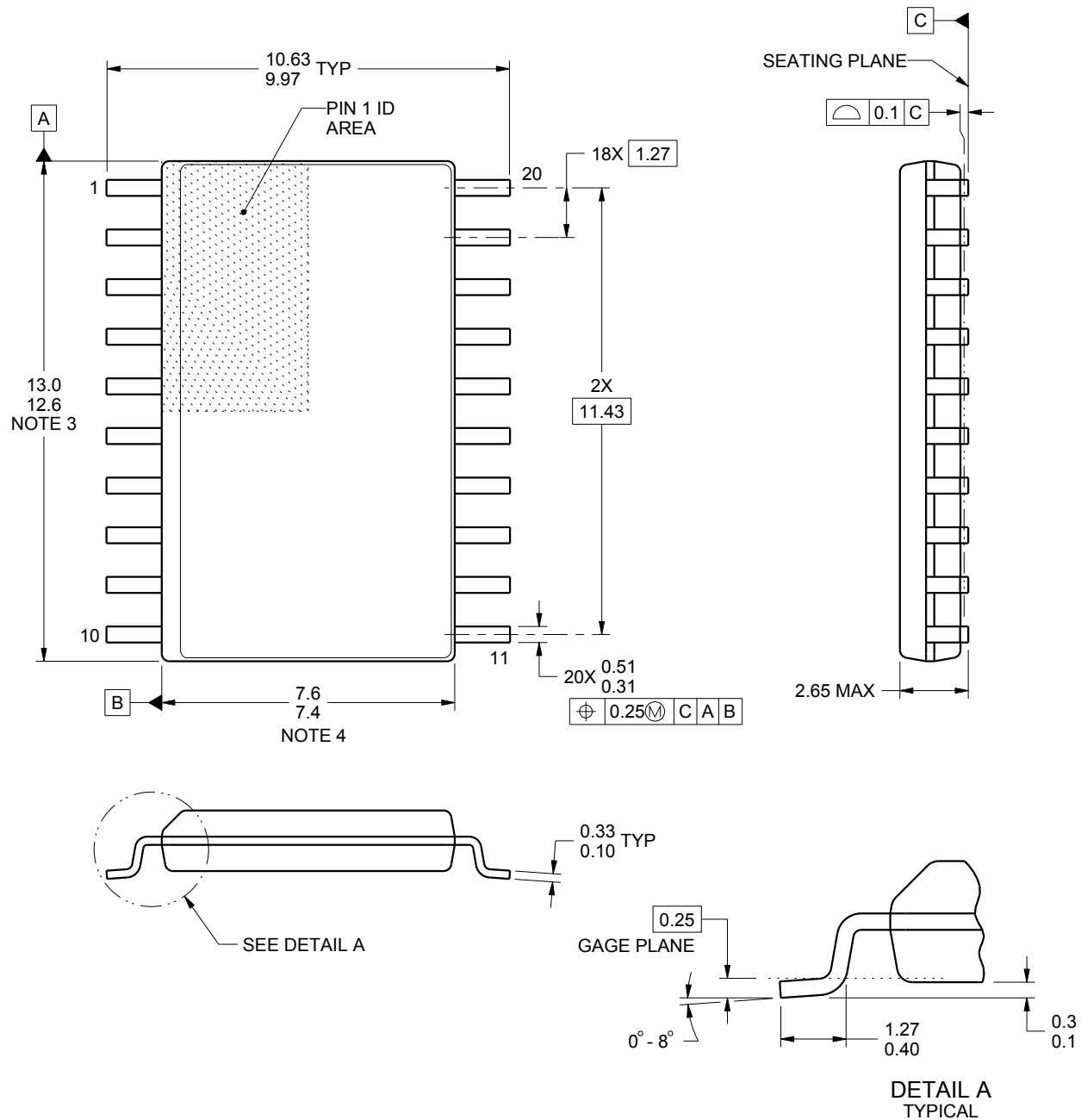
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

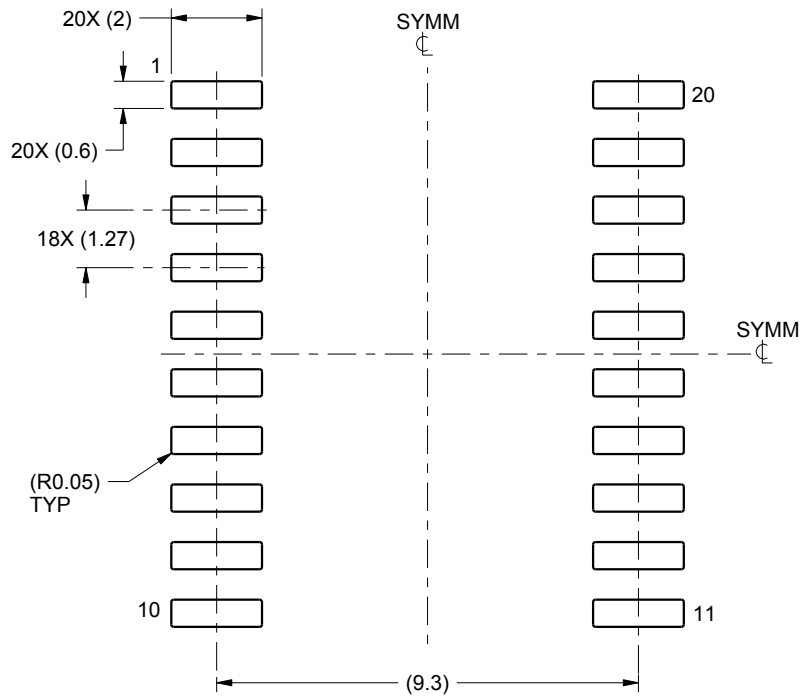
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

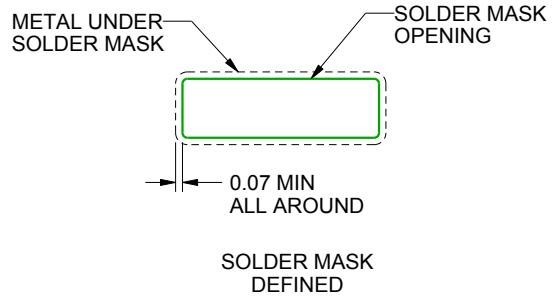
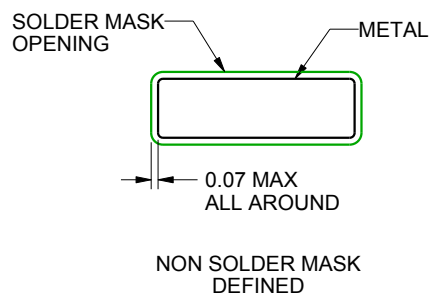
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

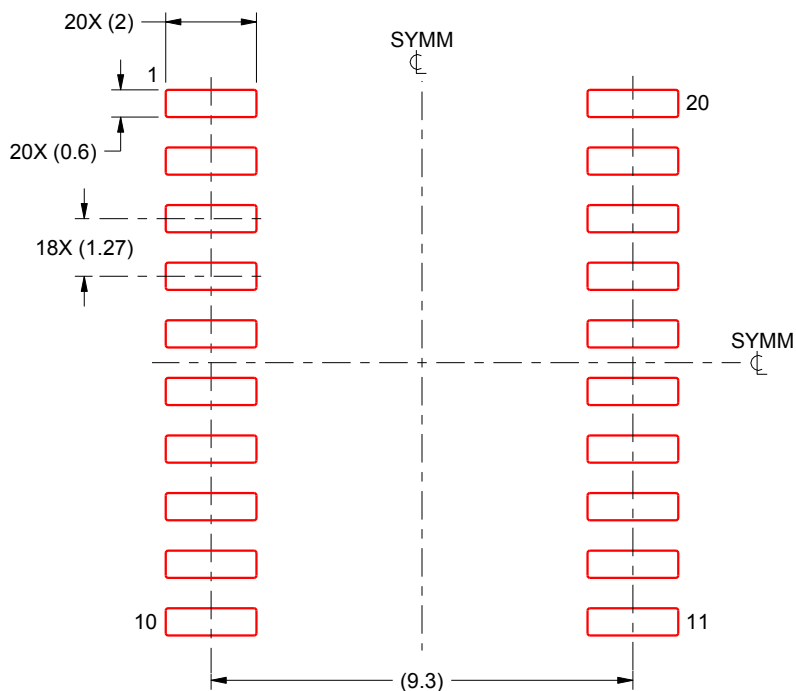
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025