

TMUXS130xA 5V, Bidirectional 16:1, 1-Channel and 8:1, 2-Channel Current Injection Controlled Multiplexers Optimized for High-Impedance Loads

1 Features

- [Injection current control](#)
- Back-powering protection
 - No ESD diode path to V_{DD}
- Wide supply range: 1.62V to 5.5V
- Low ON-capacitance
- [Bidirectional signal path](#)
- [Rail-to-rail operation](#)
- [1.8V logic compatible](#)
- [Fail-safe logic](#)
- Break-before-make switching
- Short-to-battery protection for ON and OFF channels

2 Applications

- [Data center switch](#)
- [Remote radio unit \(RRU\)](#)
- [Rack server](#)
- [Electricity meter](#)
- [Appliances](#)
- [Air conditioner units](#)
- [Multifunction printers](#)
- [String inverter](#)
- [IP network camera](#)
- [Currency counters](#)
- [Off-highway vehicles control systems](#)

3 Description

The TMUXS1306A and TMUXS1307A are general purpose complementary metal-oxide semiconductor (CMOS) multiplexers (MUX). The TMUXS1306A is an 16:1, 1-channel (single-ended) mux, while the TMUXS1307A is a 8:1, 2-channel (differential) mux. The devices support bidirectional analog and digital

signals on the source (S_x) and drain (D_x) pins ranging from GND to V_{DD} .

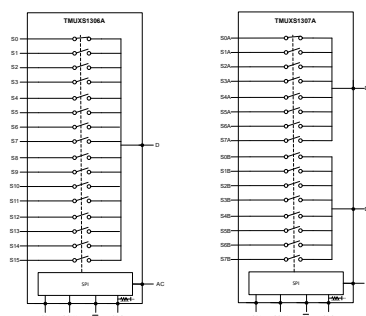
The TMUXS130xA devices have an internal injection current control feature, which eliminates the need for external diode and resistor networks typically used to protect the switch and keep the input signals within the supply voltage. The internal injection current control circuitry allows signals on disabled or enabled signal paths to exceed the supply voltage. Disabled channels with voltages above V_{DD} are prevented from affecting the signal of the enabled signal path. Additionally, the TMUXS130xA devices do not have an internal diode path to the supply pin, which eliminates the risk of damaging components connected to the supply pin or providing unintended power to the supply rail.

The switches of TMUXS130xA are controlled with a serial peripheral interface (SPI). The SPI has many error detection features, such as CRC, invalid read/write, and clock count error detection. The SPI also supports auto cycle (AC) mode (control MUX with a single GPIO), daisy chain mode, and burst mode.

Device Information

PART NUMBER	CONFIGURATION ⁽¹⁾	PACKAGE ⁽²⁾	PACKAGE SIZE ⁽³⁾
TMUXS1306A	Channel 16:1	PW (TSSOP, 24) ⁽⁴⁾	7.8mm × 6.4mm
		DGS (VSSOP, 24) ⁽⁴⁾	6.1mm × 4.9mm
		RGE (VQFN, 24)	4mm × 4mm
TMUXS1307A	2 Channel 8:1	RGE (VQFN, 24)	4mm × 4mm

- (1) See the [Device Comparison Table](#).
- (2) For more information, see [Section 14](#).
- (3) The package size (length × width) is a nominal value and includes pins, where applicable.
- (4) Preview information (not Advance Information).



TMUXS1306A and TMUXS1307A Block Diagram



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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUXS1306A	16:1, 1-channel, single-ended multiplexer
TMUXS1307A	8:1, 2-channel, differential multiplexer

5 Pin Configuration and Functions

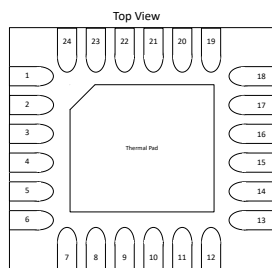


Figure 5-1. TMUXS1306A: RGE Package, 24-Pin VQFN (Top View)

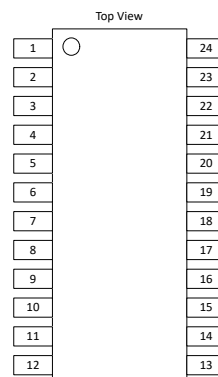


Figure 5-2. TMUXS1306A: PW and DGS 24-Pin TSSOP and VSSOP (Top View)

Table 5-1. Pin Functions: TMUXS1306A

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	RGE NO.	PW, DGS NO.		
S10	1	21	I/O	Source pin 10. Can be an input or output.
S9	2	22	I/O	Source pin 9. Can be an input or output.
S8	3	23	I/O	Source pin 8. Can be an input or output.
S7	4	2	I/O	Source pin 7. Can be an input or output.
S6	5	3	I/O	Source pin 6. Can be an input or output.
S5	6	4	I/O	Source pin 5. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
S3	8	6	I/O	Source pin 3. Can be an input or output.
S2	9	7	I/O	Source pin 2. Can be an input or output.
S1	10	8	I/O	Source pin 1. Can be an input or output.
S0	11	9	I/O	Source pin 0. Can be an input or output.
GND	12	12	P	Ground (0V) reference.
D	13	1	I/O	Drain pin (Common) of mux A. Can be an input or output.
$\overline{\text{CS}}$	14	10	I	SPI chip select pin (active low)
SCLK	15	11	I	SPI clock input
SDI	16	13	I	SPI serial data input. Data is captured on the positive edge of SCLK
SDO	17	14	O	SPI serial data output
AC	18	15	I	Toggle channel pin. Default toggles on active edge.
VDD	19	24	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V _{DD} and GND.
S15	20	16	I/O	Source pin 15. Can be an input or output.
S14	21	17	I/O	Source pin 14. Can be an input or output.
S13	22	18	I/O	Source pin 13. Can be an input or output.
S12	23	19	I/O	Source pin 12. Can be an input or output.
S11	24	20	I/O	Source pin 11. Can be an input or output.
Thermal pad		N/A FOR PW/DGS	P	Exposed thermal pad with conductive die attached. Must be tied to GND. Ground (0V) reference.

(1) I = input, O = output, I/O = input and output, P = power.

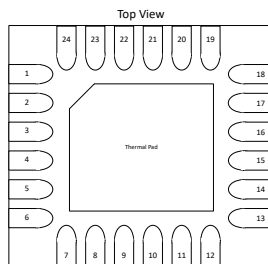


Figure 5-3. TMUXS1307A: RGE Package, 24-Pin VQFN (Top View)

Table 5-2. Pin Functions: TMUXS1307A

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
S2B	1	I/O	Source pin 2 of mux B. Can be an input or output.
S1B	2	I/O	Source pin 1 of mux B. Can be an input or output.
S0B	3	I/O	Source pin 0 of mux B. Can be an input or output.
S7A	4	I/O	Source pin 7 of mux A. Can be an input or output.
S6A	5	I/O	Source pin 6 of mux A. Can be an input or output.
S5A	6	I	Source pin 5 of mux A. Can be an input or output.
S4A	7	I/O	Source pin 4 of mux A. Can be an input or output.
S3A	8	I/O	Source pin 3 of mux A. Can be an input or output.
S2A	9	I/O	Source pin 2 of mux A. Can be an input or output.
S1A	10	I/O	Source pin 1 of mux A. Can be an input or output.
S0A	11	I/O	Source pin 0 of mux A. Can be an input or output.
DA	12	I/O	Drain pin (Common) of mux A. Can be an input or output.
AC	13	I	Toggle channel pin. Default toggles on active edge.
CS	14	I	SPI chip select pin (active low)
SCLK	15	I	SPI clock input
SDI	16	I	SPI serial data input. Data is captured on the positive edge of SCLK
SDO	17	O	SPI serial data output
DB	18	I/O	Drain pin (Common) of mux B. Can be an input or output.
VDD	19	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V _{DD} and GND.
S7B	20	I/O	Source pin 7 of mux B. Can be an input or output.
S6B	21	I/O	Source pin 6 of mux B. Can be an input or output.
S5B	22	I/O	Source pin 5 of mux B. Can be an input or output.
S4B	23	I/O	Source pin 4 of mux B. Can be an input or output.
S3B	24	I/O	Source pin 3 of mux B. Can be an input or output.
Thermal pad		P	Exposed thermal pad with conductive die attached. Must be tied to GND. Ground (0V) reference.

(1) I = input, O = output, I/O = input and output, P = power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

		MIN	MAX	UNIT
V _{DD}	Supply voltage	–0.5	6	V
V _{LOGIC}	Logic control input pin voltage (SPI pins)	–0.5	6	
V _S or V _D	Source or drain voltage (Sx, D)	–0.5	V _{DD} +1.0	
I _{LOGIC}	Logic control input pin current (SPI pins)	–30	30	mA
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +85°C	–50	50	
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +125°C	–25	25	
I _{GND}	Continuous current through GND	–100	100	
P _{tot}	Total power dissipation ⁽⁴⁾		TBD	mW
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	–65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) For TSSOP package: P_{tot} derates linearly above T_A = 80°C by 7.2mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	1.62		5.5	V
V _S or V _D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V _{DD}	V
V _{LOGIC}	Logic control input pin voltage (SPI pins)	0		5.5	V
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +85°C	–50		50	mA
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +125°C	–25		25	mA
I _{OK}	Current per input into source or drain pins when signal voltage exceeds recommended operating voltage ⁽¹⁾	–50		50	mA
I _{INJ}	Injected current into single off switch input	–50		50	mA
I _{INJ_ALL}	Total injected current into all off switch inputs combined	–100		100	mA
T _A	Ambient temperature	–40		125	°C

- (1) If source or drain voltage exceeds V_{DD}, or goes below GND, the pin is shunted to GND through an internal FET, the current must be limited within the specified value. If V_{signal} > V_{DD} or if V_{signal} < GND.

6.4 Thermal Information: TMUXS1306A

THERMAL METRIC ⁽¹⁾		TMUXS1306			UNIT
		PW (24-TSSOP)	DGS (24-VSSOP)	RGE (24-VQFN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	56.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	49.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	33.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	5.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	33.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	18.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.5 Thermal Information: TMUXS1307A

THERMAL METRIC ⁽¹⁾		TMUXS1307	UNIT
		RGE (24-VQFN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.6 Electrical Characteristics

At specified $V_{DD} \pm 10\%$ Typical values measured at nominal V_{DD}

PARAMETER		TEST CONDITIONS	V _{DD}	OPERATING FREE-AIR TEMPERATURE (T _A)									UNIT
				25°C			–40°C to 85°C			–40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH													
R _{ON}	On-state switch resistance	V _S = 0V to V _{DD} I _{SD} = 0.5mA	1.8V	650	1500	1700	1700					Ω	
			2.5V	230	600	670	670						
			3.3V	120	330	350	370						
			5V	75	195	220	270						
Δ _{RON}	On-state switch resistance matching between inputs	V _S = V _{DD} / 2 I _{SD} = 0.5mA	1.8V	10	38	45	45					Ω	
			2.5V	3	20	22	22						
			3.3V	2	8	11	15						
			5V	1	7	10	14						
I _{S(OFF)}	Source off-state leakage current	Switch Off V _D = 0.8 × V _{DD} / 0.2 × V _{DD} V _S = 0.2 × V _{DD} / 0.8 × V _{DD}	1.8V	±1		–25	25	–800	800			nA	
			2.5V	±1		–25	25	–800	800				
			3.3V	±1		–25	25	–800	800				
			5V	±1		–25	25	–800	800				
I _{D(OFF)}	Drain off-state leakage current (common drain pin)	Switch Off V _D = 0.8 × V _{DD} / 0.2 × V _{DD} V _S = 0.2 × V _{DD} / 0.8 × V _{DD}	1.8V	±1		–45	45	–800	800			nA	
			2.5V	±1		–45	45	–800	800				
			3.3V	±1		–45	45	–800	800				
			5V	±1		–45	45	–800	800				
I _{D(ON)} I _{S(ON)}	Channel on-state leakage current	Switch On V _D = V _S = 0.8 × V _{DD} or V _D = V _S = 0.2 × V _{DD}	1.8V	±1		–45	45	–800	800			nA	
			2.5V	±1		–45	45	–800	800				
			3.3V	±1		–45	45	–800	800				
			5V	±1		–45	45	–800	800				
C _{SOFF}	Source off capacitance	V _S = V _{DD} / 2 f = 1MHz	1.8V	2.2	4	4	4	4				pF	
			2.5V	2.2	4	4	4	4					
			3.3V	2.2	4	4	4	4					
			5V	2.2	4	4	4	4					
C _{DOFF}	Drain off capacitance	V _S = V _{DD} / 2 f = 1MHz	1.8V	12.5	15	15	15	15				pF	
			2.5V	12.5	15	15	15	15					
			3.3V	12.5	15	15	15	15					
			5V	12	15	15	15	15					
C _{SON} C _{DON}	On capacitance	V _S = V _{DD} / 2 f = 1MHz	1.8V	15	18	18	18	18				pF	
			2.5V	15	18	18	18	18					
			3.3V	15	18	18	18	18					
			5V	14	18	18	18	18					
POWER SUPPLY													
I _{DD}	V _{DD} supply current	Logic inputs = 0V or V _{DD}	1.8V	5	6	8						μA	
			2.5V	5	6	8							
			3.3V	5	6	8							
			5V	7.5	8	11							

6.7 Logic and Dynamic Characteristics

At specified $V_{DD} \pm 10\%$

Typical values measured at nominal V_{DD} and $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	V _{DD}	OPERATING FREE-AIR TEMPERATURE (T _A)			UNIT
				–40°C to 125°C			
				MIN	TYP	MAX	
LOGIC INPUTS (CS, SCLK, SDI, AC) AND OUTPUT (SDO)							
V _{IH}	Input logic high		1.8V	1.12	5.5	V	
			2.5V	1.13	5.5		
			3.3V	1.14	5.5		
			5V	1.25	5.5		
V _{IL}	Input logic low		1.8V	0	0.6	V	
			2.5V	0	0.75		
			3.3V	0	0.75		
			5V	0	0.75		
V _{OH}	Output logic high voltage drop	SDO pin current = -1mA	All		0.6	V	
V _{OH}	Output logic high voltage drop	SDO pin current = -3mA	All		0.6	V	
V _{OL}	Output logic low voltage	SDO pin current = 1mA	All		0.5	V	
V _{OL}	Output logic low voltage	SDO pin current = 3mA	All		0.5	V	
C _{IN}	Logic input capacitance	V _{LOGIC} = 0V, 1.8V, V _{DD} f = 1MHz	All	1	2	pF	
DYNAMIC CHARACTERISTICS							
Q _{INJ}	Charge Injection	V _S = V _{DD} / 2 R _S = 0Ω, C _L = 100pF	1.8V	–0.5	pC		
			2.5V	–0.5			
			3.3V	–0.8			
			5V	–1.5			
O _{ISO}	Off Isolation	V _{BIAS} = V _{DD} / 2 V _S = 200mVpp R _L = 50Ω, C _L = 5pF f = 100kHz	1.8V	–110	dB		
			2.5V	–110			
			3.3V	–110			
			5V	–110			
O _{ISO}	Off Isolation	V _{BIAS} = V _{DD} / 2 V _S = 200mVpp R _L = 50Ω, C _L = 5pF f = 1MHz	1.8V	–90	dB		
			2.5V	–90			
			3.3V	–90			
			5V	–90			
X _{TALK}	Crosstalk	V _{BIAS} = V _{DD} / 2 V _S = 200mVpp R _L = 50Ω, C _L = 5pF f = 100kHz	1.8V	–110	dB		
			2.5V	–110			
			3.3V	–110			
			5V	–110			
X _{TALK}	Crosstalk	V _{BIAS} = V _{DD} / 2 V _S = 200mVpp R _L = 50Ω, C _L = 5pF f = 1MHz	1.8V	–90	dB		
			2.5V	–90			
			3.3V	–90			
			5V	–90			
BW	Bandwidth	V _{BIAS} = V _{DD} / 2 V _S = 200mVpp R _L = 50Ω, C _L = 5pF	1.8V	350	MHz		
			2.5V	450			
			3.3V	500			
			5V	500			

6.8 Timing Characteristics

At specified $V_{DD} \pm 10\%$

Typical values measured at nominal V_{DD} .

PARAMETER		TEST CONDITIONS	V _{DD}	OPERATING FREE-AIR TEMPERATURE (T _A)									UNIT
				25°C			−40°C to 85°C			−40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS													
t _{PD}	Propagation delay	C _L = 50pF Sx to D, D to Sx	1.8V	15	30	30			30			ns	
			2.5V	8	15	20			20				
			3.3V	5	11	15			15				
			5V	4	9	10			10				
		CL = 15pF	5V	1.5	4	5			5				
t _{BBM}	Break before make time	R _L = 2kΩ, C _L = 10pF Sx to D, D to Sx	1.8V	1	16	1			1			ns	
			2.5V	1	22	1			1				
			3.3V	1	24	1			1				
			5V	1	33	1			1				
t _{BBM}	Break before make time	R _L = 10kΩ, C _L = 15pF Sx to D, D to Sx	1.8V	1	16	1			1			ns	
			2.5V	1	22	1			1				
			3.3V	1	24	1			1				
			5V	1	33	1			1				

6.9 Injection Current Coupling

At specified $V_{DD} \pm 10\%$

Typical values measured at nominal V_{DD} and $T_A = 25^\circ\text{C}$.

PARAMETER		V _{DD}	TEST CONDITIONS		-40°C to 125°C			UNIT
					MIN	TYP	MAX	
INJECTION CURRENT COUPLING								
ΔV _{OUT}	Maximum shift of output voltage of enabled analog input	1.8V	R _S ≤ 3.9kΩ	I _{INJ} ≤ 1mA	0.01		1	mV
		3.3V			0.05		1	
		5V			0.1		1	
		1.8V	R _S ≤ 3.9kΩ	I _{INJ} ≤ 10mA	0.01		2	
		3.3V			0.3		3	
		5V			0.06		4	
		1.8V	R _S ≤ 20kΩ	I _{INJ} ≤ 1mA	0.05		2	
		3.3V			0.05		2	
		5V			0.1		2	
		1.8V	R _S ≤ 20kΩ	I _{INJ} ≤ 10mA	0.05		15	
		3.3V			0.05		15	
		5V			0.02		15	

6.10 SPI Timing Characteristics (5.5V)

$V_L = 5\text{V} - 5.5\text{V}$, $\text{GND} = 0\text{V}$ (unless otherwise noted)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
AC_to_Dx	AC active edge to Dx	$V_{DD} = 5.5\text{V}$	-40°C to +125°C		20		ns
f_{CLK_SPI}	SCLK Frequency		-40°C to +125°C			50	MHz
t_R, t_F_SPI	SPI Clock Rise and Fall Times		-40°C to +125°C			50	ns
t_{CLK_SPI}	SCLK Period		-40°C to +125°C	20			ns
$t_{CLK_H_SPI}$	SCLK High Time		-40°C to +125°C	8			ns
$t_{CLK_L_SPI}$	SCLK Low Time		-40°C to +125°C	8			ns
t_{CSS}	Set Up Time $\overline{CS}$ to SCLK		-40°C to +125°C	10			ns
t_{SU_SPI}	Set Up Time SDI to SCLK		-40°C to +125°C	6			ns
t_{H_SPI}	Hold Time SDI to SCLK		-40°C to +125°C	8			ns
t_{CSH}	Hold Time SCLK to $\overline{CS}$		-40°C to +125°C	10			ns
t_{CSLSDO}	$\overline{CS}$ falling edge to SDO	20pF	-40°C to +125°C			25	ns
t_{SDO}	SCLK falling edge to SDO	20pF	-40°C to +125°C			25	ns
t_{CSHSDO}	$\overline{CS}$ rising edge to SDO returns to high	20pF	-40°C to +125°C			25	ns
t_{CSD}	$\overline{CS}$ high time between SPI commands		-40°C to +125°C	20			ns
$t_{CSLSCLK}$	$\overline{CS}$ falling edge to SCLK becomes stable		-40°C to +125°C	8			ns
$t_{CSHSCLK}$	$\overline{CS}$ rising edge to SCLK becomes stable		-40°C to +125°C	8			ns

6.11 SPI Timing Characteristics (3.3V)

 $V_L = 3.3V$, GND = 0V (unless otherwise noted)

 $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
AC_to_D x	AC active edge to Dx	$V_{DD} = 3.3V$		27		ns
f_{CLK_SPI}	SCLK Frequency	$-40^\circ C$ to $+125^\circ C$			50	MHz
t_R , t_F_SPI	SPI Clock Rise and Fall Times	$-40^\circ C$ to $+125^\circ C$			50	ns
t_{CLK_SPI}	SCLK Period	$-40^\circ C$ to $+125^\circ C$	20			ns
$t_{CLK_H_SPI}$	SCLK High Time	$-40^\circ C$ to $+125^\circ C$	8			ns
$t_{CLK_L_SPI}$	SCLK Low Time	$-40^\circ C$ to $+125^\circ C$	8			ns
t_{CSS}	Set Up Time $\overline{CS}$ to SCLK	$-40^\circ C$ to $+125^\circ C$	10			ns
t_{SU_SPI}	Set Up Time SDI to SCLK	$-40^\circ C$ to $+125^\circ C$	6			ns
t_{H_SPI}	Hold Time SDI to SCLK	$-40^\circ C$ to $+125^\circ C$	8			ns
t_{CSH}	Hold Time SCLK to $\overline{CS}$	$-40^\circ C$ to $+125^\circ C$	10			ns
t_{CSLSDO}	$\overline{CS}$ falling edge to SDO	20pF			25	ns
t_{SDO}	SCLK falling edge to SDO	20pF			25	ns
t_{CSHSDO}	$\overline{CS}$ rising edge to SDO returns to high	20pF			25	ns
t_{CSD}	$\overline{CS}$ high time between SPI commands	$-40^\circ C$ to $+125^\circ C$	20			ns
$t_{CSLSCLK}$	CS falling edge to SCLK becomes stable	$-40^\circ C$ to $+125^\circ C$	8			ns
$t_{CSHSCLK}$	CS rising edge to SCLK becomes stable	$-40^\circ C$ to $+125^\circ C$	8			ns

6.12 SPI Timing Characteristics (2.7V)

 $V_L = 2.7V$, GND = 0V (unless otherwise noted)

 $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
AC_to_D x	AC active edge to Dx	$V_{DD} = 2.7V$		37		ns
f_{CLK_SPI}	SCLK Frequency	$-40^\circ C$ to $+125^\circ C$			25	MHz
t_R , t_F_SPI	SPI Clock Rise and Fall Times	$-40^\circ C$ to $+125^\circ C$			25	ns
t_{CLK_SPI}	SCLK Period	$-40^\circ C$ to $+125^\circ C$	40			ns
$t_{CLK_H_SPI}$	SCLK High Time	$-40^\circ C$ to $+125^\circ C$	16			ns
$t_{CLK_L_SPI}$	SCLK Low Time	$-40^\circ C$ to $+125^\circ C$	16			ns
t_{CSS}	Set Up Time $\overline{CS}$ to SCLK	$-40^\circ C$ to $+125^\circ C$	20			ns
t_{SU_SPI}	Set Up Time SDI to SCLK	$-40^\circ C$ to $+125^\circ C$	12			ns
t_{H_SPI}	Hold Time SDI to SCLK	$-40^\circ C$ to $+125^\circ C$	18			ns
t_{CSH}	Hold Time SCLK to $\overline{CS}$	$-40^\circ C$ to $+125^\circ C$	20			ns
t_{CSLSDO}	$\overline{CS}$ falling edge to SDO	20pF			50	ns
t_{SDO}	SCLK falling edge to SDO	20pF			50	ns
t_{CSHSDO}	$\overline{CS}$ rising edge to SDO returns to high	20pF			50	ns
t_{CSD}	$\overline{CS}$ high time between SPI commands	$-40^\circ C$ to $+125^\circ C$	40			ns
$t_{CSLSCLK}$	CS falling edge to SCLK becomes stable	$-40^\circ C$ to $+125^\circ C$	16			ns

$V_L = 2.7V$, GND = 0V (unless otherwise noted)
 $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{CSHSCLK}$	CS rising edge to SCLK becomes stable		$-40^\circ C$ to $+125^\circ C$	16			ns

6.13 SPI Timing Characteristics (1.8V)

$V_L = 1.8V$, GND = 0V (unless otherwise noted)
 $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
AC_to_Dx	AC active edge to Dx	$V_{DD} = 1.8V$	$-40^\circ C$ to $+125^\circ C$		61		ns
f_{CLK_SPI}	SCLK Frequency		$-40^\circ C$ to $+125^\circ C$			25	MHz
t_R, t_F_SPI	SPI Clock Rise and Fall Times		$-40^\circ C$ to $+125^\circ C$			25	ns
t_{CLK_SPI}	SCLK Period		$-40^\circ C$ to $+125^\circ C$	40			ns
$t_{CLK_H_SPI}$	SCLK High Time		$-40^\circ C$ to $+125^\circ C$	16			ns
$t_{CLK_L_SPI}$	SCLK Low Time		$-40^\circ C$ to $+125^\circ C$	16			ns
t_{CSS}	Set Up Time $\overline{CS}$ to SCLK		$-40^\circ C$ to $+125^\circ C$	20			ns
t_{SU_SPI}	Set Up Time SDI to SCLK		$-40^\circ C$ to $+125^\circ C$	12			ns
t_{H_SPI}	Hold Time SDI to SCLK		$-40^\circ C$ to $+125^\circ C$	18			ns
t_{CSH}	Hold Time SCLK to $\overline{CS}$		$-40^\circ C$ to $+125^\circ C$	20			ns
t_{CSLSDO}	$\overline{CS}$ falling edge to SDO	20 pF	$-40^\circ C$ to $+125^\circ C$			50	ns
t_{SDO}	SCLK falling edge to SDO	20 pF	$-40^\circ C$ to $+125^\circ C$			50	ns
t_{CSHSDO}	$\overline{CS}$ rising edge to SDO returns to high	20pF	$-40^\circ C$ to $+125^\circ C$			50	ns
t_{CSD}	$\overline{CS}$ high time between SPI commands		$-40^\circ C$ to $+125^\circ C$	40			ns
$t_{CSLSCLK}$	CS falling edge to SCLK becomes stable		$-40^\circ C$ to $+125^\circ C$	16			ns
$t_{CSHSCLK}$	CS rising edge to SCLK becomes stable		$-40^\circ C$ to $+125^\circ C$	16			ns

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in the following figure. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed as shown in Figure 7-1 with $R_{ON} = V / I_{SD}$:

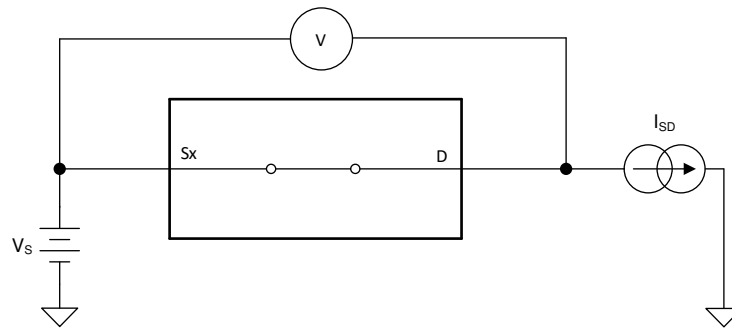


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 7-2 shows the setup used to measure both off-leakage currents.

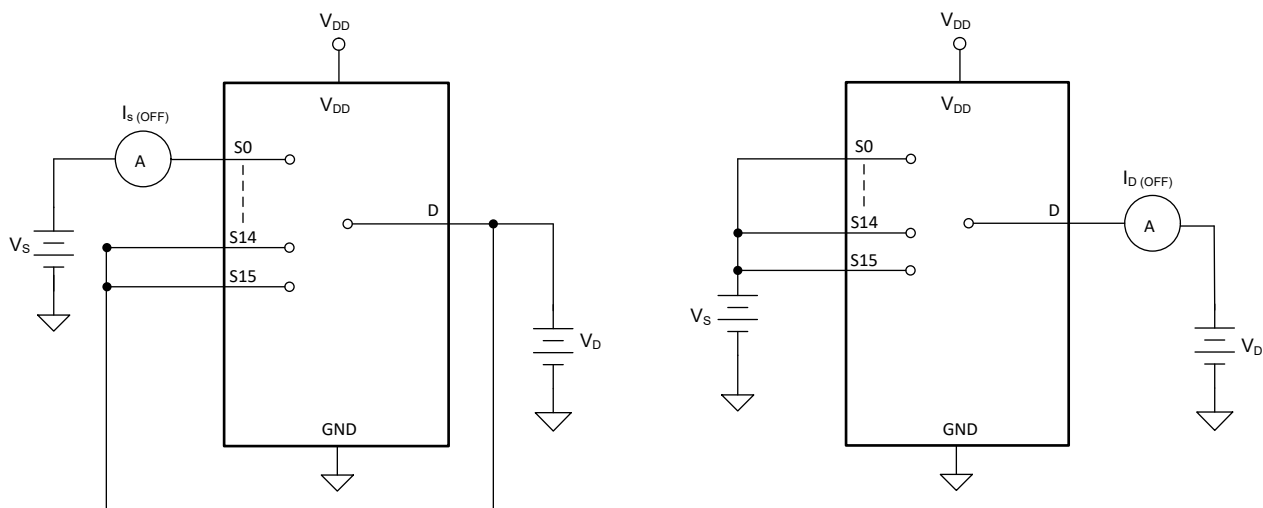


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

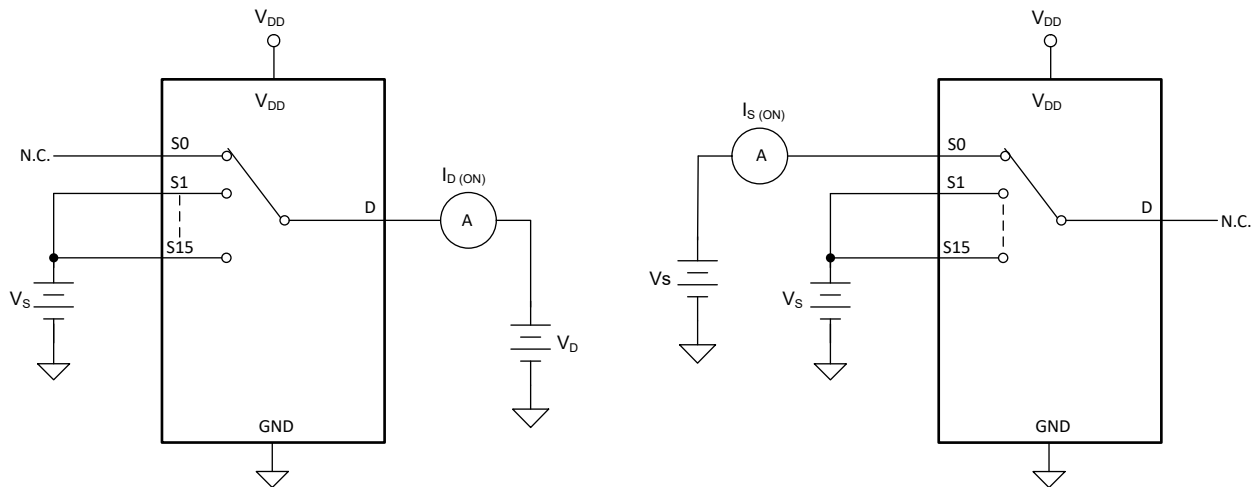


Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 50% after the address signal has risen or fallen past the 50% threshold. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{\text{TRANSITION}}$.

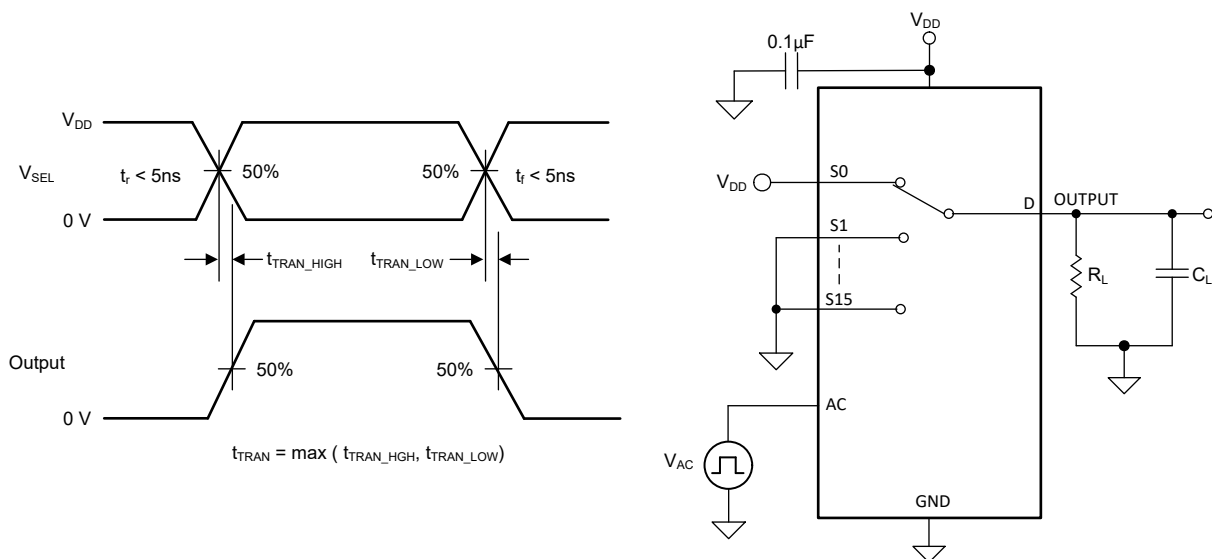


Figure 7-4. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{\text{OPEN(BBM)}}$.

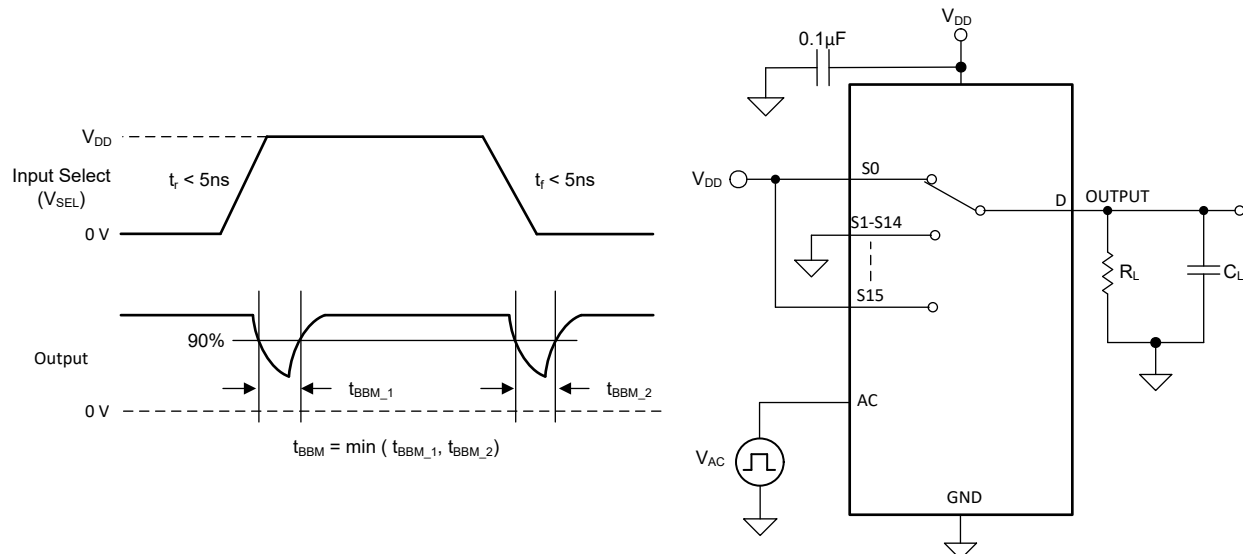


Figure 7-5. Break-Before-Make Delay Measurement Setup

7.6 $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the 50% threshold. The 10% measurement is used to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol $t_{\text{ON(EN)}}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the 50% threshold. The 90% measurement is used to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol $t_{\text{OFF(EN)}}$.

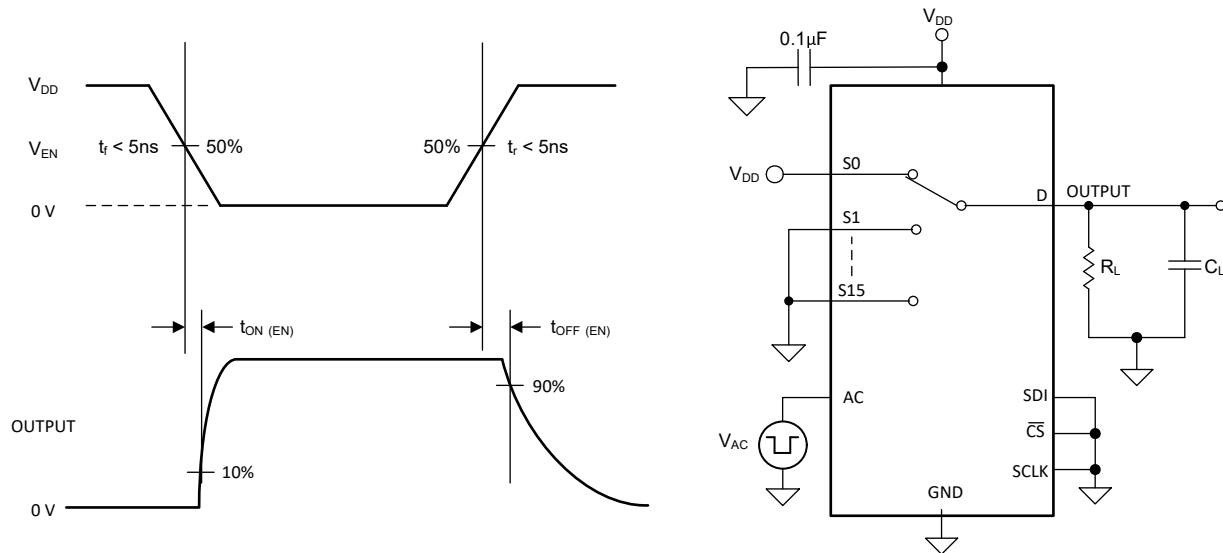


Figure 7-6. Turn-On and Turn-Off Time Measurement Setup

7.7 Charge Injection

The TMUXS1306A and TMUXS1307A device have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C . Figure 7-7 shows the setup used to measure charge injection from source (Sx) to drain (D).

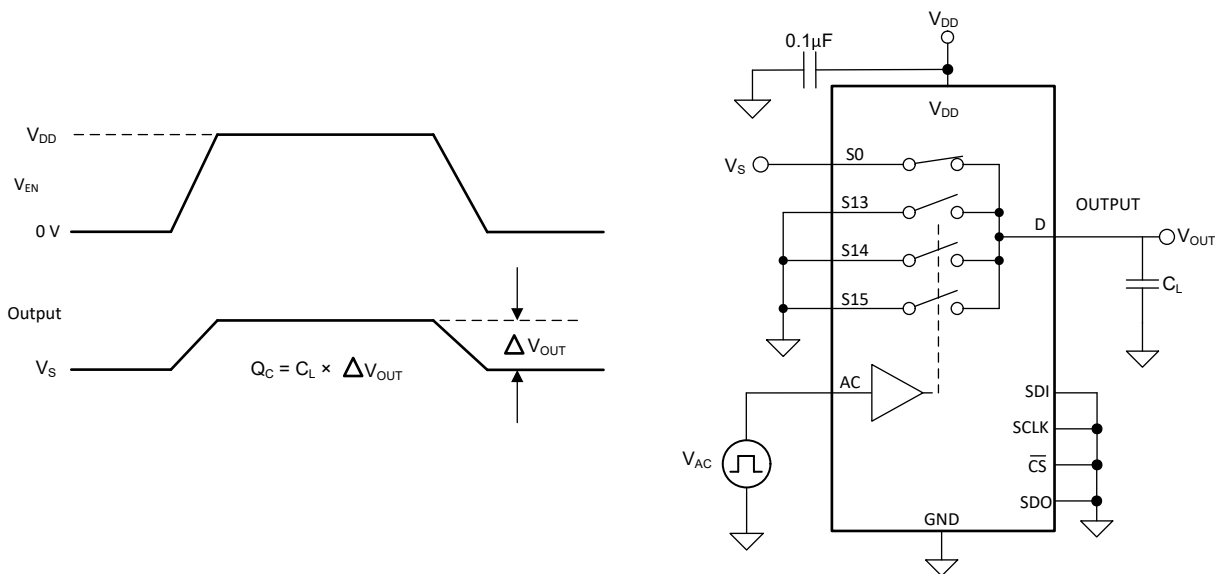


Figure 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-8 shows the setup used to measure, and the equation to compute off isolation.

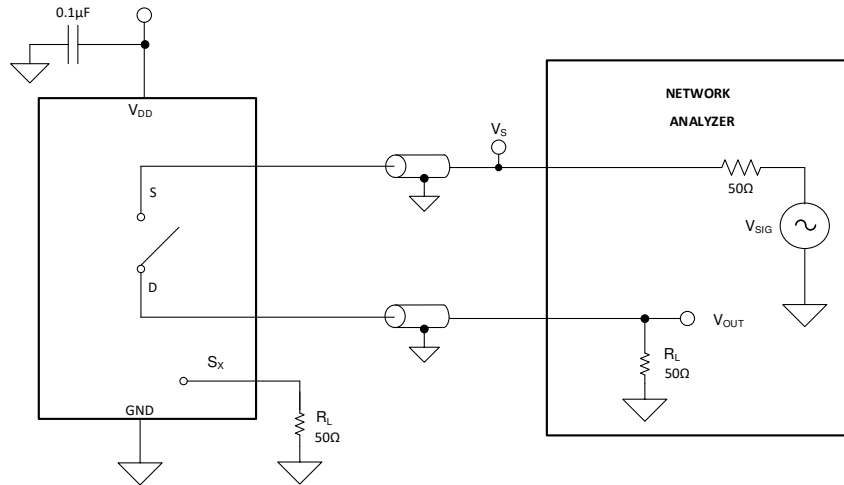


Figure 7-8. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \times \text{Log} \left(\frac{V_{OUT}}{V_S} \right) \quad (1)$$

7.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. [Figure 7-9](#) shows the setup used to measure, and the equation used to compute crosstalk.

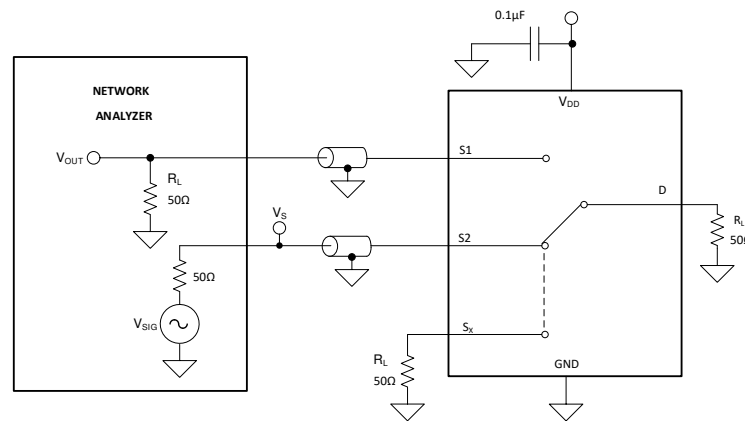


Figure 7-9. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel - to - Channel Crosstalk} = 20 \times \text{Log} \left(\frac{V_{OUT}}{V_S} \right) \quad (2)$$

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. [Figure 7-10](#) shows the setup used to measure bandwidth.

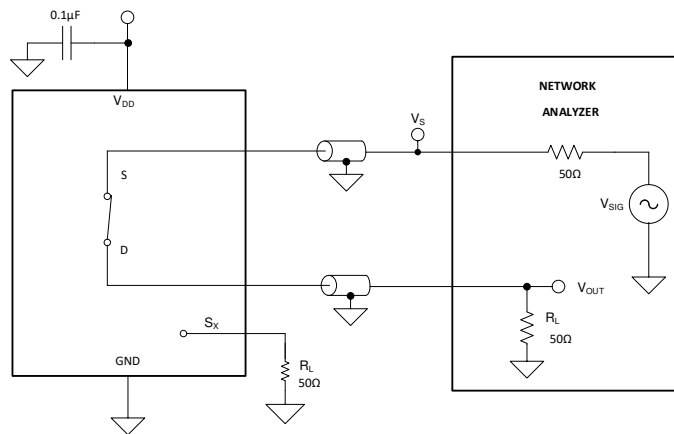


Figure 7-10. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \times \log \left(\frac{V_2}{V_1} \right) \quad (3)$$

7.11 Injection Current Control

Injection current is measured at the change in output of the enabled signal path when a current is injected into a disabled signal path. Figure 7-11 shows the setup used to measure injection current control.

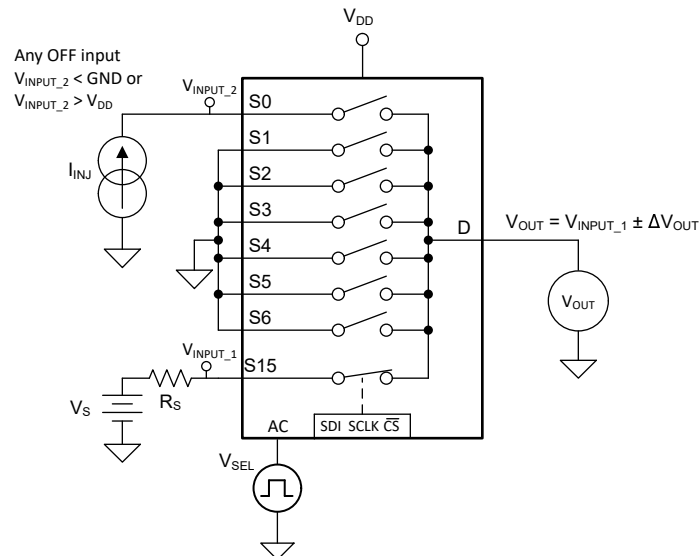


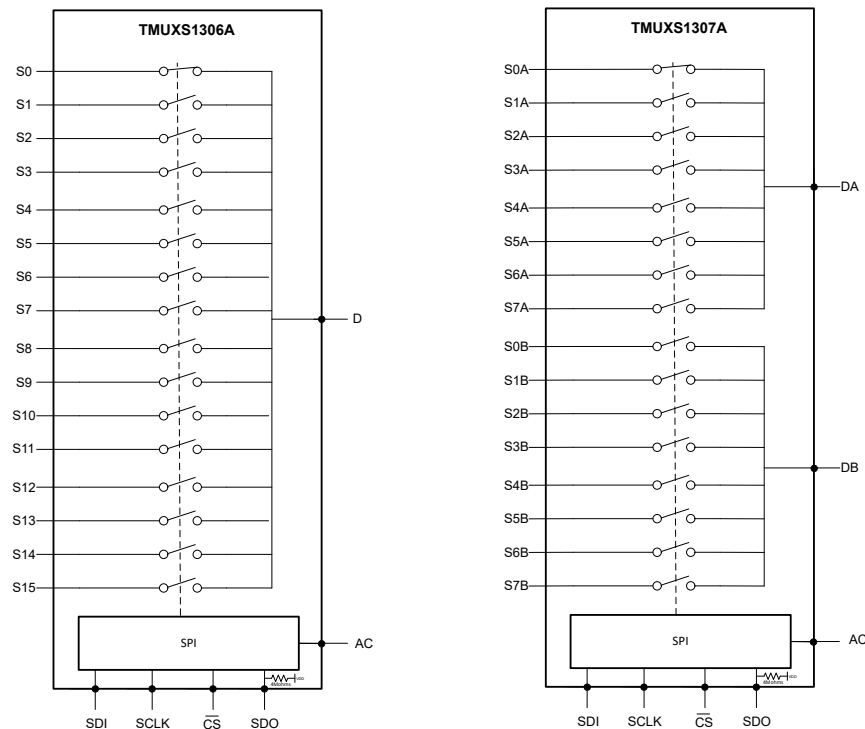
Figure 7-11. Injection Current Measurement Setup

8 Detailed Description

8.1 Overview

The TMUXS1306A is a 16:1, single-ended (1-channel) mux. The TMUXS1307A is a 8:1, differential (2-channel) mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUXS1306A and TMUXS1307A devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions so the signal paths can be used as both multiplexers and demultiplexers to support both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for the TMUXS1306A and TMUXS1307A ranges from GND to V_{DD} .

8.3.3 1.8V Logic Compatible Inputs

The TMUXS1306A and TMUXS1307A support 1.8V logic compatible control for all logic control inputs. The logic input thresholds scale very slightly with supply but still provide 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allows the multiplexers to interface with processors that have lower logic I/O rails but is based on V_{DD} voltage levels for logic output. The current consumption of the TMUXS1306A and TMUXS1307A devices increase when using 1.8V logic with higher supply voltage. For more information on 1.8V logic implementations, see also [1.8V Logic for Multiplexers and Signal Switches application brief](#).

8.3.4 Fail-Safe Logic

The TMUXS1306A and TMUXS1307A devices have fail-safe logic on the control input pins (SCLK, SDI, CS, and AC_{yc}) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-safe logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins.

For example, the fail-safe logic feature allows the IO pins of the TMUXS1306A and TMUXS1307A to be ramped to 5.5V while $V_{DD} = 0V$. Additionally, the feature enables operation of the multiplexers with $V_{DD} = 1.8V$ while allowing the IO pins to interface with a logic level of another device up to 5.5V, eliminating the potential need for an external voltage translator.

SDO outputs V_{DD} level logic and needs either translators or resistor dividers to the MCU if operating at lower MCU logic levels.

8.3.5 Injection Current Control

On a high level, Injection current control is a feature that prevents an overvoltage event on an unactive channel from impacting the signal on an active one. The pin that experiences an overvoltage event will be held at $V_{DD} + V_T$, where $V_T \approx 0.6V$. The excess current caused by clamping this voltage will flow through an internal circuit that must remain within the current specifications of the device. By doing this, the device can prevent the excess current from injecting into the ON-channel causing errors in measurement. Injection current is the current that is being forced into a pin by an input voltage (V_{IN}) higher than the positive supply ($V_{DD} + \Delta V$) or lower than ground (V_{SS}). The current flows through the input protection diodes into whichever supply of the device is potentially compromising the accuracy and reliability of the system. Injected currents can come from various sources depending on the application.

- Harsh environments and applications with long cabling, such as in factory automation and automotive systems, may be susceptible to injected currents from switching or transient events.
- Other self-contained systems can also be subject to injected current if the input signal is coming from various sensors or current sources.

Injected Current Impact: typical CMOS switches have ESD protection diodes on the inputs and outputs. These diodes not only serve as ESD protection but also provide a voltage clamp to prevent the inputs or outputs going above V_{DD} or below GND and V_{SS} . When current is injected into the pin of a disabled signal path, a small amount of current goes through the ESD diode but most of the current goes through conduction to the drain. If forward diode voltage of the ESD diode (V_F) is greater than the PMOS threshold voltage (V_T), then the PMOS of all OFF switches turns ON and there would be undesirable subthreshold leakage between the source and the drain that can lift the OFF source pins up also. [Figure 8-1](#) shows a simplified diagram of a typical CMOS switch and associated injected current path.

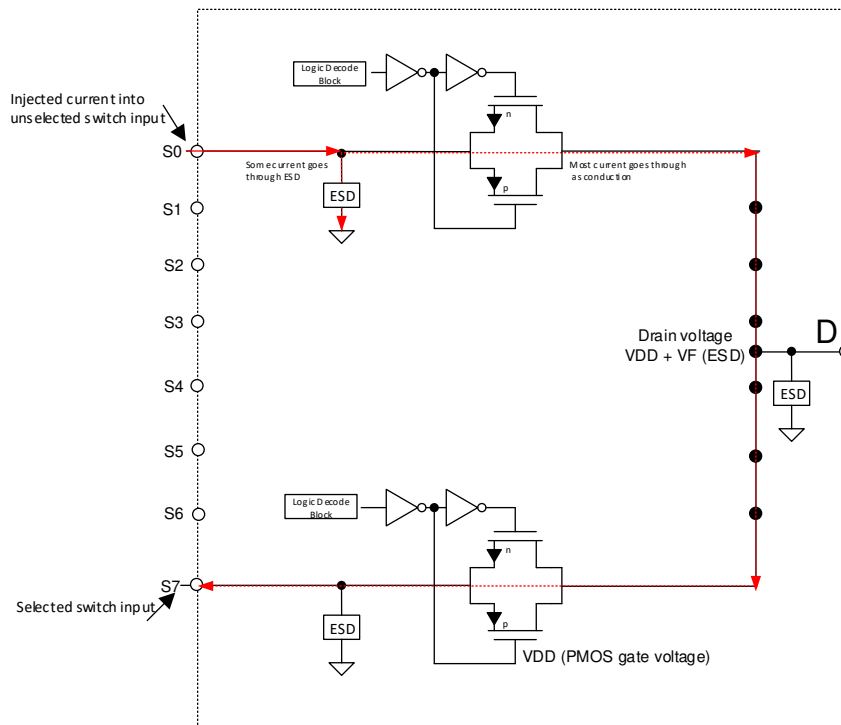


Figure 8-1. Simplified Diagram of Typical CMOS Switch and Associated Injected Current Path

It is quite difficult to cut off these current paths. The drain pin can never be allowed to exceed the voltage above V_{DD} by more than a V_T . Analog pins can be protected against current injection by adding external components like a Schottky diode from the drain pin to ground to clamp the drain voltage at $< V_{DD} + V_T$ and cut off the current path.

Change in R_{ON} due to Current Injection: because the ON resistance of the enabled FET switch is impacted by the change in the supply rail, when the drain pin voltage exceeds the supply voltage by more than a V_T , an error in the output signal voltage can be expected. This undesired change in the output can cause issues related to false trigger events and incorrect measurement readings, potentially compromising the accuracy and reliability of the system. As shown in Figure 8-2, S2 is the enabled signal path that is conducting a signal from S2 pin to D pin. Because there is an injected current at the disabled S1 pin, the voltage at that pin increases above the supply voltage and the ESD protection diode is forward biased, shifting the power supply rail. This shift in supply voltage alters the R_{ON} of the internal FET switches, causing a ΔV error on the output at the D pin.

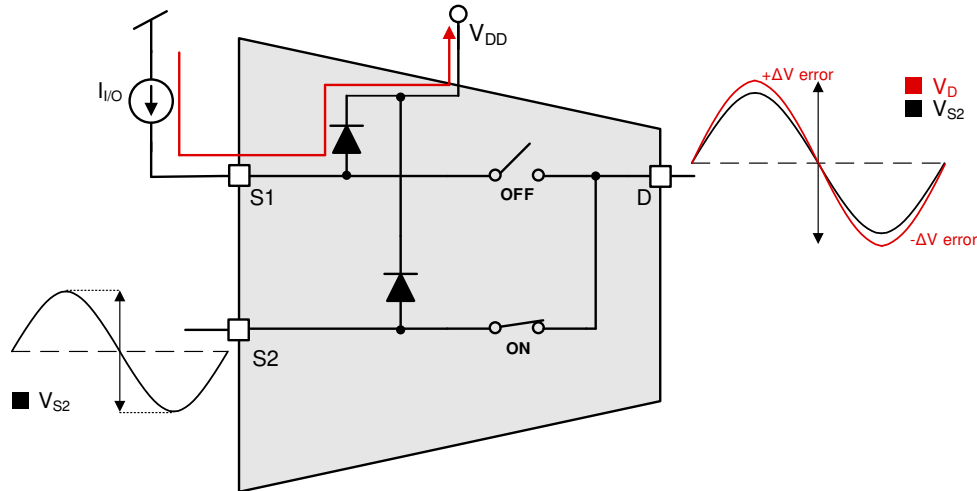


Figure 8-2. Injected Current Impact on R_{ON}

To avoid the complications of added external protection to your system, the TMUXS1306A and TMUXS1307A devices have an internal injection current control feature which eliminates the need for external diode and resistor networks typically used to protect the switch and keep the input signals within the supply voltage. The internal injection current control circuitry allows the signals on the disabled signal paths to exceed the supply voltage without affecting the signal of the enabled signal path. The injection current control circuitry also protects the TMUXS130xA from currents injected into disabled signal paths without impacting the enabled signal path, which typical CMOS switches do not support. Additionally, the TMUXS1306A and TMUXS1307A do not have any internal diode paths to the supply pin, which eliminates the risk of damaging components connected to the supply pin or providing unintended power to the system supply rail. For a simplified diagram that shows one signal path for the TMUXS130xA devices and the associated injection current circuit, refer to Section 8.2.

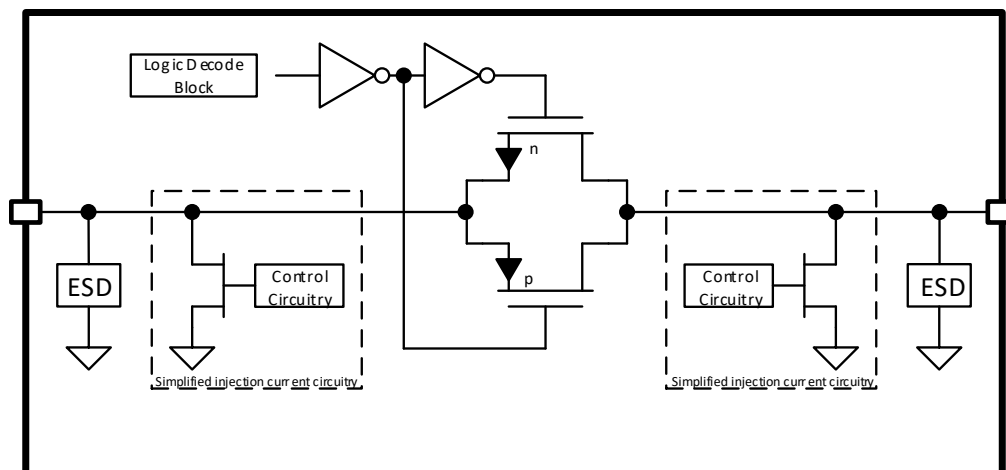


Figure 8-3. Simplified Diagram of Injection Current Control

The injection current control circuitry is independently controlled for each source or drain pin (S_x or D). The control circuitry for a particular pin is enabled when that input is disabled by the logic pins and the injected current causes the voltage at the pin to be above V_{DD} or below GND . The injection current circuit includes an FET to shunt the undesired current to GND in the case of overvoltage or injected current events. Each injection current circuit is rated to handle up to 50mA; the device, however, can support a maximum current of 100mA at any given time. Depending on the system application, a series limiting resistor may be needed and must be sized appropriately. Figure 8-3 shows the TMUXS130xA protection circuitry with an injected current at an input pin.

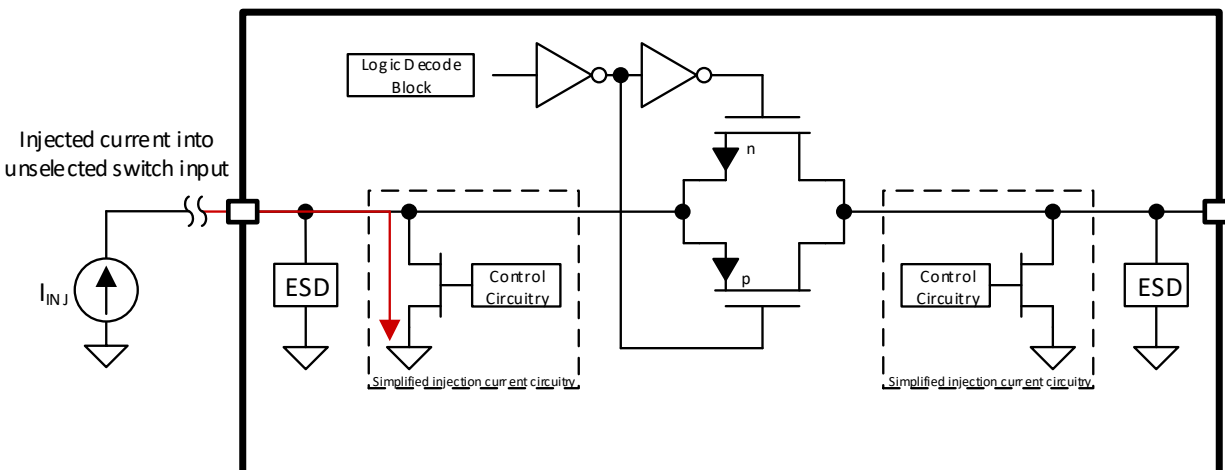


Figure 8-4. Injected Current at Input Pin

Figure 8-5 shows an example of using a series limiting resistor in the case of an overvoltage event.

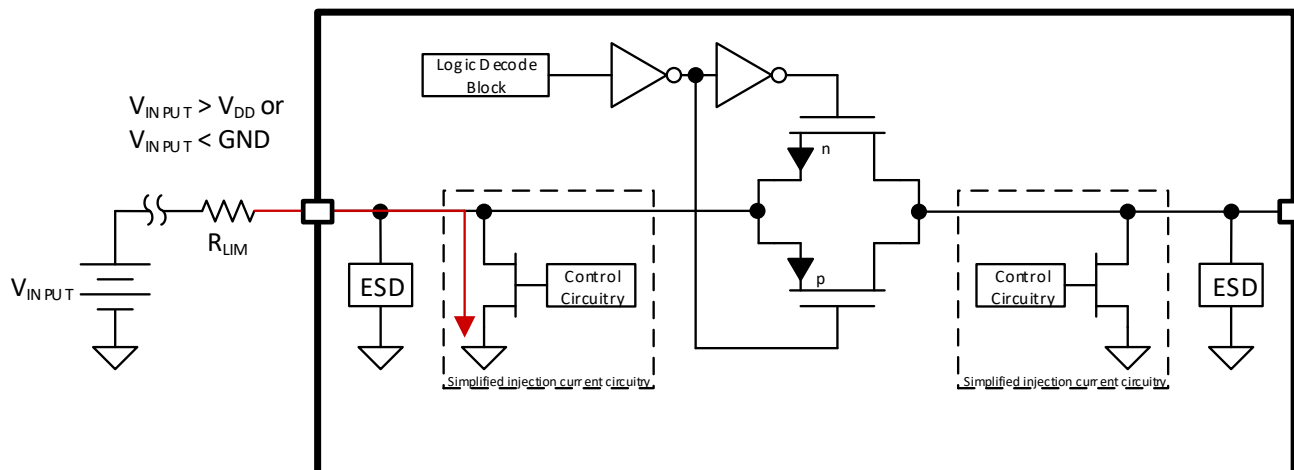


Figure 8-5. Over-Voltage Event with Series Resistor

For the injection current control circuitry to be active the voltage at the source or drain pins is greater than V_{DD} , or less than GND . With this requirement met, the protection FET will be turned on for any disabled or enabled signal path and shunt the pin to GND . In this event, a series resistor is needed to limit the total current injected into the device to be less than 100mA. Three example scenarios are outlined in the following sections.

8.4 Device Functional Modes

The TMUXS130xA has 16 input switches, one of which can be passed through to a single output that is turned on or turned off through the SPI. This device can operate without any external components.

The SPI features error detection, auto cycle mode, supports daisy chain with multiple devices, and SPI modes 0 and 3. Additionally, the SCLK can operate at speeds up to 10MHz for SPI logic levels 1.8V to 5.5V.

Table 8-1. TMUXS130xA SPI Frame

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Read/ Write	Address A6:A0							Data D15:D0															

8.4.1 SPI Operation

TMUXS130xA is a 16:1 SPI controlled multiplexer and has SPI error detection features. SPI data input on SDI is sampled on the positive edge of SCLK, but SPI output data on SDO gets shifted out on the negative edge of SCLK. TMUXS130xA is compatible with SPI modes 0 and 3. While in address mode, TMUXS130xA registers are accessed with 24-bit SPI commands sent while $\overline{CS}$ is pulled low. [Auto cycle mode](#), [Burst mode](#), and [Daisy chain mode](#) are other modes that TMUXS130xA can operate within. The following is a list of error detection and status features offered:

1. Injection-current Clamp Status - Register needs to be read, and only indicates an ACTIVE current-clamp
2. Address R/W Error Flag - Disabled by default
3. SCLK Count Error Flag - Disabled by default
4. CRC (Cyclic Redundancy Check) Enable and Error Flag - Disabled by default
5. Clearing Error Flags

TMUXS130xA SPI pins include AC (Auto-Cycle), SDI, SDO, SCLK and $\overline{CS}$.

8.4.1.1 Auto Cycle Mode

The default state of TMUXS130xA is auto cycle (AC) mode. While in auto cycle mode, the device automatically toggles from SW_n to SW_{n+1} with TMUXS1306A and then SW_{nA} to SW_{nA+1} of channel 1 and SW_{nB} to SW_{nB+1} for TMUXS1307A on the rising edge of the signal provided to the AC pin. While in auto cycle mode, the only register that can be written to is the MODCFG register; however, all registers can be read from. To leave AC mode, the user must change the first bit in register 0x0C to 0. Burst mode can also be enabled while exiting AC mode, and during the burst write AC mode can be re-enabled, and burst mode disabled.

A full cycle of auto cycle mode is considered a "Pattern". A pattern can consist of a "1" that indicates a switch is active, or a "0" which indicates a switch is inactive. For example, 0xFFFF indicates every switch is active and transitioned to in the pattern, but 0x0005 means only switches 0 and 2 are active and are cycled through with only two active edges on the AC pin.

There are eight pattern registers (0x04xx through 0x0Bxx). Each pattern register can be overwritten with custom patterns. During a device power down all registers are reset to the default states.

The ACSEL register allows the user to select multiple patterns to cycle through. For example, if a user selects patterns 0 and 1 (ACSEL = 0x0003, Pattern0 = 0xFFFF and Pattern1 = 0xAAAA) then the switches run through 0xFFFF followed by 0xAAAA, and then back to 0xFFFF.

There are multiple options in the MODCFG register that helps with the configurability of AC mode. To modify this register, the AC mode must be disabled first.

AC_1CH_ALWAYS_ON turns off all switches at the end of every pattern, requiring an additional AC to begin the next pattern. To get through a full pattern with AC_1CH_ALWAYS_ON, 16 rising edges are required, or 17 with AC_1CH_ALWAYS_ON disabled.

AC_EDGE_CONFIG sets what edge the switches transition on.

1. 0b00: sets the AC to transition on rising edge only
2. 0b01: sets AC to transition on falling edge only
3. 0b10: sets AC to transition on both rising edge AND falling edge

4. 0b11: sets AC to transition on rising edge only (repeat of 0b00)

8.4.1.2 Address Mode

For TMUXS130xA to enter address mode, AC mode must be disabled first by sending 0x0C0002. While in address mode, the SPI frame expects the following sequence:

1. $\overline{CS}$ is pulled low
2. Default of 24 SCLK cycles (or 32 SCLK cycles if CRC is enabled), 24-bit command (1 R/W bit, 7 address bits, followed by a 16-bit data)
3. $\overline{CS}$ is pulled high

When the first bit of command is a 0, this value indicates a write is being performed. When the first bit is a 1, this value indicates a read is being performed. The next seven bits following are for the target register address. The target register is determined during the 8th SCLK cycle. The last 16 bits are written to the targeted register after $\overline{CS}$ returns to a HIGH logic level (assuming no SPI errors), or the bits are ignored when performing a read. While performing a read, the last 16 bits on SDI are ignored because SDO output the addressed register state during these last 16 SCLK cycles. During the first eight bits of any command, SPI sends out eight ERRFLG bits on SDO.

8.4.1.3 Burst Mode

TMUXS130xA enters burst mode through a write to the burst mode enable bit in the MODCFG register found in the *Register Map*. Burst mode grants the ability to send numerous SPI commands consecutively without deasserting the $\overline{CS}$ pin. While in burst mode, the operation is in 24-bit frames for the first frame, followed by 16-bit subsequent commands for the burst, or with CRC enabled 32-bit frame for the initial followed by 24-bit commands. The SDO pin aligns with the same response expected while in address mode- for reads SDO returns read-back values, and for writes SDO outputs the ERRFLG status bits. The SCLK error behaves in a different manner to address mode. If the SCLK count is not a multiple of 16 or 24, then the SCLK error flag asserts (excluding the address). CRC and read/write invalid errors operate while in burst mode similarly to operation in address mode.

8.4.1.4 Daisy Chain Mode

Multiple TMUXS130xA can be chained together to operate similarly to a shift register. All SPI pins are shared across all devices in the chain, but the SDO pin is connected to the SDI of the next device in the chain. Daisy chain mode is entered by sending the command "0x57" (or "0x7D" with CRC), and an additional 0x00 for every device in the chain. For example, if there are three devices: 0x570000 is sent, 4 is 0x57000000, and so forth. When multiple devices are configured in hardware to be in daisy chain mode, the first command sent is expected to be the daisy chain mode entry command. As the first device is entering daisy chain mode, the device is simultaneously sending out "0xC0" for the first eight bits indicating no SPI errors, and then relays the daisy chain command to enter the next device into daisy chain mode. After the series of devices is in daisy chain mode, the $\overline{CS}$ pin must be pulled low to send switch state commands.

The SDO pin acts as an 8-cycle delayed SDI of the same device. After all devices in the chain have received a switch state command and the $\overline{CS}$ pin is pulled high, each device enters the switch states that are assigned to the device. While in daisy chain mode, all commands only target the switch state registers so configuration registers are unavailable. For each TMUXS1306A in the daisy chain, the command sent must have 4 bits to indicate which switch from each device is enabled. For TMUXS1307A, the daisy chain the command sent must have 8 bits to indicate which switch from each device is enabled where 0bx000x000 the 3 MSBs represent channel A (Switches 0-7) and LSBs represent channel B (Switches 8-15) and the "x" are "Don't Care". To leave daisy chain mode, a power cycle of V_{DD} is necessary.

8.4.1.5 Software Reset

While in address mode, a software reset can be performed by writing the following command to the register 0x9A:

1. 0x0002

The register values reset to default after performing a software reset.

9 TMUXS1306A Register Map

Table 9-1. TMUXS1306A Register Map

Register	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Permission
0x00	SW_DATA	SW15_EN	SW14_EN	SW13_EN	SW12_EN	SW11_EN	SW10_EN	SW9_EN	SW8_EN	SW7_EN	SW6_EN	SW5_EN	SW4_EN	SW3_EN	SW2_EN	SW1_EN	SW0_EN	0x0000	R/W
0x01	ERR_CONFIG	Reserved													RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x0000	R/W
0x02	ERR_FLAGS	Reserved									AC Counter				RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x0000	R
0x03	AC_SEL	Reserved								AC_Pattern7_EN	AC_Pattern6_EN	AC_Pattern5_EN	AC_Pattern4_EN	AC_Pattern3_EN	AC_Pattern2_EN	AC_Pattern1_EN	AC_Pattern0_EN	0x0001	R/W
0x04	PATTERN0	Pattern 0 (Configurable)																0xFF	R/W
0x05	PATTERN1	Pattern 1 (Configurable)																0xAA	R/W
0x06	PATTERN2	Pattern 2 (Configurable)																0x55	R/W
0x07	PATTERN3	Pattern 3 (Configurable)																0x00	R/W
0x08	PATTERN4	Pattern 4 (Configurable)																0xFF	R/W
0x09	PATTERN5	Pattern 5 (Configurable)																0x0F	R/W
0x0a	PATTERN6	Pattern 6 (Configurable)																0xFF	R/W
0x0B	PATTERN7	Pattern 7 (Configurable)																0xF5	R/W
0x0C	MODE_CONFIG	Reserved										BURST_MODE_EN	Reserved	AC_EDGE_CONFIG		AC_1CH_ALWAYS_ON	AC_MOD_EN	0x0003	R/W
0x17	STB_STATUS	SW15_SHORT_STATUS	SW14_SHORT_STATUS	SW13_SHORT_STATUS	SW12_SHORT_STATUS	SW11_SHORT_STATUS	SW10_SHORT_STATUS	SW9_SHORT_STATUS	SW8_SHORT_STATUS	SW7_SHORT_STATUS	SW6_SHORT_STATUS	SW5_SHORT_STATUS	SW4_SHORT_STATUS	SW3_SHORT_STATUS	SW2_SHORT_STATUS	SW1_SHORT_STATUS	SW0_SHORT_STATUS	0x0000	R
0x1A	SOFT_RESET	SOFT_RST_B																0x0000	R/W

10 TMUXS1307A Register Map

Table 10-1. TMUXS1307A Register Map

Register	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Permission
0x00	SW_DATA	SW_B7_EN	SW_B6_EN	SW_B5_EN	SW_B4_EN	SW_B3_EN	SW_B2_EN	SW_B1_EN	SW_B0_EN	SW_A7_EN	SW_A6_EN	SW_A5_EN	SW_A4_EN	SW_A3_EN	SW_A2_EN	SW_A1_EN	SW_A0_EN	0x0000	R/W
0x01	ERR_CONFIG	Reserved													RW_ERR_EN	SCL_K_ERR_EN	CRC_ERR_EN	0x0000	R/W
0x02	ERR_FLAGS	Reserved							AC Counter 2			AC Counter 1			RW_ERR_FLAG	SCL_K_ERR_FLAG	CRC_ERR_FLAG	0x0000	R
0x03	AC_SEL	Reserved								AC_Pattern7_EN	AC_Pattern6_EN	AC_Pattern5_EN	AC_Pattern4_EN	AC_Pattern3_EN	AC_Pattern2_EN	AC_Pattern1_EN	AC_Pattern0_EN	0x0001	R/W
0x04	PATTERN0	Pattern 0 (Configurable 0b-7b are CH1, 8b-15b are CH2)																0xFF FF	R/W
0x05	PATTERN1	Pattern 1 (Configurable)																0xAA AA	R/W
0x06	PATTERN2	Pattern 2 (Configurable)																0x55 55	R/W
0x07	PATTERN3	Pattern 3 (Configurable)																0x00 FF	R/W
0x08	PATTERN4	Pattern 4 (Configurable)																0xFF 00	R/W
0x09	PATTERN5	Pattern 5 (Configurable)																0x0F FF	R/W
0x0a	PATTERN6	Pattern 6 (Configurable)																0xFF F0	R/W
0x0B	PATTERN7	Pattern 7 (Configurable)																0xF5 F5	R/W
0x0C	MODE_CONFIG	Reserved										BURST_MODE_EN	Reserved	AC_EDGE_CONFIG		AC_1CH_ALWAYS_ON	AC_MOD_EN	0x0003	R/W
0x17	STB_STATUS	SW_B7_SHOT_STATUS	SW_B6_SHOT_STATUS	SW_B5_SHOT_STATUS	SW_B4_SHOT_STATUS	SW_B3_SHOT_STATUS	SW_B2_SHOT_STATUS	SW_B1_SHOT_STATUS	SW_B0_SHOT_STATUS	SW_A7_SHOT_STATUS	SW_A6_SHOT_STATUS	SW_A5_SHOT_STATUS	SW_A4_SHOT_STATUS	SW_A3_SHOT_STATUS	SW_A2_SHOT_STATUS	SW_A1_SHOT_STATUS	SW_A0_SHOT_STATUS	0x0000	R
0x1A	SOFT_RESET	SOFT_RST_B																0x0000	R/W

ADVANCE INFORMATION

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TMUXS130xA family offers protection against injection current events across a wide operating supply range (1.62V to 5.5V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/O rails. Additionally, the control input pins support fail-safe logic which allows for operation up to 5.5V, regardless of the state of the supply pin. This feature stops the logic pins from back-powering the supply rail while the injection current circuitry prevents the signal path from back-powering the supply. These features make the TMUXS130xA a family of general purpose multiplexers and switches that can reduce system complexity, board size, and overall system cost.

11.2 Typical Application

One useful application that takes advantage of the TMUXS130xA features is multiplexing various signals into an ADC that is integrated into an MCU. Utilizing an integrated ADC in an MCU allows a system to minimize cost with a potential tradeoff of system performance when compared to an external ADC. The multiplexer allows for multiple inputs or sensors to be monitored with a single ADC pin of the device, which is critical in systems with limited I/O. The TMUXS1307A is an excellent choice for a similar design example using differential signals, or as two 8:1 multiplexers.

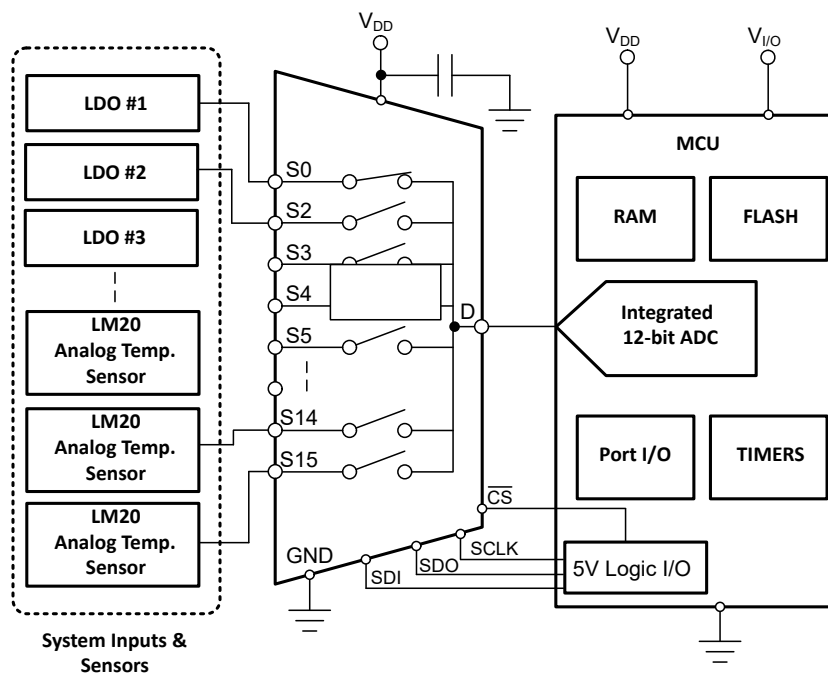


Figure 11-1. Multiplexing Signals to Integrated ADC

11.2.1 Design Requirements

For this design example, use the parameters listed in [Table 11-1](#).

Table 11-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5.0V
I/O signal range	0V to V_{DD} (Rail to Rail)
Control logic thresholds	5V
Switch inputs	Sixteen

11.2.2 Detailed Design Procedure

The TMUXS1306A and TMUXS1307A can operate without any external components except for the supply decoupling capacitors. All inputs being muxed to the ADC of the MCU must fall within the recommended operating conditions of the TMUXS1306A and TMUXS1307A, including signal range and continuous current. For this design with a supply of 5V, the signal range can be 0V to 5V; the maximum continuous current can be 100mA at an ambient temperature of 85°C or 25mA at 125°C.

11.3 Power Supply Recommendations

The TMUXS1306A and TMUXS1307A devices operate across a wide supply range of 1.62V to 5.5V.

Note

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μ F to 10 μ F from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections.

TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer good noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11.4 Layout

11.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. [Figure 11-2](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

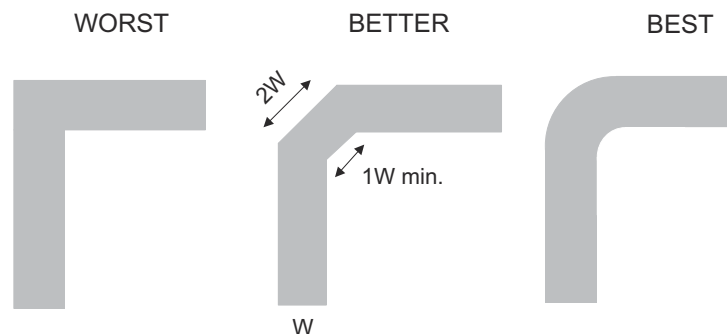


Figure 11-2. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around to minimize the capacitance. Each via introduces discontinuities in the signal transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 11-3 shows an example of a PCB layout with the TMUXS1306A and TMUXS1307A. Some key considerations are as follows:

- Decouple the V_{DD} pin with a $0.1\mu\text{F}$ capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.4.2 Layout Example

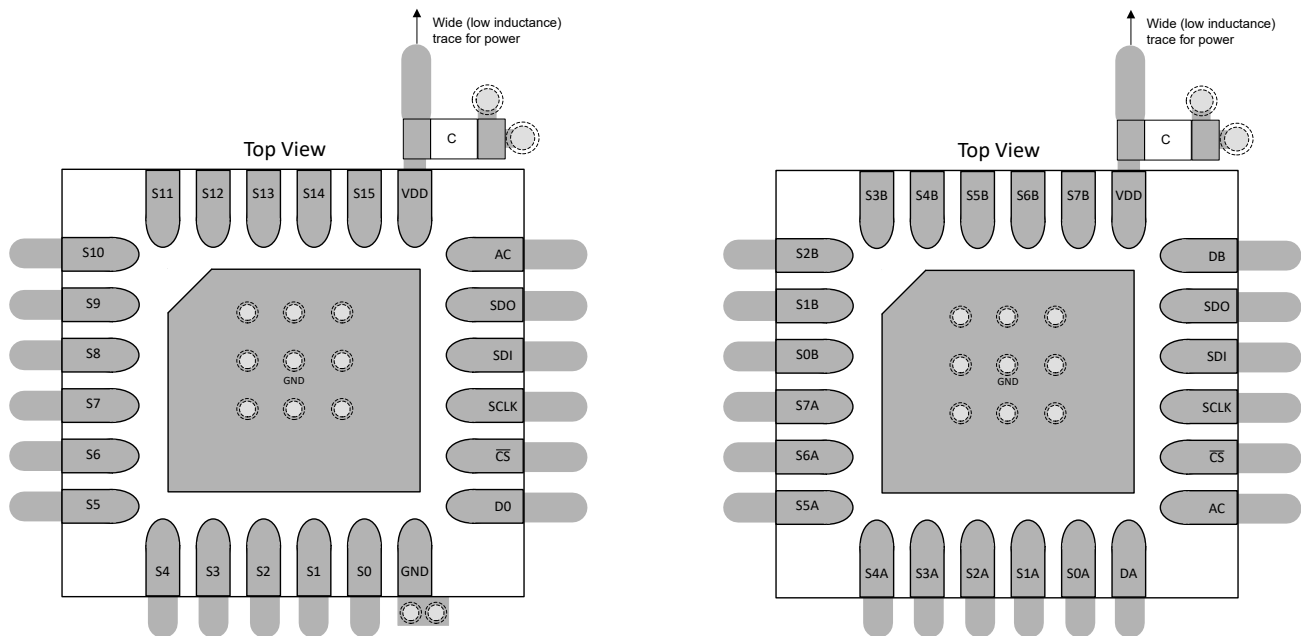


Figure 11-3. TMUXS1306A and TMUXS1307A Layout Example

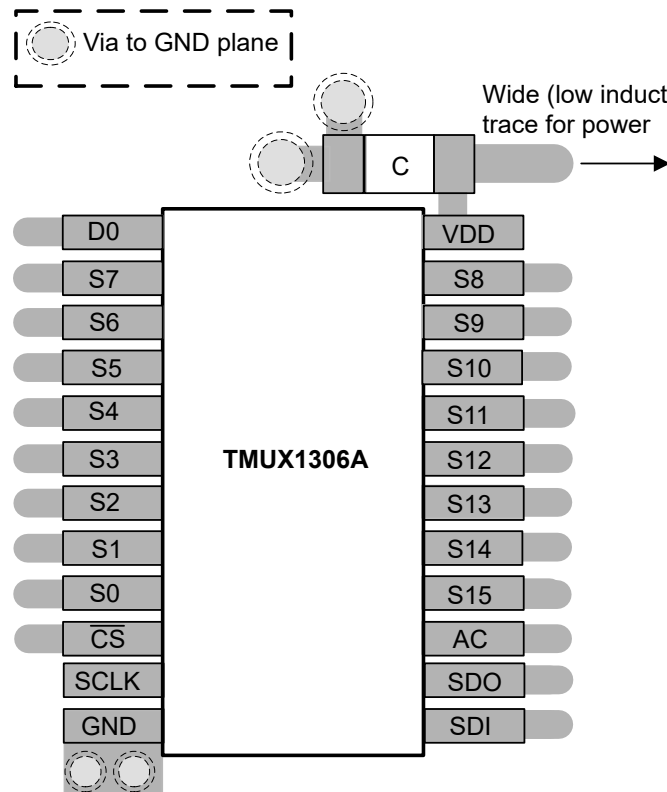


Figure 11-4. TMUXS1306A and TMUXS1307A Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [1.8V Logic for Multiplexers and Signal Switches](#) application brief
- Texas Instruments, [QFN/SON PCB Attachment](#) application note
- Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#) application note

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

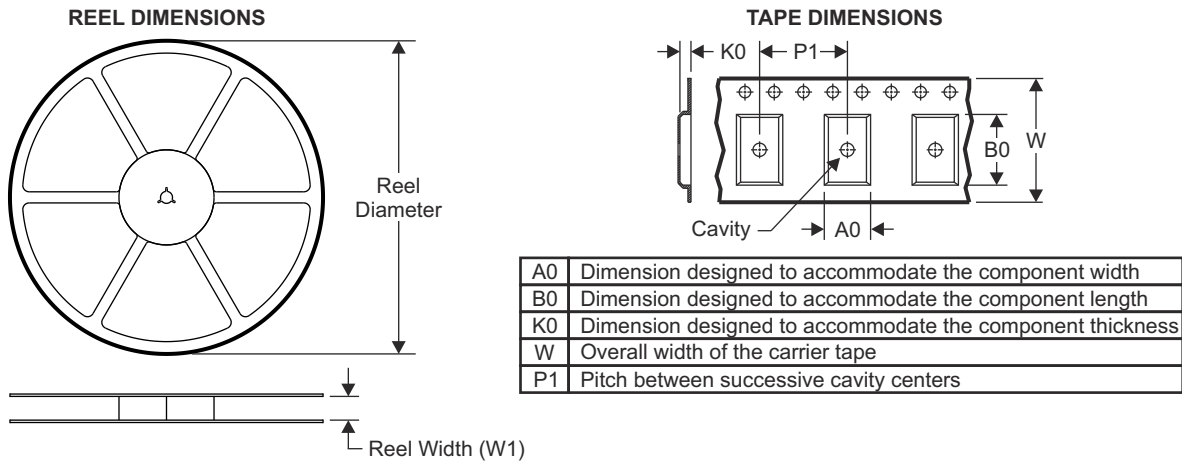
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

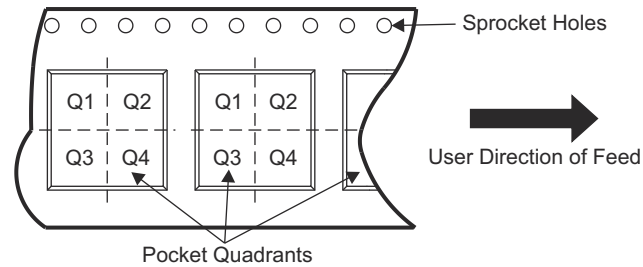
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Tape and Reel Information

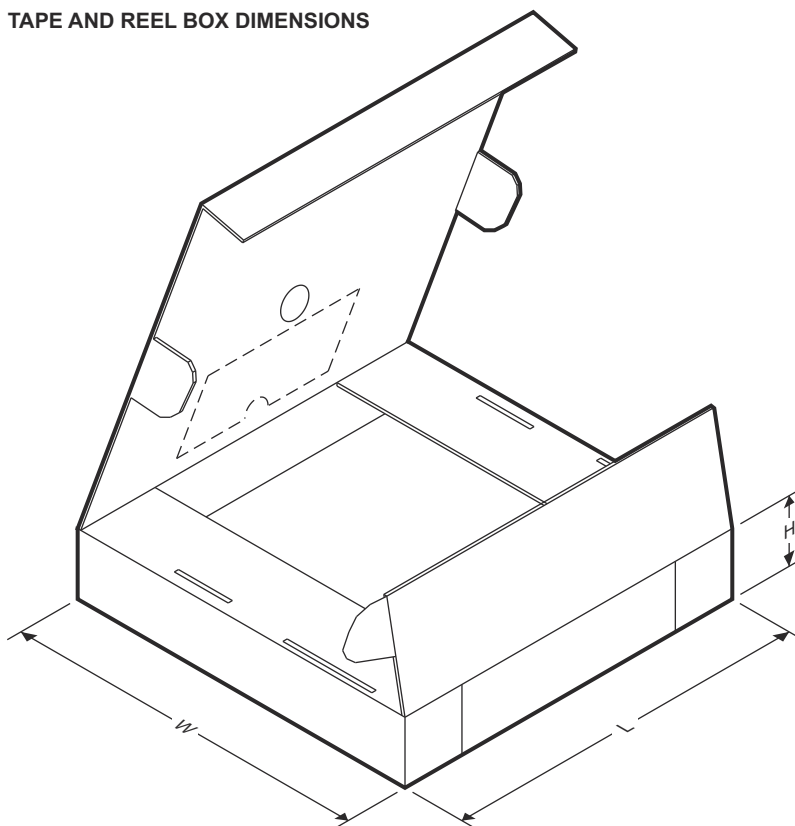


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXS1306A	RGE	RGE	24	3000	330	12.4	4.25	4.25	1.15	8	12	2
TMUXS1307A	RGE	RGE	24	3000	330	12.4	4.25	4.25	1.15	8	12	2

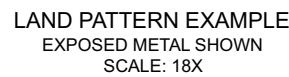
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXS1306A	VQFN	RGE	24	3000	346	346	33
TMUXS1307A	VQFN	RGE	24	3000	346	346	33

PLASTIC QUAD FLATPACK-NO LEAD

PLASTIC QUAD FLATPACK-NO LEAD



4224736/A 12/2018

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTMUXS1306ARGER	Active	Preproduction	VQFN (RGE) 24	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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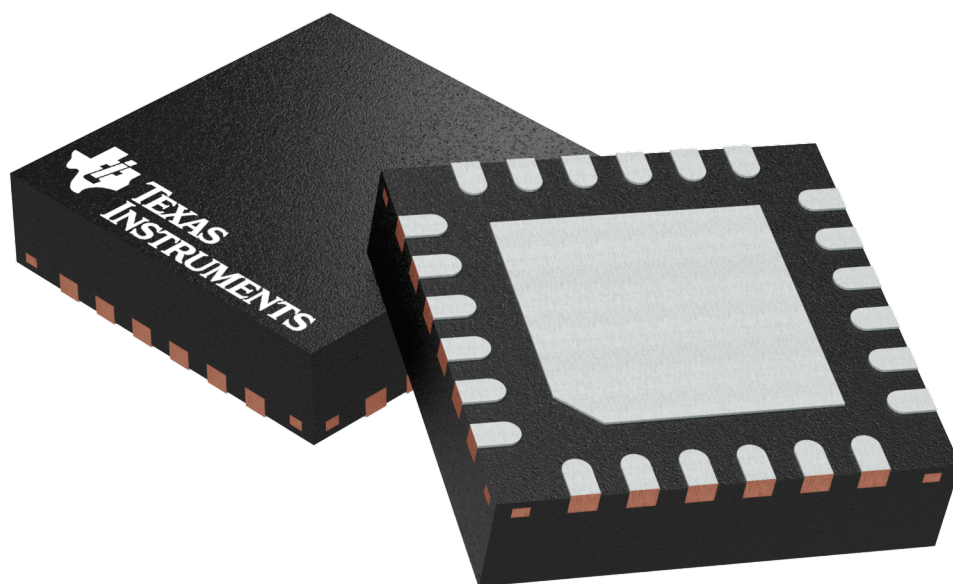
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGE 24

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

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