TMUXHS5212 32Gbps Two-Channel Differential 2:1 Mux or 1:2 Demux

1 Features

- Provides 2 differential-channels of bidirectional 2:1 mux or 1:2 demux
- Suitable for interfaces with datarates up to 32Gbps NRZ
  - Supports PCIe 5.0 (32 GT/s), USB 4.0, CXL 3.1, TBT 4, SATA 3, SAS-4, DSI/CSI, and Ethernet® applications
- −3dB differential BW of 18.5GHz typ
- Dynamic characteristics at 16GHz typ:
  - Insertion loss = −2.75dB
  - Return loss = −17dB
  - Crosstalk = −30dB
- Minimal skew:
  - Bit-to-Bit = 3ps typ
  - Channel-to-Channel = 10ps typ
- Supports common mode voltages from 0 to 1.2V
- Single supply voltage V_{CC} of 1.8V
- Adaptive common mode voltage tracking
- Low active (60µA typ) and standby current consumption (1µA typ)
- Temperature range of −40° to 105°C
- Available in 2.5mm × 2.5mm QFN package with 0.35mm pitch

2 Applications

- PC and notebooks
- Smartphone, tablets, and TV
- Gaming, home theater, and entertainment
- Data center and enterprise computing
- Test and measurements
- Factory automation and control
- Electronic point of sale (EPOS)
- Wireless infrastructure

3 Description

The TMUXHS5212 is a 2-channel bidirectional passive switch with 2:1 mux or 1:2 demux configurations. It supports differential signaling up to 32GBbps NRZ, thus enabling it for many applications including PCI Express 5.0, USB 4, 50G Ethernet, CXL 3.1 and Thunderbolt™ 4. The device operates off of a 1.8V supply with ultra low active and standby power, and its control pins are compatible with 1.8V digital inputs.

The dynamic characteristics of the TMUXHS5212 allow for high-speed switching with minimal attenuation and negligible added jitter to the eye diagram for both NRZ and PAM applications. It is designed for best intra-pair skew performance, low crosstalk, and reliable signal integrity.

The TMUXHS5212 is rated for a temperature range of -40°C to 105°C that can suit commercial, industrial and personal electronics applications.

Device Information

PART NUMBER	MAX TA	PACKAGE(1)	BODY SIZE (NOM)
TMUXHS5212	105°C	UQFN (24)	2.50mm × 2.50mm × 0.35mm pitch

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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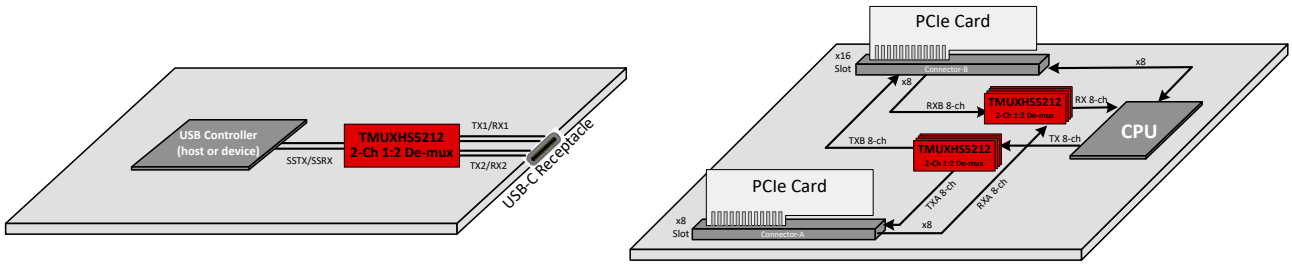

Application Use Cases

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4 Pin Configuration and Functions

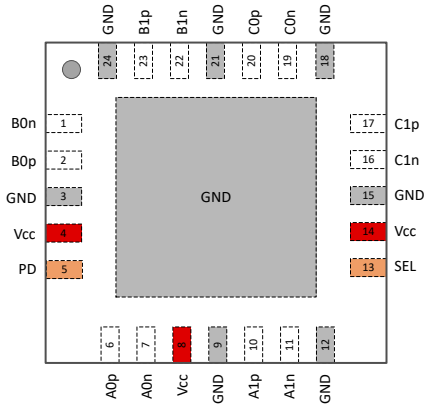

Figure 4-1. DTY Package, 24-Pin UQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A0n	7	I/O	Port A, channel 0, high-speed negative signal (connector side)
A0p	6	I/O	Port A, channel 0, high-speed positive signal (connector side)
A1n	11	I/O	Port A, channel 1, high-speed negative signal
A1p	10	I/O	Port A, channel 1, high-speed positive signal
B0n	1	I/O	Port B, channel 0, high-speed negative signal (connector side)
B0p	2	I/O	Port B, channel 0, high-speed positive signal (connector side)
B1n	22	I/O	Port B, channel 1, high-speed negative signal
B1p	23	I/O	Port B, channel 1, high-speed positive signal
C0n	19	I/O	Port C, channel 0, high-speed negative signal
C0p	20	I/O	Port C, channel 0, high-speed positive signal
C1n	16	I/O	Port C, channel 1, high-speed negative signal
C1p	17	I/O	Port C, channel 1, high-speed positive signal
GND	3, 9, 12, 15, 18, 21, 24	G	Ground
PD	5	I	Active-low chip enable. The pin can be connected to GND if always on functional behavior is desired. L: Normal operation, H: Shutdown.
SEL	13	I	Port select pin. L: Port A to Port B, H: Port A to Port C
V_{CC}	4, 8, 14	P	1.8V power

(1) I = input, O = output, G = ground, P = power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC-ABSMAX}$	Supply voltage	Supply voltage	–0.5	2.1	V
$V_{HS-ABSMAX}$	Voltage	Differential I/O	–0.5	1.4	V
$V_{CTR-ABSMAX}$	Voltage	Control pins	–0.5	2.1	V
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.65	1.8	1.98	V
V_{IH}	Input high voltage	SEL, PD pins	$0.75V_{CC}$			V
V_{IL}	Input low voltage	SEL, PD pins			$0.25V_{CC}$	V
V_{DIFF}	High-speed signal pins differential voltage	VDD=1.8V	0		1.2	V_{pp}
V_{CM}	High speed signal pins common mode voltage	High speed signal pins common mode voltage	0		1.2	V
T_A	Operating free-air/ambient temperature		–40		105	°C

5.4 Thermal Information

THERMAL METRIC(1)		TMUXHS5212 DTY (UQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	PD = 0; 0V ≤ V_{CM} ≤ 1.8; SEL = 0 or V_{CC}		60	90	µA
I_{STDN}	Device shutdown current	PD = V_{CC}		0.22	1	µA
C_{ON}	Output ON capacitance to GND	PD = 0, freq=10MHz		1.5		pF
C_{OFF}	Output OFF capacitance to GND	PD = 0, freq=10MHz		0.45		pF
R_{ON}	Output ON resistance	0V ≤ V_{CM} ≤ 1.2V; I_O = –8mA		9	15	Ω
ΔR_{ON}	On-resistance match between pairs for the same channel at same V_{CM}, V_{CC} and T_A	0V ≤ V_{CM} ≤ 1.2V; I_O = –8mA			0.25	Ω
R_{FLAT_ON}	On-resistance flatness R_{ON}(MAX) – R_{ON}(MIN) over V_{CM} range for the same channel at same V_{CC} and T_A	0V ≤ V_{CM} ≤ 1.2V; I_O = –8mA			0.75	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, PD)	V_{IN} = V_{CC}			100	nA
$I_{IL,CTRL}$	Input low current, control pins (SEL, PD)	V_{IN} = 0V			100	nA
$R_{CM,HS}$	Common mode resistance to ground on Ax pins	Each pin to GND		2.0		MΩ
$I_{IH,HS,SEL}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 1.8V for selected port - A and B with SEL = 0, and A and C with SEL = V_{CC}			8	µA
$I_{IH,HS,NSEL}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 1.8V for non-selected port - C with SEL = 0, and B with SEL = V_{CC} (1)			8	µA
$I_{IL,HS}$	Input low current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 0V			100	nA
$I_{HIZ,HS}$	Leakage current through turned off switch between Ax[p/n] to [B]x[p/n] and [C]x[p/n]	PD = VCC; Ax[p/n] = 1.8V, [B and C]x[p/n] = 0V and Ax[p/n] = 0V, [B and C]x[p/n] = 1.8V			10	µA
$R_{A,p2n}$	DC Impedance between p and n for Ax pins	PD = 0 and V_{CC}		50		KΩ

(1) There is a 20kΩ pull-down in non-selected port.

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5.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Pinout A						
I_L	Differential insertion loss	f=2.5GHz		-1		dB
		f=4.0GHz		-1.15		
		f=5.0GHz		-1.3		
		f=8.0GHz		-1.65		
		f=10.0GHz		-1.85		
		f=16.0GHz		-2.75		
BW	–3dB bandwidth			18.5		GHz
R_L	Differential return loss	f=2.5GHz		-20		dB
		f=4.0GHz		-20		
		f=5.0GHz		-16		
		f=8.0GHz		-15.5		
		f=10.0GHz		--17.66		
		f=16.0GHz		-17.2		
OIRR	Differential Off Isolation	f=2.5GHz		-28.5		dB
OIRR	Differential Off Isolation	f=4.0GHz		-25		dB
OIRR	Differential Off Isolation	f=5.0GHz		-23		dB
OIRR	Differential Off Isolation	f=8.0GHz		-19.5		dB
OIRR	Differential Off Isolation	f=10.0GHz		-17.5		dB
OIRR	Differential Off Isolation	f=16.0GHz		-13		dB
DDXT	Differential Crosstalk	f=2.5GHz		-42		dB
		f=4.0GHz		-38		
		f=5.0GHz		-37		
		f=8.0GHz		-35		
		f=10.0GHz		-33		
		f=16.0GHz		–30		

5.7 Switching Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		Test Conditions	MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	f = 1Ghz			50	ps
$t_{SW\_ON\_CM\_SHIFT}$	Switching time SEL-to-Switch ON	For different CMV			5	us
t_{SW_ON}	Switching time SEL-to-Switch ON	T>0ºC, For same CMV			100	ns
$t_{SW\_ON\_COLD}$	Switching time SEL-to-Switch ON	T<0ºC, For same CMV			1000	ns
$t_{SW\_OFF\_CM\_SHIFT}$	Switching time SEL-to-Switch OFF	For different CMV			1	us
t_{SW_OFF}	Switching time SEL-to-Switch OFF	For same CMV			100	ns
t_{SK_INTRA}	Intra-pair output skew between P and N pins for same channel	f = 1Ghz		3	8	ps
t_{SK_INTER}	Inter-pair output skew between channels	f = 1Ghz		10	20	ps

6 Detailed Description

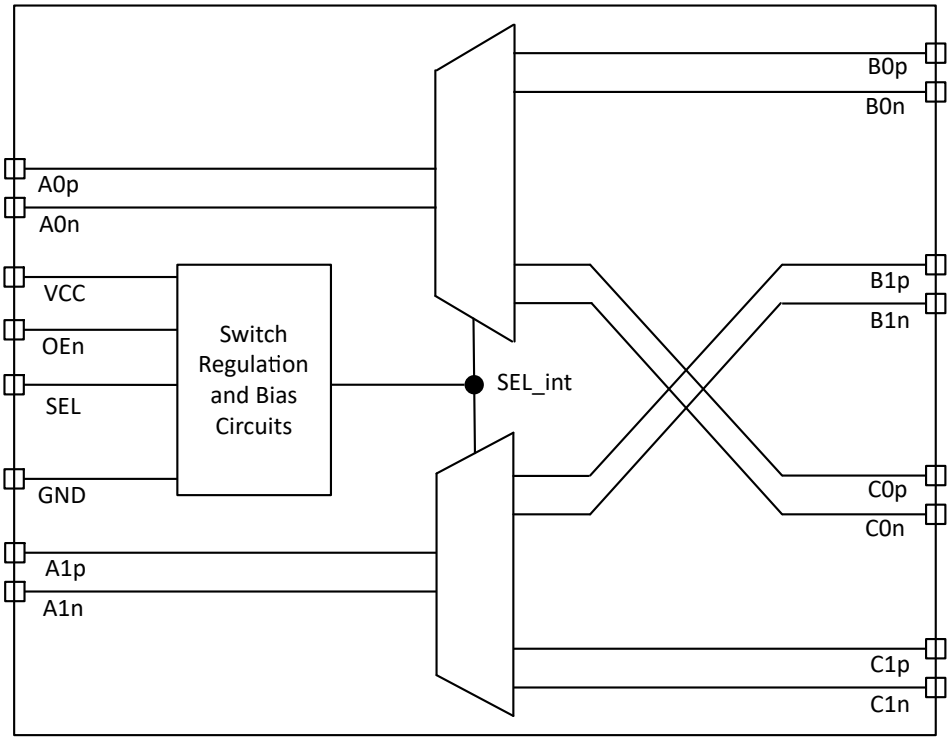
6.1 Overview

The TMUXHS5212 is a 2-channel generic analog passive 2:1 mux or 1:2 demux that can work for any high-speed differential interface up to 32GBaud. It is compatible with differential amplitudes of up to 1.2Vpp and common mode voltages (CMV) of up to 1.2V. By employing adaptive common mode voltage tracking, the TMUXHS5212 will ensure that the channel is unchanged for the CMV range, while also allowing the two channels of the device to carry different CMV levels. Additionally, two lanes can be used in such a manner where the device is switching between two different interface signals, with different data and electrical characteristics.

The dynamic characteristics of the TMUXHS5212 allow for high-speed switching with minimal attenuation to the signal eye diagram with very little added jitter. While the device is recommended for interfaces up to 32 GBd, the actual maximum data rate highly depends on the electrical channels. For low loss channels where adequate margin is maintained, the device can potentially be used for higher data rates.

The TMUXHS5212 is only recommended for differential signaling. However, certain low voltage single ended signaling (such as, Mipi DPHY LP signaling) can pass through the device. It is recommended to analyze the data line biasing of the device for such single ended use cases.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Enable and Power Savings

The TMUXHS5212 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes very-little current to achieve ultra low power in systems where power saving is critical. To enter standby mode, the PD control pin is pulled high through a resistor and must remain high. For active/normal operation, the PD control pin must be pulled low to GND or dynamically controlled to switch between H or L.

The TMUXHS5212 consumes 85µA when operational and has a shutdown mode exercisable by the PD pin resulting in 0.15µA.

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6.3.2 Data Line Biasing

The TMUXHS5212 has a weak pull-down of 1MΩ from A[0/1][p/n] pins to GND. While these resistors bias the device data channels to a common mode voltage (CMV) of 0V with very weak strength, it is recommended that the device is biased by a stronger impedance from either side of the device to a valid value in the range of 0 – 1.2V. To avoid double biasing, ensure that the appropriate AC coupling capacitors are on either side of the device.

In certain use cases, if both sides of the TMUXHS5212 are AC coupled, then it is recommended to use appropriate CMV biasing for the device. 10kΩ to GND or any other bias voltage in the CMV range for each A[0/1][p/n] pin will suffice for most use cases.

The high-speed data ports incorporate 20kΩ pull-down resistors that are switched in when a port is not selected and switched out when the port is selected. For example, when SEL = L, the C[0/1][p/n] pins have 20kΩ resistors to GND. The feature ensures that the unselected port is always biased to a known voltage for long term reliability of the device and the electrical channel.

The positive and negative terminals of data pins A[0/1] have a weak (20kΩ) differential resistor for device switch regulation operation. This does not impact signal integrity or functionality of high speed differential signaling that typically has much stronger differential impedance (such as 100Ω).

6.4 Device Functional Modes

Table 6-1. Port Select Control Logic

PORT A CHANNEL(1)	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL		PD Pin
	SEL = L	SEL = H	PD Pin
A0p	B0p	C0p	Low
A0n	B0n	C0n	Low
A1p	B1p	C1p	Low
A1n	B1n	C1n	Low
High-Z	High-Z	High-Z	High

(1) The TMUXHS5212 can tolerate polarity inversions for all differential signals on Ports A, B, and C. Ensure that the same polarity is maintained on Port A versus Ports B or C in such flexible implementation.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TMUXHS5212 is a 2-channel generic analog passive 2:1 mux or 1:2 demux that can be used for routing high-speed signals between two different locations on a circuit board. The TMUXHS5212 supports many high-speed data protocols, provided the signals' differential amplitude is within 1.2Vpp and common mode voltage (CMV) is from 0 to 1.2V. The TMUXHS5212 can be used for many high speed interfaces including the following:

- Universal Serial Bus (USB) 3.2 Gen 1 and Gen 2
- USB4 up to Gen 4
- USB Type-C
- Peripheral Component Interconnect Express (PCIe™) up to Gen 6.0
- Serial ATA (SATA/eSATA)
- Serial Attached SCSI (SAS)
- DisplayPort (DP) 2.1 (UHBR 20)
- Thunderbolt™ (TBT) 3
- Mipi Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- Low Voltage Differential Signalling (LVDS)
- Serdes Framer Interface (SFI)
- Ethernet Interfaces up to 50G

The device's mux or demux selection pin SEL can easily be controlled by an available GPIO pin of a controller or hard tied to a H or L voltage level as an application requires.

The TMUXHS5212 comes with adaptive voltage tracking that can support applications where the common mode is different between the RX and TX pair. The switch paths of the TMUXHS5212 have internal weak pull-down resistors of 1MΩ on the A port pins. While these resistors bias the device data channels to a CMV of 0V with weak strength, it is recommended that the device is biased from either side of the device to a valid value in the range of 0 – 1.2V. It is expected that the system/host controller and Device/End point common mode bias impedances are much stronger (smaller) than the TMUXHS5212 internal pull-down resistors; therefore, they are not impacted.

Many interfaces require AC coupling between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option to provide AC coupling. Avoid the 0603 and 0805 size capacitors and C-packs. When placing AC coupling capacitors, symmetric placement is best. The capacitor value must be chosen according to the specific interface the device is being used. The value of the capacitor should match for the positive and negative signal pair. For many interfaces (such as, USB 3.2 and PCIe) the designer should place them along the TX pairs on the system board, which are usually routed on the top layer of the board. Depending upon the application and interface specifications, use the appropriate value for AC coupling capacitors.

The AC coupling capacitors have several placement options. Typical use cases warrant that the capacitors are placed on one side of the TMUXHS5212. In certain use cases, if both sides of the TMUXHS5212 are AC coupled, then it is recommended to use appropriate CMV biasing for the device. 10kΩ to GND or any other bias voltage in the range of 0 – 1.2V for each A[0/1][p/n] pin will suffice for most use cases. Figure 7-1 shows a few placement options. Some interfaces such as USB SS and PCIe recommend AC coupling capacitors on the TX signals before it goes to a connector. Option (a) features TX AC coupling capacitors on the connector side of the TMUXHS5212. Option (b) illustrates the capacitors on the host of the TMUXHS5212. Option (c) showcases the TMUXHS5212 as AC coupled on both sides. The range for V_{BIAS} is within 0 – 1.2V.

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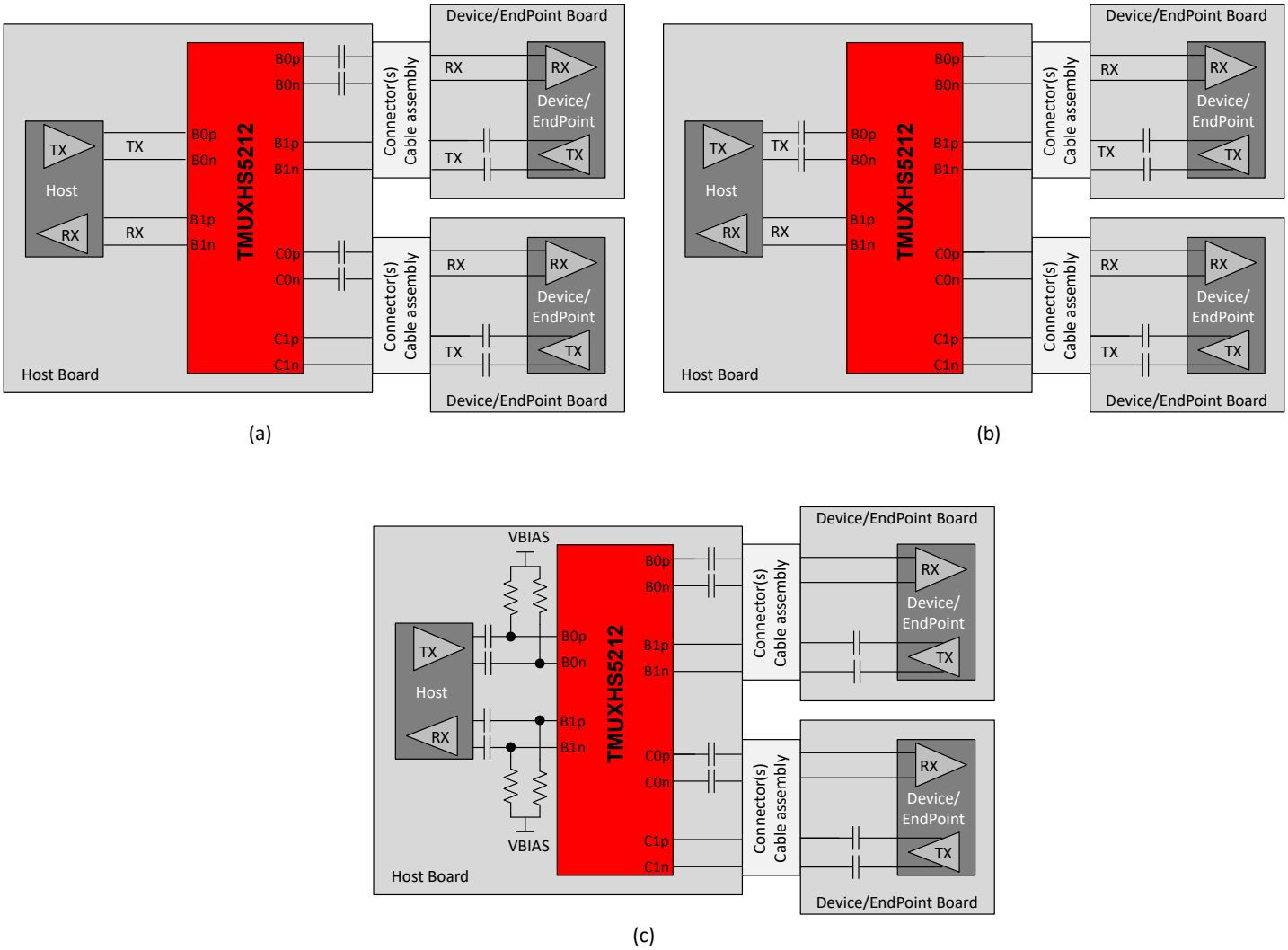

Figure 7-1. AC Coupling Capacitors Placement Options Between Host and Device/Endpoint Through TMUXHS5212

7.2 Typical Applications

7.2.1 USB 3.2/4 Implementation for USB Type-C

The TMUXHS5212 can be used in USB Type-C implementation to mux USB 3.2/4 signals (TX1 and RX1 pairs versus TX2 and RX2 pairs) to accommodate plug flips. In typical use cases, the mux selection is done by a USB Type-C Channel Configuration (CC) or Power Delivery (PD) controller. The device can used on a USB Type-C DFP, UFP, or DRP port. Figure 7-2 shows two USB Type-C connector applications with both a host and device side. The cable between the two connectors swivels the pairs to properly route the signals to the correct pin. The other applications are more generic because different connectors can be used.

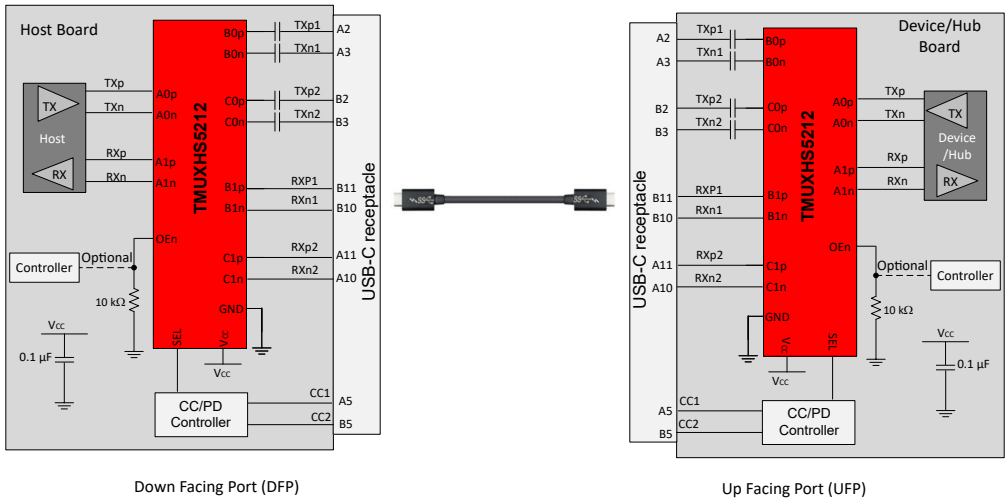

Figure 7-2. USB 3.2 Implementation for USB Type-C Connector

7.3 Systems Examples

7.3.1 USB4 / TBT 3.0 Demuxing

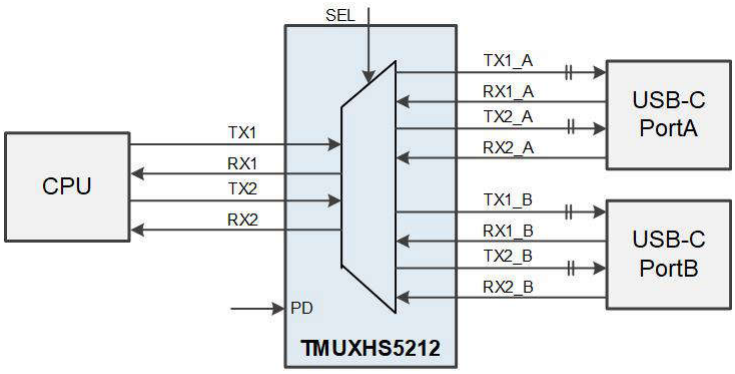

Figure 7-3. USB4 / TBT 3.0 Demuxing

7.3.2 DisplayPort Main Link Mux/Demux

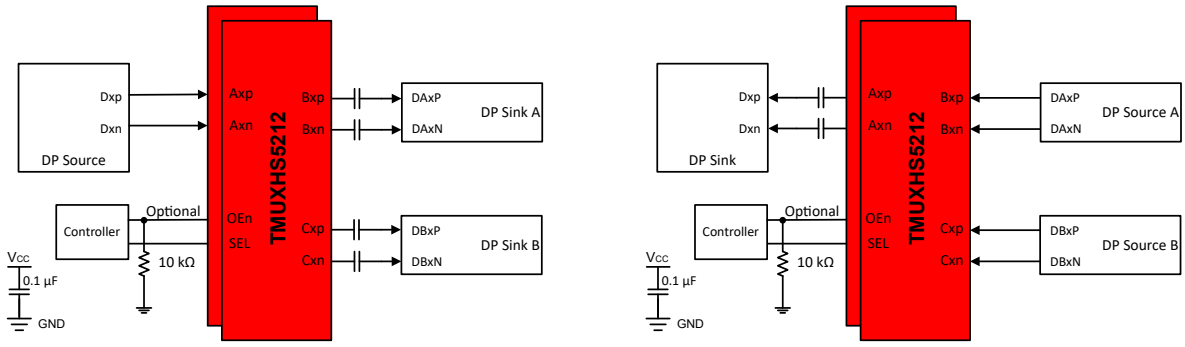

Figure 7-4. DP Main Link Mux/Demux for Dual Sink/Source

7.3.3 MIPI Camera Serial Interface

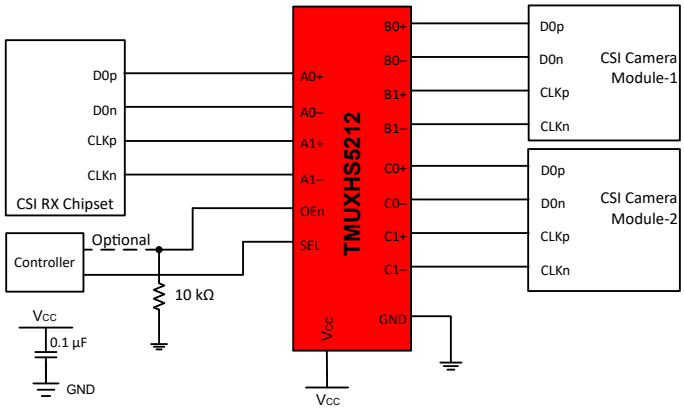

Figure 7-5. CSI Camera Selection

7.4 PCIe Lane Muxing

The TMUXHS5212 can be used to switch PCIe lanes between two slots. In many PC and server motherboards, the CPU does not have enough PCIe lanes to provide desired system flexibility for end customers. In such applications, the TMUXHS5212 can be used to switch PCIe TX and RX lanes between two slots. Figure 7-6 provides a schematic where eight TMUXHS5212 devices are used to switch eight PCIe TX and eight RX lanes. Note: the common mode voltage (CMV) bias for the TMUXHS5212 must be within the range of 0 – 1.2V. In implementations where receiver CMV bias of a PCIe root complex or an end point cannot be ensured within the CMV range, additional DC blocking capacitors and appropriate CMV biasing must be implemented.

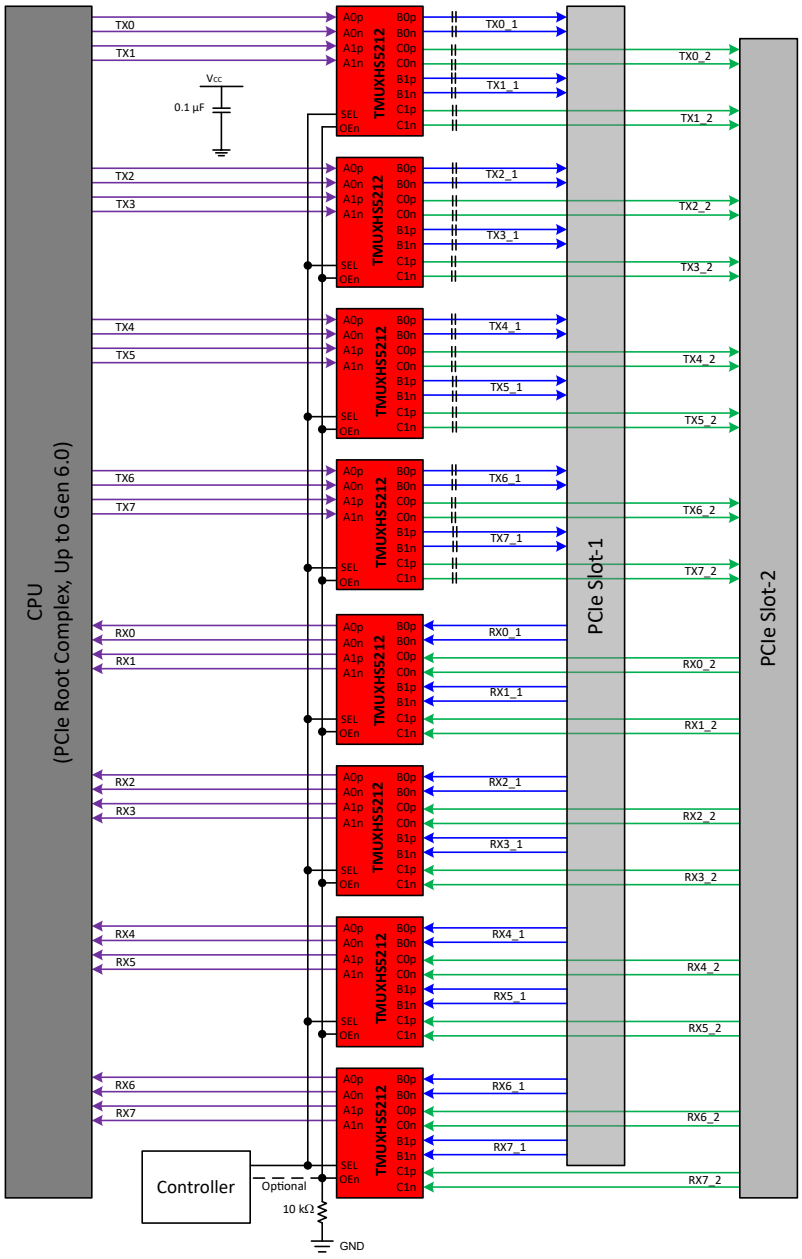

Figure 7-6. PCIe Lane Muxing

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7.4.1 Application Curves

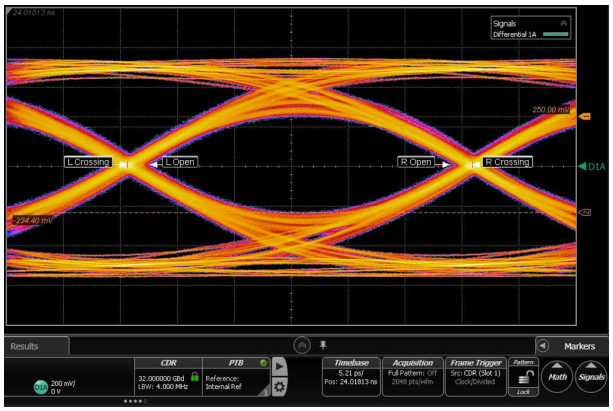

Figure 7-7. 32Gbps PRBS-7 Signals Through Calibration Traces in TI Evaluation Board

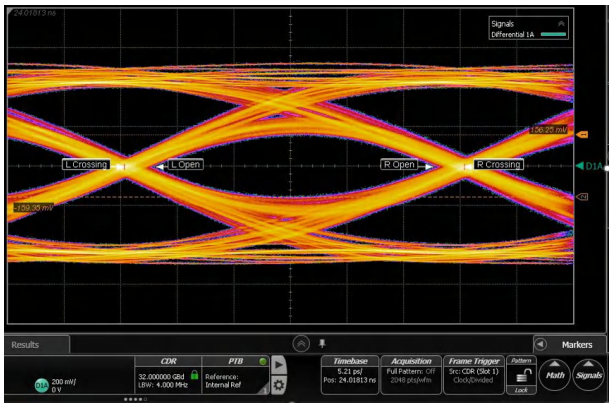

Figure 7-8. 32Gbps PRBS-7 Signals Through a Typical TMUXHS5212 Channel in TI Evaluation Board

7.5 Power Supply Recommendations

The TMUXHS5212 does not require a power supply sequence. TI, however, recommends that PD is asserted low after the device supply V_{CC} is stable and in specification. TI also recommends to place ample decoupling capacitors at the device V_{CC} near the pin.

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7.6 Layout

7.6.1 Layout Guidelines

On a high-K board, TI always recommends to solder the PowerPAD™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board, the TMUXHS5212 can operate over the full temperature range by soldering the PowerPAD onto the thermal land without vias.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs*.

The designer must use a 1oz Cu trace connecting the GND pins to the thermal land for the device to operate across the temperature range on a low-K board. A general PCB design guide for PowerPAD packages is provided in *Power-pad Thermally-Enhanced Package*.

7.6.2 Layout Example

Figure 7-9 shows a basic layout example for USB 3.2/4 Type-C MUX implementation.

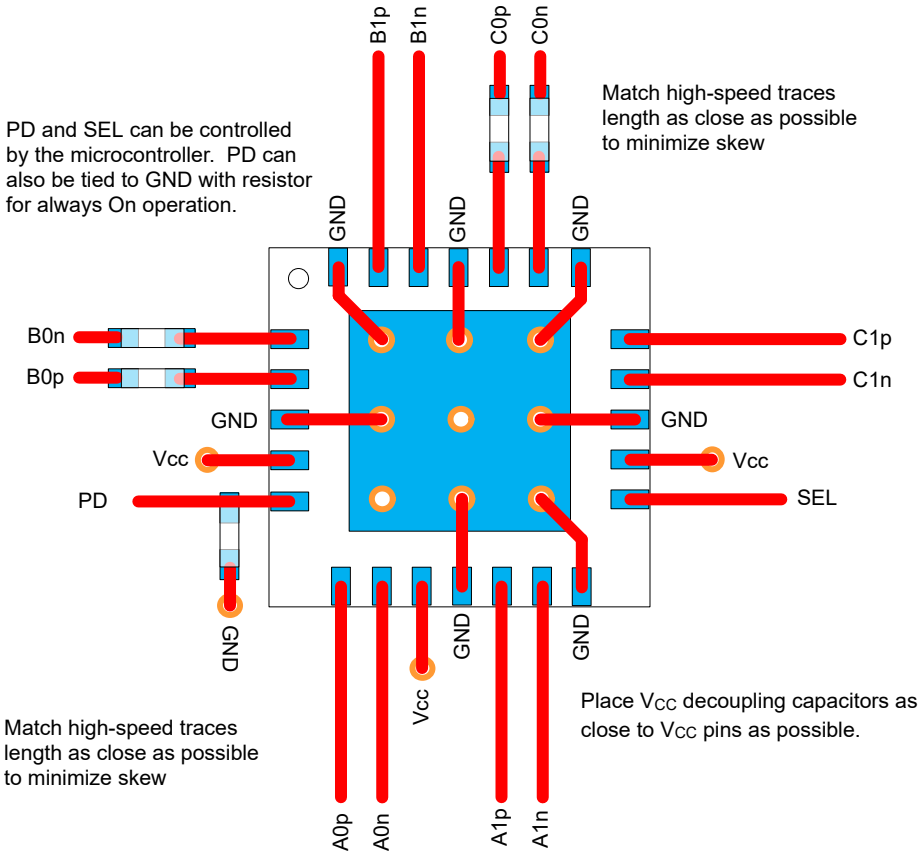

Figure 7-9. TMUXHS5212 Layout Example

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8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

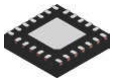
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

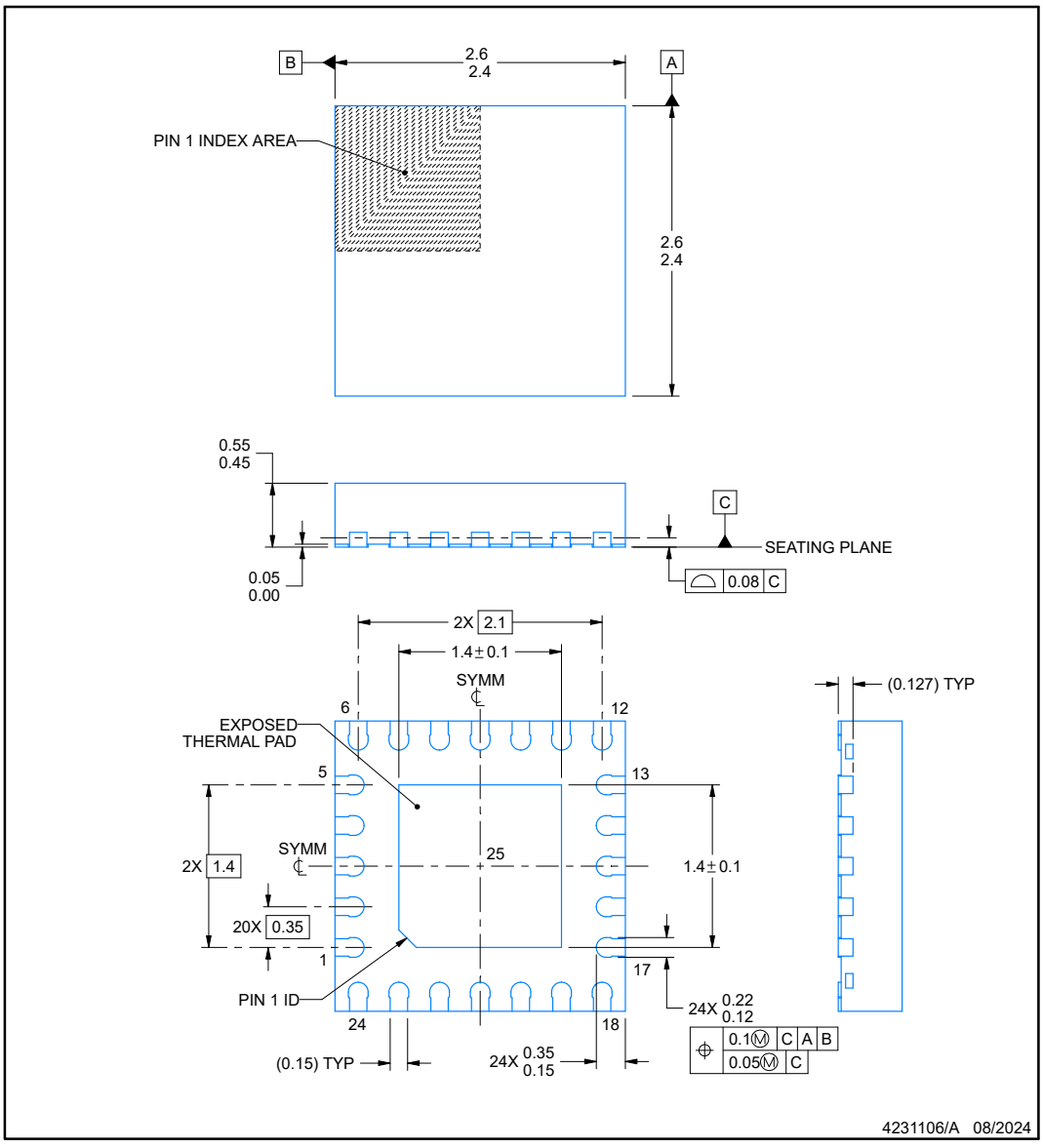
PACKAGE OUTLINE

DTY0024A



UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

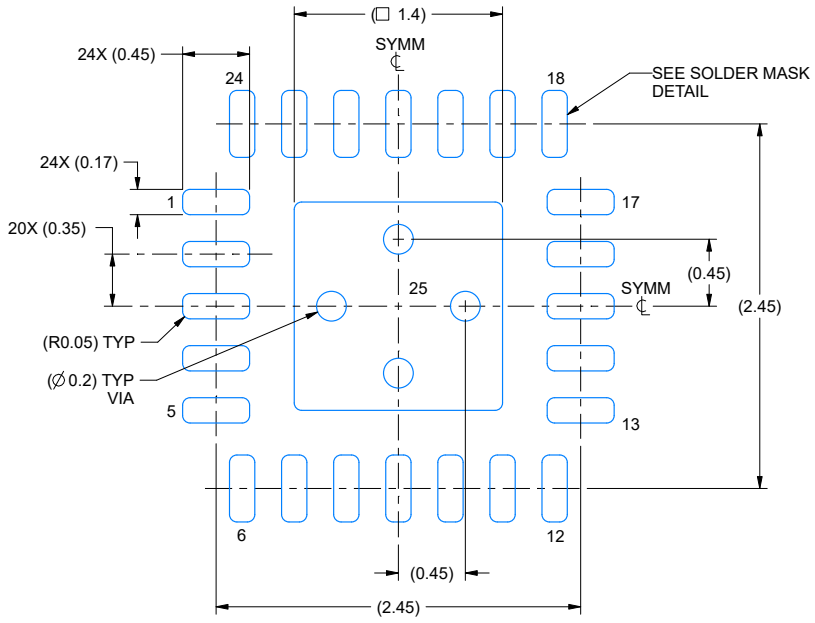
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

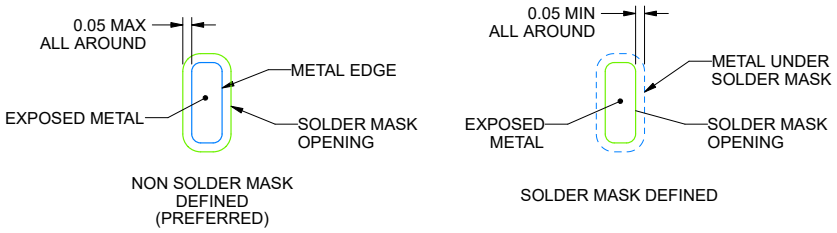
EXAMPLE BOARD LAYOUT

DTY0024A — **UQFN - 0.55 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

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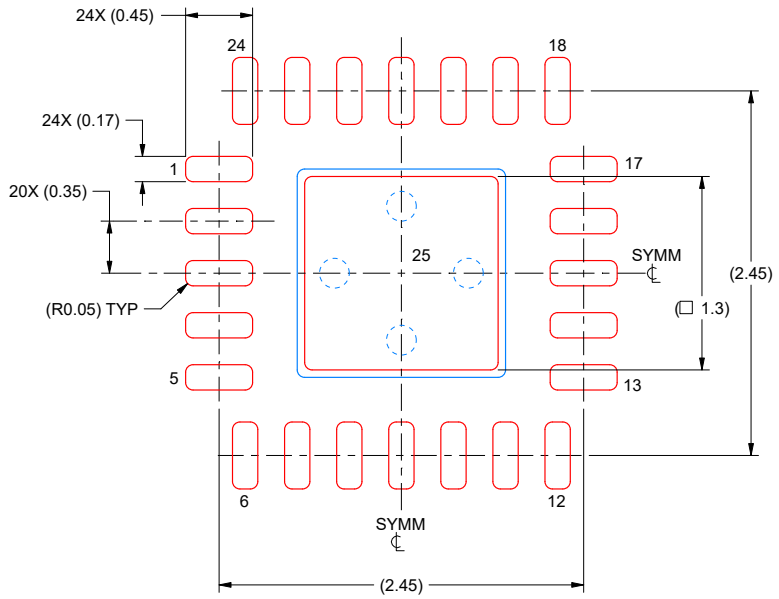
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DTY0024A — **UQFN - 0.55 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 25X

EXPOSED PAD 25
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTMUXHS5212DTYT	Active	Preproduction	null (null) |	250 | SMALL T&R	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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