

TMUX550x 40V, 130Ω, 8:1, 1-Channel, 4:1, 2-Channel Switches with 1.8V Logic

1 Features

- Low On-Capacitance
 - TMUX5508: 15.5pF
 - TMUX5509: 10.2pF
- Low I_{ON} typical Leakage: 5pA
- Low Charge Injection: 9pC
- Rail-to-Rail Operation
- Wide Supply Range: $\pm 5V$ to $\pm 20V$ dual rail, 4.5V to 40V single supply
- Low On-Resistance: 130Ω
- Break-Before-Make Switching
- Logic Levels: 1.8V
- ESD Protection HBM: 2000V
- Industry-Standard QFN, TSSOP and SOIC Packages

2 Applications

- Sample-and-hold circuits
- Feedback gain switching
- Semiconductor test equipment
- Professional Audio Equipment
- Factory Automation and Industrial Process Controls
- Programmable Logic Controllers (PLC)
- Analog Input Modules
- Digital Multimeters
- Data acquisition systems (DAQ)
- Instrumentation: lab, analytical, and portable
- Optical test equipment

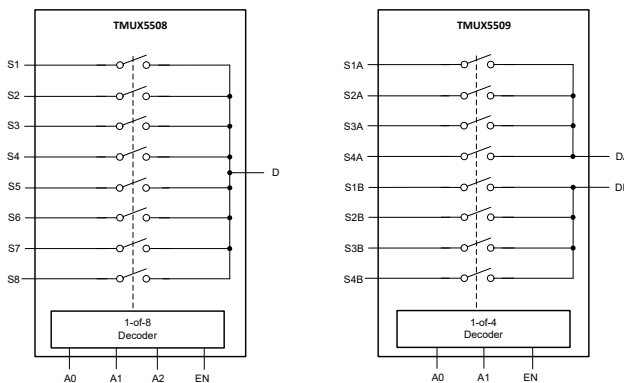
3 Description

The TMUX5508 and TMUX5509 (TMUX550x) are modern, complementary metal-oxide semiconductor (CMOS), analog multiplexers (muxes). The TMUX5508 offers 8:1 single-ended channels, and the TMUX5509 offers differential 4:1 or dual 4:1 single-ended channels. The TMUX5508 and TMUX5509 are designed to work with either dual supplies ($\pm 5V$ to $\pm 18V$) or a single supply (10V to 36V). They also perform with symmetric supplies (such as $V_{DD} = 12V$, $V_{SS} = -12V$), and unsymmetric supplies (such as $V_{DD} = 12V$, $V_{SS} = -5V$). The TMUX550x supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from VSS to VDD.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TMUX550x	RSV - QFN (16)	2.6mm × 1.8mm
	PW - TSSOP (16)	5.00mm × 4.40mm
	D - SOIC (16)	9.90mm × 3.91mm

(1) For all available packages, see [Section 12](#).



TMUX550x Block Diagram



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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX5508	8-channel, single-ended analog multiplexer (8:1 mux)
TMUX5509	4-channel differential or dual 4:1 single-ended analog multiplexer (8:2 mux)

5 Pin Configuration and Functions

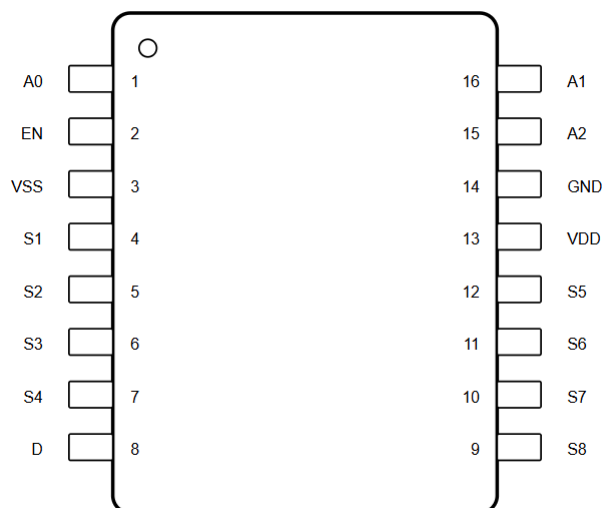


Figure 5-1. TMUX5508 PW-TSSOP and D-SOIC Pin Diagram

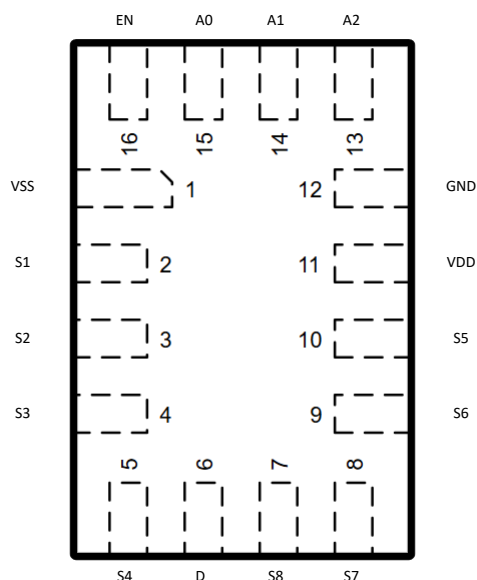


Figure 5-2. TMUX5508 RSV-QFN Pin Diagram

Table 5-1. Pin Functions: TMUX5508

PIN			TYPE	DESCRIPTION
NAME	RSV NO.	PW/SOIC NO.		
A0	15	1	Digital input	Address line 0
A1	14	16	Digital input	Address line 1
A2	13	15	Digital input	Address line 2
D	6	8	Analog input or output	Drain pin. Can be an input or output.
EN	16	2	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] logic inputs determine which switch is turned on.
GND	12	14	Power supply	Ground (0V) reference
S1	2	4	Analog input or output	Source pin 1. Can be an input or output.
S2	3	5	Analog input or output	Source pin 2. Can be an input or output.
S3	4	6	Analog input or output	Source pin 3. Can be an input or output.
S4	5	7	Analog input or output	Source pin 4. Can be an input or output.
S5		12	Analog input or output	Source pin 5. Can be an input or output.
S6	9	11	Analog input or output	Source pin 6. Can be an input or output.
S7	8	10	Analog input or output	Source pin 7. Can be an input or output.
S8	7	9	Analog input or output	Source pin 8. Can be an input or output.
VDD	11	13	Power supply	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between VDD and GND.
VSS	1	3	Power supply	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between VSS and GND.

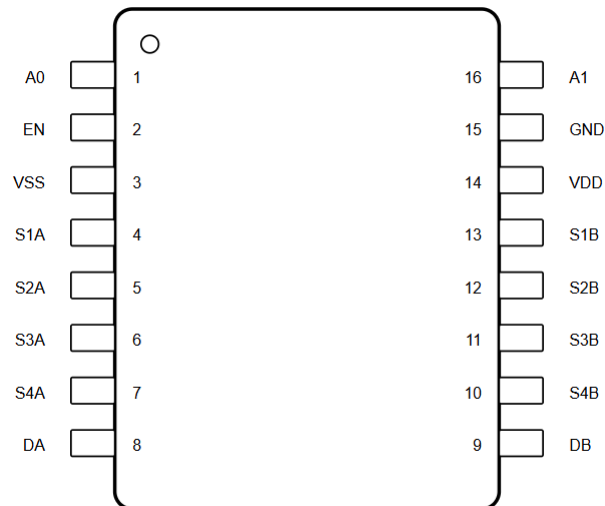


Figure 5-3. TMUX5509 PW-TSSOP and D-SOIC Pin Diagram

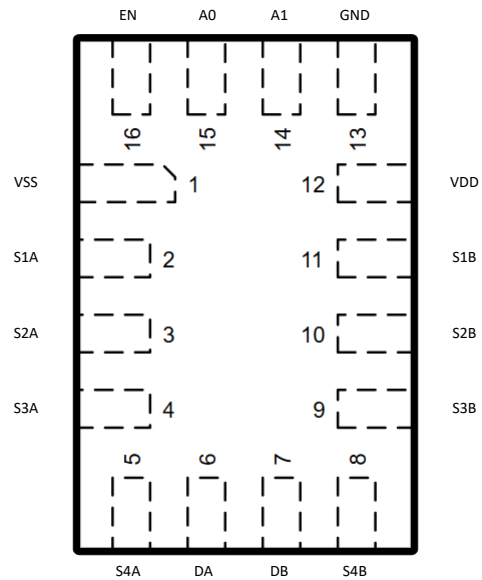


Figure 5-4. TMUX5509 RSV-QFN Pin Diagram

Table 5-2. Pin Functions: TMUX5509

PIN			TYPE	DESCRIPTION
NAME	RSV NO.	PW/SOIC NO.		
A0	15	1	Digital input	Address line 0
A1	14	16	Digital input	Address line 1
DA	6	8	Analog input or output	Drain pin A. Can be an input or output.
DB	7	9	Analog input or output	Drain pin B. Can be an input or output.
EN	16	2	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[1:0] logic inputs determine which pair of switches is turned on.
GND	13	15	Power supply	Ground (0V) reference
S1A	2	4	Analog input or output	Source pin 1A. Can be an input or output.
S2A	3	5	Analog input or output	Source pin 2A. Can be an input or output.
S3A	4	6	Analog input or output	Source pin 3A. Can be an input or output.
S4A	5	7	Analog input or output	Source pin 4A. Can be an input or output.
S1B	11	13	Analog input or output	Source pin 1B. Can be an input or output.
S2B	10	12	Analog input or output	Source pin 2B. Can be an input or output.
S3B	9	11	Analog input or output	Source pin 3B. Can be an input or output.
S4B	8	10	Analog input or output	Source pin 4B. Can be an input or output.
VDD	12	14	Power supply	Positive power supply. This pin is the most positive power supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between VDD and GND.
VSS	1	3	Power supply	Negative power supply. This pin is the most negative power supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between VSS and GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		44	V
V_{DD}		-0.5	44	V
V_{SS}		-44	0.5	V
$V_{SEL} - V_{SS}$	Logic Supply Voltage	-0.5	44	V
I_{SEL}	Logic control input pin current (SEL pins)	-30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	$V_{SS}-0.5$	$V_{DD}+0.5$	V
I_{IK}	Diode clamp current ⁽³⁾	-30	30	mA
I_S or I_D (CONT)	Source or drain current (Sx, Dx)	-20	20	mA
I_{peak}	Source or drain pulse current (Sx, Dx: pulsed at 1ms, 10% duty cycle max)	-45	45	mA
T_A	Ambient temperature	-55	150	°C
T_{stg}	Storage temperature	-65	150	°C
T_J	Junction temperature		150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}^{(1)}$	Power supply voltage differential	4.5		40	V
V_{DD}	Positive power supply voltage	4.5		40	V
V_{SS}	Negative power supply voltage (dual)	-40		0	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
$V_{SEL} - V_{SS}$	Logic Supply Voltage	0		40	V
I_S or I_D (CONT)	Source or drain continuous current (Sx, D)	-15		15	mA
V_{IH}	Logic Input High	1.3		40	
V_{IL}	Logic Input Low	0		0.8	
T_A	Ambient temperature	-40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as $4.5V \leq (V_{DD} - V_{SS}) \leq 40V$, and the minimum V_{DD} is met.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX550x			UNIT
		D (SOIC)	RSV (QFN)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.0	42.8	95.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.4	27.9	33.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	17.9	52.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.7	0.3	2.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.1	17.9	52.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	3.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.5 Electrical Characteristics (±15V Dual Supply)

$V_{DD} = +15V \pm 10\%$, $V_{SS} = -15V \pm 10\%$ GND = 0V (unless otherwise noted). Typical at $V_{DD} = +15V$, $V_{SS} = -15V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = V _{SS} +5V to V _{DD} -5V I _D = −1mA	25°C		130	150	Ω
			−40°C to +85°C			185	
			−40°C to +125°C			220	
ΔR _{ON}	On-resistance mismatch between channels	V _{DD} = 15V V _{SS} = -15V V _S = V _{SS} +5V to V _{DD} -5V I _D = −1mA	25°C		1.3	4	Ω
			−40°C to +85°C			4.8	
			−40°C to +125°C			5	
R _{ON FLAT}	On-resistance flatness	V _{DD} = 15V V _{SS} = -15V V _S = V _{SS} +5V to V _{DD} -5V I _D = −1mA	25°C		0.01	0.8	Ω
			−40°C to +85°C			0.9	
			−40°C to +125°C			1.2	
I _{S(OFF)}	TMUX5508 Source off leakage current ⁽¹⁾	V _{DD} = 16.5V, V _{SS} = −16.5V Switch state is off V _S = +10V / −10V V _D = −10V / + 10V	25°C		0.005		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{S(OFF)}	TMUX5509 Source off leakage current ⁽¹⁾	V _{DD} = 16.5V, V _{SS} = −16.5V Switch state is off V _S = +10V / −10V V _D = −10V / + 10V	25°C		0.005		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
I _{D(OFF)}	TMUX5508 Drain off leakage current ⁽¹⁾	V _{DD} = 16.5V, V _{SS} = −16.5V Switch state is off V _S = +10V / −10V V _D = −10V / + 10V	25°C		0.01		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{D(OFF)}	TMUX5509 Drain off leakage current ⁽¹⁾	V _{DD} = 16.5V, V _{SS} = −16.5V Switch state is off V _S = +10V / −10V V _D = −10V / + 10V	25°C		0.005		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
I _{S(ON)} I _{D(ON)}	TMUX5508 Channel on leakage current ⁽²⁾	V _{DD} = 16.5V, V _{SS} = −16.5V Switch state is on V _S = V _D = ±10V	25°C		0.01		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{S(ON)} I _{D(ON)}	TMUX5509 Channel on leakage current ⁽²⁾	V _{DD} = 16.5V, V _{SS} = −16.5V Switch state is on V _S = V _D = ±10V	25°C		0.005		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
POWER SUPPLY							
I _{DDQ}	V _{DD} quiescent supply current	V _{DD} = 16.5V, V _{SS} = −16.5V All switches OFF	25°C		35	60	μA
			−40°C to +85°C			65	
			−40°C to +125°C			70	
I _{DD}	V _{DD} supply current	V _{DD} = 16.5V, V _{SS} = −16.5V All switches ON	25°C		55	75	μA
			−40°C to +85°C			80	
			−40°C to +125°C			85	
I _{SSQ}	V _{SS} quiescent supply current	V _{DD} = 16.5V, V _{SS} = −16.5V All switches OFF	25°C		15	30	μA
			−40°C to +85°C			35	
			−40°C to +125°C			40	
I _{SS}	V _{SS} supply current	V _{DD} = 16.5V, V _{SS} = −16.5V All switches ON	25°C		20	40	μA
			−40°C to +85°C			45	
			−40°C to +125°C			50	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.6 Switching Characteristics ($\pm 15V$ Dual Supply)

$V_{DD} = +15V \pm 10\%$, $V_{SS} = -15V \pm 10\%$, GND = 0V (unless otherwise noted). Typical at $V_{DD} = +15V$, $V_{SS} = -15V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{tran}	Transition Time	$V_{Sx} = +10V/-10V$, $V_{Sx+1} = -10V/+10V$, $R_L = 1M\Omega$, $C_L = 35pF$	$25^\circ C$		190	230	ns
			$-40^\circ C$ to $+85^\circ C$			250	ns
			$-40^\circ C$ to $+125^\circ C$			260	ns
t_{ON}	Turn-on time from control input	$V_S = 5V$, $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		250	270	ns
			$-40^\circ C$ to $+85^\circ C$			295	ns
			$-40^\circ C$ to $+125^\circ C$			310	ns
t_{OFF}	Turn-off time from control input	$V_S = 5V$, $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		125	205	ns
			$-40^\circ C$ to $+85^\circ C$			210	ns
			$-40^\circ C$ to $+125^\circ C$			215	ns
t_{BBM}	Break-before-make time delay	$V_{Sx} = 5V$, $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		140		ns
			$-40^\circ C$ to $+85^\circ C$	80			ns
			$-40^\circ C$ to $+125^\circ C$	80			ns
Q_{INJ}	Charge injection	$V_S = 0V$, $C_L = 100pF$	$25^\circ C$		5.5		pC
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{\text{RMS}}$, $V_{\text{BIAS}} = 0V$, $f = 100kHz$	$25^\circ C$		-105		dB
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{\text{RMS}}$, $V_{\text{BIAS}} = 0V$, $f = 1MHz$	$25^\circ C$		-100		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{\text{RMS}}$, $V_{\text{BIAS}} = 0V$, $f = 100kHz$	$25^\circ C$		-95		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{\text{RMS}}$, $V_{\text{BIAS}} = 0V$, $f = 1MHz$	$25^\circ C$		-100		dB
BW	-3dB Bandwidth TMUX5508	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{\text{RMS}}$, $V_{\text{BIAS}} = 0V$	$25^\circ C$		250		MHz
BW	-3dB Bandwidth TMUX5509	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{\text{RMS}}$, $V_{\text{BIAS}} = 0V$	$25^\circ C$		415		MHz
I_L	Insertion loss	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{\text{RMS}}$, $V_{\text{BIAS}} = 0V$, $f = 1MHz$	$25^\circ C$		-7.1		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62V$ on V_{DD} and V_{SS} $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$	$25^\circ C$		-68		dB
$C_{S(\text{OFF})}$	TMUX5508Source off capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		2.3		pF
	TMUX5509Source off capacitance to ground				1.6		
$C_{D(\text{OFF})}$	TMUX5508Drain off capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		9.3		
	TMUX5509Drain off capacitance to ground				4.8		
$C_{S(\text{ON})}$, $C_{D(\text{ON})}$	TMUX5508On capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		12.5		
	TMUX5509On capacitance to ground				8.5		

6.7 Electrical Characteristics (±20V Dual Supply)

$V_{DD} = +20V$, $V_{SS} = -20V$, $GND = 0V$ (unless otherwise noted). Typical at $V_{DD} = +20V$, $V_{SS} = -20V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = V _{SS} +5V to V _{DD} -5V I _D = −1mA	25°C		130	165	Ω
			−40°C to +85°C			185	
			−40°C to +125°C			220	
ΔR _{ON}	On-resistance mismatch between channels	V _{DD} = 20V V _{SS} = -20V V _S = V _{SS} +5V to V _{DD} -5V I _D = −1mA	25°C		2.5	4	Ω
			−40°C to +85°C			5.5	
			−40°C to +125°C			12.5	
R _{ON FLAT}	On-resistance flatness	V _{DD} = 20V V _{SS} = -20V V _S = V _{SS} +5V to V _{DD} -5V I _D = −1mA	25°C		0.45	1.2	Ω
			−40°C to +85°C			7	
			−40°C to +125°C			45	
I _{S(OFF)}	TMUX5508 Source off leakage current ⁽¹⁾	V _{DD} = 20V, V _{SS} = −20V Switch state is off V _S = +15V / −15V V _D = −15V / + 15V	25°C		0.002		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{S(OFF)}	TMUX5509 Source off leakage current ⁽¹⁾	V _{DD} = 20V, V _{SS} = −20V Switch state is off V _S = +15V / −15V V _D = −15V / + 15V	25°C		0.005		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
I _{D(OFF)}	TMUX5508 Drain off leakage current ⁽¹⁾	V _{DD} = 20V, V _{SS} = −20V Switch state is off V _S = +15V / −15V V _D = −15V / + 15V	25°C		0.01		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{D(OFF)}	TMUX5509 Drain off leakage current ⁽¹⁾	V _{DD} = 20V, V _{SS} = −20V Switch state is off V _S = +15V / −15V V _D = −15V / + 15V	25°C		0.02		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
I _{S(ON)} I _{D(ON)}	TMUX5508 Channel on leakage current ⁽²⁾	V _{DD} = 20V, V _{SS} = −20V Switch state is on V _S = V _D = ±15V	25°C		0.01		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{S(ON)} I _{D(ON)}	TMUX5509 Channel on leakage current ⁽²⁾	V _{DD} = 20V, V _{SS} = −20V Switch state is on V _S = V _D = ±15V	25°C		0.01		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
POWER SUPPLY							
I _{DDQ}	V _{DD} quiescent supply current	V _{DD} = 20V, V _{SS} = −20V All switches OFF	25°C		50	65	μA
			−40°C to +85°C			70	
			−40°C to +125°C			75	
I _{DD}	V _{DD} supply current	V _{DD} = 20V, V _{SS} = −20V All switches ON	25°C		60	80	μA
			−40°C to +85°C			85	
			−40°C to +125°C			90	
I _{SSQ}	V _{SS} quiescent supply current	V _{DD} = 20V, V _{SS} = −20V All switches OFF	25°C		25	35	μA
			−40°C to +85°C			40	
			−40°C to +125°C			45	
I _{SS}	V _{SS} supply current	V _{DD} = 20V, V _{SS} = −20V All switches ON	25°C		30	40	μA
			−40°C to +85°C			45	
			−40°C to +125°C			50	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.8 Switching Characteristics ($\pm 20V$ Dual Supply)

$V_{DD} = +20V$, $V_{SS} = -20V$, $GND = 0V$ (unless otherwise noted). Typical at $V_{DD} = +20V$, $V_{SS} = -20V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{tran}	Transition Time	$V_{Sx} = +20V/-20V$, $V_{Sx+1} = -20V/+20V$, $R_L = 1M\Omega$, $C_L = 35pF$	$25^\circ C$		235	280	ns
			$-40^\circ C$ to $+85^\circ C$			300	
			$-40^\circ C$ to $+125^\circ C$			310	
t_{ON}	Turn-on time from control input	$V_S = 10V$, $R_L = 300\Omega$, $C_L = 35pF$	$25^\circ C$		285	320	ns
			$-40^\circ C$ to $+85^\circ C$			350	ns
			$-40^\circ C$ to $+125^\circ C$			380	ns
t_{OFF}	Turn-off time from control input	$V_S = 10V$, $R_L = 300\Omega$, $C_L = 35pF$	$25^\circ C$		165	215	ns
			$-40^\circ C$ to $+85^\circ C$			220	ns
			$-40^\circ C$ to $+125^\circ C$			225	μs
t_{BBM}	Break-before-make time delay	$V_S = 10V$, $R_L = 300\Omega$, $C_L = 35pF$	$25^\circ C$		185		ns
			$-40^\circ C$ to $+85^\circ C$	90			ns
			$-40^\circ C$ to $+125^\circ C$	90			ns
Q_{INJ}	Charge injection	$V_S = 0V$, $C_L = 100pF$	$25^\circ C$		6		pC
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 0V$, $f = 100kHz$	$25^\circ C$		-95		dB
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 0V$, $f = 1MHz$	$25^\circ C$		-90		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 0V$, $f = 100kHz$	$25^\circ C$		-95		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 0V$, $f = 1MHz$	$25^\circ C$		-95		dB
BW	-3dB Bandwidth TMUX5508	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 0V$,	$25^\circ C$		300		MHz
BW	-3dB Bandwidth TMUX5509	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 0V$,	$25^\circ C$		425		MHz
I_L	Insertion loss	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 0V$, $f = 1MHz$	$25^\circ C$		-7.1		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62V$ on V_{DD} and V_{SS} $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$	$25^\circ C$		-70		dB
$C_{S(OFF)}$	TMUX5508Source off capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		2.3		pF
	TMUX5509Source off capacitance to ground				1.6		
$C_{D(OFF)}$	TMUX5508Drain off capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		8.9		pF
	TMUX5509Drain off capacitance to ground				4.5		
$C_{S(ON)}$, $C_{D(ON)}$	TMUX5508On capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		12		pF
	TMUX5509On capacitance to ground				8.1		

6.9 Electrical Characteristics (12V Single Supply)

$V_{DD} = +12V \pm 10\%$, $V_{SS} = 0V$, GND = 0V (unless otherwise noted)

Typical at $V_{DD} = +12V$, $V_{SS} = 0V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = V _{SS} +3V to V _{DD} -3V I _D = −1mA	25°C		140	190	Ω
			−40°C to +85°C			215	
			−40°C to +125°C			250	
ΔR _{ON}	On-resistance mismatch between channels	V _{DD} = 12V V _S = V _{SS} +3V to V _{DD} -3V I _D = −1mA	25°C		2	6	Ω
			−40°C to +85°C			8	
			−40°C to +125°C			9	
R _{ON FLAT}	On-resistance flatness	V _{DD} = 12V V _S = V _{SS} +3V to V _{DD} -3V I _D = −1mA	25°C		30	40	Ω
			−40°C to +85°C			45	
			−40°C to +125°C			50	
I _{S(OFF)}	TMUX5508 Source off leakage current ⁽¹⁾	V _{DD} = 12V, V _{SS} = 0V Switch state is off V _S = 1V / 10V V _D = 10V / 1V	25°C		0.003		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{S(OFF)}	TMUX5509 Source off leakage current ⁽¹⁾	V _{DD} = 12V, V _{SS} = 0V Switch state is off V _S = 1V / 10V V _D = 10V / 1V	25°C		0.004		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
I _{D(OFF)}	TMUX5508 Drain off leakage current ⁽¹⁾	V _{DD} = 12V, V _{SS} = 0V Switch state is off V _S = 1V / 10V V _D = 10V / 1V	25°C		0.002		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{D(OFF)}	TMUX5509 Drain off leakage current ⁽¹⁾	V _{DD} = 12V, V _{SS} = 0V Switch state is off V _S = 1V / 10V V _D = 10V / 1V	25°C		0.003		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
I _{S(ON)} I _{D(ON)}	TMUX5508 Channel on leakage current ⁽²⁾	V _{DD} = 12V, V _{SS} = 0V Switch state is on V _S = V _D = 1V or 10V	25°C		0.003		nA
			−40°C to +85°C	−100		100	
			−40°C to +125°C	−100		100	
I _{S(ON)} I _{D(ON)}	TMUX5509 Channel on leakage current ⁽²⁾	V _{DD} = 12V, V _{SS} = 0V Switch state is on V _S = V _D = 1V or 10V	25°C		0.002		nA
			−40°C to +85°C	−50		50	
			−40°C to +125°C	−50		50	
POWER SUPPLY							
I _{DDQ}	V _{DD} quiescent supply current	V _{DD} = 12V, V _{SS} = 0V All switches OFF	25°C		45	55	μA
			−40°C to +85°C			60	
			−40°C to +125°C			65	
I _{DD}	V _{DD} supply current	V _{DD} = 12V, V _{SS} = 0V All switches ON	25°C		50	65	μA
			−40°C to +85°C			70	
			−40°C to +125°C			75	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.10 Switching Characteristics (12V Single Supply)

$V_{DD} = +12V \pm 10\%$, $V_{SS} = 0V$, $GND = 0V$ (unless otherwise noted). Typical at $V_{DD} = +12V$, $V_{SS} = 0V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{tran}	Transition Time	$V_{Sx} = +10V/0V$, $V_{Sx+1} = 0V/+10V$, $R_L = 1M\Omega$, $C_L = 35pF$	$25^\circ C$		125	185	ns
			$-40^\circ C$ to $+85^\circ C$			200	
			$-40^\circ C$ to $+125^\circ C$			210	
t_{ON}	Turn-on time from control input	$V_S = 5V$ $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		135	175	ns
			$-40^\circ C$ to $+85^\circ C$			200	
			$-40^\circ C$ to $+125^\circ C$			210	
t_{OFF}	Turn-off time from control input	$V_S = 5V$ $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		200	215	ns
			$-40^\circ C$ to $+85^\circ C$			220	
			$-40^\circ C$ to $+125^\circ C$			225	
t_{BBM}	Break-before-make time delay	$V_{Sx} = 5V$, $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		70		ns
			$-40^\circ C$ to $+85^\circ C$	45			
			$-40^\circ C$ to $+125^\circ C$	45			
Q_{INJ}	Charge injection	$V_S = 6V$, $C_L = 100pF$	$25^\circ C$		6.8		pC
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 6V$, $f = 100kHz$	$25^\circ C$		-100		dB
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 6V$, $f = 1MHz$	$25^\circ C$		-95		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 6V$, $f = 100kHz$	$25^\circ C$		-90		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 6V$, $f = 1MHz$	$25^\circ C$		-95		dB
BW	-3dB Bandwidth TMUX5508	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 6V$	$25^\circ C$		260		MHz
BW	-3dB Bandwidth TMUX5509	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 6V$	$25^\circ C$		380		MHz
I_L	Insertion loss	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 200mV_{RMS}$, $V_{BIAS} = 6V$, $f = 1MHz$	$25^\circ C$		-7.1		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62V$ on V_{DD} and V_{SS} $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$	$25^\circ C$		-60		dB
$C_{S(OFF)}$	TMUX5508Source off capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		2.4		pF
	TMUX5509Source off capacitance to ground				2.2		
$C_{D(OFF)}$	TMUX5508Drain off capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		10.6		pF
	TMUX5509Drain off capacitance to ground				7.2		
$C_{S(ON)}$, $C_{D(ON)}$	TMUX5508On capacitance to ground	$V_S = 0V$, $f = 1MHz$	$25^\circ C$		14		pF
	TMUX5509On capacitance to ground				13		

6.11 Electrical Characteristics (40V Single Supply)

$V_{DD} = +40V$, $V_{SS} = 0V$, $GND = 0V$ (unless otherwise noted). Typical at $V_{DD} = +40V$, $V_{SS} = 0V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = V _{SS} + 5V to V _{DD} -5V I _D = −1mA	25°C	130	155	Ω	
			−40°C to +85°C		190	Ω	
			−40°C to +125°C		225	Ω	
ΔR _{ON}	On-resistance mismatch between channels	V _{DD} = 40V V _S = V _{SS} + 5V to V _{DD} -5V I _D = −1mA	25°C	1.3		Ω	
			−40°C to +85°C		6	Ω	
			−40°C to +125°C		15	Ω	
R _{ON FLAT}	On-resistance flatness	V _{DD} = 40V V _S = V _{SS} + 5V to V _{DD} -5V I _D = −1mA	25°C	0.5		Ω	
			−40°C to +85°C		6.5	Ω	
			−40°C to +125°C		40	Ω	
I _{S(OFF)}	TMUX5508 Source off leakage current ⁽¹⁾	V _{DD} = 40V, V _{SS} = 0V Switch state is off V _S = 35V / 1V V _D = 1V / 35V	25°C	0.003		nA	
			−40°C to +85°C	−100	100		
			−40°C to +125°C	−100	100		
I _{S(OFF)}	TMUX5509 Source off leakage current ⁽¹⁾	V _{DD} = 40V, V _{SS} = 0V Switch state is off V _S = 35V / 1V V _D = 1V / 35V	25°C	0.005		nA	
			−40°C to +85°C	−50	50	nA	
			−40°C to +125°C	−50	50	nA	
I _{D(OFF)}	TMUX5508 Drain off leakage current ⁽¹⁾	V _{DD} = 40V, V _{SS} = 0V Switch state is off V _S = 35V / 1V V _D = 1V / 35V	25°C	0.01		nA	
			−40°C to +85°C	−100	100		
			−40°C to +125°C	−100	100		
I _{D(OFF)}	TMUX5509 Drain off leakage current ⁽¹⁾	V _{DD} = 40V, V _{SS} = 0V Switch state is off V _S = 35V / 1V V _D = 1V / 35V	25°C	0.02		nA	
			−40°C to +85°C	−50	50	nA	
			−40°C to +125°C	−50	50	nA	
I _{S(ON)} I _{D(ON)}	TMUX5508 Channel on leakage current ⁽²⁾	V _{DD} = 40V, V _{SS} = 0V Switch state is on V _S = V _D = 35V or 1V	25°C	0.01		nA	
			−40°C to +85°C	−100	100		
			−40°C to +125°C	−100	100		
I _{S(ON)} I _{D(ON)}	TMUX5509 Channel on leakage current ⁽²⁾	V _{DD} = 40V, V _{SS} = 0V Switch state is on V _S = V _D = 35V or 1V	25°C	0.01		nA	
			−40°C to +85°C	−50	50	nA	
			−40°C to +125°C	−50	50	nA	
LOGIC INPUTS (SEL / EN pins)							
POWER SUPPLY							
I _{DD}	V _{DD} supply current	V _{DD} = 40V, V _{SS} = 0V Logic inputs = 0V, 5V, or V _{DD}	25°C	60	85	μA	
			−40°C to +85°C		90	μA	
			−40°C to +125°C		95	μA	
I _{DDQ}	V _{DD} quiescent supply current	V _{DD} = 40V, V _{SS} = 0V All Switches OFF	−40°C to +125°C		80	μA	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.12 Switching Characteristics (40V Single Supply)

$V_{DD} = +40V$, $V_{SS} = 0V$, $GND = 0V$ (unless otherwise noted). Typical at $V_{DD} = +40V$, $V_{SS} = 0V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{tran}	Transition Time	$V_{Sx} = +10V/0V$, $V_{Sx+1} = 0V/+10V$, $R_L = 1M\Omega$, $C_L = 35pF$	$25^\circ C$		160	210	ns
t_{tran}	Transition Time	$V_{Sx} = +10V/0V$, $V_{Sx+1} = 0V/+10V$, $R_L = 1M\Omega$, $C_L = 35pF$	$-40^\circ C$ to $+85^\circ C$			220	ns
t_{tran}	Transition Time	$V_{Sx} = +10V/0V$, $V_{Sx+1} = 0V/+10V$, $R_L = 1M\Omega$, $C_L = 35pF$	$-40^\circ C$ to $+125^\circ C$			230	ns
t_{ON}	Turn-on time from control input	$V_S = 5V$ $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		185	205	ns
			$-40^\circ C$ to $+85^\circ C$			215	ns
			$-40^\circ C$ to $+125^\circ C$			220	ns
t_{OFF}	Turn-off time from control input	$V_S = 5V$ $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		175	200	ns
			$-40^\circ C$ to $+85^\circ C$			210	ns
			$-40^\circ C$ to $+125^\circ C$			220	ns
t_{BBM}	Break-before-make time delay	$V_{Sx} = 5V$, $R_L = 1k\Omega$, $C_L = 35pF$	$25^\circ C$		100		ns
			$-40^\circ C$ to $+85^\circ C$	50			ns
			$-40^\circ C$ to $+125^\circ C$	50			ns
Q_{INJ}	Charge injection	$V_S = 20V$, $C_L = 100pF$	$25^\circ C$		5		pC
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 6V$, $f = 100kHz$	$25^\circ C$		-100		dB
O_{ISO}	Off-isolation	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 6V$, $f = 1MHz$	$25^\circ C$		-100		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 6V$, $f = 100kHz$	$25^\circ C$		-100		dB
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 6V$, $f = 1MHz$	$25^\circ C$		-100		dB
BW	-3dB Bandwidth TMUX5508	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 6V$	$25^\circ C$		275		MHz
BW	-3dB Bandwidth TMUX5509	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 6V$	$25^\circ C$		400		MHz
I_L	Insertion loss	$R_L = 50\Omega$, $C_L = 5pF$ $V_S = 6V$, $f = 1MHz$	$25^\circ C$		-7.2		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62V$ on V_{DD} and V_{SS} $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$	$25^\circ C$		-60		dB
$C_{S(OFF)}$	TMUX5508 Source off capacitance to ground	$V_S = 20V$, $f = 1MHz$	$25^\circ C$		2.9		pF
$C_{S(OFF)}$	TMUX5509 Source off capacitance to ground	$V_S = 20V$, $f = 1MHz$	$25^\circ C$		2.3		pF
$C_{D(OFF)}$	TMUX5508 Drain off capacitance to ground	$V_S = 20V$, $f = 1MHz$	$25^\circ C$		13.2		pF
$C_{D(OFF)}$	TMUX5509 Drain off capacitance to ground	$V_S = 20V$, $f = 1MHz$	$25^\circ C$		6.8		pF
$C_{S(ON)}$, $C_{D(ON)}$	TMUX5508 On capacitance to ground	$V_S = 20V$, $f = 1MHz$	$25^\circ C$		18.8		pF
$C_{S(ON)}$, $C_{D(ON)}$	TMUX5509 On capacitance to ground	$V_S = 20V$, $f = 1MHz$	$25^\circ C$		13		pF

6.13 Typical Characteristics

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

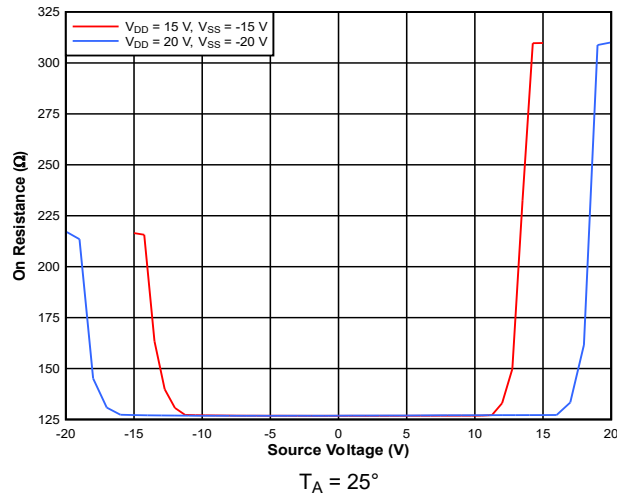


Figure 6-1. On-Resistance vs Source or Drain Voltage for Dual Supply

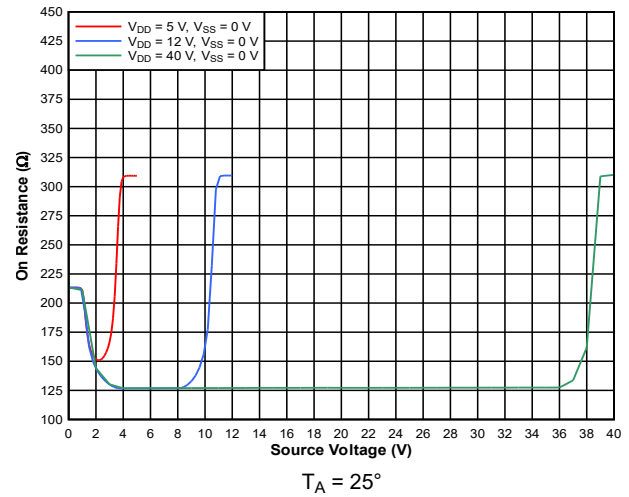


Figure 6-2. On-Resistance vs Source or Drain Voltage for Single Supply

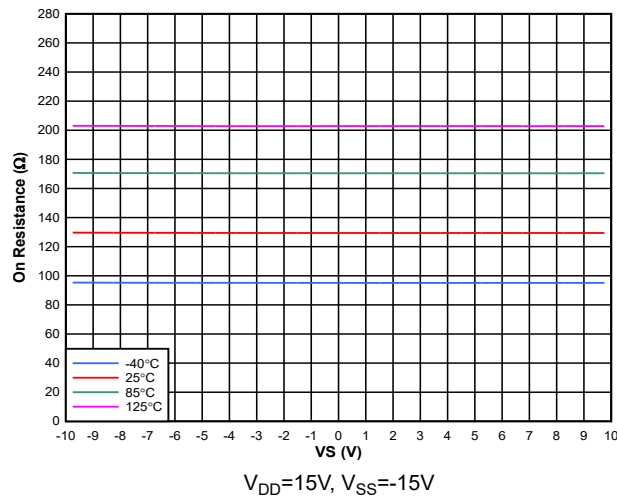


Figure 6-3. On-Resistance vs Source or Drain Operational Voltage (Flat Region)

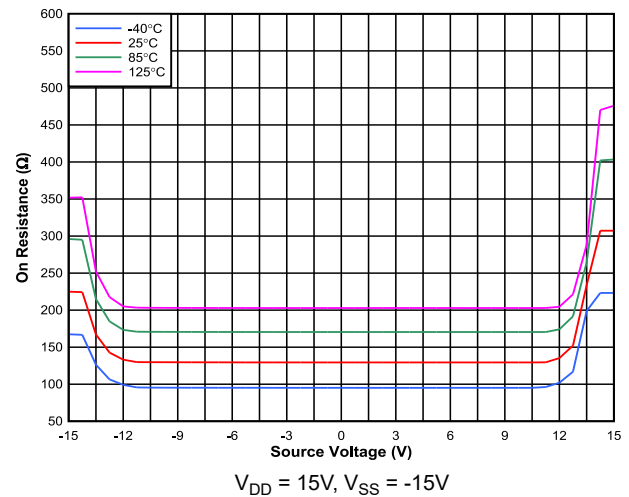


Figure 6-4. On-Resistance vs Source or Drain Voltage

6.13 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

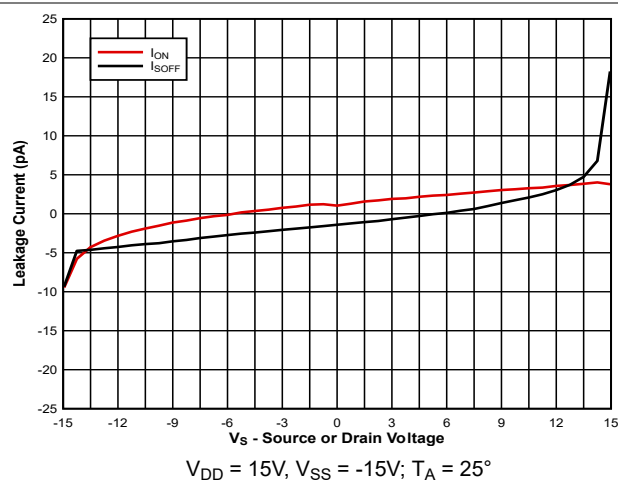


Figure 6-5. Leakage Current vs Bias Voltage

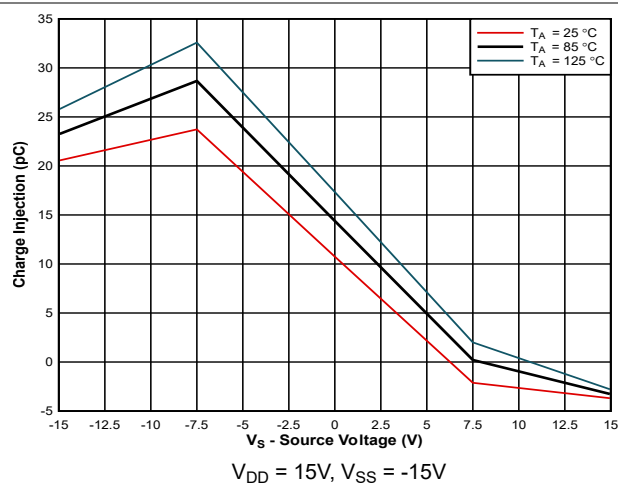


Figure 6-6. Charge Injection vs Source Voltage

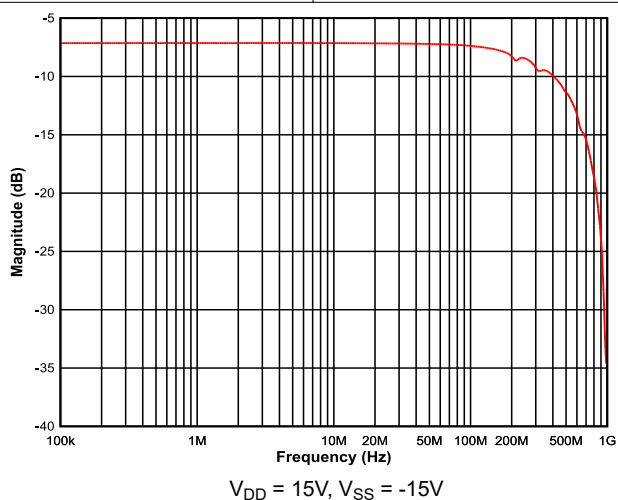


Figure 6-7. $\pm 15\text{V}$ Bandwidth vs. Frequency

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of the TMUX550x is the ohmic resistance across the source (Sx, SxA, or SxB) and drain (D, DA, or DB) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 7-1. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in Equation 1.

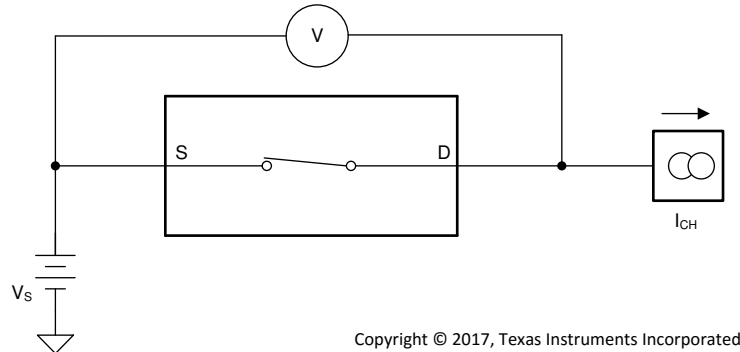


Figure 7-1. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source off-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain off-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both types of off-leakage currents is shown in Figure 7-2.

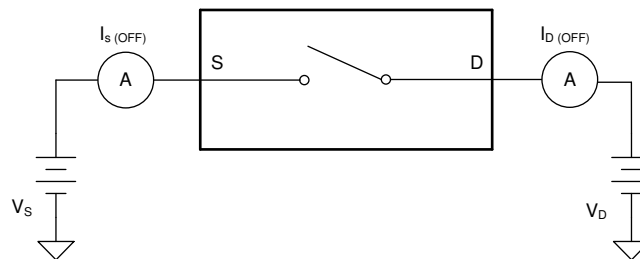
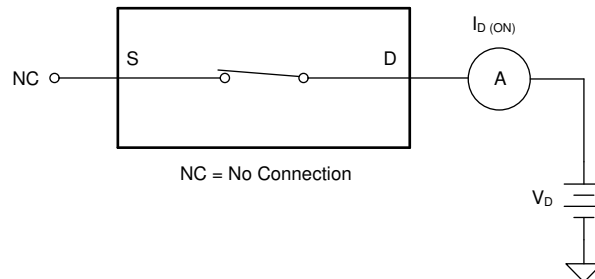


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.



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Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX550x to rise or fall to 90% of the transition after the digital address signal has fallen or risen to the 50% of the transition. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol t_t .

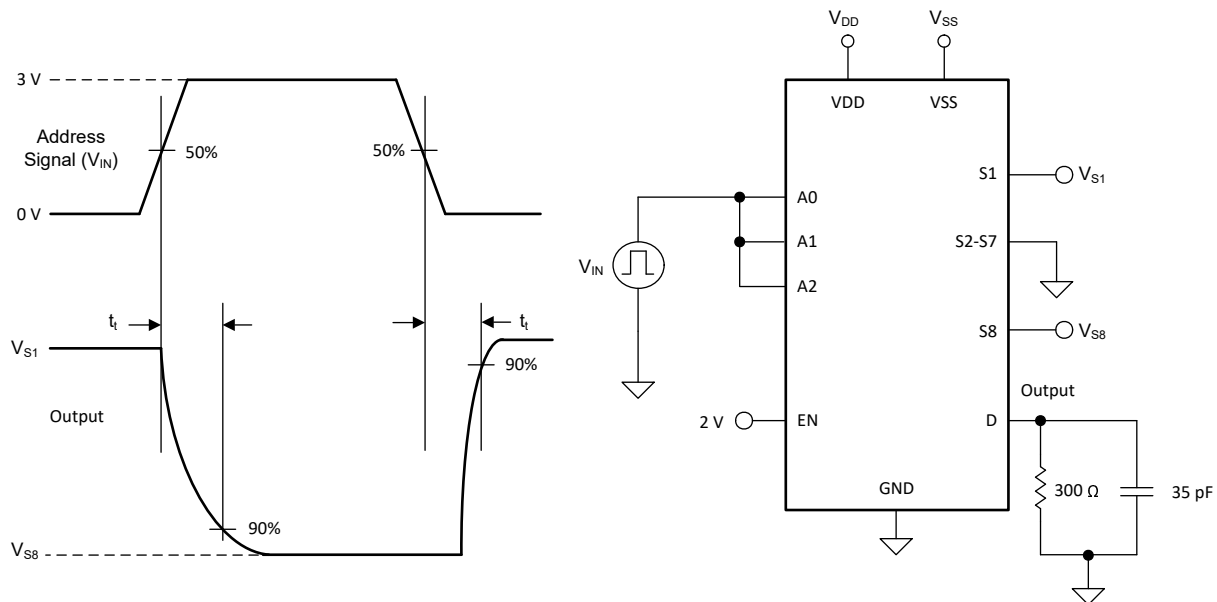


Figure 7-4. Transition-Time Measurement Setup

7.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX550x is switching. The TMUX550x output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as a break-before-make delay. Figure 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM} .

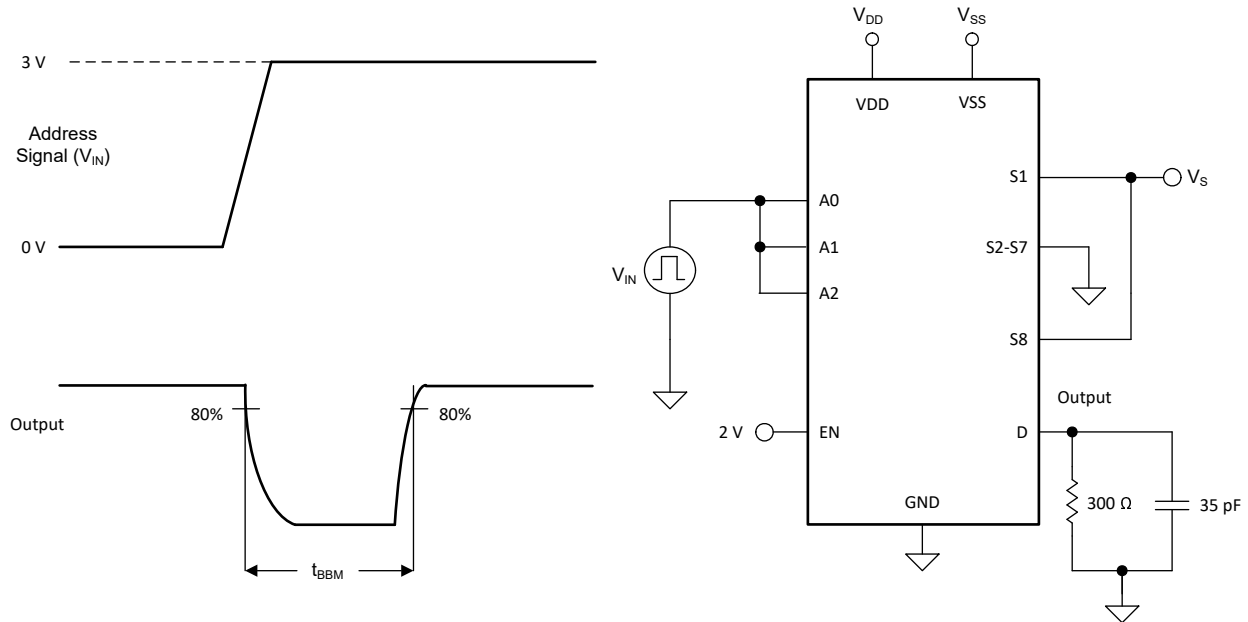


Figure 7-5. Break-Before-Make Delay Measurement Setup

7.6 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the TMUX550x to rise to a 90% final value after the enable signal has risen to a 50% final value. Figure 7-6 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON} .

Turn-off time is defined as the time taken by the output of the TMUX550x to fall to a 10% initial value after the enable signal has fallen to a 50% initial value. Figure 7-6 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF} .

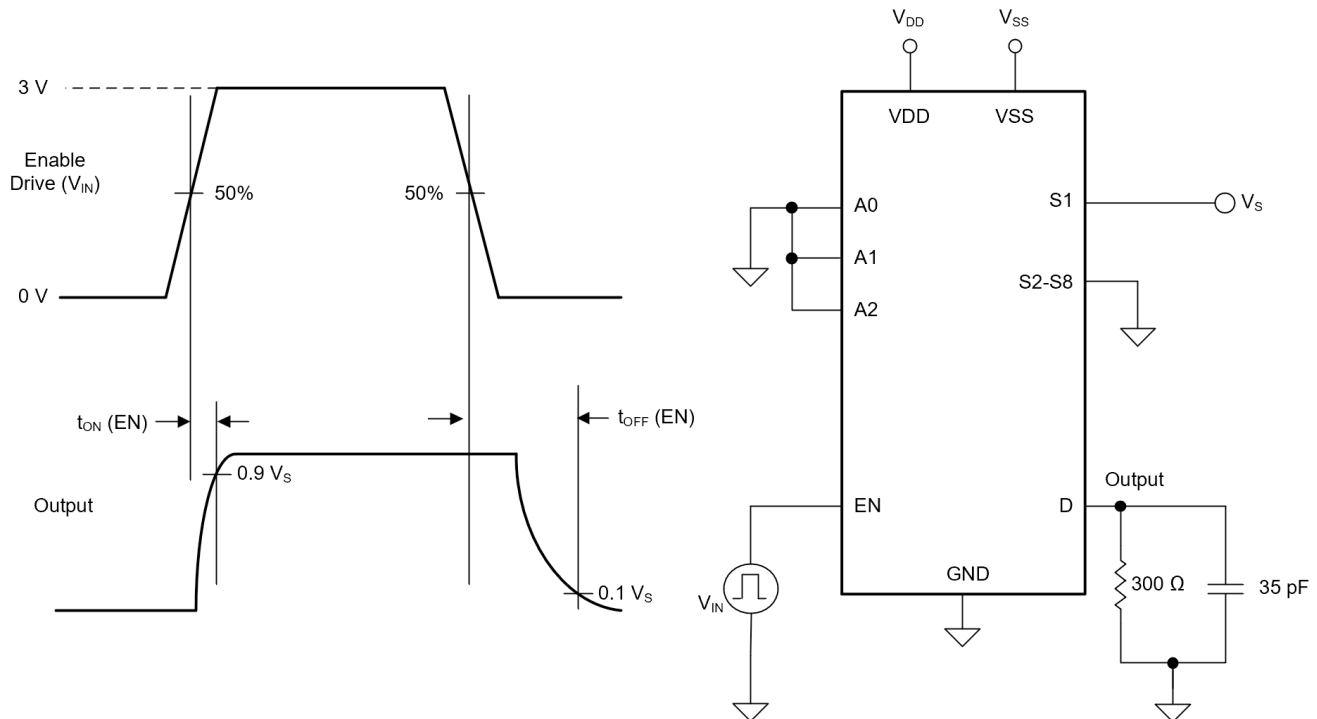


Figure 7-6. Turn-On and Turn-Off Time Measurement Setup

7.7 Charge Injection

The TMUX550x have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ} . Figure 7-7 shows the setup used to measure charge injection.

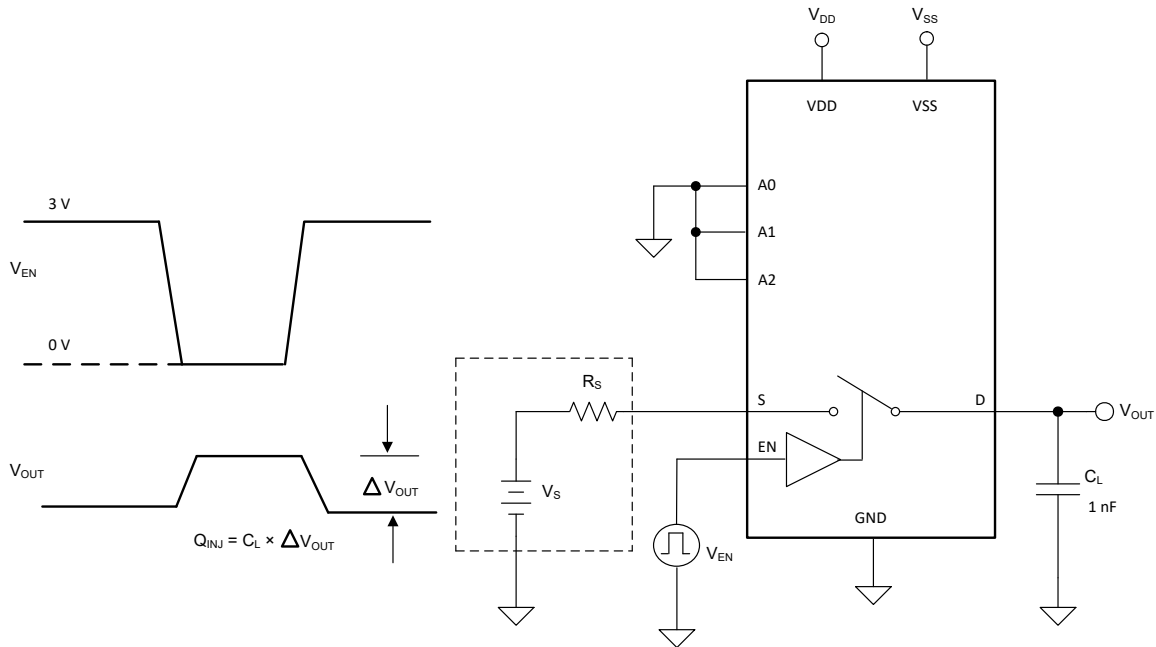
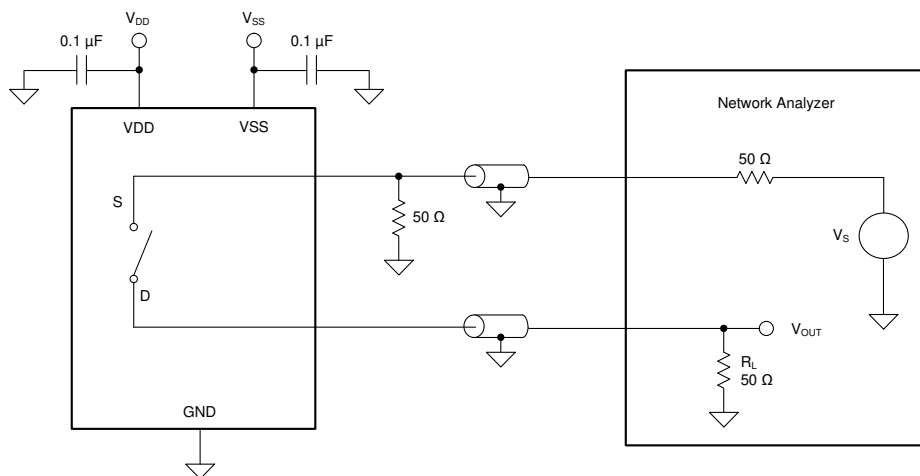


Figure 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the voltage at the drain pin (D, DA, or DB) of the TMUX550x when a $1V_{RMS}$ signal is applied to the source pin (Sx, SxA, or SxB) of an off-channel. Figure 7-8 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.



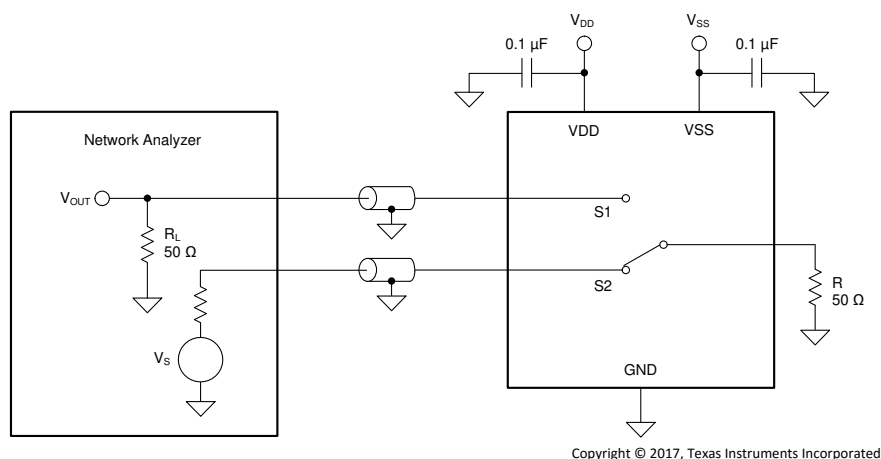
Copyright © 2017, Texas Instruments Incorporated

Figure 7-8. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{OUT}}{V_S} \right) \quad (2)$$

7.9 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx, SxA, or SxB) of an off-channel, when a $1V_{RMS}$ signal is applied at the source pin of an on-channel. Figure 7-9 shows the setup used to measure, and Equation 3 is the equation used to compute, channel-to-channel crosstalk.



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Figure 7-9. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left(\frac{V_{OUT}}{V_S} \right) \quad (3)$$

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3dB when the input is applied to the source pin of an on-channel and the output is measured at the drain pin of the TMUX550x. [Figure 7-10](#) shows the setup used to measure bandwidth of the mux. Use [Equation 4](#) to compute the attenuation.

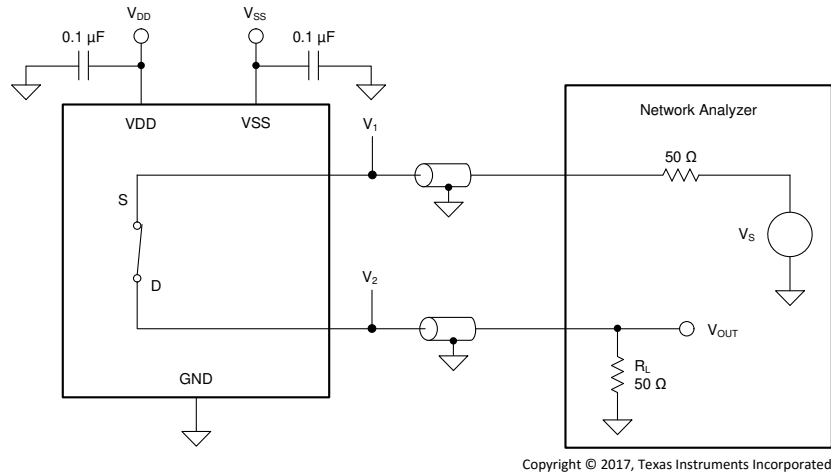


Figure 7-10. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \log\left(\frac{V_2}{V_1}\right) \quad (4)$$

7.11 THD + Noise

The total harmonic distortion (THD) of a signal is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX550x varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. [Figure 7-11](#) shows the setup used to measure the THD+N of the TMUX550x.

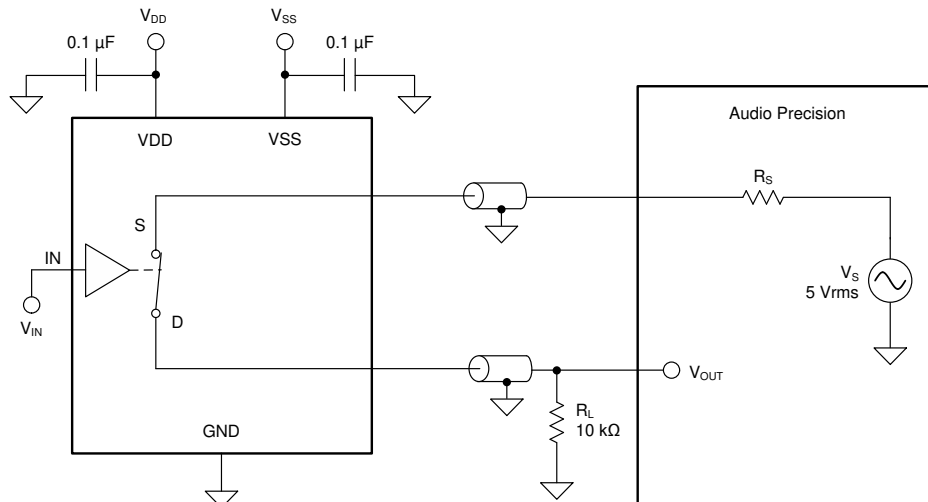


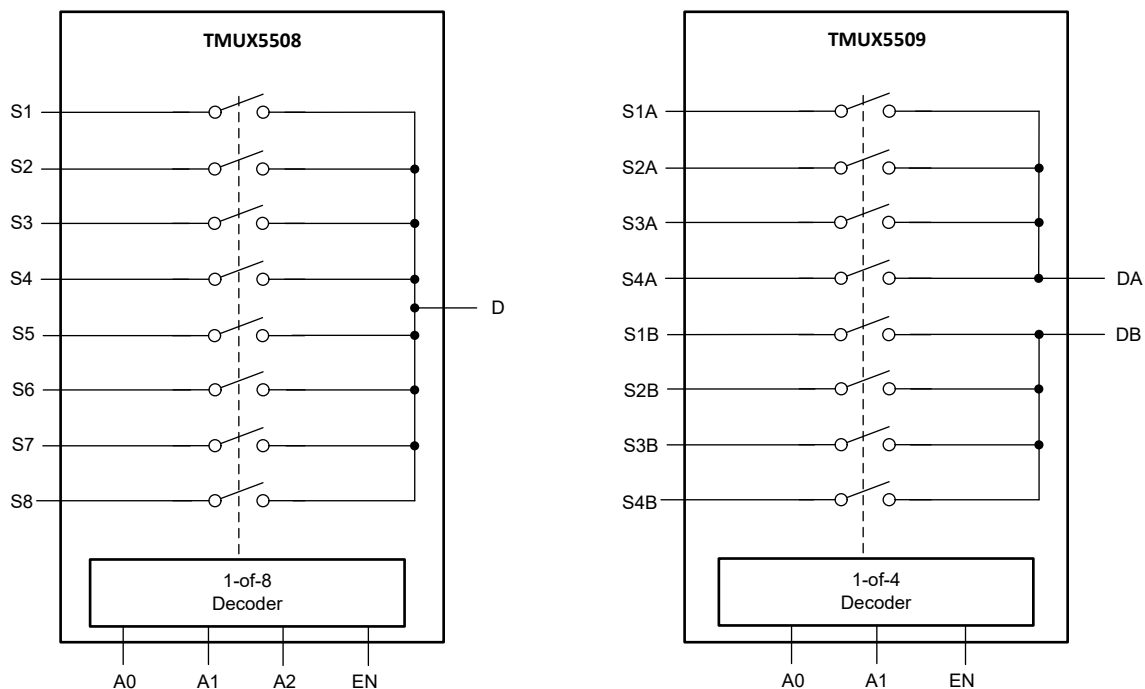
Figure 7-11. THD+N Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX550x are a family of analog multiplexers. [Section 8.2](#) provides a top-level block diagram of both the TMUX5508 and TMUX5509. The TMUX5508 is an eight-channel, single-ended, analog mux. The TMUX5509 is a four-channel, differential or dual 4:1, single-ended, analog mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX550x are operable as both a mux or demux. The source (Sx, SxA, SxB) and drain (D, DA, DB) pins of the TMUX550x are used either as input or output. Each TMUX550x channel has very similar characteristics in both directions.

8.3.2 Rail-to-Rail Operation

A valid analog signal for the TMUX550x ranges from V_{SS} to V_{DD} . The input signal to the TMUX550x can swing from V_{SS} to V_{DD} without any significant degradation in performance. The best R_{ON} performance for the signal will be 5V below V_{DD} and 5V above V_{SS} .

8.3.3 1.8V Logic Compatible Inputs

The TMUX550x has 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX550x to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8V logic implementations, see [Simplifying Design with 1.8V logic Muxes and Switches](#).

8.3.4 Flat On-Resistance

The TMUX550x is designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operating region. The flat R_{ON} response allows the device to be used in a wide variety of applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so unwanted noise is not produced from the device to affect sampling accuracy.

This architecture also keeps R_{ON} the same regardless of the supply voltage. The flattest on-resistance region extends roughly from 5V above V_{SS} to 5V below V_{DD} . As long as this headroom is maintained, the TMUX550x exhibits an extremely linear response.

8.3.5 Power-Up Sequence Free

The TMUX550x supports any power up sequencing. With the supply rails (V_{DD} and V_{SS}), any rail can be powered on first. Similarly, when powering down the supply rails can be powered down in any order.

8.4 Device Functional Modes

When the EN pin of the TMUX550x is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state irrespective of the state of the address lines. The EN pin can be connected to V_{DD} (as high as 40V).

8.5 Truth Tables

Table 8-1 and Table 8-2 provides the truth tables for the TMUX5508 and TMUX5509 respectively.

Table 8-1. TMUX5508 Truth Table

$\overline{\text{EN}}$	A2	A1	A0	Selected Signal Path Connected To Drain (D) Pin
0	0	0	0	S0
0	0	0	1	S1
0	0	1	0	S2
0	0	1	1	S3
0	1	0	0	S4
0	1	0	1	S5
0	1	1	0	S6
0	1	1	1	S7
1	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	All channels are off

(1) X denotes *do not care*.

Table 8-2. TMUX5509 Truth Table

$\overline{\text{EN}}$	A1	A0	Selected Signal Path Connected To Drain (DA and DB) Pins
0	0	0	S0A to DA S0B to DB
0	0	1	S1A to DA S1B to DB
0	1	0	S2A to DA S2B to DB
0	1	1	S3A to DA S3B to DB
1	X ⁽¹⁾	X ⁽¹⁾	All channels are off

(1) X denotes *do not care*.

9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 9-1](#).

Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (VDD)	15V
Supply (VSS)	-15V
Input/ Output signal range	-10V to 10V
Max current through each channel	20mA
Control logic thresholds	1.8V compatible

9.2.2 Application Curve

TMUX5508 and TMUX5509 have very flat RON; however, when the signal approaches within 5V of either supply, it increases. The plots below show two scenarios: 1. Operating in the signal range 5V below the supply rail and 2. Operating the signal up to the supply rail.

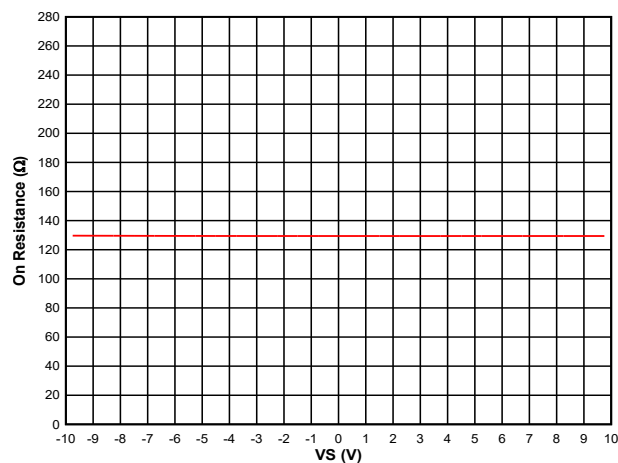


Figure 9-2. On-Resistance vs Source or Drain Voltage up to $\pm 10V$ with 15V V_{DD} and -15V V_{SS}

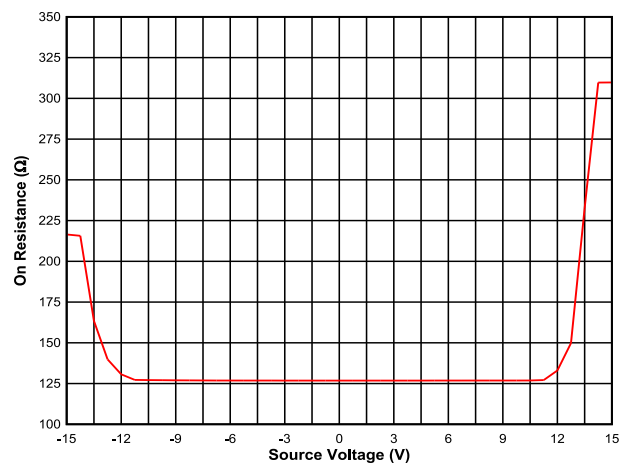


Figure 9-3. On-Resistance vs Source or Drain Voltage up to rail

9.3 Layout

9.3.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 9-4](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

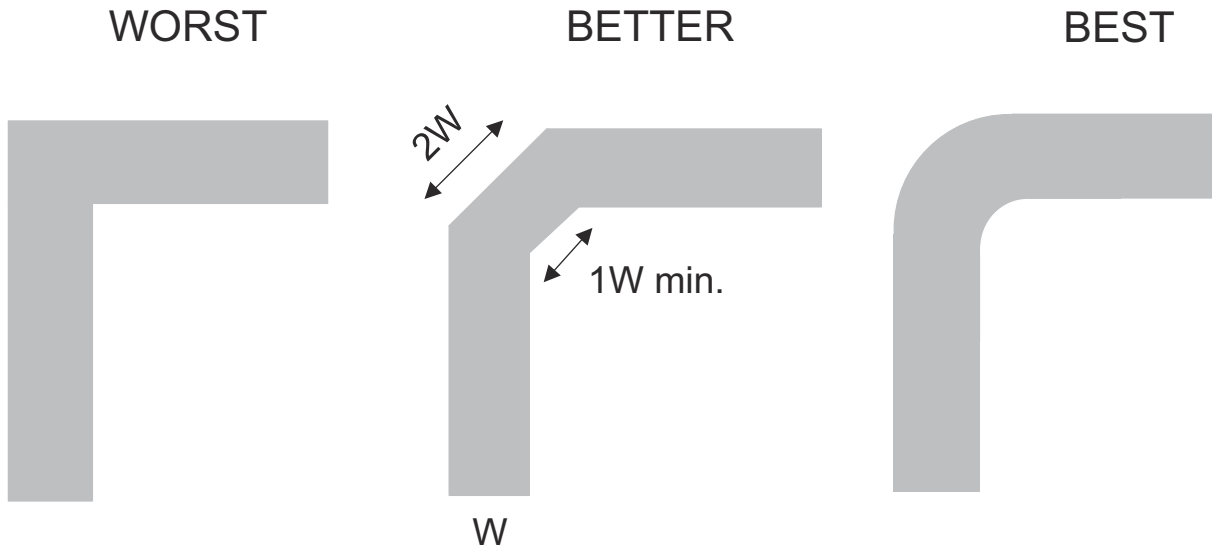


Figure 9-4. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

[Figure 9-5](#) shows an example of a PCB layout with the TMUX5508PW, and [Figure 9-6](#) shows an example of a PCB layout with TMUX5509PW. The guidelines provided in this section are also applicable to the SOIC and QFN package variants as well.

Some key considerations are:

1. Decouple the VDD and VSS pins with a 0.1µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as small as possible. For the TMUX5509 differential signals, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when necessary.

9.3.2 Layout Example

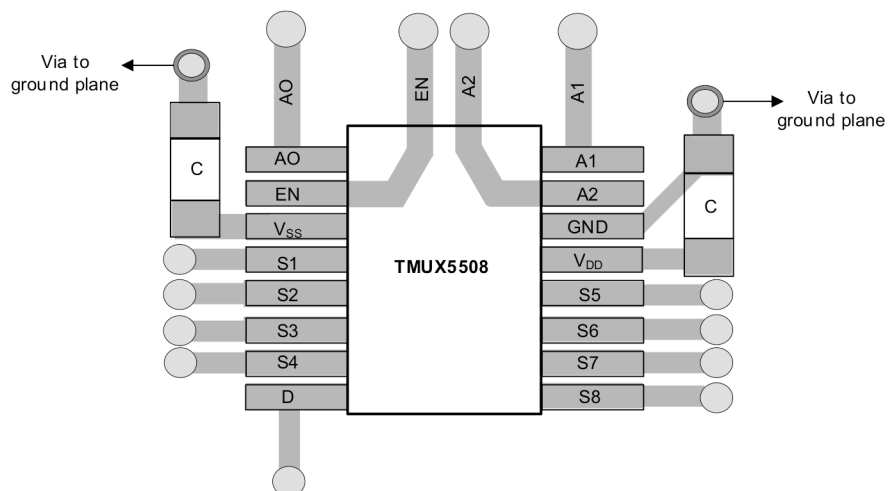


Figure 9-5. TMUX5508 Layout Example

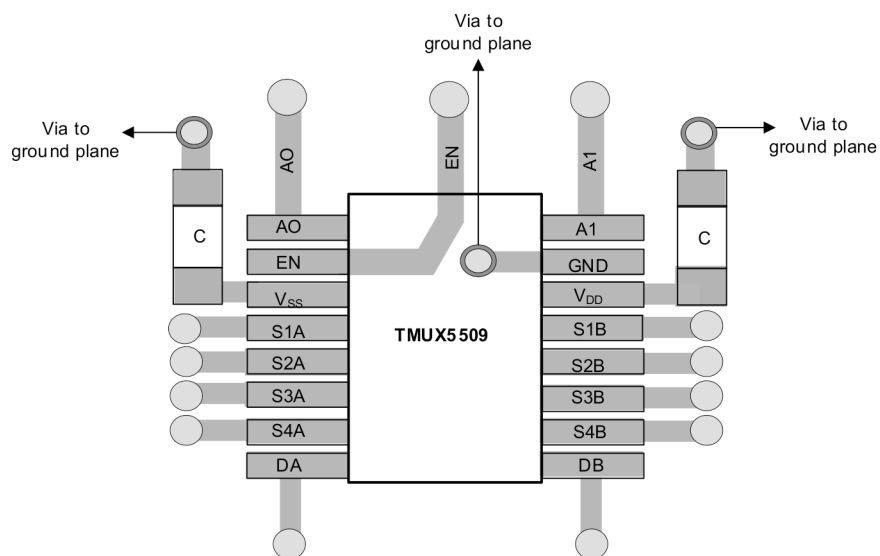


Figure 9-6. TMUX5509 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, [ADS866x 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges](#)
- Texas Instruments, [OPAx140 High-Precision, Low-Noise, Rail-to-Rail Output, 11MHz JFET Op Amp](#)
- Texas Instruments, [OPAx192 36V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2026) to Revision A (October 2026)	Page
• Updated datasheet status from <i>Advanced Information</i> to <i>Production Data</i>	1
• Added typical plots and application sections.....	8
• Updated Thermal parameters.....	8
• Updated Electrical and AC Characteristics tables.....	9

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTMUX5508RSVR	Active	Preproduction	UQFN (RSV) 16	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTMUX5509RSVR	Active	Preproduction	UQFN (RSV) 16	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TMUX5509RSVR	Active	Preproduction	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5509

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

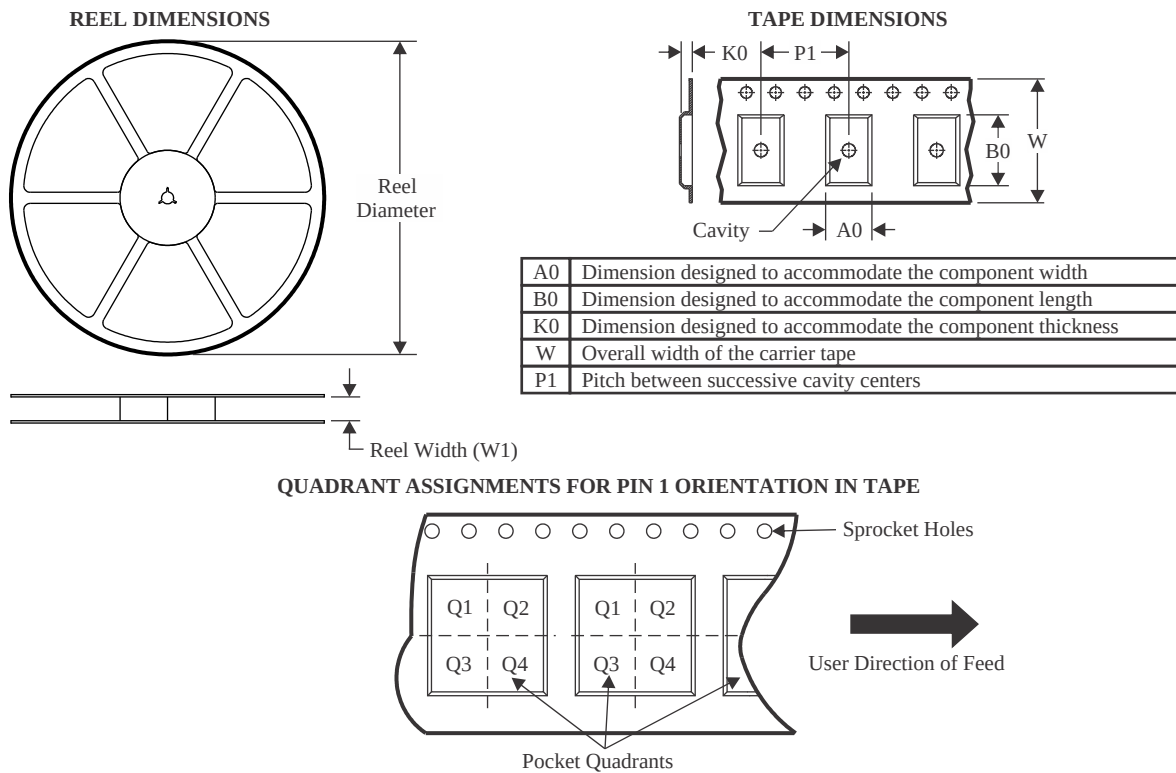
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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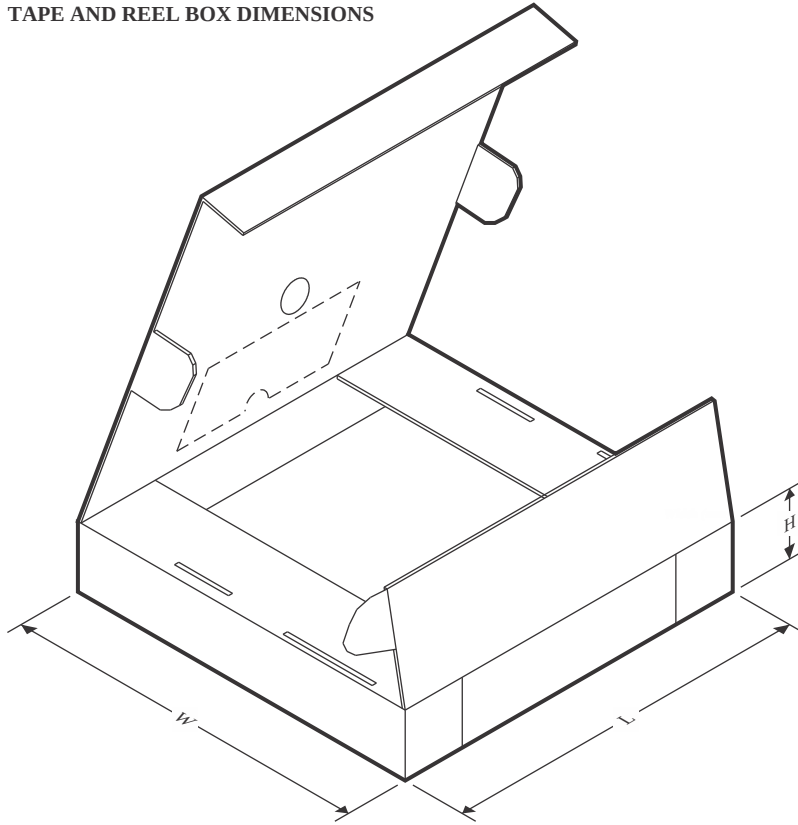
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX5509RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX5509RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

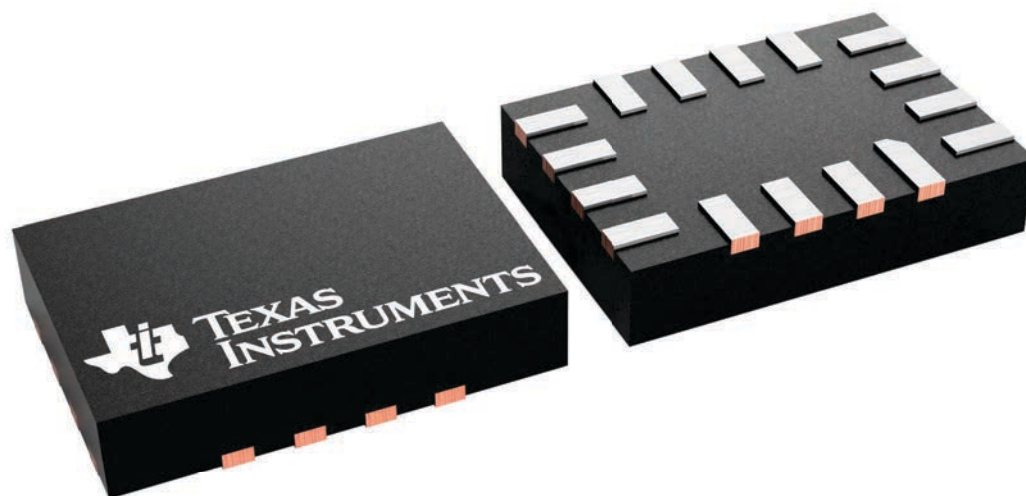
RSV 16

UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

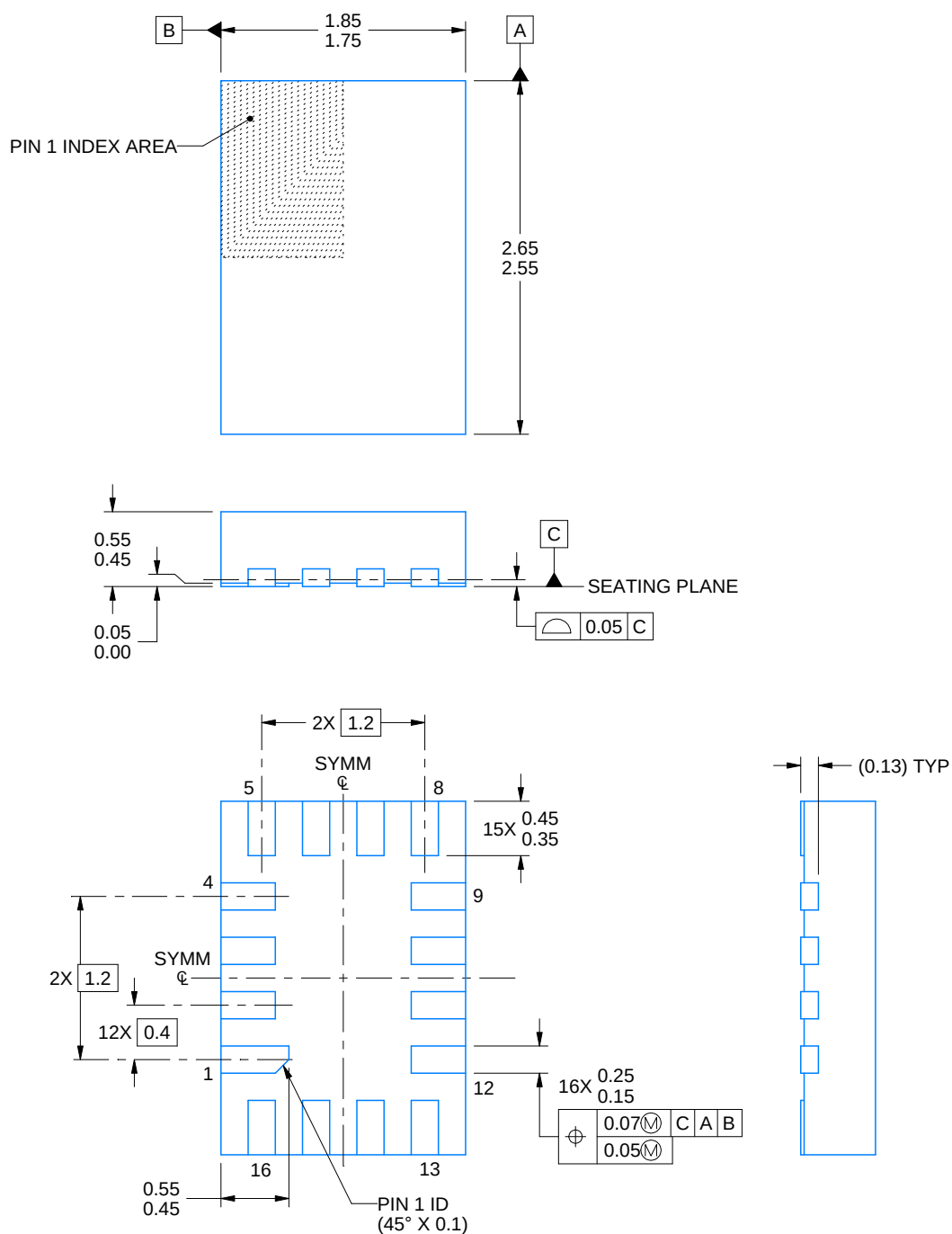
ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



4220314/C 02/2020

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

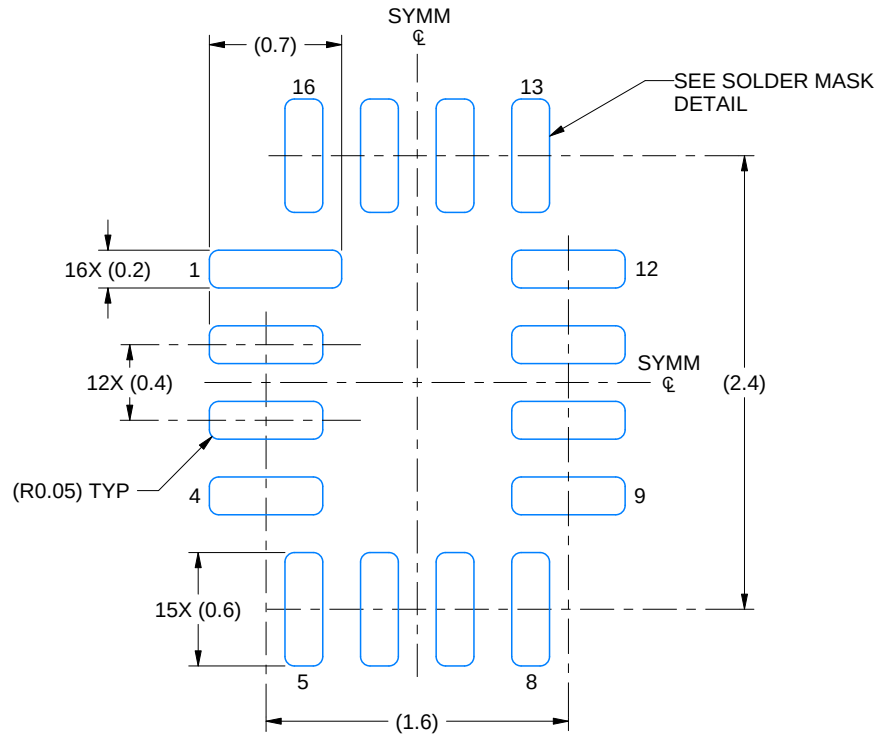
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

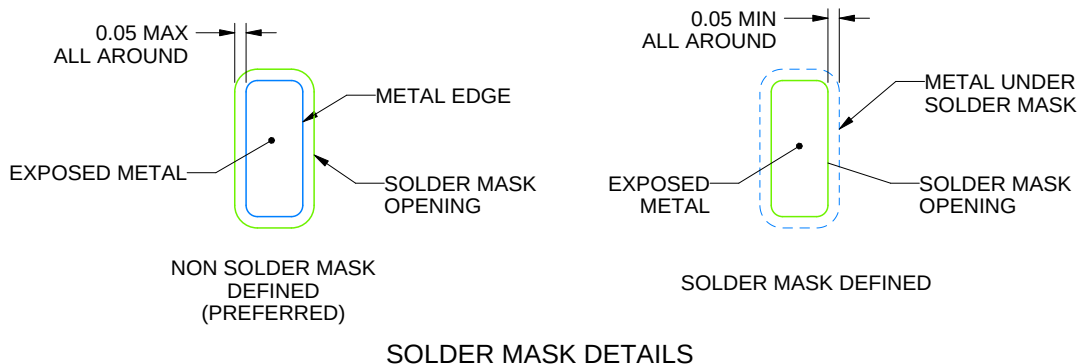
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

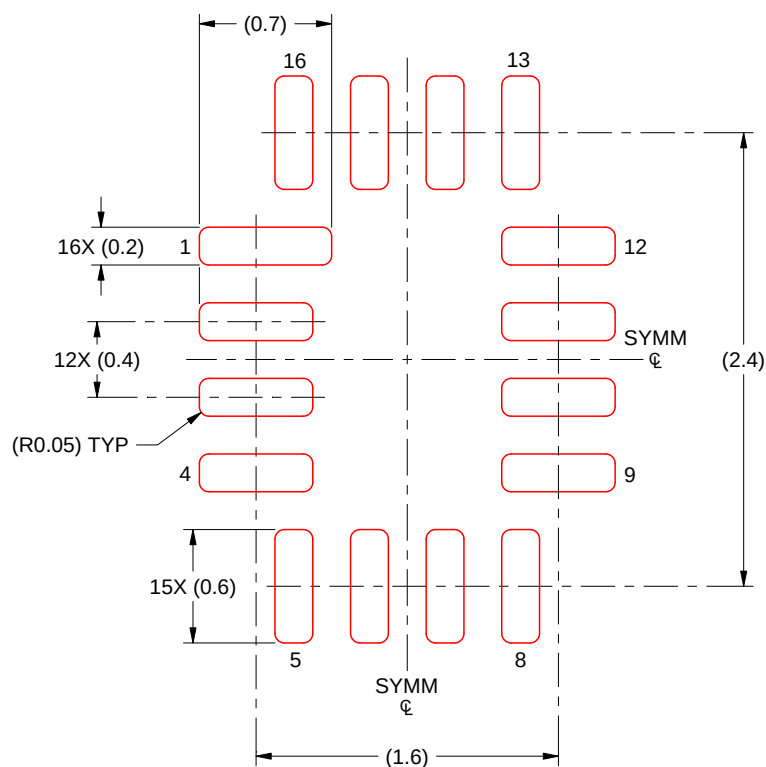
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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