TMUX142-SEP Radiation Tolerant 15V, 4:1, 2-Channel Multiplexer With 1.8V Logic

1 Features

- VID XXXX
- Space enhanced plastic
  - Supports Defense and Aerospace Applications
  - Operating temperature from –55°C to +125°C
  - Controlled baseline
  - Au (gold) bondwire and NiPdAu lead finish
  - One fabrication, assembly, and test site
  - Extended product life cycle
  - Product traceability
  - Enhanced mold compound for low outgassing
  - Meets NASA ASTM E595 outgassing specification
- Total ionizing dose characterized at 30krad (Si)
  - Total ionizing dose radiation lot acceptance (TID RLAT) for every wafer lot to 30krad (Si)
- Single-event effects (SEE) characterized:
  - Single event latch-up (SEL) immune to linear energy transfer (LET) = 47MeV-cm^2/mg
  - Single event transient (SET) characterization report available
- Single supply range: 5V to 15V
- Dual supply range: up to ±6V
- Low capacitance: 3pF
- Bidirectional signal path
- Rail-to-rail operation
- 1.8V logic compatible
- Break-before-make switching
- ESD protection HBM: 2000V

2 Applications

- Analog multiplexing and demultiplexing
- Low earth orbit (LEO) space applications
- Remote interface unit (RIU)
- Remote telemetry unit (RTU)
- System monitoring for space
- Latch-up and overvoltage detection
- Power-up sequencing protection
- Satellite telemetry and telecommand for on board data handling
- Sensor data acquisition

3 Description

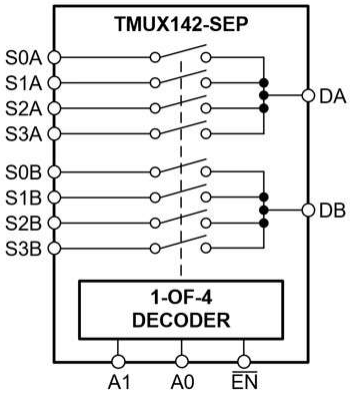
The TMUX142-SEP device is a 2-channel, 4:1 general purpose complementary metal-oxide semiconductor (CMOS) multiplexer (MUX). The device works with a single supply (5V to 15V), dual supplies (up to ±6V), or asymmetric supplies (such as V_{DD} = 6V, V_{SS} = –3V). The wide supply voltage range allows the devices to be used in a broad array of applications in space. The two channels can be used for both differential and single-ended applications.

The TMUX142-SEP supports bidirectional analog signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}. All logic inputs have 1.8V logic compatible thresholds, which is compatible for both TTL and CMOS logic when operating with a valid supply voltage.

Package Information

PART NUMBER	PACKAGE	PACKAGE SIZE(1)
TMUX142-SEP	DYY (SOT-23-THIN, 16)	4.2mm × 3.26mm

(1) For more information, see *Section 11*.



TMUX142-SEP Block Diagram

ADVANCE INFORMATION

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

ADVANCE INFORMATION

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Thermal Information....5
5.4 Recommended Operating Conditions....5
5.5 Electrical Characteristics....6
5.6 AC Performance Characteristics....8
5.7 Timing Characteristics....9
5.8 Typical Characteristics....10
6 Parameter Measurement Information....12
6.1 On-Resistance....12
6.2 Off-Leakage Current....12
6.3 On-Leakage Current....13
6.4 Transition Time....13
6.5 Break-Before-Make....14
6.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$....14
6.7 Propagation Delay....15
6.8 Charge Injection....15
6.9 Off Isolation....16
6.10 Crosstalk....16
6.11 Bandwidth....17
7 Detailed Description....18
7.1 Overview....18
7.2 Functional Block Diagram....18
7.3 Feature Description....18
8 Application and Implementation....20
8.1 Application Information....20
8.2 Typical Application....20
8.3 Design Requirements....22
8.4 Detailed Design Procedure....22
8.5 Application Curves....22
8.6 Power Supply Recommendations....22
8.7 Layout....23
9 Device and Documentation Support....24
9.1 Documentation Support....24
9.2 Receiving Notification of Documentation Updates....24
9.3 Support Resources....24
9.4 Trademarks....24
9.5 Electrostatic Discharge Caution....24
9.6 Glossary....24
10 Revision History....24
11 Mechanical, Packaging, and Orderable Information....24

Copyright © 2026 Texas Instruments Incorporated

4 Pin Configuration and Functions

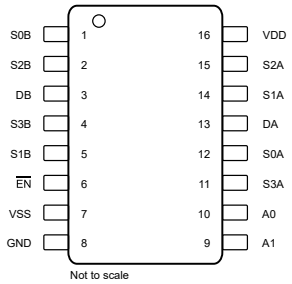


Figure 4-1. TMUX142-SEP DYY Package,16-Pin SOT-23-THIN(Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
S0B	1	I/O	Source pin 0 of mux B. Can be an input or output.
S2B	2	I/O	Source pin 2 of mux B. Can be an input or output.
DB	3	I/O	Drain pin (common) of mux B. Can be an input or output.
S3B	4	I/O	Source pin 3 of mux B. Can be an input or output.
S1B	5	I/O	Source pin 1 of mux B. Can be an input or output.
$\overline{EN}$	6	I	Active low logic enable. When this pin is high, all switches are turned off. Table 7-1 lists how the A[2:0] address inputs determine which switch is turned on when this pin is low.
V_{SS}	7	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND.
GND	8	P	Ground (0V) reference
A1	9	I	Address line 1. Table 8-2 provides information about how A1 controls the switch configuration.
A0	10	I	Address line 0. Table 8-2 provides information about how A0 controls the switch configuration.
S3A	11	I/O	Source pin 3 of mux A. Can be an input or output.
S0A	12	I/O	Source pin 0 of mux A. Can be an input or output.
DA	13	I/O	Drain pin (common) of mux A. Can be an input or output.
S1A	14	I/O	Source pin 1 of mux A. Can be an input or output.
S2A	15	I/O	Source pin 2 of mux A. Can be an input or output.
V_{DD}	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) For what to do with unused pins, refer to Section 7.3.4.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(3)

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		18	V
V_{DD}		–0.5	18	V
V_{SS}		–8	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, Ax, SELx)	–0.5	V_{DD}+0.5	V
I_{SEL} or I_{EN}	Logic control input pin current ($\overline{EN}$, Ax, SELx)	–0.5	28	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(2)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–10	10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) To avoid drawing excess current from V_{DD}, or into V_{SS}, the voltage drop across the bidirectional switch path (ΔV_{switch}) must not exceed 1.2V (600mV for high temperature).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2026 Texas Instruments Incorporated

5.3 Thermal Information

THERMAL METRIC(1)		TMUX142-SEP DYY (SOT) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$(1)	Power supply voltage differential	5		15	V
V_{DD}	Positive power supply voltage (Single Supply, Vss = 0V)	5		15	V
V_{SS}	Negative power supply voltage (Dual Supply)	–6		0	V
V_{DD_D}	Positive power supply voltage (Dual Supply)	5		6	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{Ax} or V_{EN}	Address or enable pin voltage	0		V_{DD}	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–10		10	mA
T_A	Ambient temperature	–55		125	°C

(1) V_{DD} and V_{SS} can be any value as long as $5V \le (V_{DD} – V_{SS}) \le 15V$, and the minimum V_{DD} and V_{SS} are met.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

5.5 Electrical Characteristics

Over operating free-air temperature range, Typical at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD}	V_{SS}	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY								
Supply current I_{DD}	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	5V	0V	–55°C			60	µA
				25°C		17	60	
				85°C			80	
				125°C			80	
		10V	0V	–55°C			60	
				25°C		18	60	
				85°C			80	
				125°C			80	
		5V	–5V	–55°C			60	
				25°C		18	60	
				85°C			80	µA
				125°C			80	µA
		15V	0V	–55°C			60	µA
				25°C		18	60	µA
				85°C			80	µA
				125°C			80	µA
Negative supply current I_{SS}	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	5V	–5V	–55°C			20	µA
				25°C		6	20	
				85°C			25	
				125°C			25	µA
I_{DD} disable	$\overline{EN}$ = 5V or V_{DD}	All		25°C		8		µA
				–55°C to 125°C			20	
ANALOG SWITCH								
R_{ON} Source to Drain ON-Resistance	V_S = V_{SS} to V_{DD} I_D = –1mA	5V	0V	–55°C			800	Ω
				25°C		75	1050	
				85°C			1200	
				125°C			1300	
		10V	0V	–55°C			310	
				25°C		60	400	
				85°C			520	
				125°C			550	
		5V	–5V	–55°C			310	
				25°C		60	400	
				85°C			520	Ω
				125°C			550	Ω
		15V	0V	–55°C			200	Ω
				25°C		60	240	Ω
				85°C			300	Ω
				125°C			300	Ω
ΔR_{ON}	V_S = V_{SS} to V_{DD} I_D = –1mA	All		25°C		2		Ω

Copyright © 2026 Texas Instruments Incorporated

Over operating free-air temperature range, Typical at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD}	V_{SS}	T_A	MIN	TYP	MAX	UNIT
$R_{ON\ FLAT}$	V_S = V_{SS} to V_{DD} I_D = –1mA	All		25°C		60		Ω
				–55°C to 85°C			150	
				–55°C to 125°C			150	
$I_{S(OFF)}$ $I_{D(OFF)}$	Switch State is off V_S = V_{SS} / V_{DD} V_D = V_{DD} / V_{SS}	5V	0V	25°C		±0.3	±100	nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
$I_{S(OFF)}$ $I_{D(OFF)}$	Switch State is off V_S = V_{SS} / V_{DD} V_D = V_{DD} / V_{SS}	10V	0V	25°C		±0.3	±100	nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
	Switch State is off V_S = V_{SS} / V_{DD} V_D = V_{DD} / V_{SS}	15V	0V	25°C		±0.3	±100	nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
	Switch State is off V_S = V_{SS} / V_{DD} V_D = V_{DD} / V_{SS}	5V	–5V	25°C		±0.3	±100	nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
I_{ON}	Switch State is on V_S = V_D = V_{SS} or V_{DD}	5V	0V	25°C		±0.3	±100	nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
		10V	0V	25°C		±0.3	±100	nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
		5V	–5V	25°C		±0.3	±100	nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
		15V	0V	25°C		±0.3		nA
				–55°C to 85°C			±800	nA
				–55°C to 125°C			±1000	nA
LOGIC INPUTS (ADDRESS / ENABLE pins)								
V_{IH}	Input High Voltage	All		–55°C to 125°C	1.35		V_{DD}	V
V_{IL}	Input Low Voltage	All		–55°C to 125°C	0		0.8	V
I_{IH} I_{IL}	V_{LOGIC} = 0V, 5V, or V_{DD}	All		25°C		±0.6		µA
				–55°C to 125°C	–1		1	
C_{IN}		All		25°C		2		pF

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

5.6 AC Performance Characteristics

Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = –55℃ to 125℃			UNIT
	CONDITION	V_{DD}	V_{SS}	MIN	TYP	MAX	
CAPACITANCE							
$C_{S(OFF)}$	V_S = (V_{DD} + V_{SS}) / 2V f = 1MHz	5V	–5V		3		pF
$C_{D(OFF)}$	V_S = (V_{DD} + V_{SS}) / 2V f = 1MHz	5V	–5V		6		pF
$C_{S(ON)}$ $C_{D(ON)}$	V_S = (V_{DD} + V_{SS}) / 2V f = 1MHz	5V	–5V		8		pF
DYNAMIC CHARACTERISTICS							
Bandwidth (BW) (Sine Wave Input)	V_{BIAS} = (V_{DD} + V_{SS}) / 2V_S = 200mVpp R_L = 50Ω, C_L = 5pF	+5V	–5V		600		MHz
Off Isolation Channel OFF (Sine Wave Input)	V_{BIAS} = (V_{DD} + V_{SS}) / 2V_S = 200mVpp R_L = 50Ω, C_L = 5pF f = 1MHz	+5V	–5V		–95		dB
Crosstalk (Sine Wave Input)	V_{BIAS} = (V_{DD} + V_{SS}) / 2V_S = 200mVpp R_L = 50Ω, C_L = 5pF f = 1MHz	+5V	–5V		–90		dB
Charge Injection	V_S = (V_{DD} + V_{SS}) / 2 R_S = 0Ω, C_L = 100pF	+5V	–5V		6		pC

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

5.7 Timing Characteristics

Over operating free-air temperature range, Typical at T_A = 25°C (unless otherwise noted)

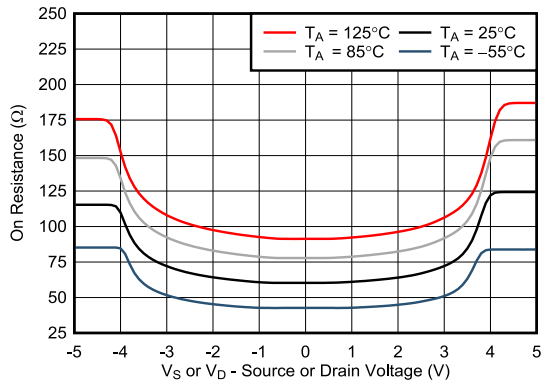
PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
		CONDITION	V_{DD}	V_{SS}	T_A				
Prop Delay	Signal Input to Signal Output	V_S = V_{SS} to V_{DD}	5V	0V	25°C		4	20	ns
			10V	0V	25°C		4	20	
			5V	–5V	25°C		4	20	
t_{TRAN}	Address-to-Signal OUT Transition time between inputs	t_r , t_f = 20ns, C_L = 50pF, R_L = 10kΩ	5V	0V	25°C		105		ns
					–55°C to +125°C			190	
			10V	0V	25°C		100		
					–55°C to +125°C			190	
			5V	–5V	25°C		100		
					–55°C to +125°C			190	
$t_{ON\ (EN)}$	Enable-to-Signal OUT Channel turning ON	t_r , t_f = 20ns, C_L = 50pF, R_L = 10kΩ	5V	0V	25°C		100		ns
					–55°C to +125°C			190	
			10V	0V	25°C		95		
					–55°C to +125°C			190	
			5V	–5V	25°C		100		
					–55°C to +125°C			190	
$t_{OFF\ (EN)}$	Enable-to-Signal OUT Channel turning OFF	t_r , t_f = 20ns, C_L = 50pF, R_L = 10kΩ	5V	0V	25°C		90		ns
					–55°C to +125°C			140	
			10V	0V	25°C		90		
					–55°C to +125°C			140	
			5V	–5V	25°C		100		
					–55°C to +125°C			160	
t_{BBM}		C_L = 15pF, R_L = 10kΩ	5V	0V	25°C		60		ns
					–55°C to +125°C	1			
			10V	0V	25°C		45		
					–55°C to +125°C	1			
		C_L = 15pF, R_L = 10kΩ	5V	–5V	25°C		45		ns
		C_L = 15pF, R_L = 10kΩ	5V	–5V	–55°C to +125°C	1			ns

ADVANCE INFORMATION

ADVANCE INFORMATION

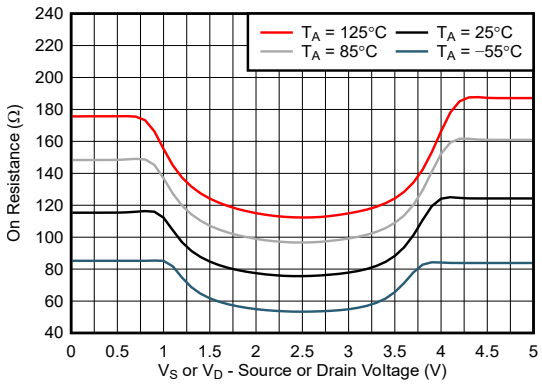
5.8 Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



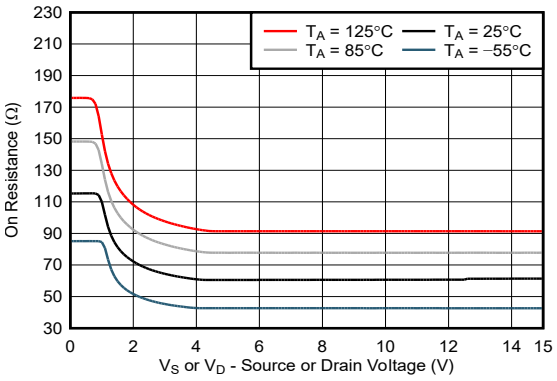
V_{DD} = 5V, V_{SS} = -5V

Figure 5-1. On-Resistance vs Temperature



V_{DD} = 5V

Figure 5-2. On-Resistance vs Temperature



V_{DD} = 15V

Figure 5-3. On-Resistance vs Temperature

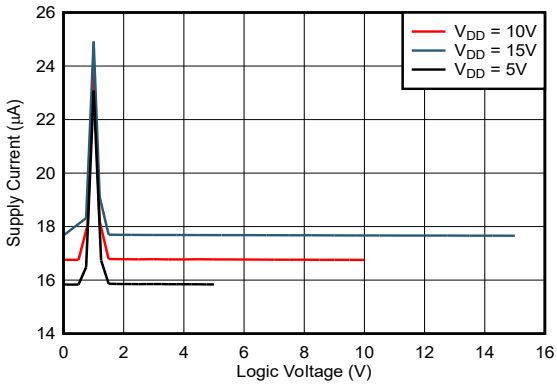
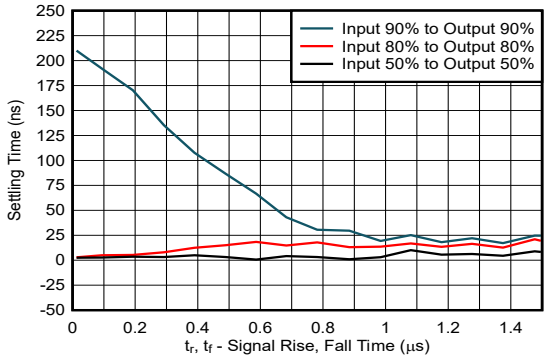
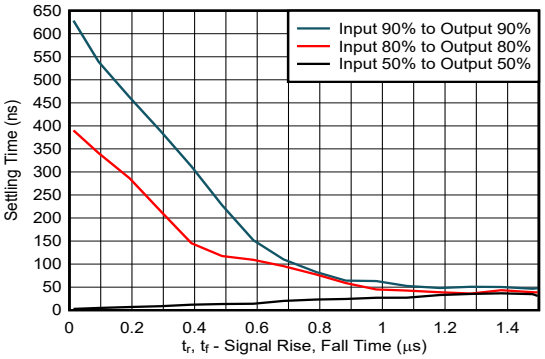


Figure 5-4. Supply Current vs Logic Voltage



V_{DD} = 5V, V_{signal} = 5V
R_L = 200kΩ, C_L = 15pF

Figure 5-5. System Settling Time



V_{DD} = 5V, V_{signal} = 5V
R_L = 10kΩ, C_L = 15pF

Figure 5-6. System Settling Time

Copyright © 2026 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)

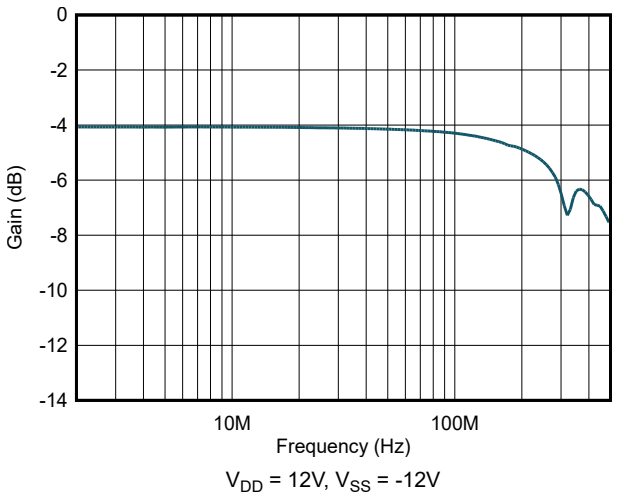


Figure 5-7. On Response vs Frequency

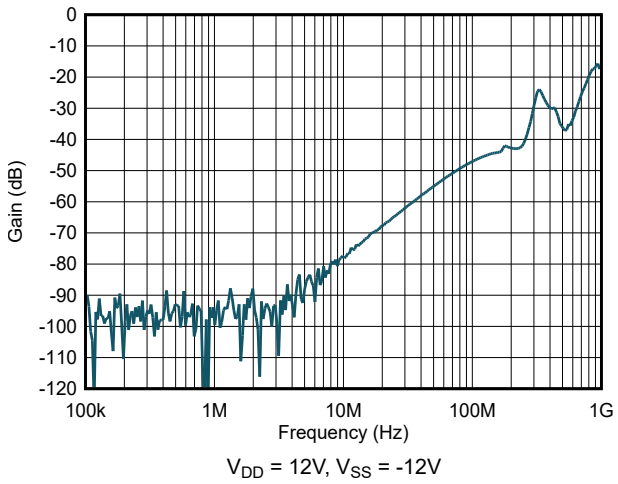


Figure 5-8. Off-Isolation vs Frequency

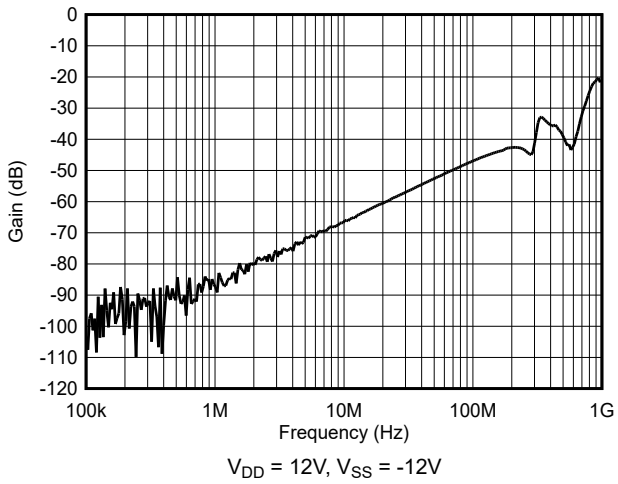


Figure 5-9. Xtalk vs Frequency

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in the following figure. Figure 6-1 shows how the R_{ON} is computed with R_{ON} = V / I_{SD}, and the voltage (V) and current (I_{SD}) are measured using this setup.

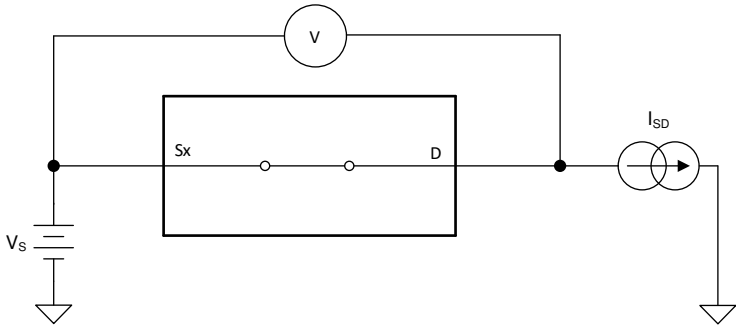


Figure 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

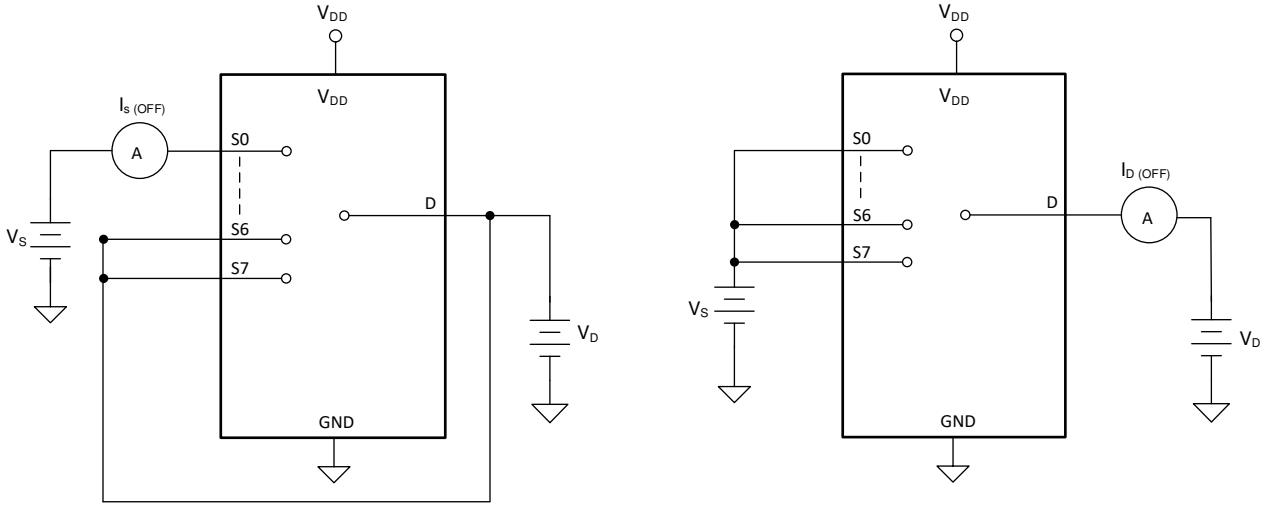


Figure 6-2. Off-Leakage Measurement Setup

Copyright © 2026 Texas Instruments Incorporated

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

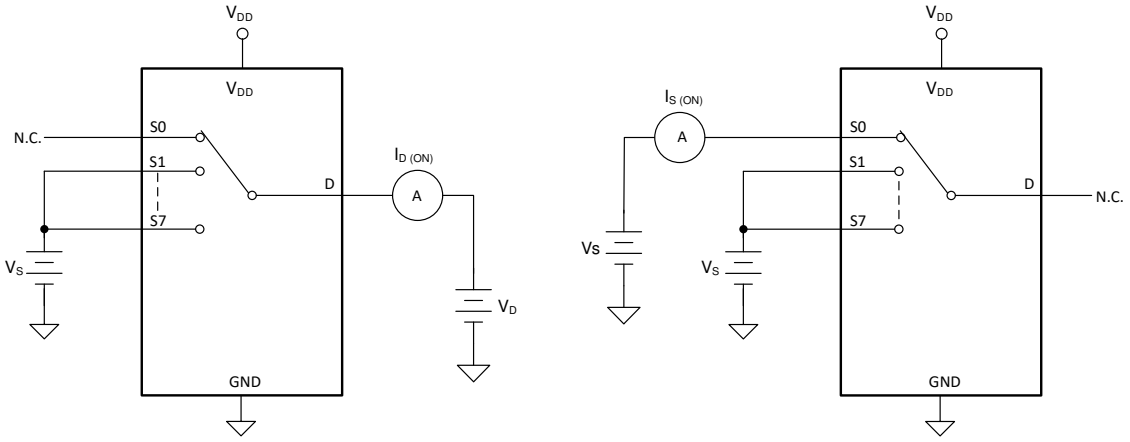


Figure 6-3. On-Leakage Measurement Setup

6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the 50% threshold. Figure 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

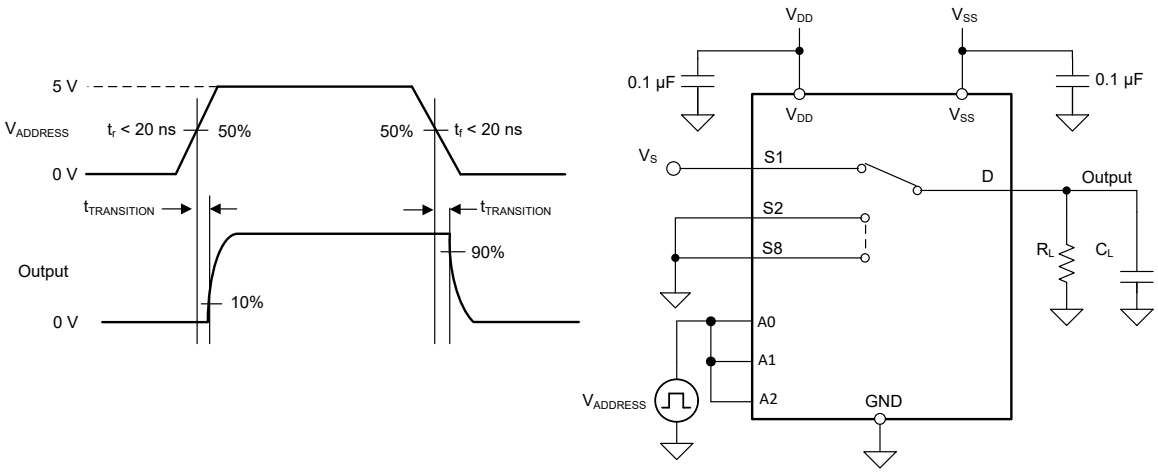


Figure 6-4. Transition-Time Measurement Setup

ADVANCE INFORMATION

ADVANCE INFORMATION

6.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

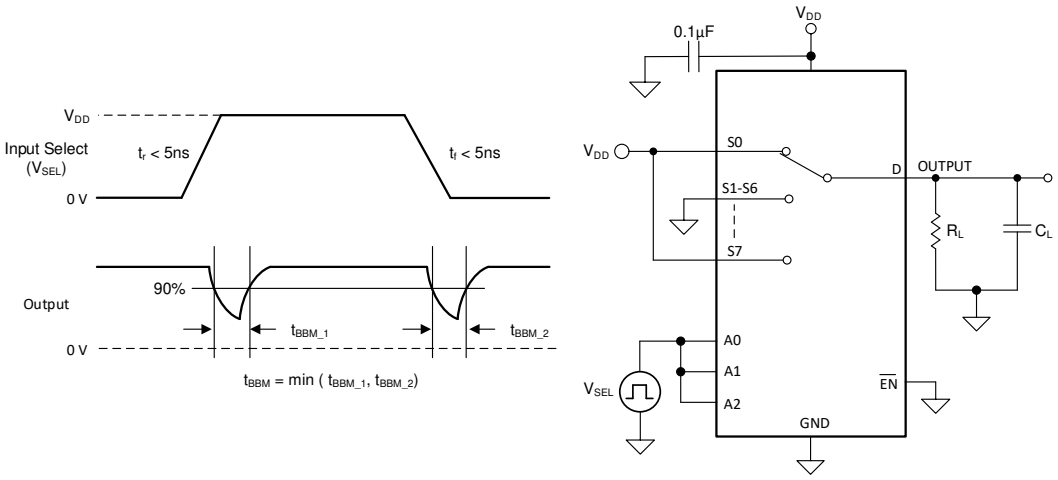


Figure 6-5. Break-Before-Make Delay Measurement Setup

6.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the 50% threshold. The 10% measurement is used to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-6 shows the setup used to measure transition time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the 50% threshold. The 90% measurement is used to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-6 shows the setup used to measure transition time, denoted by the symbol $t_{OFF(EN)}$.

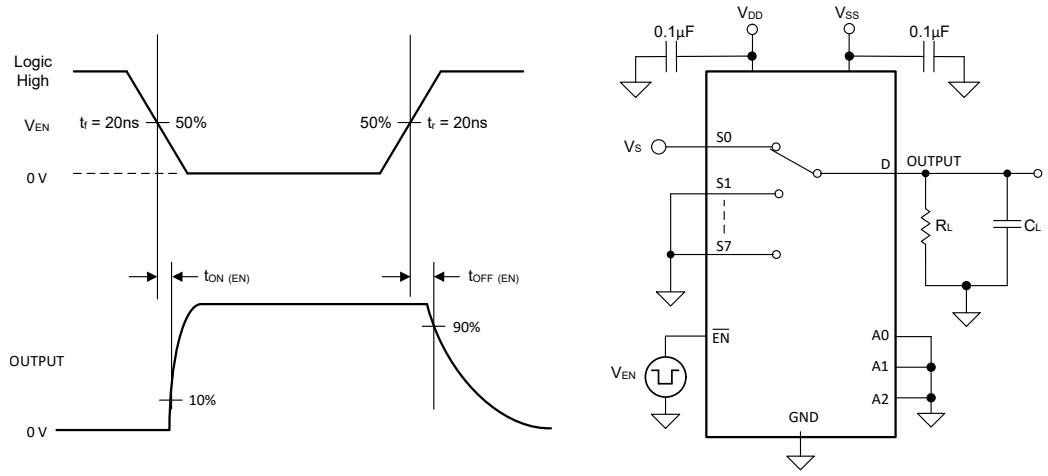


Figure 6-6. Turn-On and Turn-Off Time Measurement Setup

Copyright © 2026 Texas Instruments Incorporated

6.7 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-7 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

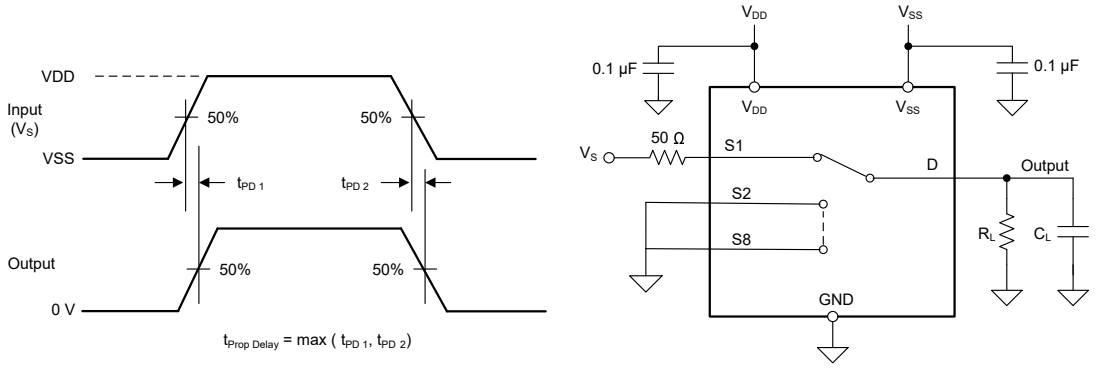


Figure 6-7. Propagation Delay Measurement Setup

6.8 Charge Injection

Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-8 shows the setup used to measure charge injection from source (Sx) to drain (D).

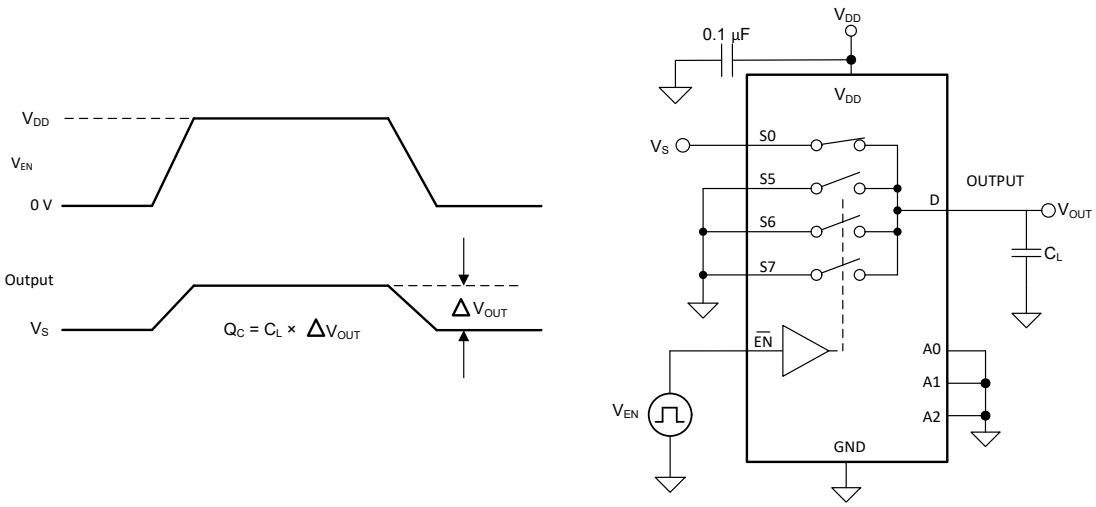


Figure 6-8. Charge-Injection Measurement Setup

ADVANCE INFORMATION

ADVANCE INFORMATION

6.9 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-9 shows the setup used to measure, and the equation to compute off isolation.

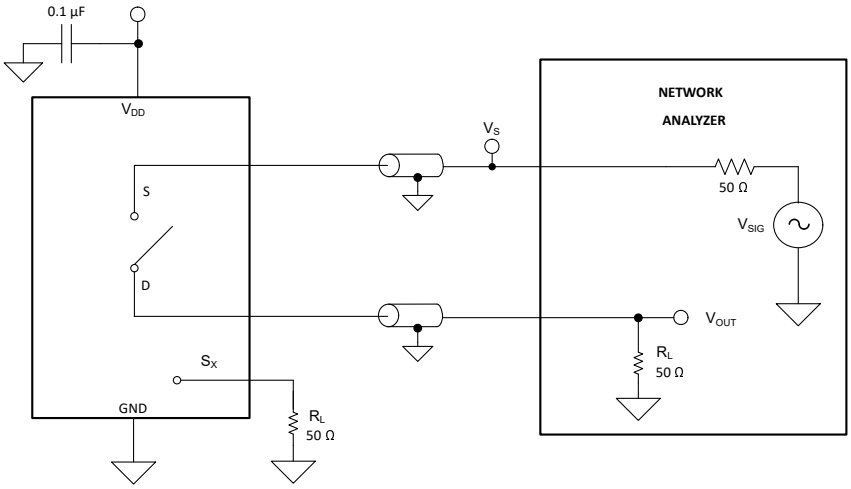


Figure 6-9. Off Isolation Measurement Setup

$$Off\ Isolation\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

6.10 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-10 shows the setup used to measure, and the equation used to compute crosstalk.

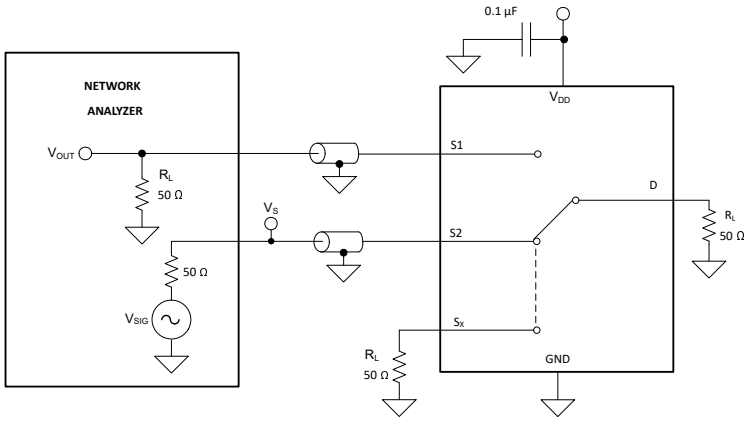


Figure 6-10. Channel-to-Channel Crosstalk Measurement Setup

$$Channel-to-Channel\ Crosstalk\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

Copyright © 2026 Texas Instruments Incorporated

6.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 6-11 shows the setup used to measure bandwidth.

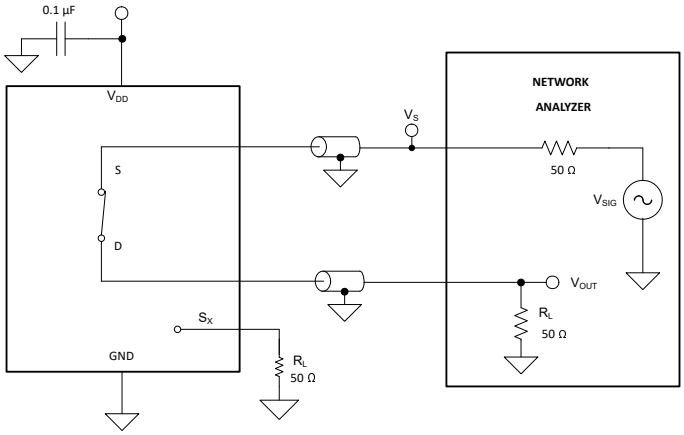


Figure 6-11. Bandwidth Measurement Setup

$$Attenuation = 20 \times Log\left(\frac{V_2}{V_1}\right) \quad (3)$$

ADVANCE INFORMATION

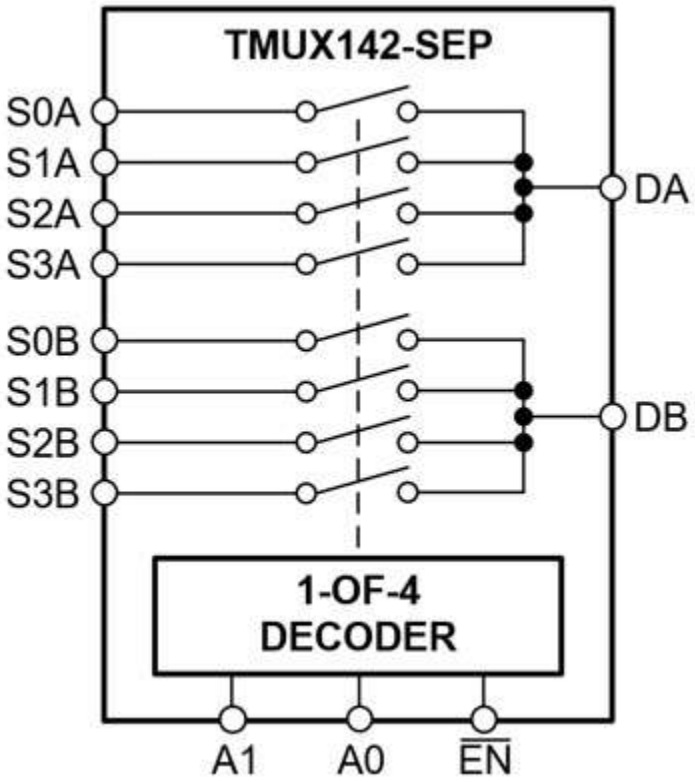
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The TMUX142-SEP is a 4:1, two-channel mux that can be used for both differential and single-ended applications. Each channel is turned on or turned off based on the state of the address lines and enable pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX142-SEP device conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions so the signal paths can be used as both multiplexers and demultiplexer to support analog signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for the TMUX142-SEP ranges from V_{SS} to V_{DD}.

7.3.3 1.8V Logic Compatible Inputs

The TMUX142-SEP support 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the multiplexers to interface with processors that have lower logic I/O rails and eliminates the need for an external voltage translator, which saves both space and BOM cost. For more information on 1.8V logic implementation, refer to Simplifying Design with 1.8V logic Muxes and Switches.

7.3.4 Device Functional Modes

When the $\overline{EN}$ pin of the device is pulled low, one of the switches is closed based on the state of the address or select pins. When the $\overline{EN}$ pin is pulled high, all the switches are in an open state regardless of the state of the address or select pins.

Copyright © 2026 Texas Instruments Incorporated

Unused logic control pins must be tied to GND or V_{DD} to be certain that the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (Sx and Dx) must be connected to GND.

7.3.5 Truth Tables

Table 7-1, provides the truth tables for the TMUX142-SEP.

Table 7-1. TMXU142-SEP Truth Table

$\overline{EN}$	A1	A0	Selected Signal Path Connected To Drain (D) Pin
0	0	0	S0A to DA S0B to DB
0	0	1	S1A to DA S1B to DB
0	1	0	S2A to DA S2B to DB
0	1	1	S3A to DA S3B to DB
1	X(1)	X(1)	All inputs are unselected (HI-Z)

(1) X denotes *do not care*.

The Enable pin, $\overline{EN}$, of the TMUX142-SEP devices have a weak internal pull-up resistor to put the devices into a disabled state upon power up. The SELx / Address pins (Ax) have weak internal pull-down resistors to put the switch into a defined logic state.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

8 Application and Implementation

Note

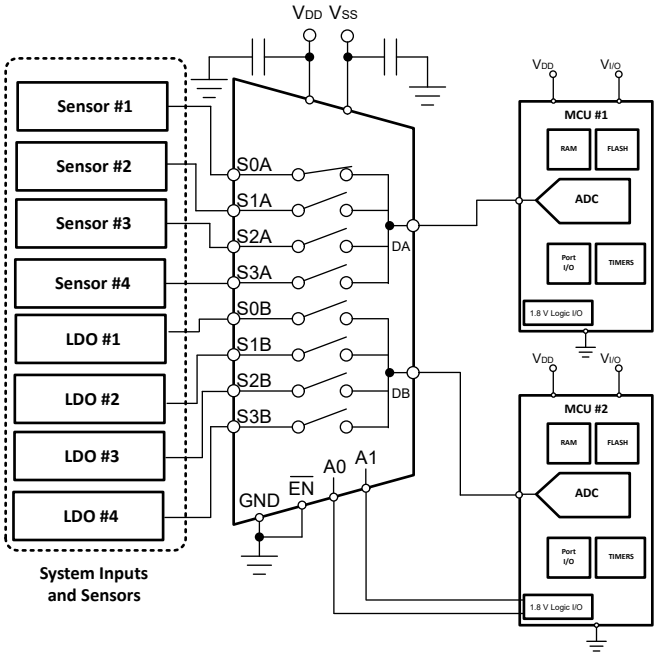
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMUX142-SEP offers good system performance across a wide operating supply (5V to 15V, ±6V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/Os. These features make the TMUX142-SEP multiplexer a good design for many systems as these features can reduce system complexity, board size, and overall system cost.

8.2 Typical Application

One useful application to take advantage of the TMUX142-SEP features is multiplexing various signals into an ADC that is integrated into an MCU. Utilizing an integrated ADC in an MCU allows a system to minimize cost with a potential tradeoff of system performance when compared to an external ADC. The multiplexer allows for multiple inputs or sensors to be monitored with a single ADC pin of the device, which is critical in systems with limited I/Os.



ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

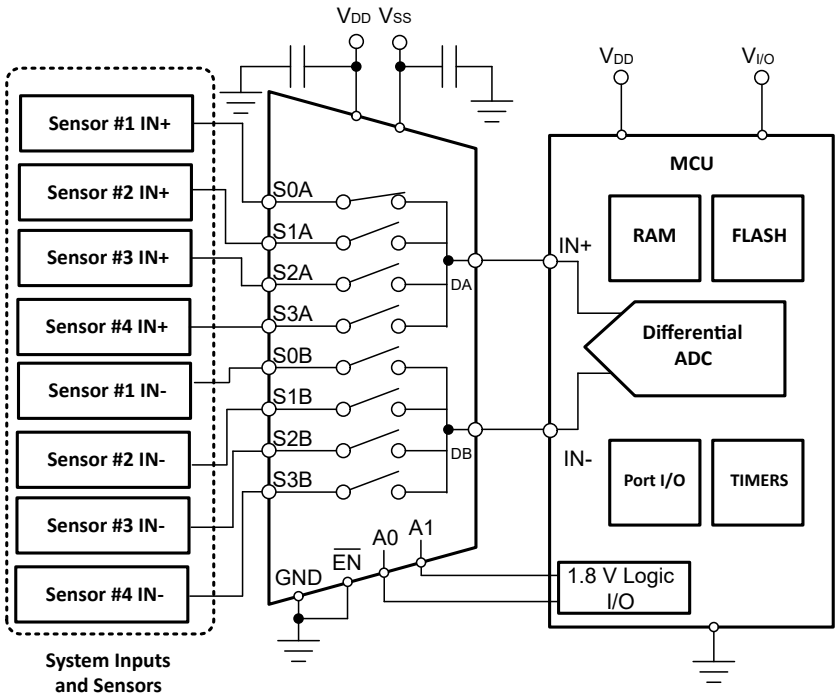


Figure 8-1. Multiplexing Signals to an Integrated ADC with TMUX142-SEP

ADVANCE INFORMATION

ADVANCE INFORMATION

8.3 Design Requirements

Table 8-1 lists the parameters that must be used for this design example.

Table 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	12V
I/O signal range	0V to V_{DD} (rail-to-rail)
Control logic thresholds	1.8V compatible

8.4 Detailed Design Procedure

The TMUX142-SEP can operate without any external components except for the supply decoupling capacitors. The MCU can control the enable and address pins through GPIOs to toggle between various inputs of the multiplexer. The enable pin ($\overline{EN}$) must be connected to power if the functionality is not required in the system. All inputs being muxed to the ADC of the MCU must fall within the *Recommended Operating Conditions*, including signal range and continuous current. For this design with a supply of 12V, the signal range can be 0V to 12V.

8.5 Application Curves

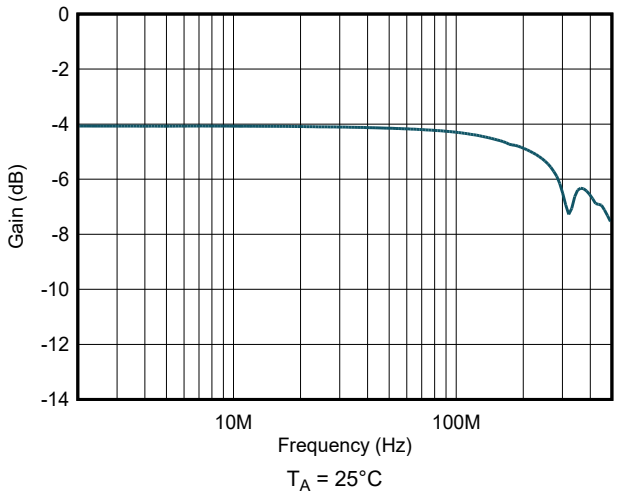


Figure 8-2. Bandwidth

8.6 Power Supply Recommendations

The TMUX142-SEP operates across a wide supply range from 5V to 15V single supply and up to ±6V dual supply.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply pins to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF from V_{DD} to ground and V_{SS} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections.

TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems or systems in harsh noise environments, avoid use of vias for connecting the capacitors to the device pins for better noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

Copyright © 2026 Texas Instruments Incorporated

8.7 Layout

8.7.1 Layout Guidelines

Route high-speed signals using minimal vias and corners, which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around Th via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

- Decouple the V_{DD} and V_{SS} pins with a 0.1µF capacitor, placed as close to the pin as possible. Verify that the capacitor voltage rating is sufficient.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

8.7.2 Layout Example

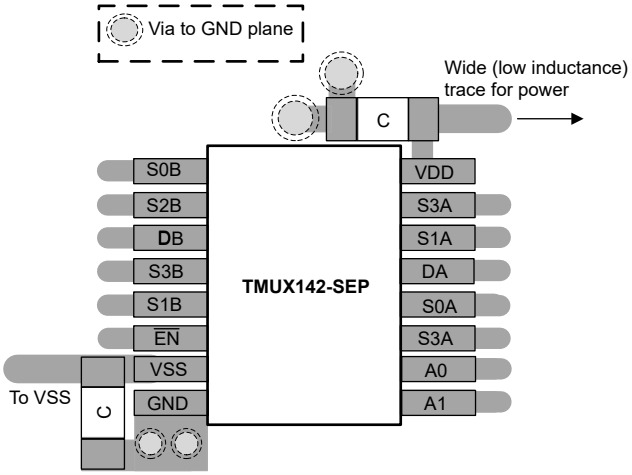


Figure 8-3. Layout Example

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

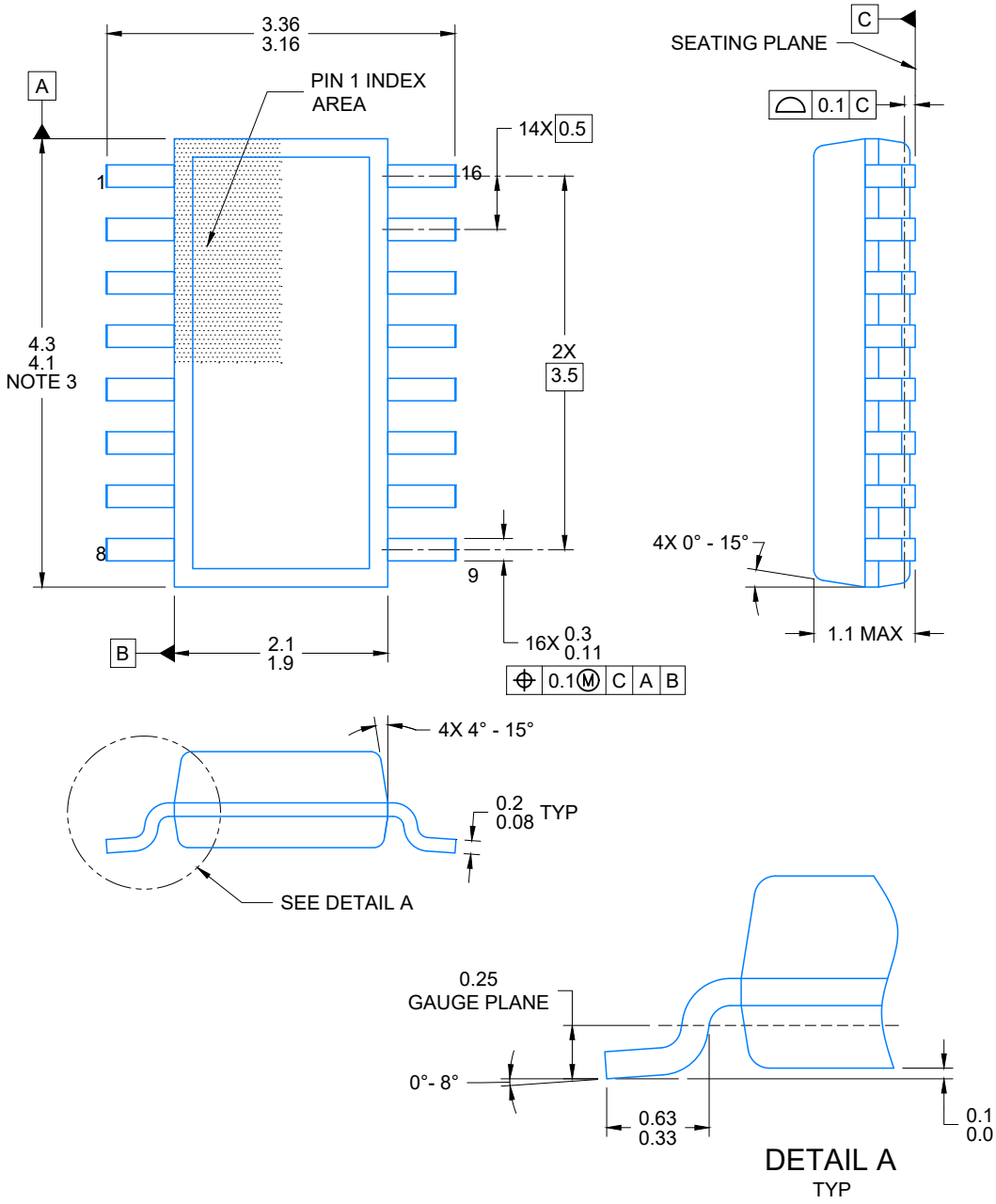
Copyright © 2026 Texas Instruments Incorporated

PACKAGE OUTLINE

DYY0016A

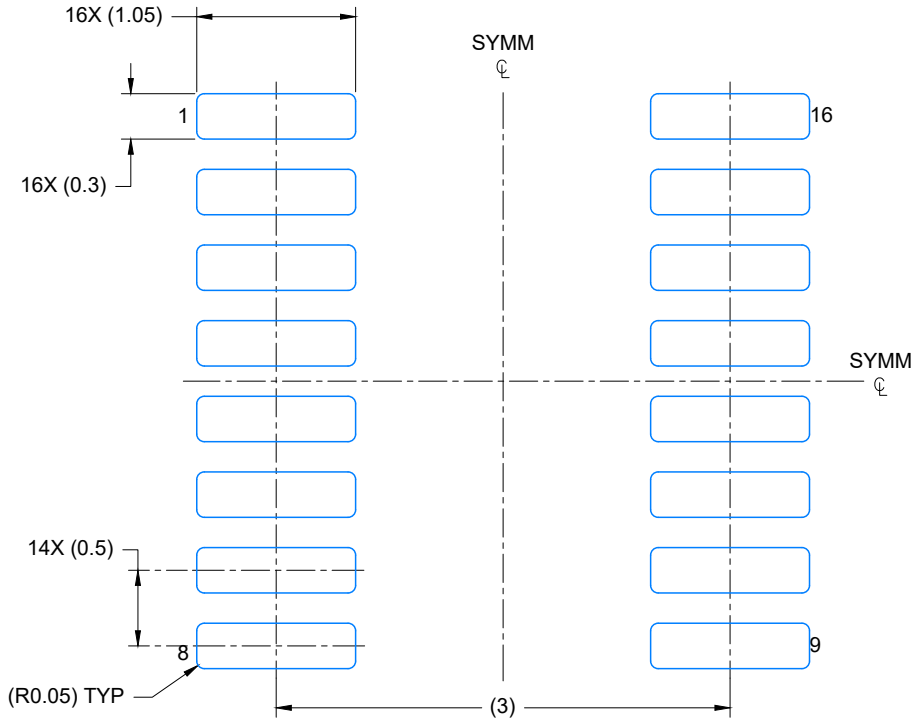
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

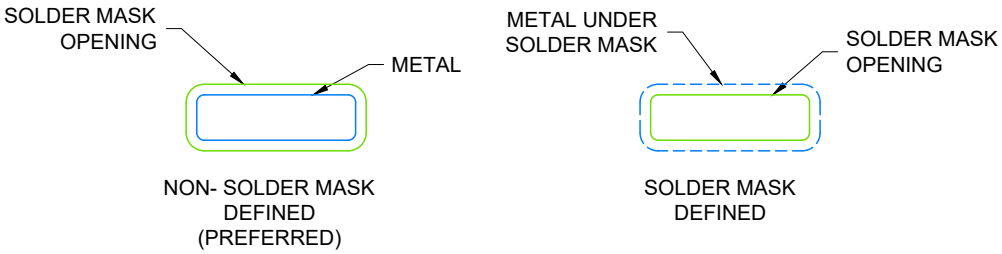


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

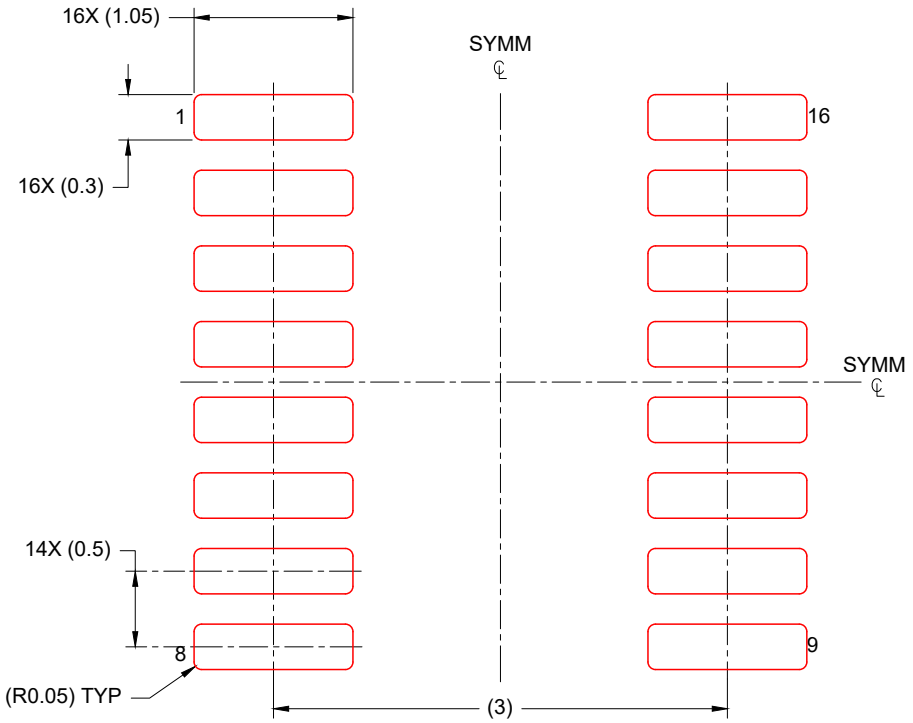
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025