# TLV902x and TLV903x Precision Comparator Family

## 1 Features

- Supply range: 1.65V to 5.5V
- Precision input offset voltage: 300µV
- Rail-to-Rail input with fault-tolerance
- Typical propagation delay: 100ns
- Low quiescent current per channel: 16µA
- Low input bias current: 5pA
- Open-drain output option (TLV902x)
- Push-pull output option (TLV903x)
- Full temperature range: -40°C to +125°C
- ESD protection: 2kV
- Alternate Single Pinout (TLV90x0)

## 2 Applications

- Appliances
- Building automation
- Factory automation and control
- Motor drives
- Infotainment and cluster

## 3 Description

The TLV902x and TLV903x are a family of single, dual and quad channel comparators. The family offers low input offset voltage, fault-tolerant inputs and a excellent speed-to-power combination. The family has a propagation delay of 100ns with a quiescent supply current of only 18µA per channel.

These comparators feature fault-tolerant inputs that can go up to 6V without damage and with no output phase inversion. This family of comparators is designed for precision voltage monitoring in harsh, noisy environments.

The TLV902x have an open-drain output that can be pulled-up below or beyond the supply voltage. These devices are designed for low voltage logic translators.

The TLV903x have a push-pull output stage capable of sinking and sourcing many milliamps of current to drive LEDs or capacitive loads for MOSFET gates.

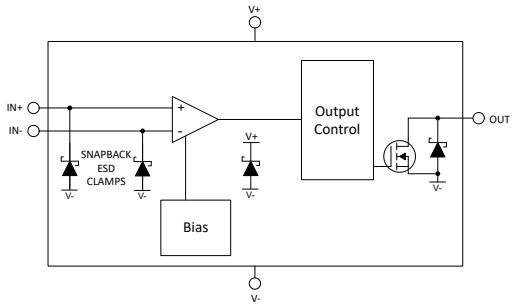
The TLV90x0 and TLV90x1 are alternate pinouts of the single device.

The family is specified for the Industrial temperature range of -40°C to +125°C and are available in a standard leaded and leadless packages.

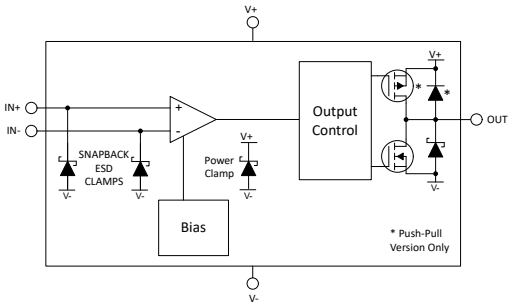
**Package Information**

| PART NUMBER | PACKAGE (1) | PACKAGE SIZE(2) |
|---|---|---|
| TLV90x0<br>TLV90x1<br>(Single) | DCK (SC-70, 5) | 1.25mm × 2.00mm |
| | DBV (SOT-23, 5) | 1.60mm × 2.90mm |
| TLV9022<br>TLV9032<br>(Dual) | D (SOIC, 8) | 3.91mm × 4.90mm |
| | PW (TSSOP, 8) | 3.00mm × 4.40mm |
| | DGK (VSSOP, 8) | 3.00mm × 3.00mm |
| | DSG (WSON, 8) | 2.00mm × 2.00mm |
| | DDF (SOT-23, 8) | 1.60mm × 2.90mm |
| TLV9024<br>TLV9034<br>(Quad) | D (SOIC, 14) | 3.91mm × 8.65mm |
| | PW (TSSOP, 14) | 4.40mm × 5.00mm |
| | (SOT-23, 14) | 4.20mm × 2.00mm |
| | RTE (WQFN, 16) | 3.00mm × 3.00mm |
| | RUC (X2QFN, 14) | 2.00mm × 2.00mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**TLV902x Block Diagram**




**TLV903x Block Diagram**

# Table of Contents

# 4 Pin Configuration and Functions

## 4.1 Pin Functions: TLV90x0 and TLV90x1 Single

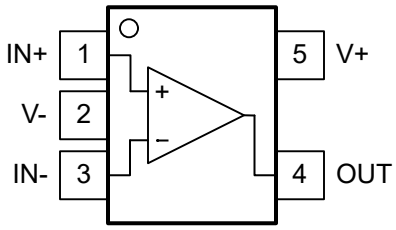



**Figure 4-1. TLV9020, TLV9030 DCK and DBV Packages**
**Standard *South East* Pinout**
**5-Pin SC-70 and SOT-23**
**Top View**

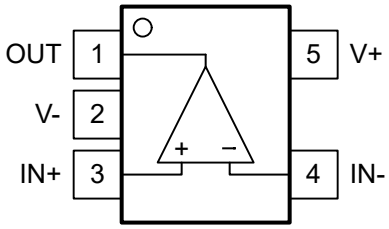



**Figure 4-2. TLV9021, TLV9031 DCK and DBV Packages**
**Standard *North West* Pinout**
**5-Pin SC-70 and SOT-23**
**Top View**

**Table 4-1. Pin Functions: TLV90x0 and TLV90x1**

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| | TLV90x0 | TLV90x1 | | |
| NAME | NO. | NO. | | |
| IN+ | 1 | 3 | I | Non-Inverting (Positive) Input |
| IN– | 3 | 4 | I | Inverting (Negative) Input |
| OUT | 4 | 1 | O | Output |
| V+ | 5 | 5 | — | Positive Power Supply |
| V- | 2 | 2 | — | Negative Power Supply |

(1) I = Input, O = Output

## 4.2 Pin Functions: TLV90x2 Dual

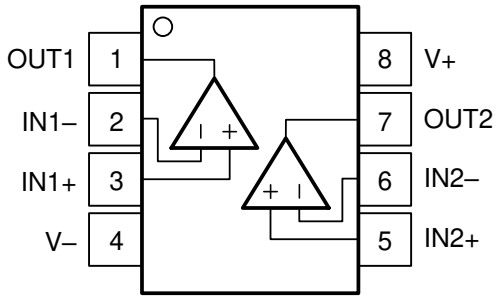
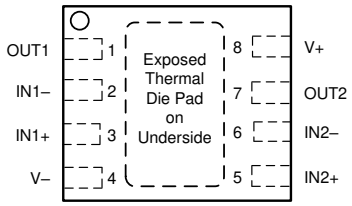



**Figure 4-3. D, DGK, PW, DDF Packages**
**8-Pin SOIC, VSSOP, TSSOP, SOT-23-8**
**Top View**




NOTE: Connect exposed thermal pad directly to V- pin.

**Figure 4-4. DSG Package**
**8-Pad WSON With Exposed Thermal Pad**
**Top View**

**Table 4-2. Pin Functions: TLV90x2**

| PIN | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN1– | 2 | I | Inverting input pin of comparator 1 |
| IN1+ | 3 | I | Noninverting input pin of comparator 1 |
| IN2– | 6 | I | Inverting input pin of comparator 2 |
| IN2+ | 5 | I | Noninverting input pin of comparator 2 |
| OUT1 | 1 | O | Output pin of the comparator 1 |
| OUT2 | 7 | O | Output pin of the comparator 2 |
| Thermal Pad | — | — | Connect directly to V- pin |
| V– | 4 | — | Negative (low) supply |
| V+ | 8 | — | Positive supply |

(1) I = input, O = output

## 4.3 Pin Functions: TLV90x4 Quad

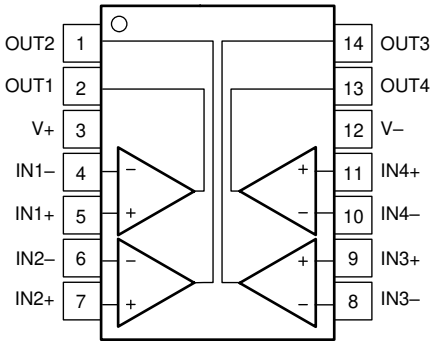



**Figure 4-5. D, PW, DYY Package, 14-Pin SOIC, TSSOP, SOT-23, Top View**

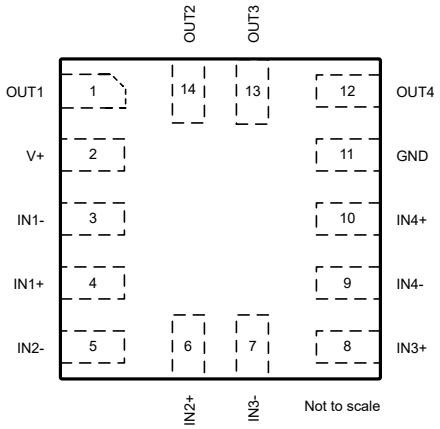
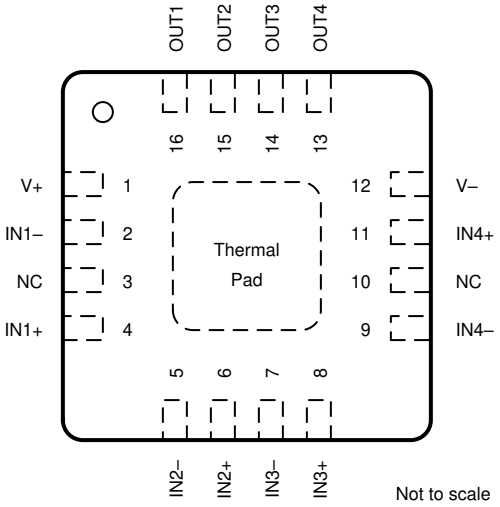



**Figure 4-6. RUC Package, 14-Pin X2QFN, Top View**




NOTE: Connect exposed thermal pad directly to V- pin.

**Figure 4-7. RTE Package, 16-Pad WQFN With Thermal Pad, Top View**

**Table 4-3. Pin Functions: TLV90x4**

| PIN | | | | TYPE[2] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME [1] | SOIC | X2QFN | WQFN | | |
| IN1– | 4 | 3 | 2 | I | Negative input pin of the comparator 1 |
| IN1+ | 5 | 4 | 4 | I | Positive input pin of the comparator 1 |
| IN2– | 6 | 5 | 5 | I | Negative input pin of the comparator 2 |
| IN2+ | 7 | 6 | 6 | I | Positive input pin of the comparator 2 |
| IN3– | 8 | 7 | 7 | I | Negative input pin of the comparator 3 |
| IN3+ | 9 | 8 | 8 | I | Positive input pin of the comparator 3 |
| IN4– | 10 | 9 | 9 | I | Negative input pin of the comparator 4 |
| IN4+ | 11 | 10 | 11 | I | Positive input pin of the comparator 4 |
| NC | — | — | 3 | — | No Internal Connection - Leave floating or GND |

**Table 4-3. Pin Functions: TLV90x4 (continued)**

| PIN | | | | TYPE[2] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME [1] | SOIC | X2QFN | WQFN | | |
| NC | — | — | 10 | — | No Internal Connection - Leave floating or GND |
| OUT1 | 2 | 1 | 16 | O | Output pin of the comparator1 |
| OUT2 | 1 | 14 | 15 | O | Output pin of the comparator 2 |
| OUT3 | 14 | 13 | 14 | O | Output pin of the comparator 3 |
| OUT4 | 13 | 12 | 13 | O | Output pin of the comparator 4 |
| Thermal Pad | — | — | PAD | — | Connect directly to V- pin. |
| V– | 12 | 11 | 12 | — | Negative supply |
| V+ | 3 | 2 | 1 | — | Positive supply |

(1) Some manufacturers transpose the names of channels 1 and 2. Electrically the pinouts are identical, just a difference in channel naming convention.
(2) I = input, O = output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_S$ = (V+) – (V–) | –0.3 | 6 | V |
| Input pins | (IN+, IN–) from V–(2) | –0.3 | 6 | V |
| Current into Input pins | (IN+, IN–) | –10 | 10 | mA |
| Output | (OUT) from V–, open drain only(3) | –0.3 | 6 | V |
| Output | (OUT) from V–, push-pull only | –0.3 | (V+) + 0.3 | V |
| Output | short circuit duration(4) | | 10 | s |
| Junction temperature | $T_J$ | | 150 | °C |
| Storage temperature | $T_{stg}$ | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less. Additionally, Inputs (IN+, IN–) can be greater than V+ and OUT as long as the input is within the –0.3V to 6V range
(3) Output (OUT) for open drain can be greater than V+ and inputs (IN+, IN–) as long as the pins are within the –0.3V to 6V range
(4) Short-circuit to V– or V+. Short circuits from outputs can cause excessive heating and eventual destruction.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_S$ = (V+) – (V–) | 1.65 | 5.5 | V |
| Input voltage range | (IN+, IN–) from (V–) | –0.2 | 5.7 | V |
| Ambient temperature | $T_A$ | –40 | 125 | °C |

## 5.4 Thermal Information, TLV90x0,TLV90x1

| THERMAL METRIC (1) | | TLV90x0,TLV90x1 | | UNIT |
|---|---|---|---|---|
| | | DCK (SC-70) | DBV (SOT-23) | |
| | | 5 PINS | 5 PINS | |
| $R_{qJA}$ | Junction-to-ambient thermal resistance | 238.5 | 223.7 | °C/W |
| $R_{qJC(top)}$ | Junction-to-case (top) thermal resistance | 134.0 | 123.2 | °C/W |
| $R_{qJB}$ | Junction-to-board thermal resistance | 87.6 | 91.4 | °C/W |
| $y_{JT}$ | Junction-to-top characterization parameter | 59.1 | 58.7 | °C/W |
| $y_{JB}$ | Junction-to-board characterization parameter | 87.2 | 91.0 | °C/W |
| $R_{qJC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.5 Thermal Information, TLV90x2

| THERMAL METRIC (1) | | TLV90x2 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | DGK (VSSOP) | DSG (WSON) | DDF (SOT-23) | |
| | | 8 PINS | 8 PINS | 8 PINS | 8 PINS | 8 PINS | |
| $R_{qJA}$ | Junction-to-ambient thermal resistance | 167.7 | 221.7 | 215.8 | 175.2 | 240.0 | °C/W |
| $R_{qJC(top)}$ | Junction-to-case (top) thermal resistance | 107.0 | 109.1 | 105.2 | 178.1 | 151.0 | °C/W |
| $R_{qJB}$ | Junction-to-board thermal resistance | 111.2 | 152.5 | 137.5 | 139.5 | 157.0 | °C/W |
| $y_{JT}$ | Junction-to-top characterization parameter | 53.1 | 36.4 | 39.6 | 47.2 | 32.8 | °C/W |
| $y_{JB}$ | Junction-to-board characterization parameter | 110.4 | 150.7 | 135.9 | 138.9 | 155.4 | °C/W |
| $R_{qJC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | – | – | 127.3 | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.6 Thermal Information, TLV90x4

| THERMAL METRIC(1) | | TLV90x4 | TLV90x4 | TLV90x4 | TLV90x4 | TLV90x4 | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | RUC (X2QFN) | RTE (WQFN) | DYY (SOT-23) | |
| | | 14 PINS | 14 PINS | 14 PINS | 16 PINS | 14 PINS | |
| $R_{qJA}$ | Junction-to-ambient thermal resistance | 136.0 | 155.0 | 215.0 | 134.1 | 211.1 | °C/W |
| $R_{qJC(top)}$ | Junction-to-case (top) thermal resistance | 91.2 | 82.0 | 77.5 | 122.6 | 121.1 | °C/W |
| $R_{qJB}$ | Junction-to-board thermal resistance | 92.0 | 98.5 | 160.3 | 109.3 | 120.4 | °C/W |
| $y_{JT}$ | Junction-to-top characterization parameter | 46.9 | 25.7 | 10.0 | 30.9 | 22.3 | °C/W |
| $y_{JB}$ | Junction-to-board characterization parameter | 91.6 | 97.6 | 160.1 | 108.3 | 120.1 | °C/W |
| $R_{qJC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | – | - | 98.7 | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.7 Electrical Characteristics, TLV90x0,TLV90x1

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5V, $V_{CM}$ = (V–) at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V | –1.5 | ±0.3 | 1.5 | mV |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | –2 | | 2 | |
| $dV_{IO}/dT$ | Input offset voltage drift | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | | ±0.5 | | µV/°C |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current | $V_S$ = 1.8V and 5V, No Load, Output Low | | 17.1 | 30 | µA |
| $I_Q$ | Quiescent current | $V_S$ = 1.8V and 5V, No Load, Output Low, $T_A$ = –40°C to +125°C | | | 35 | |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C (push-pull verison) | 75 | 95 | | dB |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C (open drain version) | 80 | 95 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $V_{CM}$ = $V_S$/2 | | 5 | | pA |
| $I_{OS}$ | Input offset current | $V_{CM}$ = $V_S$/2 | | 1 | | pA |
| **INPUT CAPACITANCE** | | | | | | |
| $C_{ID}$ | Input Capacitance, Differential | $V_{CM}$ = $V_S$/2 | | 2 | | pF |
| $C_{IC}$ | Input Capacitance, Common Mode | $V_{CM}$ = $V_S$/2 | | 3 | | pF |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM-Range}$ | Common-mode voltage range | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | (V–) – 0.2 | | (V+) + 0.2 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 5V, (V–) – 0.2V < $V_{CM}$ < (V+) + 0.2V, $T_A$ = –40°C to +125°C | 60 | 70 | | dB |
| CMRR | Common-mode rejection ratio | $V_S$ = 1.8V, (V–) – 0.2V < $V_{CM}$ < (V+) + 0.2V, $T_A$ = –40°C to +125°C | 50 | 60 | | dB |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{VD}$ | Large signal differential voltage amplification | For open drain version only | 50 | 200 | | V/mV |
| **OUTPUT** | | | | | | |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = 25°C | | 75 | 125 | mV |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = –40°C to +125°C | | | 175 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = 25°C (push-pull only) | | 75 | 125 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = –40°C to +125°C (push-pull only) | | | 175 | mV |
| $I_{LKG}$ | Open-drain output leakage current | $V_{PULLUP}$ = (V+), $T_A$ = 25°C (open drain only) | | 100 | | pA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sinking | 90 | 100 | | mA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sourcing (push-pull only) | 90 | 100 | | mA |

## 5.8 Switching Characteristics, TLV90x0,TLV90x1

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5V, $V_{CM}$ = $V_S$ / 2, $C_L$ = 15pF at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $T_{PD-HL}$ | Propagation delay time, high-to-low | $V_{ID}$ = –100mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5KΩ for open drain only) | | 100 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100mV; Delay from mid-point of input to mid-point of output (for push-pull only) | | 115 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5KΩ for open drain only) | | 150 | | ns |
| $T_{FALL}$ | 5V Output Fall Time, 80% to 20% | $V_{ID}$ = –100mV | | 3 | | ns |
| $T_{RISE}$ | 5V Output Rise Time, 20% to 80% | $V_{ID}$ = 100mV (for push-pull only) | | 3 | | ns |
| $F_{TOGGLE}$ | 5V, Toggle Frequency | $V_{ID}$ = 100mV ($R_P$ = 2.5KΩ for open drain only) | | 3 | | MHz |
| **POWER ON TIME** | | | | | | |
| $P_{ON}$ | Power on-time | $V_S$ = 1.8V and 5V, $V_{CM}$ = (V–), $V_{ID}$ = –0.1V, $V_{PULL-UP}$ = $V_S$ / 2, Delay from $V_S$ / 2 to $V_{OUT}$ = 0.1x $V_S$ / 2 ($R_P$ = 2.5KΩ for open drain only) | | 20 | | µs |

## 5.9 Electrical Characteristics, TLV90x2

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5V, $V_{CM}$ = (V–) at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V | –1.5 | ±0.3 | 1.5 | mV |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | –2 | | 2 | |
| $dV_{IO}/dT$ | Input offset voltage drift | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | | ±0.5 | | µV/°C |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current per comparator | $V_S$ = 1.8V and 5V, No Load, Output Low | | 16 | 30 | µA |
| $I_Q$ | Quiescent current per comparator | $V_S$ = 1.8V and 5V, No Load, Output Low, $T_A$ = –40°C to +125°C | | | 35 | |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C, (push-pull verison) | 75 | 95 | | dB |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C (open drain version) | 80 | 95 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $V_{CM}$ = $V_S$/2 | | 5 | | pA |
| $I_{OS}$ | Input offset current | $V_{CM}$ = $V_S$/2 | | 1 | | pA |
| **INPUT CAPACITANCE** | | | | | | |
| $C_{ID}$ | Input Capacitance, Differential | $V_{CM}$ = $V_S$/2 | | 2 | | pF |
| $C_{IC}$ | Input Capacitance, Common Mode | $V_{CM}$ = $V_S$/2 | | 3 | | pF |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM\text{-}Range}$ | Common-mode voltage range | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | (V–) – 0.2 | | (V+) + 0.2 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 5V, (V–) – 0.2V < $V_{CM}$ < (V+) + 0.2V, $T_A$ = –40°C to +125°C | 60 | 70 | | dB |
| CMRR | Common-mode rejection ratio | $V_S$ = 1.8V, (V–) – 0.2V < $V_{CM}$ < (V+) + 0.2V, $T_A$ = –40°C to +125°C | 50 | 60 | | dB |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{VD}$ | Large signal differential voltage amplification | For open drain version only | 50 | 200 | | V/mV |
| **OUTPUT** | | | | | | |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = 25°C | | 75 | 125 | mV |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = –40°C to +125°C | | | 175 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = 25°C (push-pull only) | | 75 | 125 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = –40°C to +125°C (push-pull only) | | | 175 | mV |
| $I_{LKG}$ | Open-drain output leakage current | $V_{PULLUP}$ = (V+), $T_A$ = 25°C (open drain only) | | 100 | | pA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sinking | 90 | 100 | | mA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sourcing (push-pull only) | 90 | 100 | | mA |

## 5.10 Switching Characteristics, TLV90x2

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5V, $V_{CM}$ = $V_S$ / 2, $C_L$ = 15pF at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $T_{PD-HL}$ | Propagation delay time, high-to-low | $V_{ID}$ = –100mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5kΩ for open drain only) | | 100 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100mV; Delay from mid-point of input to mid-point of output (for push-pull only) | | 115 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5kΩ for open drain only) | | 150 | | ns |
| $T_{FALL}$ | 5V Output Fall Time, 80% to 20% | $V_{ID}$ = –100mV | | 3 | | ns |
| $T_{RISE}$ | 5V Output Rise Time, 20% to 80% | $V_{ID}$ = 100mV (for push-pull only) | | 3 | | ns |
| $F_{TOGGLE}$ | 5V, Toggle Frequency | $V_{ID}$ = 100mV ($R_P$ = 2.5kΩ for open drain only) | | 3 | | MHz |
| **POWER ON TIME** | | | | | | |
| $P_{ON}$ | Power on-time | $V_S$ = 1.8V and 5V, $V_{CM}$ = (V–), $V_{ID}$ = –0.1V, $V_{PULL-UP}$ = $V_S$ / 2, Delay from $V_S$ / 2 to $V_{OUT}$ = 0.1x $V_S$ / 2 ($R_P$ = 2.5kΩ for open drain only) | | 20 | | µs |

## 5.11 Electrical Characteristics, TLV90x4

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5V, $V_{CM}$ = (V–) at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V | –1.5 | ±0.3 | 1.5 | mV |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | –2 | | 2 | |
| $dV_{IO}/dT$ | Input offset voltage drift | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | | ±0.5 | | µV/°C |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current per comparator | $V_S$ = 1.8V and 5V, No Load, Output Low | | 16 | 30 | µA |
| $I_Q$ | Quiescent current per comparator | $V_S$ = 1.8V and 5V, No Load, Output Low, $T_A$ = –40°C to +125°C | | | 35 | |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C, (push-pull version) | | | 177.8 | µV/V |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C, (push-pull version) | 75 | 95 | | dB |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C, (open drain version) | | | 100 | µV/V |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –40°C to +125°C, (open drain version) | 80 | 95 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $V_{CM}$ = $V_S$/2 | | 5 | | pA |
| $I_{OS}$ | Input offset current | $V_{CM}$ = $V_S$/2 | | 1 | | pA |
| **INPUT CAPACITANCE** | | | | | | |
| $C_{ID}$ | Input Capacitance, Differential | $V_{CM}$ = $V_S$/2 | | 2 | | pF |
| $C_{IC}$ | Input Capacitance, Common Mode | $V_{CM}$ = $V_S$/2 | | 3 | | pF |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM\text{-}Range}$ | Common-mode voltage range | $V_S$ = 1.8V and 5V, $T_A$ = –40°C to +125°C | (V–) – 0.2 | | (V+) + 0.2 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 5V, (V–) – 0.2V < $V_{CM}$ < (V+) + 0.2V, $T_A$ = –40°C to +125°C | 60 | 70 | | dB |
| CMRR | Common-mode rejection ratio | $V_S$ = 1.8V, (V–) – 0.2V < $V_{CM}$ < (V+) + 0.2V, $T_A$ = –40°C to +125°C | 50 | 60 | | dB |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{VD}$ | Large signal differential voltage amplification | For open-drain version only | 50 | 200 | | V/mV |
| **OUTPUT** | | | | | | |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = 25°C | | 75 | 125 | mV |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = –40°C to +125°C | | | 175 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = 25°C (push-pull only) | | 75 | 125 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = –40°C to +125°C (push-pull only) | | | 175 | mV |
| $I_{LKG}$ | Open-drain output leakage current | $V_{PULLUP}$ = (V+), $T_A$ = 25°C (open drain only) | | 100 | | pA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sinking | 90 | 100 | | mA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sourcing (push-pull only) | 90 | 100 | | mA |

## 5.12 Switching Characteristics, TLV90x4

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5 V, $V_{CM}$ = $V_S$ / 2, $C_L$ = 15 pF at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $T_{PD-HL}$ | Propagation delay time, high-to-low | $V_{ID}$ = –100 mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5 KΩ for open drain only) | | 100 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100 mV; Delay from mid-point of input to mid-point of output (for push-pull only) | | 115 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100 mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5 KΩ for open drain only) | | 150 | | ns |
| $T_{FALL}$ | 5V Output Fall Time, 80% to 20% | $V_{ID}$ = –100 mV | | 3 | | ns |
| $T_{RISE}$ | 5V Output Rise Time, 20% to 80% | $V_{ID}$ = 100 mV, for push-pull only | | 3 | | ns |
| $F_{TOGGLE}$ | 5V, Toggle Frequency | $V_{ID}$ = 100 mV ($R_P$ = 2.5 KΩ for open drain only) | | 3 | | MHz |
| **POWER ON TIME** | | | | | | |
| $P_{ON}$ | Power on-time | $V_S$ = 1.8 V and 5 V, $V_{CM}$ = (V–), $V_{ID}$ = –0.1 V, $V_{PULL-UP}$ = $V_S$ / 2, Delay from $V_S$ / 2 to $V_{OUT}$ = 0.1 x $V_S$ / 2 ($R_P$ = 2.5 KΩ for open drain only) | | 30 | | µs |

## 5.13 Typical Characteristics

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

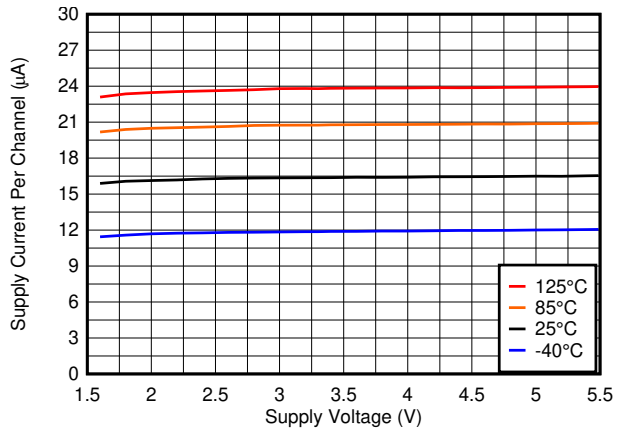



**Figure 5-1. Supply Current vs. Supply Voltage**

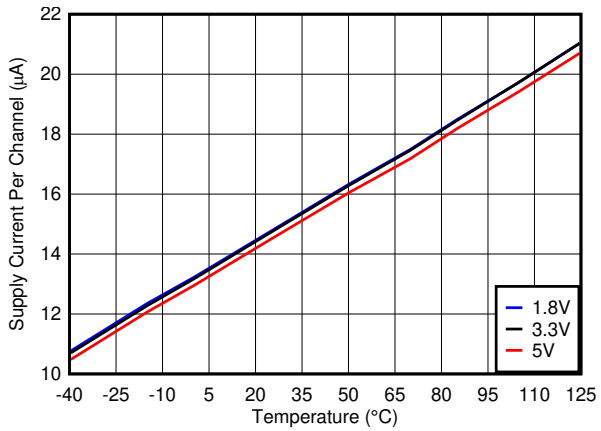



**Figure 5-2. Supply Current vs. Temperature**

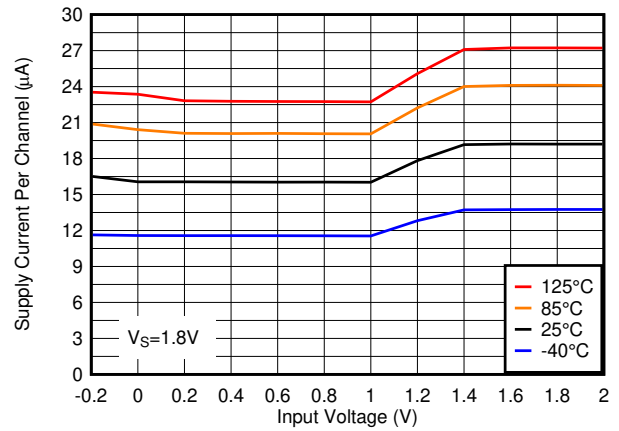



**Figure 5-3. Supply Current vs. Input Voltage, 1.8V**

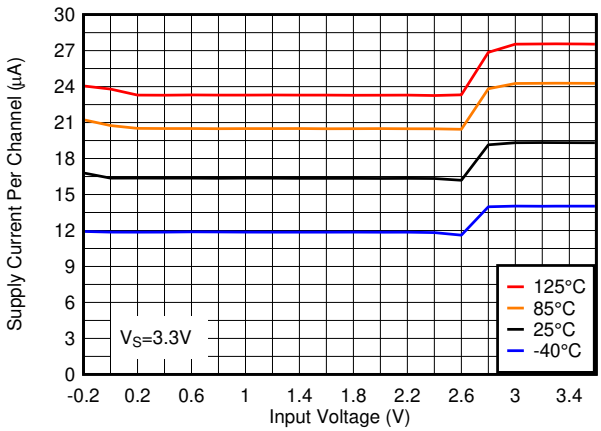



**Figure 5-4. Supply Current vs. Input Voltage, 3.3V**

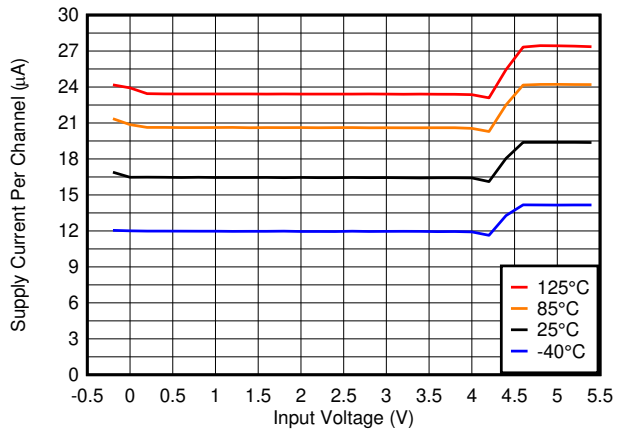



**Figure 5-5. Supply Current vs. Input Voltage, 5V**

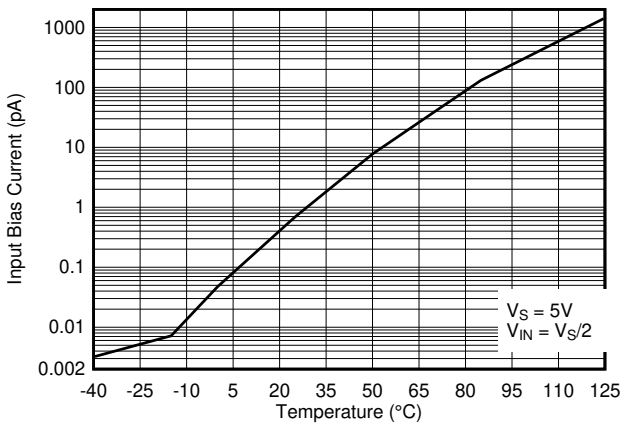



**Figure 5-6. Input Bias Current vs. Temperature**

## 5.13 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

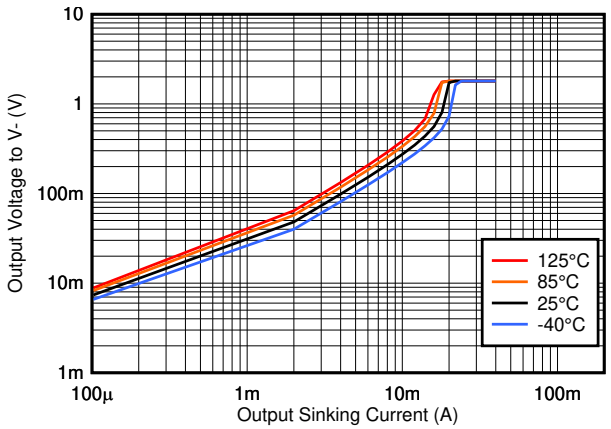



**Figure 5-7. Output Sinking Current vs. Output Voltage, 1.8V**

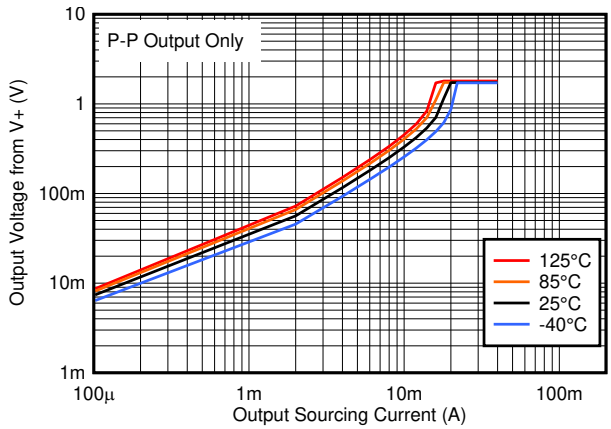



**Figure 5-8. Output Sourcing Current vs. Output Voltage, 1.8V**

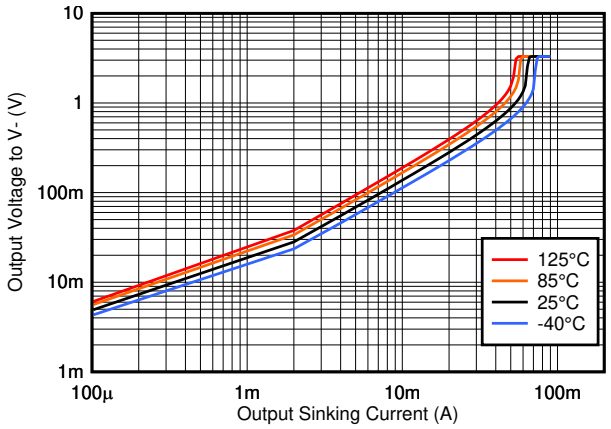



**Figure 5-9. Output Sinking Current vs. Output Voltage, 3.3V**

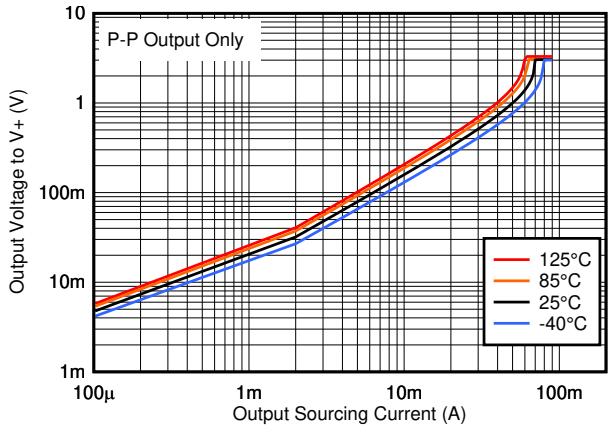



**Figure 5-10. Output Sourcing Current vs. Output Voltage, 3.3V**

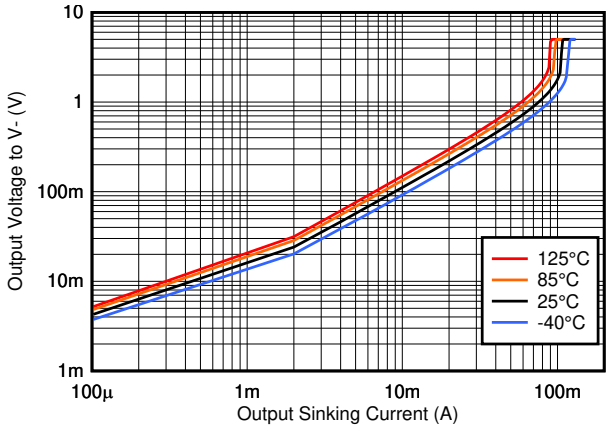



**Figure 5-11. Output Sinking Current vs. Output Voltage, 5V**

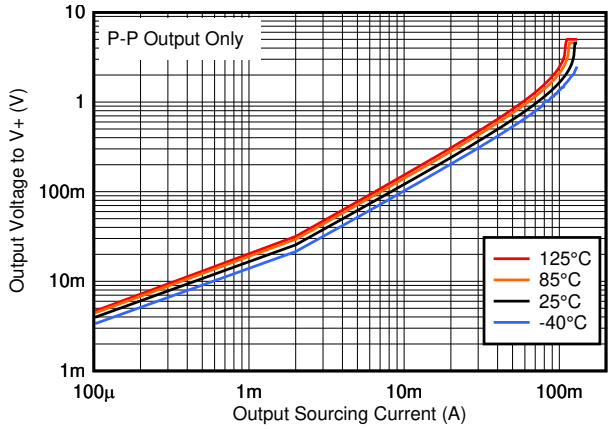



**Figure 5-12. Output Sourcing Current vs. Output Voltage, 5V**

## 5.13 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

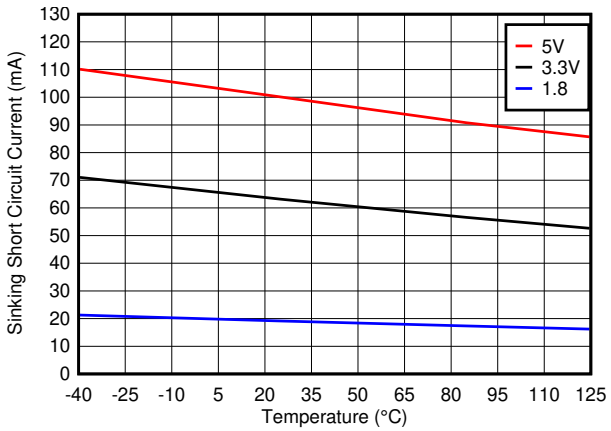



**Figure 5-13. Sinking Short Circuit Current vs. Temperature**

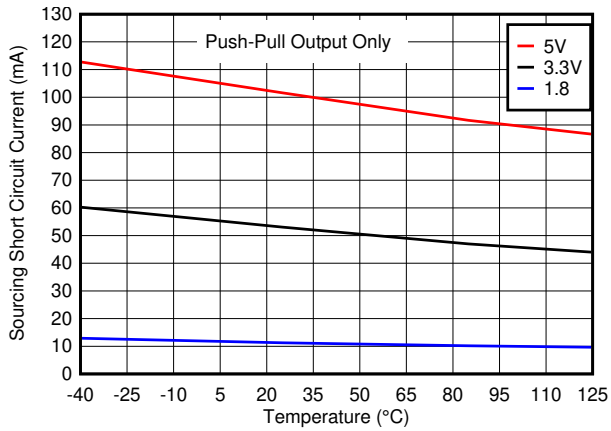



**Figure 5-14. Sourcing Short Circuit Current vs. Temperature**

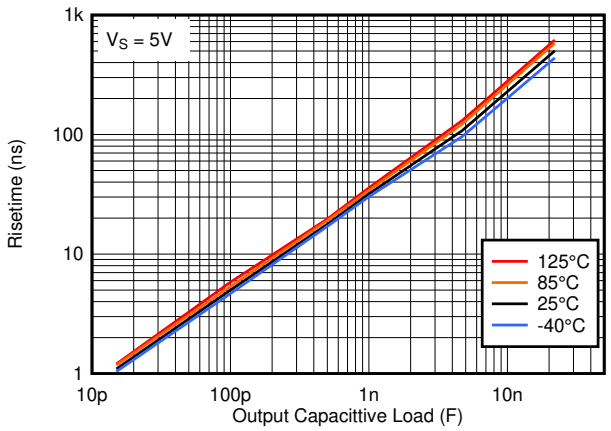



**Figure 5-15. Risetime vs. Capacitive Load**

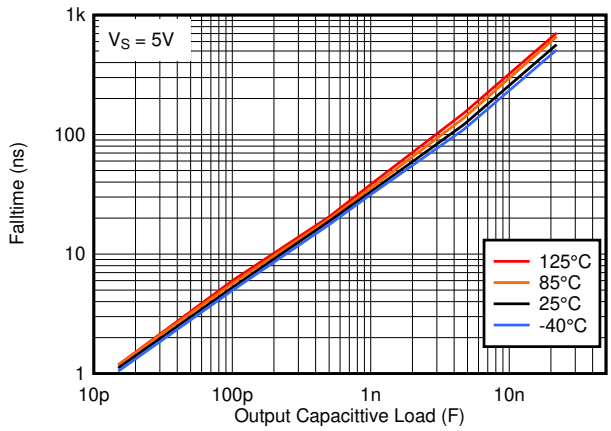



**Figure 5-16. Falltime vs. Capacitive Load**

## 5.13 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

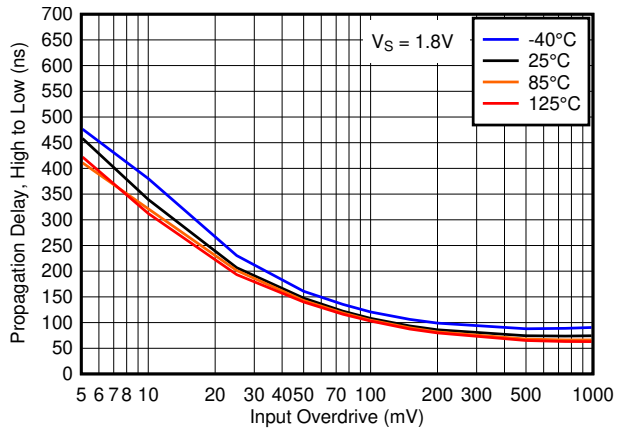



**Figure 5-17. Propagation Delay, High to Low, 1.8V**

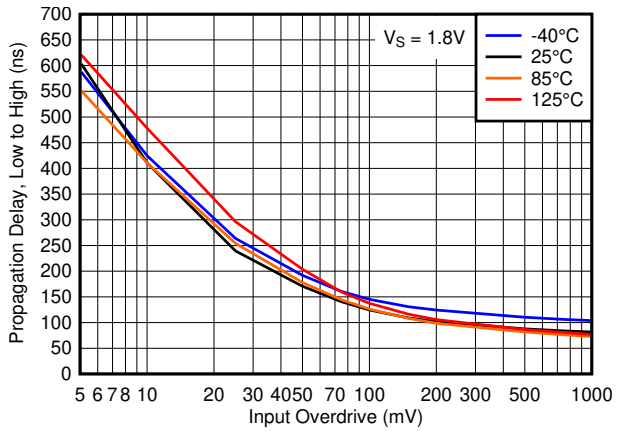



**Figure 5-18. Propagation Delay, Low to High, 1.8V**

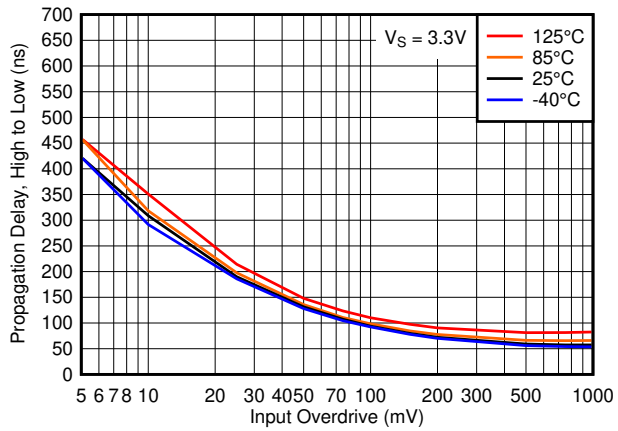



**Figure 5-19. Propagation Delay, High to Low, 3.3V**

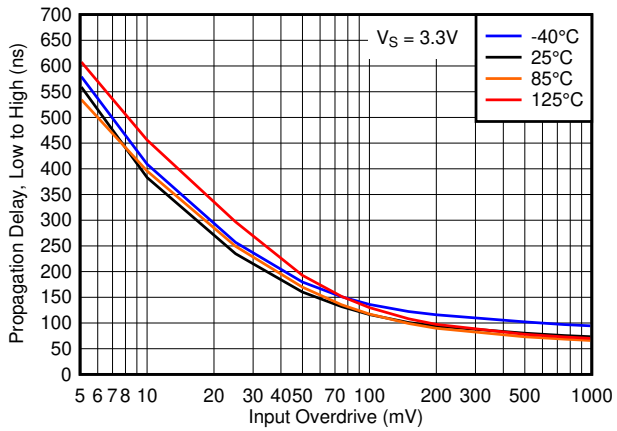



**Figure 5-20. Propagation Delay, Low to High, 3.3V**

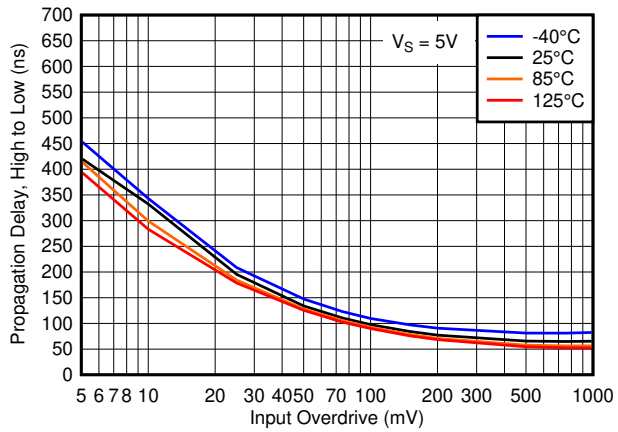



**Figure 5-21. Propagation Delay, High to Low, 5V**

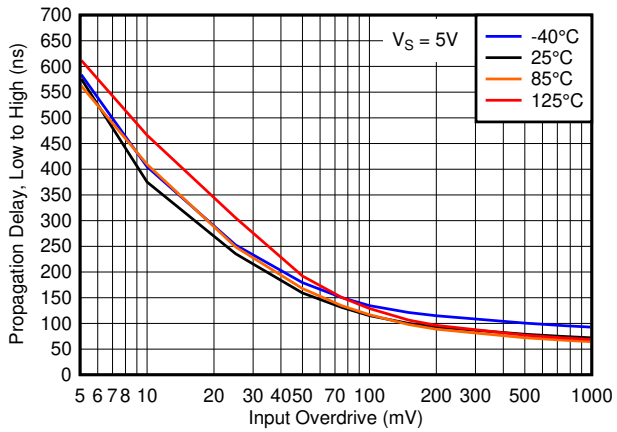



**Figure 5-22. Propagation Delay, Low to High, 5V**

## 5.13 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

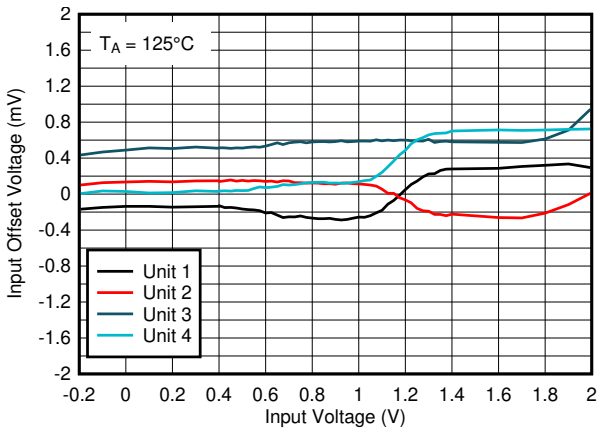



**Figure 5-23. Offset Voltage vs. Input Votlage at 125°C, 1.8V**

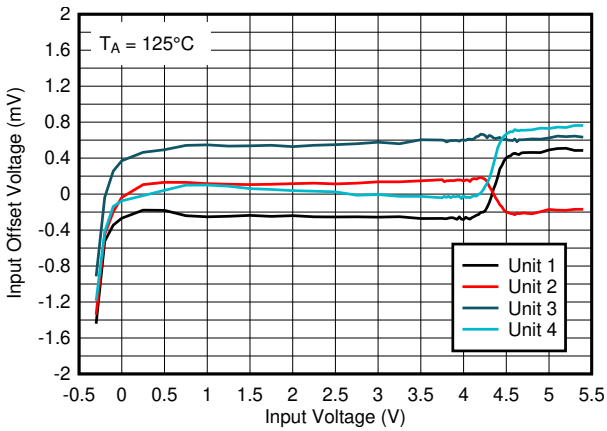



**Figure 5-24. Offset Voltage vs. Input Votlage at 125°C, 5V**

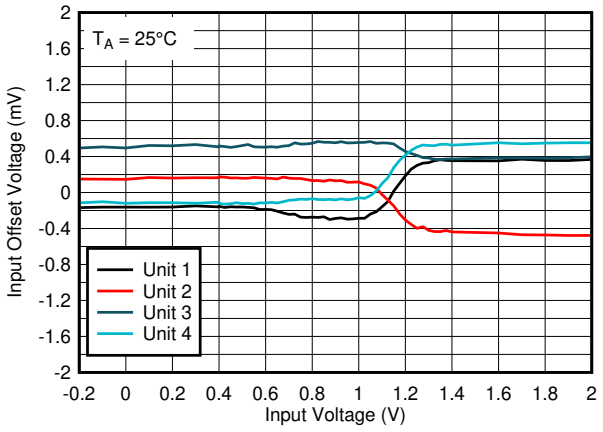



**Figure 5-25. Offset Voltage vs. Input Votlage at 25°C, 1.8V**

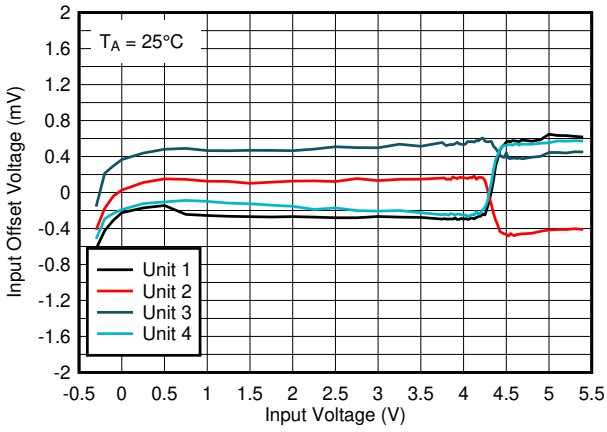



**Figure 5-26. Offset Voltage vs. Input Votlage at 25°C, 5V**

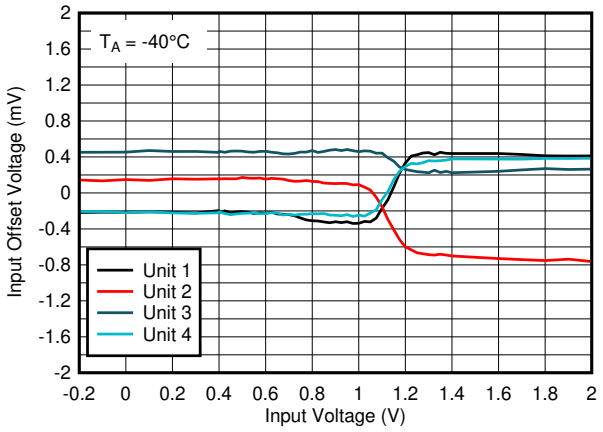



**Figure 5-27. Offset Voltage vs. Input Votlage at -40°C, 1.8V**

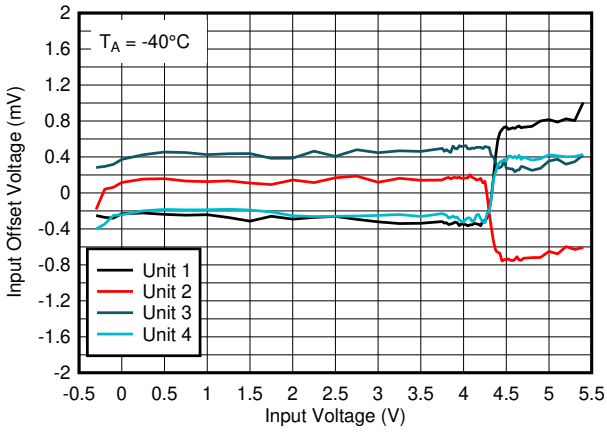



**Figure 5-28. Offset Voltage vs. Input Votlage at -40°C, 5V**

## 5.13 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

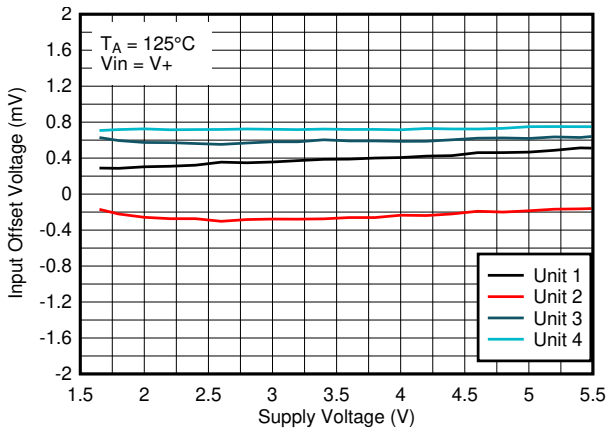



**Figure 5-29. Offset Voltage vs. Supply Voltage at 125°C, $V_{IN}$=V+**

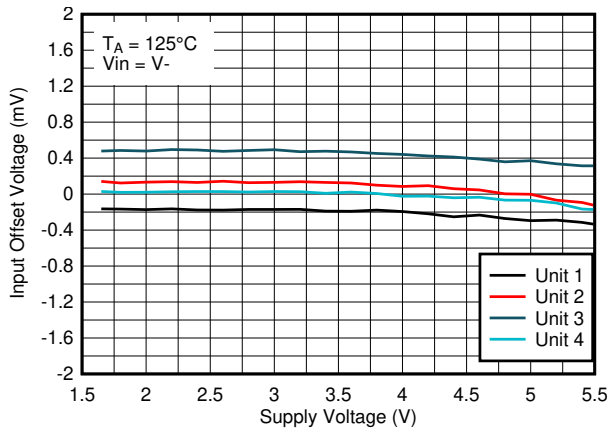



**Figure 5-30. Offset Voltage vs. Supply Voltage at 125°C, $V_{IN}$=V-**

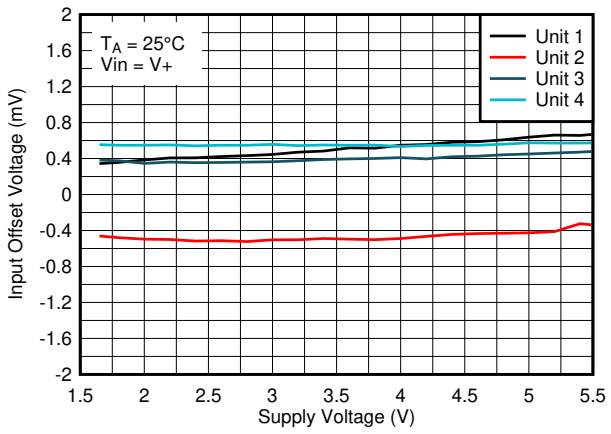



**Figure 5-31. Offset Voltage vs. Supply Voltage at 25°C, $V_{IN}$=V+**

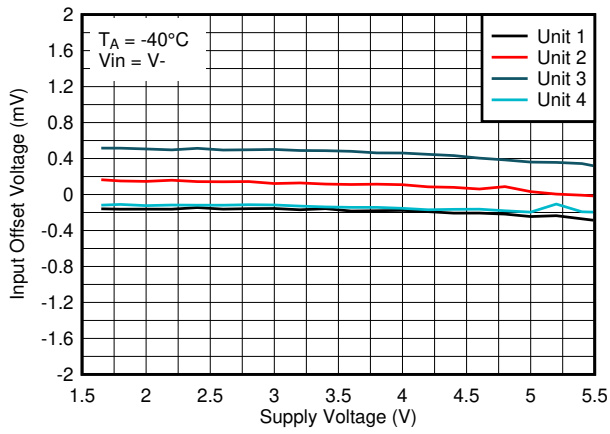



**Figure 5-32. Offset Voltage vs. Supply Voltage at 25°C, $V_{IN}$=V-**

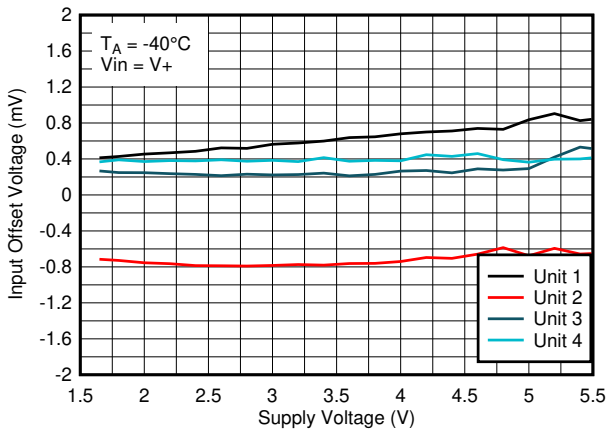



**Figure 5-33. Offset Voltage vs. Supply Voltage at -40°C, $V_{IN}$=V+**

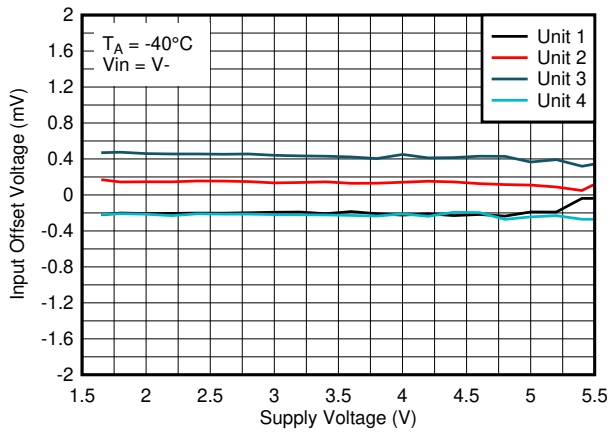


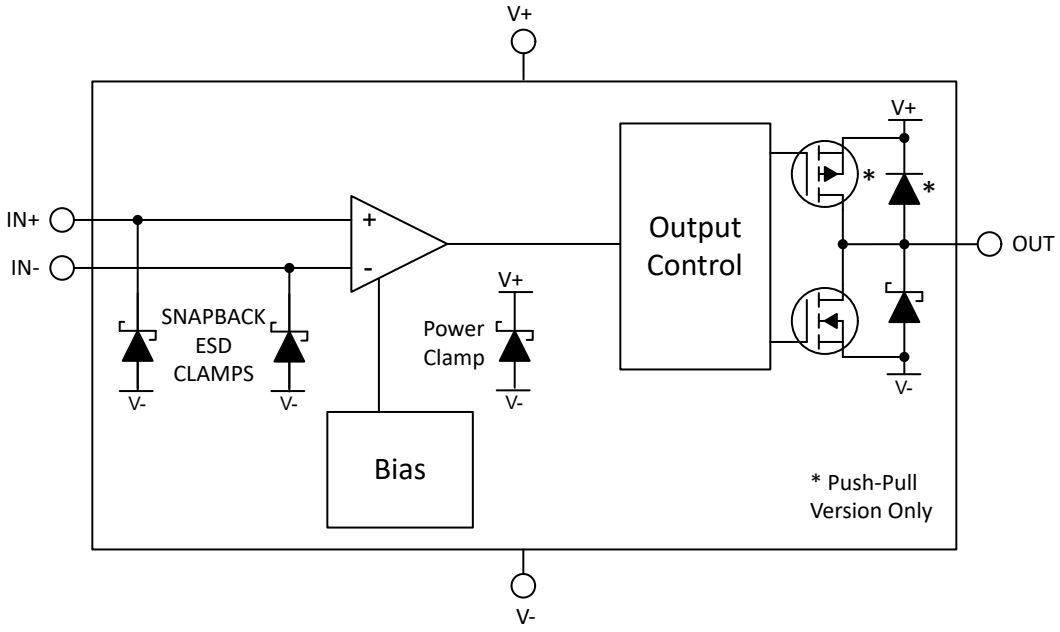

**Figure 5-34. Offset Voltage vs. Supply Voltage at -40°C, $V_{IN}$=V-**

# 6 Detailed Description

## 6.1 Overview

The TLV902x and TLV903x devices are precision, micro-power comparators with fail-safe inputs and push-pull and open-drain output options. Operating down to 1.65V while only consuming only 16µA per channel, the TLV902x and TLV903x are designed for portable, automotive and industrial applications.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

The TLV902x (open-drain output) and TLV903x (push-pull output) devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The TLV90xx family feature a rail-to-rail input stage capable of operating up to 200mV beyond the power supply rails. The comparators also feature push-pull and open-drain output stage options.

## 6.4 Device Functional Modes

### *6.4.1 Outputs*

#### 6.4.1.1 TLV9022 and TLV9024 Open Drain Output

The TLV902x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 5.5V, independent of the comparator supply voltage ($V_S$). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower pull-up resistor values helps increase the rising edge risetime, but at the expense of increasing $V_{OL}$ and higher power dissipation. The risetime is dependant on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1MΩ) creates an exponential rising edge due to the RC time constant and increases the risetime.

Unused open drain outputs must be left floating, or can be tied to the V- pin if floating pins are not allowed. While an individual output can typically sink up to 125mA, the total combined current for all channels must be less than 200mA.

#### 6.4.1.2 TLV9032 and TLV9034 Push-Pull Output

The TLV903x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output. While an individual output can typically sink and source up to 100mA, the total combined current for all channels must be less than 200mA.

### *6.4.2 Inputs*

#### 6.4.2.1 Rail to Rail Input

The TLV90xx input voltage range extends from 200mV below V- to 200mV above V+. The differential input voltage ($V_{ID}$) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input pins exceed V+ or V-.

#### 6.4.2.2 Fault Tolerant Inputs

The TLV90xx inputs are fault tolerant up to 5.5V independent of $V_S$. Fault tolerant is defined as maintaining the same high input impedance when $V_S$ is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0V and 5.5V, even while $V_S$ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains the value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid, the output state is correct.

The following is a summary of input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random). *Do not* operate in this region.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain data sheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

#### 6.4.2.3 Input Protection

The input bias current is typically 5pA for input voltages between V+ and V-. The comparator inputs are protected from negative voltage by the internal ESD diodes connected to V-. As the input voltage goes under V-, or above the input Absolute Maximum ratings, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents when the clamps conduct. See the ESD section for more information.

### 6.4.3 ESD Protection

The TLV90xx family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to V-, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapback "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener.

The TLV902x open-drain output protection also consists of a ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 5.5V.

The TLV903x push-pull output protection consists of a ESD clamp between the output and V-, but also includes a ESD diode clamp to V+, as the output must not exceed the supply rails.

If the inputs are to be connected to a low impedance source, TI recommends adding a current-limiting resistor in series with the input to limit input currents when the clamps conduct. The current must be limited 10mA or less. This series resistance can be part of any resistive input dividers or networks. TI does not specify the performance of the ESD clamps and external clamping must be added if the inputs or output can exceed the maximum ratings as part of normal operation.

### 6.4.4 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ as long as the input is directly connected to the V+ pin to avoid transients.

### 6.4.5 Hysteresis

The TLV90xx family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, there is a possibility for the output to "chatter" (oscillate) when the absolute differential voltage near zero as the comparator triggers on internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See Section 7.1.2 in the following section.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Application Information

### *7.1.1 Basic Comparator Definitions*

#### 7.1.1.1 Operation

The basic comparator compares the input voltage ($V_{IN}$) on one input to a reference voltage ($V_{REF}$) on the other input. In the Comparator Timing Diagram example below, if $V_{IN}$ is less than $V_{REF}$, the output voltage ($V_O$) is logic low ($V_{OL}$). If $V_{IN}$ is greater than $V_{REF}$, the output voltage ($V_O$) is at logic high ($V_{OH}$). Output Conditions summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

**Table 7-1. Output Conditions**

| Inputs Condition | Output |
|---|---|
| IN+ > IN- | HIGH ($V_{OH}$) |
| IN+ = IN- | Indeterminate (chatters - see Hysteresis) |
| IN+ < IN- | LOW ($V_{OL}$) |

#### 7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as $t_{pLH}$ and $t_{pHL}$ in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output.

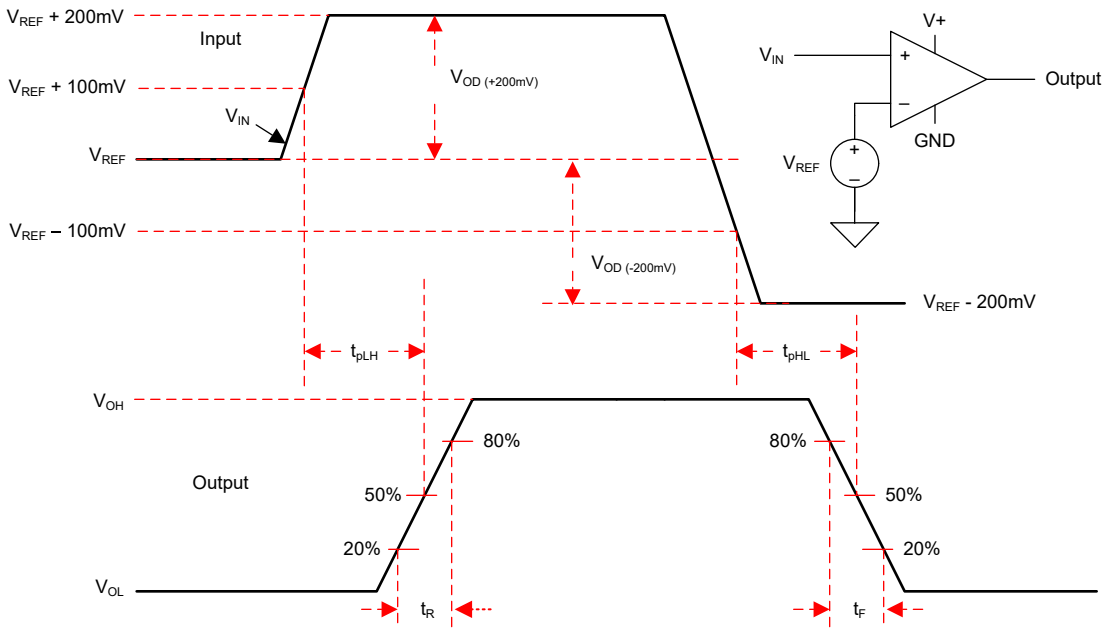



**Figure 7-1. Comparator Timing Diagram**

#### 7.1.1.3 Overdrive Voltage

The overdrive voltage, $V_{OD}$, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 7-1 example. The overdrive voltage can influence the propagation delay ($t_p$). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime ($t_r$) and falltime ($t_f$) is the time from the 20% and 80% points of the output waveform.

### *7.1.2 Hysteresis*

The basic comparator configuration can oscillate or produce a noisy *chatter* output if the applied differential input voltage is near the offset voltage of the comparator. This typically occurs when the input signal moves very slowly across the switching threshold of the comparator.

the addition of hysteresis or positive feedback prevents this problem.

The hysteresis transfer curve is shown in Figure 7-2. This curve is a function of three components: $V_{TH}$, $V_{OS}$, and $V_{HYST}$:

- $V_{TH}$ is the actual set voltage or threshold trip voltage.
- $V_{OS}$ is the internal offset voltage between $V_{IN+}$ and $V_{IN–}$. This voltage is added to $V_{TH}$ to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$ is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

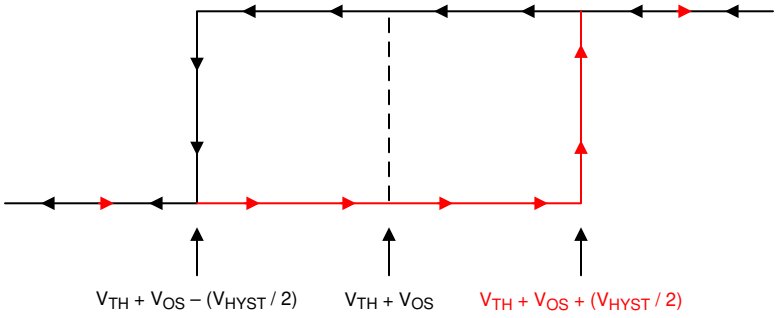



**Figure 7-2. Hysteresis Transfer Curve**

For more information, see the *Comparator with and without hysteresis circuit* application note.

#### 7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V+), as shown in Figure 7-3.

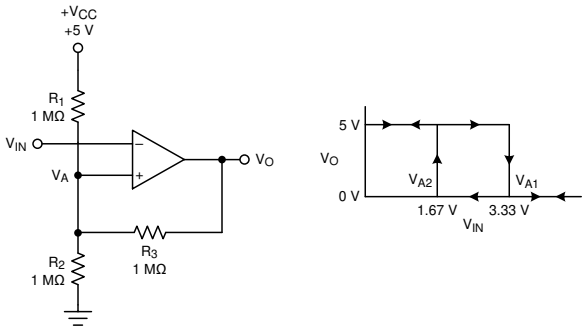



**Figure 7-3. TLV903xin an Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in Figure 7-3.

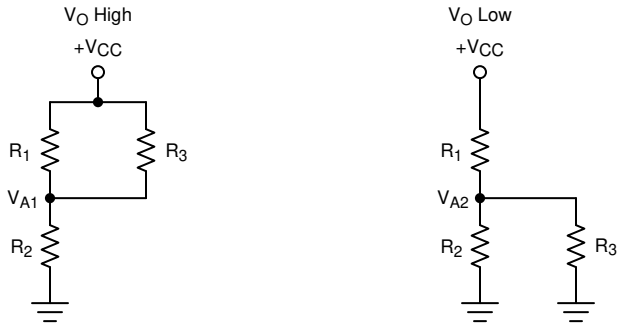



**Figure 7-4. Inverting Configuration Resistor Equivalent Networks**

When $V_{IN}$ is less than $V_A$, the output voltage is high (for simplicity, assume $V_O$ switches as high as $V_{CC}$). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 7-4.

Equation 1 below defines the high-to-low trip voltage ($V_{A1}$).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When $V_{IN}$ is greater than $V_A$, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage ($V_{A2}$).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

#### 7.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference ($V_{REF}$) at the inverting input, as shown in Figure 7-5,

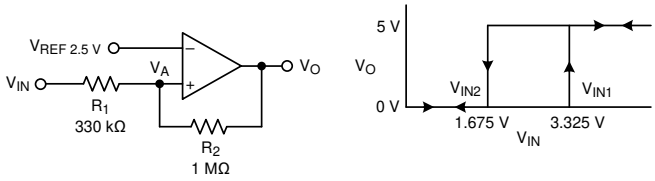



**Figure 7-5. TLV903x in a Non-Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in Figure 7-6.

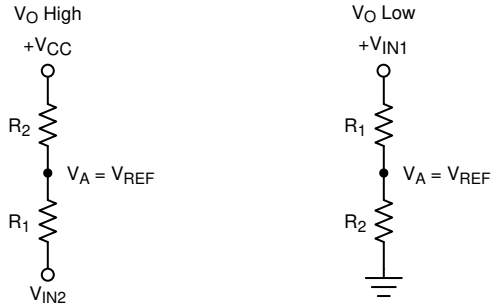



**Figure 7-6. Non-Inverting Configuration Resistor Networks**

When $V_{IN}$ is less than $V_{REF}$, the output is low. For the output to switch from low to high, $V_{IN}$ must rise above the $V_{IN1}$ threshold. Use Equation 4 to calculate $V_{IN1}$.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When $V_{IN}$ is greater than $V_{REF}$, the output is high. For the comparator to switch back to a low state, $V_{IN}$ must drop below $V_{IN2}$. Use Equation 5 to calculate $V_{IN2}$.

$$V_{IN2} = \frac{V_{REF}(R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between $V_{IN1}$ and $V_{IN2}$, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

For more information, see the *Inverting comparator with hysteresis circuit* application note" and *Non-Inverting Comparator With Hysteresis Circuit* application note.

#### 7.1.2.3 Inverting and Non-Inverting Hysteresis Using Open-Drain Output

An open drain output device, such as the TLV902x, can also be used, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + $R_{PULLUP}$. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

## 7.2 Typical Applications

### *7.2.1 Window Comparator*

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 7-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV902x) if the outputs are directly connected together.

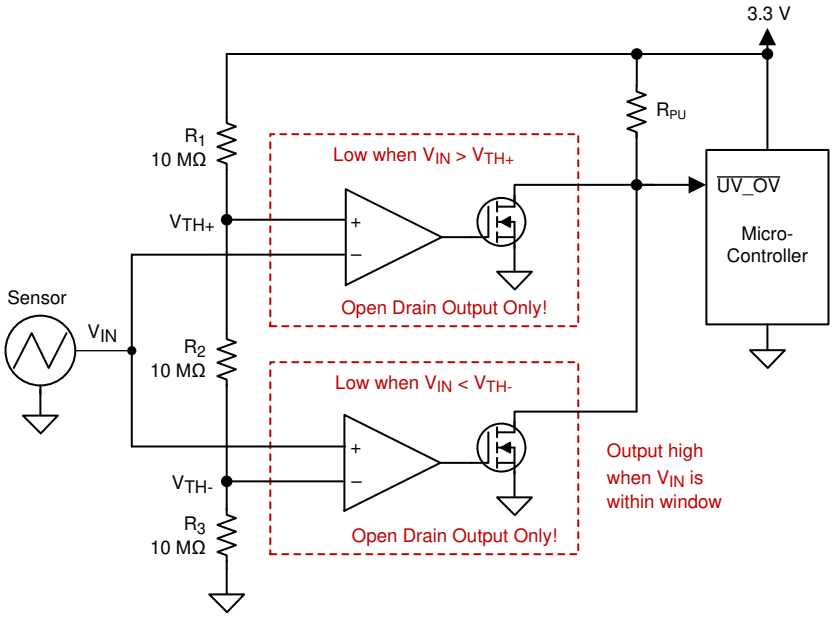



**Figure 7-7. Window Comparator**

#### 7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

#### 7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 7-7. Connect $V_{CC}$ to a 3.3V power supply and $V_{EE}$ to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ($V_{TH+}$ and $V_{TH–}$).

With each resistor being equal, $V_{TH+}$ is 2.2V and $V_{TH-}$ is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs are low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in Figure 7-8.

#### 7.2.1.3 Application Curve

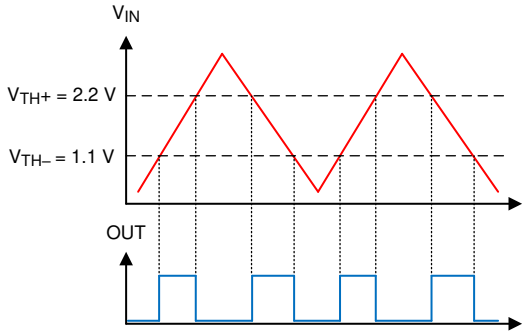



**Figure 7-8. Window Comparator Results**

For more information, see the *Window comparator circuit* application note.

### *7.2.2 Square-Wave Oscillator*

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV903x) is recommended for best symmetry.

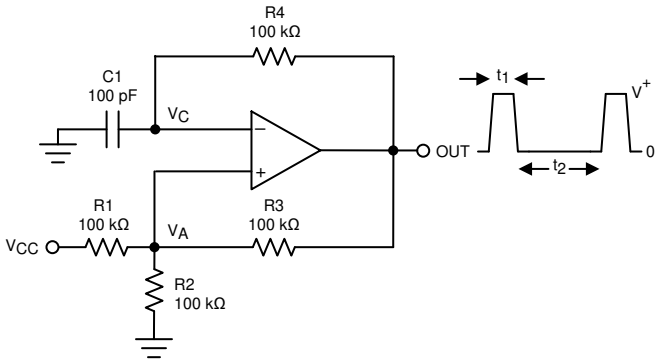



**Figure 7-9. Square-Wave Oscillator**

#### 7.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor $C_1$ and resistor $R_4$. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which can help to reduce BOM cost and board space. R4 must be over several kilo-ohms to minimize loading the output.

#### 7.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

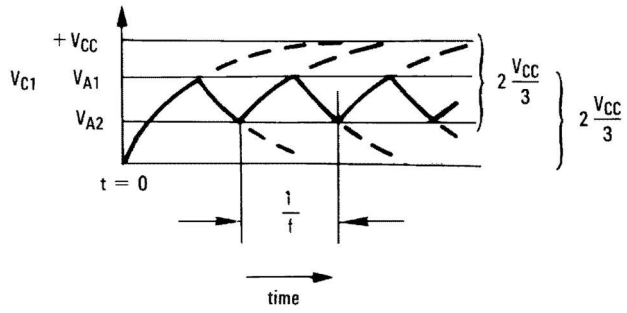



**Figure 7-10. Square-Wave Oscillator Timing Thresholds**

First consider the output of Figure Figure 7-9 as high, which indicates the inverted input $V_C$ is lower than the noninverting input ($V_A$). This causes the $C_1$ to be charged through $R_4$, and the voltage $V_C$ increases until the inverting input is equal to the noninverting input. The value of $V_A$ at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \parallel R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + R_2 \parallel R_3} \tag{8}$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The $C_1$ now discharges though the $R_4$, and the voltage $V_{CC}$ decreases until the voltage reaches $V_{A2}$. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for $C_1$ from $2V_{CC}/3$ to $V_{CC}$ / 3 then back to $2V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2\ R_4C_1 \times \ln 2$.

The oscillation frequency can be obtained by Equation 9:

$$f = 1 \div (2\ R4 \times C1 \times \ln 2) \tag{9}$$

#### 7.2.2.3 Application Curve

Figure 7-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100k\Omega$
- $C_1 = 100pF$, $C_L = 20pF$
- V+ = 5V, V– = GND
- $C_{stray}$ (not shown) from $V_A$ TO GND = 10pF

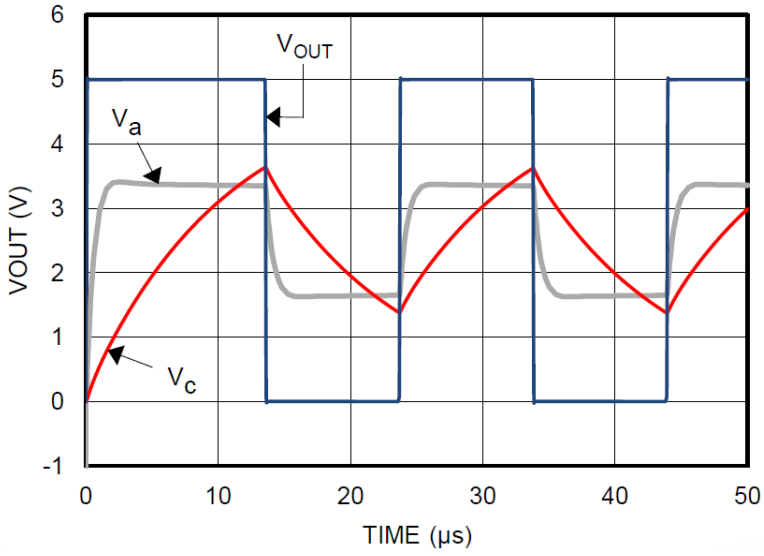



**Figure 7-11. Square-Wave Oscillator Output Waveform**

### *7.2.3 Adjustable Pulse Width Generator*

*Figure 7-12* is a variation on the Square-Wave Oscillator that allows adjusting the pulse widths.

$R_4$ and $R_5$ provide separate charge and discharge paths for the capacitor C depending on the output state.

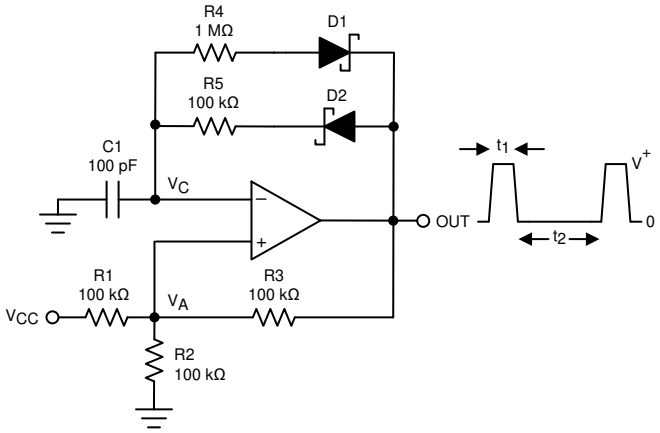



**Figure 7-12. Adjustable Pulse Width Generator**

The charge path is set through $R_5$ and $D_2$ when the output is high. Similarly, the discharge path for the capacitor is set by $R_4$ and $D_1$ when the output is low.

The pulse width $t_1$ is determined by the RC time constant of $R_5$ and C. Thus, the time $t_2$ between the pulses can be changed by varying $R_4$, and the pulse width can be altered by $R_5$. The frequency of the output can be changed by varying both $R_4$ and $R_5$. At low voltages, the effects of the diode forward drop (0.8V, or 0.15V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

### *7.2.4 Time Delay Generator*

The circuit shown in Figure 7-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

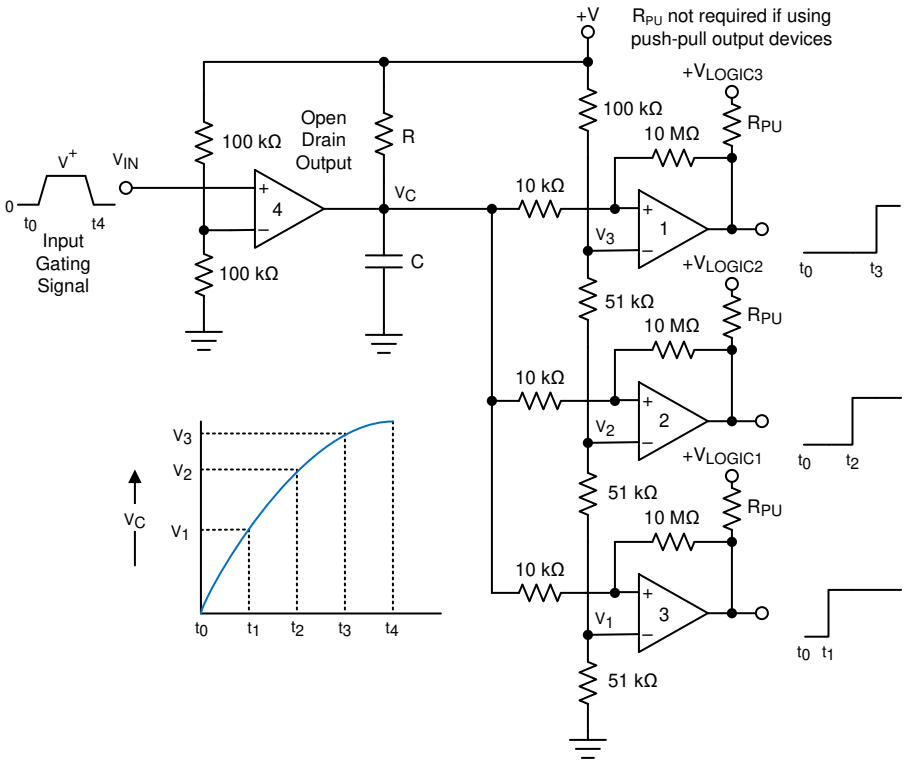



**Figure 7-13. Time Delay Generator**

Consider the case of $V_{IN}$ = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding the node to 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when $V_C$ rises above the reference voltages $V_1$, $V_2$ and $V_3$. A small amount of hysteresis has been provided by the 10kΩ and 10MΩ resistors to insure smooth switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100kΩ and C = 0.01µF to 1µF.

All outputs immediately go low when $V_{IN}$ falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV902x), whereas comparators 1 though 3 can be either open drain or push-pull output, depending on system requirements. $R_{PU}$ is not required for push-pull output devices.

### *7.2.5 Logic Level Shifter*

The output of the TLV902x is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

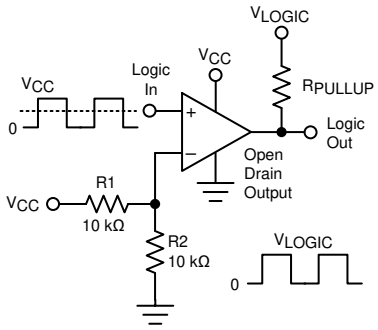



**Figure 7-14. Universal Logic Level Shifter**

The two 10kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and can be connected to any pull-up voltage between 0V and 5.5V. The pullup voltage must match the driven logic input "high" level.

### 7.2.6 One-Shot Multivibrator

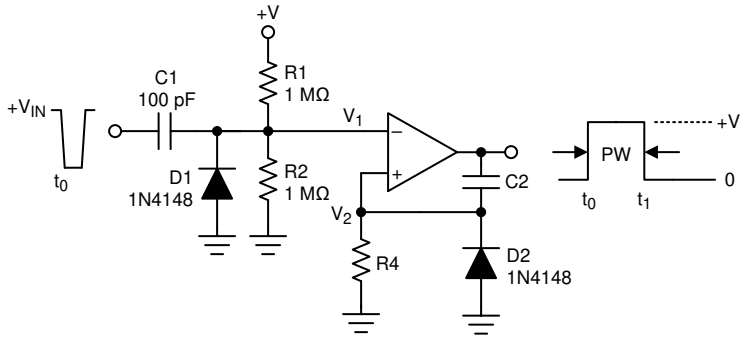



**Figure 7-15. One-Shot Multivibrator**

A monostable multivibrator has one stable state in which the output can remain indefinitely. The circuit can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of $C_2$ and $R_4$. The resistor divider of $R_1$ and $R_2$ can be used to determine the magnitude of the input trigger pulse. The output changes state when $V_1 < V_2$. Diode $D_2$ provides a rapid discharge path for capacitor $C_2$ to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

### 7.2.7 Bi-Stable Multivibrator

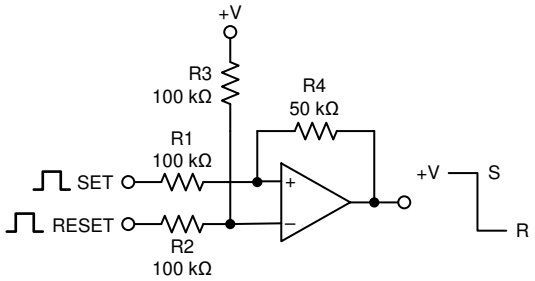



**Figure 7-16. Bi-Stable Multivibrator**

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of $R_2$ and $R_3$. A pulse applied to the SET terminal that sets the output of the comparator high. The resistor divider of $R_1$, $R_4$, and $R_5$ now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET toggles the output low.

### 7.2.8 Zero Crossing Detector

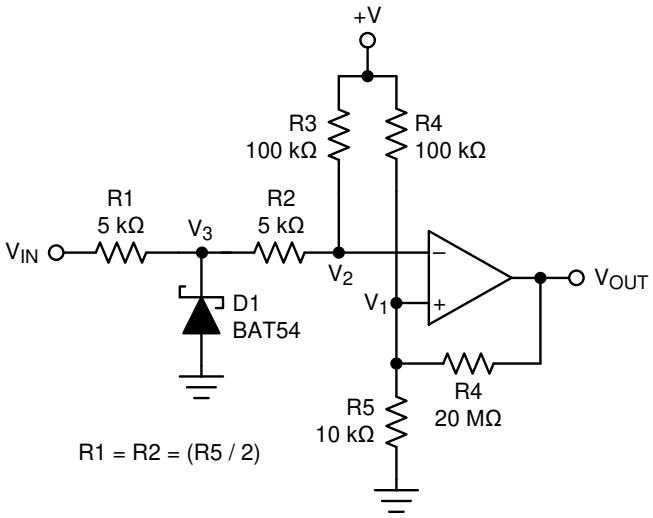



**Figure 7-17. Zero Crossing Detector**

A voltage divider of $R_4$ and $R_5$ establishes a reference voltage $V_1$ at the non-inverting input. By making the series resistance of $R_1$ and $R_2$ equal to $R_5$, the comparator switches when $V_{IN}$ = 0. Diode $D_1$ makes sure that $V_3$ clamps near ground. The voltage divider of $R_2$ and $R_3$ prevents $V_2$ from going below ground. A small amount of hysteresis is used to provide rapid output voltage transitions.

### 7.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of $R_1$ and $C_1$ establishes an mean reference voltage $V_{REF}$, which tracks the mean amplitude of the $V_{IN}$ signal. The noninverting input is directly connected to $V_{REF}$ through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

When the waveform is data, TI recommends that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs can suffer from timing distortions caused by the changing $V_{REF}$ average voltage.

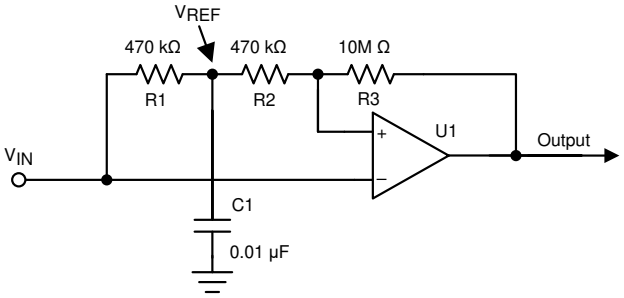



**Figure 7-18. Pulse Slicer Using TLV903x**

For this design, follow these design requirements:

- The RC constant value ($R_2$ and $C_1$) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with $R_2$ and $R_{43}$ helps to avoid spurious output toggles.

The TLV902x can also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 7-19 shows the results of a 9600 baud data signal riding on a varying baseline.

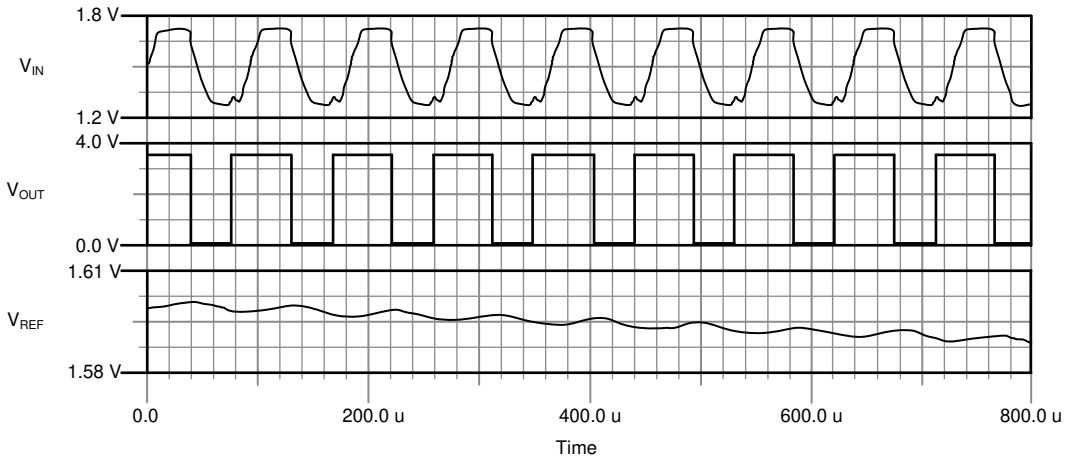



**Figure 7-19. Pulse Slicer Waveforms**

## 7.3 Power Supply Recommendations

Due to the fast output edges, proper supply bypassing is critical to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between $V_{CC}$ pin and ground pins. Narrow, peak currents can be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from either *split* supplies (V+, V, and GND), or a *single* supply (V+ and GND), with GND applied to the V- pin.

Input signals must stay within the specified input range (between V+ and V-) for either type.

Note that on *split* supplies, the output now swings *low* ($V_{OL}$) to V- potential and not GND.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

For accurate comparator applications a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the $V_{CC}$ and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a $V_{CC}$ or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

### 7.4.2 Layout Example

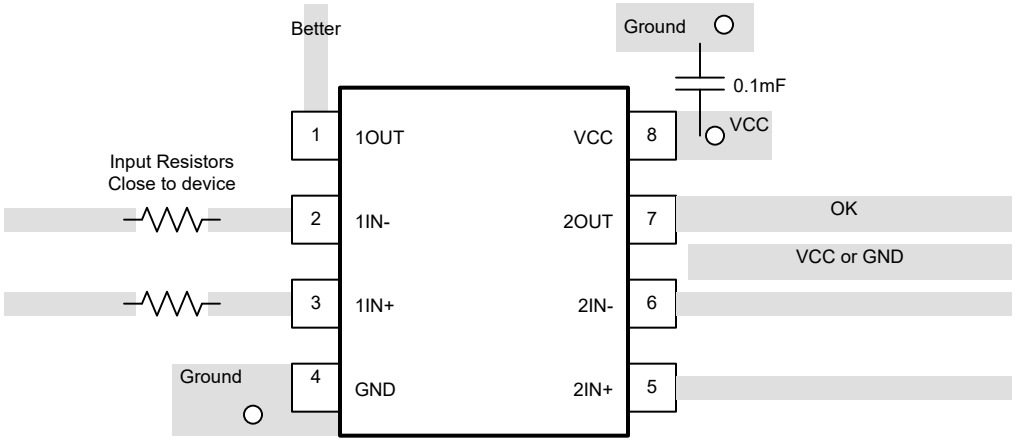



**Figure 7-20. Dual Layout Example**

# 8 Device and Documentation Support

## 8.1 Documentation Support

### 8.1.1 Related Documentation

- Texas Instruments, *Analog Engineers Circuit Cookbook: Amplifiers* (see Comparators section) E-Book
- Texas Instruments, *A Quad of Independently Func Comparators* application note
- Texas Instruments, *Comparator with and without hysteresis circuit* circuit design
- Texas Instruments, *Comparator With Hysteresis Design Guide* reference guide
- Texas Instruments, *How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications* application brief
- Texas Instruments, *Inverting comparator with hysteresis circuit* application brief
- Texas Instruments, *Non-Inverting Comparator With Hysteresis Circuit* circuit design
- Texas Instruments, *PWM generator circuit* circuit design
- Texas Instruments, *Window comparator circuit* circuit design
- Texas Instruments, *Window Comparator Design Guide* reference guide
- Texas Instruments, *Zero crossing detection using comparator circuit* application brief

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (February 2025) to Revision H (November 2025) | Page |
|---|---|
| • Added X2QFN (RUC) package for TLV9024 and TLV9034 | 1 |
| • Deleted Power-on Reset (POR) feature throughout | 1 |
| • Updated status from Production Mix to Production Data | 1 |

**Changes from Revision F (March 2023) to Revision G (February 2025)** **Page**

- Changed status of dual WSON package....1
- Added Quad RUC package drawing....5

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV9020DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T20 |
| TLV9020DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T20 |
| TLV9020DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OR |
| TLV9020DCKR.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OR |
| TLV9021DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T21 |
| TLV9021DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T21 |
| TLV9021DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OT |
| TLV9021DCKR.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OT |
| TLV9022DDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2H3F |
| TLV9022DDFR.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2H3F |
| TLV9022DGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 2IFT |
| TLV9022DGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 2IFT |
| TLV9022DR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9022 |
| TLV9022DR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9022 |
| TLV9022DSGR | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 9022 |
| TLV9022DSGR.A | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 9022 |
| TLV9022DSGRG4 | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 9022 |
| TLV9022DSGRG4.A | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 9022 |
| TLV9022PWR | Active | Production | TSSOP (PW) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9022 |
| TLV9022PWR.A | Active | Production | TSSOP (PW) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9022 |
| TLV9024DR | Active | Production | SOIC (D) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9024D |
| TLV9024DR.A | Active | Production | SOIC (D) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9024D |
| TLV9024DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9024 |
| TLV9024DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9024 |
| TLV9024PWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | TLV9024 |
| TLV9024PWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9024 |
| TLV9024RTER | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9024 |
| TLV9024RTER.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9024 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV9024RTERG4 | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9024 |
| TLV9024RTERG4.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9024 |
| TLV9024RUCR | Active | Production | QFN (RUC) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1ZI |
| TLV9030DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T30 |
| TLV9030DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T30 |
| TLV9030DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OS |
| TLV9030DCKR.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OS |
| TLV9031DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T31 |
| TLV9031DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T31 |
| TLV9031DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OU |
| TLV9031DCKR.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OU |
| TLV9032DDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2H2F |
| TLV9032DDFR.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2H2F |
| TLV9032DGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 2IGT |
| TLV9032DGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2IGT |
| TLV9032DR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9032 |
| TLV9032DR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9032 |
| TLV9032DRG4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9032 |
| TLV9032DRG4.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9032 |
| TLV9032DSGR | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 9032 |
| TLV9032DSGR.A | Active | Production | WSON (DSG) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 9032 |
| TLV9032PWR | Active | Production | TSSOP (PW) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9032 |
| TLV9032PWR.A | Active | Production | TSSOP (PW) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9032 |
| TLV9034DR | Active | Production | SOIC (D) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9034D |
| TLV9034DR.A | Active | Production | SOIC (D) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9034D |
| TLV9034DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9034 |
| TLV9034DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9034 |
| TLV9034PWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | TLV9034 |
| TLV9034PWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV9034 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV9034RTER | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9034 |
| TLV9034RTER.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9034 |
| TLV9034RUCR | Active | Production | QFN (RUC) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TTI |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TLV9020, TLV9021, TLV9022, TLV9024, TLV9030, TLV9031, TLV9032, TLV9034 :**

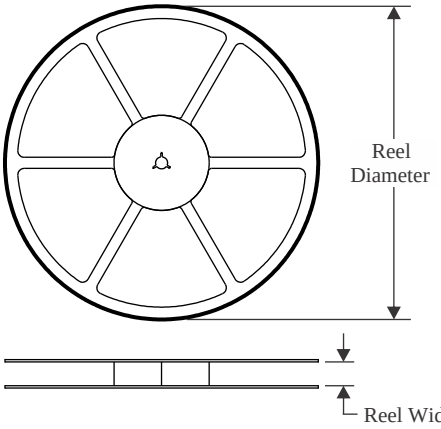
- Automotive : TLV9020-Q1, TLV9021-Q1, TLV9022-Q1, TLV9024-Q1, TLV9030-Q1, TLV9031-Q1, TLV9032-Q1, TLV9034-Q1
- Enhanced Product : TLV9024-EP, TLV9034-EP

NOTE: Qualified Version Definitions:

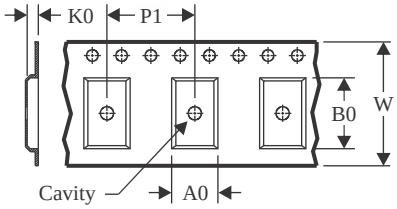
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

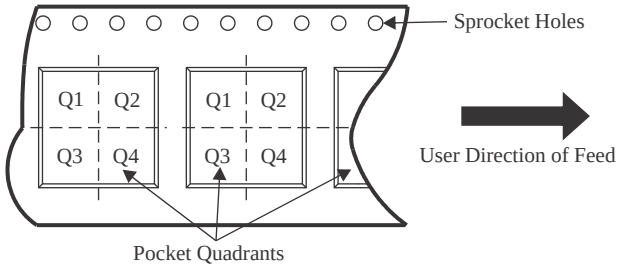



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

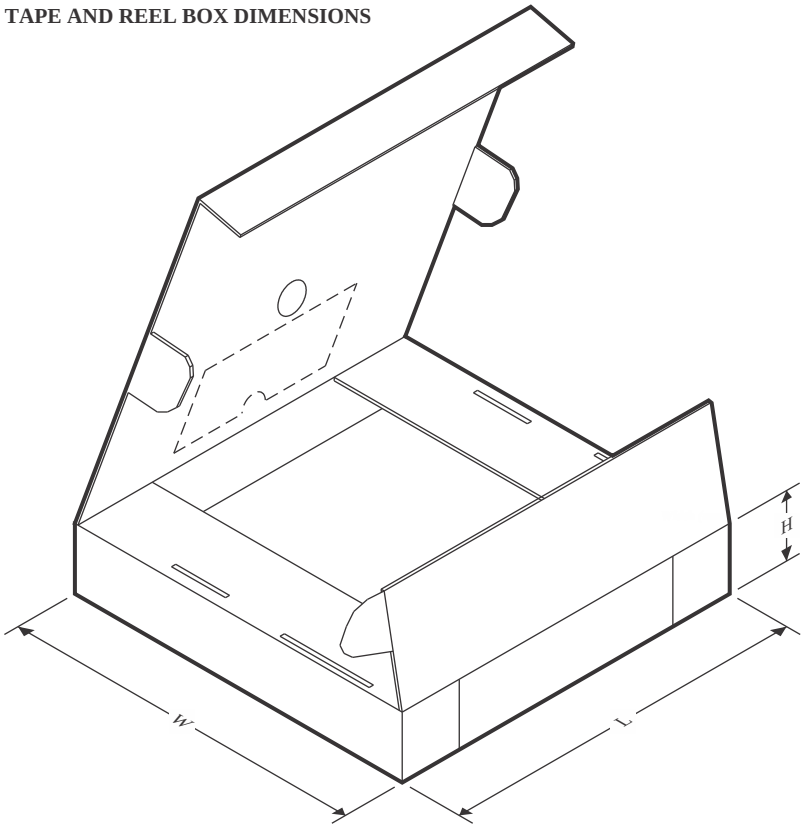



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV9020DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9020DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV9021DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9021DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV9022DDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9022DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.25 | 3.35 | 1.25 | 8.0 | 12.0 | Q1 |
| TLV9022DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9022DSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV9022DSGRG4 | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV9022PWR | TSSOP | PW | 8 | 2500 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9024DR | SOIC | D | 14 | 3000 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV9024DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TLV9024PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9024RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TLV9024RTERG4 | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV9030DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9030DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV9031DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9031DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV9032DDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9032DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9032DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9032DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9032DSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV9032PWR | TSSOP | PW | 8 | 2500 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9034DR | SOIC | D | 14 | 3000 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV9034DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TLV9034PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9034RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV9020DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9020DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV9021DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9021DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV9022DDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9022DGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TLV9022DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9022DSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9022DSGRG4 | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9022PWR | TSSOP | PW | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9024DR | SOIC | D | 14 | 3000 | 353.0 | 353.0 | 32.0 |
| TLV9024DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| TLV9024PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV9024RTER | WQFN | RTE | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| TLV9024RTERG4 | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TLV9030DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9030DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV9031DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

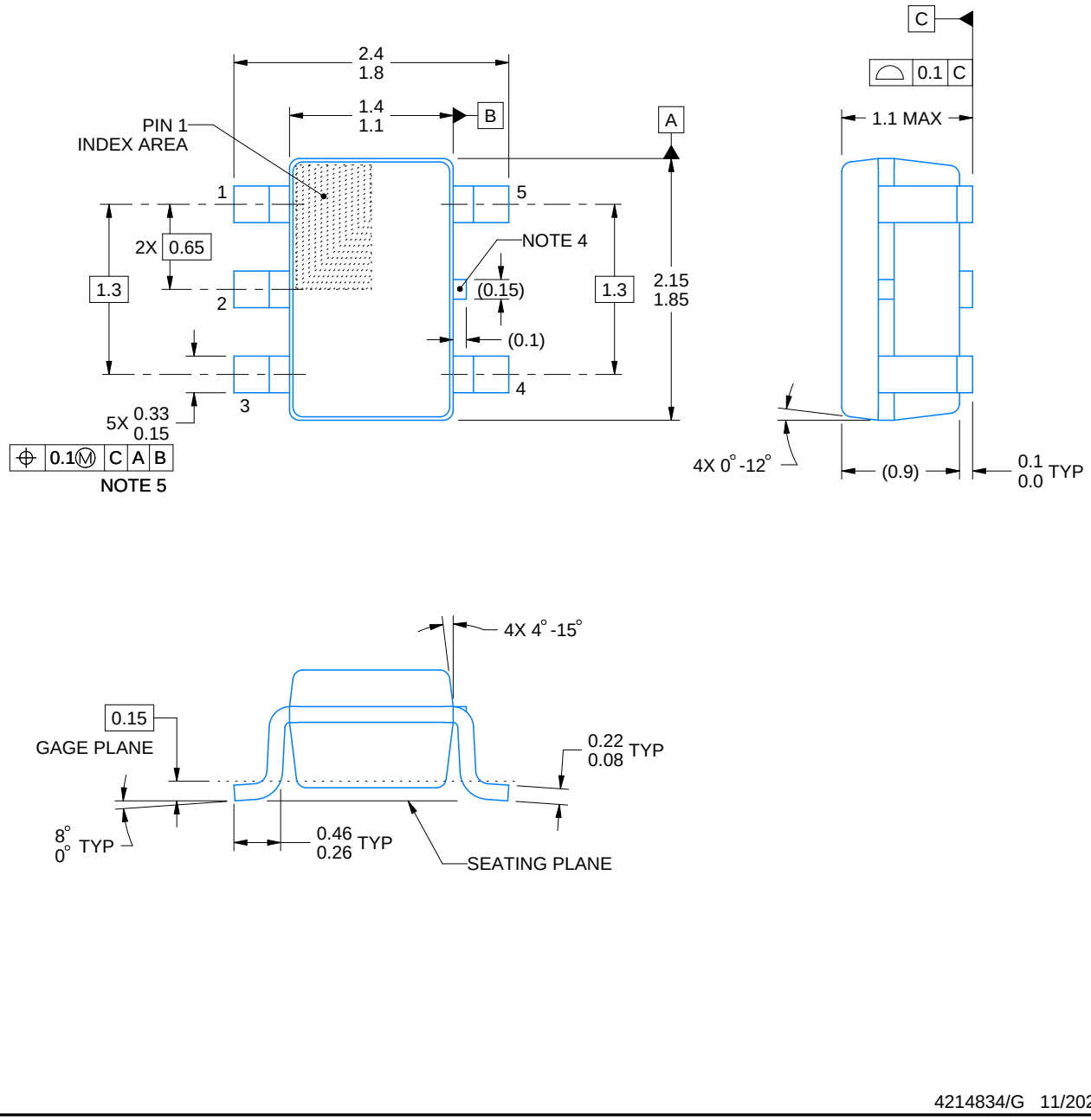
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV9031DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV9032DDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9032DGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9032DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9032DRG4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9032DSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9032PWR | TSSOP | PW | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9034DR | SOIC | D | 14 | 3000 | 353.0 | 353.0 | 32.0 |
| TLV9034DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| TLV9034PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV9034RTER | WQFN | RTE | 16 | 3000 | 360.0 | 360.0 | 36.0 |

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

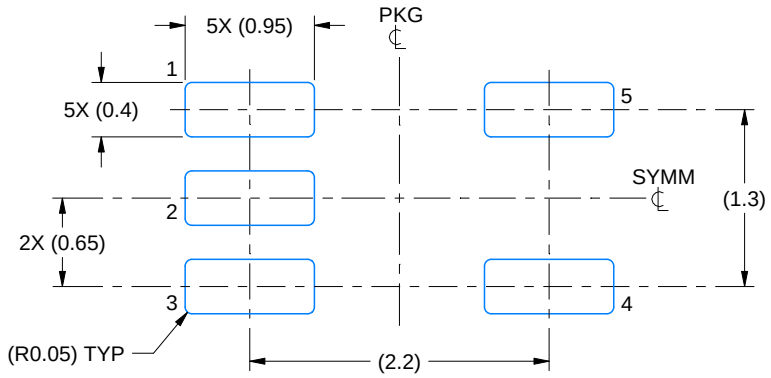
SMALL OUTLINE TRANSISTOR



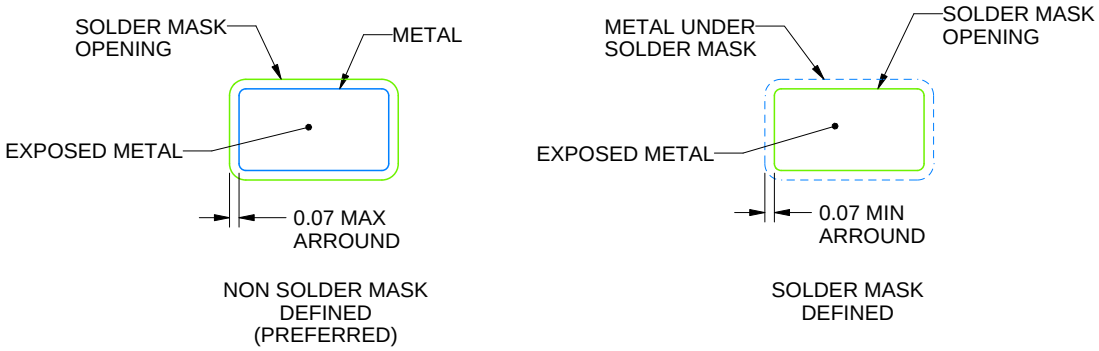

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

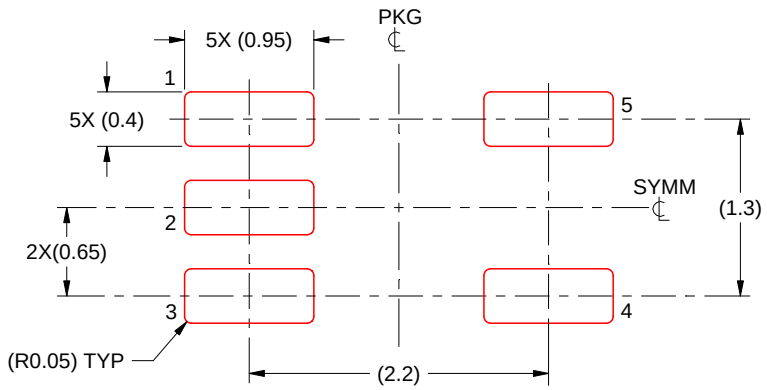



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

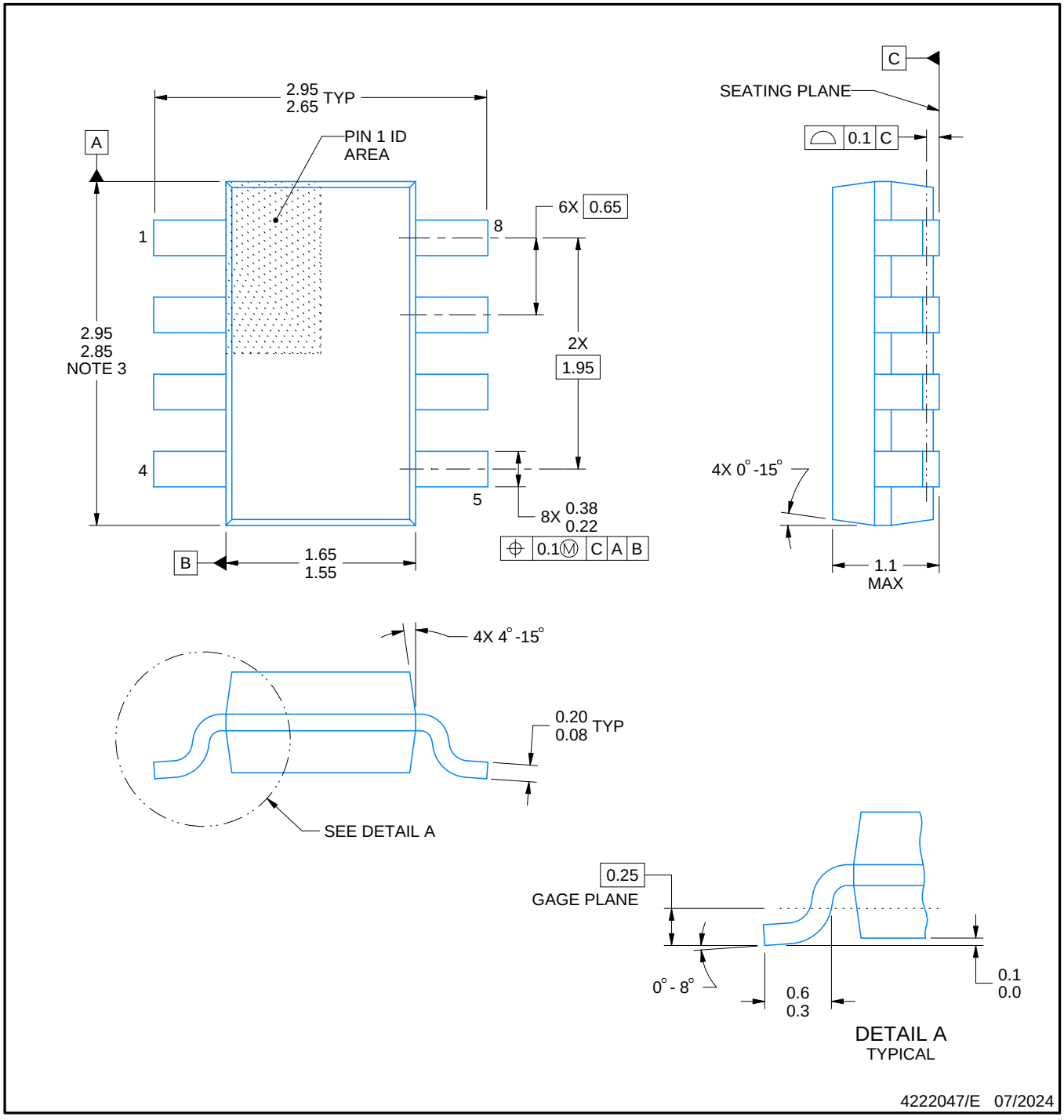
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DDF0008A

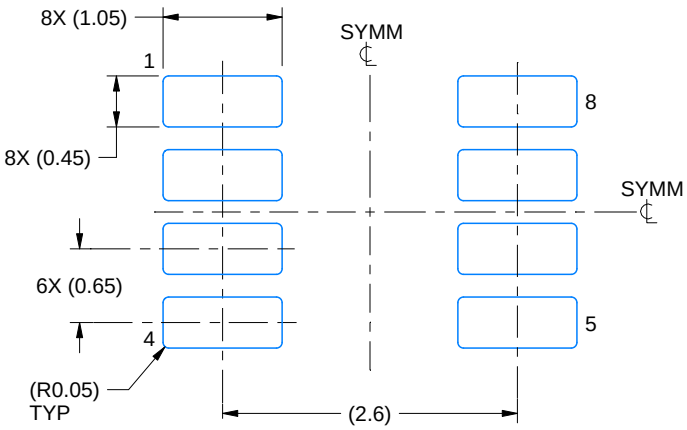
## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

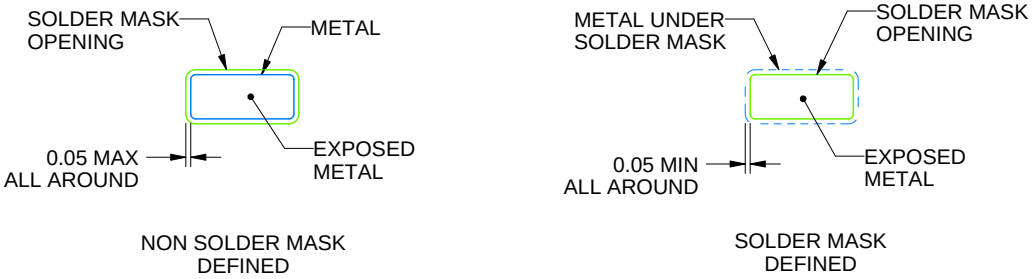



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

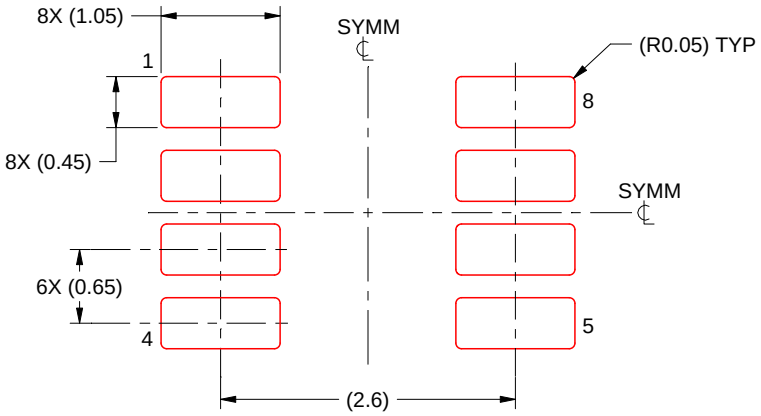
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DDF0008A

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

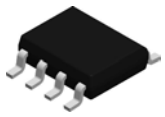



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

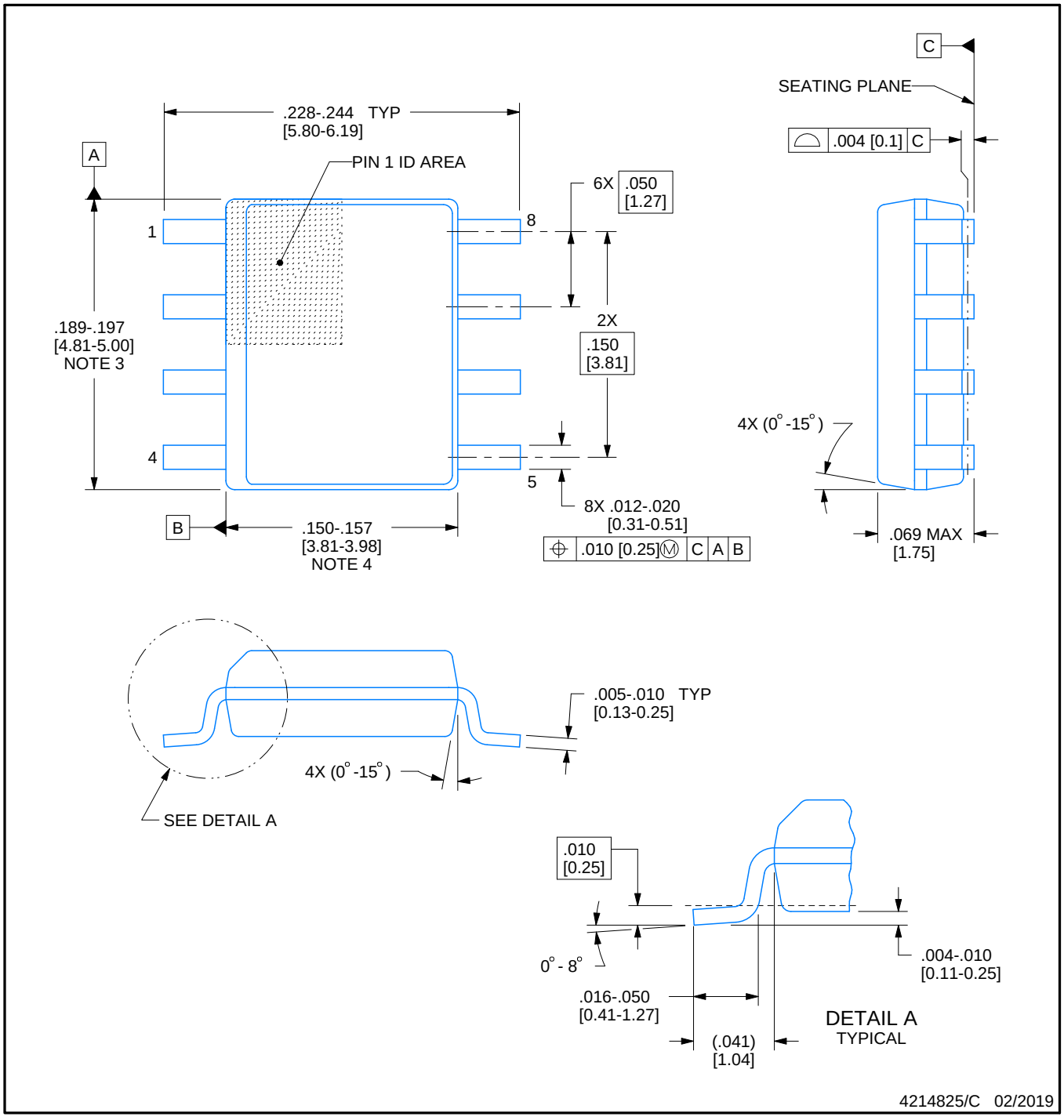


# PACKAGE OUTLINE

## D0008A

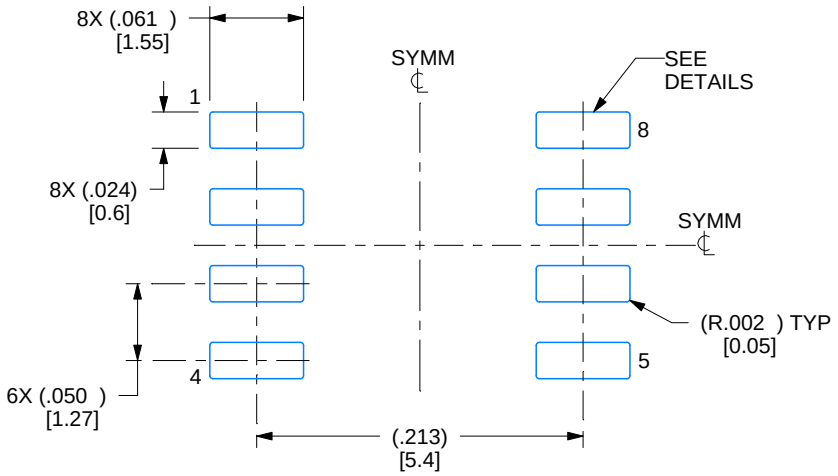
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

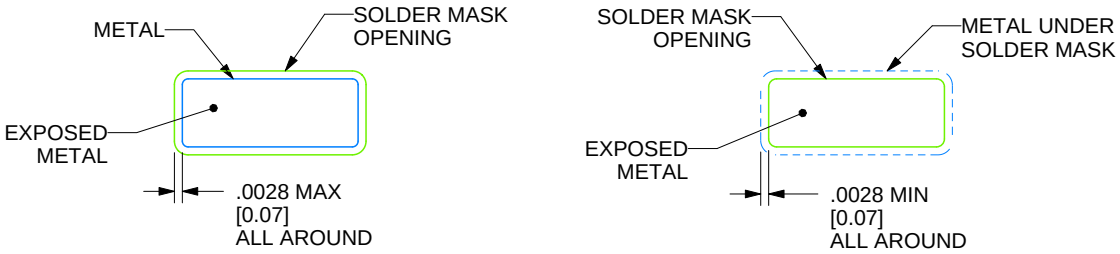



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

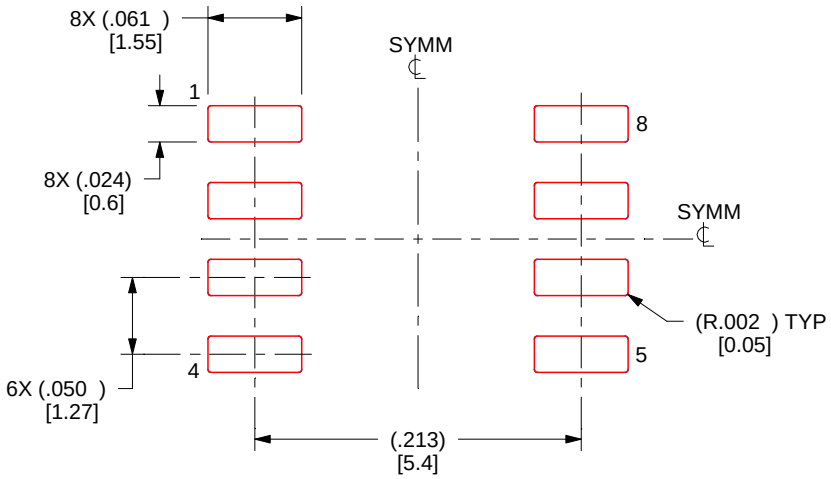
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

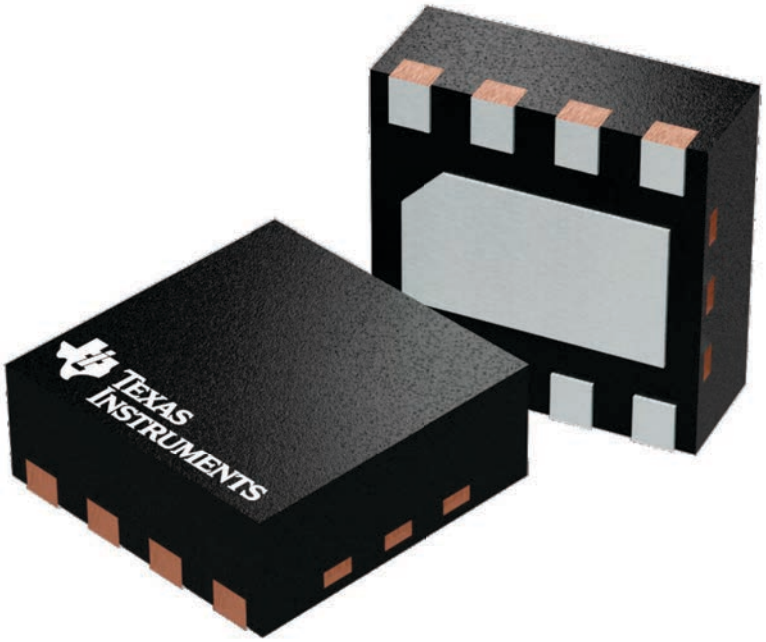
## DSG 8

## WSON - 0.8 mm max height

**2 x 2, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



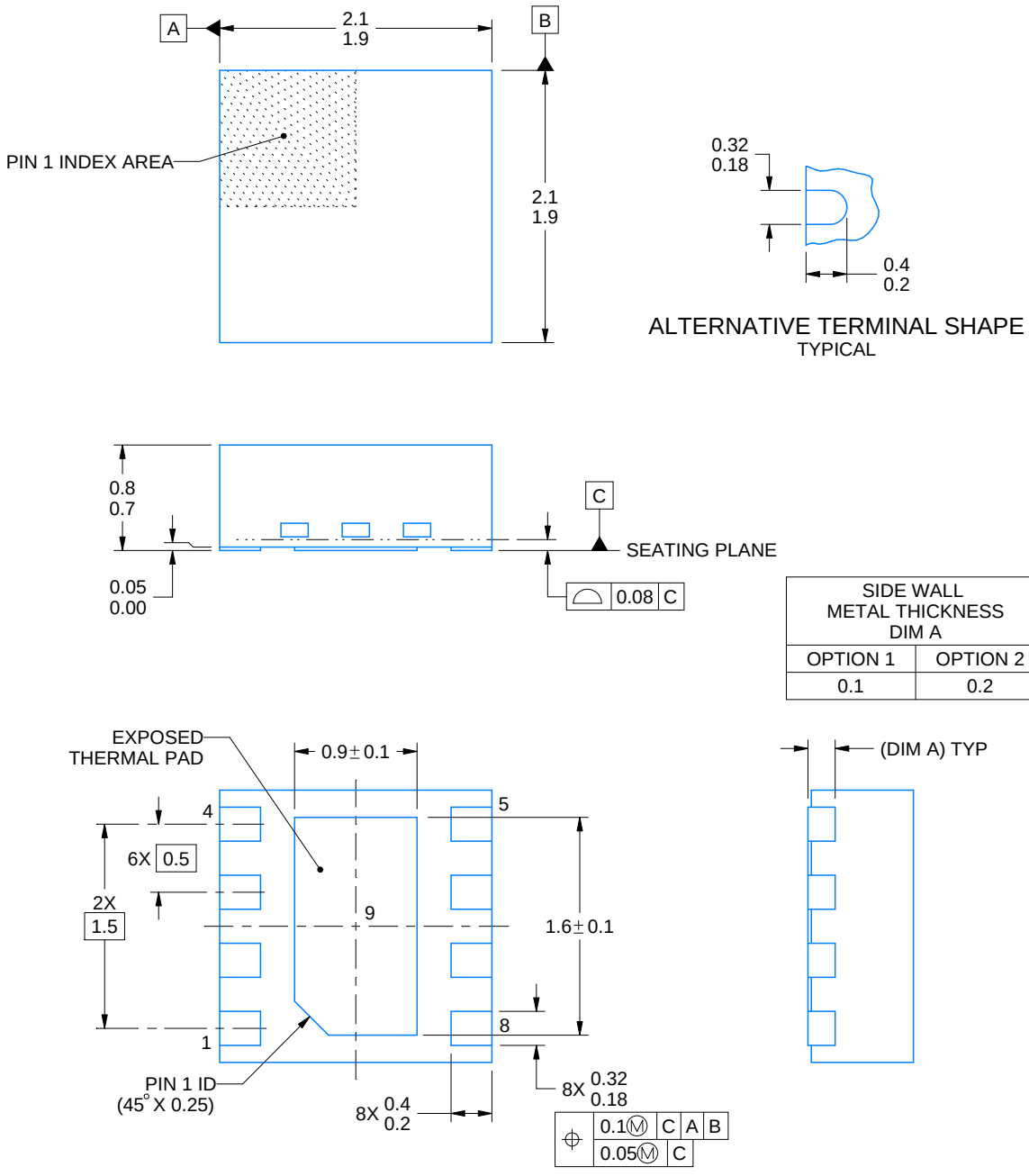

4224783/A

# PACKAGE OUTLINE

## DSG0008A

## WSON - 0.8 mm max height

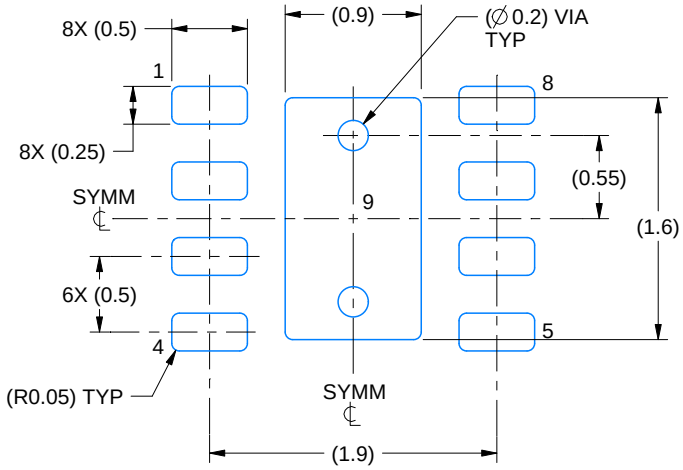
PLASTIC SMALL OUTLINE - NO LEAD



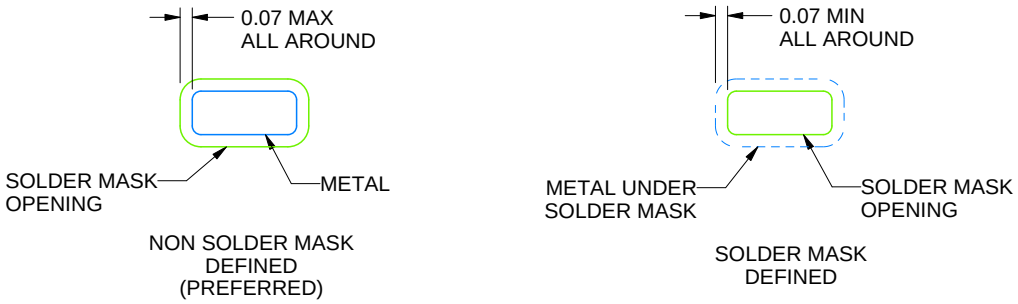

4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

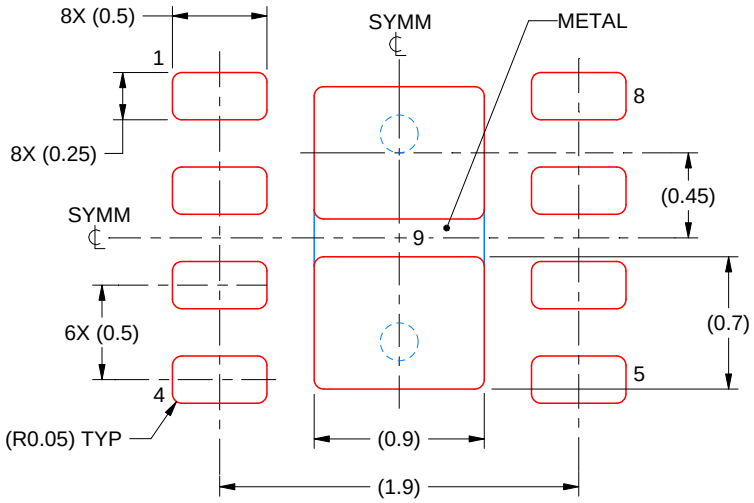



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

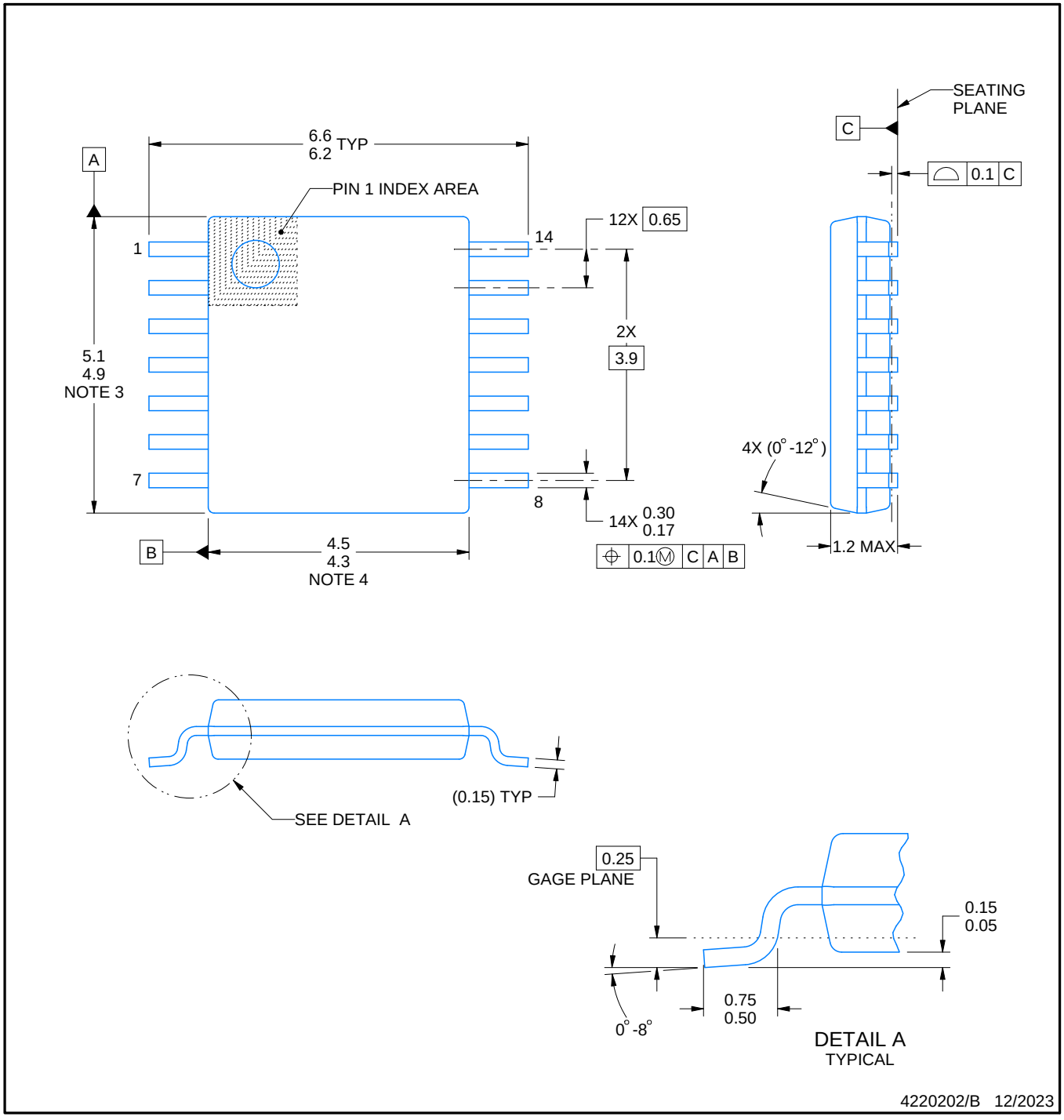
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PW0014A

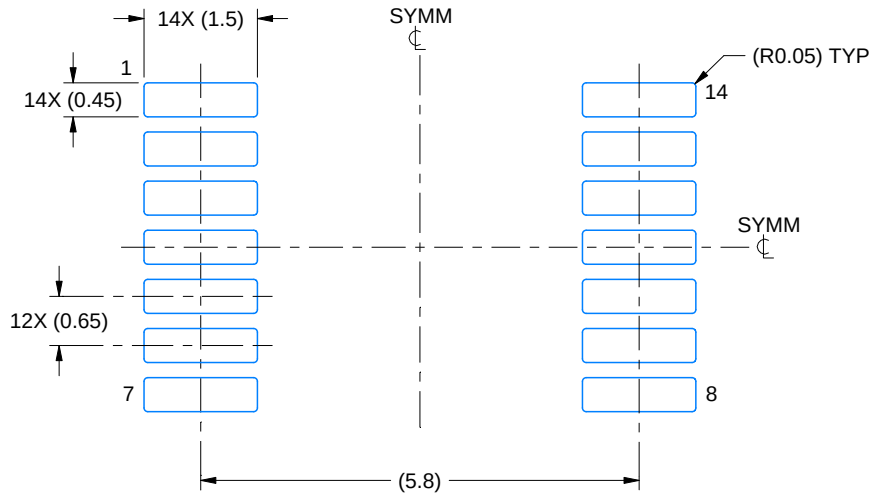
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

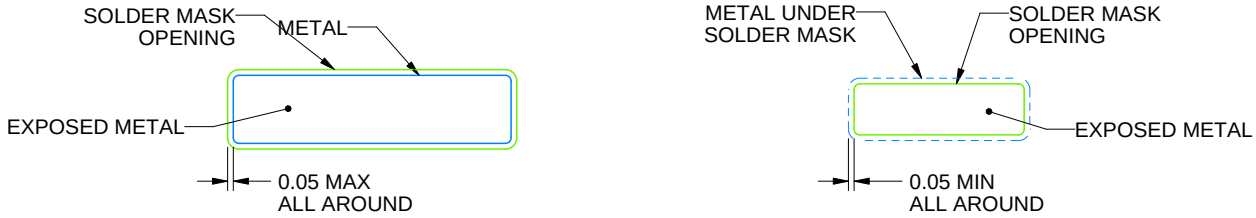



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

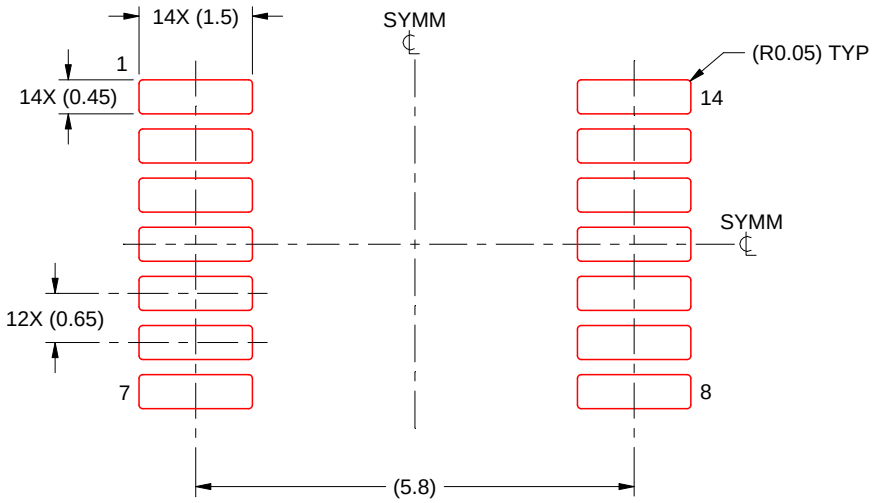



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

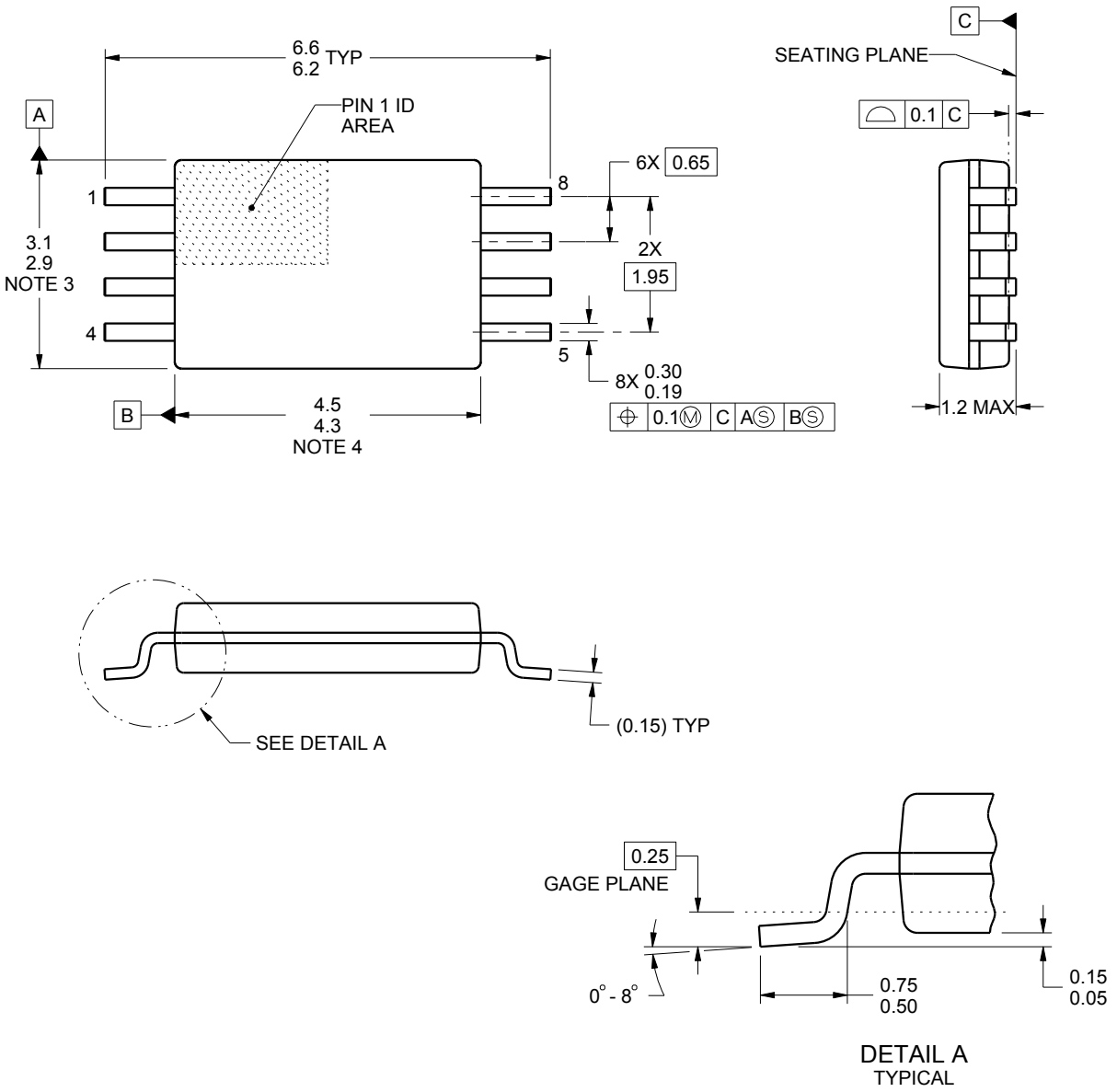
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0008A

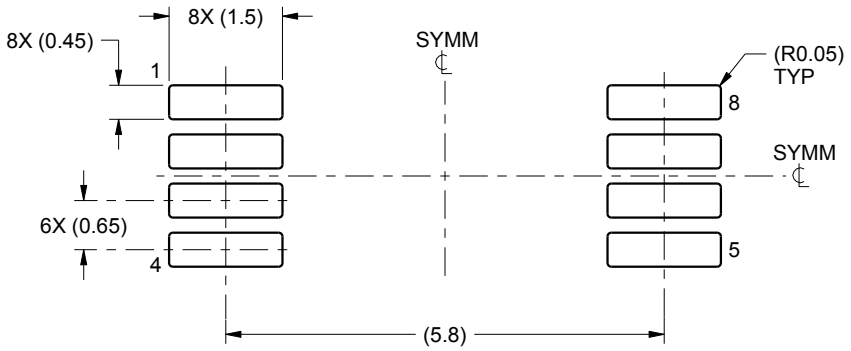
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

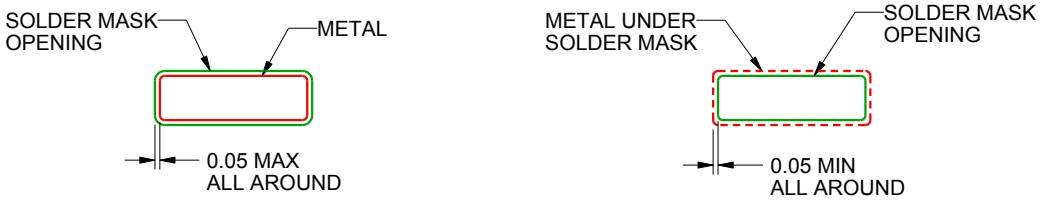



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

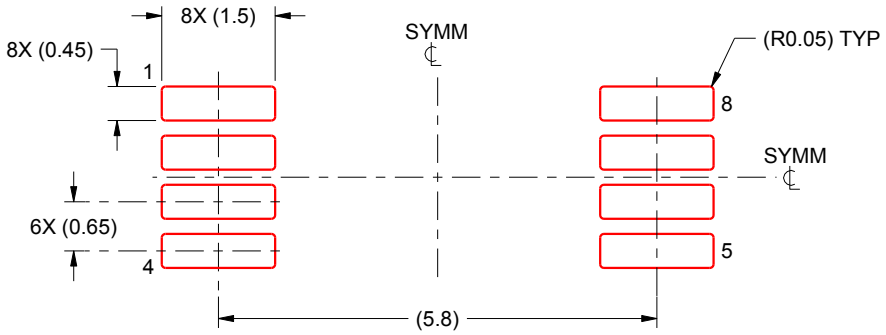



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

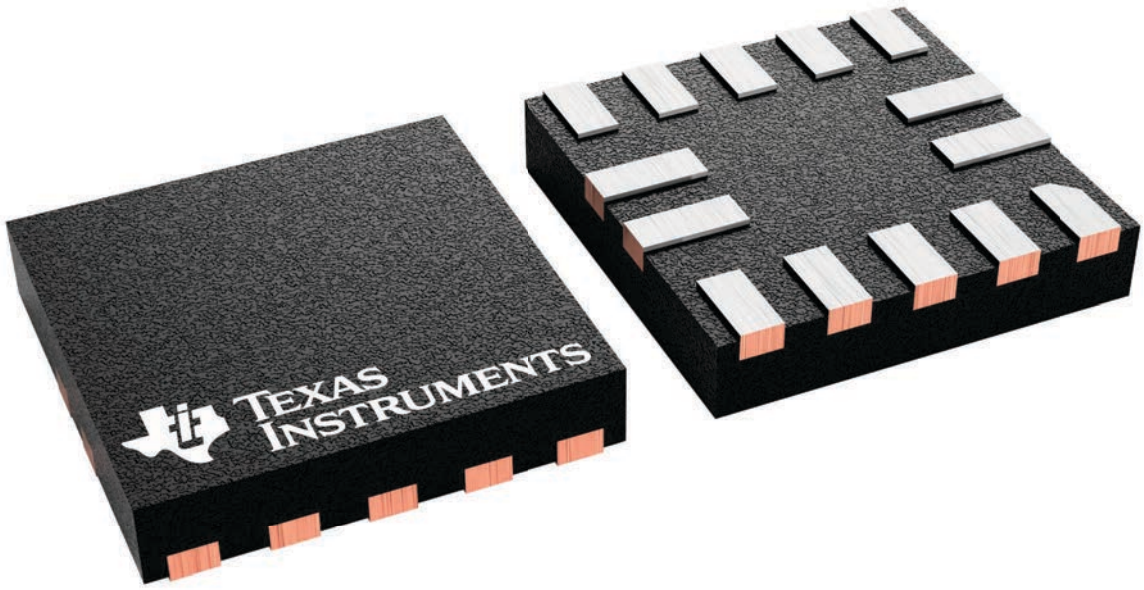
## RUC 14

## X2QFN - 0.4 mm max height

**2 x 2, 0.4 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

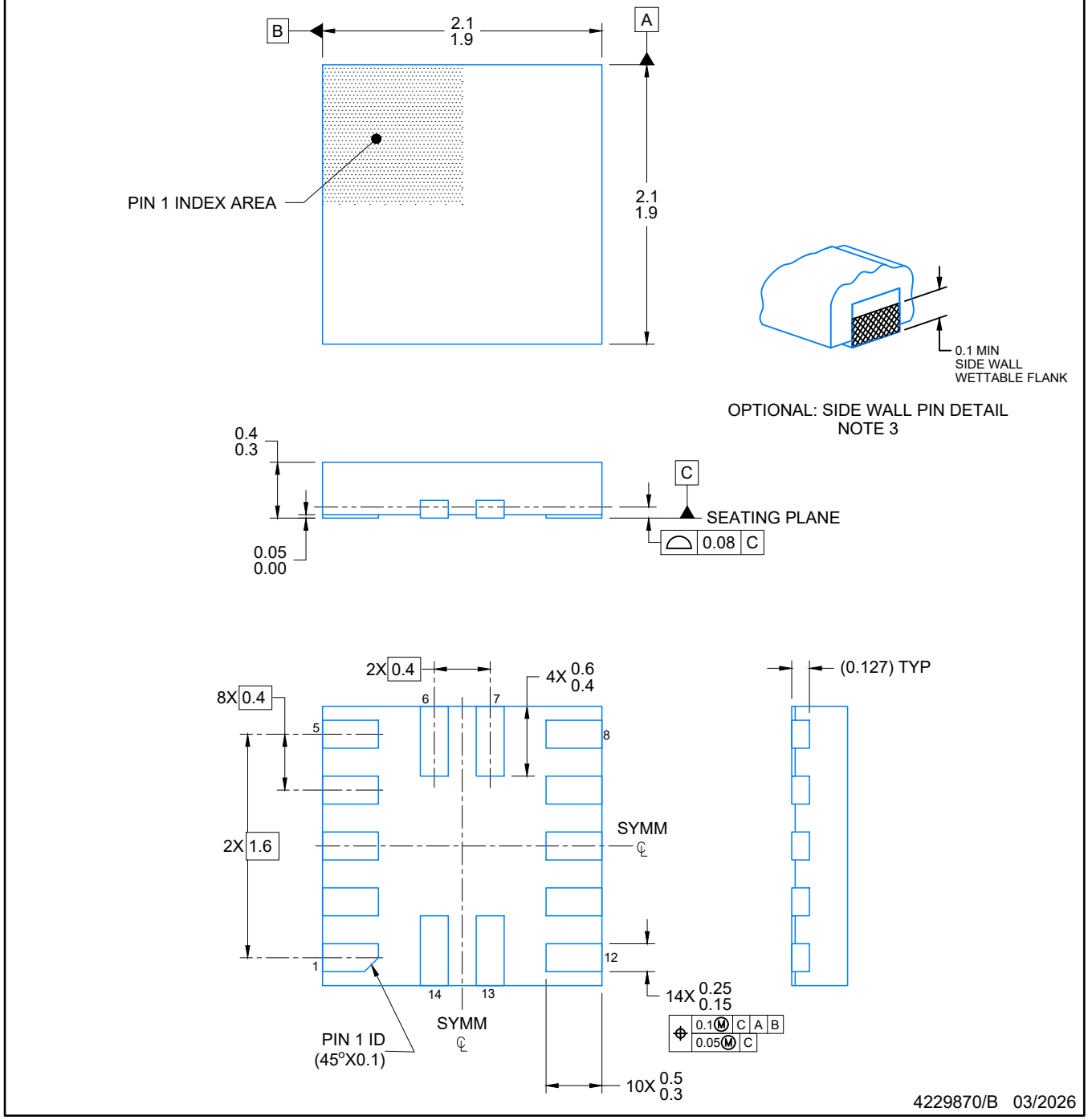


# PACKAGE OUTLINE

## RUC0014B

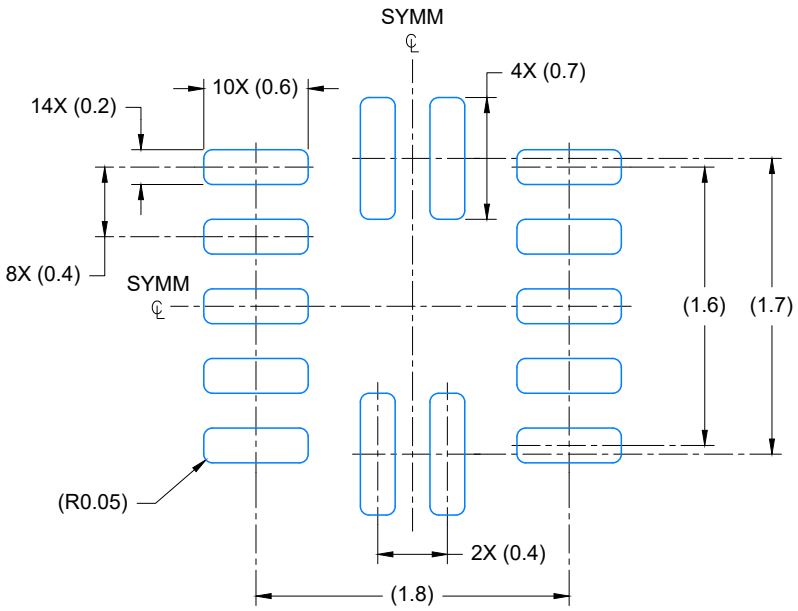
## X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

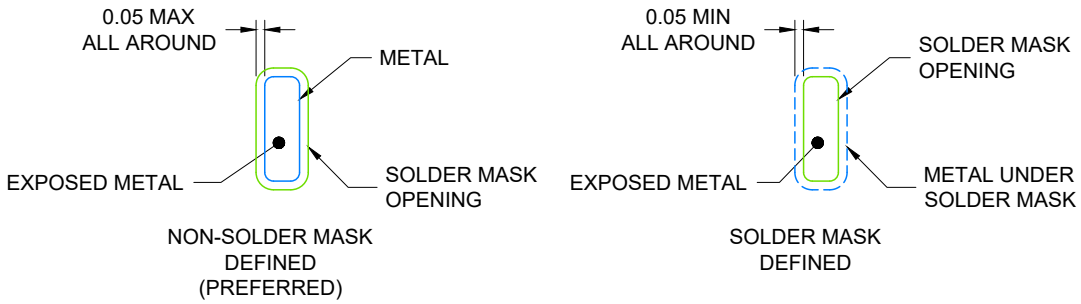



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

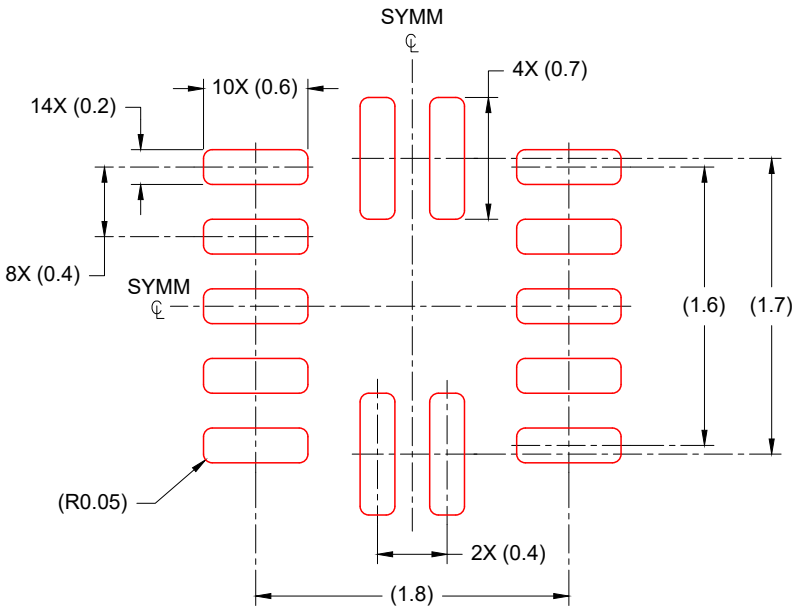



SOLDER MASK DETAILS

4229870/B 03/2026

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

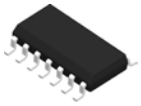



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4229870/B 03/2026

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

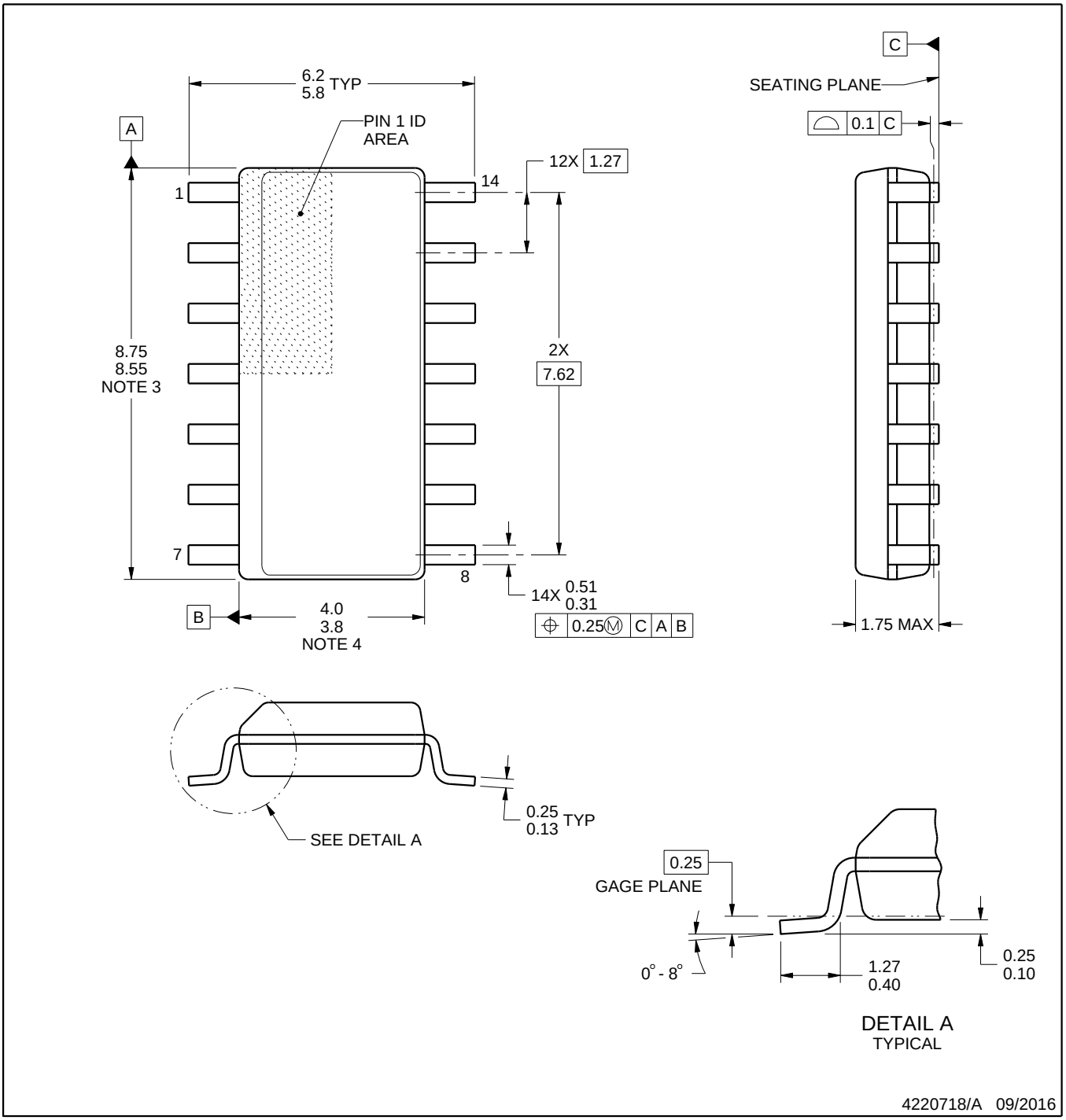


# PACKAGE OUTLINE

## D0014A

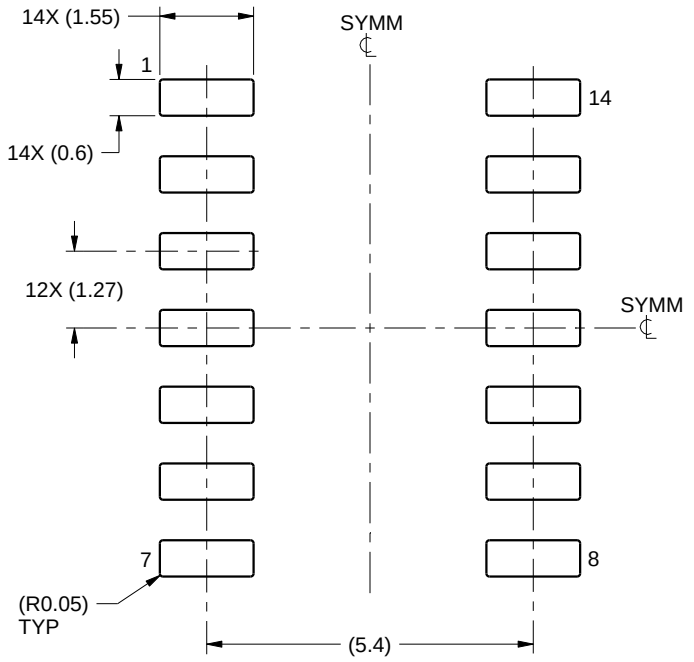
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

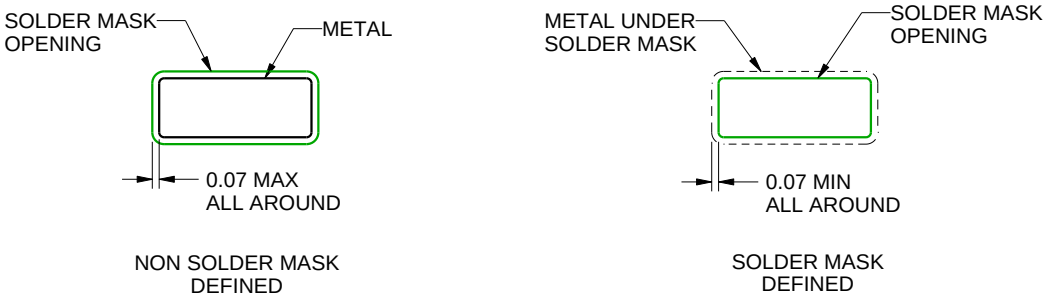



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

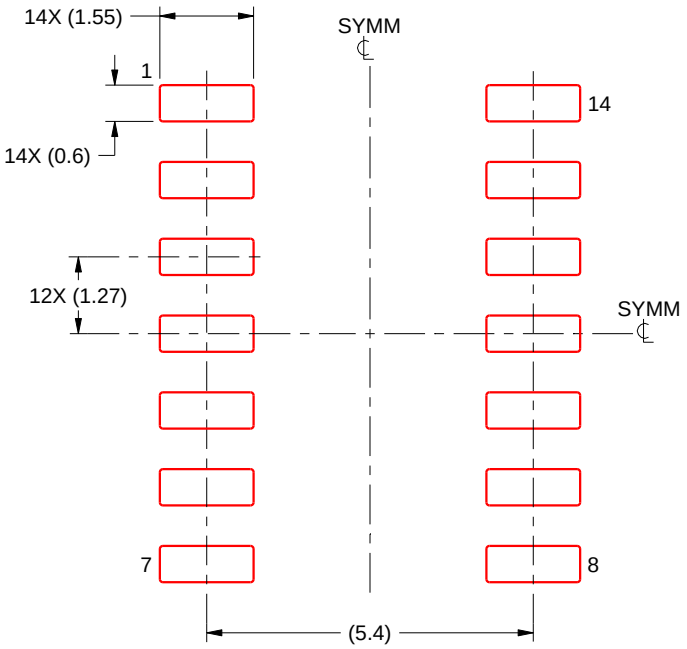
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

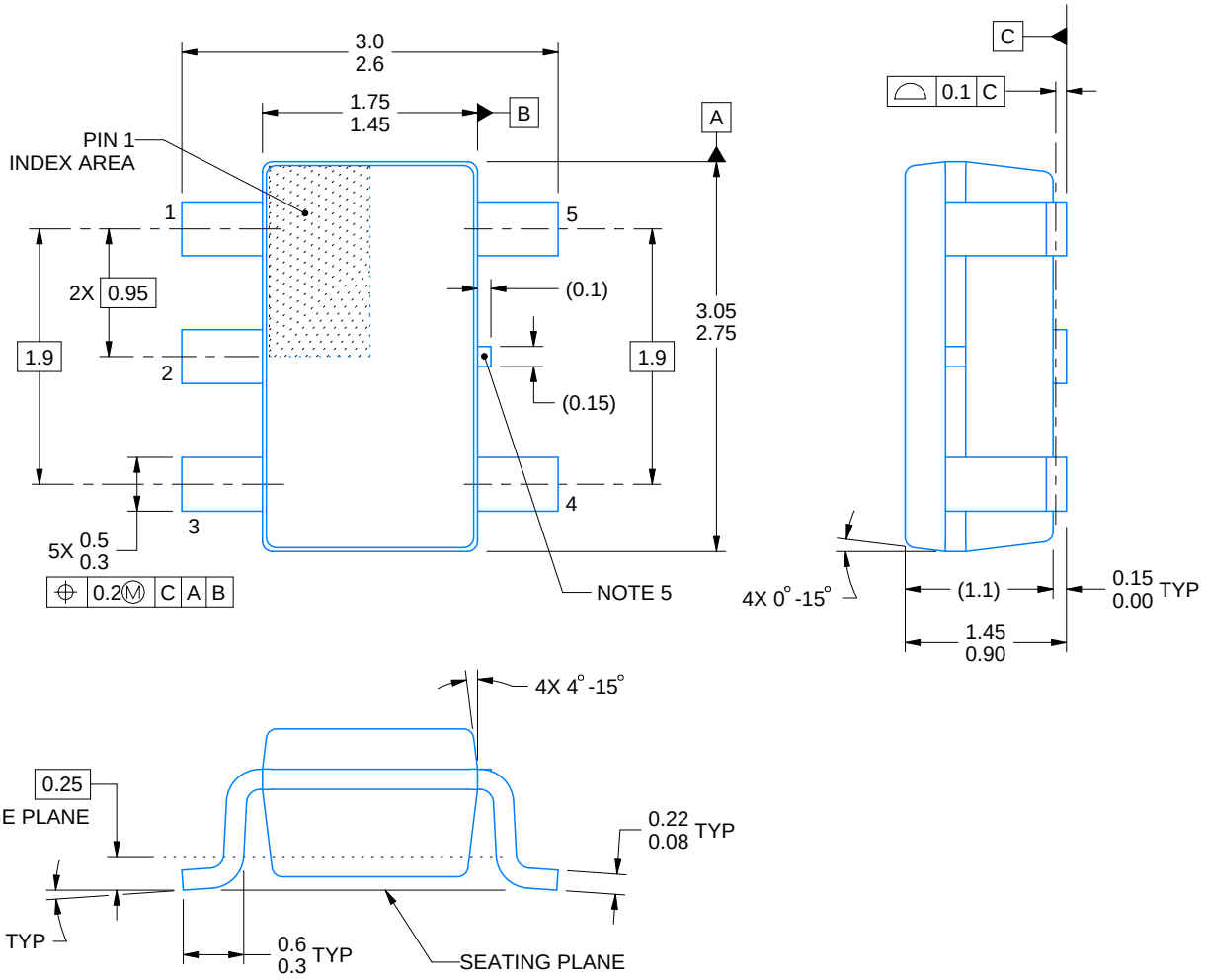
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

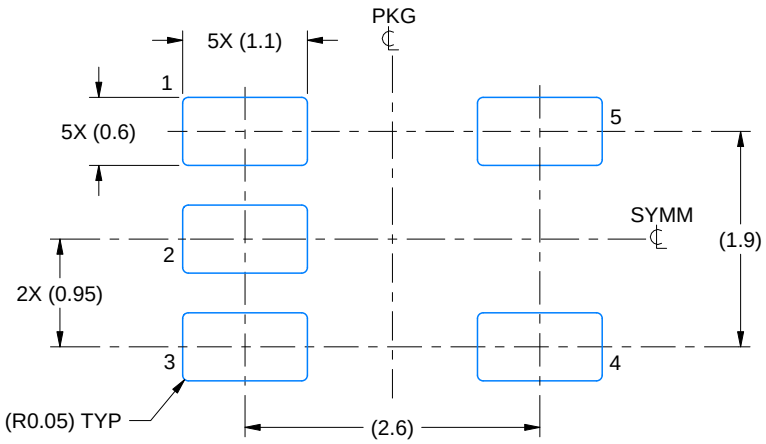
SMALL OUTLINE TRANSISTOR



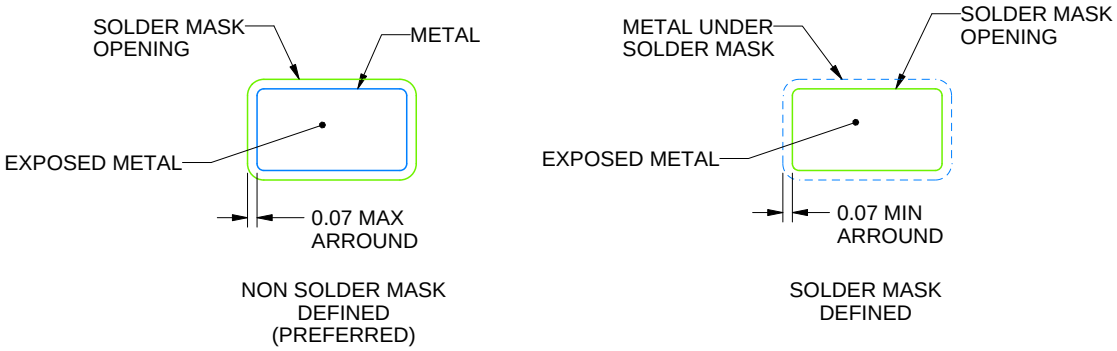

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

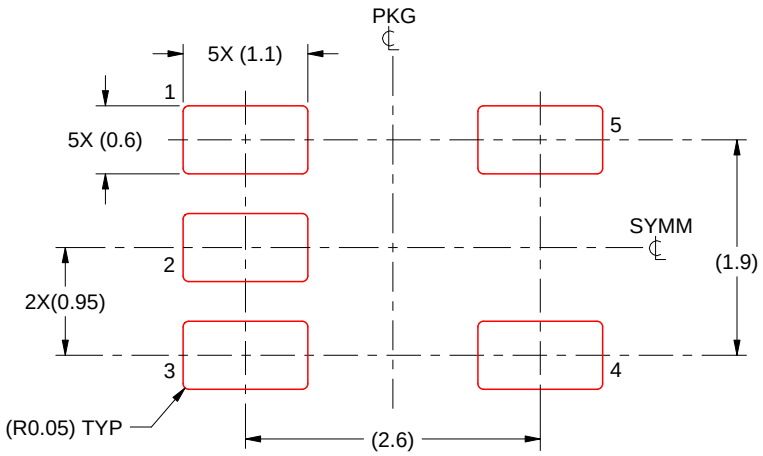



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

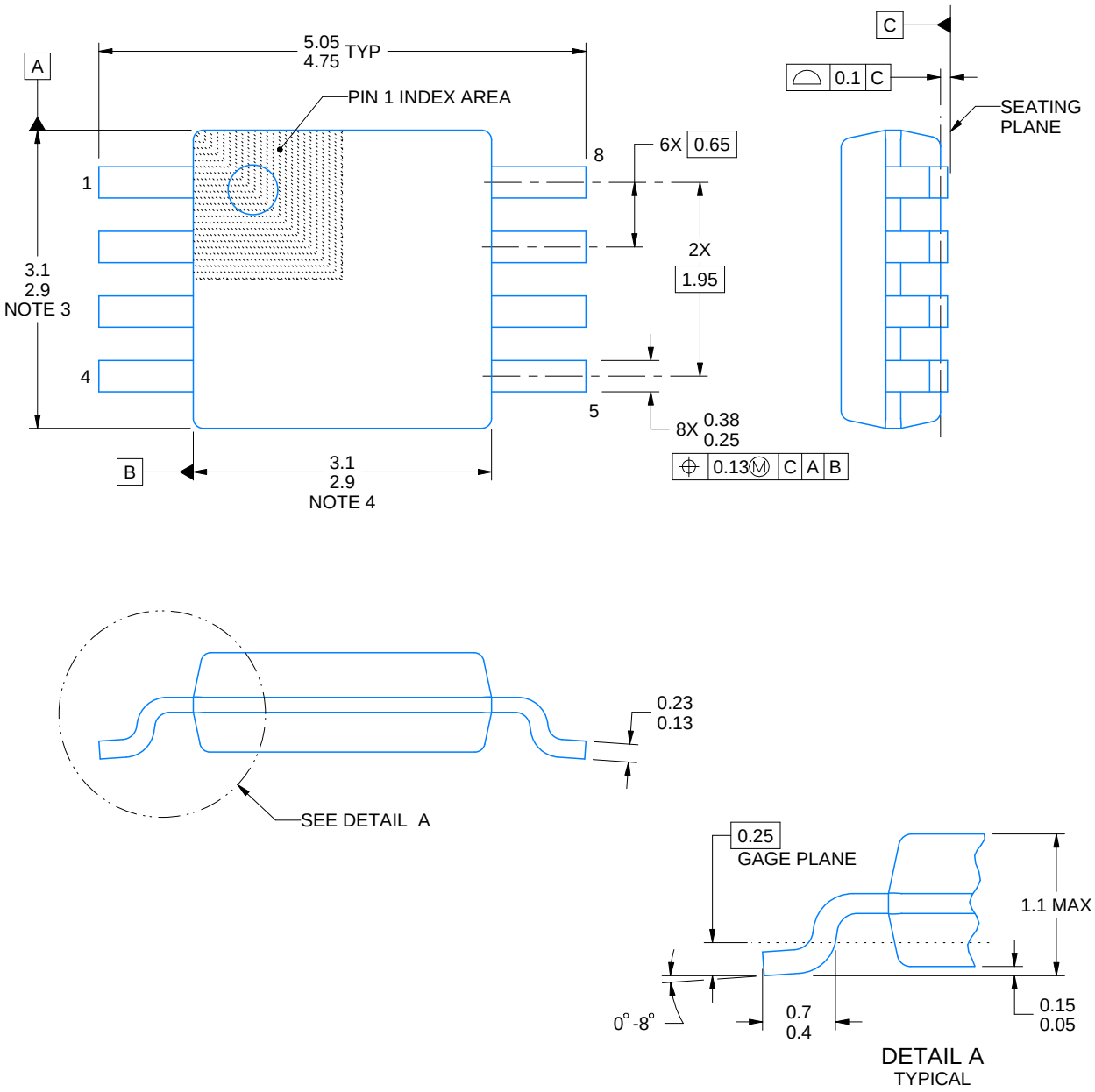
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

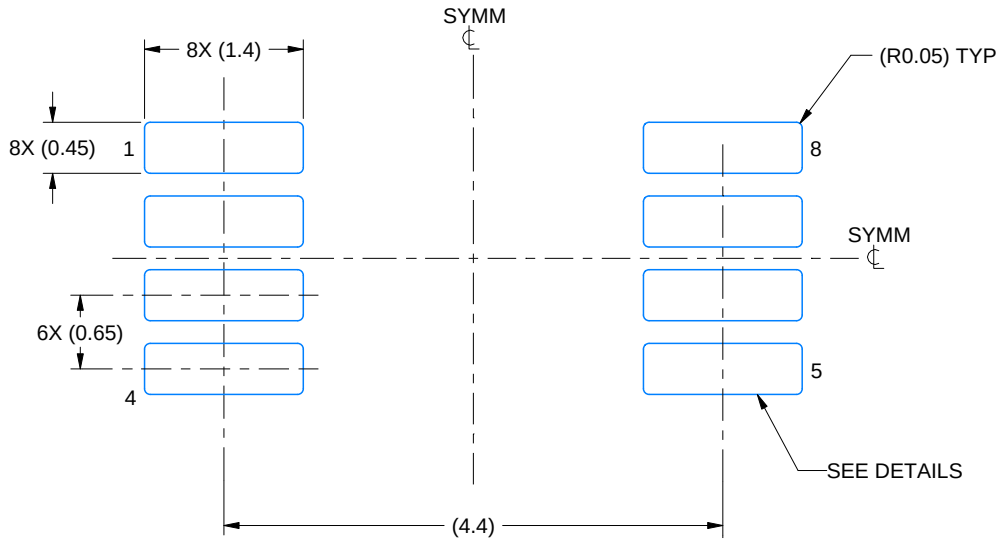
SMALL OUTLINE PACKAGE



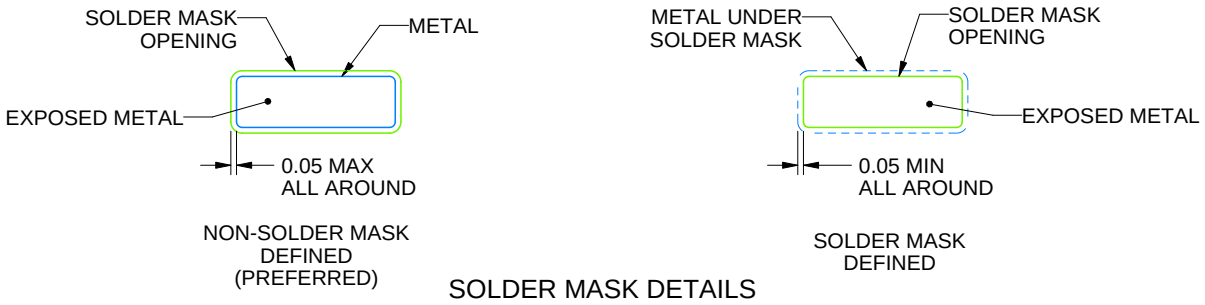

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

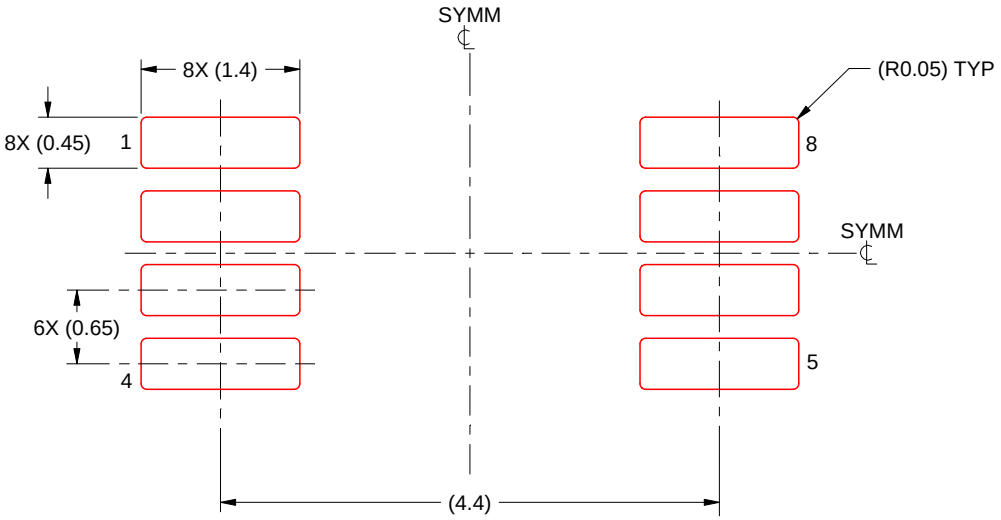



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

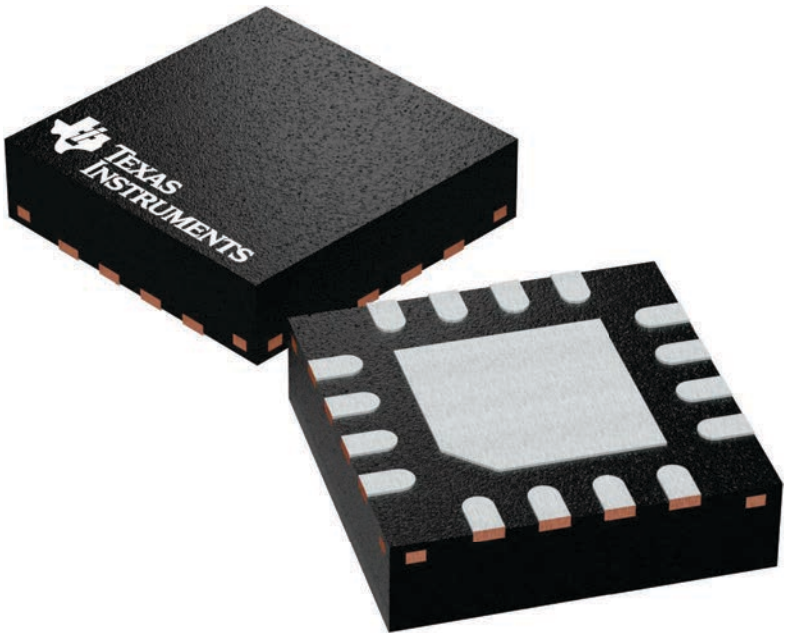
## RTE 16

## WQFN - 0.8 mm max height

**3 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

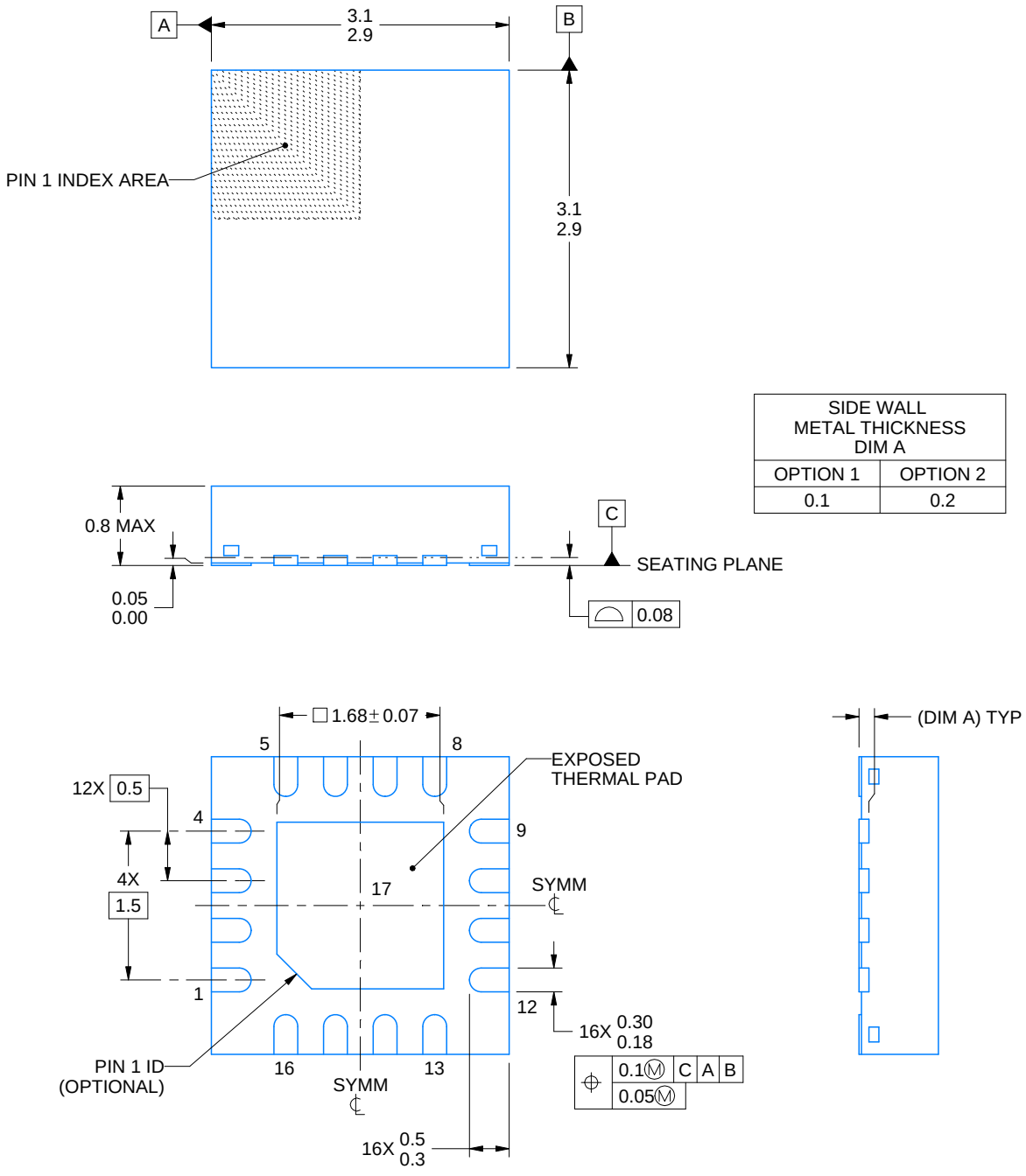


# RTE0016C

# PACKAGE OUTLINE

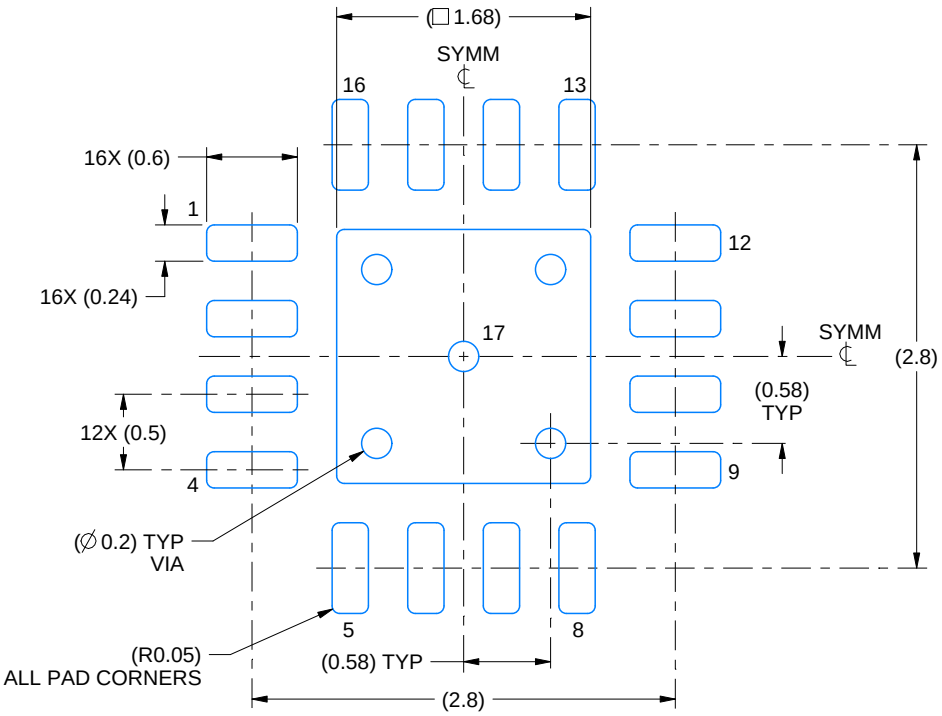
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

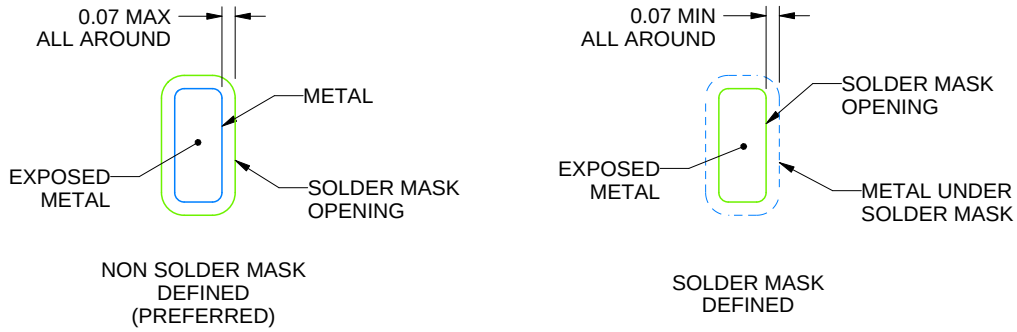



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

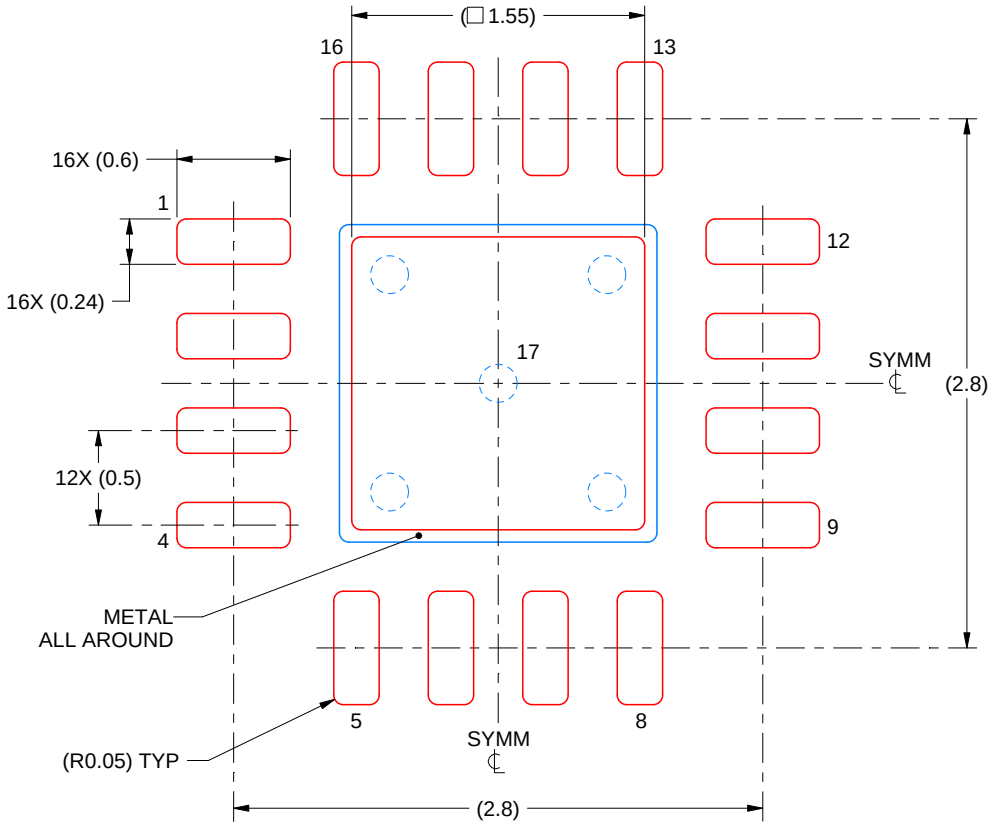



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

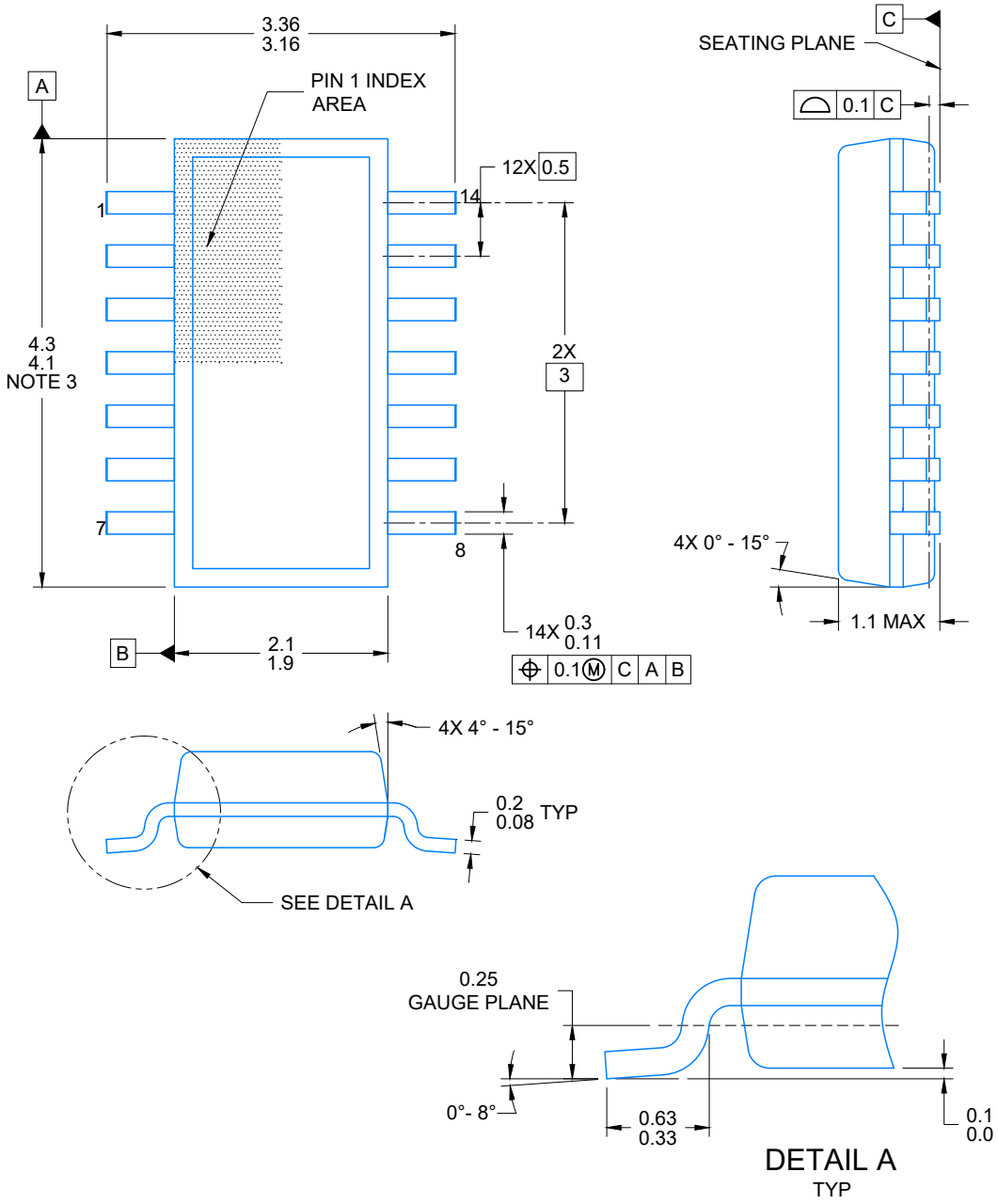
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DYY0014A

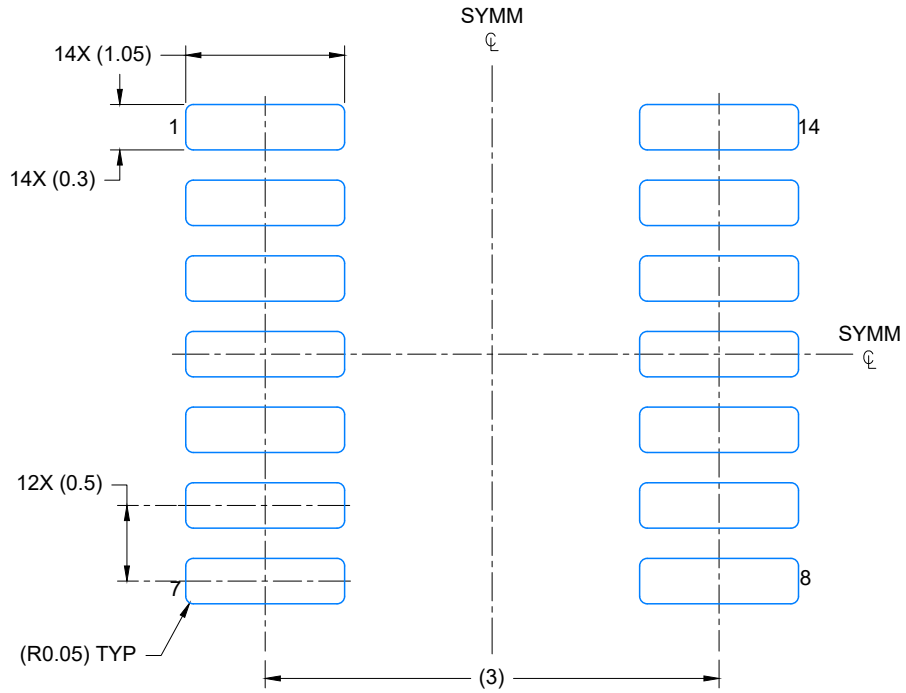
## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

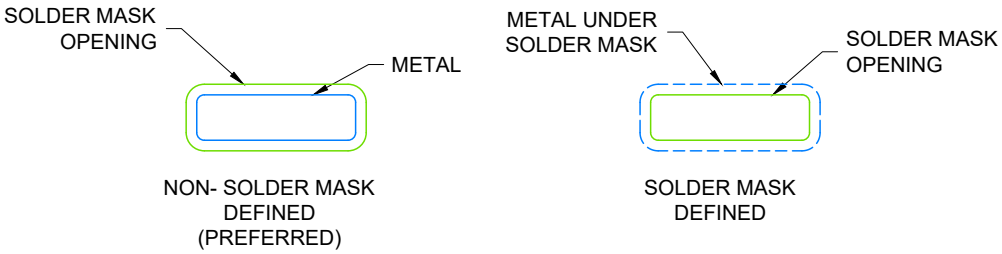



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

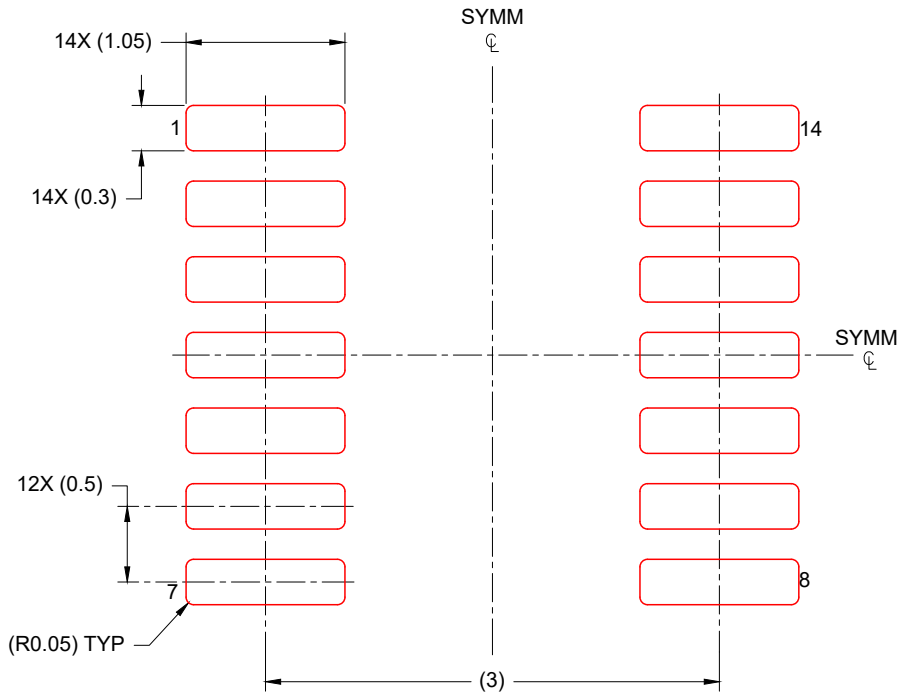



SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.



Last updated 10/2025