# TLV774-Q1 300mA, Small-Size, High-PSRR, Automotive Low-Dropout Regulator

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Ambient temperature: –40°C to +125°C, $T_A$
  - Junction temperature: –40°C to +150°C, $T_J$
- High PSRR: 60dB (1kHz), 45dB (1MHz)
- $V_{IN}$ range: 1.4V to 5.5V
- Fixed output voltage range: 0.6V to 3.3V
- Output voltage accuracy: 2%
- Low dropout voltage:
  - 165mV maximum at 300mA ($3.3V_{OUT}$)
- Foldback current limit
- Active output pulldown resistor
- Package: 2mm × 2mm, 6-pin WSON (DRV)

## 2 Applications

- Automotive head unit
- Automotive cluster display
- Passive entry passive start (PEPS)

## 3 Description

The TLV774-Q1 is a small, low-dropout (LDO) linear regulator that sources 300mA of output current. This LDO is designed to provide a voltage source with high PSRR. This device also provides load and line transient performance that meets the requirements of a variety of circuits. With a 1.4V to 5.5V input voltage range and a 0.6V to 3.3V output voltage range, the TLV774-Q1 is flexible enough for use in multiple applications.

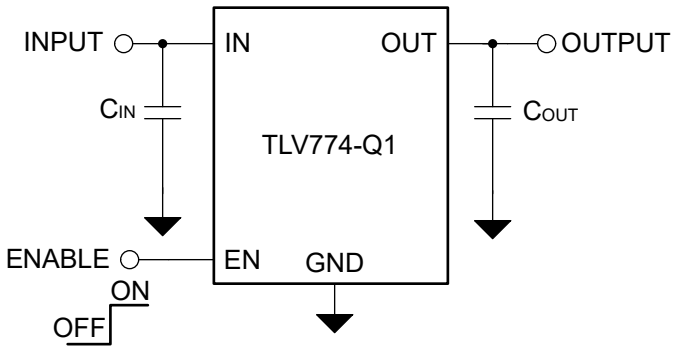
The TLV774-Q1 features an internal soft-start circuit to avoid excessive inrush current, therefore minimizing the input voltage drop during start-up. An active pulldown circuit quickly discharges the output when the LDO is disabled and provides a known start-up state. The EN input allows an external logic signal to enable or disable the regulated output. The LDO is stable with small ceramic capacitors, allowing for a small overall package size. The operating junction temperature range is from −40°C to +150°C. This LDO is available in a standard 2mm × 2mm WSON (DRV) package.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TLV774-Q1 | DRV (WSON, 6) | 2mm × 2mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ADVANCE INFORMATION




**Typical Application Circuit**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

ADVANCE INFORMATION

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Pin Configuration and Functions**....3
**5 Specifications**....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....5
5.5 Electrical Characteristics....5
5.6 Switching Characteristics....6
5.7 Typical Characteristics....7
**6 Detailed Description**....10
6.1 Overview....10
6.2 Functional Block Diagram....10
6.3 Feature Description....10
6.4 Device Functional Modes....12
**7 Application and Implementation**....13
7.1 Application Information....13
7.2 Typical Application....14
7.3 Power Supply Recommendations....15
7.4 Layout....15
**8 Device and Documentation Support**....16
8.1 Device Support....16
8.2 Documentation Support....16
8.3 Receiving Notification of Documentation Updates....16
8.4 Support Resources....16
8.5 Trademarks....16
8.6 Electrostatic Discharge Caution....16
8.7 Glossary....16
**9 Revision History**....16
**10 Mechanical, Packaging, and Orderable Information**....17


Copyright © 2026 Texas Instruments Incorporated

# 4 Pin Configuration and Functions

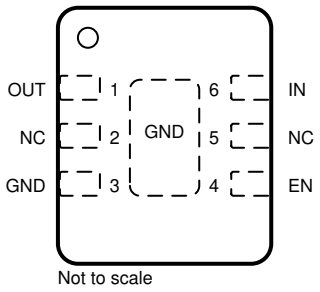



**Figure 4-1. DRV Package, 2mm × 2mm, 6-Pin WSON (Top View)**

**Table 4-1. Pin Functions**

| NAME | WSON | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| EN | 4 | I | Enable input. A low voltage (< $V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{EN(HI)}$) on this pin enables the regulator output. |
| GND | 3 | G | Common ground |
| IN | 6 | I | Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground. See the *Section 5.3* table. Place the input capacitor as close to the IN and GND pins of the device as possible. |
| NC | 2, 5 | — | No internal connection |
| OUT | 1 | O | Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Section 5.3* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal pulldown resistor prevents a charge from remaining on $V_{OUT}$ when the regulator is in shutdown mode ($V_{EN}$< $V_{EN(LOW)}$). |
| Thermal Pad | | — | Thermal pad for the package. Connect this pad to GND or leave floating.<br>Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance. |

(1) I = input, O = output, I/O = input or output, and G = ground.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | Input, $V_{IN}$ | | –0.3 | 6.5 | V |
| | Output, $V_{OUT}$ | | –0.3 | 6.0 or $V_{IN}$ + 0.3 (2) | |
| | Enable, $V_{EN}$ | | –0.3 | 6.5 | |
| Current | Maximum output, $I_{OUT}$(4) | | Internally limited | | |
| Power | Maximum power dissipation, $P_D$ | DRV (SON) | | 600 | mW |
| Temperature | Operating junction, $T_J$ | | –55 | 150 | °C |
| | Storage, $T_{stg}$ | | –65 | 150 | |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The maximum value of $V_{OUT}$ is the lesser of 6.0V or ($V_{IN}$ + 0.3V).
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage | 1.4 | | 5.5 | V |
| $V_{EN}$ | Enable input voltage | 0 | | 5.5 | V |
| $V_{OUT}$ | Nominal output voltage range | 0.6 | | 3.3 | V |
| $I_{OUT}$ | Output current | 0 | | 300 | mA |
| $C_{IN}$ | Input capacitor(2) | | 1 | | µF |
| $C_{OUT}$ | Output capacitance(3) | 0.47 | | 47 | µF |
| ESR | Output capacitor effective series resistance | | | 100 | mΩ |
| $T_J$ | Operating junction temperature | –40 | | 150 | °C |
| $T_A$ | Operating ambient temperature | –40 | | 125 | °C |

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47µF minimum is recommended to counteract the effect of source resistance and inductance, which in some cases causes symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients. If needed use a larger input capacitance, depending on the characteristics of the input voltage source.
(3) Effective output capacitance of 0.47µF minimum and 40µF maximum is required for stability. The effective output capacitance must account for tolerance, temperature, voltage, and any other factors that affect the value, and is often 50% smaller than the capacitors specified value.


Copyright © 2026 Texas Instruments Incorporated

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TLV774-Q1 DRV (WSON) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.5 Electrical Characteristics

specifications apply for $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V or 1.4V, whichever is greater, $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 1mA, $C_{IN}$ = 1µF, and $C_{OUT}$ = 1µF (unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta V_{OUT}$ | Output voltage tolerance | | 0.6V ≤ $V_{OUT}$ < 1.8V | –2.5 | | 2.5 | % |
| | | | 1.8V ≤ $V_{OUT}$ ≤ 3.3V | –2 | | 2 | |
| | | $T_J$ = –40°C to 150°C | 0.6V ≤ $V_{OUT}$ < 1.8V | –3.33 | | 3.33 | |
| | | | 1.8V ≤ $V_{OUT}$ ≤ 3.3V | –3 | | 3 | |
| $\Delta V_{OUT}$ / $\Delta V_{IN}$ | Line regulation | $V_{IN}$ = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V | | | 0.01 | 0.1 | %/V |
| $\Delta V_{OUT}$ / $\Delta I_{OUT}$ | Load regulation | $I_{OUT}$ = 1mA to 300mA | | | 85 | 110 | µV/mA |
| $I_{GND}$ | Quiescent ground current | $I_{OUT}$ = 0mA, $T_J$ = –40°C to 150°C | $V_{EN}$ = $V_{IN}$ = 1.6V | | 80 | | µA |
| | | | $V_{EN}$ = $V_{IN}$ = 4V | | 94 | | |
| | | | $V_{EN}$ = $V_{IN}$ = 5.5V | | 102 | 153 | |
| $I_{SHDN}$ | Shutdown ground current | $V_{EN}$ < $V_{EN(LOW)}$, $V_{IN}$ = 5.5V, $T_J$ = –40°C to 150°C | | | 0.01 | 2 | µA |
| $V_{DO}$ | Dropout voltage | $I_{OUT}$ = 300mA, $V_{IN}$ = $V_{OUT(NOM)}$ | 1.2V ≤ $V_{OUT}$ < 1.8V[1] | | | 360 | mV |
| | | | 1.8V ≤ $V_{OUT}$ < 2.5V | | | 200 | |
| | | | 2.5V ≤ $V_{OUT}$ < 2.8V | | | 150 | |
| | | | 2.8V ≤ $V_{OUT}$ ≤ 3.3V | | | 165 | |
| | | $I_{OUT}$ = 300mA, $V_{IN}$ = $V_{OUT(NOM)}$, $T_J$ = –40°C to 150°C | 1.2V ≤ $V_{OUT}$ < 1.8V[1] | | | 370 | |
| | | | 1.8V ≤ $V_{OUT}$ < 2.5V | | | 260 | |
| | | | 2.5V ≤ $V_{OUT}$ < 2.8V | | | 190 | |
| | | | 2.8V ≤ $V_{OUT}$ ≤ 3.3V | | | 200 | |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.8 × $V_{OUT(NOM)}$, $T_J$ = –40°C to 150°C | | 400 | | 800 | mA |
| $I_{SC}$ | Short-circuit current limit | $V_{OUT}$ = 0V | | | 75 | | mA |
| PSRR | Power-supply rejection ratio | $I_{OUT}$ = 150mA, $V_{IN}$ = $V_{OUT}$ + 1.0V | f = 1kHz | | 60 | | dB |
| | | | f = 100kHz | | 56 | | |
| | | | f = 1MHz | | 45 | | |
| $V_N$ | Output noise voltage | BW = 10Hz to 100kHz, $I_{OUT}$ = 50mA | | | 75 × Vout | | $\mu V_{RMS}$ |
| $R_{PULLDOWN}$ | Output automatic discharge pulldown resistance | $V_{EN}$ < $V_{EN(LOW)}$ (output disabled), $V_{IN}$ = 3.3V | | | 135 | | Ω |
| $T_{SD}$ | Thermal shutdown | $T_J$ rising | | | 165 | | °C |
| | | $T_J$ falling | | | 155 | | |
| $V_{EN(LOW)}$ | EN pin low (disabled) | $T_J$ = –40°C to 150°C | | 0 | | 0.35 | V |
| $V_{EN(HI)}$ | EN pin high (enabled) | $T_J$ = –40°C to 150°C | | 0.9 | | 5.5 | V |
| $V_{EN(HYST)}$ | Enable hysteresis | | | | 33 | | mV |
| $V_{UVLO}$ | UVLO threshold | $V_{IN}$ rising | | | 1.3 | 1.39 | V |
| | | $V_{IN}$ falling | | | 1.25 | | |
| $V_{UVLO(HYST)}$ | UVLO hysteresis | | | | 55 | | mV |

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

## 5.5 Electrical Characteristics (continued)

specifications apply for $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V or 1.4V, whichever is greater, $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 1mA, $C_{IN}$ = 1µF, and $C_{OUT}$ = 1µF (unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{EN}$ | EN input leakage current | $V_{IN}$ = $V_{EN}$ = 5.5V | | 0.01 | 1 | µA |

(1) For $V_{OUT}$ < 1.4V, dropout is tested with $V_{IN}$ = 1.4V.

## 5.6 Switching Characteristics

specifications apply for $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V or 1.4V, whichever is greater, $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 1mA, $C_{IN}$ = 1µF, and $C_{OUT}$ = 1µF (unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STR}$ | Start-up time ($V_{EN}$) | From $V_{EN}$ > $V_{EN(HI)}$ to $V_{OUT}$ = 95% of $V_{OUT(NOM)}$, $V_{IN}$ rise time = 1V/µs | | 400 | | µs |

ADVANCE INFORMATION


Copyright © 2026 Texas Instruments Incorporated

## 5.7 Typical Characteristics

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V, $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)

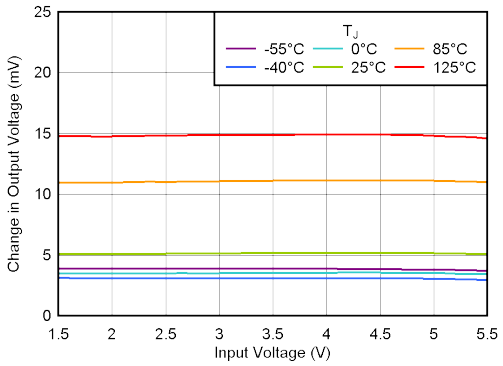



**Figure 5-1. Line Regulation vs $V_{IN}$**

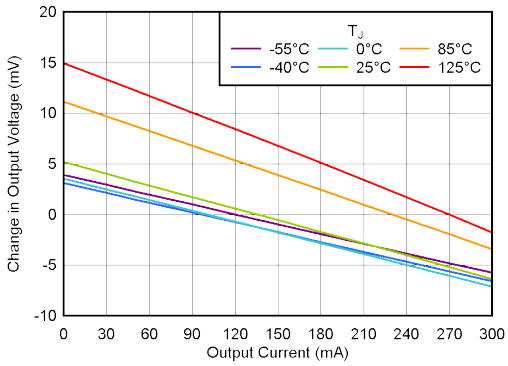



**Figure 5-2. Load Regulation vs $I_{OUT}$**

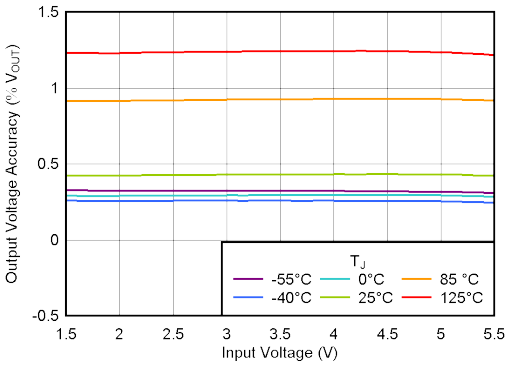



**Figure 5-3. Output Voltage Accuracy vs $V_{IN}$**

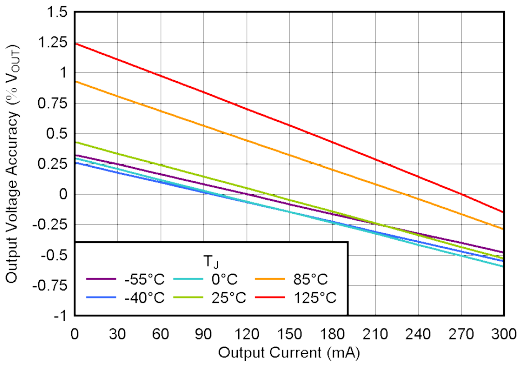
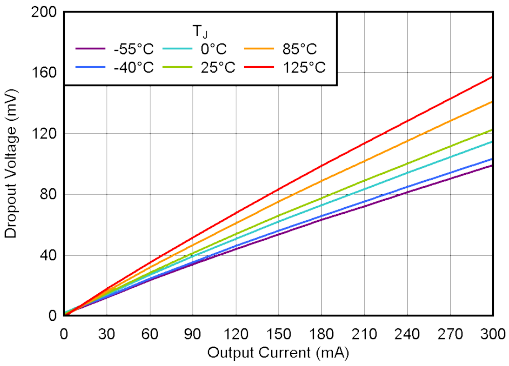
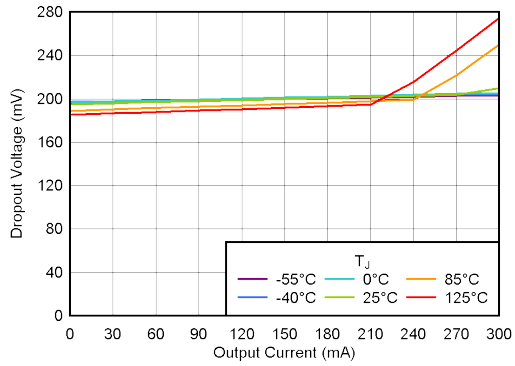



**Figure 5-4. Output Voltage Accuracy vs $I_{OUT}$**




$V_{OUT}$ = 3.3V, test condition: $V_{IN}$ = $V_{OUT(NOM)}$

**Figure 5-5. Dropout Voltage vs $I_{OUT}$**




$V_{OUT}$ = 1.2V, test condition: $V_{IN}$ = 1.4V

**Figure 5-6. Dropout Voltage vs $I_{OUT}$**

ADVANCE INFORMATION

ADVANCE INFORMATION

## 5.7 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V, $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)

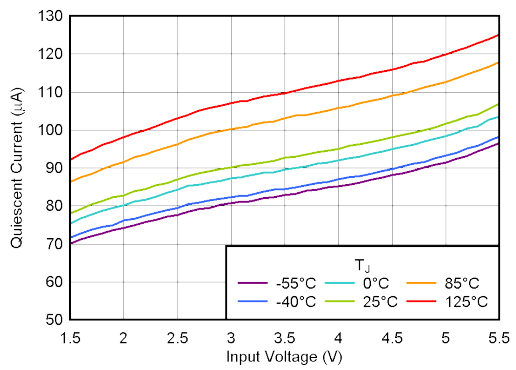



**Figure 5-7. Quiescent Current vs $V_{IN}$**

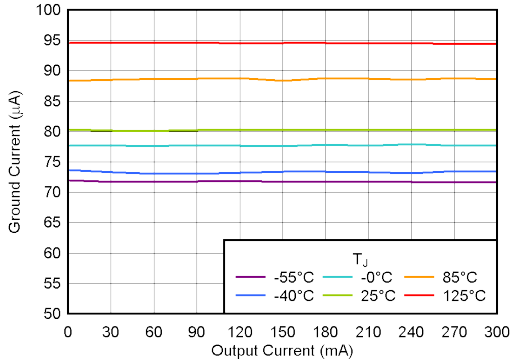
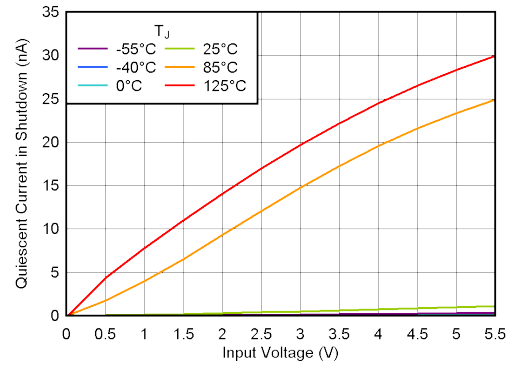
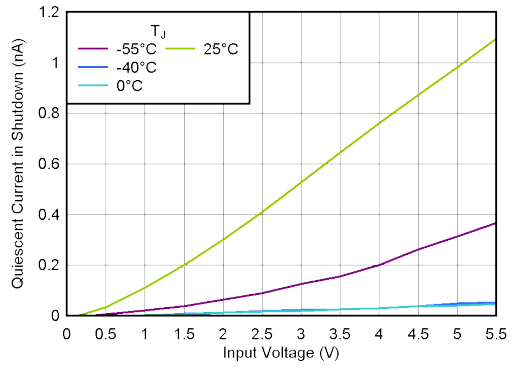



**Figure 5-8. Ground Current vs $I_{OUT}$**




$V_{EN}$ = 0V, $C_{IN}$ = 0µF

**Figure 5-9. Shutdown Current vs $V_{IN}$**




$V_{EN}$ = 0V, $C_{IN}$ = 0µF

**Figure 5-10. Shutdown Current vs $V_{IN}$**

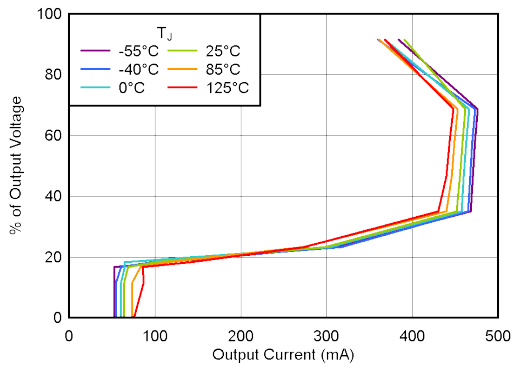



**Figure 5-11. Current Limit**

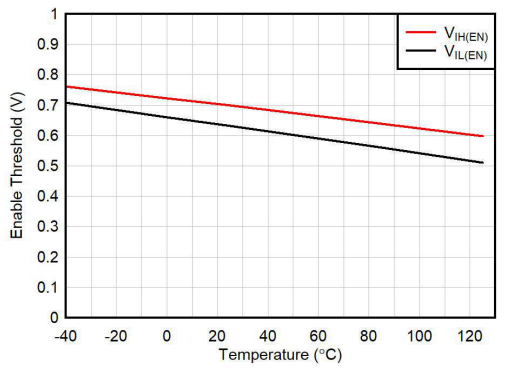
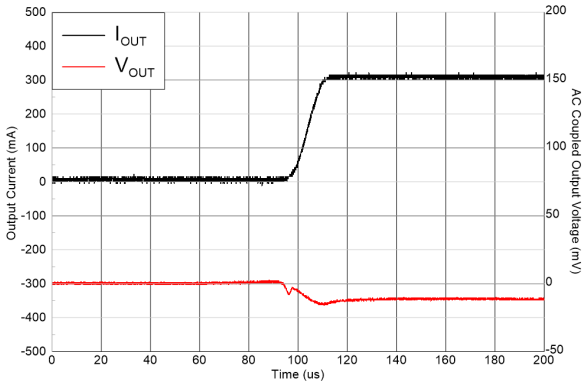



**Figure 5-12. Enable Logic Threshold vs Temperature**


Copyright © 2026 Texas Instruments Incorporated

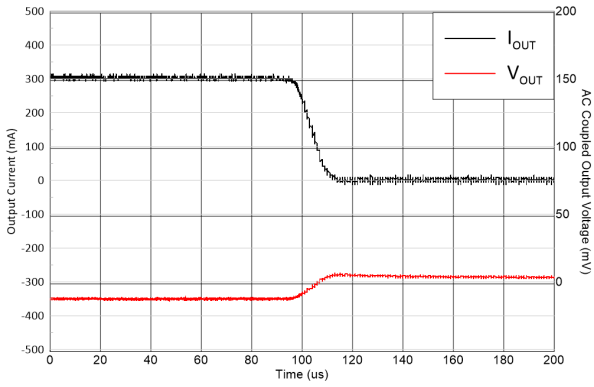
## 5.7 Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V, $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



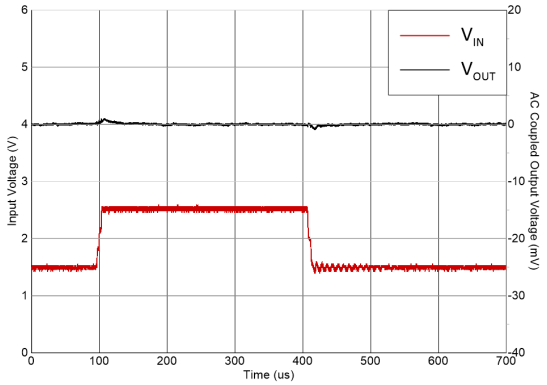

$V_{IN}$ = $V_{OUT(nom)}$ + 1.0V, $I_{OUT}$ = 0mA to 300mA, $t_{RISING}$ = 10µs

**Figure 5-13. Load Transient**



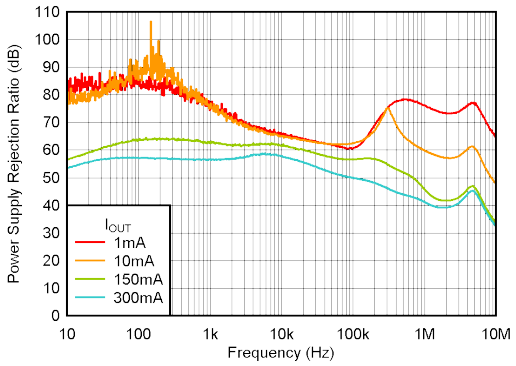

$V_{IN}$ = $V_{OUT(nom)}$ + 1.0V, $I_{OUT}$ = 300mA to 0mA, $t_{FALLING}$ = 10µs

**Figure 5-14. Load Transient**




$V_{IN}$ = $V_{OUT}$ + 0.3V to $V_{OUT}$ +1.3V

**Figure 5-15. Line Transient**




$V_{IN}$ = $V_{OUT(nom)}$ + 1.0V

**Figure 5-16. PSRR vs Frequency**

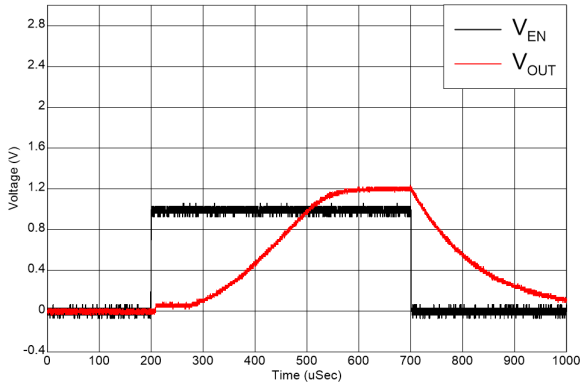
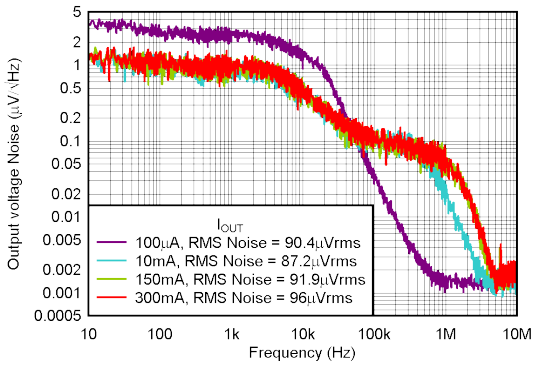



**Figure 5-17. Start-Up**




$V_{OUT}$ = 1.2V, RMS noise BW = 10Hz to 100kHz

**Figure 5-18. Noise**

ADVANCE INFORMATION

ADVANCE INFORMATION

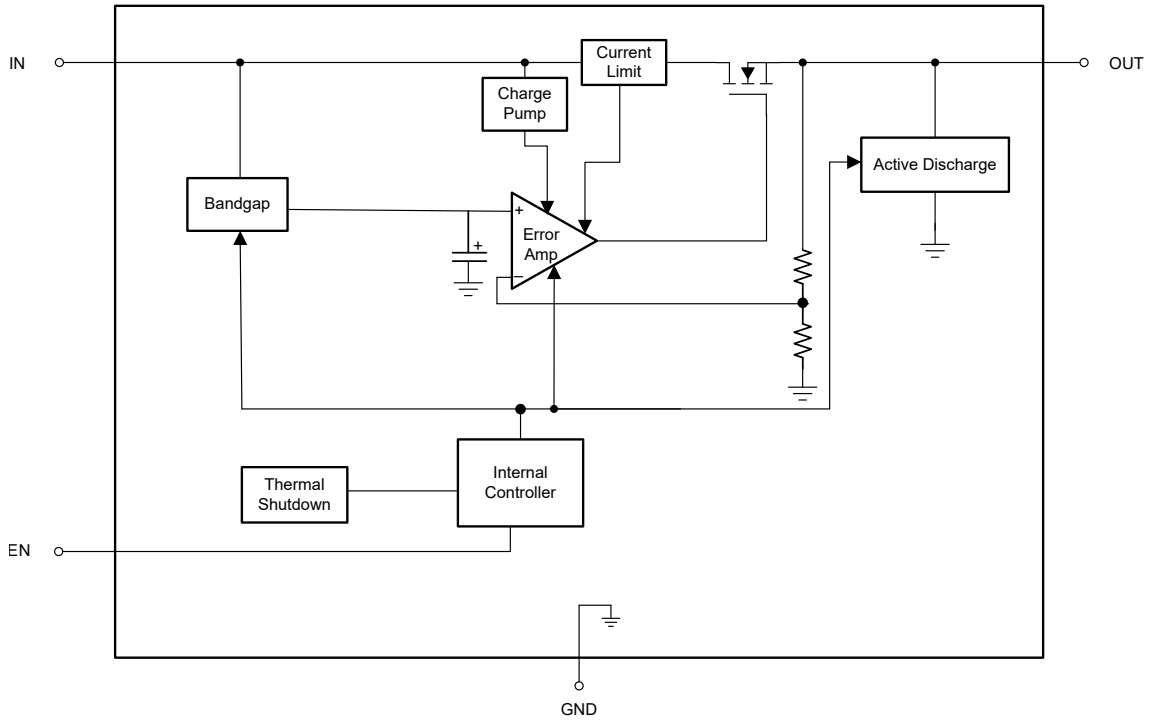
# 6 Detailed Description

## 6.1 Overview

The TLV774-Q1 provides high PSRR and good transient response in a small, 300mA LDO.

This LDO is designed to operate with a single 1µF input capacitor and a single 1µF ceramic output capacitor.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### 6.3.1 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as $V_{IN}$ – $V_{OUT}$ at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, and $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Section 5.3* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

### 6.3.2 Active Discharge

The regulator has an internal MOSFET that connects a pulldown resistor between the output and ground when the device is disabled. This connection actively discharges the output voltage. The active discharge circuit is activated by the enable pin or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.


Copyright © 2026 Texas Instruments Incorporated

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses. Reverse current flow from the output to the input potentially causes damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

### 6.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current termed the *short-circuit current limit ($I_{SC}$)*. $I_{CL}$ and $I_{SC}$ are listed in the *Section 5.5* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

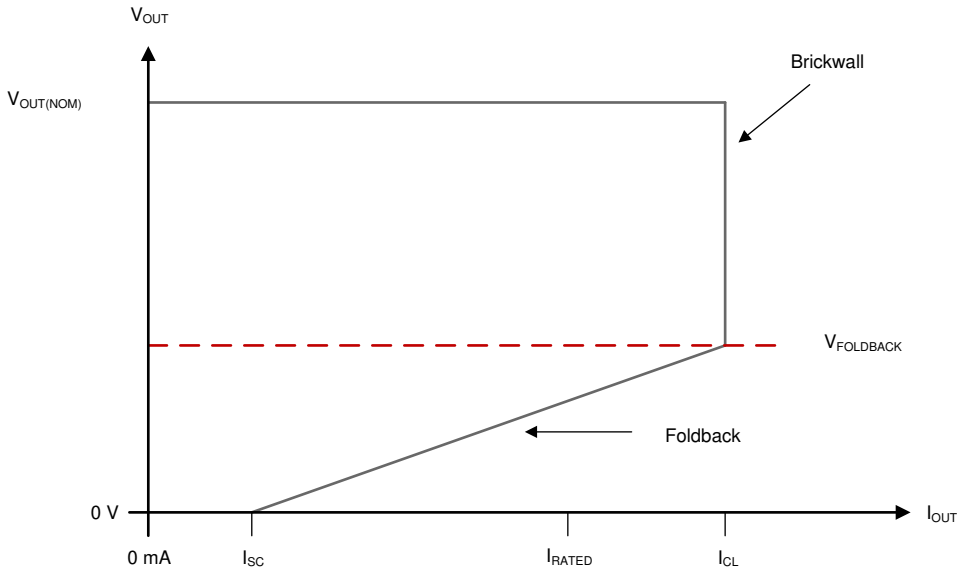



**Figure 6-1. Foldback Current Limit**

### 6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

large $V_{IN}$ – $V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Section 5.3* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

## 6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Section 5.5* table for parameter values.

**Table 6-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and $V_{DO}$ is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

### 6.4.3 Disabled

Shutdown the device output by forcing the enable pin voltage to less than the maximum EN pin low-level input voltage (see the *Section 5.5* table). When disabled, the pass transistor turns off and internal circuits shut down. The output voltage is also actively discharged to ground by an internal discharge circuit from the output to ground.

ADVANCE INFORMATION


Copyright © 2026 Texas Instruments Incorporated

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

### *7.1.1 Recommended Capacitor Types*

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Section 5.3* table account for an effective capacitance of approximately 50% of the nominal value.

### *7.1.2 Input and Output Capacitor Requirements*

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. For typical operation of the TLV774-Q1, connect a 1µF capacitor to the input. Use a higher value capacitor if large, fast rise-time, load, or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *Section 5.3* table for stability. Make sure the minimum derated output capacitance is equal to or greater than 0.47µF. When the output voltage is ramping up, the inrush current depends on the size of the output capacitance. During start-up, the output current is potentially as high as the current limit value for larger output capacitors.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

## 7.2 Typical Application

### 7.2.1 Application

Figure 7-1 shows a typical application circuit for the TLV774-Q1.

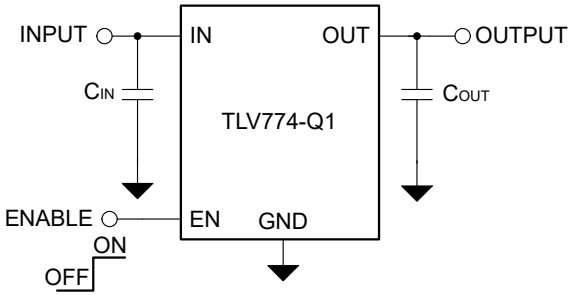



**Figure 7-1. TLV774-Q1 Typical Application**

### 7.2.2 Design Requirements

Table 7-1 shows the design requirements for Figure 7-1.

**Table 7-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage range | 4.0V ± 5% |
| Output voltage | 3.3V |
| Output current | 200mA |
| Maximum ambient temperature | 125°C |

### 7.2.3 Detailed Design Procedure

For this design example, the 3.3V output version (TLV774-Q1 3.3V) is selected. A nominal 4.0V input supply is assumed. Use a minimum 1µF input capacitor to minimize the effect of resistance and inductance between the 4.0V source and LDO input. Use a minimum 0.47µF output capacitance for stability and good load transient response. The dropout voltage ($V_{DO}$) is less than 165mV maximum at a 3.3V output voltage and 300mA output current. There are no dropout issues with a minimum 3.8V input voltage (4.0V − 5%) and a maximum 200mA output current.

### 7.2.4 Application Curves

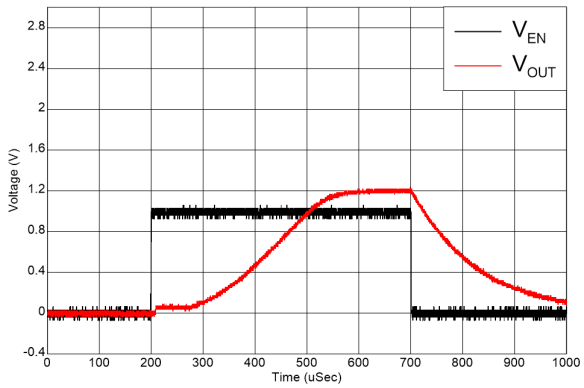



**Figure 7-2. Start-Up**

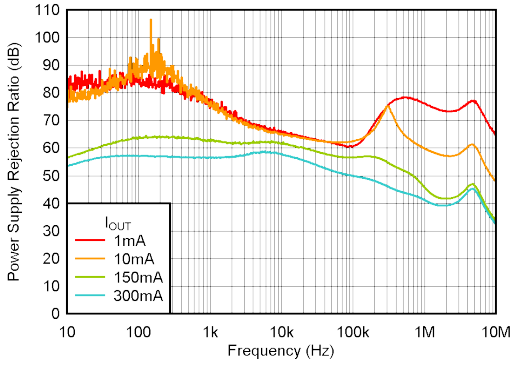



**Figure 7-3. PSRR**


Copyright © 2026 Texas Instruments Incorporated

## 7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.4V to 5.5V. Make sure the input supply is well regulated and free of spurious noise. Also make sure the output voltage is well regulated and dynamic performance is optimum. Thus, set the input supply to at least $V_{OUT(nom)}$ + 0.5V or 1.4V, whichever is greater.

Use a 1µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Take care in placing a thermal via directly beneath the thermal pad of the package. A via potentially wicks solder or solder paste away from the thermal pad joint during the soldering process. Thus, leading to a compromised solder joint on the thermal pad.

### *7.4.2 Layout Example*

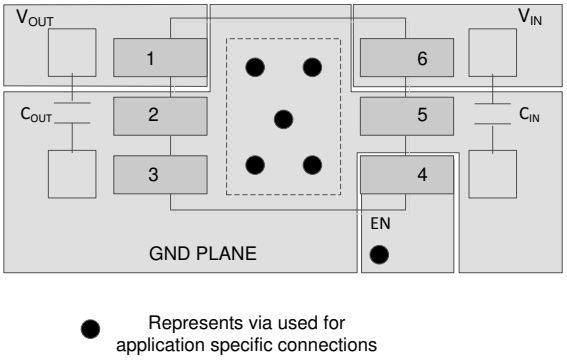



**Figure 7-4. DRV Package (WSON) Typical Layout**

ADVANCE INFORMATION

ADVANCE INFORMATION

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

## 8.1 Device Support

### *8.1.1 Device Nomenclature*

**Table 8-1. Device Nomenclature**

| PRODUCT(1) | DESCRIPTION |
|---|---|
| **TLV774xx(x)(P)QyyyzQ1** | **xx(x)** is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number. Otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V).<br>**(P)** indicates an active output discharge feature.<br>**yyy** is the package designator.<br>**z** is the package quantity. R is for reel (3000 pieces). |

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the device product folder on www.ti.com.

## 8.2 Documentation Support

### *8.2.1 Related Documentation*

For related documentation, see the following:

Texas Instruments, *Know Your Limits* application note

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| September 2026 | * | Initial Release |


Copyright © 2026 Texas Instruments Incorporated

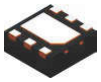
## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, see also the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

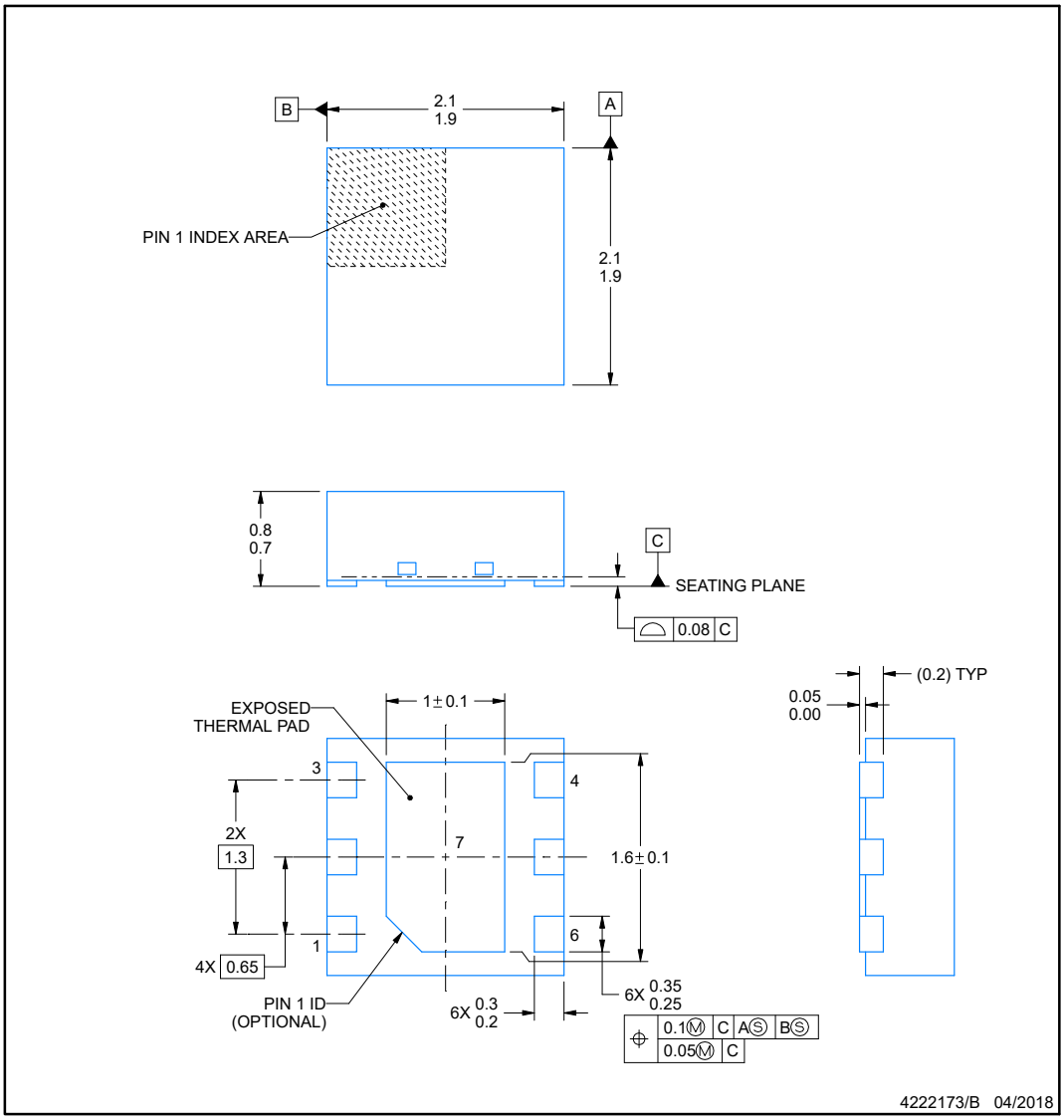
## DRV0006A



## PACKAGE OUTLINE

### WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

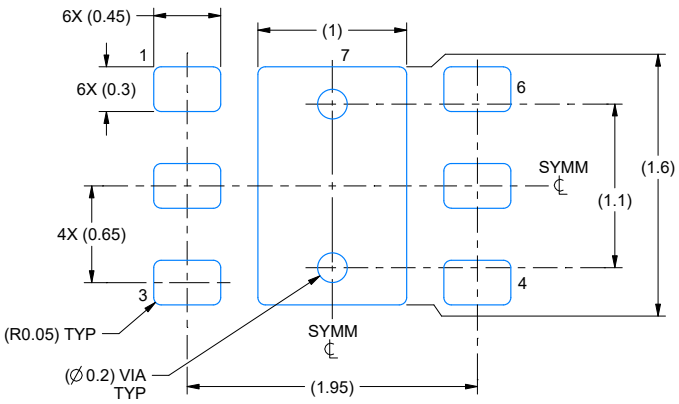
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.


Copyright © 2026 Texas Instruments Incorporated

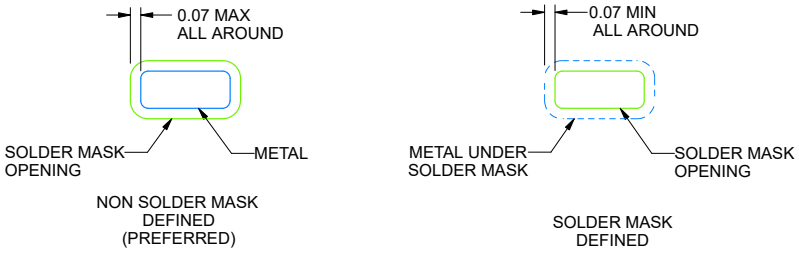
## EXAMPLE BOARD LAYOUT

**DRV0006A** — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SCALE:25X




SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



Copyright © 2026 Texas Instruments Incorporated

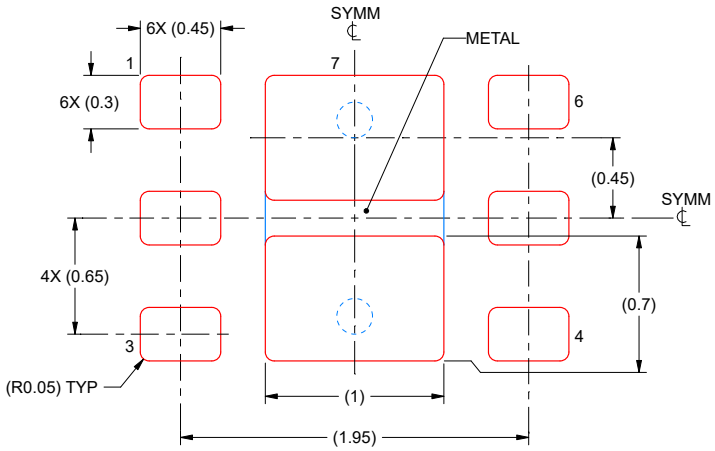

ADVANCE INFORMATION

ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

**DRV0006A** — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



Copyright © 2026 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PTLV77418PQDRVRQ1 | Active | Preproduction | WSON (DRV) \| 6 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| PTLV77433PQDRVRQ1 | Active | Preproduction | WSON (DRV) \| 6 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV774-Q1 :**

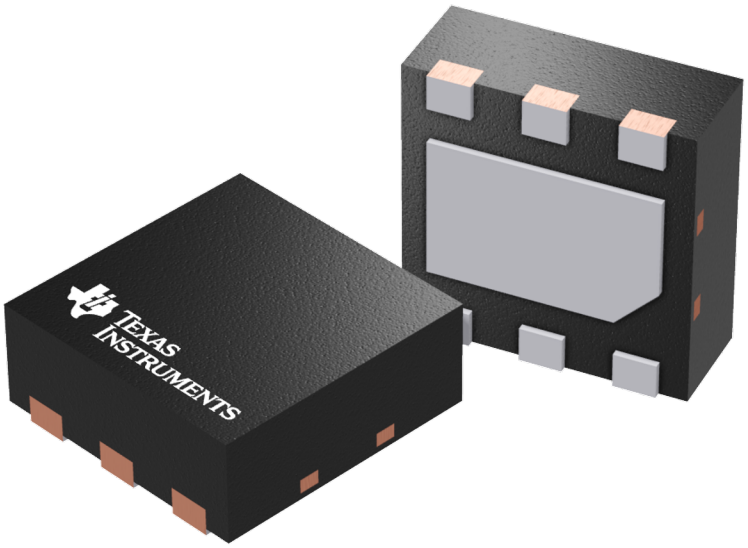
- Catalog : TLV774

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025