TLV62090 3A High Efficiency Synchronous Step-Down Converter with DCS-Control™

1 Features

- 2.5 V to 5.5 V Input Voltage Range
- DCS-Control™
- Up To 98% Efficiency
- Power Save Mode
- 20 µA Operating Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- 1.4 MHz Typical Switching Frequency
- 0.8 V to V_{IN} Adjustable Output Voltage
- Output Discharge Function
- Adjustable Softstart
- Hiccup Short Circuit Protection
- Output Voltage Tracking
- Pin-to-Pin Compatible with TPS62090, TLV62095 and TPS62095
- For Improved Feature Set, See TPS62090
- Create a Custom Design using the TLV62090 with the WEBENCH® Power Designer

2 Applications

- Distributed Power Supplies
- Notebook, Netbook Computers
- Hard Disk Drives (HDD)
- Solid State Drives (SSD)
- Processor Supply
- Battery Powered Applications

3 Description

The TLV62090 device is a high frequency synchronous step-down converter optimized for small solution size, high efficiency and suitable for battery powered applications. To maximize efficiency, the converter operates in pulse width modulation (PWM) mode with a nominal switching frequency of 1.4 MHz and it automatically enters power save mode operation at light load currents. When used in distributed power supplies and point of load regulation, the device allows voltage tracking to other voltage rails and tolerates output capacitors ranging from 10 µF up to 150 µF and beyond. Using the DCS-Control topology, the device achieves excellent load transient performance and accurate output voltage regulation.

The output voltage start-up ramp is controlled by the softstart pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the enable (EN) and power good (PG) pins. In power save mode, the device operates with typically 20-µA quiescent current. Power save mode is entered automatically and seamlessly, maintaining high efficiency over the entire load current range.

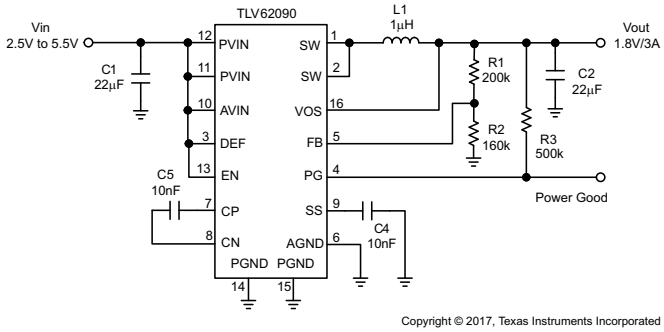
The device is available in a 3 mm x 3 mm 16-pin VQFN (RGT) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV62090	VQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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Efficiency vs Output Current

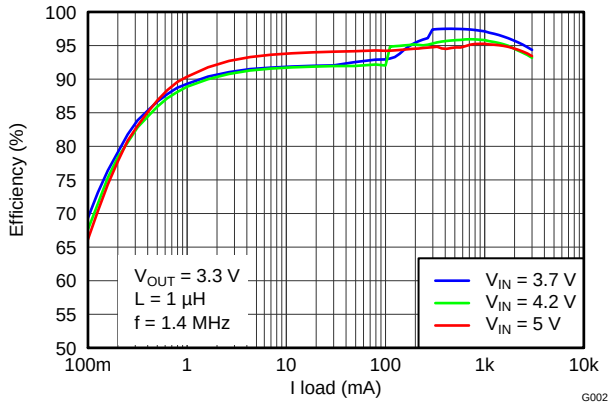


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2016) to Revision F — **Page**

- Added *Feature*: Pin-to-Pin Compatible with TPS62090, TLV62095 and TPS62095 ... 1
- Added *Feature*: For Improved Feature Set, See TPS62090 ... 1
- Added WEBENCH information to the *Features*, *Detailed Design Procedure*, and *Device Support* sections ... 1
- Added SW (AC, less than 10 ns) to the *Absolute Maximum Rating* table ... 5
- Added additional frequency curves to the *Typical Characteristics* section ... 7
- Added Table 1, Power Good Pin Logic ... 12

Changes from Revision D (September 2015) to Revision E — **Page**

- Changed title From: *3A High Efficient Synchronous* To: *3A High Efficiency Synchronous* ... 1
- Changed *Features* From: 95% Converter Efficiency To: Up To 98% Efficiency ... 1
- Changed *Features* From: Two Level Short Circuit Protection To: Hiccup Short Circuit Protection ... 1
- Changed text in the *Description* From: the device operates at typically 20 µA quiescent current. To: the device operates with typically 20-µA quiescent current. ... 1
- Deleted Note from the pinout drawing: *The exposed Thermal Pad is connected to AGND.* ... 4
- Changed the *Pin Functions* table I/O column ... 4
- Changed the *Pin Functions* table Description column for pins FB, EN, and Thermal Pad ... 4
- Added pins CN and CP to the Voltage range in *Absolute Maximum Ratings*(1) ... 5
- Deleted "Continuous total power dissipation" from *Absolute Maximum Ratings*(1) ... 5
- Deleted Note 1 from *Recommended Operating Conditions* ... 5
- Added EN = Low to the Description of R_{PD} in *Electrical Characteristics* table ... 6
- Deleted I_{PG} from the *Electrical Characteristics* table ... 6
- Changed L_{IMF} to I_{LIMF} for High side FET switch current limit in the *Electrical Characteristics table* ... 6
- Changed V_s to V_{OUT} for Output voltage range in the *Electrical Characteristics table* ... 6
- Changed Figure 1 through Figure 2 ... 7
- Added Note 1 to the *Functional Block Diagram* ... 9

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- Changed "Softstart (SS) and Output Capacitor during Startup" To: Softstart (SS) and Hiccup Current Limit During Startup 10
- Changed text From: "start-up especially for larger output capacitors >22 µF." To: "start-up especially for larger output capacitors." in *Softstart (SS) and Hiccup Current Limit During Startup* 10
- Rewrite the description in Voltage Tracking (SS) 10
- Deleted text "in PFM mode and with a minimum quiescent current while" from *Power Save Mode Operation* 13
- Changed $V_{OUT(max)}$ to V_{OUT} in Equation 4 13
- Deleted text "$V_{OUT(max)}$ = nominal output voltage plus maximum output voltage tolerance" from Equation 4 13
- Added Note to *Application and Implementation* 14
- Added 10 nF to the description of C4, C5 in Table 3 15
- Updated the Isat/DCR (max) column of Table 5 16
- Deleted text" The inductor needs to be rated for a saturation current as high as the typical switch current limit, of 4.6 A or according to Equation 5 and Equation 6." from *Inductor Selection* 16
- Changed Equation 5 and Equation 6 16
- Changed the *Input and Output Capacitor Selection* section 16
- Changed Figure 19 18
- Changed Figure 20 18

Changes from Revision C (May 2014) to Revision D **Page**

- Moved Storage temperature From: *ESD Ratings* To: *Absolute Maximum Ratings*(1) 5
- Changed table From: *Handling Ratings* To: *ESD Ratings* 5
- Added PWM mode, T_J = 25°C to Feedback voltage accuracy section of the *Electrical Characteristics* table 6

Changes from Revision B (April 2012) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted text: "TPS62090 adjustable output version" from the Feedback voltage accuracy section of the *Electrical Characteristics* table 6
- Changed Figure 1 From: Resistance (Ω) To: Resistance (mΩ) 7
- Added Application Curves to the Application Information section 18
- Deleted Typical applications from the Application Information section for: 1.8 V Adjustable Version, 1.5 V Adjustable Version, 1.2 V Adjustable Version and 1.05 V Adjustable Version 20

Changes from Revision A (March 2012) to Revision B **Page**

- Changed the Input voltage range MAX value From: 6V To 5.5V in *Electrical Characteristics* 6

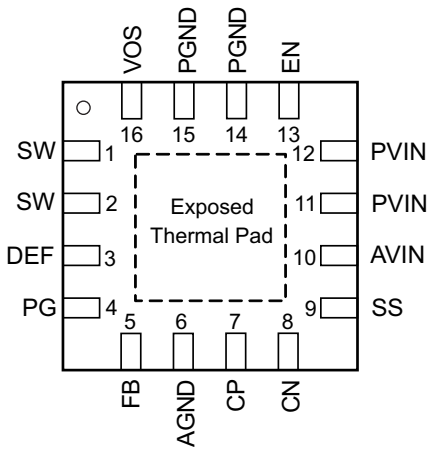
Changes from Original (March 2012) to Revision A **Page**

- Changed Vin From: 2.5V to 6V To: 2.5V to 5.5V in Figure 11 14

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5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1, 2	I/O	Switch pin of the power stage.
DEF	3	I	This pin is used for internal logic and needs to be pulled high. This pin should not be left floating.
PG	4	O	Power good open drain output. This pin is high impedance if the output voltage is within regulation. This pin is pulled low if the output is below its nominal value. The pull up resistor can not be connected to any voltage higher than the input voltage of the device.
FB	5	I	Feedback pin of the device. Connect a resistor divider to set the output voltage.
AGND	6		Analog ground.
CP	7	I/O	Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
CN	8	I/O	Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
SS	9	I	Softstart control pin. A capacitor is connected to this pin and sets the softstart time. Leaving this pin floating sets the minimum start-up time.
AVIN	10	I	Bias supply input voltage pin.
PVIN	11,12	I	Power supply input voltage pin.
EN	13	I	Device enable. To enable the device this pin needs to be pulled high. Pulling this pin low disables the device. This pin has a pull down resistor of typically 400 kΩ, which is active when EN is low.
PGND	14,15		Power ground connection.
VOS	16	I	Output voltage sense pin. This pin needs to be connected to the output voltage.
Exposed Thermal Pad			The exposed thermal pad is connected to AGND. It must be soldered for mechanical reliability.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		VALUE		UNIT
		MIN	MAX	
Voltage range(2)	PVIN, AVIN, FB, SS, EN, DEF, VOS	– 0.3	7	V
	SW (DC), PG	– 0.3	V_{IN} + 0.3	
	SW (AC, less than 10 ns)(3)	– 3.0	10	
	CN, CP	– 0.3	V_{IN} + 7	
Power Good sink current	PG		1	mA
Operating junction temperature range, T_J		– 40	150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

6.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range V_{IN}	2.5		5.5	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV62090	UNITS
		VQFN (16 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60	
$R_{\theta JB}$	Junction-to-board thermal resistance	20	
ψ_{JT}	Junction-to-top characterization parameter	1.5	
ψ_{JB}	Junction-to-board characterization parameter	20	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V_{IN} = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_{QIN}	Quiescent current	Not switching, FB = FB +5%, into PVIN and AVIN		20		µA
I_{sd}	Shutdown current	Into PVIN and AVIN		0.6	5	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis			200		mV
T_{SD}	Thermal shutdown	Temperature rising		150		ºC
	Thermal shutdown hysteresis			20		ºC
CONTROL SIGNAL EN						
V_H	High level input voltage	V_{IN} = 2.5 V to 5.5 V	1	0.65		V
V_L	Low level input voltage	V_{IN} = 2.5 V to 5.5 V		0.60	0.4	V
I_{lkg}	Input leakage current	EN = GND or V_{IN}		10	100	nA
R_{PD}	Pull down resistance	EN = Low		400		kΩ
SOFTSTART						
I_{SS}	Softstart current		6.3	7.5	8.7	µA
POWER GOOD						
V_{TH_PG}	Power good threshold	Output voltage rising	93%	95%	97%	
		Output voltage falling	88%	90%	92%	
V_L	Low level voltage	$I_{(sink)}$ = 1 mA			0.4	V
I_{lkg}	Leakage current	V_{PG} = 3.6 V		10	100	nA
POWER SWITCH						
$R_{DS(on)}$	High side FET on-resistance	I_{SW} = 500 mA		50		mΩ
	Low side FET on-resistance	I_{SW} = 500 mA		40		mΩ
I_{LIMF}	High side FET switch current limit		3.7	4.6	5.5	A
f_s	Switching frequency	I_{OUT} = 3 A		1.4		MHz
OUTPUT						
V_{OUT}	Output voltage range		0.8		V_{IN}	V
R_{od}	Output discharge resistor	EN = GND, V_{OUT} = 1.8 V		200		Ω
V_{FB}	Feedback regulation voltage	PWM Mode		0.8		V
V_{FB}	Feedback voltage accuracy $V_{IN} \geq V_{OUT}$ + 1 V	I_{OUT} = 1 A, PWM mode, T_J = 25°C	-1%		+1%	
		I_{OUT} = 1 A, PWM mode	-1.4%		+1.4%	
		I_{OUT} = 0 mA, $V_{OUT} \geq$ 1.2 V, PFM mode (1)	-1.4%		+3%	
		I_{OUT} = 0 mA, V_{OUT} < 1.2 V, PFM mode (2)	-1.4%		+3.7%	
I_{FB}	Feedback input bias current	V_{FB} = 0.8 V		10	100	nA
	Line regulation	V_{OUT} = 1.8 V, PWM operation		0.016		%/V
	Load regulation	V_{OUT} = 1.8 V, PWM operation		0.04		%/A

(1) Conditions: L = 1 µH, C_{OUT} = 22 µF. For more information, see the *Power Save Mode Operation* section of this data sheet.
(2) For output voltages < 1.2 V, use a 2 x 22 µF output capacitance to achieve +3% output voltage accuracy in PFM mode.

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6.6 Typical Characteristics

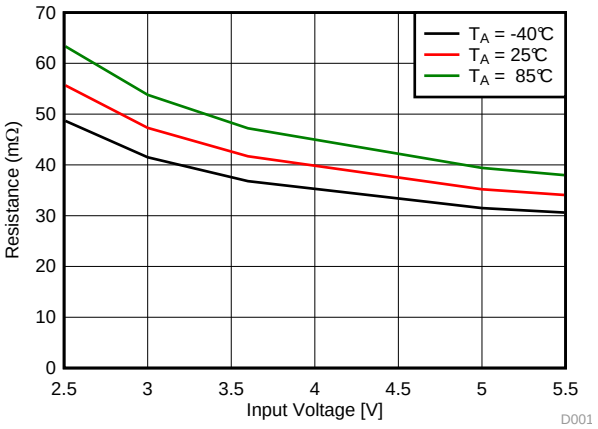
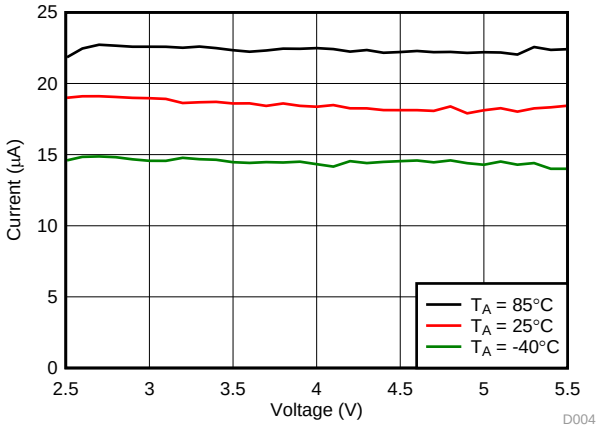
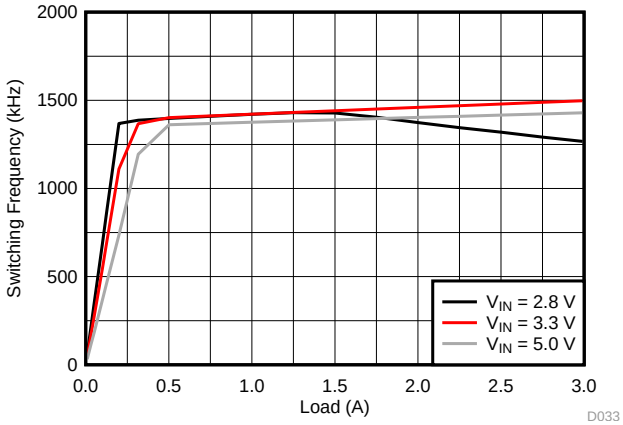


Figure 1. High Side FET On-Resistance vs Input Voltage



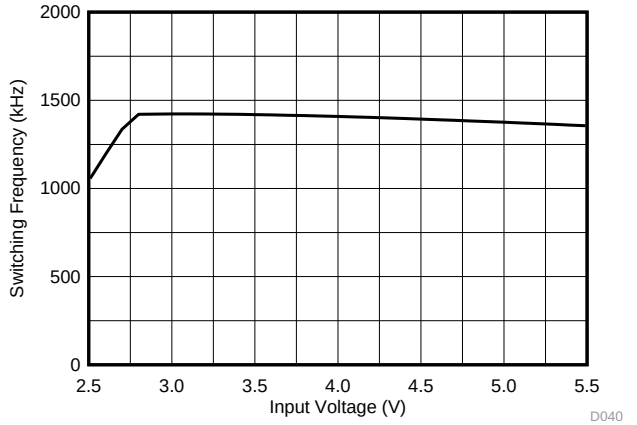
V_{OUT} = 1.8 V L = 1 µH

Figure 2. Quiescent Current vs Input Voltage



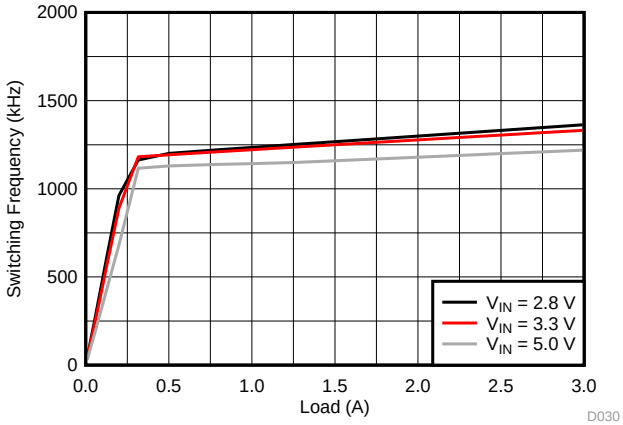
V_{OUT} = 1.8 V L = 1 µH

Figure 3. Switching Frequency vs Load Current



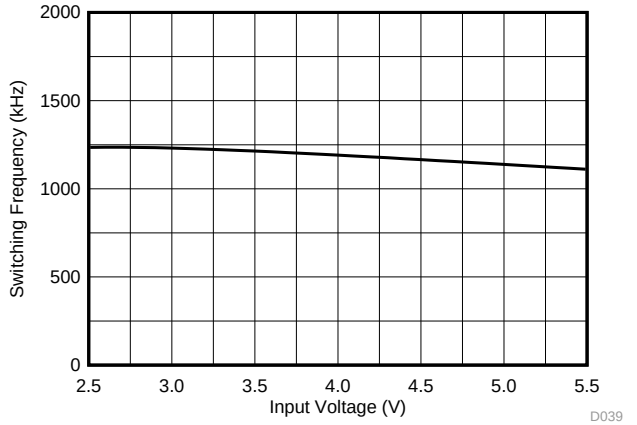
V_{OUT} = 1.8 V L = 1 µH I_{OUT} = 1 A

Figure 4. Switching Frequency vs Input Voltage



V_{OUT} = 1.0 V L = 1 µH

Figure 5. Switching Frequency vs Load Current

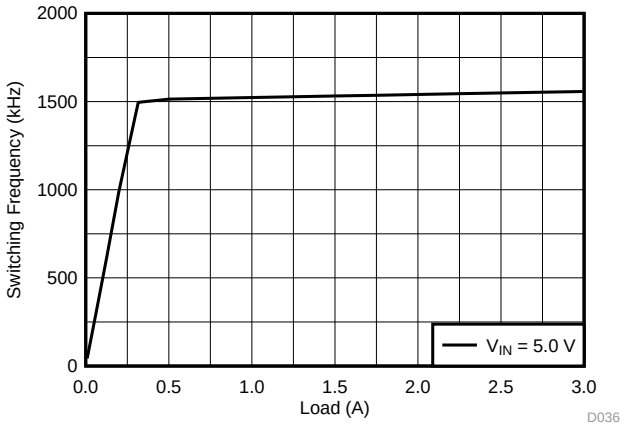


V_{OUT} = 1.0 V L = 1 µH I_{OUT} = 1 A

Figure 6. Switching Frequency vs Input Voltage

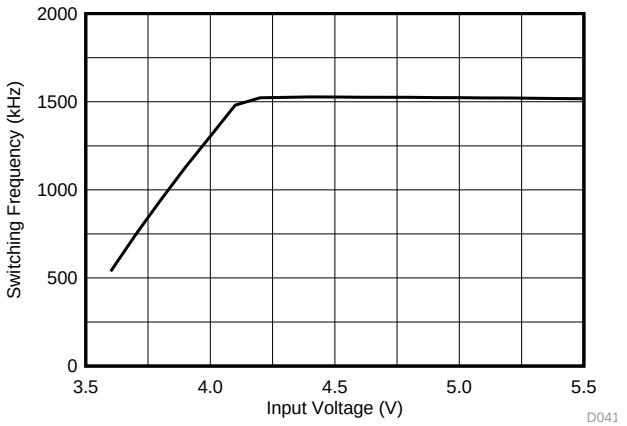
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Typical Characteristics (continued)



V_{OUT} = 3.3 V L = 1 µH

Figure 7. Switching Frequency vs Load Current



V_{OUT} = 3.3 V L = 1 µH I_{OUT} = 1 A

Figure 8. Switching Frequency vs Input Voltage

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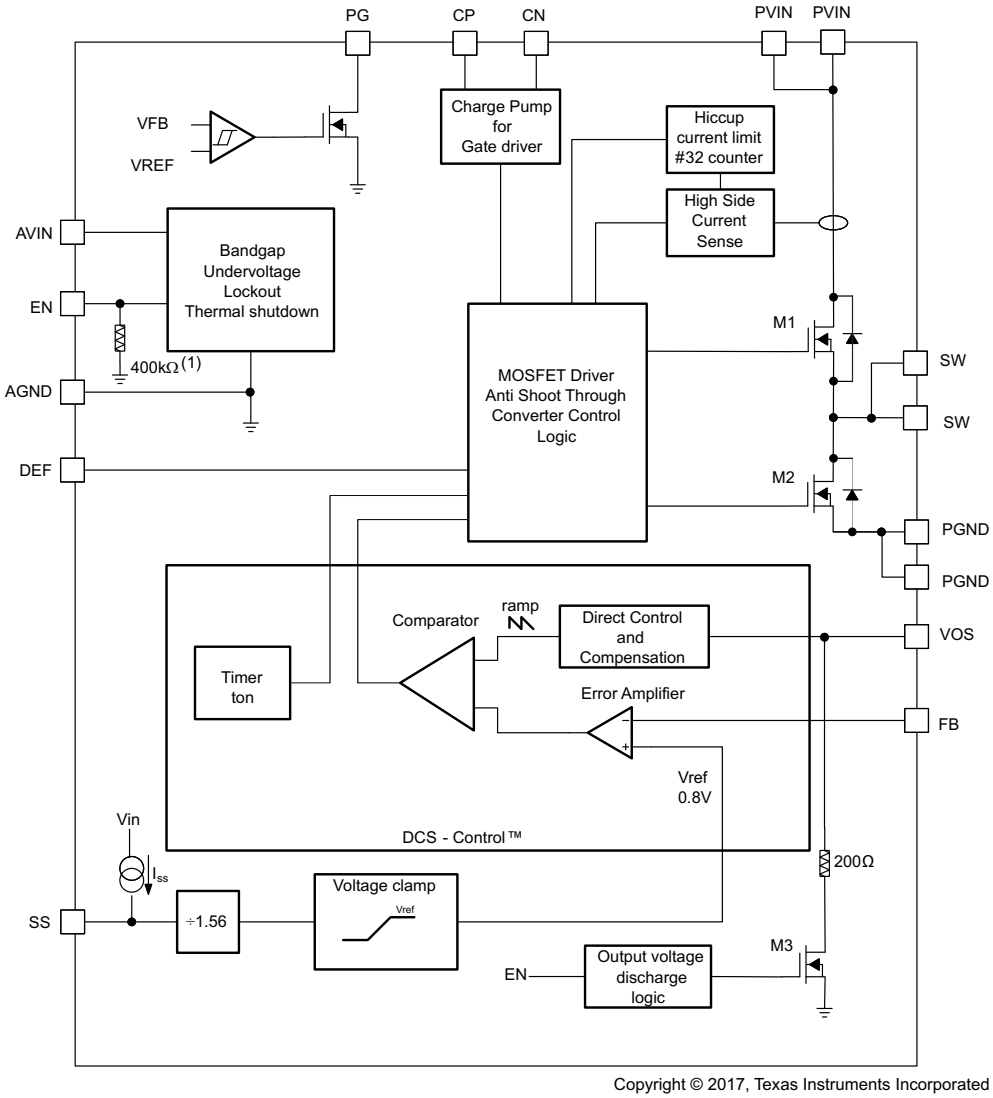
7 Detailed Description

7.1 Overview

The TLV62090 synchronous switched mode converter is based on DCS-Control™ (direct control with seamless transition into power save mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage-mode control.

The DCS-Control™ topology operates in pulse width modulation (PWM) mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 1.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the current consumption to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to power save mode without effects on the output voltage. The TLV62090 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



(1) The resistor is disconnected when EN is high.

7.3 Feature Description

7.3.1 Enable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 0.6 µA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 200 Ω discharges the output through the VOS pin smoothly. An internal pull-down resistor of 400 kΩ is connected to the EN pin when the EN pin is low. The pull-down resistor is disconnected when the EN pin is high.

7.3.2 Softstart (SS) and Hiccup Current Limit During Startup

To minimize inrush current during start up, the device has an adjustable softstart depending on the capacitor value connected to the SS pin. The device charges the softstart capacitor with a constant current of typically 7.5 µA. The feedback voltage follows this voltage with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. Softstart operation is completed once the voltage at the softstart capacitor has reached typically 1.25 V. The softstart time is calculated using Equation 1. The larger the softstart capacitor, the longer the softstart time. The relation between softstart voltage and feedback voltage is estimated using Equation 2.

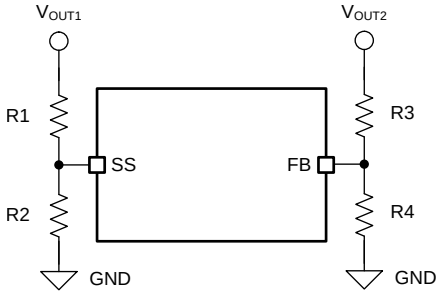
$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \quad (1)$$

$$V_{FB} = \frac{V_{SS}}{1.56} \quad (2)$$

During startup, the switch current limit is reduced to 1/3 (~1.5 A) of its typical current limit of 4.6 A. Once the output voltage exceeds typically 0.6 V, the current limit is released to its nominal value. The device provides a reduced load current of ~1.5 A when the output voltage is below typically 0.6 V. Due to this, a small or no softstart time may trigger the short circuit protection during startup especially for larger output capacitors. This is avoided by using a larger softstart capacitance to extend the softstart time. See *Short Circuit Protection (Hiccup-Mode)* for details of the reduced current limit during startup. Leaving the softstart pin floating sets the minimum startup time (around 50 µs).

7.3.3 Voltage Tracking (SS)

The SS pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in Figure 9. The internal reference voltage follows the voltage at the SS pin with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in Figure 10.



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Figure 9. Output Voltage Tracking

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Feature Description (continued)

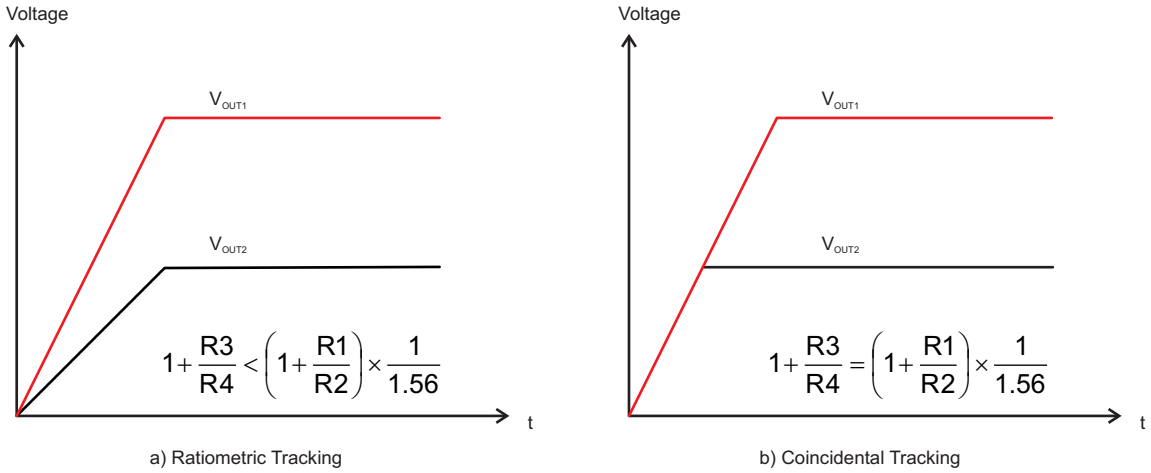


Figure 10. Voltage Tracking Options

The R2 value should be set properly to achieve accurate voltage tracking by taking 7.5 µA soft startup current into account. 1 kΩ or smaller is a sufficient value for R2.

For decreasing the SS pin voltage, the device doesn't sink current from the output when the device is in power save mode. So the resulting decreases of the output voltage may be slower than the SS pin voltage if the load is light. When driving the SS pin with an external voltage, do not exceed the voltage rating of the SS pin which is 7 V.

7.3.4 Short Circuit Protection (Hiccup-Mode)

The device is protected against hard short circuits to GND and over-current events. This is implemented by a two level short circuit protection. During startup and when the output is shorted to GND, the switch current limit is reduced to 1/3 of its typical current limit of 4.6 A. Once the output voltage exceeds typically 0.6 V, the current limit is released to its nominal value. The full current limit is implemented as a hiccup current limit. Once the internal current limit is triggered 32 times, the device stops switching and starts a new startup sequence after a typical delay time of 66 µS. The device goes through these cycles until the high current condition is released.

7.3.5 Output Discharge Function

To make sure the device starts up under defined conditions, the output gets discharged via the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This happens when the device is disabled or if thermal shutdown, undervoltage lockout or short circuit hiccup-mode are triggered.

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Feature Description (continued)

7.3.6 Power Good Output (PG)

The power good output is low when the output voltage is below its nominal value. The power good becomes high impedance once the output is within 5% of regulation. The PG pin is an open drain output and is specified to typically sink up to 1 mA. This output requires a pull-up resistor to be monitored properly. The pull-up resistor cannot be connected to any voltage higher than the input voltage of the device. The PG output is low when the device is disabled, in thermal shutdown or UVLO. The PG output can be left floating if unused. Table 1 shows the PG pin logic.

Table 1. Power Good Pin Logic

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\ V < VIN \leq V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} \leq 0.7\ V$	√	

7.3.7 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2 V with a 200 mV hysteresis.

7.3.8 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 150°C with a 20°C hysteresis.

7.3.9 Charge Pump (CP, CN)

The CP and CN pins must attach to an external 10 nF capacitor to complete a charge pump for the gate driver. This capacitor must be rated for the input voltage. It is not recommended to connect any other circuits to the CP or CN pins.

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7.4 Device Functional Modes

7.4.1 PWM Operation

At medium to heavy load currents, the device operates with pulse width modulation (PWM) at a nominal switching frequency of 1.4 MHz. As the load current decreases, the converter enters power save mode operation reducing its switching frequency. The device enters power save mode at the boundary to discontinuous conduction mode (DCM).

7.4.2 Power Save Mode Operation

As the load current decreases, the converter enters power save mode operation. During power save mode, the converter operates with reduced switching frequency maintaining high efficiency. Power save mode is based on a fixed on-time architecture following Equation 3.

$$ton = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{ton^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}} \right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (3)$$

In power save mode, the output voltage rises slightly above the nominal output voltage in PWM mode, as shown in Figure 15. This effect is reduced by increasing the output capacitance or the inductor value. This effect is also reduced by programming the output voltage of the TLV62090 lower than the target value. As an example, if the target output voltage is 3.3 V, then the TLV62090 can be programmed to 3.3 V - 0.8%. As a result the output voltage accuracy is now -2.2% to +2.2% instead of -1.4% to 3%. The output voltage accuracy in pulse frequency modulation (PFM) operation is reflected in the electrical specification table and given for a 22-µF output capacitor.

7.4.3 Low Dropout Operation (100% Duty Cycle)

The device offers a low input to output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below its nominal regulation value is given by:

$$V_{IN(min)} = V_{OUT} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (4)$$

Where

$R_{DS(on)}$ = High side FET on-resistance

R_L = DC resistance of the inductor

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV62090 is a 3-A high frequency synchronous step-down converter optimized for small solution size, high efficiency and suitable for battery powered applications.

8.2 Typical Application

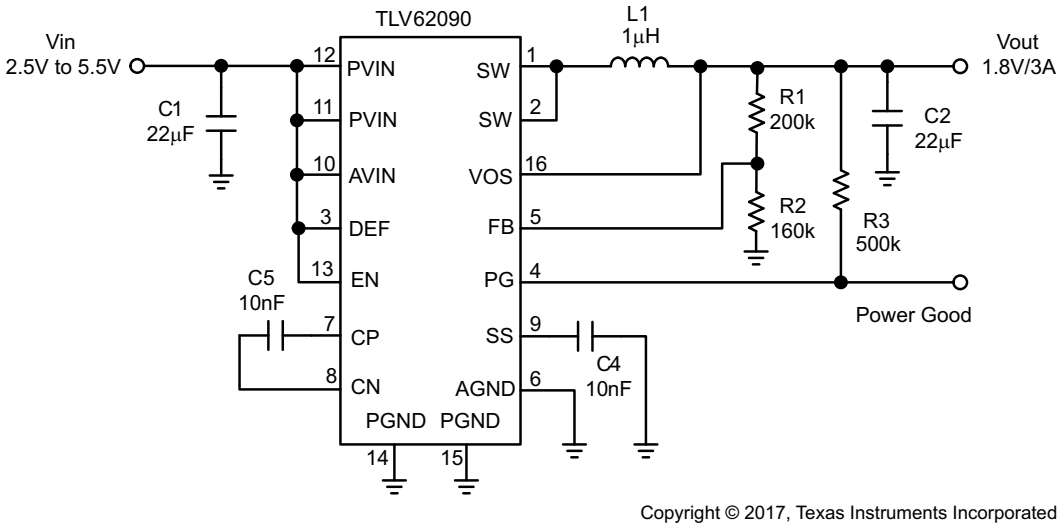


Figure 11. TLV62090 Typical Application Circuit

8.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions.

For the typical application example, the following input parameters are used. See Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5 V to 5.5 V
Output Voltage	1.8 V
Transient Response	±5% VOUT
Input Voltage Ripple	400 mV
Output Voltage Ripple	30 mV
Output current rating	3 A
Operating frequency	1.4 MHz

Table 3 shows the list of components for the Application Characteristic Curves.

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Table 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
TLV62090	High efficiency step-down converter	Texas Instruments
L1	Inductor: 1 µH	Coilcraft XFL4020-102
C1	Ceramic capacitor: 22 µF	(6.3V, X5R, 0805)
C2	Ceramic capacitor: 22 µF	(6.3V, X5R, 0805)
C4, C5	Ceramic capacitor, 10 nF	Standard
R1, R2, R3	Resistor	Standard

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TLV62090 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance
   – Run thermal simulations to understand the thermal performance of your board
   – Export your customized schematic and layout into popular CAD formats
   – Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

The first step is the selection of the output filter components. To simplify this process, Table 4 outlines possible inductor and capacitor value combinations.

Table 4. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	100	150
0.47		√	√	√	√
1.0	√	√(3)	√	√	√
2.2	√	√	√	√	√
3.3					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) Typical application configuration. Other check mark indicates alternative filter combinations

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8.2.2.2 Inductor Selection

The inductor selection is affected by several parameters like inductor ripple current, output voltage ripple, transition point into power save mode, and efficiency. See Table 5 for typical inductors.

Table 5. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR (max)
0.6 µH	Coilcraft XAL4012-601	4 x 4 x 2.1	7.9A/10.5 mΩ
1 µH	Coilcraft XAL4020-102	4 x 4 x 2.1	6.7A/14.6 mΩ
1 µH	Coilcraft XFL4020-102	4 x 4 x 2.1	4.5 A/11.9 mΩ
0.47 µH	TOKO DFE252012CR47	2.5 x 2 x 1.2	3.7A/39 mΩ
1 µH	TOKO DFE252012C1R0	2.5 x 2 x 1.2	3.0A/59 mΩ
0.68 µH	TOKO DFE322512CR68	3.2 x 2.5 x 1.2	3.5A/35 mΩ
1 µH	TOKO DFE322512C1R0	3.2 x 2.5 x 1.2	3.1A/45 mΩ

In addition, the inductor has to be rated for the appropriate saturation current and DC resistance (DCR). Equation 5 and Equation 6 calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency can be taken from the data sheet graphs or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$\Delta I_L = \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{f \times L} \quad (5)$$

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (6)$$

where

- f = Converter switching frequency (typically 1.4 MHz)
- L = Selected inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as a conservative assumption)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of about 20% should be added to cover for load transients during operation.

8.2.2.3 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR (X5R or X7R) ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 22-µF or larger input capacitor is recommended. The output capacitor value can range from 10 µF up to 150 µF and beyond. Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values.

The recommended typical output capacitor value is 22 µF (nominal) and can vary over a wide range as outline in the output filter selection table. For output voltages above 1.8 V, noise can cause duty cycle jitter. This does not degrade device performance. Using an output capacitor of 2 x 22 µF (nominal) for output voltages >1.8 V avoids duty cycle jitter.

Ceramic capacitor have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating.

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8.2.2.4 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (7)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8\ V}{5\ \mu A} \approx 160\ k\Omega \quad (8)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (9)$$

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5 µA for the feedback current I_{FB}. Larger currents through R2 improve noise sensitivity and output voltage accuracy. A feed forward capacitor is not required for proper operation.

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8.2.3 Application Curves

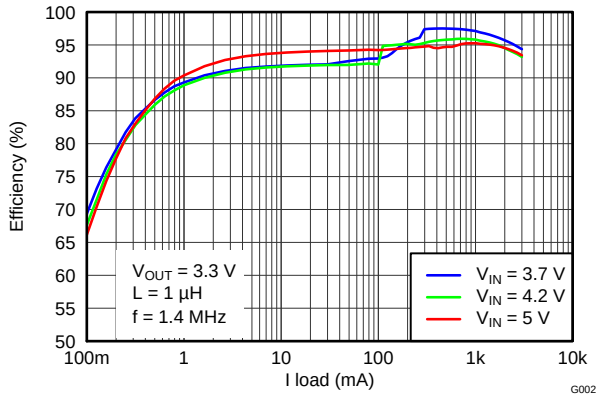


Figure 12. Efficiency vs Load Current

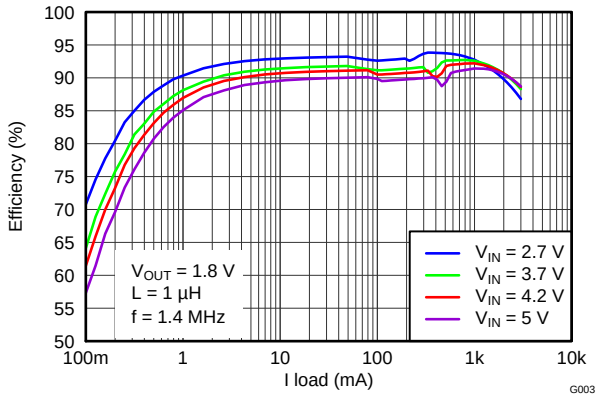


Figure 13. Efficiency vs Load Current

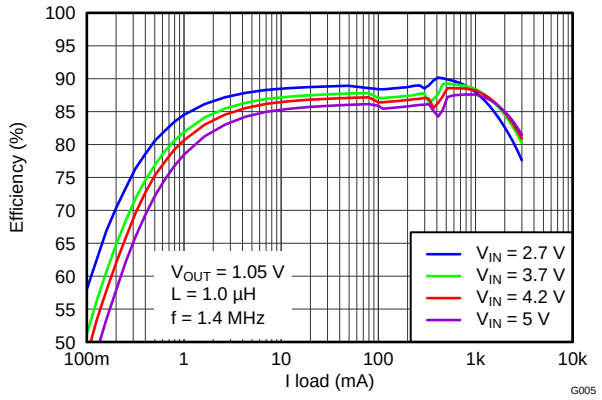


Figure 14. Efficiency vs Load Current

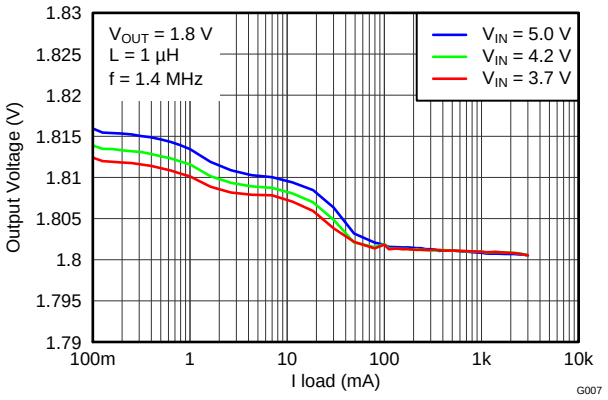


Figure 15. Output Voltage vs Load Current

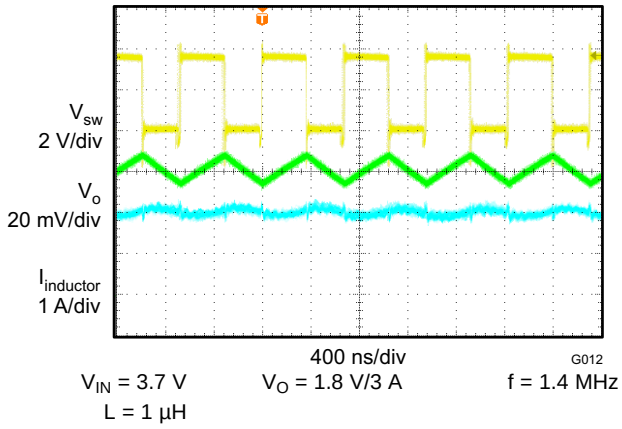


Figure 16. PWM Operation

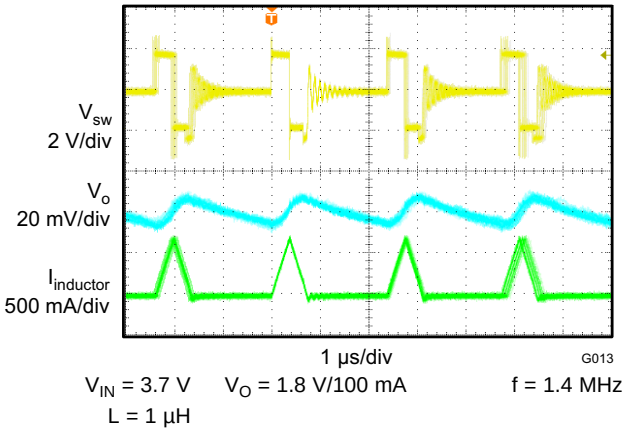


Figure 17. PFM Operation

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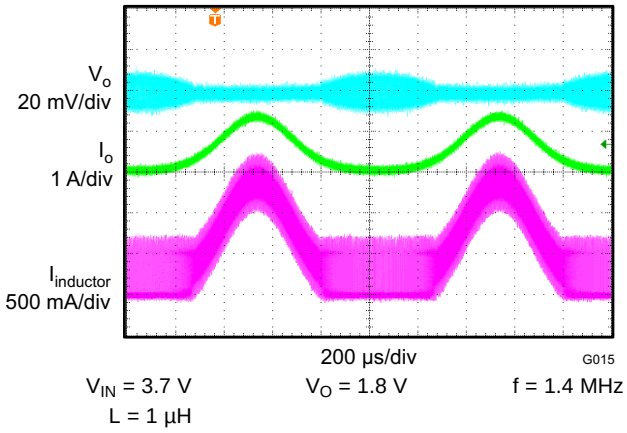


Figure 18. Load Sweep, 0 to 1.5 A

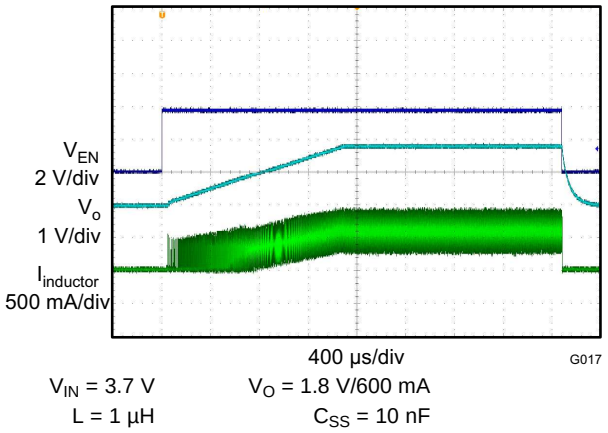


Figure 19. Start-Up

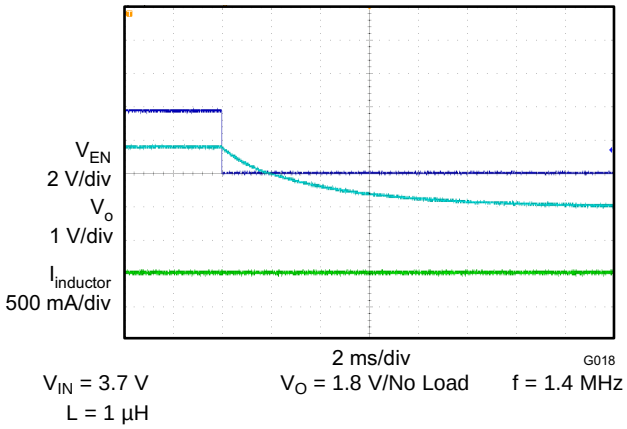


Figure 20. Shutdown

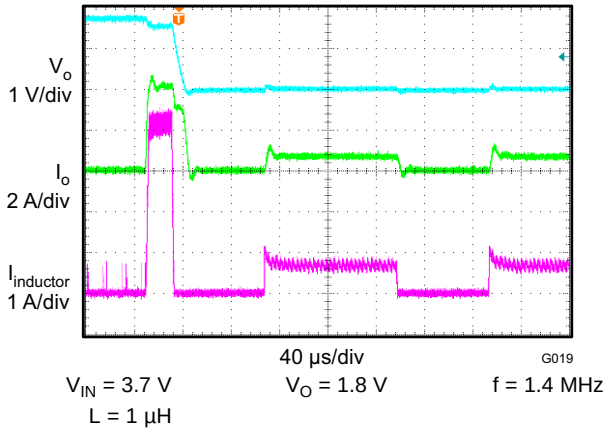


Figure 21. Hiccup Short Circuit Protection

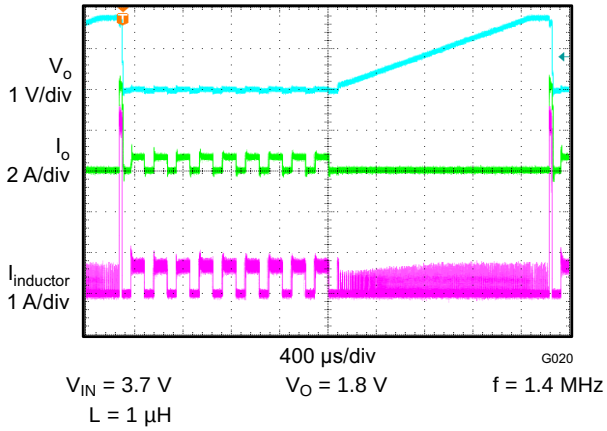


Figure 22. Hiccup Short Circuit Protection

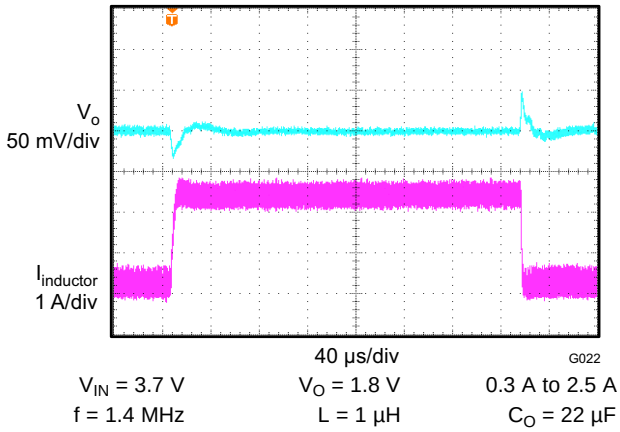


Figure 23. Load Transient Response

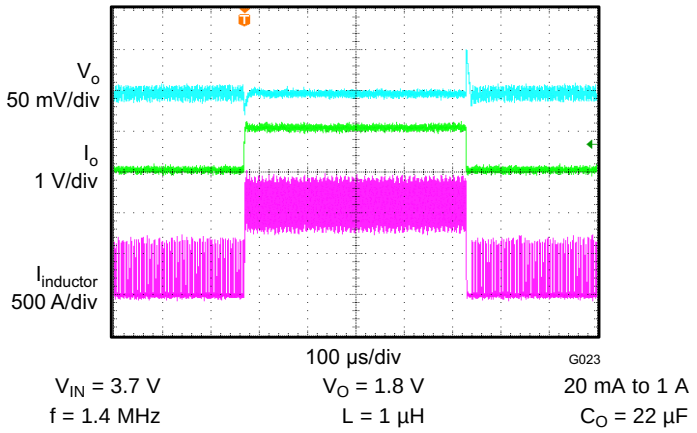


Figure 24. Load Transient Response

9 Power Supply Recommendations

The TLV62090 device has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TLV62090.

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10 Layout

10.1 Layout Guideline

- It is recommended to place the input capacitor as close as possible to the IC pins PVIN and PGND.
- The VOS connection is noise sensitive and needs to be routed short and direct to the output terminal of the inductor.
- The exposed thermal pad of the package, analog ground (pin 6) and power ground (pin 14, 15) should have a single point connection at the exposed thermal pad of the package. This minimizes switch node jitter.
- The charge pump capacitor connected to CP and CN should be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits.
- See Figure 25 and the evaluation module User Guide (SLVU670) for an example of component placement, routing and thermal design.

10.2 Layout Example

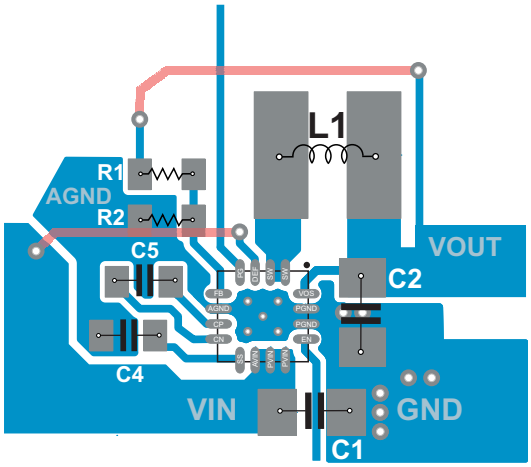


Figure 25. Recommended Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TLV62090 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Third-Party Products Disclaimer

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The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
is a trademark of ~ Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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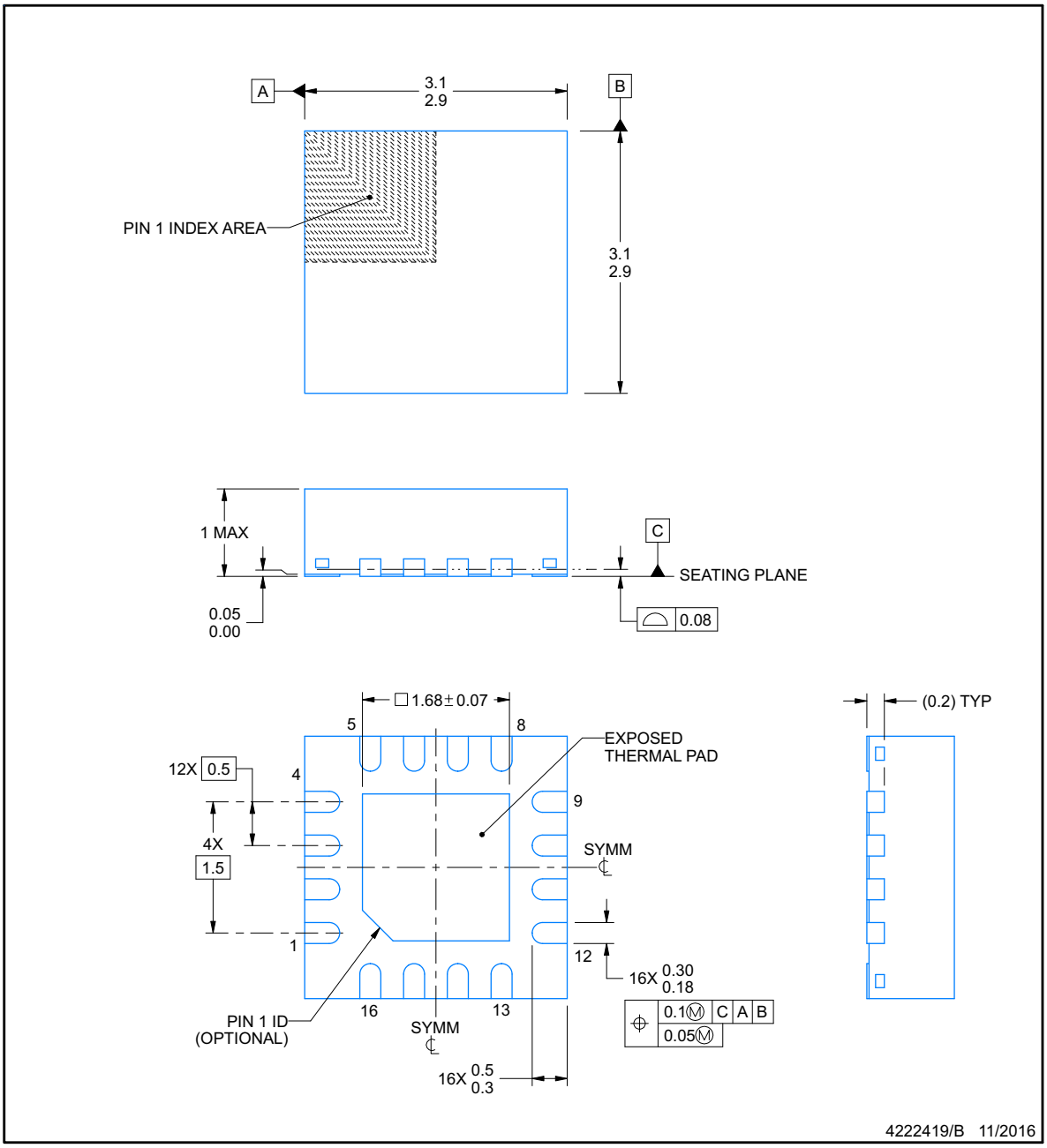
RGT0016C



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

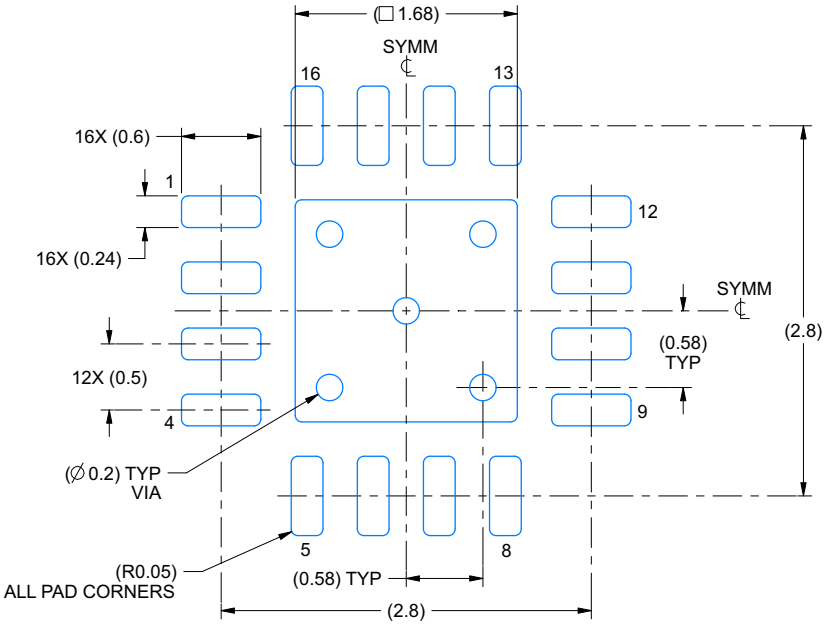
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EXAMPLE BOARD LAYOUT

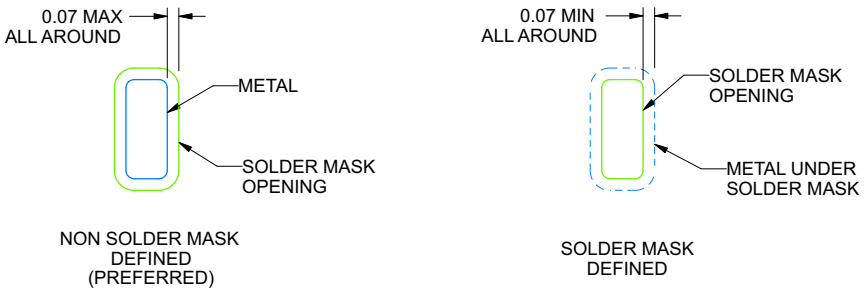
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222419/B 11/2016

NOTES: (continued)

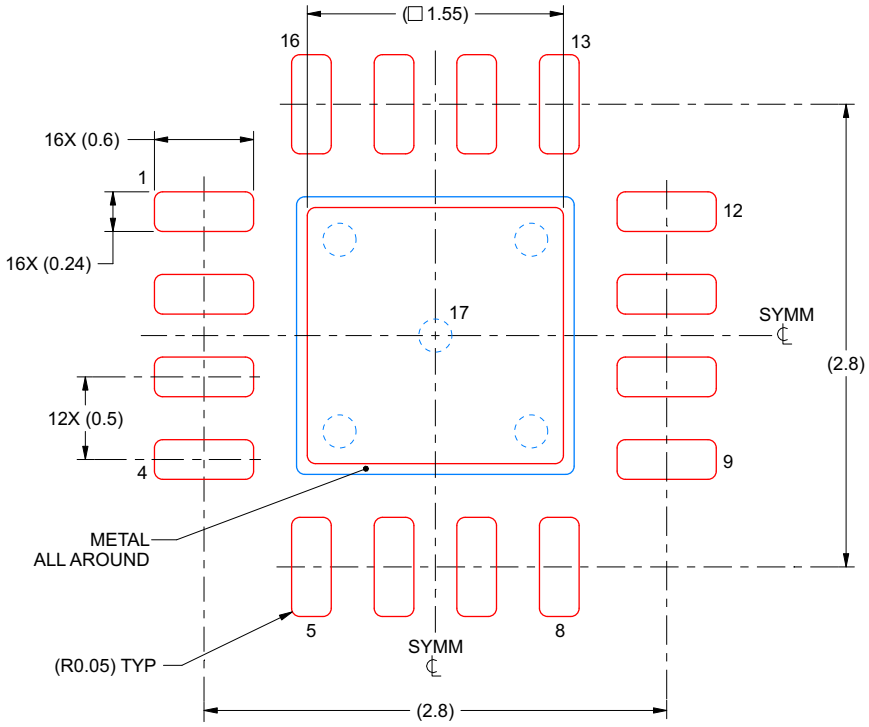
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RGT0016C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/B 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV62090RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTRG4	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTRG4.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTRG4.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV
TLV62090RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

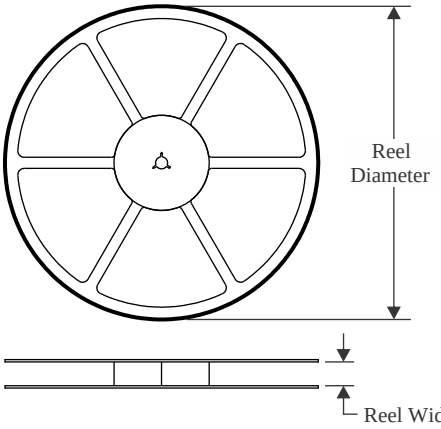
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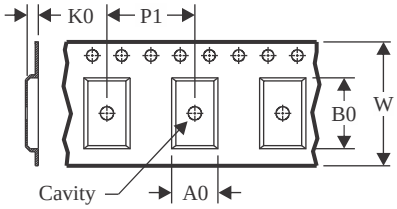
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

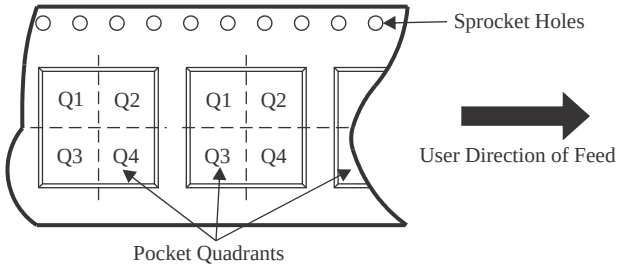


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

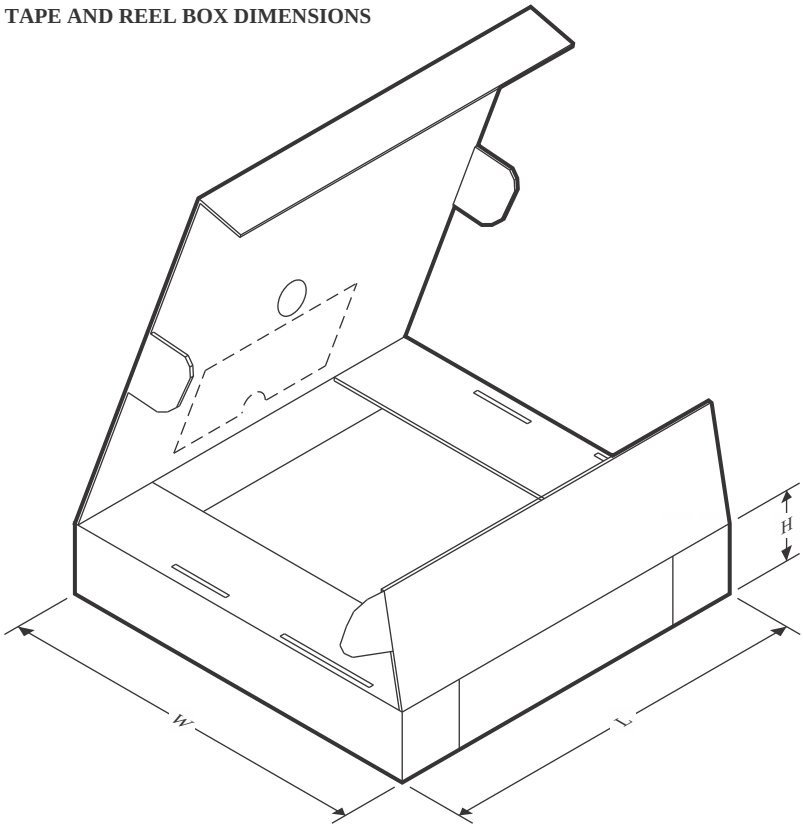
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62090RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62090RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62090RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62090RGTRG4	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62090RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62090RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62090RGTR	VQFN	RGT	16	3000	338.0	355.0	35.0
TLV62090RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TLV62090RGTR	VQFN	RGT	16	3000	360.0	360.0	36.0
TLV62090RGTRG4	VQFN	RGT	16	3000	346.0	346.0	33.0
TLV62090RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TLV62090RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

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