TLV370x Family of Nanopower, Push-Pull Output Comparators

1 Features

- Low supply current: 56nA/per channel
- Input common-mode range exceeds the rails: –0.1V to V_{CC} + 5V
- Supply voltage range: 2.5V to 16V
- Reverse battery protection up to 20V
- Push-pull CMOS output stage
- Specified Temperature Range
  - 0°C to 70°C – Commercial grade
  - –40°C to 125°C – Industrial grade
- Ultra-small packaging
  - 5-Pin SOT-23 (TLV3701)
  - 8-Pin MSOP (TLV3702)
- Universal op-amp EVM (Reference SLOU060 for more information)

2 Applications

- Portable battery monitoring
- Consumer medical electronics
- Security detection systems
- Handheld instruments
- Ultra-low power systems

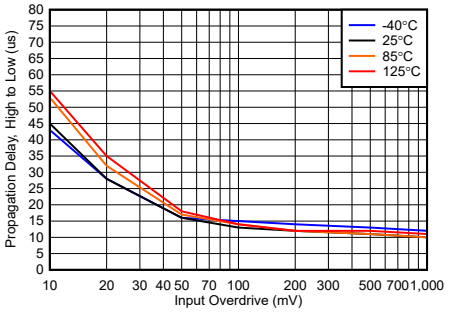


Figure 3-1. Prop Delay, High to Low, 12V

3 Description

The TLV370x is Texas Instruments' first family of nanopower comparators with only 560nA per channel supply current, which make this device ideal for battery power and wireless handset applications.

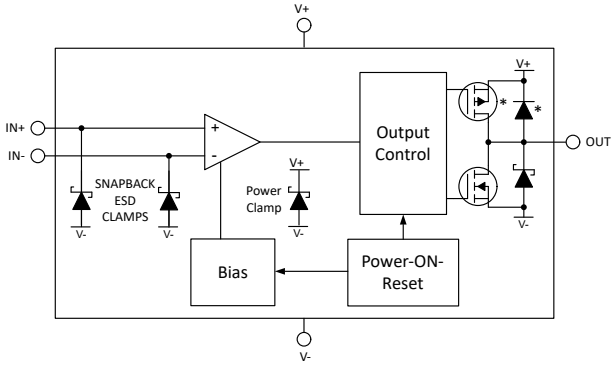
The TLV370x has a minimum operating supply voltage of 2.7V over the extended industrial temperature range (T_A = –40°C to 125°C), while having an input common-mode range of –0.1 to V_{CC} + 5V. The low supply current makes it an ideal choice for battery-powered portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an overcurrent condition due to improper battery installation. For harsh environments, the inputs can be taken 5V above the positive supply rail without damage to the device.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV3701	SOT-23 (5)	2.9mm × 2.8mm
	SOIC (8)	4.9mm × 6mm
TLV3702	SOIC (8)	4.9mm × 6mm
	VSSOP (8)	3mm × 4.9mm
	PDIP (8)	10.2mm × 9.4mm
TLV3704	SOIC (14)	8.65mm × 6mm
	PDIP (14)	19.3mm × 9.4mm
	TSSOP (14)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison Tables

Table 4-1. Selection of Comparators (1)

DEVICE	V_{CC} (V)	V_{IO} (µV)	I_{CC}/Ch (µA)	I_{IB} (pA)	t_{PLH} (µs)	t_{PHL} (µs)	t_f (µs)	t_r (µs)	RAIL-TO-RAIL	OUTPUT STAGE
TLV370x	2.5 – 16	250	0.56	80	56	83	22	8	I	PP
TLV340x	2.5 – 16	250	0.47	80	55	30	5	—	I	OD
TLC3702/4	3 – 16	1200	9	5	1.1	0.65	0.5	0.125	—	PP
TLC393/339	3 – 16	1400	11	5	1.1	0.55	0.22	—	—	OD
TLC372/4	3 – 16	1000	75	5	0.65	0.65	—	—	—	OD

(1) All specifications are typical values measured at 5V.

Table 4-2. TLV3701 Available Options

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D)(1)	SOT-23 (DBV)(2)	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	5000 µV	TLV3701CD	TLV3701CDBV	VBCC	—
–40°C to 125°C		TLV3701ID	TLV3701IDBV	VBCI	TLV3701IP

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV3701CDR).
(2) This package is only available taped and reeled. For standard quantities (3000 pieces per reel), add an R suffix (that is, TLV3701 CDBVR). For small quantities (250 pieces per mini-reel), add a T suffix to the part number (for example, TLV3701CDBVT).

Table 4-3. TLV3702 Available Options

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D)(1)	MSOP (DGK)	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	5000 µV	TLV3702CD	TLV3702CDGK	xxTIAKC	—
–40°C to 125°C		TLV3702ID	TLV3702IDGK	xxTIAKD	TLV3702IP

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV3702CDR).

Table 4-4. TLV3704 Available Options

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)(1)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	5000 µV	TLV3704CD	—	TLV3704CPW
–40°C to 125°C		TLV3704ID	TLV3704IN	TLV3704IPW

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV3704CDR).

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5 Pin Configuration and Functions

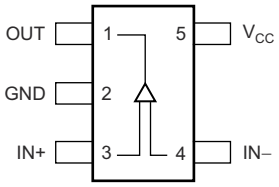


Figure 5-1. TLV3701 DBV Package 5-Pin SOT-23 Top View

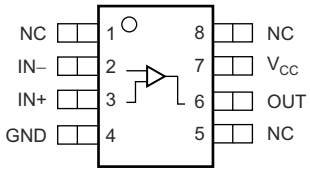


Figure 5-2. TLV3701 D or P Package 8-Pin SOIC or PDIP Top View

TLV3701 Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC, PDIP		
GND	2	4	—	Ground
IN–	4	2	I	Negative (inverting) input
IN+	3	3	I	Positive (noninverting) input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V_{CC}	5	7	—	Positive power supply

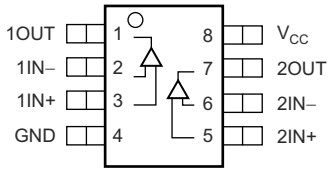


Figure 5-3. TLV3702 D, DGK, or P Package 8-Pin SOIC, VSSOP, or PDIP Top View

TLV3702 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	4	—	Ground
1IN–	2	I	Inverting input, channel 1
2IN–	6	I	Inverting input, channel 2
1IN+	3	I	Noninverting input, channel 1
2IN+	5	I	Noninverting input, channel 2
1OUT	1	O	Output, channel 1
2OUT	7	O	Output, channel 2
V_{CC}	8	—	Positive power supply

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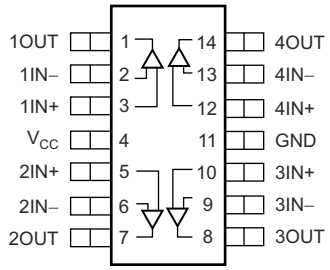


Figure 5-4. TLV3704 D, N, or PW Package 14-Pin SOIC, PDIP, or TSSOP Top View

TLV3704 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	11	—	Ground
1IN–	2	I	Inverting input, channel 1
2IN–	6	I	Inverting input, channel 2
3IN–	9	I	Inverting input, channel 3
4IN–	13	I	Inverting input, channel 4
1IN+	3	I	Noninverting input, channel 1
2IN+	5	I	Noninverting input, channel 2
3IN+	10	I	Noninverting input, channel 3
4IN+	12	I	Noninverting input, channel 4
1OUT	1	O	Output, channel 1
2OUT	7	O	Output, channel 2
3OUT	8	O	Output, channel 3
4OUT	14	O	Output, channel 4
V_{CC}	4	—	Positive power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		17	V
Differential input voltage, V_{ID}		±20	V
Input voltage, V_I (2) (3)	0	V_{CC} + 5	V
Input current, I_I		±10	mA
Output current, I_O		±10	mA
Maximum junction temperature, T_J		150	°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Input voltage range is limited to 20V maximum or V_{CC} + 5V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±TBD	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	C-suffix	2.5	16	V
		I-suffix	2.7	16	
	Split supply	C-suffix	±1.25	±8	
		I-suffix	±1.35	±8	
Common-mode input voltage, V_{ICR}			–0.1	V_{CC} + 5	V
Operating free-air temperature, T_A	C-suffix		0	70	°C
	I-suffix		–40	125	

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6.4 Thermal Information – TLV3701

THERMAL METRIC[1]		TLV3701			UNIT
		DBV (SOT-23)	D (SOIC)	P (PDIP)	
		5 PINS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.6	124.8	82.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.4	69.1	84.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	67.9	59.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.9	22.3	45.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.6	67.2	59.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Thermal Information – TLV3702

THERMAL METRIC[1]		TLV3702			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	163.9	77.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.4	65.7	79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.2	85.3	54	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.6	9	39.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.5	83.9	53.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.6 Thermal Information – TLV3704

THERMAL METRIC[1]		TLV3704			UNIT
		D (SOIC)	N (PDIP)	PW (TSSOP)	
		14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.4	58.1	105.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.1	50.9	33.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.8	38	49.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	23.6	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.4	37.7	48.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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6.7 Electrical Characteristics

At specified operating free-air temperature range, V_{CC} = 2.7V, 5V, 15V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
DC PERFORMANCE								
V_{IO}	Input offset voltage	$V_{IC} = V_{CC}/2$, R_S = 50Ω		25°C		250	5000	µV
				Full range			7000	
α_{VIO}	Offset voltage drift	$V_{IC} = V_{CC}/2$, R_S = 50Ω		25°C		3		µV/°C
V_{HYS}	Input hysteresis voltage	$V_{IC} = V_{CC}/2$, R_S = 50Ω		25°C	1	2.8	5	mV
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7V, R_S = 50Ω		25°C		72		dB
		V_{IC} = 0 to 5V, R_S = 50Ω		25°C		76		
		V_{IC} = 0 to 15V, R_S = 50Ω		25°C		88		
A_{VD}	Large-signal differential voltage amplification			25°C		1000		V/mV
INPUT/OUTPUT CHARACTERISTICS								
I_{IO}	Input offset current	$V_{IC} = V_{CC}/2$, R_S = 50Ω		25°C		20	100	pA
				Full range			1000	
I_{IB}	Input bias current	$V_{IC} = V_{CC}/2$, R_S = 50Ω		25°C		80	250	pA
				Full range			1500	
$r_{i(d)}$	Differential input resistance			25°C		300		MΩ
V_{OH}	High-level output voltage	$V_{IC} = V_{CC}/2$, I_{OH} = 2µA, V_{ID} = 1V		25°C		V_{CC} – 80		mV
		$V_{IC} = V_{CC}/2$, I_{OH} = – 50µA, V_{ID} = 1V		25°C	V_{CC} – 320			
				Full range	V_{CC} – 450			
V_{OL}	Low-level output voltage	$V_{IC} = V_{CC}/2$, I_{OH} = 2µA, V_{ID} = – 1V		25°C		8		mV
		$V_{IC} = V_{CC}/2$, I_{OH} = 50µA, V_{ID} = – 1V		25°C		80	200	
				Full range			300	
POWER SUPPLY								
I_{CC}	Supply current (per channel)	Output state high		25°C		560	800	nA
				Full range			1000	
PSRR	Power supply rejection ratio	$V_{IC} = V_{CC}/2$ V, No load	V_{CC} = 2.7V to 5V	25°C	75	100		dB
				Full range	70			
			V_{CC} = 5V to 15V	25°C	85	105		
				Full range	80			

(1) Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

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6.8 Switching Characteristics

At specified operating free-air temperature range, V_{CC} = 2.7V, 5V, 15V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(PLH)}$	Propagation response time, low-to-high-level output(1)	f = 10kHz, V_{STEP} = 100mV, C_L = 10pF	Overdrive = 10mV		34		µs
			Overdrive = 50mV		16		
$t_{(PHL)}$	Propagation response time, high-to-low-level output(1)	f = 10kHz, V_{STEP} = 100mV, C_L = 10pF	Overdrive = 10mV		45		µs
			Overdrive = 50mV		16		
t_r	Rise time	C_L = 10pF			0.2		µs
t_f	Fall time	C_L = 10pF			0.2		µs
t_{su}	Start-up time	V_{CC} = 2.7 to 15V(2)	25°C		3		ms

(1) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.
(2) The definition of start-up time is the time period between the supply voltage reaching minimum supply (V_{CCmin}) and the device IQ activating (I_{CCmin}) with a valid device output voltage. Single device only.

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6.9 Typical Characteristics

At T_A = 25°C, V_S = 12V, VCM = V_S/2 V, R_P = 1MΩ (Open Drain only), C_L = 25pF, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

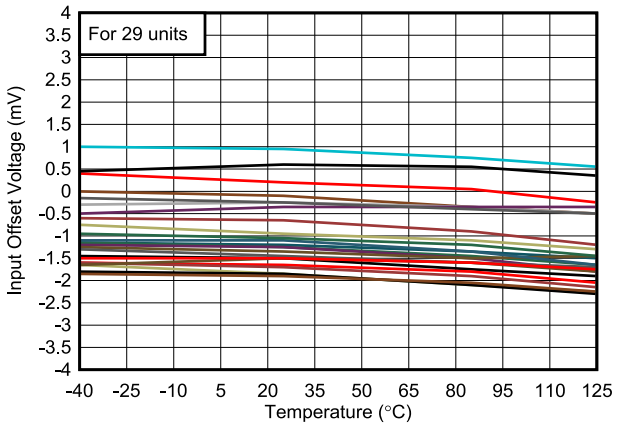


Figure 6-1. Offset vs. Temperature

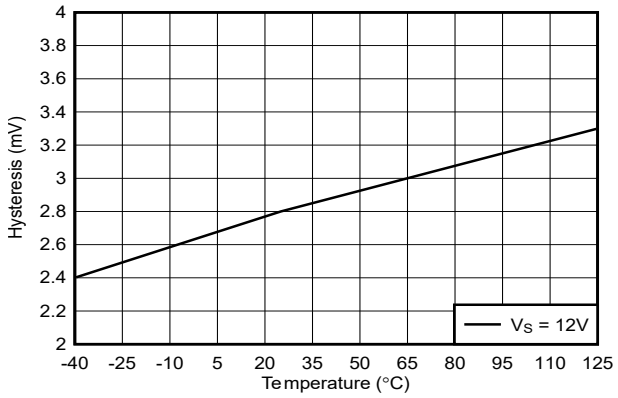


Figure 6-2. Hysteresis vs. Temperature

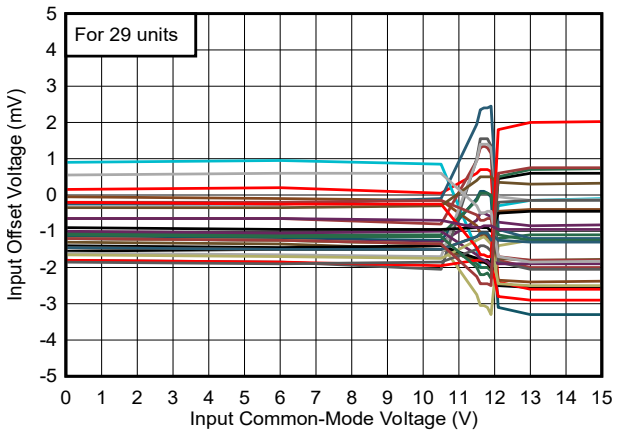


Figure 6-3. Offset vs. Common-Mode, 12V

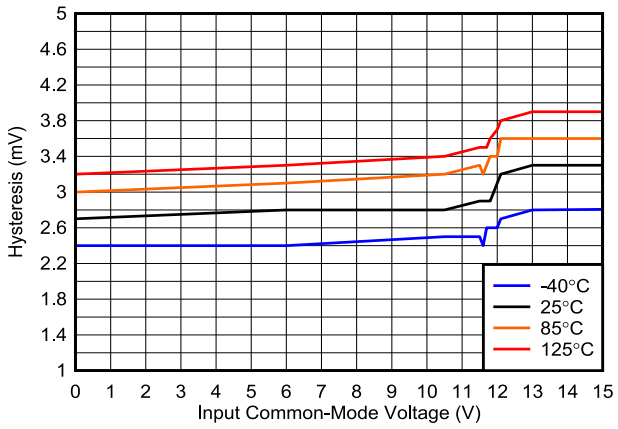


Figure 6-4. Hysteresis vs. Common-Mode, 12V

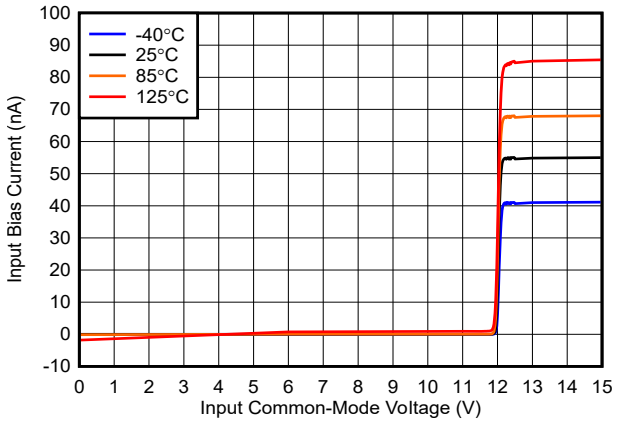


Figure 6-5. Bias Current vs. Common-Mode, 12V

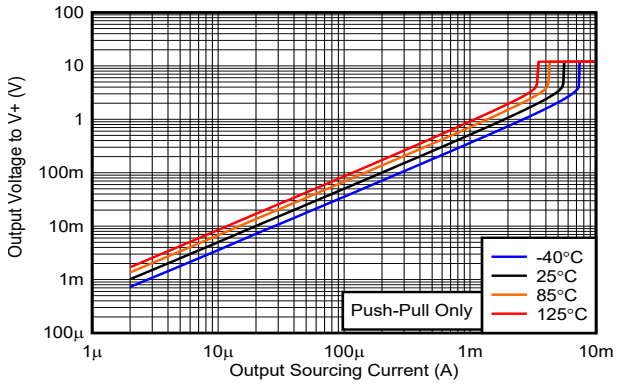


Figure 6-6. Output Voltage vs. Output Sourcing Current, 12V

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6.9 Typical Characteristics (continued)

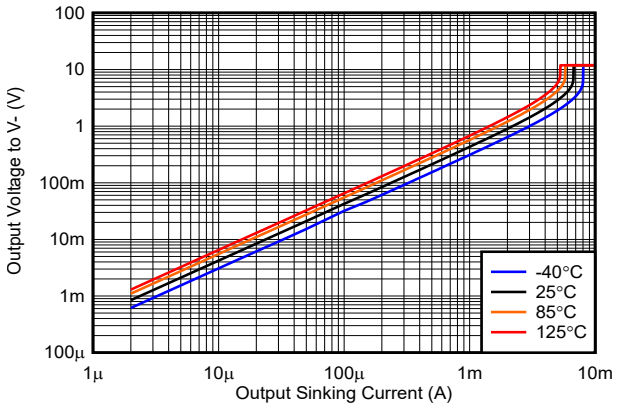


Figure 6-7. Output Voltage vs. Output Sinking Current, 12V

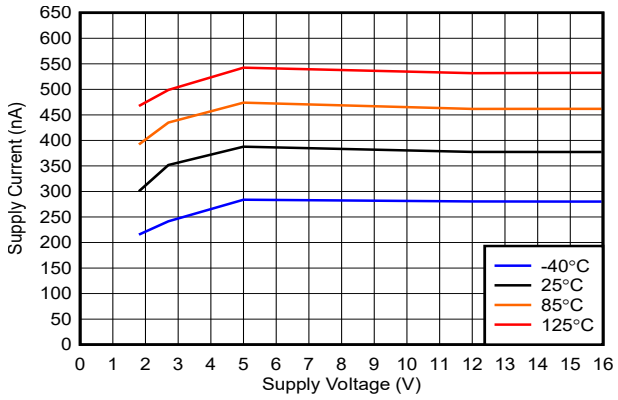


Figure 6-8. Supply Current vs. Supply Voltage (Output Low), Push-Pull

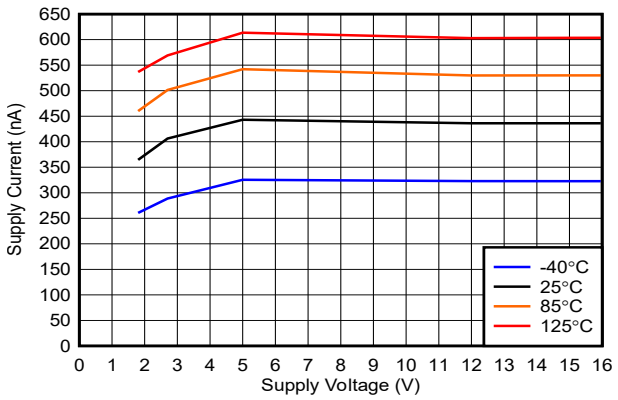


Figure 6-9. Supply Current vs. Supply Voltage (Output High), Push-Pull

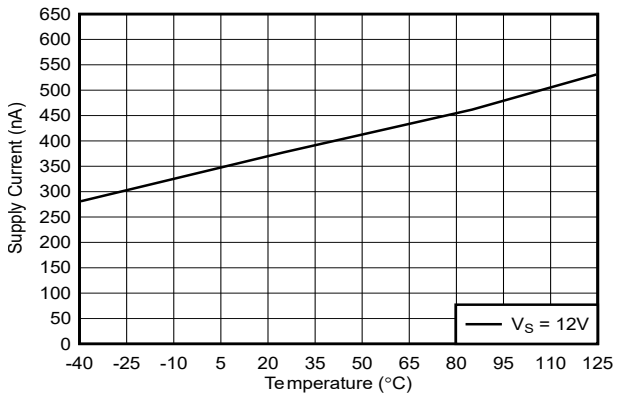


Figure 6-10. Supply Current vs. Temperature (Output Low), Push-Pull

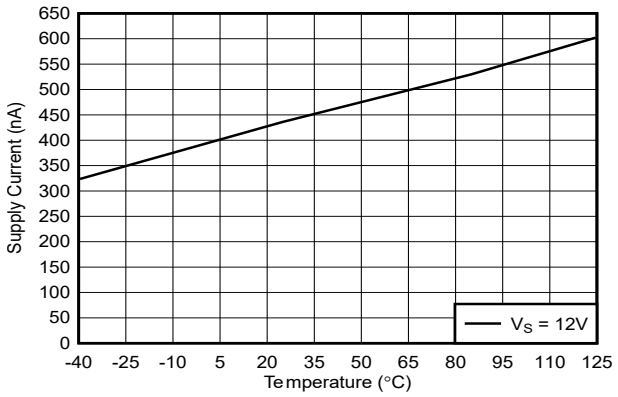


Figure 6-11. Supply Current vs. Temperature (Output High), Push-Pull

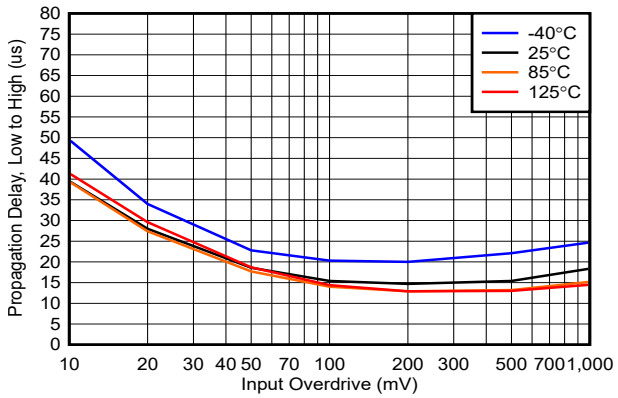


Figure 6-12. Propagation Delay, Low to High, 12V, Push-Pull

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6.9 Typical Characteristics (continued)

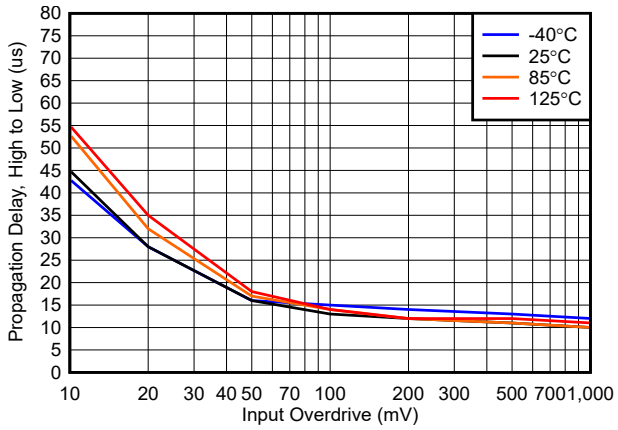


Figure 6-13. Propagation Delay, High to Low, 12V

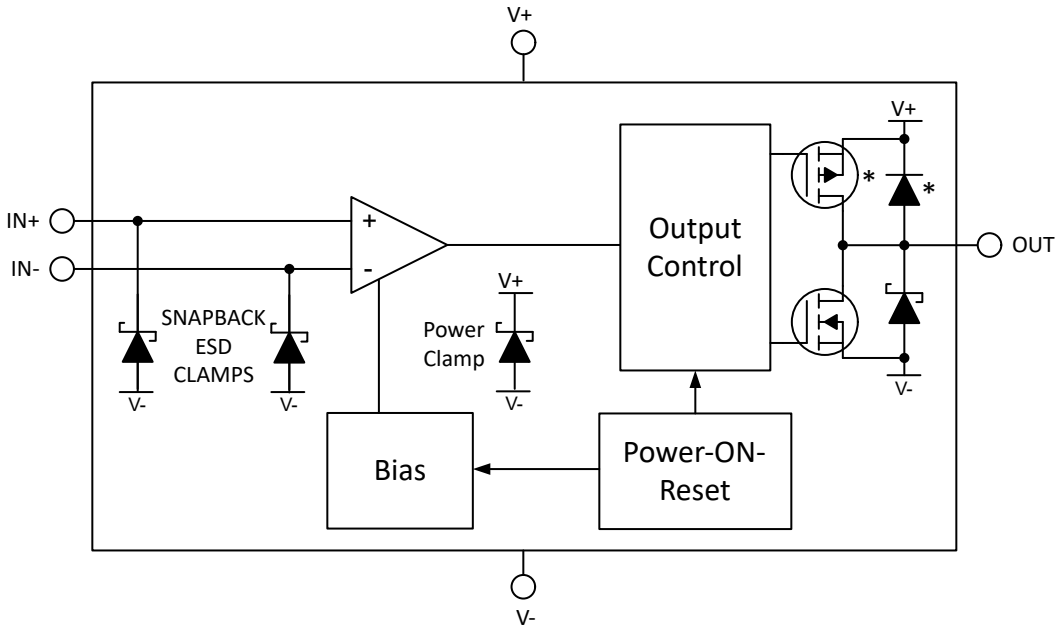
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7 Detailed Description

7.1 Overview

The TLV370x is a family of nanopower comparators drawing only 560nA per channel supply current. Having a minimum operating supply voltage of 2.7V over the extended industrial temperature range (T_A = –40°C to +125°C), while having an input common-mode range of –0.1 to V_{CC} + 5V makes this device ideal for battery-powered and wireless handset applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLV370x comparators are specified for use on a single supply from 2.5V to 16V (or a dual supply from ±1.25V to ±16V) over a temperature range of −40°C to +125°C.

7.3.1.1 Power-On Reset (POR)

The TLV370x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 3ms after the V_{POR} of 1.5V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV370x push-pull output devices, the output is held low during the POR period (t_{on}).

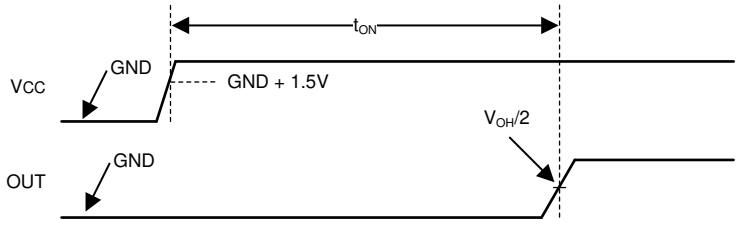
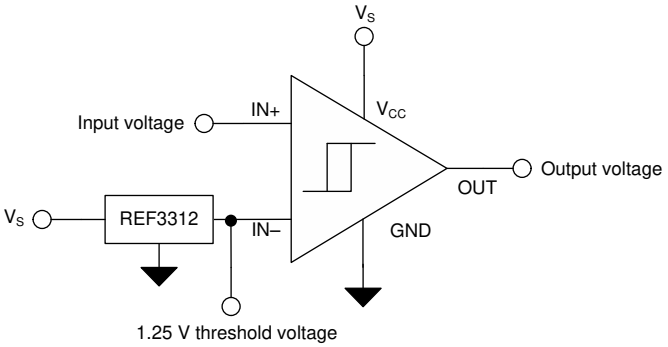


Figure 7-1. Power-On Reset Timing Diagram

7.3.2 Setting the Threshold

Using a low-power, stable reference is important when setting the transition point for the devices. The REF3312, as shown in Figure 7-2, provides a 1.25V reference voltage with low drift and only 3.9µA of quiescent current.



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Figure 7-2. Setting the Threshold

7.4 Device Functional Modes

The TLV370x has a single functional mode and is operational when the power supply voltage applied ranges from 2.5V (±1.25V) to 16V (±8V).

7.4.1 Inputs

7.4.1.1 Operating Common-Mode Ranges

The TLV370x devices have two operating common-mode ranges: within-the-rail and over-the-rail.

Within-the-Rail Operation: IN+ and IN- are less than (V+)

When an input pin is operating less than (V+), there are two operating regions defined where input voltages can be compared: low common-mode and high-common mode. In low-common mode which extends typically from 0V to (V+) - 1V, the typical input bias current is less than 1pA. In high common-mode which extends typically from (V+) - 1V to (V+), the typical input bias current is less than 14nA.

Over-the-Rail Operation: IN+ and/or IN- are greater than (V+)

The TLV370x devices have a distinctive input stage that allows the input common mode range to extend from 0V to 16V independent of the supply voltage. This feature means that operation at low supply voltages does not limit the range of input voltages that can be compared. When an input pin is operating over-the-rail (above (V+)), the bias current increases to a typical value of 55nA.

7.4.1.2 Fail-Safe Inputs

A feature of the TLV370x family is that the inputs are fail safe up to 16V, independent of (V+). The inputs are maintained as high input impedance and can be of any value between -0.1V and 16V, even while (V+) is unpowered or below the minimum supply voltage. This feature avoids power sequencing or transient issues since the inputs are not diode clamped to (V+).

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8 Application and Implementation

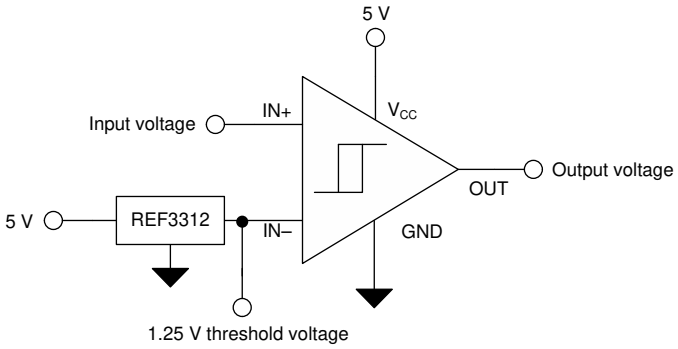
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Many applications require the detection of a signal (voltage or current) that exceeds a particular threshold voltage or current. Using a comparator to make that threshold detection is the easiest, lowest power and highest speed way to make a threshold detection.

8.2 Typical Application



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Figure 8-1. 1.25V Threshold Detector

8.2.1 Design Requirements

- Detect when a signal is above or below 1.25V
- Operate from a single 5V power supply
- Rail-to-rail input voltage range from 0 to 5V
- Rail-to-rail output voltage range from 0 to 5V

8.2.2 Detailed Design Procedure

The input voltage range in the circuit illustrated in Figure 8-1 is limited only by the power supply applied to the TV3701. In this example with the selection of a 5V, single-supply power supply, the input voltage range is limited to 0 to V_S + 5V, or 0 to 10V. The threshold voltage of 1.25V can be derived in a variety of ways. As the TLV3701 is a very low-power device, it is desirable to also use very low power to create the threshold voltage. The REF3312 series voltage reference is selected for its stable output voltage of 1.25V and its low power consumption of only 3.9µA. The TLV3701 is an push-pull output comparator, and does not require a pullup resistor to save power.

8.2.3 Application Curve

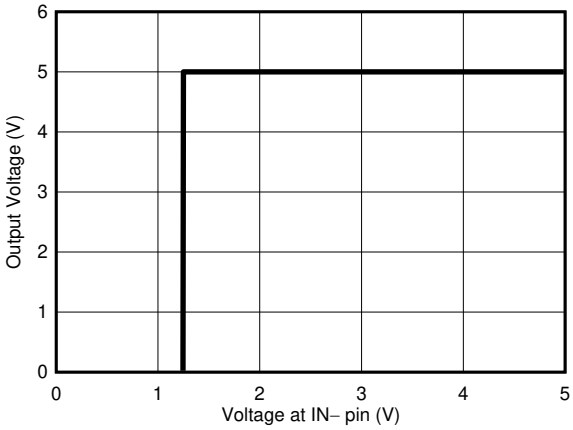


Figure 8-2. Transfer Function for the Threshold Detector

8.3 Power Supply Recommendations

The TLV370x device is specified for operation from 2.5V to 16V (±1.25 to ±8V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 6.9*.

8.4 Layout

8.4.1 Layout Guidelines

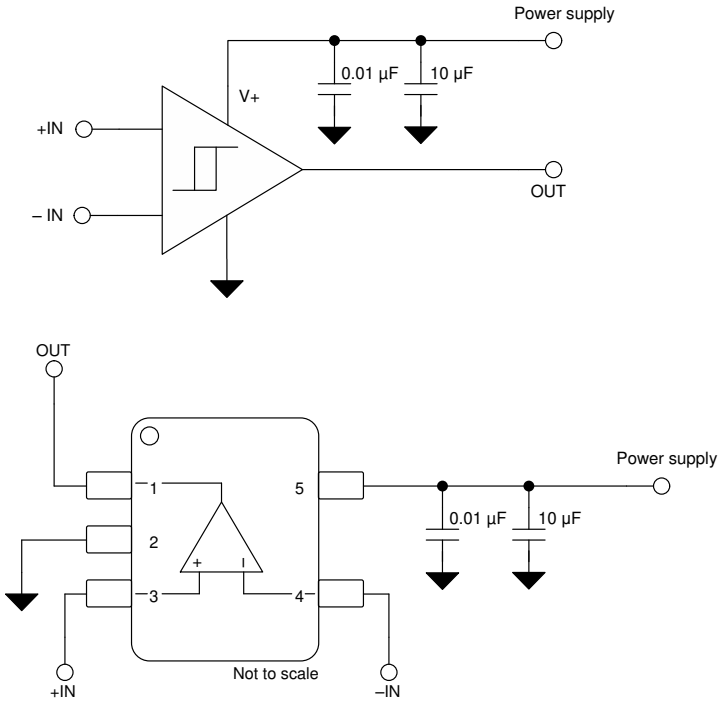
Figure 8-3 shows the typical connections for the TLV370x. To minimize supply noise, power supplies must be capacitively decoupled by a 0.01µF ceramic capacitor in parallel with a 10µF electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (the use of a ground plane) helps to maintain the specified performance of the TLV370x family.

For best results, maintain the following layout guidelines:

1. Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The top-side ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

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8.4.2 Layout Example



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Figure 8-3. TLV3701 SOT-23 Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (8-pin SOIC), PW (8-pin TSSOP), DGK (8-pin MSOP), DBV (6-pin SOT-23, 5-pin SOT23, and 3-pin SOT-23), DCK (6-pin SC-70 and 5-pin SC-70), and DRL (6-pin SOT-563). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

9.1.1.2 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP, and SOT-23 packages are all supported.

Note

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

9.2 Documentation Support

9.2.1 Related Documentation

The following documents are relevant for using the TLV370x devices and are recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- Texas Instruments, *Universal Op Amp EVM User Guide*
- Texas Instruments, *Hardware Pace Using Slope Detection*
- Texas Instruments, *Bipolar High-voltage Differential Interface for Low-Voltage Comparators*
- Texas Instruments, *AC-Coupled Single Supply Comparator*
- Texas Instruments, *ECG Implementation on the TMS320VC5505 DSP Medical Development Kit*
- Texas Instruments, *REF33xx 3.9-µA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/°C Drift Voltage Reference*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision D (May 2017) to Revision E (December 2025) **Page**

- Removed Dissipation Ratings table....6
- Updated Switching Characteristics table....9
- Updated Typical Performance Curves....10
- Updated the Functional Block Diagram....13
- Added Power-On Reset information....13
- Added Device Functional Modes information....14

Changes from Revision C (March 2017) to Revision D (May 2017) **Page**

- Changed Wording of Start-up time table note....9

Changes from Revision B (August 2001) to Revision C (March 2017) **Page**

- Added *Device Information* table, *Device Comparison* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Changed VOH typical value from 0.08 to 80 to reflect proper units....8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3701CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3701C
TLV3701CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3701C
TLV3701CDBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	0 to 70	VBCC
TLV3701ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3701I
TLV3701ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3701I
TLV3701IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBCI
TLV3701IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBCI
TLV3701IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV3701IDBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	VBCI
TLV3701IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3701I
TLV3701IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3701I
TLV3701IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV3701I
TLV3701IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV3701I
TLV3702CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3702C
TLV3702CDGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	0 to 70	AKC
TLV3702CDGKR	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	0 to 70	AKC
TLV3702ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	3702I
TLV3702IDGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	AKD
TLV3702IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKD
TLV3702IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKD
TLV3702IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV3702IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702I
TLV3702IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702I
TLV3702IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV3702I
TLV3702IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV3702I
TLV3704CD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3704C
TLV3704CD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3704C
TLV3704CPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	3704C
TLV3704ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3704ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I
TLV3704IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I
TLV3704IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I
TLV3704IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV3704I
TLV3704IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV3704I
TLV3704IPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	3704I
TLV3704IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I
TLV3704IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3701, TLV3702 :

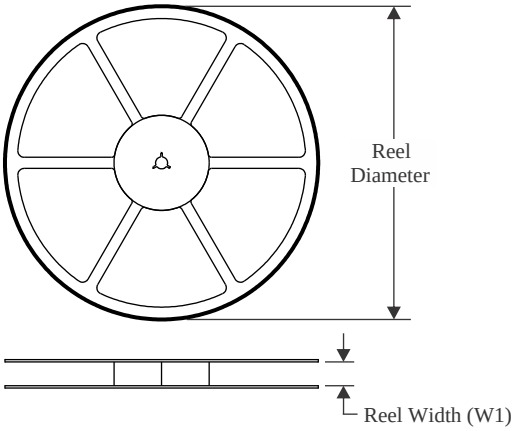
- Automotive : TLV3701-Q1, TLV3702-Q1
- Enhanced Product : TLV3701-EP

NOTE: Qualified Version Definitions:

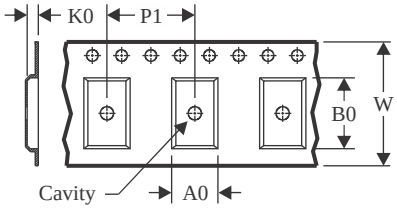
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

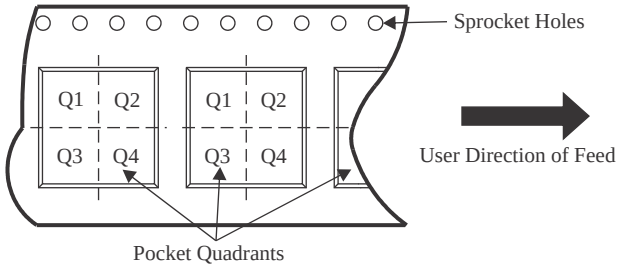


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

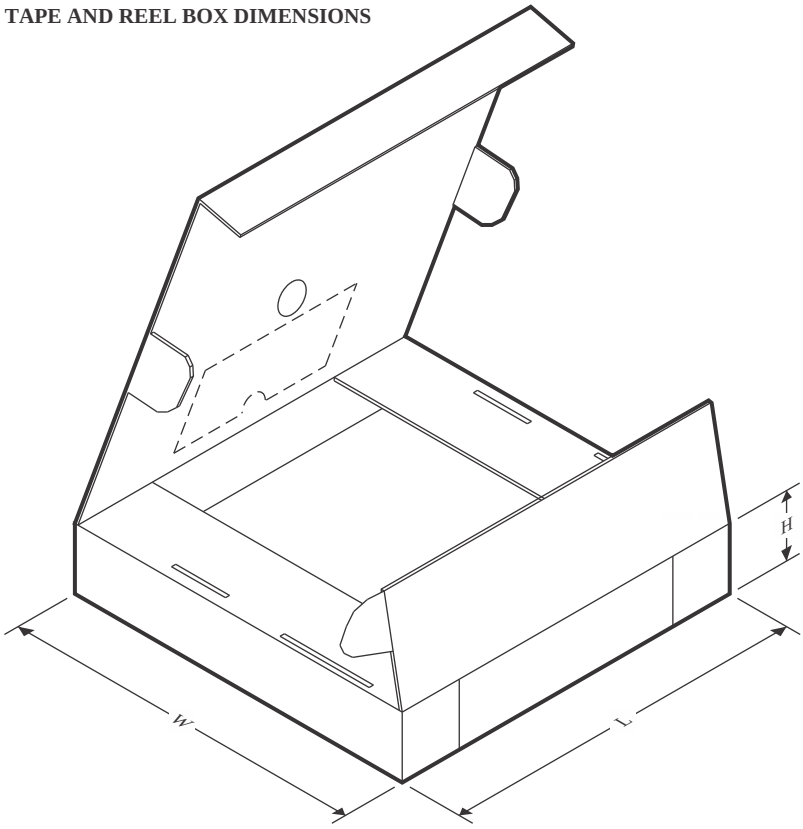
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3701IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3701IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3701IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3702IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3702IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3704IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV3704IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

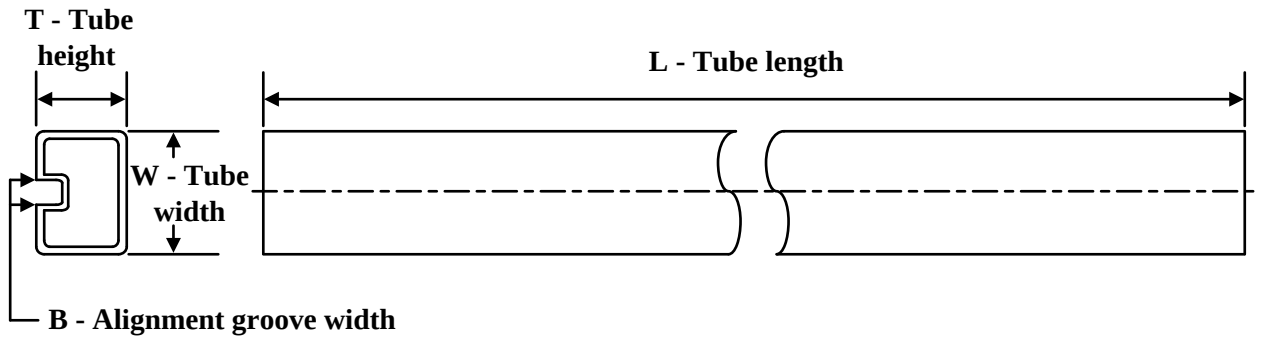
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3701IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV3701IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV3701IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV3702IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV3702IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV3704IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV3704IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

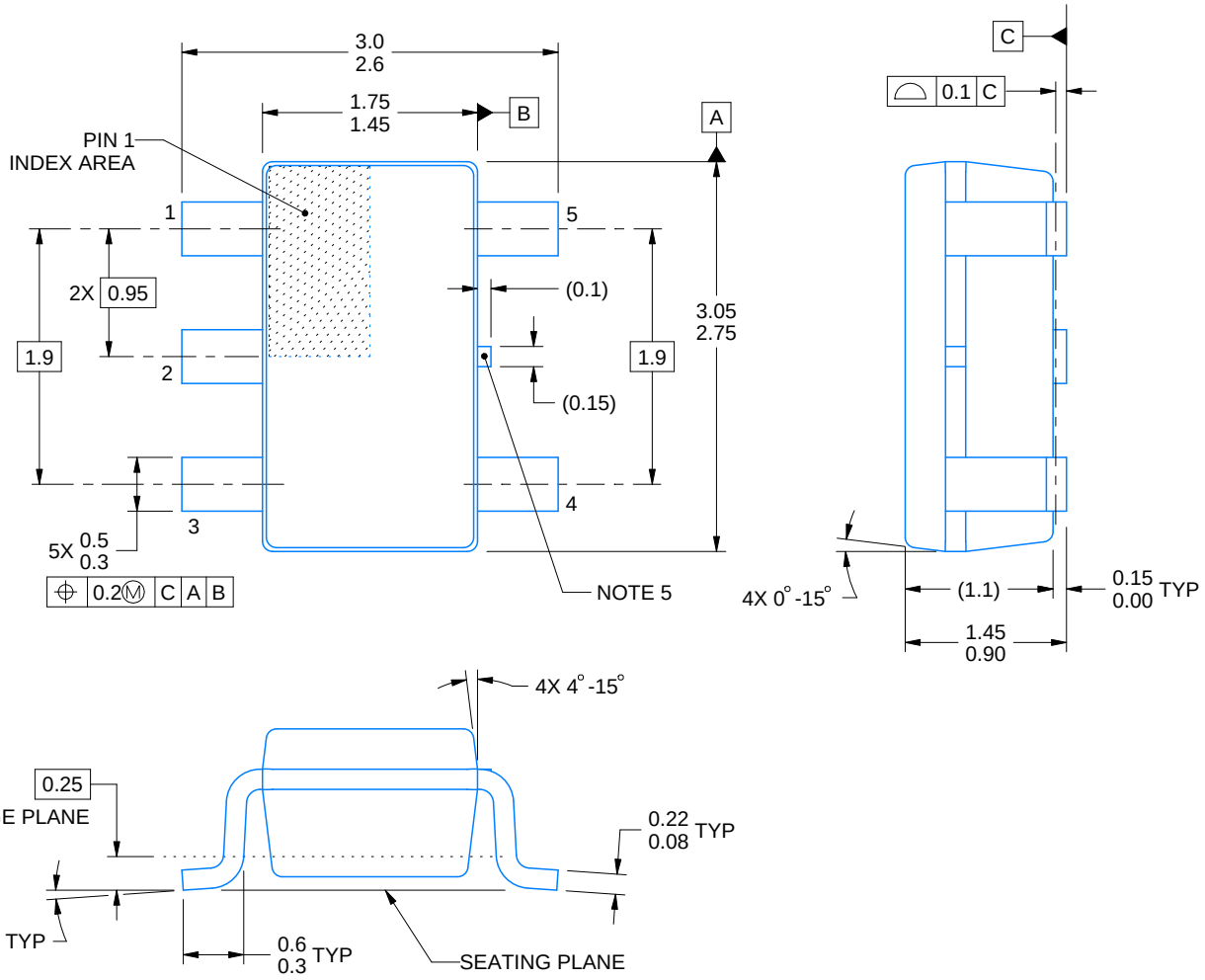
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV3701CD	D	SOIC	8	75	507	8	3940	4.32
TLV3701CD.A	D	SOIC	8	75	507	8	3940	4.32
TLV3701ID	D	SOIC	8	75	507	8	3940	4.32
TLV3701ID.A	D	SOIC	8	75	507	8	3940	4.32
TLV3701IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV3701IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLV3702IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV3702IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLV3704CD	D	SOIC	14	50	507	8	3940	4.32
TLV3704CD.A	D	SOIC	14	50	507	8	3940	4.32
TLV3704ID	D	SOIC	14	50	507	8	3940	4.32
TLV3704ID.A	D	SOIC	14	50	507	8	3940	4.32
TLV3704IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV3704IN.A	N	PDIP	14	25	506	13.97	11230	4.32

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

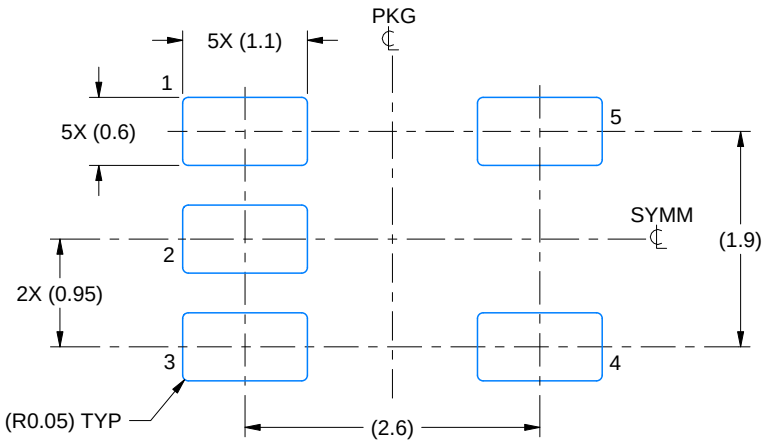
SMALL OUTLINE TRANSISTOR



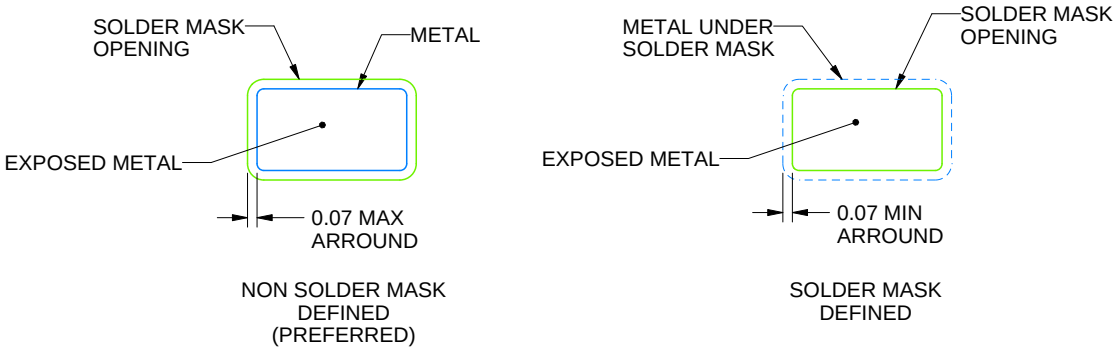
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

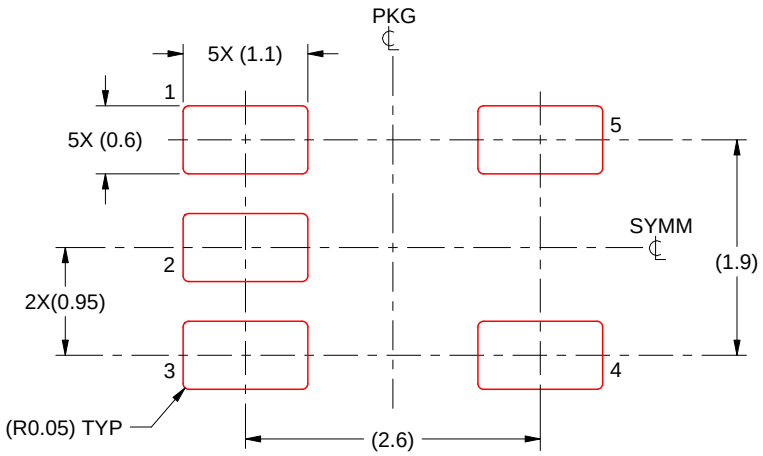


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

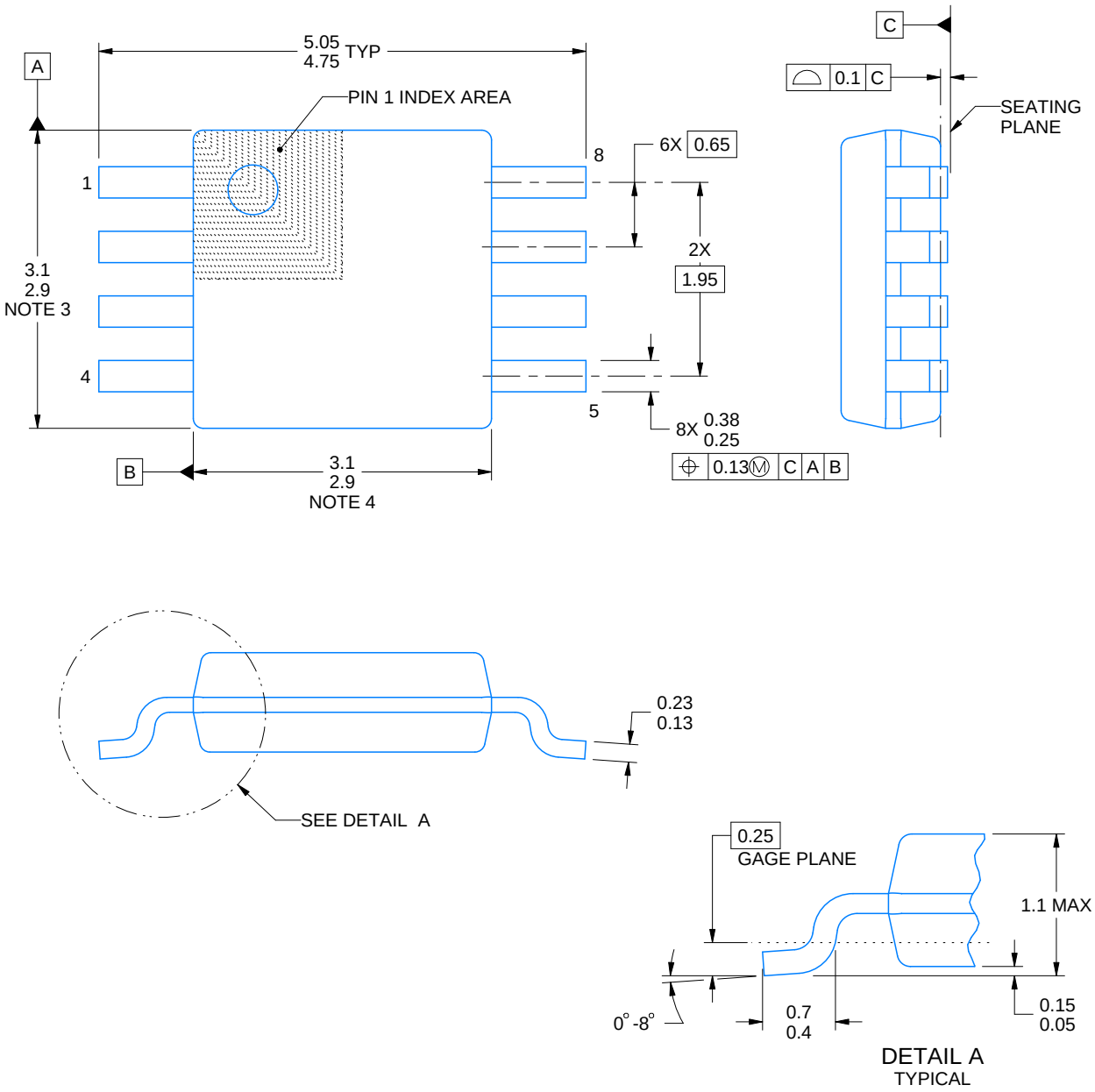
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

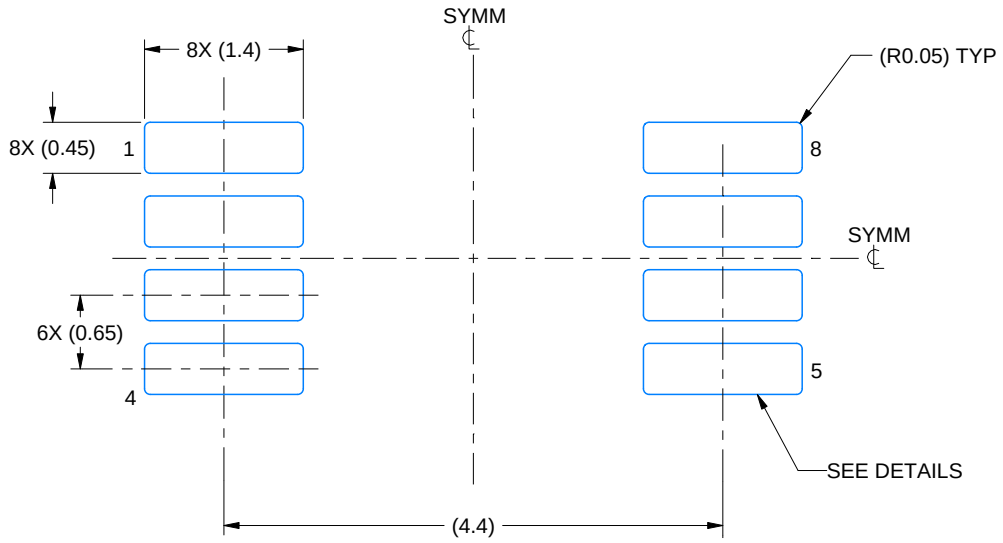
SMALL OUTLINE PACKAGE



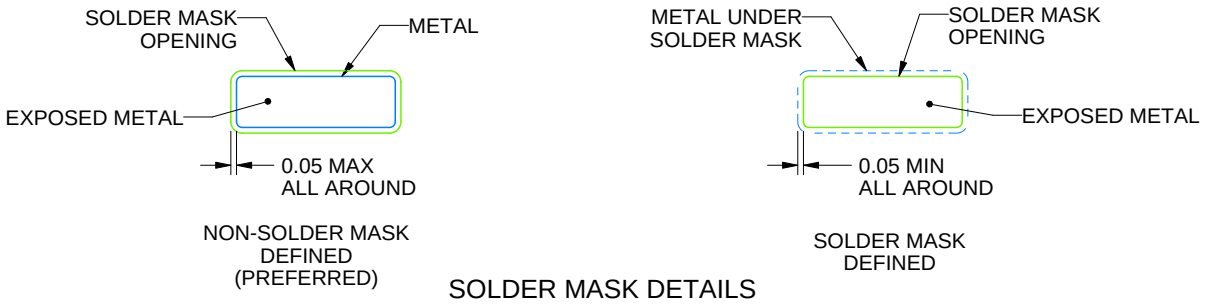
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

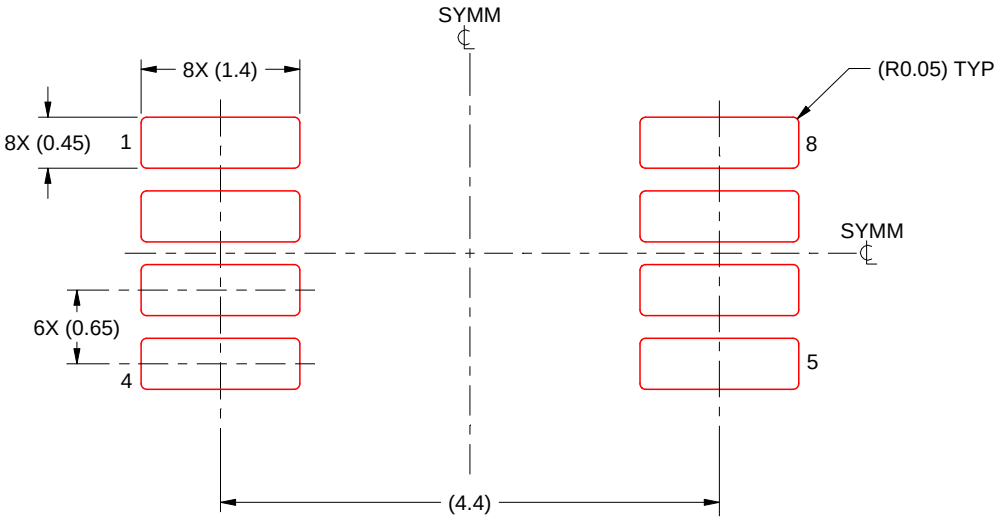


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

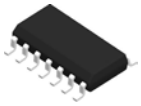


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

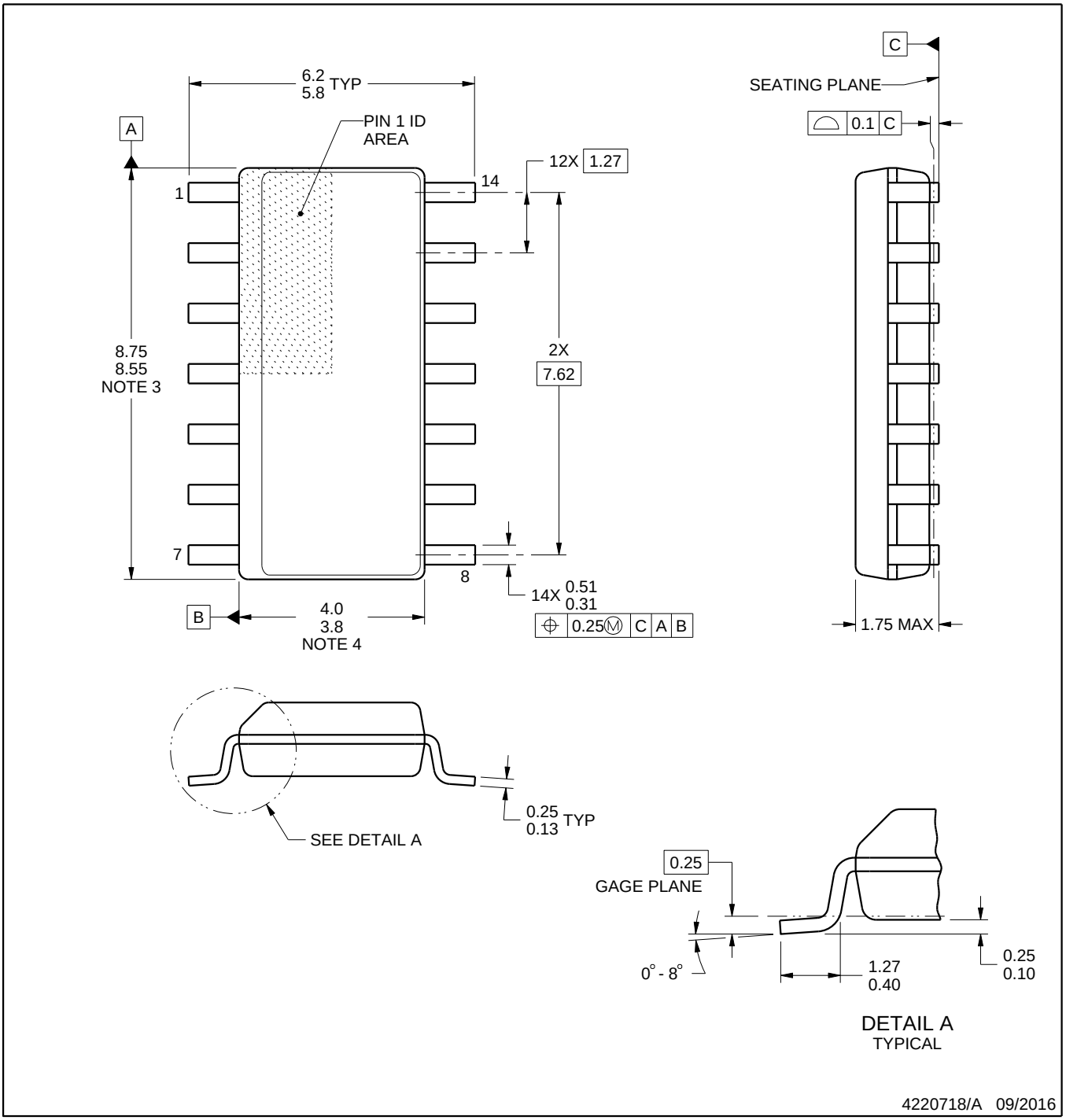


PACKAGE OUTLINE

D0014A

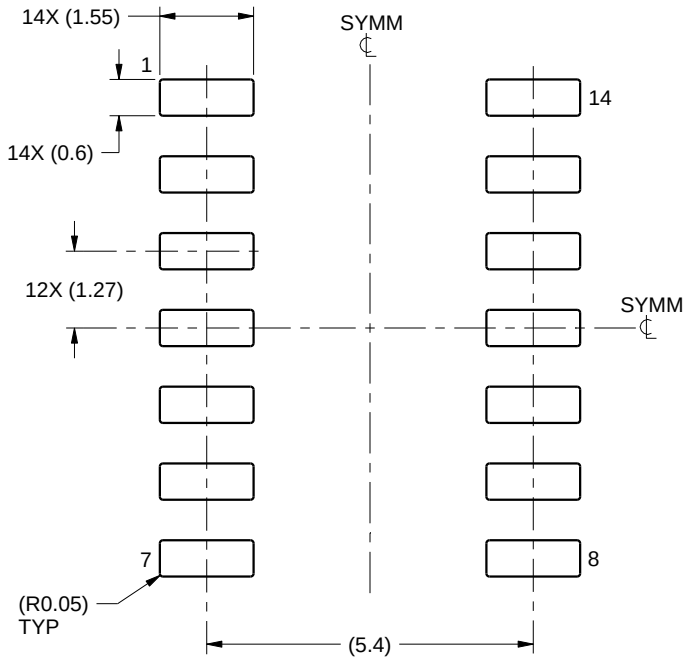
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

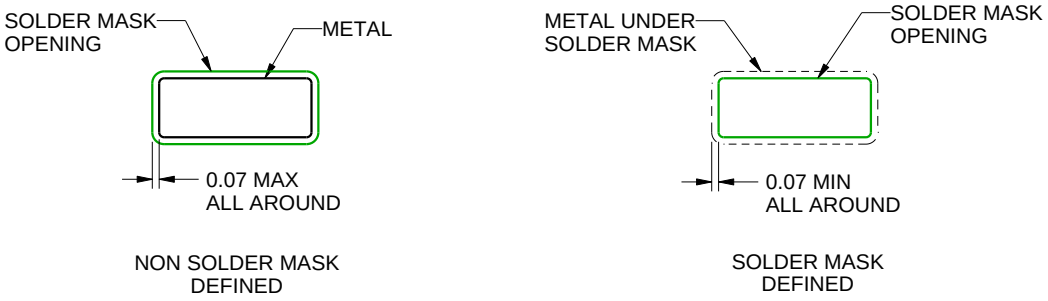


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

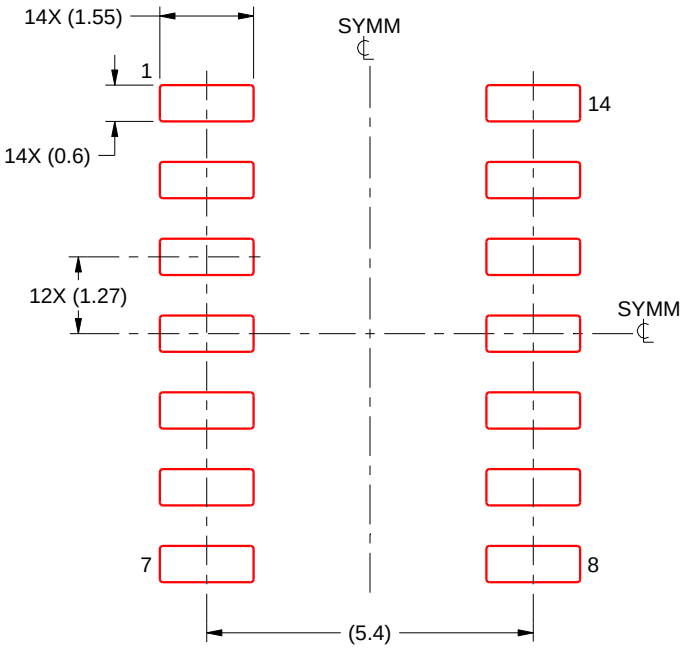
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

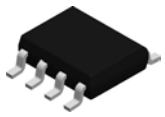


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

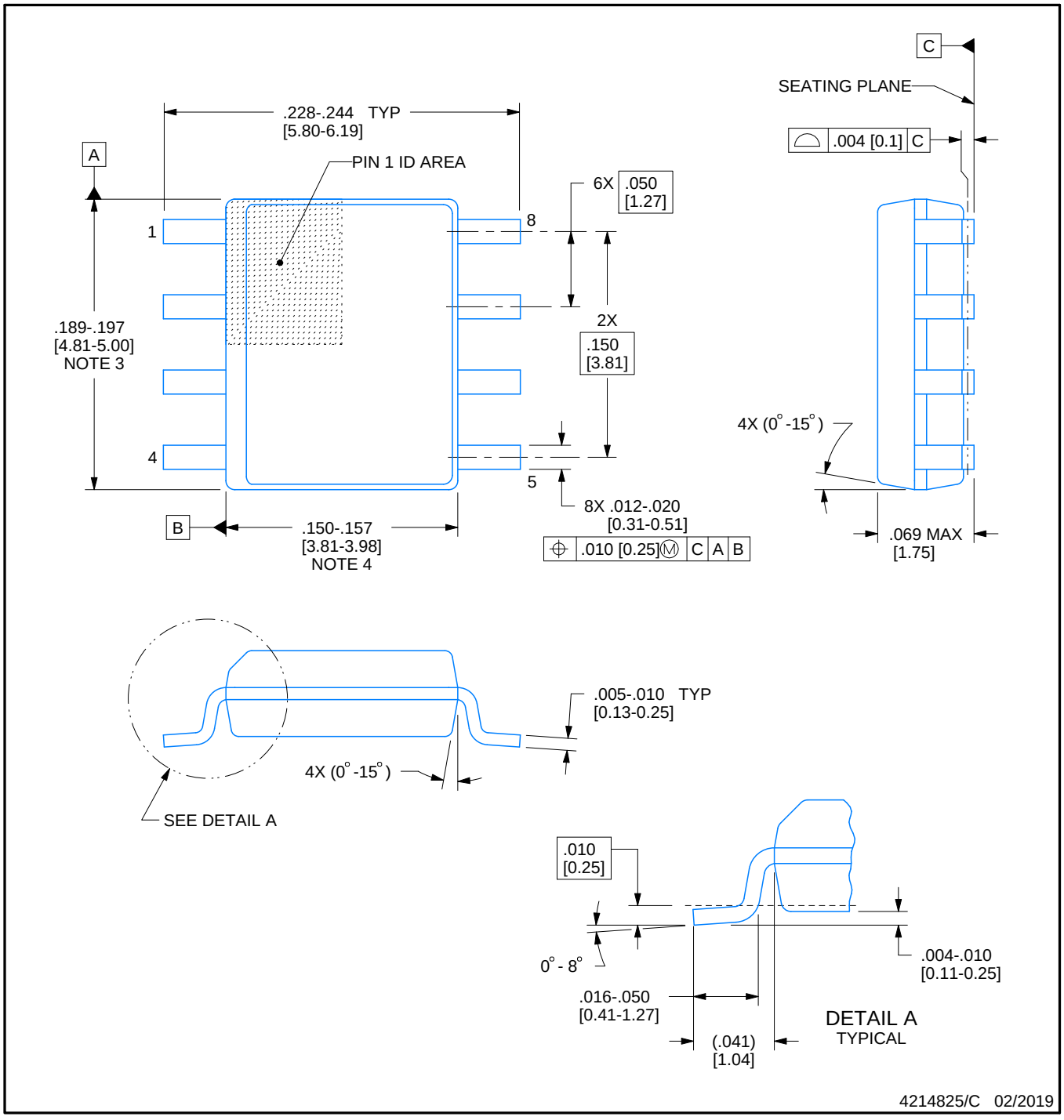


PACKAGE OUTLINE

D0008A

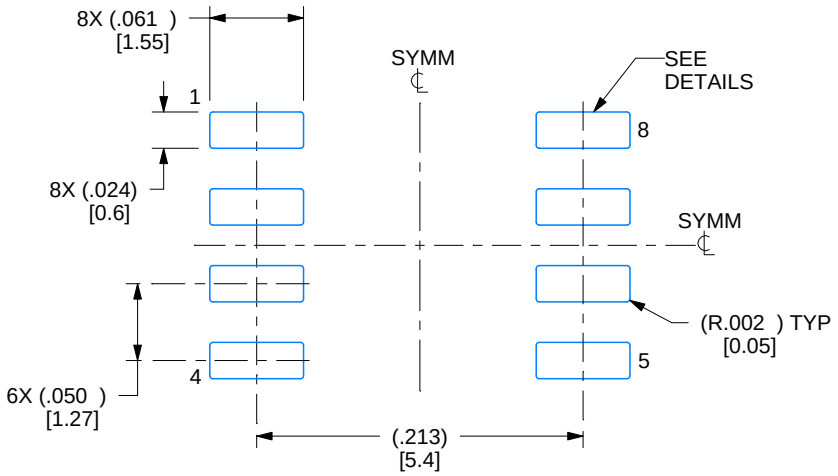
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

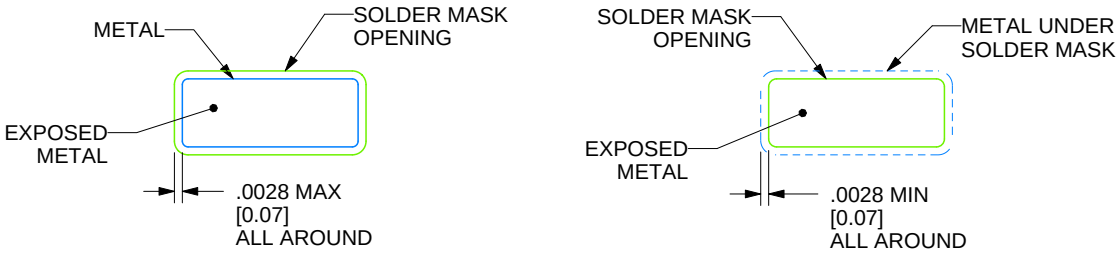


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

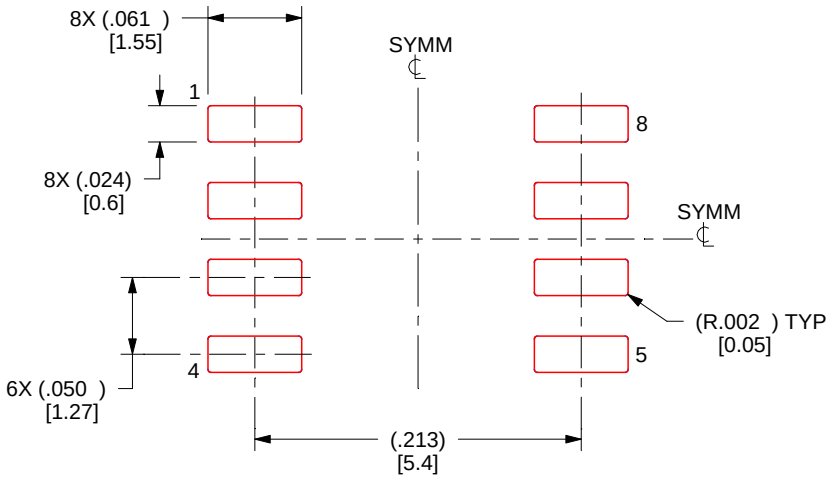
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



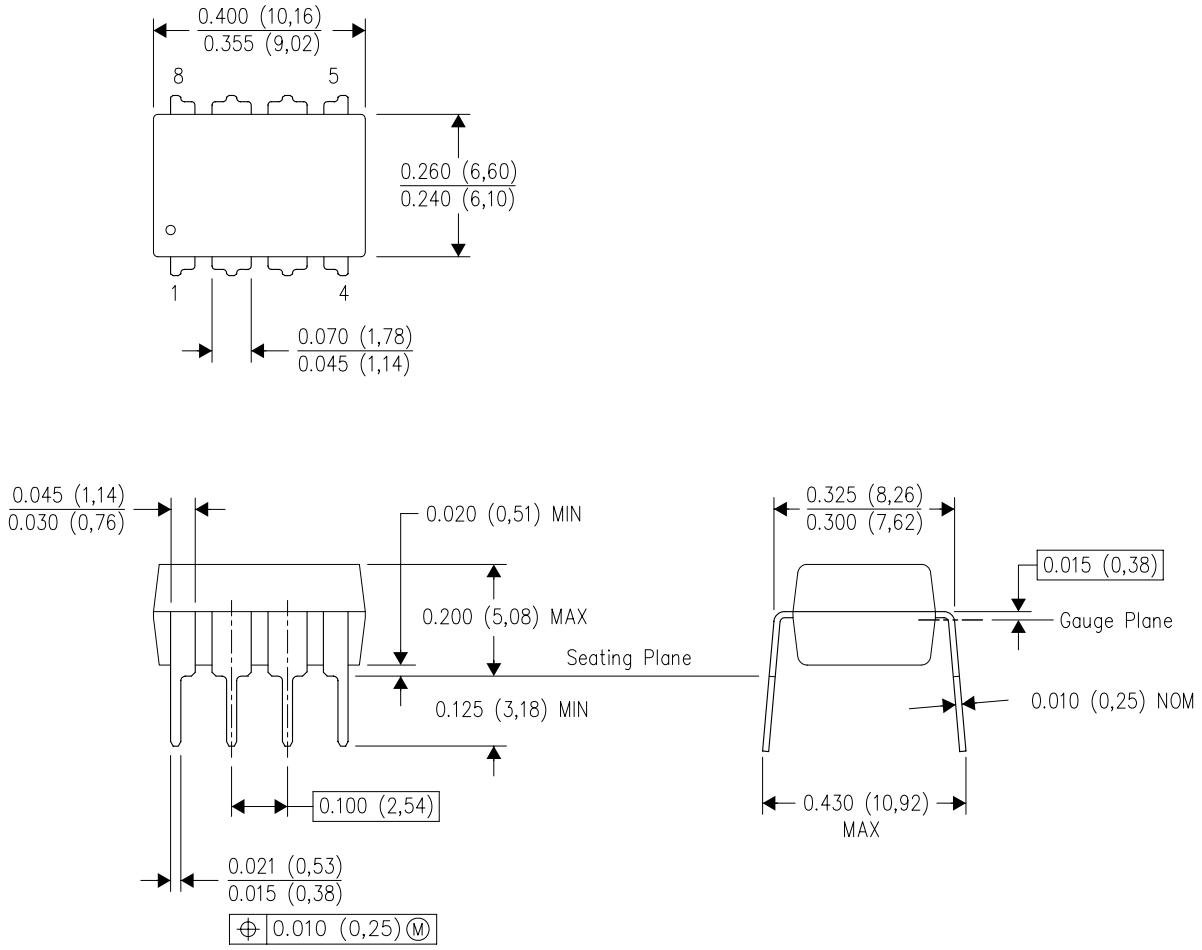
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

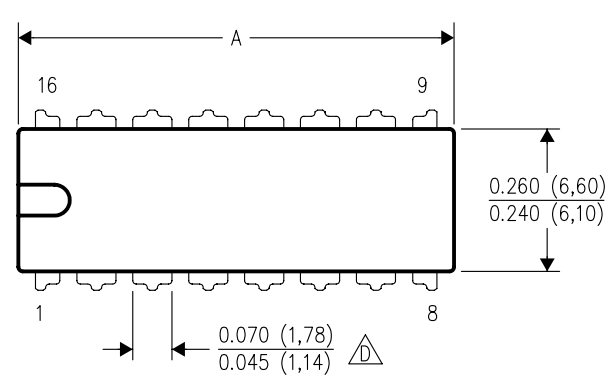


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

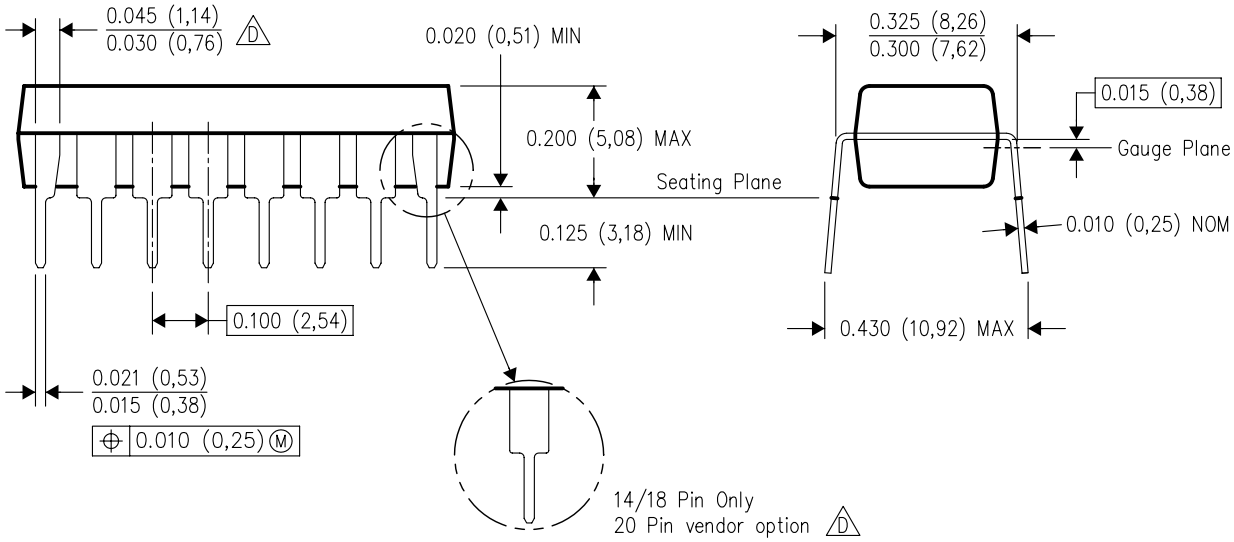
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

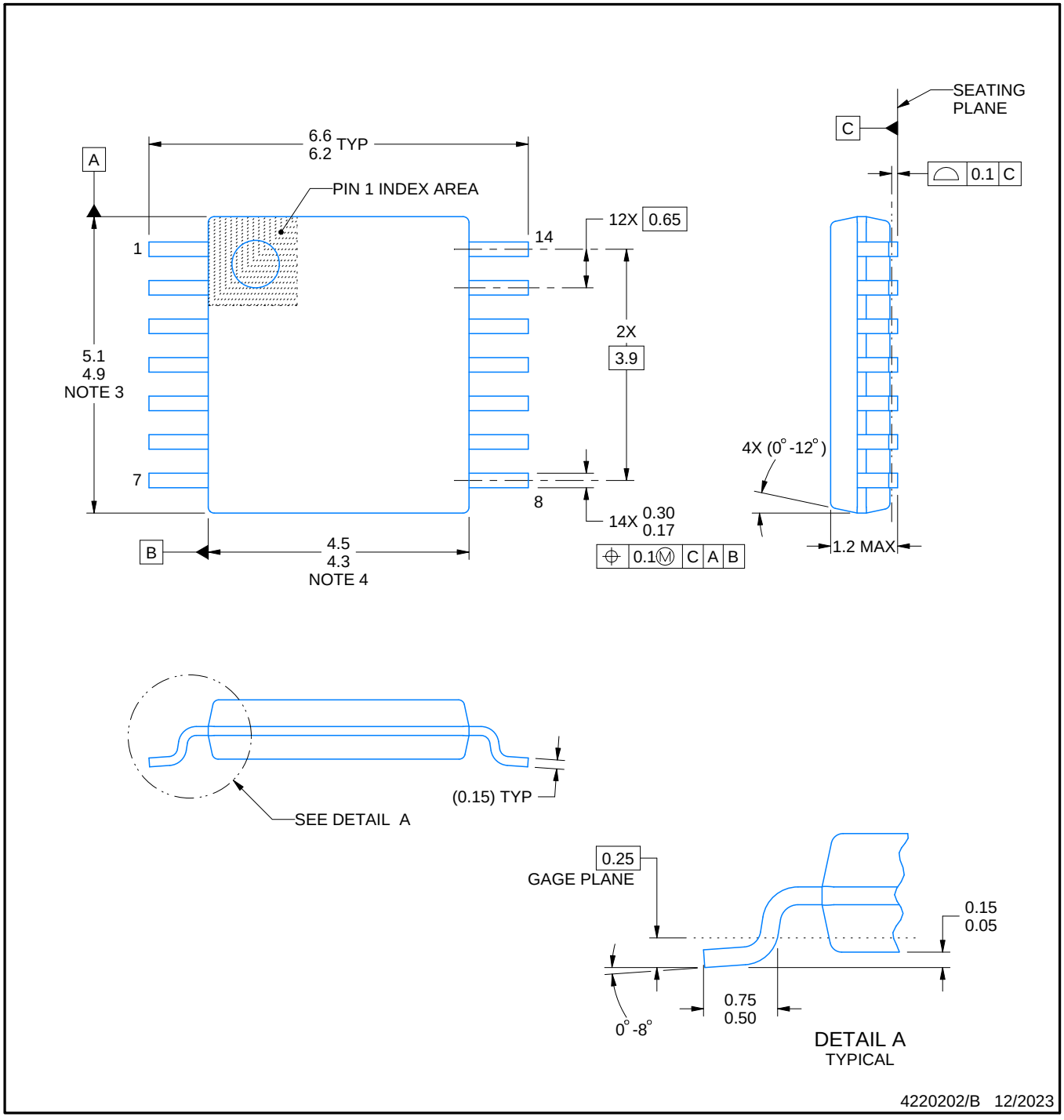
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

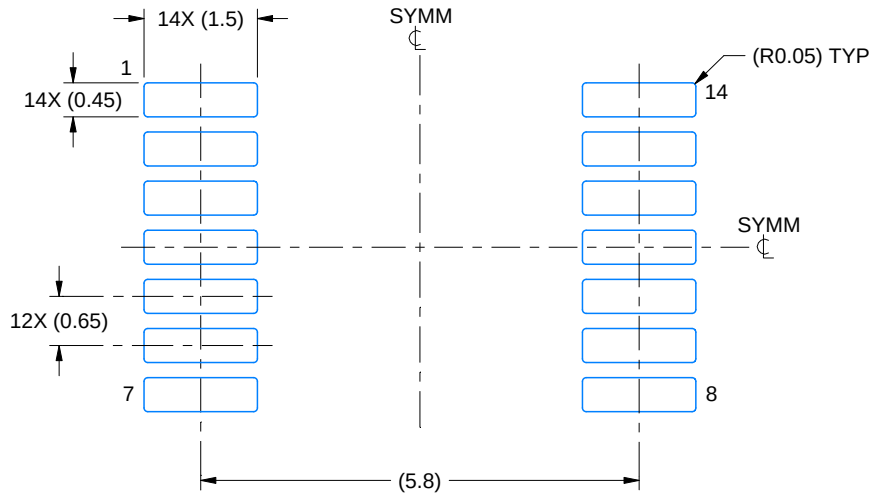
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

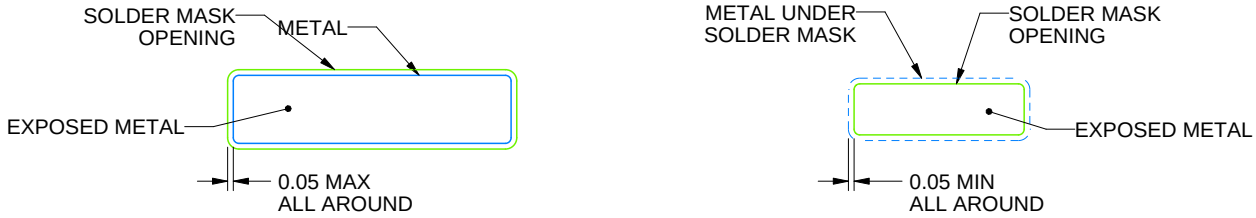


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

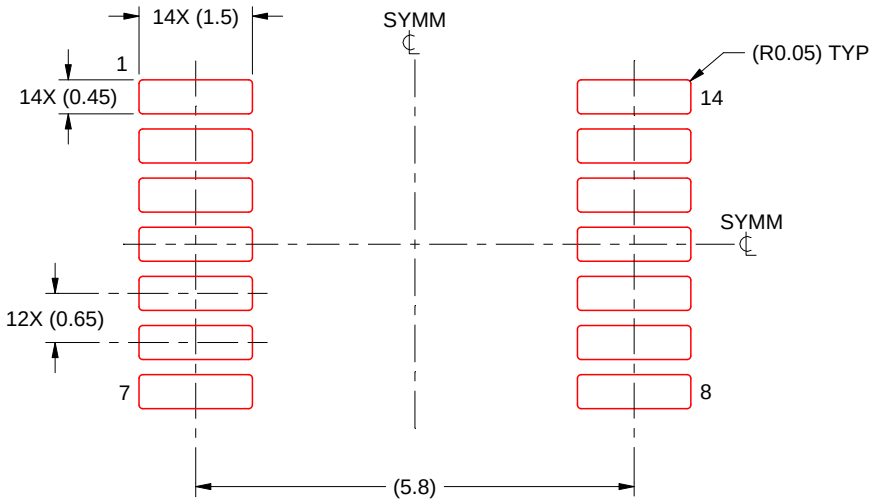


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025