TLV320AIC3212 Ultra-Low Power Stereo Audio Codec With Receiver Driver, DirectPath Headphone, and Stereo Class-D Speaker Amplifier

1 Features

- Stereo Audio DAC With 101=dB SNR
- 2.7-mW Stereo 48-kHz DAC Playback
- Stereo Audio ADC With 93-dB SNR
- 5.6-mW Stereo 48-kHz ADC Record
- 8 kHz to 192 kHz Playback and Record
- 30-mW DirectPath™ Headphone Driver Eliminates Large Output DC-Blocking Capacitors
- 128-mW Differential Receiver Output Driver
- Stereo Class-D Speaker Drivers
  - 1.7 W (8 Ω, 5.5 V, 10% THDN)
  - 1.4 W (8 Ω, 5.5 V, 1% THDN)
- Stereo Line Outputs
- PowerTune™ - Adjusts Power vs SNR
- Extensive Signal Processing Options
- Eight Single-Ended or 4 Fully-Differential Analog Inputs
- Stereo Digital and Analog Microphone Inputs
- Low Power Analog Bypass Mode
- Programmable PLL, Plus Low-Frequency Clocking
- Programmable 12-Bit SAR ADC
- SPI and I^2C Control Interfaces
- Three Independent Digital Audio Serial Interfaces
- 4.81 mm × 4.81 mm × 0.625 mm 81-Ball WCSP (YZF) Package

2 Applications

- Mobile Handsets
- Tablets and eBooks
- Portable Navigation Devices (PND)
- Portable Media Players (PMP)
- Portable Gaming Systems
- Portable Computing

3 Description

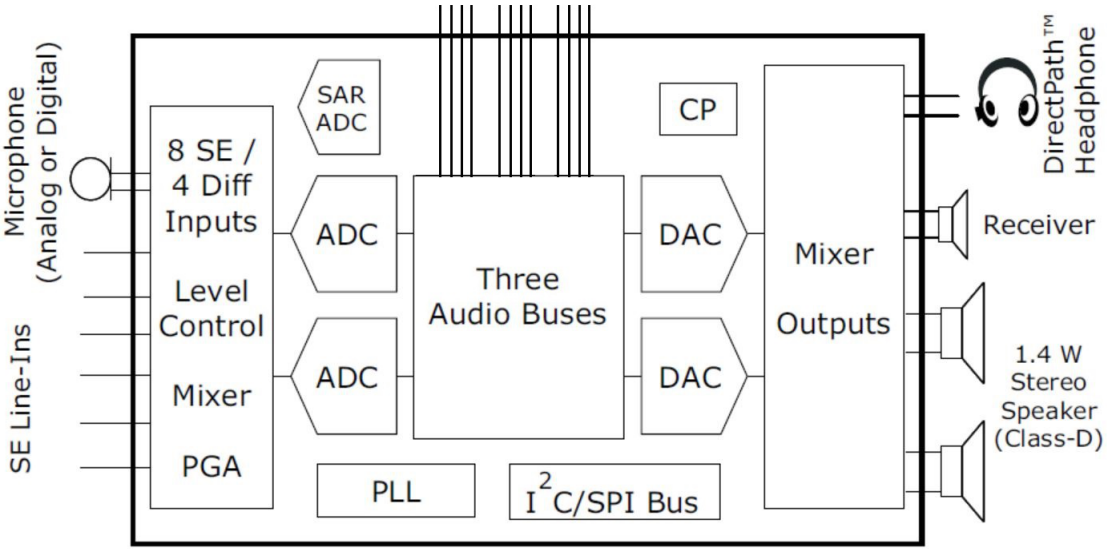
The TLV320AIC3212 (also referred to as the AIC3212) device is a flexible, highly-integrated, low-power, low-voltage stereo audio codec. The AIC3212 features digital microphone inputs and programmable outputs, PowerTune capabilities, selectable audio-processing blocks, predefined and parameterizable signal processing blocks, integrated PLL, and flexible audio interfaces. Extensive register-based control of power, input and output channel configuration, gains, effects, pin-multiplexing and clocks are included, allowing the device to be precisely targeted to its application.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV320AIC3212	DSBGA (81)	4.81 mm × 4.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2012) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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5 Description (continued)

Combined with the advanced PowerTune technology, the device can execute operations from 8-kHz mono voice playback to stereo 192-kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC3212 covers operations from 8-kHz mono to 192-kHz stereo recording, and contains programmable input channel configurations which cover single-ended and differential setups, as well as floating or mixing input signals. It also provides a digitally-controlled stereo microphone preamplifier and integrated microphone bias. One application of the digital signal processing blocks is removable of audible noise that may be introduced by mechanical coupling, for example, optical zooming in a digital camera. The record path can also be configured as a stereo digital microphone Pulse Density Modulation (PDM) interface typically used at 64 Fs or 128 Fs.

The playback path offers signal processing blocks for filtering and effects; headphone, line, receiver, and Class-D speaker outputs; flexible mixing of DAC; and analog input signals as well as programmable volume controls. The playback path contains two high-power DirectPath headphone output drivers which eliminate the need for ac coupling capacitors. A built in charge pump generates the negative supply for the ground centered headphone drivers. These headphone output drivers can be configured in multiple ways, including stereo, and mono BTL. In addition, playback audio can be routed to integrated stereo Class-D speaker drivers or a differential receiver amplifier.

The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern while lowest possible noise is important. With PowerTune the TLV320AIC3212 can address both cases.

The required internal clock of the TLV320AIC3212 can be derived from multiple sources, including the MCLK1 pin, the MCLK2 pin, the BCLK1 pin, the BCLK2 pin, several general purpose I/O pins or the output of the internal PLL, where the input to the PLL again can be derived from similar pins. Although using the internal fractional PLL ensures the availability of a suitable clock signal, TI does not recommend this for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512 kHz to 50 MHz. To enable even lower clock frequencies, an integrated low-frequency clock multiplier can also be used as an input to the PLL.

The TLV320AIC3212 has a 12-bit SAR ADC converter that supports system voltage measurements. These system voltage measurements can be sourced from three dedicated analog inputs (IN1L/AUX1, IN1R/AUX2, or VBAT pins), or, alternatively, an on-chip temperature sensor that can be read by the SAR ADC.

The TLV320AIC3212 also features three full Digital Audio Serial Interfaces, each supporting I2S, DSP/TDM, RJF, LJF, and mono PCM formats. This enables the digital playback (DAC) and record (ADC) paths to select from three independent digital audio buses or chips.

The device is available in the 4.81 mm × 4.81 mm × 0.625 mm 81-Ball WCSP (YZF) package.

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6 Device Comparison Table

PARAMETRICS	TLV320AIC3212	TLV320AIC3262	TLV320AIC3268	TLV320AIC3204	TLV320AIC3254
DACs (number)	2	2	2	2	2
ADCs (number)	2	2	2	2	2
Number of Inputs / Number of Outputs	8/7	8/7	8/7	6/4	6/4
Resolution (Bits)	16, 20, 24, 32	16, 20, 24, 32	16, 20, 24, 32	16, 20, 24, 32	16, 20, 24, 32
Control Interface	I2C, SPI	I2C, SPI	I2C, SPI	I2C, SPI	I2C, SPI
Digital Audio Interface	I2S, TDM, DSP, L&R, PCM	I2S, TDM, DSP, L&R, PCM	I2S, TDM, DSP, L&R, PCM	I2S, TDM, DSP, L&R	I2S, TDM, DSP, L&R
Number of of Digital Audio Interfaces	3	3	3	1	1
Speaker Amplifier Type	Class-D	Class-D	Class-D	—	—
Configurable miniDSP	No	Yes	Yes	No	Yes
Headphone Driver	Yes	Yes	Yes	Yes	Yes

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7 Pin Configuration and Functions

YZF Package
81-Pin DSBGA
Top View

	9	8	7	6	5	4	3	2	1
J	DVDD	GPIO1	DOUT3	DOUT2	GPI1	IOVSS	DVDD	WCLK1	DIN1
H	IOVDD	GPIO2	BCLK3	GPO1	SDA	SCL	IOVDD	DOUT1	BCLK1
G	MCLK2	$\overline{\text{RESET}}$	SPI_SELECT	DIN3	WCLK3	WCLK2	DIN2	BCLK2	MCLK1
F	VBAT	IOVSS	GPI4	GPI2	GPI3	DVSS	AVDD_18	IN2R	IN2L
E	SPKRP	SPK_V	DVSS	AVSS2	AVSS3	AVSS1	AVSS	IN3L	IN3R
D	SRVDD	SRVSS	LOR	HPVSS _SENSE	IN4R	IN1R/AUX2	IN1L/AUX1	VREF_SAR	VREF _AUDIO
C	SPKRM	SPKLM	AVDD4_18	LOL	AVDD2_18	MICBIAS	MICBIAS _EXT	AVDD1_18	IN4L
B	SLVSS	SLVDD	CPFCP	CPVSS	HPL	HVDD_18	RECM	RECP	MICDET
A	SPKLP	AVSS4	CPVDD_18	CPFCM	VNEG	HPR	RECVDD_33	RECVSS	AVDD3_33

P0044-07

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	AVDD3_33	P	3.3-V Power Supply for Micbias
A2	RECVSS	P	Receiver Driver Ground
A3	RECVDD_33	P	3.3-V Power Supply for Receiver Driver
A4	HPR	O	Right Headphone Output
A5	VNEG	I/O	Charge Pump Negative Supply
A6	CPFCM	I/O	Charge Pump Flying Capacitor M terminal
A7	CPVDD_18	P	Power Supply Input for Charge Pump

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
A8	AVSS4	P	Analog Ground for Class-D
A9	SPKLP	O	Left Channel P side Class-D Output
B1	MICDET	I/O	Headset Detection Pin
B2	RECP	O	Receiver Driver P side Output
B3	RECM	O	Receiver Driver M side Output
B4	HVDD_18	P	Headphone Amp Power Supply
B5	HPL	O	Left Headphone Output
B6	CPVSS	P	Charge Pump Ground
B7	CPFCP	I/O	Charge Pump Flying Capacitor P Terminal
B8	SLVDD	P	Left Channel Class-D Output Stage Power Supply
B9	SLVSS	P	Left Channel Class-D Output Stage Ground
C1	IN4L	I	Analog Input 4 Left
C2	AVDD1_18	P	1.8-V Analog Power Supply
C3	MICBIAS_EXT	O	Output Bias Voltage for Headset Microphone.
C4	MICBIAS	O	Output Bias Voltage for Microphone to be used for on-board Microphones
C5	AVDD2_18	P	1.8-V Analog Power Supply
C6	LOL	O	Left Line Output
C7	AVDD4_18	P	1.8-V Analog Power Supply for Class-D
C8	SPKLM	O	Left Channel M side Class-D Output
C9	SPKRM	O	Right Channel M side Class-D Output
D1	VREF_AUDIO	O	Analog Reference Filter Output
D2	VREF_SAR	I/O	SAR ADC Voltage Reference Input or Internal SAR ADC Voltage Reference Bypass Capacitor Pin
D3	IN1L/AUX1	I	Analog Input 1 Left, Auxiliary 1 Input to SAR ADC (Special Function: Left Channel High Impedance Input for Capacitive Sensor Measurement)
D4	IN1R/AUX2	I	Analog Input 1 Right, Auxiliary 2 Input to SAR ADC (Special Function: Right Channel High Impedance Input for Capacitive Sensor Measurement)
D5	IN4R	I	Analog Input 4 Right
D6	HPVSS_SENSE	I	Headphone Ground Sense Terminal
D7	LOR	O	Right Line Output
D8	SRVSS	P	Right Channel Class-D Output Stage Ground
D9	SRVDD	P	Right Channel Class-D Output Stage Power Supply
E1	IN3R	I	Analog Input 3 Right
E2	IN3L	I	Analog Input 3 Left
E3	AVSS	P	Analog Ground
E4	AVSS1	P	Analog Ground
E5	AVSS3	P	Analog Ground
E6	AVSS2	P	Analog Ground
E7	DVSS	P	Digital Ground
E8	SPK_V	P	Class-D Output Stage Power Supply (Connect to SRVDD through a Resistor)
E9	SPKRP	O	Right Channel P side Class-D Output
F1	IN2L	I	Analog Input 2 Left
F2	IN2R	I	Analog Input 2 Right
F3	AVDD_18	P	1.8-V Analog Power Supply
F4	DVSS	P	Digital Ground

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
F5	GPI3	I	Multi Function Digital Input 3 Primary: (SPI_SELECT = 1) ADC Bit Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Word Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) Secondary: (SPI_SELECT = 0) I^2C Address Bit 1 (I2C_ADDR0, LSB)
F6	GPI2	I	Multi Function Digital Input 2 Primary: General Purpose Input Secondary: Audio Serial Data Bus 1 Data Input Digital Microphone Data Input General Clock Input Low-Frequency Clock Input ADC Word Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Bit Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface)
F7	GPI4	I	Multi Function Digital Input 4 Primary: (SPI_SELECT = 1) ADC Bit Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Word Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) Secondary: (SPI_SELECT = 0) I^2C Address Bit 2 (I2C_ADDR1, MSB)
F8	IOVSS	P	Digital I/O Buffer Ground
F9	VBAT	I	Battery Monitor Voltage Input
G1	MCLK1	I	Master Clock Input 1
G2	BCLK2	I/O	Primary: Audio Serial Data Bus 2 Bit Clock Secondary: General Purpose Input General Purpose Output General CLKOUT Output ADC MOD Clock Output SAR ADC Interrupt INT1 Output INT2 Output General Clock Input Low-Frequency Clock Input
G3	DIN2	I	Primary: Audio Serial Data Bus 2 Data Input Secondary: Digital Microphone Data Input General Purpose Input Low-Frequency Clock Input
G4	WCLK2	I/O	Primary: Audio Serial Data Bus 2 Word Clock Secondary: General Purpose Input General Purpose Output CLKOUT Output ADC MOD Clock Output SAR ADC Interrupt INT1 Output INT2 Output Low-Frequency Clock Input

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
G5	WCLK3	I/O	Primary: Audio Serial Data Bus 3 Word Clock Secondary: General Purpose Output General Purpose Input Low-Frequency Clock Input
G6	DIN3	I	Audio Serial Data Bus 3 Data Input
G7	SPI_SELECT	I	Control Interface Select SPI_SELECT = 1: SPI Interface selected SPI_SELECT = 0: I^2C Interface selected
G8	RESET	I	Active Low Reset
G9	MCLK2	I	Master Clock 2 Primary: Clock Input Secondary: Digital Microphone Data Input Low-Frequency Clock Input
H1	BCLK1	I/O	Primary: Audio Serial Data Bus 1 Bit Clock Secondary: General Clock Input
H2	DOUT1	O	Primary: Audio Serial Data Bus 1 Data Output Secondary: General Purpose Output CLKOUT Output SAR ADC Interrupt INT1 Output INT2 Output
H3	IOVDD	P	Digital I/O Buffer Supply
H4	SCL	I/O	I^2C Interface Serial Clock (SPI_SELECT = 0) SPI interface mode chip-select signal (SPI_SELECT = 1)
H5	SDA	I/O	I^2C interface mode serial data input (SPI_SELECT = 0) SPI interface mode serial data input (SPI_SELECT = 1)
H6	GPO1	O	Multifunction Digital Output 1 Primary: (SPI_SELECT = 1) Serial Data Output Secondary: (SPI_SELECT = 0) General Purpose Output CLKOUT Output ADC MOD Clock Output SAR ADC Interrupt INT1 Output INT2 Output
H7	BCLK3	I/O	Primary: Audio Serial Data Bus 3 Bit Clock Secondary: General Purpose Input General Purpose Output Low-Frequency Clock Input

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
H8	GPIO2	I/O	Multi Function Digital IO 2 Outputs: General Purpose Output ADC MOD Clock Output For Digital Microphone CLKOUT Output SAR ADC Interrupt INT1 Output INT2 Output Audio Serial Data Bus 1 Bit Clock Output ADC Word Clock Output for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Bit Clock Output for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) Inputs: General Purpose Input Digital Microphone Data Input Audio Serial Data Bus 1 Bit Clock Input General Clock Input Low-Frequency Clock Input ADC Word Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Bit Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface)
H9	IOVDD	P	Digital I/O Buffer Supply
J1	DIN1	I	Primary: Audio Serial Data Bus 1 Data Input Secondary: General Clock Input Digital Microphone Data Input
J2	WCLK1	I/O	Primary: Audio Serial Data Bus 1 Word Clock Secondary: Low-Frequency Clock Input General CLKOUT Output
J3	DVDD	P	1.8V Digital Power Supply
J4	IOVSS	P	Digital I/O Buffer Ground
J5	GPI1	I	Multifunction Digital Input 1 Primary: (SPI_SELECT = 1) SPI Serial Clock Secondary: (SPI_SELECT = 0) Digital Microphone Data Input General Clock Input Low-Frequency Clock Input General Purpose Input ADC Word Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Bit Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface)
J6	DOUT2	O	Primary: Audio Serial Data Bus 2 Data Output Secondary: General Purpose Output ADC MOD Clock Output SAR ADC Interrupt INT1 Output INT2 Output

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
J7	DOUT3	O	Primary: Audio Serial Data Bus 3 Data Output Secondary: General Purpose Output Audio Serial Data Bus 1 Word Clock Output
J8	GPIO1	I/O	Multi Function Digital IO 1 Outputs: General Purpose Output ADC MOD Clock Output CLKOUT Output SAR ADC Interrupt INT1 Output INT2 Output Audio Serial Data Bus 1 Word Clock Output ADC Word Clock Output for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Bit Clock Output for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) Inputs: General Purpose Input Digital Microphone Data Input Audio Serial Data Bus 1 Word Clock Input General Clock Input Low-Frequency Clock Input ADC Word Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface) ADC Bit Clock Input for Audio Serial Data Bus 1, 2, or 3 (Six-Wire Audio Interface)
J9	DVDD	P	1.8V Digital Power Supply

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18 to AVSS1, AVSS2, AVSS4, AVSS respectively (2)	–0.3	2.2	V
AVDD3_33 to AVSS3 and RECVDD_33 to RECVSS	–0.3	3.9	V
DVDD to DVSS	–0.3	2.2	V
IOVDD to IOVSS	–0.3	3.9	V
HVDD_18 to AVSS	–0.3	2.2	V
CPVDD_18 to CPVSS	–0.3	2.2	V
SLVDD to SLVSS, SRVDD to SRVSS, SPK_V to SRVSS (3)	–0.3	6	V
Digital input voltage to ground	IOVSS – 0.3	IOVDD + 0.3	V
Analog input voltage to ground	AVSS – 0.3	AVDDx_18 + 0.3	V
VBAT	–0.3	6	V
Operating temperature	–40	85	°C
Junction temperature (T_J Max)		105	°C
Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) TI recommends to keep all AVDDx_18 supplies within ± 50 mV of each other.
(3) TI recommends to keep SLVDD, SRVDD, and SPK_V supplies within ± 50 mV of each other.

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8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2400	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18	Power supply voltage range	Referenced to AVSS1, AVSS2, AVSS4, AVSS respectively[1] TI recommends connecting each of these supplies to a single supply rail.		1.5	1.8	1.95	V
AVDD3_33 , RECVDD_33		Referenced to AVSS3 and RECVSS respectively		1.65[2]	3.3	3.6	
IOVDD		Referenced to IOVSS[1]		1.1		3.6	
DVDD[3]		Referenced to DVSS[1]			1.8	1.95	
CPVDD_18	Power supply voltage range	Referenced to CPVSS [1]		1.26	1.8	1.95	V
HVDD_18		Referenced to AVSS[1]	Ground-centered configuration	1.5[2]	1.8	1.95	
			Unipolar configuration	1.65[2]		3.6	
SLVDD[1]	Power supply voltage range	Referenced to SLVSS[1]		2.7		5.5	V
SRVDD[1]	Power supply voltage range	Referenced to SRVSS[1]		2.7		5.5	V
SPK_V[1]	Power supply voltage range	Referenced to SRVSS[1]		2.7		5.5	V
VREF_SAR	External voltage reference for SAR	Referenced to AVSS			1.8	AVDDx_18	V
	PLL input frequency[4]	Clock divider uses fractional divide (D > 0), P=1, PLL_CLKIN_DIV=1, DVDD ≥ 1.65V (Refer to table in SLAU360, *Maximum TLV320AIC3212 Clock Frequencies*)		10		20	MHz
		Clock divider uses integer divide (D = 0), P=1, PLL_CLKIN_DIV=1, DVDD ≥ 1.65V (Refer to table in SLAU360, *Maximum TLV320AIC3212 Clock Frequencies*)		0.512		20	MHz
MCLK	Master clock frequency	MCLK; Master Clock Frequency; IOVDD ≥ 1.65V				50	MHz
		MCLK; Master Clock Frequency; IOVDD ≥ 1.1V				33	
SCL	SCL clock frequency					400	kHz
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration		14.4	16		Ω
SPKLP-SPKLM, SPKRP-SPKRM	Speaker output load resistance	Differential		7.2	8		Ω
RECP-RECM	Receiver output resistance	Differential		24.4	32		Ω
C_{IN}	Charge pump input capacitor (CPVDD to CPVSS terminals)				10		µF
C_O	Charge pump output capacitor (VNEG terminal)	Type X7R			2.2		µF

(1) All grounds on board are tied together, so they should not differ in voltage by more than 0.1 V max, for any combination of ground signals. AVDDx_18 are within ±0.05 V of each other. SLVDD, SRVDD, and SPK_V are within ±0.05 V of each other.
(2) Minimum voltage for HVDD_18 and RECVDD_33 should be greater than or equal to AVDD2_18. Minimum voltage for AVDD3_33 should be greater than or equal to AVDD1_18 and AVDD2_18.
(3) At DVDD values lower than 1.65 V, the PLL does not function. Please see table in SLAU360, *Maximum TLV320AIC3212 Clock Frequencies* for details on maximum clock frequencies.
(4) The PLL Input Frequency refers to clock frequency after PLL_CLKIN_DIV divider. Frequencies higher than 20 MHz can be sent as an input to this PLL_CLKIN_DIV and reduced in frequency prior to input to the PLL.

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Recommended Operating Conditions (continued)

			MIN	NOM	MAX	UNIT
C_F	Charge pump flying capacitor (CPFCP to CPFCM terminals)	Type X7R		2.2		µF
TOPR	Operating temperature range		–40		85	°C

8.4 Thermal Information

THERMAL METRIC[1]		TLV320AIC3212 YZF (DSBGA) 81 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics, SAR ADC

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; fS (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAR ADC INPUTS						
Analog Input	Input voltage range	IN1L/AUX1 or IN1R/AUX2 Selected	0		VREF_SAR	V
	Input impedance			$1 \div (f \times C_{SAR_IN})$ (1)		kΩ
	Input capacitance, C_{SAR_IN}			25		pF
	Input leakage current			1		µA
Battery Input	VBAT Input voltage range	VBAT (Battery measurement) selected	2.2		5.5	V
	VBAT Input impedance			5		kΩ
	VBAT Input capacitance			25		pF
	VBAT Input leakage current			1		µA
SAR ADC CONVERSION						
	Resolution	Programmable: 8-bit, 10-bit, 12-bit	8		12	Bits
	No missing codes	12-bit resolution		11		Bits
IN1L/ AUX1	Integral linearity	12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, External Reference = 1.8V (2)		±1		LSB
	Offset error			±1		LSB
	Gain error			0.07%		
	Noise	DC voltage applied to IN1L/AUX1 = 1 V, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, External Reference = 1.8V (3)(2)		±1		LSB
VBAT	Accuracy	12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, Internal Reference = 1.25V		2%		
	Offset error			±2		LSB
	Gain error			1.5%		
	Noise	DC voltage applied to VBAT = 3.6 V, 12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, Internal Reference = 1.25V		±0.5		LSB
CONVERSION RATE						
	Normal conversion operation	12-bit resolution, SAR ADC clock = 12 MHz External Clock, Conversion clock = External Clock / 4, External Reference = 1.8V (2). With Fast SPI reading of data.			119	kHz
	High-speed conversion operation	8-bit resolution,SAR ADC clock = 12 MHz External Clock, Internal Conversion clock = External Clock (Conversion accuracy is reduced.), External Reference = 1.8V (2). With Fast SPI reading of data.			250	kHz
VOLTAGE REFERENCE - VREF_SAR						
	Voltage range	Internal VREF_SAR		1.25±0.05		V
		External VREF_SAR	1.25		AVDDx_18	V
	Reference Noise	CM=0.9V, C_{ref} = 1µF		32		μV_{RMS}
	Decoupling Capacitor			1		µF

(1) SAR input impedance is dependent on the sampling frequency (f designated in Hz), and the sampling capacitor is C_{SAR_IN} = 25 pF.
(2) When using External SAR reference, this external reference must be restricted $V_{EXT_SAR_REF} \leq$ AVDD_18 and AVDD2_18.
(3) Noise from external reference voltage is excluded from this measurement.

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8.6 Electrical Characteristics, ADC

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; fS (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC (CM = 0.9 V)						
	Input signal level (0dB)	Single-ended, CM = 0.9 V		0.5		V_{RMS}
	Device Setup	1-kHz sine wave input, Single-ended Configuration IN2R to Right ADC and IN2L to Left ADC, R_{in} = 20 kΩ, f_s = 48 kHz, AOSR = 128, MCLK = 256*f_s, PLL Disabled; AGC = OFF, Channel Gain = 0 dB, Processing Block = PRB_R1, Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Inputs AC-shorted to ground	85	93		dB
		IN1R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and AC-shorted to ground IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and AC-shorted to ground		93		
DR	Dynamic range A-weighted(1) (2)	–60dB full-scale, 1-kHz input signal		93		dB
THD+N	Total Harmonic Distortion plus Noise	–3 dB full-scale, 1-kHz input signal		–87	–70	dB
		IN1R,IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC –3-dB full-scale, 1-kHz input signal		–87		
	Gain Error	1kHz sine wave input at -3dBFS, Single-ended configuration R_{in} = 20 K f_s = 48 kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled AGC = OFF, Channel Gain=0 dB, Processing Block = PRB_R1, Power Tune = PTM_R4, CM=0.9 V		0.1		dB
	Input Channel Separation	1kHz sine wave input at –3 dBFS, Single-ended configuration IN1L routed to Left ADC, IN1R routed to Right ADC, R_{in} = 20 K AGC = OFF, AOSR = 128, Channel Gain=0 dB, CM=0.9 V		110		dB
	Input Pin Crosstalk	1-kHz sine wave input at –3 dBFS on IN2L, IN2L internally not routed. IN1L routed to Left ADC, AC-coupled to ground 1-kHz sine wave input at –3 dBFS on IN2R, IN2R internally not routed. IN1R routed to Right ADC, AC-coupled to ground Single-ended configuration R_{in} = 20 kΩ, AOSR=128 Channel Gain=0 dB, CM=0.9 V		116		dB
	PSRR	217Hz, 100mVpp signal on AVDD_18, AVDDx_18 Single-ended configuration, Rin=20 kΩ, Channel Gain=0 dB; CM=0.9 V		59		dB
AUDIO ADC (CM = 0.75 V)						
	Input signal level (0dB)	Single-ended, CM=0.75 V, AVDD_18, AVDDx_18 = 1.5 V		0.375		V_{RMS}
	Device Setup	1-kHz sine wave input, Single-ended Configuration IN2R to Right ADC and IN2L to Left ADC, R_{in} = 20 K, f_s = 48 kHz, AOSR = 128, MCLK = 256*f_s, PLL Disabled; AGC = OFF, Channel Gain = 0 dB, Processing Block = PRB_R1, Power Tune = PTM_R4				

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with pre-analyzer 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

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Electrical Characteristics, ADC (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; fS (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio, A-weighted (1) (2)	Inputs AC-shorted to ground		91		dB
		IN1R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and AC-shorted to ground IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and AC-shorted to ground		91		dB
DR	Dynamic range A-weighted (1) (2)	–60-dB full-scale, 1-kHz input signal		91		dB
THD+N	Total Harmonic Distortion plus Noise	–3-dB full-scale, 1-kHz input signal		–85		dB
AUDIO ADC (Differential Input, CM = 0.9 V)						
	Input signal level (0dB)	Differential, CM=0.9 V, AVDD_18, AVDDx_18 = 1.8 V		1		V_{RMS}
	Device Setup	1-kHz sine wave input, Differential Configuration IN1L, IN1R Routed to Right ADC, IN2L, IN2R Routed to Left ADC R_{in} = 20 kΩ, f_s = 48 kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled, AGC = OFF, Channel Gain = 0 dB, Processing Block = PRB_R1, Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted (1) (2)	Inputs AC-shorted to ground		94		dB
DR	Dynamic range A-weighted (1) (2)	–60-dB full-scale, 1-kHz input signal		94		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–88		dB
	Gain Error	1-kHz sine wave input at –3 dBFS, Differential configuration R_{in} = 20 kΩ, f_s = 48 kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled AGC = OFF, Channel Gain=0 dB, Processing Block = PRB_R1, Power Tune = PTM_R4, CM=0.9 V		0.1		dB
	Input Channel Separation	1kHz sine wave input at –3 dBFS, Differential configuration IN1L/IN1R differential signal routed to Right ADC, IN2L/IN2R differential signal routed to Left ADC, R_{in} = 20 kΩ AGC = OFF, AOSR = 128, Channel Gain=0 dB, CM=0.9 V		107		dB
	Input Pin Crosstalk	1-kHz sine wave input at –3 dBFS on IN2L/IN2R, IN2L/IN2R internally not routed. IN1L/IN1R differentially routed to Right ADC, AC-coupled to ground 1-kHz sine wave input at –3 dBFS on IN2L/IN2R, IN2L/IN2R internally not routed. IN3L/IN3R differentially routed to Left ADC, AC-coupled to ground Differential configuration R_{in} = 20 kΩ, AOSR=128 Channel Gain=0 dB, CM=0.9 V		109		dB
	PSRR	217 Hz, 100 mVpp signal on AVDD_18, AVDDx_18 Differential configuration, Rin=20 K, Channel Gain=0 dB; CM=0.9 V		59		dB
AUDIO ADC						
	ADC programmable gain amplifier gain	IN1 - IN3, Single-Ended, Rin = 10 K, PGA gain set to 0 dB		0		dB
		IN1 - IN3, Single-Ended, Rin = 10 K, PGA gain set to 47.5 dB		47.5		dB
		IN1 - IN3, Single-Ended, Rin = 20 K, PGA gain set to 0 dB		–6		dB
		IN1 - IN3, Single-Ended, Rin = 20 K, PGA gain set to 47.5 dB		41.5		dB
		IN1 - IN3, Single-Ended, Rin = 40 K, PGA gain set to 0 dB		–12		dB
		IN1 - IN3, Single-Ended, Rin = 40 K, PGA gain set to 47.5 dB		35.5		dB
		IN4, Single-Ended, Rin = 20 K, PGA gain set to 0 dB		–6		dB
		IN4, Single-Ended, Rin = 20 K, PGA gain set to 47.5 dB		41.5		dB
	ADC programmable gain amplifier step size	1-kHz tone		0.5		dB

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8.7 Electrical Characteristics, Bypass Outputs

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO RECEIVER AMPLIFIER, DIRECT MODE						
	Device Setup	Load = 32Ω (differential), 56pF; Input CM=0.9V; Output CM=1.65V; IN1L routed to RECP and IN1R routed to RECM; Channel Gain=0dB				
	Full scale differential input voltage (0dB)			1		V_{RMS}
	Gain Error	707mVrms (-3dBFS), 1-kHz input signal		0.5		dB
	Noise, A-weighted(1)	Idle Channel, IN1L and IN1R ac-shorted to ground		13		μV_{RMS}
THD+N	Total Harmonic Distortion plus Noise	707mVrms (-3dBFS), 1-kHz input signal		–88		dB
ANALOG BYPASS TO HEADPHONE AMPLIFIER, PGA MODE						
	Device Setup	Load = 16 Ω (single-ended), 56 pF; HVDD_18 = 3.3 V Input CM=0.9 V; Output CM=1.65 V IN1L routed to ADCPGA_L, ADCPGA_L routed through MAL to HPL; and IN1R routed to ADCPGA_R, ADCPGA_R routed through MAR to HPR; R_{in} = 20 K; Channel Gain = 0 dB				
	Full scale input voltage (0 dB)			0.5		V_{RMS}
	Gain Error	446 mVrms (–1dBFS), 1-kHz input signal		–1.2		dB
	Noise, A-weighted(1)	Idle Channel, IN1L and IN1R AC-shorted to ground		6		μV_{RMS}
THD+N	Total Harmonic Distortion plus Noise	446 mVrms (–1dBFS), 1-kHz input signal		–81		dB
ANALOG BYPASS TO HEADPHONE AMPLIFIER (GROUND-CENTERED CIRCUIT CONFIGURATION), PGA MODE						
	Device Setup	Load = 16 Ω (single-ended), 56 pF; Input CM=0.9 V; IN1L routed to ADCPGA_L, ADCPGA_L routed through MAL to HPL; and IN1R routed to ADCPGA_R, ADCPGA_R routed through MAR to HPR; R_{in} = 20 K; Channel Gain = 0 dB				
	Full scale input voltage (0dB)			0.5		V_{RMS}
	Gain Error	446 mVrms (-1dBFS), 1-kHz input signal		–1		dB
	Noise, A-weighted(1)	Idle Channel, IN1L and IN1R ac-shorted to ground		11		μV_{RMS}
THD+N	Total Harmonic Distortion plus Noise	446mVrms (-1dBFS), 1-kHz input signal		–67		dB
ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE						
	Device Setup	Load = 10KOhm (single-ended), 56pF; Input and Output CM=0.9V; IN1L routed to ADCPGA_L and IN1R routed to ADCPGA_R; Rin = 20k ADCPGA_L routed through MAL to LOL and ADCPGA_R routed through MAR to LOR; Channel Gain = 0dB				
	Full scale input voltage (0dB)			0.5		V_{RMS}
	Gain Error	446mVrms (-1dBFS), 1-kHz input signal		–0.7		dB

(1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

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Electrical Characteristics, Bypass Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Noise, A-weighted(1)	Idle Channel, IN1L and IN1R ac-shorted to ground		6		μV_{RMS}
	Channel Gain=40dB, Inputs ac-shorted to ground, Input Referred		3		μV_{RMS}
ANALOG BYPASS TO LINE-OUT AMPLIFIER, DIRECT MODE					
Device Setup	Load = 10 kΩ (single-ended), 56 pF; Input and Output CM=0.9 V; IN1L routed to LOL and IN1R routed to LOR; Channel Gain = 0 dB				
Full scale input voltage (0dB)			0.5		V_{RMS}
Gain Error	446mVrms (-1dBFS), 1-kHz input signal		–0.3		dB
Noise, A-weighted(1)	Idle Channel, IN1L and IN1R AC-shorted to ground		3		μV_{RMS}

8.8 Electrical Characteristics, Microphone Interface

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS (MICBIAS or MICBIAS_EXT)					
Bias voltage	CM=0.9V, AVDD3_33 = 1.8 V				
	Micbias Mode 0		1.63		V
	Micbias Mode 3		AVDD3_33		V
	CM=0.75V, AVDD3_33 = 1.8 V				
	Micbias Mode 0		1.36		V
	Micbias Mode 3		AVDD3_33		V
MICROPHONE BIAS (MICBIAS or MICBIAS_EXT)					
Bias voltage	CM=0.9 V, AVDD3_33 = 3.3 V				
	Micbias Mode 0		1.63		V
	Micbias Mode 1		2.36		V
	Micbias Mode 2		2.91		V
	Micbias Mode 3		AVDD3_33		V
	CM=0.75 V, AVDD3_33 = 3.3 V				
	Micbias Mode 0		1.36		V
	Micbias Mode 1		1.97		V
	Micbias Mode 2		2.42		V
	Micbias Mode 3		AVDD3_33		V
Output Noise	CM=0.9V, Micbias Mode 2, A-weighted, 20-Hz to 20-kHz bandwidth, Current load = 0 mA.		26		μV_{RMS}
			184		nV/√Hz
Current Sourcing	Micbias Mode 0 (CM=0.9V)(1)		3		mA
	Micbias Mode 1 or Micbias Mode 2 (CM=0.9 V)(2)		7		mA
Inline Resistance	Micbias Mode 3		63.6		Ω

(1) To provide 3 mA, Micbias Mode 0 voltage yields typical voltage of 1.60 V for Common Mode of 0.9 V.
(2) To provide 7 mA, Micbias Mode 1 voltage yields typical voltage of 2.31 V, and Micbias Mode 2 voltage yields typical voltage of 2.86 V for Common Mode of 0.9 V.

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8.9 Electrical Characteristics, Audio DAC Outputs

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT						
	Device Setup	Load = 10 kΩ (single-ended), 56 pF Input & Output CM=0.9 V DOSR = 128, MCLK=256* f_s, Channel Gain = 0 dB, Processing Block = PRB_P1, Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input	85	101		dB
DR	Dynamic range, A-weighted (1) (2)	–60-dB 1-kHz input full-scale signal, Word length=20 bits		101		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–88		dB
	DAC Gain Error	–3dB full-scale, 1-kHz input signal		0.1		dB
	DAC Mute Attenuation	Mute		119		dB
	DAC channel separation	–1 dB, 1kHz signal, between left and right Line out		108		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVDD_18, AVDDx_18		71		dB
		100mVpp, 217Hz signal applied to AVDD_18, AVDDx_18		71		dB
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT						
	Device Setup	Load = 10 kΩ (single-ended), 56pF Input & Output CM=0.75V; AVDD_18, AVDDx_18, HVDD_18=1.5V DOSR = 128 MCLK=256* fs Channel Gain = 0dB Processing Block = PRB_P1 Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input		99		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1 kHz input full-scale signal, Word length=20 bits		99		dB
THD+N	Total Harmonic Distortion plus Noise	–3 dB full-scale, 1-kHz input signal		–88		dB
AUDIO DAC – MONO DIFFERENTIAL LINE OUTPUT						
	Device Setup	Load = 10 kΩ (differential), 56pF Input & Output CM=0.9V, LOL signal routed to LOR amplifier DOSR = 128, MCLK=256* f_s, Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P4				
	Full scale output voltage (0dB)			1		V_{RMS}
SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input		101		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal,		101		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–86		dB
	DAC Gain Error	–3dB full-scale, 1-kHz input signal		0.1		dB

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

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Electrical Characteristics, Audio DAC Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC Mute Attenuation	Mute		97		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVDD_18, AVDDx_18		62		dB
		100mVpp, 217Hz signal applied to AVDD_18, AVDDx_18		63		dB
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (GROUND-CENTERED CIRCUIT CONFIGURATION)						
	Device Setup	Load = 16Ω (single-ended), 56pF, Input CM=0.9V; DOSR = 128, MCLK=256* f_s, Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P3, Headphone Output Strength=100%				
Output 1	Output voltage			0.5		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (3) (4)	All zeros fed to DAC input	80	94		dB
DR	Dynamic range, A-weighted (3) (4)	–60dB 1 kHz input full-scale signal		93		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–71	–55	dB
	DAC Gain Error	–3dB, 1kHz input full scale signal		–0.2		dB
	DAC Mute Attenuation	Mute		92		dB
	DAC channel separation	–3dB, 1kHz signal, between left and right HP out		83		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVDD_18, AVDD1x_18		55		dB
		100mVpp, 217Hz signal applied to AVDD_18, AVDD1x_18		55		dB
	Power Delivered	THDN ≤ -40dB, Load = 16Ω		15		mW
Output 2	Output voltage	Load = 16Ω (single-ended), Channel Gain = 5dB		0.8		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (3) (4)	All zeros fed to DAC input, Load = 16Ω		96		dB
	Power Delivered	THDN ≤ -40dB, Load = 16Ω		24		mW
Output 3	Output voltage	Load = 32Ω (single-ended), Channel Gain = 5dB		0.9		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (3) (4)	All zeros fed to DAC input, Load = 32Ω		97		dB
	Power Delivered	THDN ≤ -40dB, Load = 32Ω		22		mW
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (UNIPOLAR CIRCUIT CONFIGURATION)						
	Device Setup	Load = 16Ω (single-ended), 56pF Input & Output CM=0.9V, DOSR = 128, MCLK=256* f_s, Channel Gain=0dB Processing Block = PRB_P1 Power Tune = PTM_P4 Headphone Output Control = 100%				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (3) (4)	All zeros fed to DAC input		100		dB
DR	Dynamic range, A-weighted (3) (4)	–60dB 1kHz input full-scale signal, Power Tune = PTM_P4		100		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–79		dB
	DAC Gain Error	–3dB, 1kHz input full scale signal		–0.2		dB

(3) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(4) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

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Electrical Characteristics, Audio DAC Outputs (continued)

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC Mute Attenuation	Mute		119		dB
	DAC channel separation	–1dB, 1kHz signal, between left and right HP out		88		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVDD_18, AVDD1x_18		64		dB
		100mVpp, 217Hz signal applied to AVDD_18, AVDD1x_18		70		dB
	Power Delivered	R_L=16Ω THDN ≤ -40dB, Input CM=0.9V, Output CM=0.9V		15		mW
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (UNIPOLAR CIRCUIT CONFIGURATION)						
	Device Setup	Load = 16Ω (single-ended), 56pF, Input & Output CM=0.75V; AVDD_18, AVDDx_18, HVDD_18=1.5V, DOSR = 128, MCLK=256* f_S, Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P4 Headphone Output Control = 100%				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (3) (4)	All zeros fed to DAC input		99		dB
DR	Dynamic range, A-weighted (3) (4)	-60dB 1 kHz input full-scale signal		99		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–77		dB
AUDIO DAC – MONO DIFFERENTIAL RECEIVER OUTPUT						
	Device Setup	Load = 32 Ω (differential), 56pF, Output CM=1.65V, AVDDx_18=1.8V, DOSR = 128 MCLK=256* f_S, Left DAC routed to LOL to RECP, LOL signal routed to LOR to RECM, Channel (Receiver Driver) Gain = 6dB for full scale output signal, Processing Block = PRB_P4, Power Tune = PTM_P4				
	Full scale output voltage (0dB)			2		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (3) (4)	All zeros fed to DAC input	90	99		dB
DR	Dynamic range, A-weighted (3) (4)	–60dB 1kHz input full-scale signal		97		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–81		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVDD_18, AVDD1x_18		56		dB
		100mVpp, 217Hz signal applied to AVDD_18, AVDD1x_18		58		dB
	Power Delivered	R_L=32Ω THDN ≤ -40dB, Input CM=0.9V, Output CM=1.65V		117		mW

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8.10 Electrical Characteristics, Class-D Outputs

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC OUTPUT to CLASS-D SPEAKER OUTPUT; Load = 8Ω (Differential), 56pF+33µH							
	Output voltage	SLVDD=SRVDD=3.6, BTL measurement, DAC input = 0dBFS, class-D gain = 12dB, THD+N ≤ –20dB, CM=0.9V			2.67		V_{RMS}
SNR	Signal-to-noise ratio	SLVDD=SRVDD=3.6V, BTL measurement, class-D gain = 6dB, measured as idle-channel noise, A-weighted (with respect to full-scale output value of 2 Vrms)(1) (2), CM=0.9V			91		dB
THD	Total harmonic distortion	SLVDD=SRVDD=3.6V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V			–66		dB
THD+N	Total harmonic distortion + noise	SLVDD=SRVDD=3.6V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V			–66		dB
PSRR	Power-supply rejection ratio	SLVDD=SRVDD=3.6V, BTL measurement, ripple on SPKVDD = 200 mVp-p at 1 kHz, CM=0.9V			67		dB
		SLVDD=SRVDD=3.6V, BTL measurement, ripple on SPKVDD = 200 mVp-p at 217 Hz, CM=0.9V			67		dB
	Mute attenuation	Analog Mute Only			102		dB
P_O	Maximum output power	THD+N = 10%, f = 1 kHz, Class-D Gain = 12 dB, CM = 0.9 V, R_L = 8 Ω	SLVDD = SRVDD = 3.6 V		0.72		W
			SLVDD = SRVDD = 4.2 V		1.00		
			SLVDD = SRVDD = 5.5 V		1.70		
		THD+N = 1%, f = 1 kHz, Class-D Gain = 12 dB, CM = 0.9 V, R_L = 8 Ω	SLVDD = SRVDD = 3.6 V		0.58		
			SLVDD = SRVDD = 4.2 V		0.80		
			SLVDD = SRVDD = 5.5 V		1.37		
DAC OUTPUT to CLASS-D SPEAKER OUTPUT; Load = 8 Ω (Differential), 56pF+33µH							
	Output voltage	SLVDD=SRVDD=5.0V, BTL measurement, DAC input = 0dBFS, class-D gain = 12dB, THD+N ≤ –20dB, CM=0.9V			3.46		V_{RMS}
SNR	Signal-to-noise ratio	SLVDD=SRVDD=5.0V, BTL measurement, class-D gain = 6dB, measured as idle-channel noise, A-weighted (with respect to full-scale output value of 2 Vrms)(1) (2) , CM=0.9V			91		
THD	Total harmonic distortion	SLVDD=SRVDD=5.0V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V			–70		
THD+N	Total harmonic distortion + noise	SLVDD=SRVDD=5.0V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V			–70		
PSRR	Power-supply rejection ratio	SLVDD=SRVDD=5.0V, BTL measurement, ripple on SPKVDD = 200mVp-p at 1kHz, CM=0.9V			67		
		SLVDD=SRVDD=5.0V, BTL measurement, ripple on SPKVDD = 200 mVp-p at 217 Hz, CM=0.9V			67		
	Mute attenuation	Analog Mute Only			102		dB
P_O	Maximum output power	THD+N = 10%, f = 1 kHz, Class-D Gain = 12 dB, CM = 0.9 V, R_L = 8 Ω	SLVDD = SRVDD = 5.0 V		1.41		W

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

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8.11 Electrical Characteristics, Miscellaneous

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE - VREF_AUDIO					
Reference Voltage Settings	CMMode = 0 (0.9V)		0.9		V
	CMMode = 1 (0.75V)		0.75		
Reference Noise	CM=0.9V, A-weighted, 20Hz to 20kHz bandwidth, C_{ref} = 1µF		1.2		μV_{RMS}
Decoupling Capacitor			1		µF
Bias Current			99		µA
SHUTDOWN POWER					
Device Setup	Coarse AVdd supply turned off, All External analog supplies powered and set available, No external digital input is toggled, register values are retained.				
P(total)(1)	Sum of all supply currents, all supplies at 1.8 V except for SLVDD = SRVDD = SPK_V = 3.6 V and RECVDD_33 = AVDD3_33 = 3.3 V		9.8		µW
I(DVDD)			2.6		µA
I(IOVDD)			0.15		µA
I(AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18, HVDD_18, CPVDD_18)			1.15		µA
I(RECVDD_33, AVDD3_33)			0.15		µA
I(SLVDD, SRVDD, SPK_V)			0.5		µA

(1) For further details on playback and recording power consumption, refer to Powertune section in SLAU360.

8.12 Electrical Characteristics, Logic Levels

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDD = 1.8 V; AVDD3_33, RECVDD_33 = 3.3 V; SLVDD, SRVDD, SPK_V = 3.6 V; f S (Audio) = 48 kHz; Audio Word Length = 16 bits; Cext = 1 µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC FAMILY (CMOS)						
V_{IH}	Logic Level	I_{IH} = 5 µA, IOVDD > 1.65 V	0.7 × IOVDD			V
		I_{IH} = 5 µA, 1.2 V ≤ IOVDD <1.65 V	0.9 × IOVDD			V
		I_{IH} = 5 µA, IOVDD < 1.2 V	IOVDD			V
V_{IL}		I_{IL} = 5 µA, IOVDD > 1.65 V	–0.3		0.3 × IOVDD	V
		I_{IL} = 5 µA, 1.2 V ≤ IOVDD <1.65 V			0.1 × IOVDD	V
		I_{IL} = 5 µA, IOVDD < 1.2 V			0	V
V_{OH}		I_{OH} = 3-mA load, IOVDD > 1.65 V	0.8 × IOVDD			V
		I_{OH} = 1-mA load, IOVDD < 1.65 V	0.8 × IOVDD			V
V_{OL}		I_{OL} = 3-mA load, IOVDD > 1.65 V			0.1 × IOVDD	V
		I_{OL} = 1-mA load, IOVDD < 1.65 V			0.1 × IOVDD	V
	Capacitive Load			10		pF

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8.13 Audio Data Serial Interface Timing (I^2S): I^2S/LJF/RJF Timing in Master Mode

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface number 1, Audio Serial Interface number 2 and Audio Serial Interface number 3.

WCLK represents WCLK1 pin for Audio Serial Interface number 1, WCLK2 pin for Audio Serial Interface number 2, and WCLK3 pin for Audio Serial Interface number 3. **BCLK** represents BCLK1 pin for Audio Serial Interface number 1, BCLK2 pin for Audio Serial Interface number 2, and BCLK3 pin for Audio Serial Interface number 3. **DOUT** represents DOUT1 pin for Audio Serial Interface number 1, DOUT2 pin for Audio Serial Interface number 2, and DOUT3 pin for Audio Serial Interface number 3. **DIN** represents DIN1 pin for Audio Serial Interface number 1, DIN2 pin for Audio Serial Interface number 2, and DIN3 pin for Audio Serial Interface number 3. Specifications are at 25° C with DVDD = 1.8 V and IOVDD = 1.8 V. (See Figure 1)

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		22		20	ns
t_d (DO-WS)	WCLK to DOUT delay (For LJF Mode only)		22		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	4		4		ns
t_h(DI)	DIN hold	4		4		ns
t_r	BCLK Rise time		10		8	ns
t_f	BCLK Fall time		10		8	ns

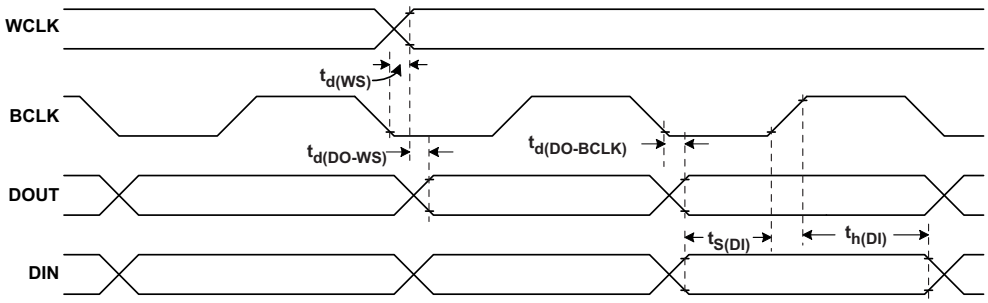


Figure 1. I^2S/LJF/RJF Timing in Master Mode

8.14 Audio Data Serial Interface Timing (I^2S): I^2S/LJF/RJF Timing in Slave Mode

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface number 1, Audio Serial Interface number 2 and Audio Serial Interface number 3.

WCLK represents WCLK1 pin for Audio Serial Interface number 1, WCLK2 pin for Audio Serial Interface number 2, and WCLK3 pin for Audio Serial Interface number 3. **BCLK** represents BCLK1 pin for Audio Serial Interface number 1, BCLK2 pin for Audio Serial Interface number 2, and BCLK3 pin for Audio Serial Interface number 3. **DOUT** represents DOUT1 pin for Audio Serial Interface number 1, DOUT2 pin for Audio Serial Interface number 2, and DOUT3 pin for Audio Serial Interface number 3. **DIN** represents DIN1 pin for Audio Serial Interface number 1, DIN2 pin for Audio Serial Interface number 2, and DIN3 pin for Audio Serial Interface number 3. Specifications are at 25° C with DVDD = 1.8 V and IOVDD = 1.8 V. (See Figure 2)

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	30		30		ns
t_L (BCLK)	BCLK low period	30		30		ns
t_s (WS)	WCLK setup	4		4		ns
t_h (WS)	WCLK hold	4		4		ns
t_d (DO-WS)	WCLK to DOUT delay (For LJF mode only)		22		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	4		4		ns
t_h(DI)	DIN hold	4		4		ns
t_r	BCLK Rise time		5		4	ns
t_f	BCLK Fall time		5		4	ns

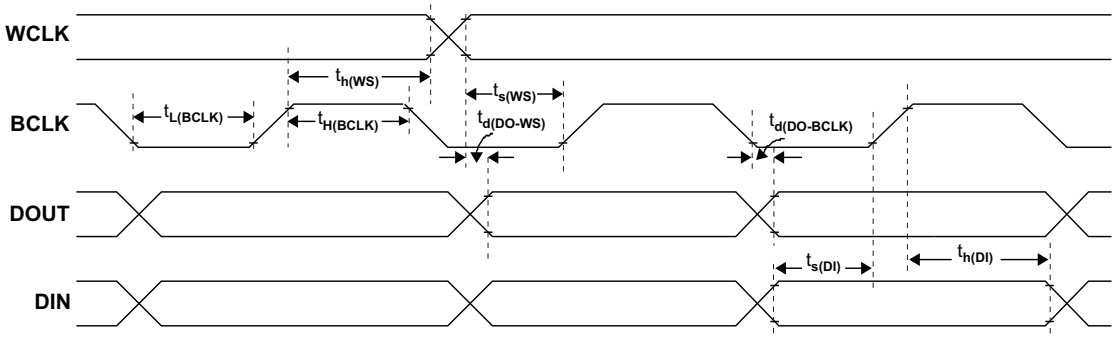


Figure 2. I^2S/LJF/RJF Timing in Slave Mode

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8.15 Typical DSP Timing: DSP/Mono PCM Timing in Master Mode

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface number 1, Audio Serial Interface number 2 and Audio Serial Interface number 3.

Specifications are at 25° C with DVDD = 1.8 V. (See Figure 3)

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d (WS)	WCLK delay		22		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	4		4		ns
t_h(DI)	DIN hold	4		4		ns
t_r	BCLK Rise time		10		8	ns
t_f	BCLK Fall time		10		8	ns

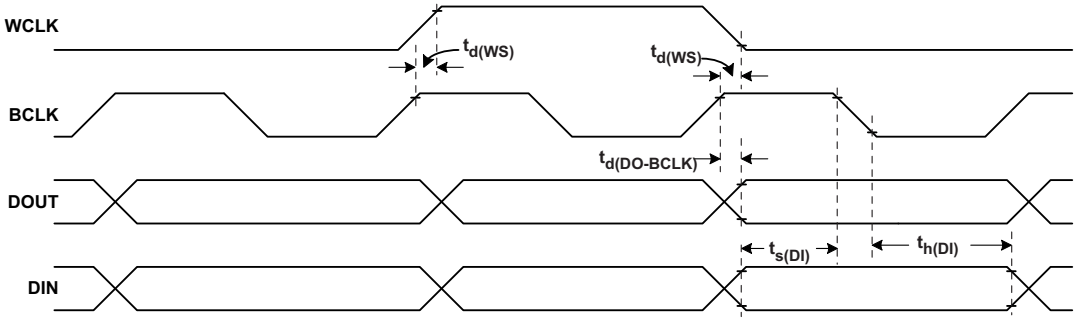


Figure 3. DSP/Mono PCM Timing in Master Mode

8.16 Typical DSP Timing: DSP/Mono PCM Timing in Slave Mode

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface number 1, Audio Serial Interface number 2 and Audio Serial Interface number 3.

Specifications are at 25° C with DVDD = 1.8 V. (See Figure 4)

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	30		30		ns
t_L (BCLK)	BCLK low period	30		30		ns
t_s(WS)	WCLK setup	4		4		ns
t_h(WS)	WCLK hold	4		4		ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	5		5		ns
t_h(DI)	DIN hold	5		5		ns
t_r	BCLK Rise time		5		4	ns
t_f	BCLK Fall time		5		4	ns

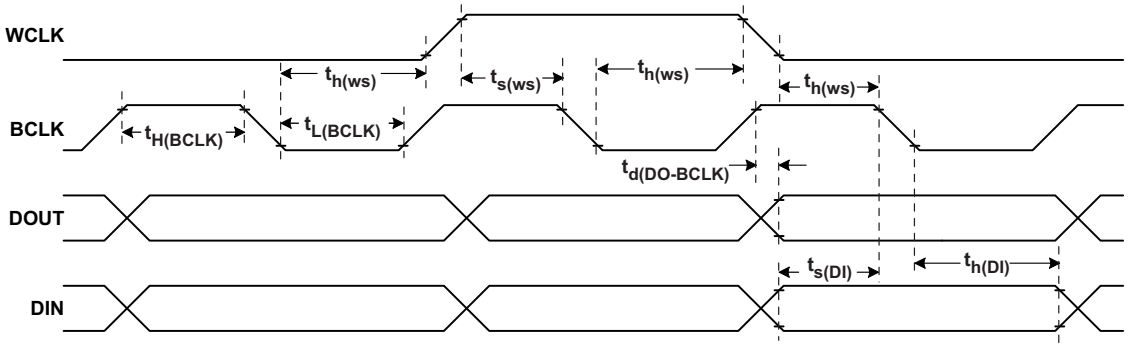


Figure 4. DSP/Mono PCM Timing in Slave Mode

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8.17 I²C Interface Timing

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface number 1, Audio Serial Interface number 2 and Audio Serial Interface number 3. (See Figure 5)

PARAMETER		STANDARD-MODE			FAST-MODE			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency	0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0			0.8			µs
t_{LOW}	LOW period of the SCL clock	4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock	4.0			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			0.8			µs
$t_{HD;DAT}$	Data hold time: For I2C bus devices	0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data set-up time	250			100			ns
t_r	SDA and SCL Rise Time			1000	20+0.1C_b		300	ns
t_f	SDA and SCL Fall Time			300	20+0.1C_b		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0			0.8			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			1.3			µs
C_b	Capacitive load for each bus line			400			400	pF

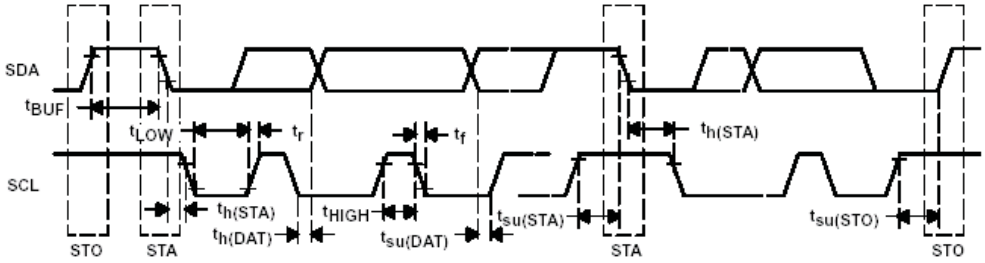


Figure 5. I²C Interface Timing Diagram

8.18 SPI Timing

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface number 1, Audio Serial Interface number 2 and Audio Serial Interface number 3.

$\overline{\textbf{SS}}$ = SCL pin, **SCLK** = GPI1 pin, **MISO** = GPO1 pin, and **MOSI** = SDA pin. Specifications are at 25° C with DVDD = 1.8 V. (See Figure 6)

PARAMETER		IOVDD=1.8 V			IOVDD=3.3 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{sck}	SCLK Period (1)	50			40			ns
t_{sckh}	SCLK Pulse width High	25			20			ns
t_{sckl}	SCLK Pulse width Low	25			20			ns
t_{lead}	Enable Lead Time	25			20			ns
t_{trail}	Enable Trail Time	25			20			ns
$t_{d;seqxfr}$	Sequential Transfer Delay	25			20			ns
t_a	Slave DOUT (MISO) access time			25			20	ns
t_{dis}	Slave DOUT (MISO) disable time			25			20	ns
t_{su}	DIN (MOSI) data setup time	8			8			ns
$t_{h;DIN}$	DIN (MOSI) data hold time	8			8			ns
$t_{v;DOUT}$	DOUT (MISO) data valid time			20			14	ns
t_r	SCLK Rise Time			4			4	ns
t_f	SCLK Fall Time			4			4	ns

(1) These parameters are based on characterization and are not tested in production.

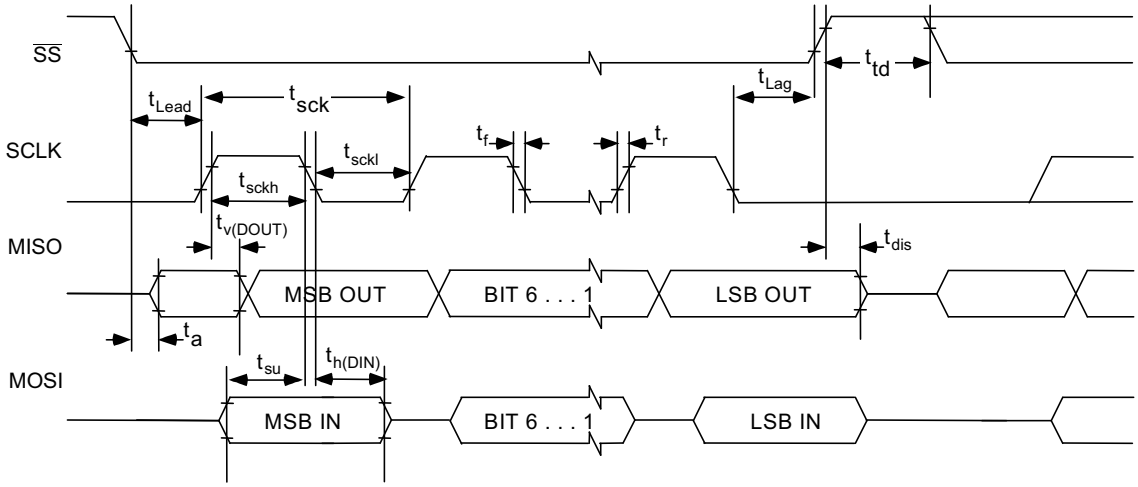


Figure 6. SPI Timing Diagram

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8.19 Typical Characteristics

8.19.1 Audio ADC Performance

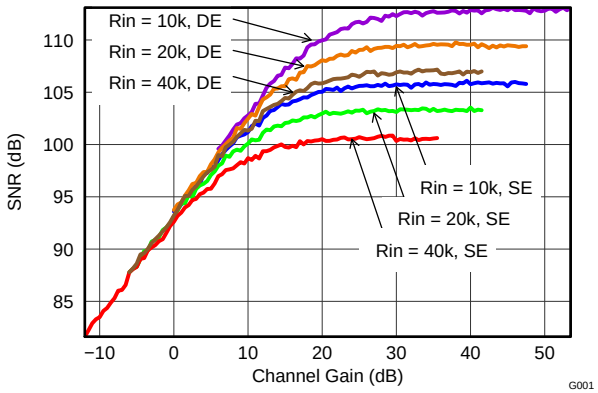


Figure 7. ADC SNR vs Channel Gain Input-Referred

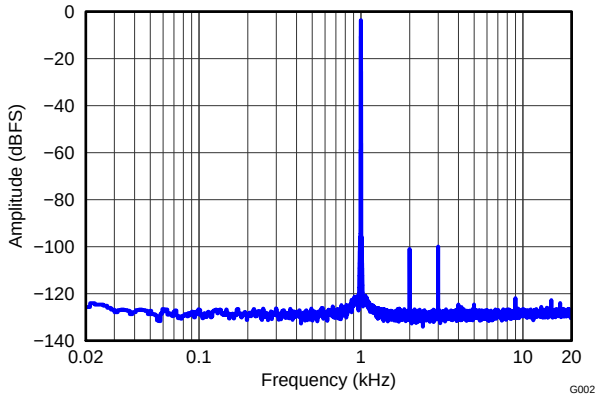


Figure 8. ADC Single Ended Input to ADC Fft at -3 DBR vs Frequency

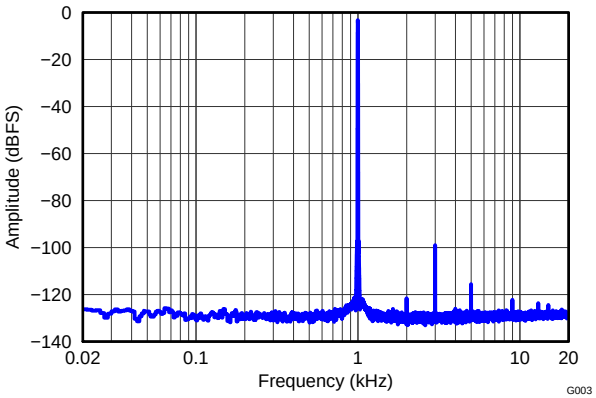


Figure 9. ADC Differential Input to ADC FFT at -3 DBR vs Frequency

8.19.2 Audio DAC Performance

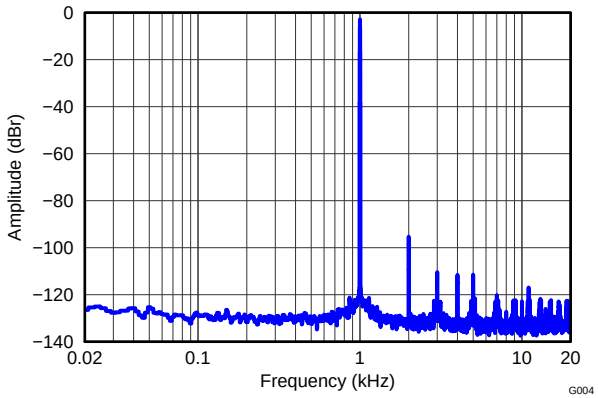


Figure 10. DAC to Line Output FFT Amplitude at -3 dBFS vs Frequency 10-kΩ Load

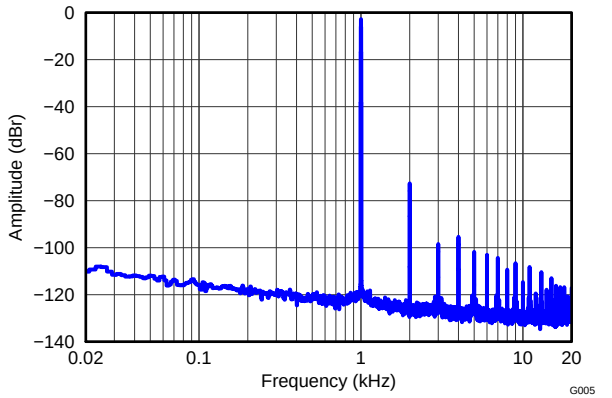


Figure 11. DAC to Headphone Output (GCHP) FFT Amplitude at -3 dBFS vs Frequency 16-Ω Load

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Audio DAC Performance (continued)

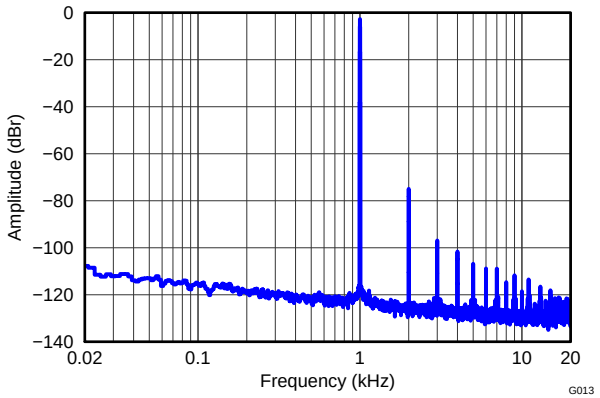


Figure 12. DAC to Headphone Output (GCHP) FFT Amplitude at -3 dBFS vs Frequency 32-Ω Load

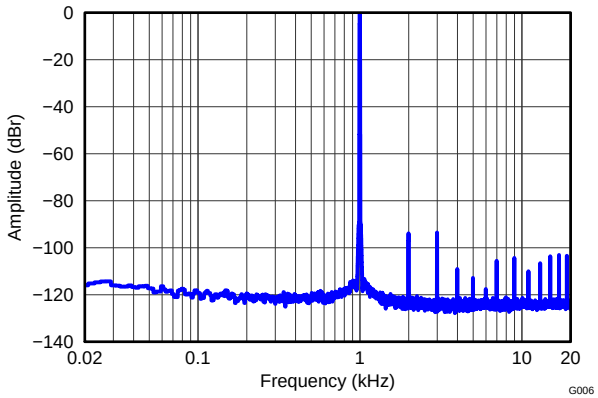


Figure 13. DAC to Differential Receiver Output FFT Amplitude at -3 dBFS vs Frequency 32Ω Load

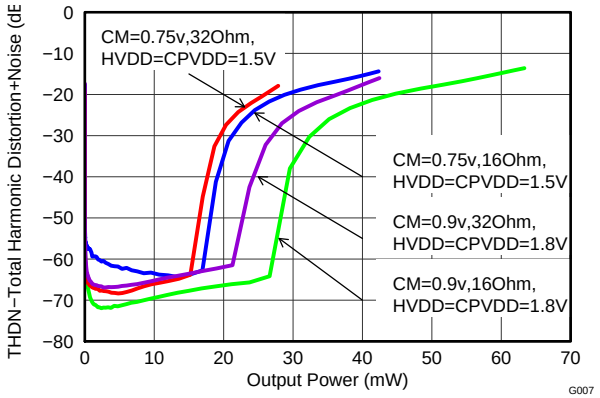


Figure 14. Total Harmonic Distortion+Noise vs Headphone (GCHP) Output Power 9-dB Gain

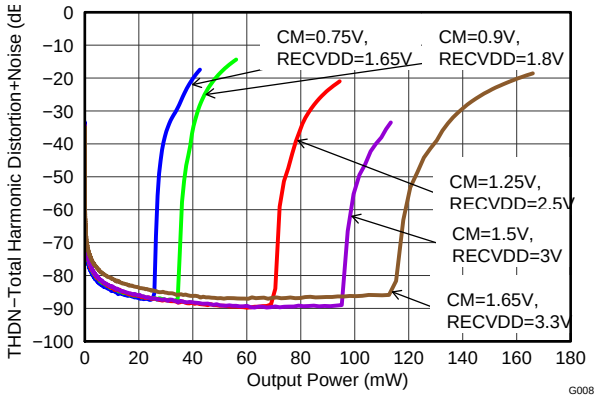


Figure 15. Total Harmonic Distortion+Noise vs Differential Receiver Output Power 32-Ω Load

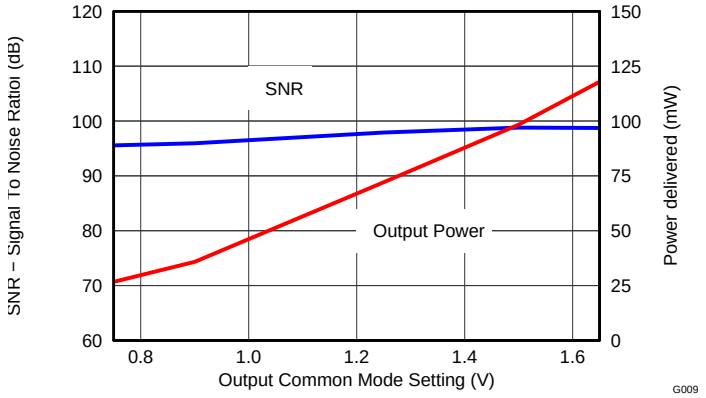


Figure 16. Differential Receiver SNR and Output Power vs Output Common Mode Setting 32-Ω Load

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8.19.3 Class-D Driver Performance

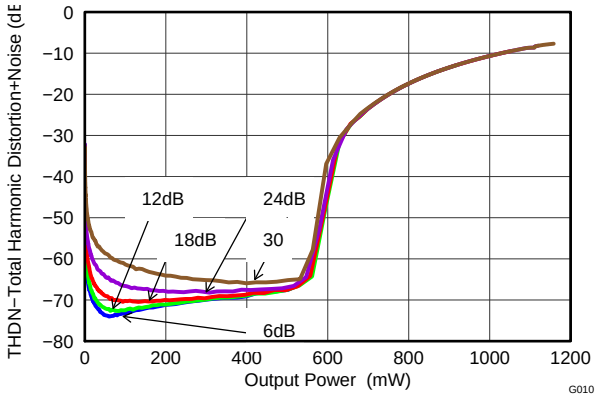


Figure 17. Total Harmonic Distortion + Noise vs Output Power with Different Gain Settings, 8-Ω Load, SLVDD=SRVDD=SPK_V=3.6V

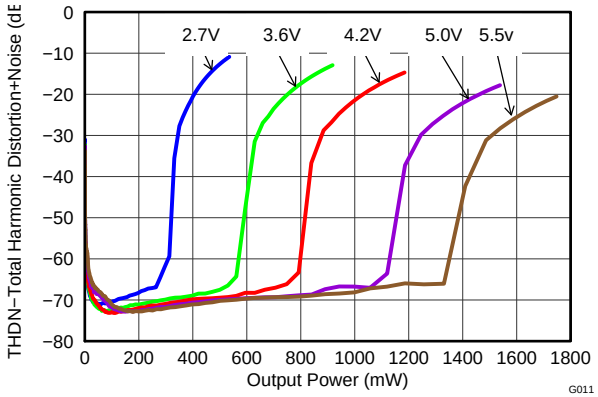


Figure 18. Total Harmonic Distortion + Noise vs Output Power with Different SLVDD/SRVDD/SPK_V Supplies, 8Ω Load, 12dB Gain

8.19.4 MICBIAS Performance

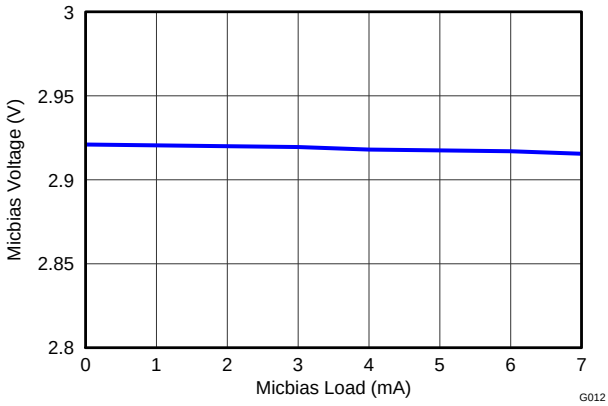


Figure 19. MICBIAS Mode 2, CM = 0.9V, AVDD3_33 OP STAGE vs MICBIAS Load Current

9 Parameter Measurement Information

All parameters are measured according to the conditions described in *Specifications*.

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10 Detailed Description

10.1 Overview

The TLV320AIC3212 device is a flexible, highly-integrated, low-power, low-voltage stereo audio codec with digital microphone inputs and programmable outputs, PowerTune capabilities, selectable audio-processing blocks, fixed predefined and parameterizable signal processing blocks, integrated PLL, and flexible digital audio interfaces. The device is intended for applications in mobile handsets, tablets, eBooks, portable navigation devices, portable media player, portable gaming systems, and portable computing. Available in a 4.81mm × 4.81mm 81-ball WCSP (YZF) Package, the device includes an extensive register-based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks, allowing the codec to be precisely targeted to its application.

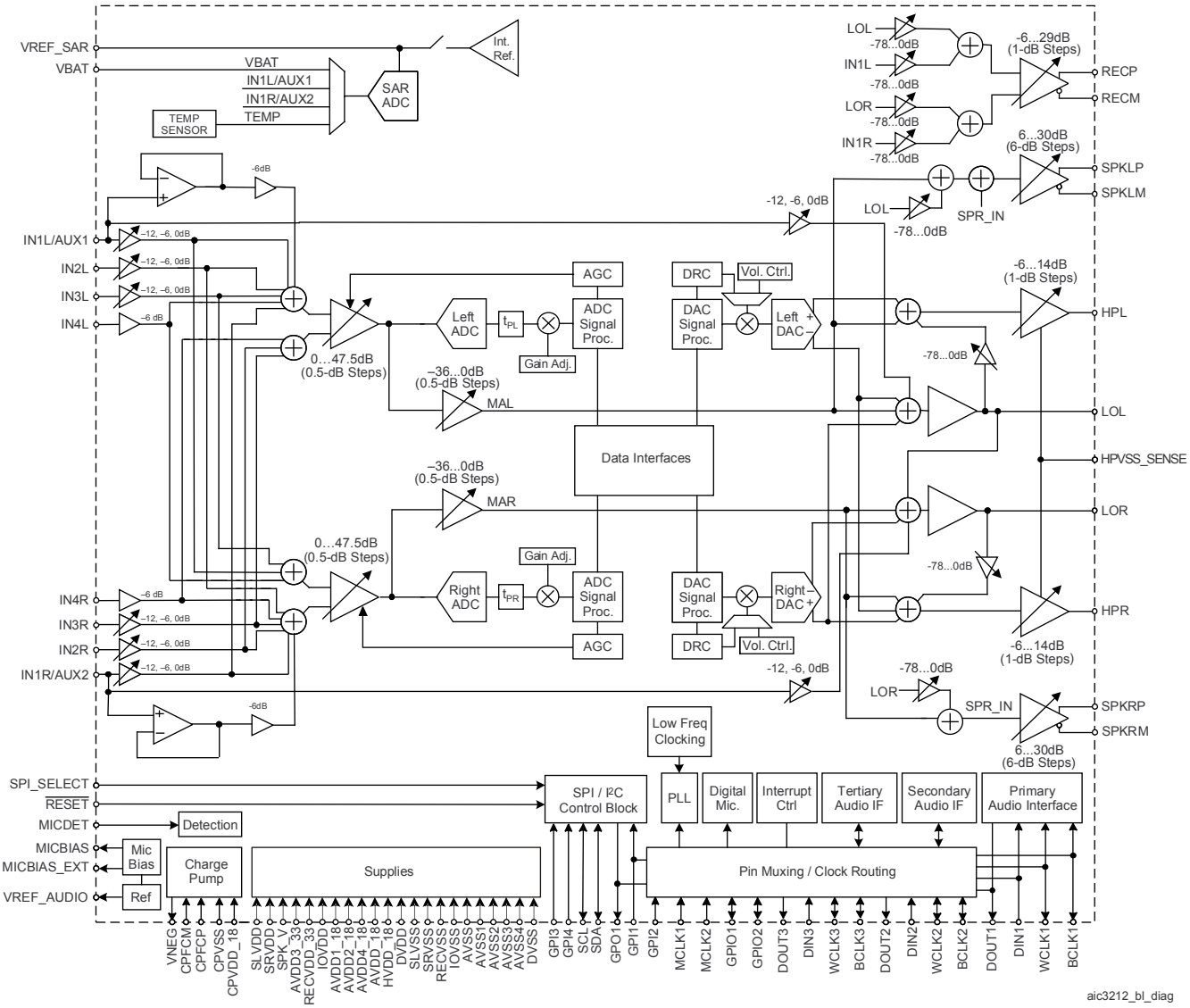
The TLV320AIC3212 consists of the following blocks:

- 5.6-mW Stereo Audio ADC with 93dB SNR
- 2.7-mW Stereo 48kHz DAC Playback
- 30-mW DirectPath Headphone Driver
- 128-mW Differential Receiver Output Driver
- Stereo Class-D Speaker Drivers
- Programmable 12-Bit SAR ADC
- SPI and I2C Control Interfaces
- Three Independent Digital Audio Serial Interfaces
- Programmable PLL Generator

The TLV320AIC3212 features PowerTune to trade power dissipation versus performance. This mechanism has many modes that can be selected at the time of device configuration.

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10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Device Connections

10.3.1.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are hardware-control pins $\overline{\text{RESET}}$ and SPI_SELECT pin. Depending on the state of SPI_SELECT, four pins SCL, SDA, GPO1, and GPI1 are configured for either I^2C or SPI protocol. Only in I^2C mode, GPI3 and GPI4 provide four possible I^2C addresses for the TLV320AIC3212.

Other digital IO pins can be configured for various functions via register control.

10.3.1.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

The possible analog routings of analog input pins to ADCs and output amplifiers as well as the routing from DACs to output amplifiers can be seen in the Analog Routing Diagram.

10.3.1.3 Multifunction Pins

Table 1 show the possible allocation of pins for specific functions.

Table 1. Multifunction Pin Assignments for Pins MCLK1, MCLK2, WCLK1, BCLK1, DIN1, DOUT1, WCLK2, BCLK2, DIN2, and DOUT2

		1	2	3	4	5	6	7	8	9	10
	PIN FUNCTION	**MCLK1**	**MCLK2**	**WCLK1**	**BCLK1**	**DIN1**	**DOUT1**	**WCLK2**	**BCLK2**	**DIN2**	**DOUT2**
A	INT1 Output						E	E	E		E
B	INT2 Output						E	E	E		E
C	SAR ADC Interrupt						E	E	E		E
D	CLOCKOUT Output			E			E	E	E		
E	ADC_MOD_CLOCK Output							E	E		E
F	Single DOUT for ASI1						E, D				
F	Single DOUT for ASI2										E, D
F	Single DOUT for ASI3										
I	General Purpose Output (via Reg)						E(1)	E	E		E
F	Single DIN for ASI1					E, D(2)					
F	Single DIN for ASI2									E, D	
F	Single DIN for ASI3										
J	Digital Mic Data		E			E				E	

(1) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (for example, if DOUT1 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)
(2) D: Default Function

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Feature Description (continued)

Table 1. Multifunction Pin Assignments for Pins MCLK1, MCLK2, WCLK1, BCLK1, DIN1, DOUT1, WCLK2, BCLK2, DIN2, and DOUT2 (continued)

		1	2	3	4	5	6	7	8	9	10
	PIN FUNCTION	**MCLK1**	**MCLK2**	**WCLK1**	**BCLK1**	**DIN1**	**DOUT1**	**WCLK2**	**BCLK2**	**DIN2**	**DOUT2**
K	Input to PLL_CLKIN	S(3), D	S		S(4)	S			S(4)		
L	Input to ADC_CLKIN	S(3), D	S		S(4)				S(4)		
M	Input to DAC_CLKIN	S(3), D	S		S(4)				S(4)		
N	Input to CDIV_CLKIN	S(3), D	S		S	S			S		
O	Input to LFR_CLKIN	S(3), D	S	S				S	S	S	
P	Input to HF_CLK	S(3)									
Q	Input to REF_1MHz_CLK	S(3)									
R	General Purpose Input (via Reg)					E		E	E	E	
T	WCLK Output for ASI1			E							
U	WCLK Input for ASI1			S, D							
V	BCLK Output for ASI1				E						
W	BCLK Input for ASI1				S(4), D						
X	WCLK Output for ASI2							E			
Y	WCLK Input for ASI2							S, D			
Z	BCLK Output for ASI2								E		
AA	BCLK Input for ASI2								S(4), D		
BB	WCLK Output for ASI3										
CC	WCLK Input for ASI3										
DD	BCLK Output for ASI3										
EE	BCLK Input for ASI3										

(3) S(3): The MCLK1 pin could be chosen to drive the PLL, ADC Clock, DAC Clock, CDIV Clock, LFR Clock, HF Clock, and REF_1MHz_CLK inputs **simultaneously**
(4) S(4): The BCLK1 or BCLK2 pins could be chosen to drive the PLL, ADC Clock, DAC Clock, and audio interface bit clock inputs **simultaneously**

Table 2. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, GPI1, GPI2, GPI3, and GPI4

		11	12	13	14	15	16	17	18	19	20	21
	PIN FUNCTION	**WCLK3**	**BCLK3**	**DIN3**	**DOUT3**	**GPIO1**	**GPIO2**	**GPO1/ MISO(1)**	**GPI1/ SCLK(1)**	**GPI2**	**GPI3(2)**	**GPI4(2)**
A	INT1 Output					E	E	E				
B	INT2 Output					E	E	E				
C	SAR ADC Interrupt					E	E	E				
D	CLOCKOUT Output					E	E	E				
E	ADC_MOD_CLOCK Output					E	E	E				
F	Single DOUT for ASI1							E				
F	Single DOUT for ASI2											
F	Single DOUT for ASI3				E, D							
I	General Purpose Output (via Reg)	E(3)	E		E	E	E	E				

(1) GPO1 and GPI1 can only be utilized for functions defined in this table when part utilizes I^2C for control. In SPI mode, these pins serve as the MISO and SCLK, respectively.
(2) GPI3 and GPI4 can only be utilized for functions defined in this table when part utilizes SPI for control. In I^2C mode, these pins serve as I^2C address pins.
(3) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (for example, if WCLK3 has been allocated for General Purpose Output, it cannot be used as the ASI3 WCLK output at the same time)

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Table 2. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, GPI1, GPI2, GPI3, and GPI4 (continued)

		11	12	13	14	15	16	17	18	19	20	21
	PIN FUNCTION	**WCLK3**	**BCLK3**	**DIN3**	**DOUT3**	**GPIO1**	**GPIO2**	**GPO1/ MISO(1)**	**GPI1/ SCLK(1)**	**GPI2**	**GPI3(2)**	**GPI4(2)**
F	Single DIN for ASI1									E		
F	Single DIN for ASI2											
F	Single DIN for ASI3			E, D								
J	Digital Mic Data					E	E		E	E		
K	Input to PLL_CLKIN					S(4)	S(4)		S(4)	S(4)		
L	Input to ADC_CLKIN					S(4)	S(4)		S(4)	S(4)		
M	Input to DAC_CLKIN					S(4)	S(4)		S(4)	S(4)		
N	Input to CDIV_CLKIN								S	S		
O	Input to LFR_CLKIN	S	S			S	S		S	S		
P	Input to HF_CLK											
Q	Input to REF_1MHz_CLK											
R	General Purpose Input (via Reg)	E	E	E		E	E		E	E		
T	WCLK Output for ASI1				E	E						
U	WCLK Input for ASI1					E						
V	BCLK Output for ASI1						E					
W	BCLK Input for ASI1						E					
X	WCLK Output for ASI2											
Y	WCLK Input for ASI2											
Z	BCLK Output for ASI2											
AA	BCLK Input for ASI2											
BB	WCLK Output for ASI3	E										
CC	WCLK Input for ASI3	S, D(5)										
DD	BCLK Output for ASI3		E									
EE	BCLK Input for ASI3		S, D									
FF	ADC BCLK Input for ASI1					E	E		E	E	E	E
GG	ADC WCLK Input for ASI1					E	E		E	E	E	E
HH	ADC BCLK Output for ASI1					E	E					
II	ADC WCLK Output for ASI1					E	E					
JJ	ADC BCLK Input for ASI2					E	E		E	E	E	E
KK	ADC WCLK Input for ASI2					E	E		E	E	E	E
LL	ADC BCLK Output for ASI2					E	E					
MM	ADC WCLK Output for ASI2					E	E					
NN	ADC BCLK Input for ASI3					E	E		E	E	E	E
OO	ADC WCLK Input for ASI3					E	E		E	E	E	E

(4) S(4): The GPIO1, GPIO2, GPI1, or GPI2 pins could be chosen to drive the PLL, ADC Clock, and DAC Clock inputs **simultaneously**
(5) D: Default Function

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Table 2. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, GPI1, GPI2, GPI3, and GPI4 (continued)

		11	12	13	14	15	16	17	18	19	20	21
	PIN FUNCTION	**WCLK3**	**BCLK3**	**DIN3**	**DOUT3**	**GPIO1**	**GPIO2**	**GPO1/ MISO(1)**	**GPI1/ SCLK(1)**	**GPI2**	**GPI3(2)**	**GPI4(2)**
PP	ADC BCLK Output for ASI3					E	E					
QQ	ADC WCLK Output for ASI3					E	E					

10.3.2 Analog Audio I/O

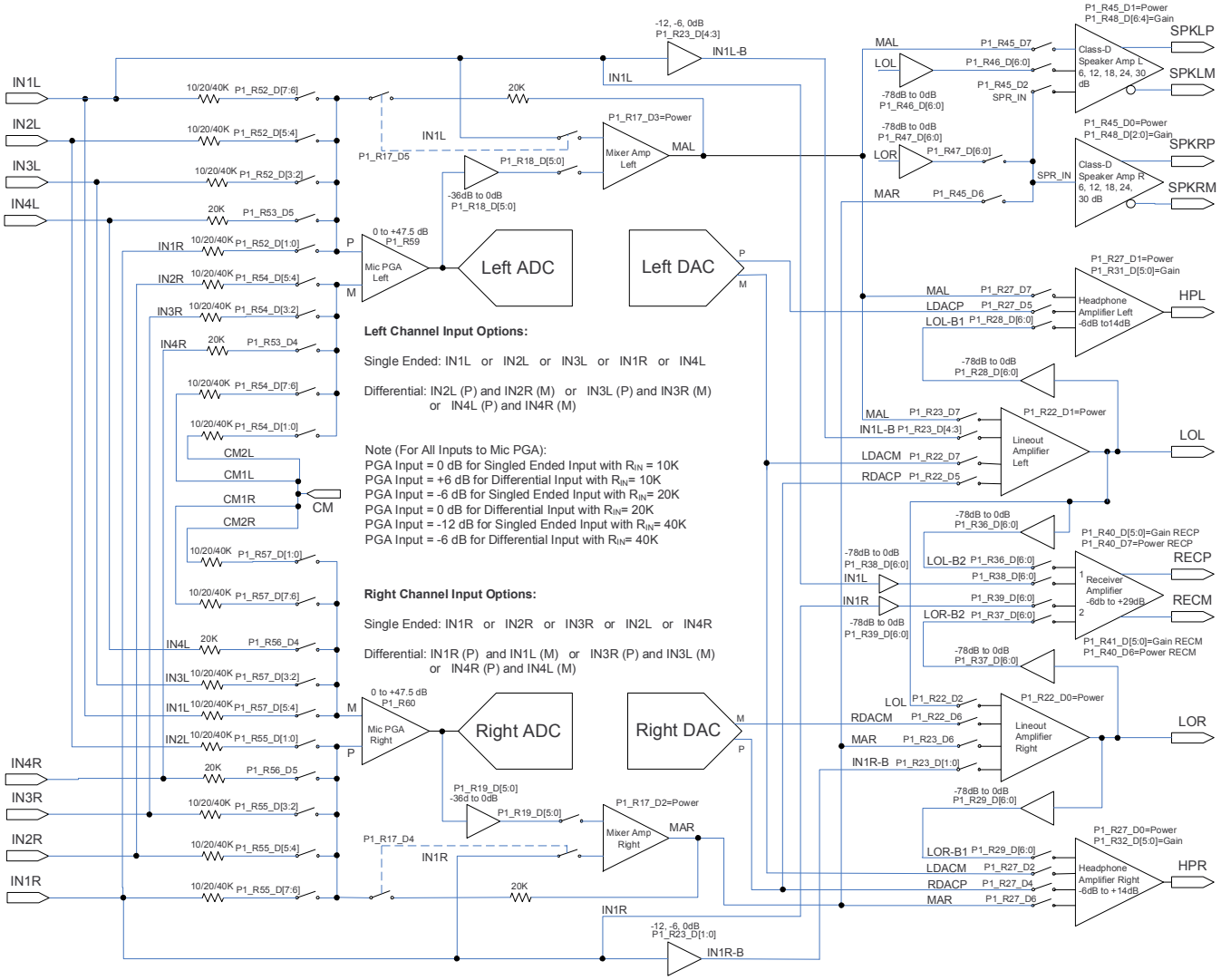


Figure 20. Analog Routing Diagram

10.3.2.1 Analog Low Power Bypass

The TLV320AIC3212 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input terminal to an amplifier driving an analog output terminal. Neither the ADC nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode. In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1L to the left lineout amplifier (LOL) and IN1R to LOR. Additionally, line-level signals can be routed directly from these analog inputs to the differential receiver amplifier, which outputs on RECP and RECM.

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10.3.2.2 Headphone Outputs

The stereo headphone drivers on terminals HPL and HPR can drive loads with impedances down to 16 Ω in single-ended DC-coupled headphone configurations. An integral charge pump generates the negative supply required to operate the headphone drivers in dc-coupled mode, where the common mode of the output signal is made equal to the ground of the headphone load using a ground-sense circuit. Operation of headphone drivers in dc-coupled (ground centered mode) eliminates the need for large DC-blocking capacitors.

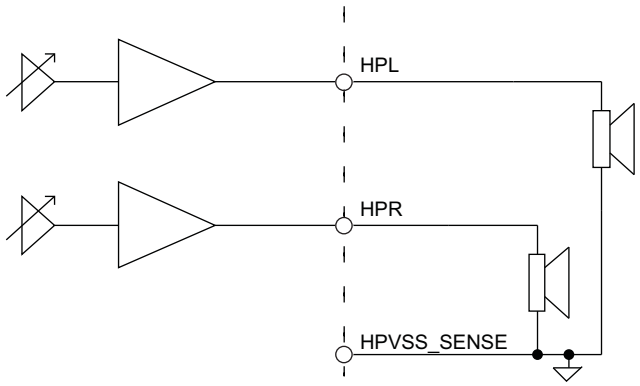


Figure 21. TLV320AIC3212 Ground-Centered Headphone Output

Alternatively the headphone amplifier can also be operated in a unipolar circuit configuration using DC blocking capacitors.

10.3.2.2.1 Using the Headphone Amplifier

The headphone drivers are capable of driving a mixed combination of DAC signal, left and right ADC PGA signal, and LOL and LOR output signals by configuring B0_P1_R27-R29. The ADC PGA signals can be attenuated up to 36 dB before routing to headphone drivers by configuring B0_P1_R18 and B0_P1_R19. The line-output signals can be attenuated up to 78 dB before routing to headphone drivers by configuring B0_P1_R28 and B0_P1_R29. The level of the DAC signal can be controlled using the digital volume control of the DAC by configuring B0_P0_R64-R66. To control the output-voltage swing of headphone drivers, the headphone driver volume control provides a range of –6.0 dB to +14.0 dB(1) in steps of 1 dB. These can be configured by programming B0_P1_R27, B0_P1_R31, and B0_P1_R32. In addition, finer volume controls are also available when routing LOL or LOR to the headphone drivers by controlling B0_P1_R27-R28. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Register B0_P1_R9_D[6:5] allows the headphone output stage to be scaled to tradeoff power delivered vs quiescent power consumption. (1)

10.3.2.2.2 Ground-Centered Headphone Amplifier Configuration

Among the other advantages of the ground-centered connection is inherent freedom from turnon transients that can cause audible pops, sometimes at uncomfortable volumes.

(1) If the device must be placed into 'mute' from the –6.0 dB setting, set the device at a gain of –5.0 dB first, then place the device into mute.

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10.3.2.2.2.1 Circuit Topology

The power supply hook up scheme for the ground centered configuration is shown in HVDD_18 terminal supplies the positive side of the headphone amplifier. CPVDD_18 terminal supplies the charge pump which in turn supplies the negative side of the headphone amplifier. Two capacitors are required for the charge pump circuit to work. These capacitors should be X7R rated.

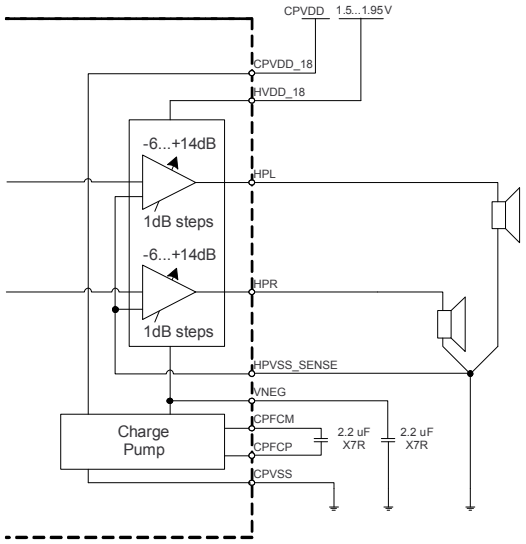


Figure 22. Ground-Centered Headphone Connections

10.3.2.2.2.2 Charge Pump Setup and Operation

The built in charge pump draws charge from the CPVDD_18 supply, and by switching the external capacitor between CPFCP and CPFCM, generates the negative voltage on VNEG terminal. The charge-pump circuit uses the principles of switched-capacitor charge conservation to generate the VNEG supply in a very efficient fashion.

To turn on the charge pump circuit when headphone drivers are powered, program B0_P1_R35_D[1:0] to 00. When the charge pump circuit is disabled, VNEG acts as a ground terminal, allowing unipolar configuration of the headphone amps. By default, the charge pump is disabled. The switching rate of the charge pump can be controlled by B0_P1_R33. Because the charge pump can demand significant inrush currents from the supply, it is important to have a capacitor connected in close proximity to the CPVDD_18 and CPVSS terminals of the device. At 500-kHz clock rate this requires approximately a 10-µF capacitor. The ESR and ESL of the capacitor must be low to allow fast switching currents.

The ground-centered mode of operation is enabled by configuring B0_P1_R31_D7 to 1. Note that the HPL and HPR gain settings are ganged in Ground-Cetered Mode of operation (B0_P1_R32_D7 = 1). The HPL and HPR gain settings cannot be ganged if using the Stereo Unipolar Configuration.

10.3.2.2.2.3 Output Power Optimization

The device can be optimized for a specific output-power range. The charge pump and the headphone driver circuitry can be reduced in power so less overall power is consumed. The headphone driver power can be programmed in B0_P1_R9. The control of charge pump switching current is programmed in B0_P1_R34_D[4:2].

10.3.2.2.2.4 Offset Correction and Start-Up

The TLV320AIC3212 offers an offset-correction scheme that is based on calibration during power up. This scheme minimizes the differences in DC voltage between HPVSS_SENSE and HPL/HPR outputs.

The offset calibration happens after the headphones are powered up in ground-centered configuration. All other headphone configurations like signal routings, gain settings, and mute removal must be configured before headphone power-up. Any change in these settings while the headphones are powered up may result in additional offsets and are best avoided.

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The offset-calibration block has a few programmable parameters that the user must control. The user can either choose to calibrate the offset only for the selected input routing or all input configurations. The calibration data is stored in internal memory until the next hardware reset or until AVDDx power is removed.

Programming B0_P1_R34_D[1:0] as 10 causes the offset to be calibrated for the selected input mode. Programming B0_P1_R34_D[1:0] as “11” causes the offset to be calibrated for all possible configurations. All related blocks must be powered while doing offset correction.

Programming B0_P1_R34_D[1:0] as 00 (default) disables the offset correction block. While the offset is being calibrated, no signal should be applied to the headphone amplifier, that is the DAC should be kept muted and analog bypass routing should be kept at the highest attenuation.

10.3.2.2.2.5 Ground-Centered Headphone Setup

There are four practical device setups for ground-centered operation , shown in Table 3:

Table 3. Ground-Centered Headphone Setup Performance Options

AUDIO OUTPUT POWER		HIGH PERFORMANCE			LOW POWER CONSUMPTION		
		16Ω	32Ω	600Ω	16Ω	32Ω	600Ω
High	SNR	94 dB	97 dB	98 dB	91 dB	94 dB	95 dB
	Output Power	25 mW	22 mW	1.4mW	24 mW	23 mW	1.5mW
	Idle Power Consumption	23 mW	21 mW	19mW	20 mW	15 mW	12 mW
		High-Output, High-Performance Setup			High-Output, Low-Power Setup		
Medium	SNR	92.5 dB	93 dB	93.5 dB	80.5 dB	85.5 dB	85.5 dB
	Output Power	16 mW	8.5 mW	0.5 mW	0.9 mW	1.5mW	0.1 mW
	Idle Power Consumption	14 mW	12 mW	9.7 mW	8.0 mW	6.6mW	5.1 mW
		Medium-Output, High-Performance Setup			Medium-Output, Low-Power Setup		

10.3.2.2.2.5.1 High Audio Output Power, High Performance Setup

This setup describes the register programming necessary to configure the device for a combination of high audio output power and high performance. To achieve this combination the parameters must be programmed to the values in Table 4. For the full setup script, see .

Table 4. Setup A - High Audio Output Power, High Performance

PARAMETER	VALUE	PROGRAMMING
CM	0.9	B0_P1_R8_D2 = "0"
PTM	PTM_P3	B0_P1_R3_D[4:2] = "000", B0_P1_R4_D[4:2] = "000"
Processing Block	1 to 6,22,23,24	B0_P0_R60_D[4:0]
DAC OSR	128	B0_P0_R13 = 0x00, B0_P0_R14 = 0x80
HP sizing	100	B0_P1_R9_D[6:5] = "00"
Gain	5dB	B0_P1_R31 = 0x85, B0_P1_R32 = 0x85
DVDD	1.8	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.8	Apply 1.8 to 1.95V

10.3.2.2.2.5.2 High Audio Output Power, Low Power Consumption Setup

This setup describes the register programming necessary to configure the device for a combination of high audio output power and low power consumption. To achieve this combination the parameters must be programmed to the values in Table 5. For the full setup script, see .

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Table 5. Setup B - High Audio Output Power, Low Power Consumption

PARAMETER	VALUE	PROGRAMMING
CM	0.75	B0_P1_R8_D2 = "1"
PTM	PTM_P2	B0_P1_R3_D[4:2] = "001", B0_P1_R4_D[4:2] = "001"
Processing Block	7 to 16	B0_P0_R60_D[4:0]
DAC OSR	64	B0_P0_R13 = 0x00, B0_P0_R14 = 0x40
HP sizing	100	B0_P1_R9_D[6:5] = "00"
Gain	12dB	B0_P1_R31 = 0x8c, B0_P1_R32 = 0x8c
DVDD	1.26	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.8	Apply 1.5 to 1.95V

10.3.2.2.2.5.3 Medium Audio Output Power, High Performance Setup

This setup describes the register programming necessary to configure the device for a combination of medium audio output power and high performance. To achieve this combination the parameters must be programmed to the values in Table 6. For the full setup script, see .

Table 6. Setup C - Medium Audio Output Power, High Performance

PARAMETER	VALUE	PROGRAMMING
CM	0.75	B0_P1_R8_D2 = "1"
PTM	PTM_P2	B0_P1_R3_D[4:2] = "001", B0_P1_R4_D[4:2] = "001"
Processing Block	7 to 16	B0_P0_R60_D[4:0]
DAC OSR	64	B0_P0_R13 = 0x00, B0_P0_R14 = 0x40
HP sizing	100	B0_P1_R9_D[6:5] = "00"
Gain	7dB	B0_P1_R31 = 0x87, B0_P1_R32 = 0x87
DVDD	1.26	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.5	Apply 1.8 to 1.95V

10.3.2.2.2.5.4 Lowest Power Consumption, Medium Audio Output Power Setup

This setup describes the register programming necessary to configure the device for a combination of medium audio output power and lowest power consumption. To achieve this combination the parameters must be programmed to the values in Table 7. For the full setup script, see .

Table 7. Setup D - Lowest Power Consumption, Medium Audio Output Power

PARAMETER	VALUE	PROGRAMMING
CM	0.75	B0_P1_R8_D2 = "1"
PTM	PTM_P1	B0_P1_R3_D[4:2] = "010", B0_P1_R4_D[4:2] = "010"
Processing Block	26	B0_P0_R60_D[4:0] = "1 1010"
DAC OSR	64	B0_P0_R13 = 0x00, B0_P0_R14 = 0x40
HP sizing	25	B0_P1_R9_D[6:5] = "11"
Gain	10dB	B0_P1_R31 = 0x8a , B0_P1_R32 = 0x8a
DVdd	1.26	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.5	Apply 1.5 to 1.95V

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10.3.2.2.3 Stereo Unipolar Configuration

10.3.2.2.3.1 Circuit Topology

The power supply hook up scheme for the unipolar configuration is shown in Figure 23. HVDD_18 terminal supplies the positive side of the headphone amplifier. The negative side is connected to ground potential (VNEG). It is recommended to connect the CPVDD_18 terminal to DVdd, although the charge pump *must not* be enabled while the device is connected in unipolar configuration.

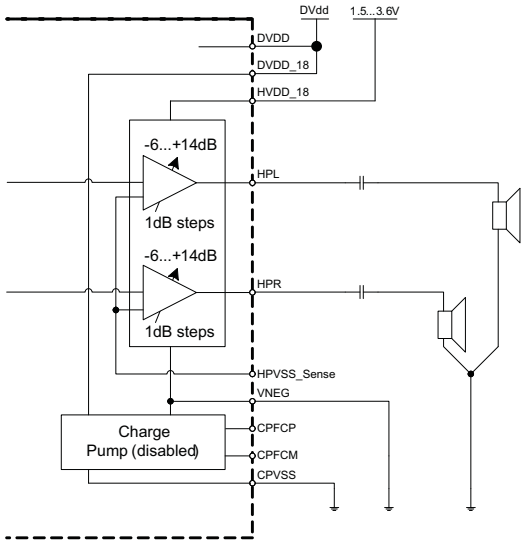


Figure 23. Unipolar Stereo Headphone Circuit

The left and right DAC channels are routed to the corresponding left and right headphone amplifier. This configuration is also used to drive line-level loads. To enable cap-coupled mode, B0_P1_R31_D7 should be set to 0. Note that the recommended range for the HVDD_18 supply in cap-coupled mode (1.65 V - 3.6 V) is different than the recommended range for the default ground-centered configuration (1.5 V - 1.95 V). In cap-coupled mode only, the Headphone output common mode can be controlled by changing B0_P1_R8_D[4:3].

10.3.2.2.3.2 Unipolar Turn-On Transient (Pop) Reduction

The TLV320AIC3212 headphone drivers also support pop-free operation in unipolar, ac-coupled configuration. Because the HPL and HPR are high-power drivers, pop can result due to sudden transient changes in the output drivers if care is not taken. The most critical care is required while using the drivers as stereo single-ended capacitively-coupled drivers as shown in Figure 23. The output drivers achieve pop-free power-up by using slow power-up modes. Conceptually, the circuit during power-up can be visualized as

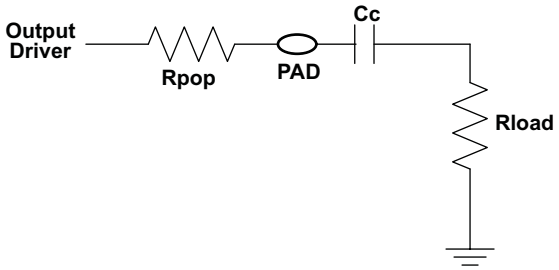


Figure 24. Conceptual Circuit for Pop-Free Power-up

The value of R_{pop} can be chosen by setting register B0_P1_R11_D[1:0].

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Table 8. R_{pop} Values (External C_c = 47uF)

B0_P1_R11_D[1:0]	R_{pop} VALUE
10	2 kΩ
01	6 kΩ
00	25 kΩ

To minimize audible artifacts, two parameters can be adjusted to match application requirements. The voltage V_{load} across R_{load} at the beginning of slow charging should not be more than a few mV. At that time the voltage across R_{load} can be determined as:

$$V_{load} = \frac{R_{load}}{R_{load} + R_{pop}} \times V_{cm} \quad (1)$$

For a typical R_{load} of 32 Ω, R_{pop} of 6 kΩ or 25 kΩ will deliver good results (see Table 8 for register settings).

According to the conceptual circuit in Figure 24, the voltage on PAD will exponentially settle to the output common-mode voltage based on the value of R_{pop} and C_c. Thus, the output drivers must be in slow power-up mode for time T, such that at the end of the slow power-on period, the voltage on V_{pad} is very close to the common-mode voltage. The TLV320AIC3212 allows the time T to be adjusted to allow for a wide range of R_{load} and C_c by programming B0_P1_R11_D[5:2]. For the time adjustments, the value of C_c is assumed to be 47µF. N=5 is expected to yield good results.

Table 9. N Values (External C_c = 47 µF)

B0_P1_R11_D[5:2]	Slow Charging Time = N * RC_Time_Constant (for R_{pop} and C_c = 47µF)
0000	N=0
0001	N=0.5
0010	N=0.625
0011	N=0.75
0100	N=0.875
0101	N=1.0
0110	N=2.0
0111	N=3.0
1000	N=4.0
1001	N=5.0 (Typical Value)
1010	N=6.0
1011	N=7.0
1100	N=8.0
1101	N=16 (Not valid for R_{pop}=25kΩ)
1110	N=24 (Not valid for R_{pop}=25kΩ)
1111	N=32 (Not valid for R_{pop}=25kΩ)

Again, for example, for R_{load}=32 Ω, C_c=47 µF and common mode of 0.9 V, the number of time constants required for pop-free operation is 5 or 6. A higher or lower C_c value will require higher or lower value for N.

During the slow-charging period, no signal is routed to the output driver. Therefore, choosing a larger than necessary value of N results in a delay from power-up to signal at output. At the same time, choosing N to be smaller than the optimal value results in poor pop performance at power-up.

The signals being routed to headphone drivers (for example, DAC and IN) often have DC offsets due to less-than-ideal processing. As a result, when these signals are routed to output drivers, the offset voltage causes a pop. To improve the pop-performance in such situations, a feature is provided to soft-step the DC-offset. At the beginning of the signal routing, a high-value attenuation can be applied which can be progressively reduced in steps until the desired gain in the channel is reached. The time interval between each of these gain changes can be controlled by programming B0_P1_R11_D[7:6]. This gain soft-stepping is applied only during the initial routing of the signal to the output driver and not during subsequent gain changes.

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Table 10. Soft-Stepping Step Time

B0_P1_R11_D[7:6]	SOFT-STEPPING STEP TIME DURING INITIAL SIGNAL ROUTING
00	0 ms (soft-stepping disabled)
01	50ms
10	100ms
11	200ms

It is recommended to use the following sequence for achieving optimal pop performance at power-up:

1. Choose the value of R_{pop}, N (time constants) and soft-stepping step time for slow power-up.
2. Choose the configuration for output drivers, including common modes and output stage power connections
3. Select the signals to be routed to headphones.
4. Power-up the blocks driving signals into HPL and HPR, but keep it muted
5. Unmute HPL and HPR and set the desired gain setting.
6. Power-on the HPL and HPR drivers.
7. Unmute the block driving signals to HPL and HPR after the Driver PGA flags are set to indicate completion of soft-stepping after power-up. These flags can be read from B0_P1_R63_D[7:6].

It is important to configure the Headphone Output driver depop control registers before powering up the headphone; these register contents should not be changed when the headphone drivers are powered up.

Before powering down the HPL and HPR drivers, it is recommended that user read back the flags in B0_P1_R63. For example. before powering down the HPL driver, ensure that bit B0_P1_R63_D7 = 1 and bit B0_P1_R64_D7 = 1 if LOL is routed to HPL and bit B0_P1_R65_D5 = 1 if the Left Mixer is routed to HPL. The output driver should be powered down only after a steady-state power-up condition has been achieved. This steady state power-up condition also must be satisfied for changing the HPL/R driver mute control (setting both B0_P1_R31_D[5:0] and B0_P1_R32_D[5:0] to "11 1001"), that is, muting and unmuting should be done after the gain and volume controls associated with routing to HPL/R finished soft-stepping.

In the differential configuration of HPL and HPR, when no coupling capacitor is used, the slow charging method for pop-free performance need not be used. In the differential load configuration for HPL and HPR, it is recommended to not use the output driver MUTE feature, because a pop may result.

During the power-down state, the headphone outputs are weakly pulled to ground using an approximately 50kΩ resistor to ground, to maintain the output voltage on HPL and HPR terminals.

10.3.2.2.4 Mono Differential DAC to Mono Differential Headphone Output

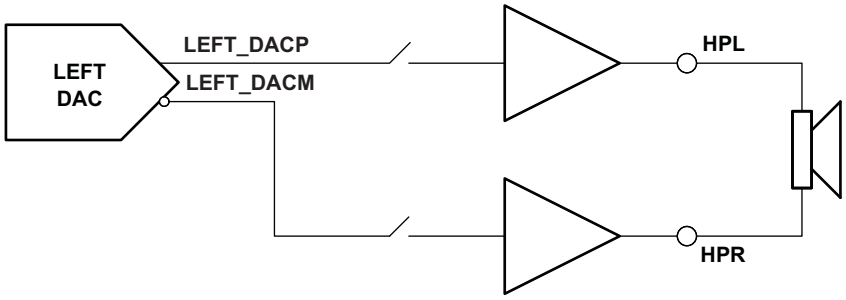


Figure 25. Low Power Mono DAC to Differential Headphone

This configuration, available in unipolar configuration of the HP amplifier supplies, supports the routing of the two differential outputs of the mono, left channel DAC to the headphone amplifiers in differential mode (B0_P1_R27_D5 = 1 and B0_P1_R27_D2 = 1).

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10.3.2.3 Stereo Line Outputs

The stereo line level drivers on LOL and LOR terminals can drive a wide range of line level resistive impedances in the range of 600Ω to 10 kΩ. The output common mode of line level drivers can be configured to equal the analog input common-mode setting, either 0.75V or 0.9V. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal, and signal mixing is register-programmable.

10.3.2.3.1 Line Out Amplifier Configurations

Signal mixing can be configured by programming B0_P1_R22 and B0_P1_R23. To route the output of Left DAC and Right DAC for stereo single-ended output, as shown in Figure 26, LDACM can be routed to LOL driver by setting B0_P1_R22_D7 = 1, and RDACM can be routed to LOR driver by setting B0_P1_R22_D6 = 1. Alternatively, stereo single-ended signals can also be routed through the mixer amplifiers by configuring B0_P1_R23_D[7:6]. For lowest-power operation, stereo single-ended signals can also be routed in direct terminal bypass with possible gains of 0dB, -6dB, or -12dB by configuring B0_P1_R23_D[4:3] and B0_P1_R23_D[1:0]. While each of these two bypass cases could be used in a stereo single-ended configuration, a mono differential input signal could also be used.

The output of the stereo line out drivers can also be routed to the stereo headphone drivers, with 0 dB to –72 dB gain controls in steps of 0.5 dB on each headphone channel. This enables the DAC output or bypass signals to be simultaneously played back to the stereo headphone drivers as well as stereo line-level drivers. This routing and volume control is achieved in B0_P1_R28 and B0_P1_R29.

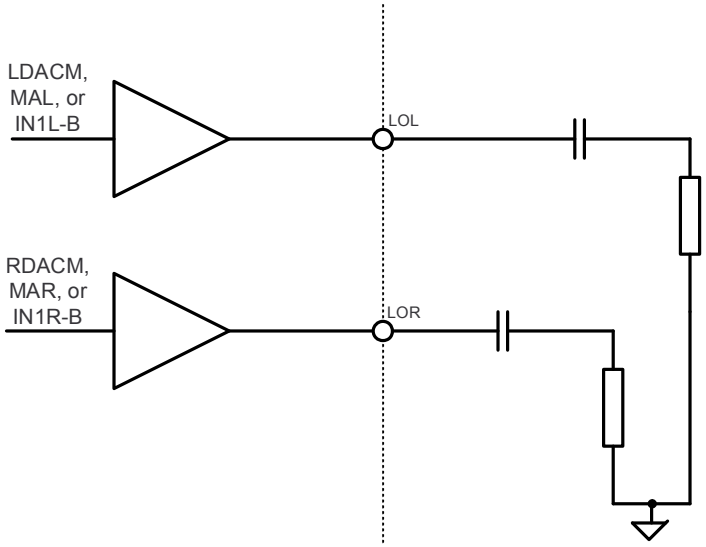


Figure 26. Stereo Single-Ended Line-out

Additionally, the two line-level drivers can be configured to act as a mono differential line level driver by routing the output of LOL to LOR (B0_P1_R22_D2 = 1). This differential signal takes either LDACM, MAL, or IN1L-B as a single-ended mono signal and creates a differential mono output signal on LOL and LOR.

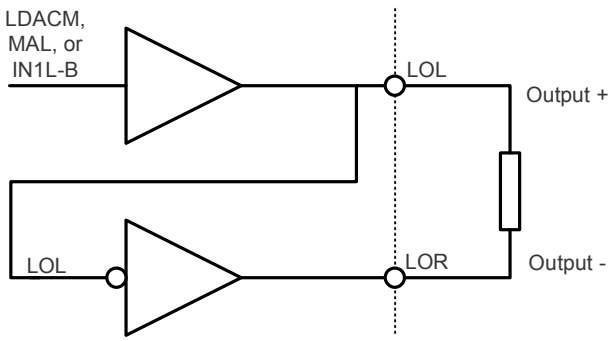


Figure 27. Single Channel Input to Differential Line-out

For digital outputs from the DAC, the two line-level drivers can be fed the differential output signal from the Right DAC by configuring B0_P1_R22_D5 = 1.

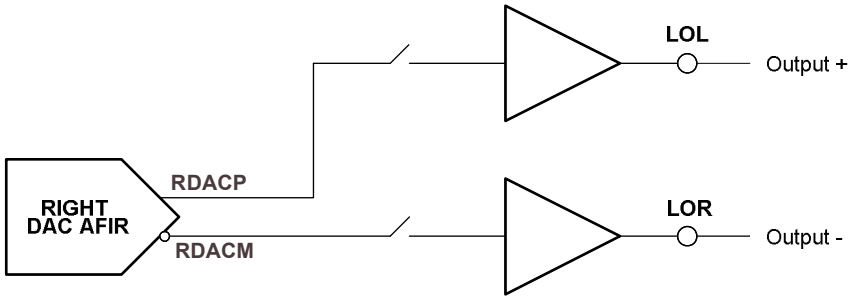


Figure 28. Mono DAC Output to Differential Line-out

10.3.2.4 Differential Receiver Output

The differential receiver amplifier output spans the RECP and RECM terminals and can drive a 32-Ω receiver driver. With output common-mode setting of 1.65 V and RECVDD_33 supply at 3.3 V, the receiver driver can drive up to a 1-Vrms output signal. With the RECVDD_33 supply at 3.3 V, the receiver driver can deliver greater than 128 mW into a 32-Ω BTL load. If desired, the RECVDD_33 supply can be set to 1.8 V, at which the driver can deliver about 40mW into the 32Ω BTL load.

10.3.2.5 Stereo Class-D Speaker Outputs

The integrated Class-D stereo speaker drivers (SPKLP/SPKLN and SPKRP/SPKRN) are capable of driving two 8Ω differential loads. The speaker drivers can be powered directly from the power supply (2.7V to 5.5V) on the SLVDD and SRVDD terminals, however the voltage (including spike voltage) must be limited below the Absolute Maximum Voltage of 6.0 V.

The speaker drivers are capable of supplying 750 mW per channel at 10% THD+N with a 3.6-V power supply and 1.46 W per channel at 10% THD+N with a 5.0-V power supply. Separate left and right channels can be sent to each Class-D driver through the Lineout signal path, or from the mixer amplifiers in the ADC bypass. If only one speaker is being utilized for playback, the analog mixer before the Left Speaker amplifier can sum the left and right audio signals for monophonic playback.

10.3.3 ADC / Digital Microphone Interface

The TLV320AIC3212 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3212 features a large set of options for signal conditioning as well as signal routing:

- 2 ADCs
- 8 analog inputs which can be mixed and/or multiplexed in single-ended and/or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Fine gain adjust of digital channels with 0.1 dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function
- Automatic gain control (AGC)

In addition to the standard set of ADC features the TLV320AIC3212 also offers the following special functions:

- Built in microphone biases
- Stereo digital microphone interface
  - Allows 2 total microphones

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  - Up to 2 digital microphones
  - Up to 2 analog microphones
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive coefficient update mode

10.3.3.1 ADC Processing Blocks — Overview

The TLV320AIC3212 ADC channel includes a built-in digital decimation filter to process the oversampled data from the to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

10.3.3.1.1 ADC Processing Blocks

The TLV320AIC3212 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Decreasing the use of signal-processing capabilities reduces the power consumed by the device. Table 11 gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user programmable coefficients.

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Table 11. ADC Processing Blocks

PROCESSING BLOCKS	CHANNEL	DECIMATION FILTER	1ST ORDER IIR AVAILABLE	NUMBER BIQUADS	FIR	REQUIRED AOSR VALUE	RESOURCE CLASS
PRB_R1(1)	Stereo	A	Yes	0	No	128,64,32,16,8,4	7
PRB_R2	Stereo	A	Yes	5	No	128,64,32,16,8,4	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64,32,16,8,4	8
PRB_R4	Left	A	Yes	0	No	128,64,32,16,8,4	4
PRB_R5	Left	A	Yes	5	No	128,64,32,16,8,4	4
PRB_R6	Left	A	Yes	0	25-Tap	128,64,32,16,8,4	4
PRB_R7	Stereo	B	Yes	0	No	64,32,16,8,4,2	3
PRB_R8	Stereo	B	Yes	3	No	64,32,16,8,4,2	4
PRB_R9	Stereo	B	Yes	0	17-Tap	64,32,16,8,4,2	4
PRB_R10	Left	B	Yes	0	No	64,32,16,8,4,2	2
PRB_R11	Left	B	Yes	3	No	64,32,16,8,4,2	2
PRB_R12	Left	B	Yes	0	17-Tap	64,32,16,8,4,2	2
PRB_R13	Stereo	C	Yes	0	No	32,16,8,4,2,1	3
PRB_R14	Stereo	C	Yes	5	No	32,16,8,4,2,1	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32,16,8,4,2,1	4
PRB_R16	Left	C	Yes	0	No	32,16,8,4,2,1	2
PRB_R17	Left	C	Yes	5	No	32,16,8,4,2,1	2
PRB_R18	Left	C	Yes	0	25-Tap	32,16,8,4,2,1	2

(1) Default

For more detailed information see the *Application Reference Guide*, SLAU360.

10.3.4 DAC

The TLV320AIC3212 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3212 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3212 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3212 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
  - Usable in single-ended stereo or differential mono mode
  - Analog volume setting with a range of -6 to +14 dB
- 2 line-out amplifiers
  - Usable in single-ended stereo or differential mono mode
- 2 Class-D speaker amplifiers
  - Usable in stereo differential mode
  - Analog volume control with a settings of +6, +12, +18, +24, and +30 dB
- 1 Receiver amplifier
  - Usable in mono differential mode
  - Analog volume setting with a range of -6 to +29 dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

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In addition to the standard set of DAC features the TLV320AIC3212 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive coefficient update mode

10.3.4.1 DAC Processing Blocks — Overview

10.3.4.1.1 DAC Processing Blocks

The TLV320AIC3212 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. Table 12 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 12. Overview – DAC Predefined Processing Blocks

PROCESSING BLOCK NO.	INTERPOLATION FILTER	CHANNEL	1ST ORDER IIR AVAILABLE	NUM. OF BIQUADS	DRC	3D	BEEP GENERATOR	RC CLASS
PRB_P1(1)	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	5
PRB_P7	B	Stereo	Yes	0	No	No	No	5
PRB_P8	B	Stereo	No	4	Yes	No	No	9
PRB_P9	B	Stereo	No	4	No	No	No	7
PRB_P10	B	Stereo	Yes	6	Yes	No	No	9
PRB_P11	B	Stereo	Yes	6	No	No	No	7
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	5
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	13

(1) Default

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Table 12. Overview – DAC Predefined Processing Blocks (continued)

PROCESSING BLOCK NO.	INTERPOLATION FILTER	CHANNEL	1ST ORDER IIR AVAILABLE	NUM. OF BIQUADS	DRC	3D	BEEP GENERATOR	RC CLASS
PRB_P26	D	Stereo	No	0	No	No	No	1

For more detailed information see the *Application Reference Guide*, SLAU360.

10.3.5 Device Power Consumption

Device power consumption largely depends on PowerTune configuration. For information on device power consumption, see the *TLV320AIC3212 Application Reference Guide*, SLAU360.

10.3.6 Powertune

The TLV320AIC3212 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application.

For more detailed information see the *Application Reference Guide*, SLAU360.

10.3.7 Clock Generation and PLL

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output terminal and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3212.

The ADC_CLKIN and DAC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the selectable processing block sections.

For more detailed information see the *Application Reference Guide*, SLAU360.

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10.3.8 Interfaces

10.3.8.1 Control Interfaces

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output terminal and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3212.

The ADC_CLKIN and DAC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the selectable processing block sections.

10.3.8.1.1 I^2C Control

The TLV320AIC3212 supports the I^2C control protocol, and will respond by default (GPI3 and GPI4 grounded) to the 7-bit I^2C address of 0011000. With the two I^2C address terminals, GPI3 and GPI4, the device can be configured to respond to one of four 7-bit I^2C addresses, 0011000, 0011001, 0011010, or 0011011. The full 8-bit I^2C address can be calculated as:

8-Bit I^2C Address = "00110" + GPI4 + GPI3 + R/W

Example: to write to the TLV320AIC3212 with GPI4 = 1 and GPI3 = 0 the 8-Bit I^2C Address is "00110" + GPI4 + GPI3 + R/W = "00110100" = 0x34

I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

10.3.8.1.2 SPI Control

In the SPI control mode, the TLV320AIC3212 uses the terminals SCL as $\overline{SS}$, GPI1 as SCLK, GPO1 as MISO, SDA as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0) and clock phase setting of 1 (typical microprocessor SPI control bit CPHA = 1). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3212) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI terminal under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI terminal, a byte shifts out on the MISO terminal to the master shift register.

The TLV320AIC3212 interface is designed so that with a clock-phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI terminal and the slave begins driving its MISO terminal on the first serial clock edge. The SSZ terminal can remain low between transmissions; however, the TLV320AIC3212 only interprets the first 8 bits transmitted after the falling edge of SSZ as a command byte, and the next 8 bits as a data byte only if writing to a register. Reserved register bits should be written to their default values. The TLV320AIC3212 is entirely controlled by registers. Reading and writing these registers is accomplished by an 8-bit command sent to the MOSI terminal of the part prior to the data for that register. The command is structured as shown in Figure 29. The first 7 bits specify the address of the register which is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction of data flow on the serial bus. In the case of a register write, the R/W bit should be set to 0. A second byte of data is sent to the MOSI terminal and contains the data to be written to the register. Reading of registers is accomplished in a similar fashion. The 8-bit command word sends the 7-bit register address, followed by the R/W bit = 1 to signify a register read is occurring. The 8-bit register data is then clocked out of the part on the MISO terminal during the second 8 SCLK clocks in the frame.

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Figure 29. Command Word

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR(6)	ADDR(5)	ADDR(4)	ADDR(3)	ADDR(2)	ADDR(1)	ADDR(0)	R/WZ

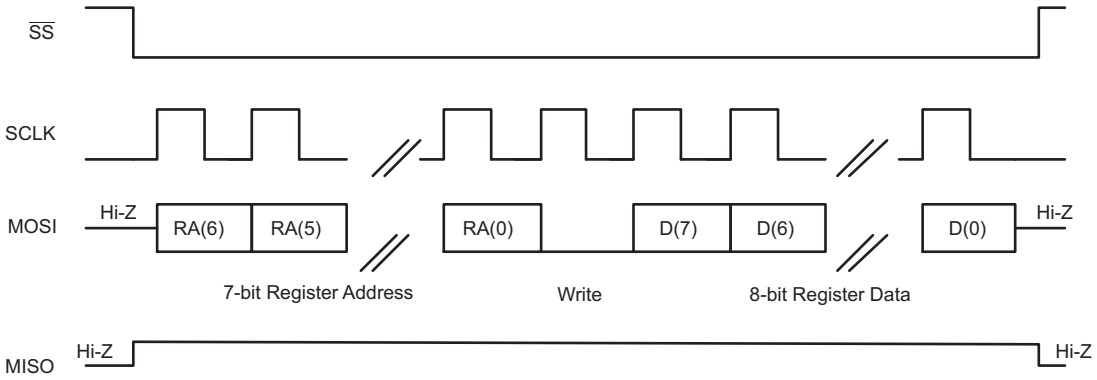


Figure 30. SPI Timing Diagram for Register Write

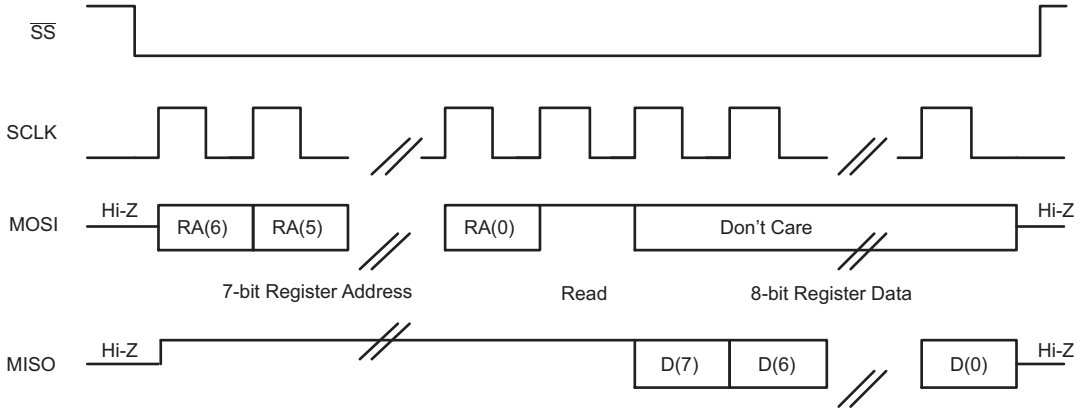


Figure 31. SPI Timing Diagram for Register Read

For more detailed information see the *Application Reference Guide*, SLAU360.

10.3.8.2 Digital Audio Interfaces

The TLV320AIC3212 features three digital audio data serial interfaces, or audio buses. Any of these digital audio interfaces can be selected for playback and recording through the stereo DACs and stereo ADCs respectively. This enables this audio codec to handle digital audio from different devices on a mobile platform. A common example of this would be individual connections to an application processor, a communication baseband processor, or a Bluetooth chipset. By utilizing the TLV320AIC3212 as the center of the audio processing in a portable audio system, hardware design of the audio system is greatly simplified. In addition to these three individual digital audio interfaces, a fourth set of digital audio pins can be muxed into Audio Serial Interface 1. In other words, four separate 4-wire digital audio buses can be connected to the TLV320AIC3212. However, it should be noted that only one of the three audio serial interfaces can be routed to/from the DACs/ADCs at a time.

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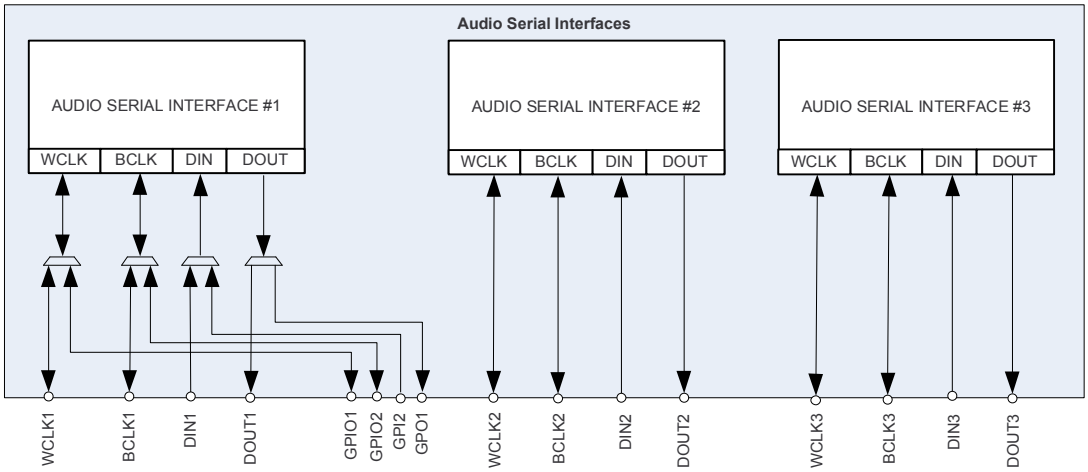


Figure 32. Typical Multiple Connections to Three Audio Serial Interfaces

Each audio bus on the TLV320AIC3212 is very flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master or slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

Each of the three audio buses of the TLV320AIC3212 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate word clocks.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC3212s may share the same audio bus. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate bit clocks.

The TLV320AIC3212 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks.

The TLV320AIC3212 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen.

The TLV320AIC3212 further includes programmability to 3-state the DOUT line during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the terminals associated with the interface are put into a 3-state output condition.

By default, when the word-clocks and bit-clocks are generated by the TLV320AIC3212, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

For more detailed information see the *TLV320AIC3212 Application Reference Guide*, SLAU360.

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10.3.9 Device Special Functions

The following special functions are available to support advanced system requirements:

- SAR ADC
- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the *Application Reference Guide*, SLAU360.

10.4 Device Functional Modes

10.4.1 Recording Mode

The recording mode is activated once the ADC side is enabled. The record path operates from 8 kHz mono to 192 kHz stereo recording, and contains programmable input channel configurations supporting single-ended and differential setups, as well as floating or mixing input signals. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling. The record path can also be configured as a stereo digital microphone PDM interface typically used at 64 Fs or 128 Fs. The TLV320AIC3212 includes Automatic Gain Control (AGC) for ADC recording.

10.4.2 Playback Mode

Once the DAC side is enabled, the playback mode is activated. The playback path offers signal processing blocks for filtering and effects; headphone, line, receiver, and Class-D speaker outputs; flexible mixing of DAC; and analog input signals as well as programmable volume controls. The playback path contains two high-power headphone output drivers which eliminate the need for ac coupling capacitors. These headphone output drivers can be configured in multiple ways, including stereo and mono BTL. In addition, playback audio can be routed to integrated stereo Class-D speaker drivers or a differential receiver amplifier.

10.4.3 Analog Low Power Bypass Modes

The TLV320AIC3212 is a versatile device designed for ultra low-power applications. In some cases, only a few features of the device are required. For these applications, the unused stages of the device must be powered down to save power and an alternate route should be used. This is called analog low power bypass path. The bypass path modes let the device to save power by turning off unused stages, like ADC, DAC and PGA.

The TLV320AIC3212 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed form an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode. In analog low-power bypass mode, line level signals can be routed directly form the analog inputs IN1L to the left lineout amplifier (LOL) and IN1R to LOR. Additionally, line-level signals can be routed directly from these analog inputs to the differential receiver amplifier, which outputs on RECP and RECM.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1L to the positive input on differential receiver amplifier (RECP) and IN1R to RECM, with gain control of –78 dB to 0 dB. This is configured on B0_P1_R38_D[6:0] for the channel and B0_P1_R38_D[6:0] for the left channel and B0_P1_R39_D[6:0] for the right channel.

To use the mixer amplifiers, power them on through B0_P1_R17_D[3:2].

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10.5 Register Maps

Table 13. Summary of Register Map

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	0	0x00	0x00	0x00	Page Select Register
0	0	1	0x00	0x00	0x01	Software Reset Register
0	0	2-3	0x00	0x00	0x02-0x03	Reserved Registers
0	0	4	0x00	0x00	0x04	Clock Control Register 1, Clock Input Multiplexers
0	0	5	0x00	0x00	0x05	Clock Control Register 2, PLL Input Multiplexer
0	0	6	0x00	0x00	0x06	Clock Control Register 3, PLL P and R Values
0	0	7	0x00	0x00	0x07	Clock Control Register 4, PLL J Value
0	0	8	0x00	0x00	0x08	Clock Control Register 5, PLL D Values (MSB)
0	0	9	0x00	0x00	0x09	Clock Control Register 6, PLL D Values (LSB)
0	0	10	0x00	0x00	0x0A	Clock Control Register 7, PLL_CLKIN Divider
0	0	11	0x00	0x00	0x0B	Clock Control Register 8, NDAC Divider Values
0	0	12	0x00	0x00	0x0C	Clock Control Register 9, MDAC Divider Values
0	0	13	0x00	0x00	0x0D	DAC OSR Control Register 1, MSB Value
0	0	14	0x00	0x00	0x0E	DAC OSR Control Register 2, LSB Value
0	0	15-17	0x00	0x00	0x0F-0x11	Reserved Registers
0	0	18	0x00	0x00	0x12	Clock Control Register 10, NADC Values
0	0	19	0x00	0x00	0x13	Clock Control Register 11, MADC Values
0	0	20	0x00	0x00	0x14	ADC Oversampling (AOSR) Register
0	0	21	0x00	0x00	0x15	CLKOUT MUX
0	0	22	0x00	0x00	0x16	Clock Control Register 12, CLKOUT M Divider Value
0	0	23	0x00	0x00	0x17	Timer clock
0	0	24	0x00	0x00	0x18	Low Frequency Clock Generation Control
0	0	25	0x00	0x00	0x19	High Frequency Clock Generation Control 1
0	0	26	0x00	0x00	0x1A	High Frequency Clock Generation Control 2
0	0	27	0x00	0x00	0x1B	High Frequency Clock Generation Control 3
0	0	28	0x00	0x00	0x1C	High Frequency Clock Generation Control 4
0	0	29	0x00	0x00	0x1D	High Frequency Clock Trim Control 1
0	0	30	0x00	0x00	0x1E	High Frequency Clock Trim Control 2
0	0	31	0x00	0x00	0x1F	High Frequency Clock Trim Control 3
0	0	32	0x00	0x00	0x20	High Frequency Clock Trim Control 4
0	0	33-35	0x00	0x00	0x21-0x23	Reserved Registers
0	0	36	0x00	0x00	0x24	ADC Flag Register
0	0	37	0x00	0x00	0x25	DAC Flag Register
0	0	38	0x00	0x00	0x26	DAC Flag Register
0	0	39-41	0x00	0x00	0x27-0x29	Reserved Registers
0	0	42	0x00	0x00	0x2A	Sticky Flag Register 1
0	0	43	0x00	0x00	0x2B	Interrupt Flag Register 1
0	0	44	0x00	0x00	0x2C	Sticky Flag Register 2
0	0	45	0x00	0x00	0x2D	Sticky Flag Register 3
0	0	46	0x00	0x00	0x2E	Interrupt Flag Register 2
0	0	47	0x00	0x00	0x2F	Interrupt Flag Register 3

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Register Maps (continued)

Table 13. Summary of Register Map (continued)

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	48	0x00	0x00	0x30	INT1 Interrupt Control
0	0	49	0x00	0x00	0x31	INT2 Interrupt Control
0	0	50	0x00	0x00	0x32	SAR Control 1
0	0	51	0x00	0x00	0x33	Interrupt Format Control Register
0	0	52-59	0x00	0x00	0x34-0x3B	Reserved Registers
0	0	60	0x00	0x00	0x3C	DAC Processing Block Control
0	0	61	0x00	0x00	0x3D	ADC Processing Block Control
0	0	62	0x00	0x00	0x3E	Reserved Register
0	0	63	0x00	0x00	0x3F	Primary DAC Power and Soft-Stepping Control
0	0	64	0x00	0x00	0x40	Primary DAC Master Volume Configuration
0	0	65	0x00	0x00	0x41	Primary DAC Left Volume Control Setting
0	0	66	0x00	0x00	0x42	Primary DAC Right Volume Control Setting
0	0	67	0x00	0x00	0x43	Headset Detection
0	0	68	0x00	0x00	0x44	DRC Control Register 1
0	0	69	0x00	0x00	0x45	DRC Control Register 2
0	0	70	0x00	0x00	0x46	DRC Control Register 3
0	0	71	0x00	0x00	0x47	Beep Generator Register 1
0	0	72	0x00	0x00	0x48	Beep Generator Register 2
0	0	73	0x00	0x00	0x49	Beep Generator Register 3
0	0	74	0x00	0x00	0x4A	Beep Generator Register 4
0	0	75	0x00	0x00	0x4B	Beep Generator Register 5
0	0	76	0x00	0x00	0x4C	Beep Sin(x) MSB
0	0	77	0x00	0x00	0x4D	Beep Sin(x) LSB
0	0	78	0x00	0x00	0x4E	Beep Cos(x) MSB
0	0	79	0x00	0x00	0x4F	Beep Cos(x) LSB
0	0	80	0x00	0x00	0x50	Reserved Register
0	0	81	0x00	0x00	0x51	ADC Channel Power Control
0	0	82	0x00	0x00	0x52	ADC Fine Gain Volume Control
0	0	83	0x00	0x00	0x53	Left ADC Volume Control
0	0	84	0x00	0x00	0x54	Right ADC Volume Control
0	0	85	0x00	0x00	0x55	ADC Phase Control
0	0	86	0x00	0x00	0x56	Left AGC Control 1
0	0	87	0x00	0x00	0x57	Left AGC Control 2
0	0	88	0x00	0x00	0x58	Left AGC Control 3
0	0	89	0x00	0x00	0x59	Left AGC Attack Time
0	0	90	0x00	0x00	0x5A	Left AGC Decay Time
0	0	91	0x00	0x00	0x5B	Left AGC Noise Debounce
0	0	92	0x00	0x00	0x5C	Left AGC Signal Debounce
0	0	93	0x00	0x00	0x5D	Left AGC Gain
0	0	94	0x00	0x00	0x5E	Right AGC Control 1
0	0	95	0x00	0x00	0x5F	Right AGC Control 2
0	0	96	0x00	0x00	0x60	Right AGC Control 3
0	0	97	0x00	0x00	0x61	Right AGC Attack Time

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Register Maps (continued)

Table 13. Summary of Register Map (continued)

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	98	0x00	0x00	0x62	Right AGC Decay Time
0	0	99	0x00	0x00	0x63	Right AGC Noise Debounce
0	0	100	0x00	0x00	0x64	Right AGC Signal Debounce
0	0	101	0x00	0x00	0x65	Right AGC Gain
0	0	102	0x00	0x00	0x66	ADC DC Measurement Control Register 1
0	0	103	0x00	0x00	0x67	ADC DC Measurement Control Register 2
0	0	104	0x00	0x00	0x68	Left Channel DC Measurement Output Register 1 (MSB Byte)
0	0	105	0x00	0x00	0x69	Left Channel DC Measurement Output Register 2 (Middle Byte)
0	0	106	0x00	0x00	0x6A	Left Channel DC Measurement Output Register 3 (LSB Byte)
0	0	107	0x00	0x00	0x6B	Right Channel DC Measurement Output Register 1 (MSB Byte)
0	0	108	0x00	0x00	0x6C	Right Channel DC Measurement Output Register 2 (Middle Byte)
0	0	109	0x00	0x00	0x6D	Right Channel DC Measurement Output Register 3 (LSB Byte)
0	0	110-114	0x00	0x00	0x6E-0x72	Reserved Registers
0	0	115	0x00	0x00	0x73	I2C Interface Miscellaneous Control
0	0	116-126	0x00	0x00	0x74-0x7E	Reserved Registers
0	0	127	0x00	0x00	0x7F	Book Selection Register
0	1	0	0x00	0x01	0x00	Page Select Register
0	1	1	0x00	0x01	0x01	Power Configuration Register
0	1	2	0x00	0x01	0x02	Reserved Register
0	1	3	0x00	0x01	0x03	Left DAC PowerTune Configuration Register
0	1	4	0x00	0x01	0x04	Right DAC PowerTune Configuration Register
0	1	5-7	0x00	0x01	0x05-0x07	Reserved Registers
0	1	8	0x00	0x01	0x08	Common Mode Register
0	1	9	0x00	0x01	0x09	Headphone Output Driver Control
0	1	10	0x00	0x01	0x0A	Receiver Output Driver Control
0	1	11	0x00	0x01	0x0B	Headphone Output Driver De-pop Control
0	1	12	0x00	0x01	0x0C	Receiver Output Driver De-Pop Control
0	1	13-16	0x00	0x01	0x0D-0x10	Reserved Registers
0	1	17	0x00	0x01	0x11	Mixer Amplifier Control
0	1	18	0x00	0x01	0x12	Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control
0	1	19	0x00	0x01	0x13	Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control
0	1	20-21	0x00	0x01	0x14-0x15	Reserved Registers
0	1	22	0x00	0x01	0x16	Lineout Amplifier Control 1
0	1	23	0x00	0x01	0x17	Lineout Amplifier Control 2
0	1	24-26	0x00	0x01	0x18-0x1A	Reserved
0	1	27	0x00	0x01	0x1B	Headphone Amplifier Control 1
0	1	28	0x00	0x01	0x1C	Headphone Amplifier Control 2
0	1	29	0x00	0x01	0x1D	Headphone Amplifier Control 3
0	1	30	0x00	0x01	0x1E	Reserved Register
0	1	31	0x00	0x01	0x1F	HPL Driver Volume Control

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Register Maps (continued)

Table 13. Summary of Register Map (continued)

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	1	32	0x00	0x01	0x20	HPR Driver Volume Control
0	1	33	0x00	0x01	0x21	Charge Pump Control 1
0	1	34	0x00	0x01	0x22	Charge Pump Control 2
0	1	35	0x00	0x01	0x23	Charge Pump Control 3
0	1	36	0x00	0x01	0x24	Receiver Amplifier Control 1
0	1	37	0x00	0x01	0x25	Receiver Amplifier Control 2
0	1	38	0x00	0x01	0x26	Receiver Amplifier Control 3
0	1	39	0x00	0x01	0x27	Receiver Amplifier Control 4
0	1	40	0x00	0x01	0x28	Receiver Amplifier Control 5
0	1	41	0x00	0x01	0x29	Receiver Amplifier Control 6
0	1	42	0x00	0x01	0x2A	Receiver Amplifier Control 7
0	1	43-44	0x00	0x01	0x2B-0x2C	Reserved Registers
0	1	45	0x00	0x01	0x2D	Speaker Amplifier Control 1
0	1	46	0x00	0x01	0x2E	Speaker Amplifier Control 2
0	1	47	0x00	0x01	0x2F	Speaker Amplifier Control 3
0	1	48	0x00	0x01	0x30	Speaker Amplifier Volume Controls
0	1	49-50	0x00	0x01	0x31-0x32	Reserved Registers
0	1	51	0x00	0x01	0x33	Microphone Bias Control
0	1	52	0x00	0x01	0x34	Input Select 1 for Left Microphone PGA P-Terminal
0	1	53	0x00	0x01	0x35	Input Select 2 for Left Microphone PGA P-Terminal
0	1	54	0x00	0x01	0x36	Input Select for Left Microphone PGA M-Terminal
0	1	55	0x00	0x01	0x37	Input Select 1 for Right Microphone PGA P-Terminal
0	1	56	0x00	0x01	0x38	Input Select 2 for Right Microphone PGA P-Terminal
0	1	57	0x00	0x01	0x39	Input Select for Right Microphone PGA M-Terminal
0	1	58	0x00	0x01	0x3A	Input Common Mode Control
0	1	59	0x00	0x01	0x3B	Left Microphone PGA Control
0	1	60	0x00	0x01	0x3C	Right Microphone PGA Control
0	1	61	0x00	0x01	0x3D	ADC PowerTune Configuration Register
0	1	62	0x00	0x01	0x3E	ADC Analog PGA Gain Flag Register
0	1	63	0x00	0x01	0x3F	DAC Analog Gain Flags Register 1
0	1	64	0x00	0x01	0x40	DAC Analog Gain Flags Register 2
0	1	65	0x00	0x01	0x41	Analog Bypass Gain Flags Register
0	1	66	0x00	0x01	0x42	Driver Power-Up Flags Register
0	1	67-118	0x00	0x01	0x43-0x76	Reserved Registers
0	1	119	0x00	0x01	0x77	Headset Detection Tuning Register 1
0	1	120	0x00	0x01	0x78	Headset Detection Tuning Register 2
0	1	121	0x00	0x01	0x79	Microphone PGA Power-Up Control Register
0	1	122	0x00	0x01	0x7A	Reference Powerup Delay Register
0	1	123-127	0x00	0x01	0x7B-0x7F	Reserved Registers
0	3	0	0x00	0x03	0x00	Page Select Register
0	3	1	0x00	0x03	0x01	Reserved Register

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Register Maps (continued)

Table 13. Summary of Register Map (continued)

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	3	2	0x00	0x03	0x02	Primary SAR ADC Control
0	3	3	0x00	0x03	0x03	Primary SAR ADC Conversion Mode
0	3	4-5	0x00	0x03	0x04-0x05	Reserved Registers
0	3	6	0x00	0x03	0x06	SAR Reference Control
0	3	7-8	0x00	0x03	0x07-0x08	Reserved Registers
0	3	9	0x00	0x03	0x09	SAR ADC Flags Register 1
0	3	10	0x00	0x03	0x0A	SAR ADC Flags Register 2
0	3	11-12	0x00	0x03	0x0B-0x0C	Reserved Registers
0	3	13	0x00	0x03	0x0D	SAR ADC Buffer Mode Control
0	3	14	0x00	0x03	0x0E	Reserved Register
0	3	15	0x00	0x03	0x0F	Scan Mode Timer Control
0	3	16	0x00	0x03	0x10	Reserved Register
0	3	17	0x00	0x03	0x11	SAR ADC Clock Control
0	3	18	0x00	0x03	0x12	SAR ADC Buffer Mode Data Read Control
0	3	19	0x00	0x03	0x13	SAR ADC Measurement Control
0	3	20	0x00	0x03	0x14	Reserved Register
0	3	21	0x00	0x03	0x15	SAR ADC Measurement Threshold Flags
0	3	22	0x00	0x03	0x16	IN1L Max Threshold Check Control 1
0	3	23	0x00	0x03	0x17	IN1L Max Threshold Check Control 2
0	3	24	0x00	0x03	0x18	IN1L Min Threshold Check Control 1
0	3	25	0x00	0x03	0x19	IN1L Min Threshold Check Control 2
0	3	26	0x00	0x03	0x1A	IN1R Max Threshold Check Control 1
0	3	27	0x00	0x03	0x1B	IN1R Max Threshold Check Control 2
0	3	28	0x00	0x03	0x1C	IN1R Min Threshold Check Control 1
0	3	29	0x00	0x03	0x1D	IN1R Min Threshold Check Control 2
0	3	30	0x00	0x03	0x1E	TEMP Max Threshold Check Control 1
0	3	31	0x00	0x03	0x1F	TEMP Max Threshold Check Control 2
0	3	32	0x00	0x03	0x20	TEMP Min Threshold Check Control 1
0	3	33	0x00	0x03	0x21	TEMP Min Threshold Check Control 2
0	3	34-53	0x00	0x03	0x22-0x35	Reserved Registers
0	3	54	0x00	0x03	0x36	IN1L Measurement Data (MSB)
0	3	55	0x00	0x03	0x37	IN1L Measurement Data (LSB)
0	3	56	0x00	0x03	0x38	IN1R Measurement Data (MSB)
0	3	57	0x00	0x03	0x39	IN1R Measurement Data (LSB)
0	3	58	0x00	0x03	0x3A	VBAT Measurement Data (MSB)
0	3	59	0x00	0x03	0x3B	VBAT Measurement Data (LSB)
0	3	60-65	0x00	0x03	0x3C-0x41	Reserved Registers
0	3	66	0x00	0x03	0x42	TEMP1 Measurement Data (MSB)
0	3	67	0x00	0x03	0x43	TEMP1 Measurement Data (LSB)
0	3	68	0x00	0x03	0x44	TEMP2 Measurement Data (MSB)
0	3	69	0x00	0x03	0x45	TEMP2 Measurement Data (LSB)

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Register Maps (continued)

Table 13. Summary of Register Map (continued)

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	3	70-127	0x00	0x03	0x46-0x7F	Reserved Registers
0	4	0	0x00	0x04	0x00	Page Select Register
0	4	1	0x00	0x04	0x01	Audio Serial Interface 1, Audio Bus Format Control Register
0	4	2	0x00	0x04	0x02	Audio Serial Interface 1, Left Ch_Offset_1 Control Register
0	4	3	0x00	0x04	0x03	Audio Serial Interface 1, Right Ch_Offset_2 Control Register
0	4	4	0x00	0x04	0x04	Audio Serial Interface 1, Channel Setup Register
0	4	5-6	0x00	0x04	0x05-0x06	Reserved Registers
0	4	7	0x00	0x04	0x07	Audio Serial Interface 1, ADC Input Control
0	4	8	0x00	0x04	0x08	Audio Serial Interface 1, DAC Output Control
0	4	9	0x00	0x04	0x09	Audio Serial Interface 1, Control Register 9, ADC Slot Tristate Control
0	4	10	0x00	0x04	0x0A	Audio Serial Interface 1, WCLK and BCLK Control Register
0	4	11	0x00	0x04	0x0B	Audio Serial Interface 1, Bit Clock N Divider Input Control
0	4	12	0x00	0x04	0x0C	Audio Serial Interface 1, Bit Clock N Divider
0	4	13	0x00	0x04	0x0D	Audio Serial Interface 1, Word Clock N Divider
0	4	14	0x00	0x04	0x0E	Audio Serial Interface 1, BCLK and WCLK Output
0	4	15	0x00	0x04	0x0F	Audio Serial Interface 1, Data Output
0	4	16	0x00	0x04	0x10	Audio Serial Interface 1, ADC WCLK and BCLK Control
0	4	17	0x00	0x04	0x11	Audio Serial Interface 2, Audio Bus Format Control Register
0	4	18	0x00	0x04	0x12	Audio Serial Interface 2, Data Offset Control Register
0	4	19-22	0x00	0x04	0x13-0x16	Reserved Registers
0	4	23	0x00	0x04	0x17	Audio Serial Interface 2, ADC Input Control
0	4	24	0x00	0x04	0x18	Audio Serial Interface 2, DAC Output Control
0	4	25	0x00	0x04	0x19	Reserved Register
0	4	26	0x00	0x04	0x1A	Audio Serial Interface 2, WCLK and BCLK Control Register
0	4	27	0x00	0x04	0x1B	Audio Serial Interface 2, Bit Clock N Divider Input Control
0	4	28	0x00	0x04	0x1C	Audio Serial Interface 2, Bit Clock N Divider
0	4	29	0x00	0x04	0x1D	Audio Serial Interface 2, Word Clock N Divider
0	4	30	0x00	0x04	0x1E	Audio Serial Interface 2, BCLK and WCLK Output
0	4	31	0x00	0x04	0x1F	Audio Serial Interface 2, Data Output
0	4	32	0x00	0x04	0x20	Audio Serial Interface 2, ADC WCLK and BCLK Control
0	4	33	0x00	0x04	0x21	Audio Serial Interface 3, Audio Bus Format Control Register
0	4	34	0x00	0x04	0x22	Audio Serial Interface 3, Data Offset Control Register
0	4	35-38	0x00	0x04	0x23-0x26	Reserved Registers
0	4	39	0x00	0x04	0x27	Audio Serial Interface 3, ADC Input Control
0	4	40	0x00	0x04	0x28	Audio Serial Interface 3, DAC Output Control
0	4	41	0x00	0x04	0x29	Reserved Register
0	4	42	0x00	0x04	0x2A	Audio Serial Interface 3, WCLK and BCLK Control Register
0	4	43	0x00	0x04	0x2B	Audio Serial Interface 3, Bit Clock N Divider Input Control
0	4	44	0x00	0x04	0x2C	Audio Serial Interface 3, Bit Clock N Divider
0	4	45	0x00	0x04	0x2D	Audio Serial Interface 3, Word Clock N Divider
0	4	46	0x00	0x04	0x2E	Audio Serial Interface 3, BCLK and WCLK Output

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Register Maps (continued)

Table 13. Summary of Register Map (continued)

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	4	47	0x00	0x04	0x2F	Audio Serial Interface 3, Data Output
0	4	48	0x00	0x04	0x30	Audio Serial Interface 3, ADC WCLK and BCLK Control
0	4	49-64	0x00	0x04	0x31-0x40	Reserved Registers
0	4	65	0x00	0x04	0x41	WCLK1 (Input/Output) Pin Control
0	4	66	0x00	0x04	0x42	Reserved Register
0	4	67	0x00	0x04	0x43	DOUT1 (Output) Pin Control
0	4	68	0x00	0x04	0x44	DIN1 (Input) Pin Control
0	4	69	0x00	0x04	0x45	WCLK2 (Input/Output) Pin Control
0	4	70	0x00	0x04	0x46	BCLK2 (Input/Output) Pin Control
0	4	71	0x00	0x04	0x47	DOUT2 (Output) Pin Control
0	4	72	0x00	0x04	0x48	DIN2 (Input) Pin Control
0	4	73	0x00	0x04	0x49	WCLK3 (Input/Output) Pin Control
0	4	74	0x00	0x04	0x4A	BCLK3 (Input/Output) Pin Control
0	4	75	0x00	0x04	0x4B	DOUT3 (Output) Pin Control
0	4	76	0x00	0x04	0x4C	DIN3 (Input) Pin Control
0	4	77-81	0x00	0x04	0x4D-0x51	Reserved Registers
0	4	82	0x00	0x04	0x52	MCLK2 (Input) Pin Control
0	4	83-85	0x00	0x04	0x53-0x55	Reserved Registers
0	4	86	0x00	0x04	0x56	GPIO1 (Input/Output) Pin Control
0	4	87	0x00	0x04	0x57	GPIO2 (Input/Output) Pin Control
0	4	88-90	0x00	0x04	0x58-0x5A	Reserved Registers
0	4	91	0x00	0x04	0x5B	GPI1 (Input) Pin Control
0	4	92	0x00	0x04	0x5C	GPI2 (Input) Pin Control
0	4	93-95	0x00	0x04	0x5D-0x5F	Reserved Registers
0	4	96	0x00	0x04	0x60	GPO1 (Output) Pin Control
0	4	97-100	0x00	0x04	0x61-0x64	Reserved Registers
0	4	101	0x00	0x04	0x65	Digital Microphone Input Pin Control
0	4	102-117	0x00	0x04	0x66-0x75	Reserved Registers
0	4	118	0x00	0x04	0x76	ADC/DAC Data Port Control
0	4	119	0x00	0x04	0x77	Digital Audio Engine Synchronization Control
0	4	120-127	0x00	0x04	0x78-0x7F	Reserved Registers
0	252	0	0x00	0xFC	0x00	Page Select Register
0	252	1	0x00	0xFC	0x01	SAR Buffer Mode Data (MSB) and Buffer Flags
0	252	2	0x00	0xFC	0x02	SAR Buffer Mode Data (LSB)
0	252	3-127	0x00	0xFC	0x03-0x7F	Reserved Registers
40	0	0	0x28	0x00	0x00	Page Select Register
40	0	1	0x28	0x00	0x01	ADC Adaptive CRAM Configuration Register

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Register Maps (continued)

Table 13. Summary of Register Map (continued)

DECIMAL			HEX			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
40	0	2-126	0x28	0x00	0x02-0x7E	Reserved Registers
40	0	127	0x28	0x00	0x7F	Book Selection Register
40	1-17	0	0x28	0x01-0x11	0x00	Page Select Register
40	1-17	1-7	0x28	0x01-0x11	0x01-0x07	Reserved Registers
40	1-17	8-127	0x28	0x01-0x11	0x08-0x7F	ADC Adaptive Coefficients C(0:509)
40	18	0	0x28	0x12	0x00	Page Select Register
40	18	1-7	0x28	0x12	0x01-0x07	Reserved Registers
40	18	8-15	0x28	0x12	0x08-0x0F	ADC Adaptive Coefficients C(510:511)
40	18	16-127	0x28	0x12	0x10-0x7F	Reserved Registers
80	0	0	0x50	0x00	0x00	Page Select Register
80	0	1	0x50	0x00	0x01	DAC Adaptive Coefficient Bank Configuration Register
80	0	2-126	0x50	0x00	0x02-0x7E	Reserved Registers
80	0	127	0x50	0x00	0x7F	Book Selection Register
80	1-17	0	0x50	0x01-0x11	0x00	Page Select Register
80	1-17	1-7	0x50	0x01-0x11	0x01-0x07	Reserved Registers
80	1-17	8-127	0x50	0x01-0x11	0x08-0x7F	DAC Adaptive Coefficient Bank C(0:509)
80	18	0	0x50	0x12	0x00	Page Select Register
80	18	1-7	0x50	0x12	0x01-0x07	Reserved Registers
80	18	8-15	0x50	0x12	0x08-0x0F	DAC Adaptive Coefficient Bank C(510:511)
80	18	16-127	0x50	0x12	0x10-0x7F	Reserved Registers

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11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in all available modes of operation. Additionally, some of the application circuits are available as reference designs and can be found on the TI website. Also see the TLV320AIC3212 product page for information on ordering the EVM. Not all configurations are available as reference designs; however, any design variation can be supported by TI through schematic and layout reviews. Visit support.ti.com for additional design assistance. Also, join the audio converters discussion forum at http://e2e.ti.com.

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11.2 Typical Application

Figure 33 shows a typical circuit configuration for a system utilizing TLV320AIC3212. Note that while this circuit configuration shows all three Audio Serial Interfaces connected to a single Host Processor, it is also quite common for these Audio Serial Interfaces to connect to separate devices (for example, Host Processor on Audio Serial Interface number 1, and modems and/or Bluetooth devices on the other audio serial interfaces).

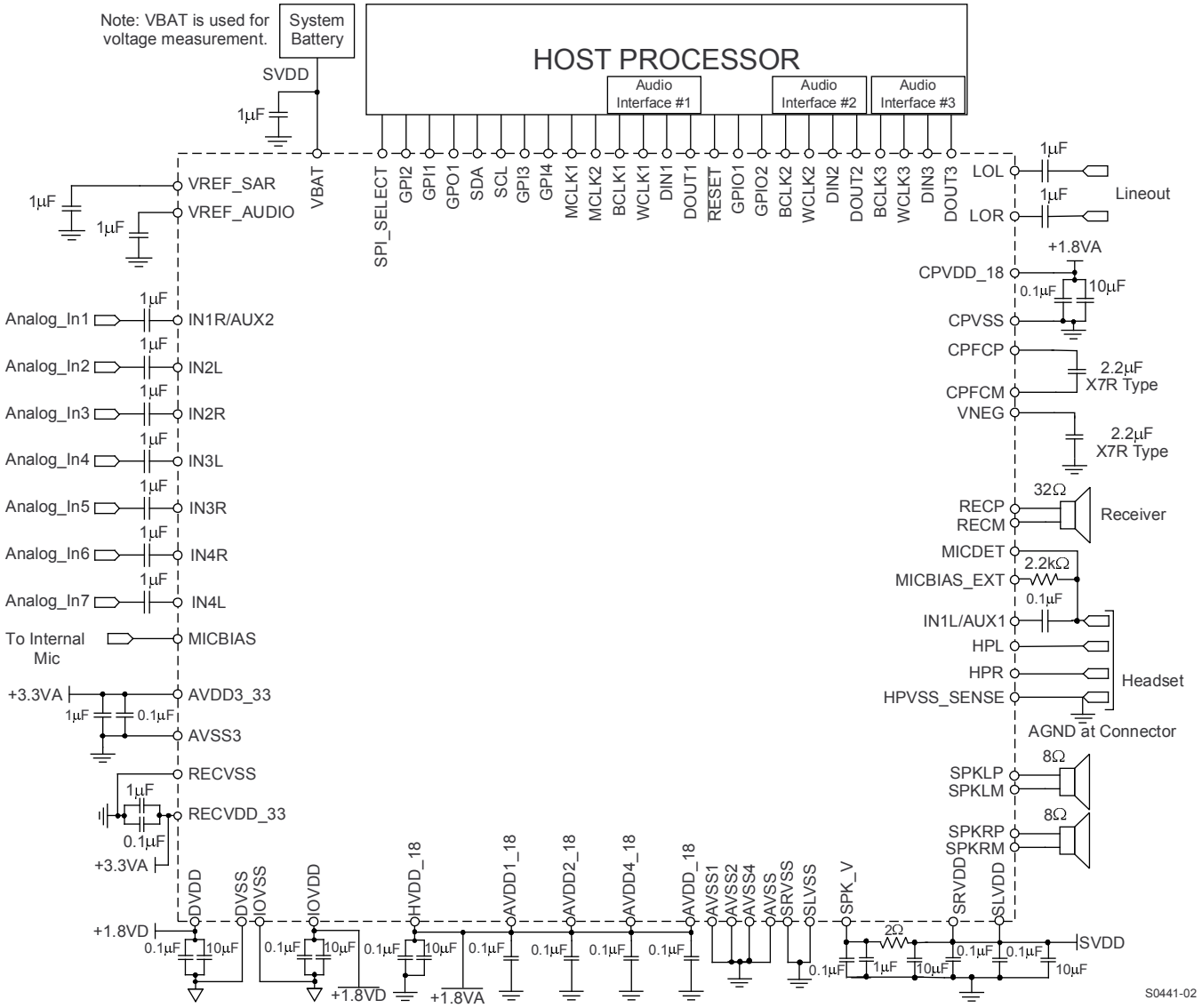


Figure 33. Typical Circuit Configuration

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Typical Application (continued)

11.2.1 Design Requirements

This section gives the power-consumption values for various PowerTune modes. All measurements were taken with the PLL turned off and the ADC configured for single-ended input.

Table 14. ADC, Stereo, 48 kHz, Highest Performance, DVDD = IOVDD = 1.8 V, AVDDx_18 = 1.8 V(1)

	DEVICE COMMON MODE SETTING = 0.75 V				DEVICE COMMON MODE SETTING = 0.9 V				UNIT
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	
0 dB full scale	X	375	375	375	X	500	500	500	mV_{RMS}
Maximum allowed input level w.r.t. 0 dB full scale	X	–12	0	0	X	–12	0	0	dB full scale
Effective SNR w.r.t. maximum allowed input level	X	78.2	91.2	91	X	79.5	93.1	93	dB
Power consumption	X	12.3	14.6	18.8	X	12.3	14.6	18.8	mW

(1) AOSR = 128, Processing Block = PRB_R1 (Decimation Filter A)

Table 15. Alternative Processing Blocks

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_R2	A	+1.2
PRB_R3	A	+0.8

Table 16. ADC, Stereo, 48 kHz, Lowest Power Consumption(1)

	PTM_R1 CM = 0.75 V AVdd = 1.5 V	PTM_R3 CM = 0.9 V AVdd = 1.8 V	UNIT
0 dB full scale	375	500	mV_{RMS}
Maximum allowed input level w.r.t. 0 dB full scale	–2	0	dB full scale
Effective SNR w.r.t. maximum allowed input level	85.9	90.8	dB
Power consumption	5.6	9.5	mW

(1) AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B), DVdd = 1.26 V

Table 17. Alternative Processing Blocks

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_R8	B	+0.4
PRB_R9	B	+0.2
PRB_R1	A	+1.2
PRB_R2	A	+1.8
PRB_R3	A	+1.6

Table 18. DAC, Stereo, 48 kHz, Highest Performance, DVDD = IOVDD = 1.8 V, AVDDx_18 = 1.8 V(1)

		DEVICE COMMON MODE SETTING = 0.75 V				DEVICE COMMON MODE SETTING = 0.9 V				UNIT
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	
0 dB full scale		75	225	375	375	100	300	500	500	mV_{RMS}
Line out	Effective SNR w.r.t. 0 dB full scale	89.5	96.3	99.3	99.2	91.7	98.4	101.2	101.2	dB
	Power consumption	11.3	11.9	12.4	12.4	11.5	12.2	12.9	12.9	mW

(1) DOSR = 128, Processing Block = PRB_P8 (Interpolation Filter B)

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Table 19. Alternative Processing Blocks

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P1	A	–0.1
PRB_P2	A	+2.6
PRB_P3	A	+1.1
PRB_P7	B	–2.8
PRB_P9	B	–1.7
PRB_P10	B	+0.6
PRB_P11	B	–1.2
PRB_P23	A	–0.1
PRB_P24	A	+2.8
PRB_P25	A	+3.6

Table 20. DAC, Stereo, 48 kHz, Lowest Power Consumption(1)

		CM = 0.75 V AVdd = 1.5 V PRB_P26 PTM_P1	CM = 0.9 V AVdd = 1.8 V PRB_P26 PTM_P1	CM = 0.75 V AVdd = 1.5 V PRB_P7 PTM_P4	UNIT
0 dB full scale		75	100	375	mV_{RMS}
Line out	Effective SNR w.r.t. 0 dB full scale	88.6	90.7	99.2	dB
	Power consumption	2.7	3.3	5.2	mW

(1) DOSR = 64, Interpolation Filter D, DVdd = 1.26 V

Table 21. Alternative Processing Blocks

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)(1)
PRB_P1	A	+3.1
PRB_P2	A	+4.4
PRB_P3	A	+3.6
PRB_P7	B	+1.7
PRB_P9	B	+2.3
PRB_P10	B	+3.4
PRB_P11	B	+2.5
PRB_P23	A	+3.1
PRB_P24	A	+4.5
PRB_P25	A	+4.8

(1) Estimated power change is w.r.t. PRB_P26.

For more possible configurations and measurements, please consult the *TLV320AIC3212 Application Reference Guide*.

11.2.2 Detailed Design Procedure

For more detailed information see the TLV320AIC3212 *Application Reference Guide*, SLAU360.

11.2.2.1 Charge Pump Flying and Holding Capacitor

The TLV320AIC3212 features a built in charge-pump to generate a negative supply rail, VNEG from CPVDD_18. The negative voltage is used by the headphone amplifier to enable driving the output signal biased around ground potential. For proper operation of the charge pump and headphone amplifier, it is recommended that the flying capacitor connected between CPFCP and CPFCM terminals and the holding capacitor connected between VNEG and ground be of X7R type. It is recommended to use 2.2µF as capacitor value. Failure to use X7R type capacitor can result in degraded performance of charge pump and headphone amplifier.

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11.2.2.2 Reference Filtering Capacitor

The TLV320AIC3212 has a built-in bandgap used to generate reference voltages and currents for the device. To achieve high SNR, the reference voltage on VREF_AUDIO should be filtered using a 10µF capacitor from VREF_AUDIO terminal to ground.

11.2.2.3 MICBIAS

TLV320AIC3212 has a built-in bias voltage output for biasing of microphones. No intentional capacitors should be connected directly to the MICBIAS output for filtering.

11.2.3 Application Curves

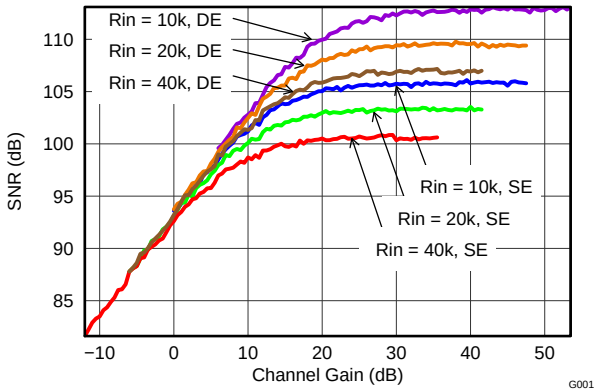


Figure 34. ADC SNR vs Channel Gain Input-Referred

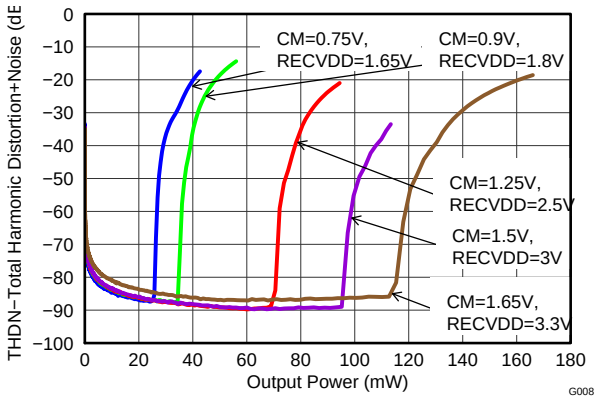


Figure 35. Total Harmonic Distortion+Noise vs Differential Receiver Output Power 32-Ω Load

12 Power Supply Recommendations

The TLV320AIC3212 integrates a large amount of digital and analog functionality, and each of these blocks can be powered separately to enable the system to select appropriate power supplies for desired performance and power consumption. The device has separate power domains for digital IO, digital core, analog core, analog input, receiver driver, charge-pump input, headphone driver, and speaker drivers. If desired, all of the supplies (except for the supplies for speaker drivers, which can directly connect to the battery) can be connected together and be supplied from one source in the range of 1.65 V to 1.95 V. Individually, the IOVDD voltage can be supplied in the range of 1.1 V to 3.6 V. For improved power efficiency, the digital core power supply can range from 1.26 V to 1.95 V. The analog core voltages (AVDD1_18, AVDD2_18, AVDD4_18, and AVDD_18) can range from 1.5 V to 1.95 V. The microphone bias (AVDD3_33) and receiver driver supply (RECVDD_33) voltages can range from 1.65 V to 3.6 V. The charge-pump input voltage (CPVDD_18) can range from 1.26 V to 1.95 V, and the headphone driver supply (HVDD_18) voltage can range from 1.5 V to 1.95 V. The speaker driver voltages (SLVDD, SRVDD, and SPK_V) can range from 2.7 V to 5.5 V.

For more detailed information see the *Application Reference Guide*, SLAU360.

13 Layout

13.1 Layout Guidelines

Each system design and PCB layout is unique. The layout should be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize TLV320AIC3212 performance:

- The decoupling capacitors for the power supplies should be placed close to the device terminals. Figure 33 shows the recommended decoupling capacitors for the TLV320AIC3212.
- Place the flying capacitor between CPFCP and CPFCM near the device terminals, with minimal VIAS in the trace between the device terminals and the capacitor. Similarly, keep the decoupling capacitor on VNEG near the device terminal with minimal VIAS in the trace between the device terminal, capacitor, and PCB ground.
- TLV320AIC3212 internal voltage references must be filtered using external capacitors. Place the filter capacitors on VREF_SAR and VREF_AUDIO near the device terminals for optimal performance.
- For analog differential audio signals, the signals should be routed differentially on the PCB for better noise immunity. Avoid crossing of digital and analog signals to avoid undesirable crosstalk.
- Analog, speaker and digital grounds should be separated to prevent possible digital noise from affecting the analog performance of the board.

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13.2 Layout Examples

Figure 36, Figure 37, and Figure 38 show some recommendations that must be followed to ensure the best performance of the device. See the *TLV320AIC3212EVM* (SLAU435) for details.

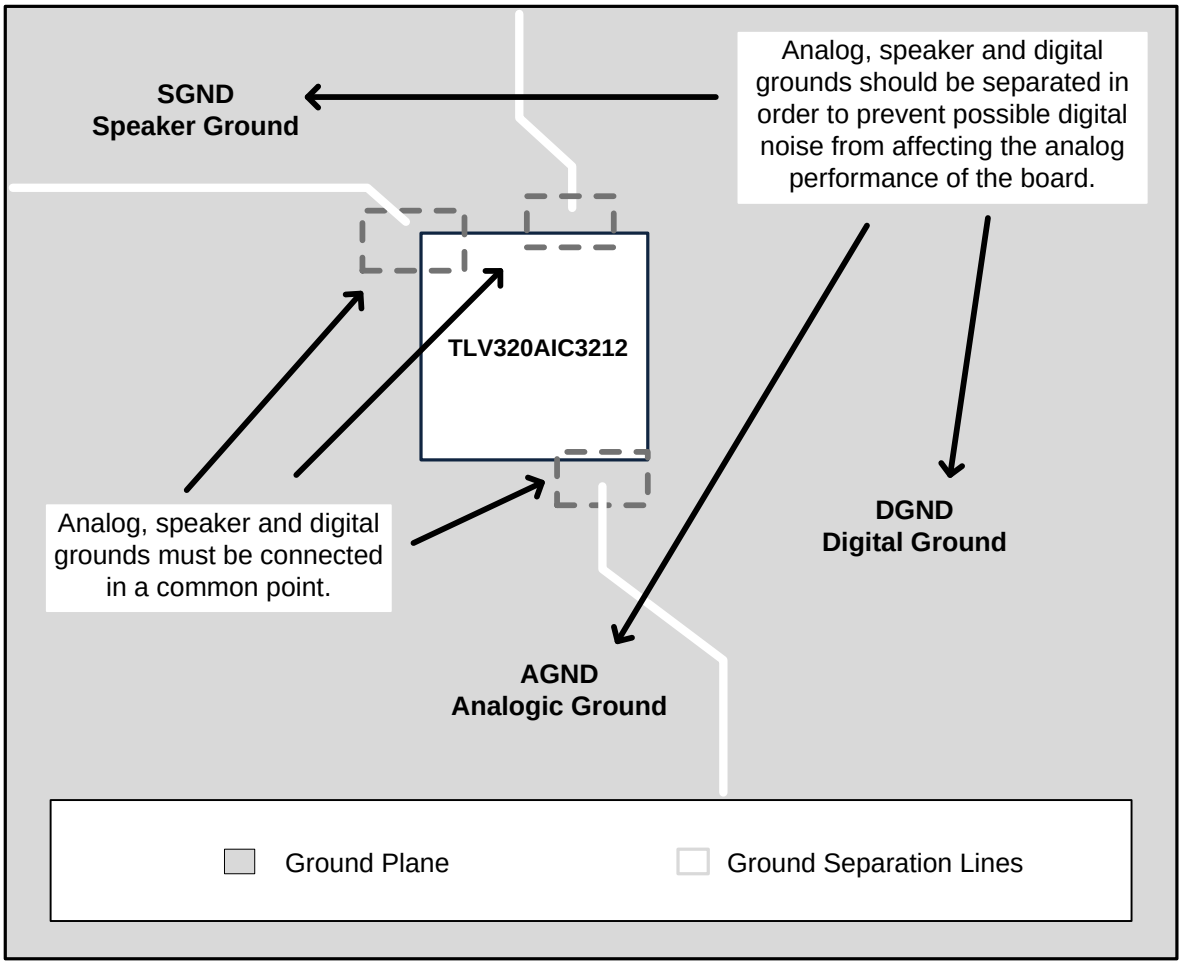


Figure 36. Ground Layer

Layout Examples (continued)

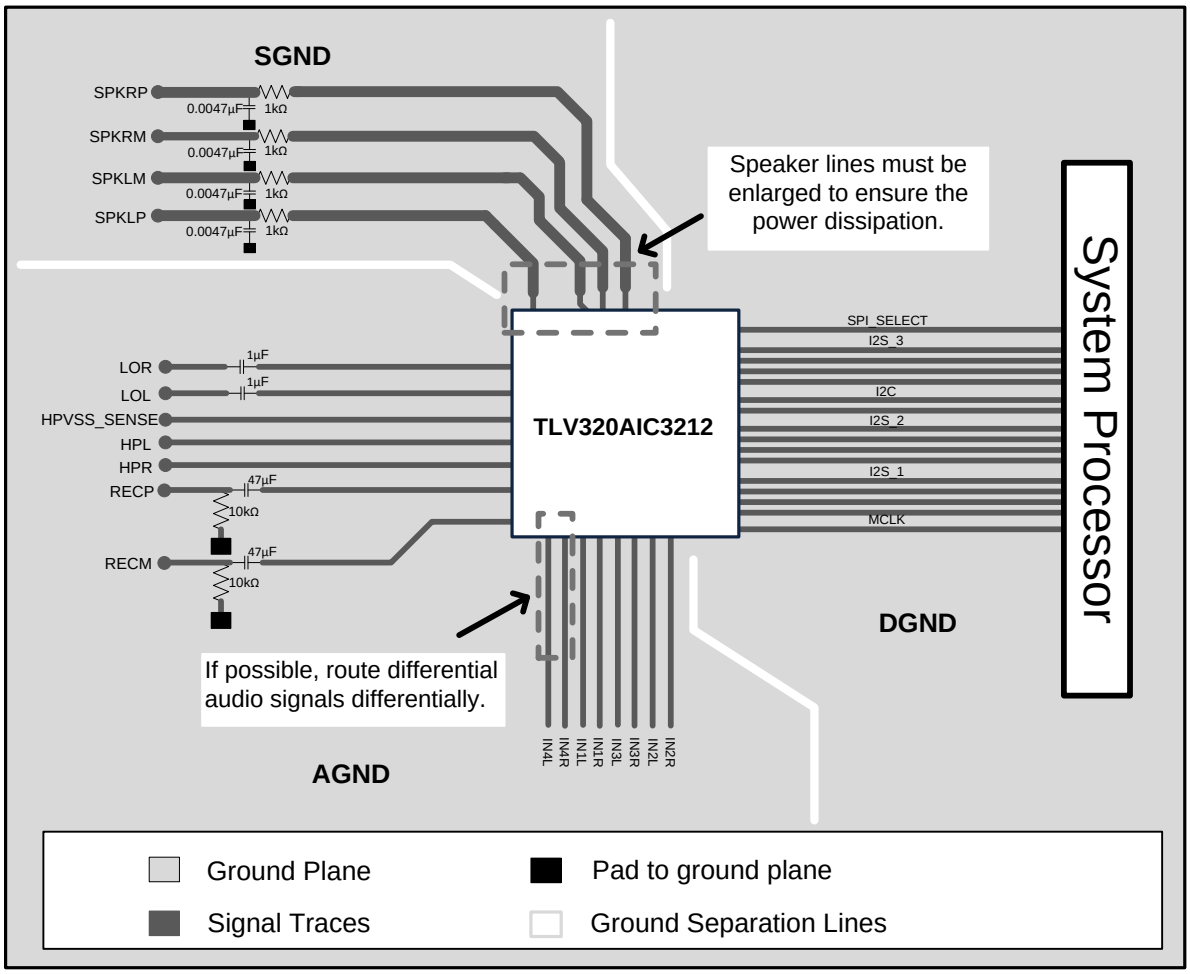


Figure 37. I/O Layer

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Layout Examples (continued)

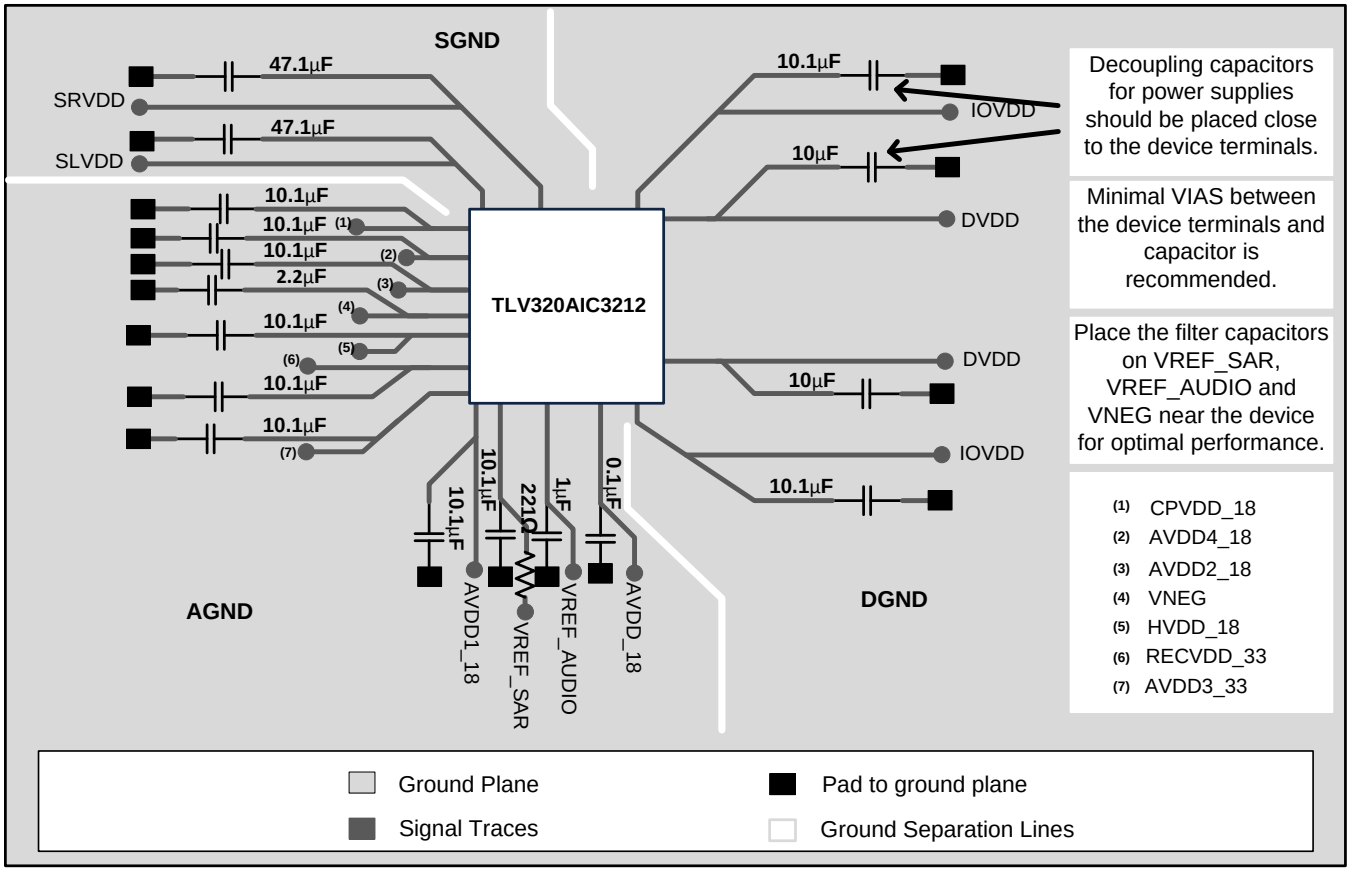


Figure 38. Power Layer

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

For related documentation, see the following:

- *Application Reference Guide*, SLAU360
- *TLV320AIC3212EVM-U Evaluation Module* , SLAU435

14.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.3 Trademarks

DirectPath, PowerTune, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV320AIC3212IYZFR	Active	Production	DSBGA (YZF) | 81	2500 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIC3212
TLV320AIC3212IYZFR.A	Active	Production	DSBGA (YZF) | 81	2500 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIC3212
TLV320AIC3212IYZFT	Active	Production	DSBGA (YZF) | 81	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIC3212
TLV320AIC3212IYZFT.A	Active	Production	DSBGA (YZF) | 81	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIC3212

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

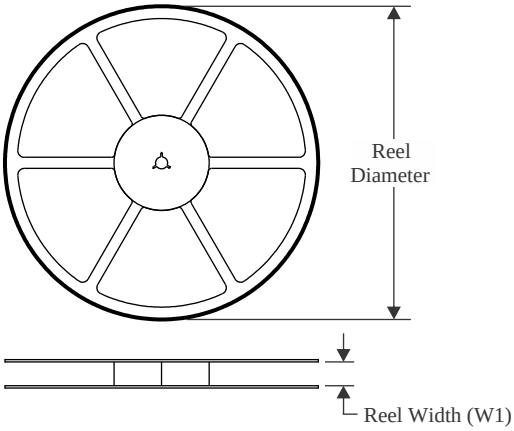
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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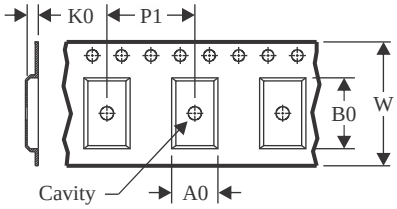
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

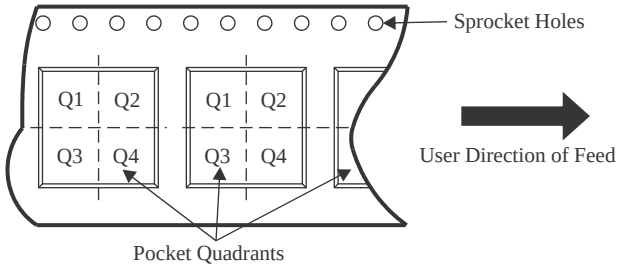


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

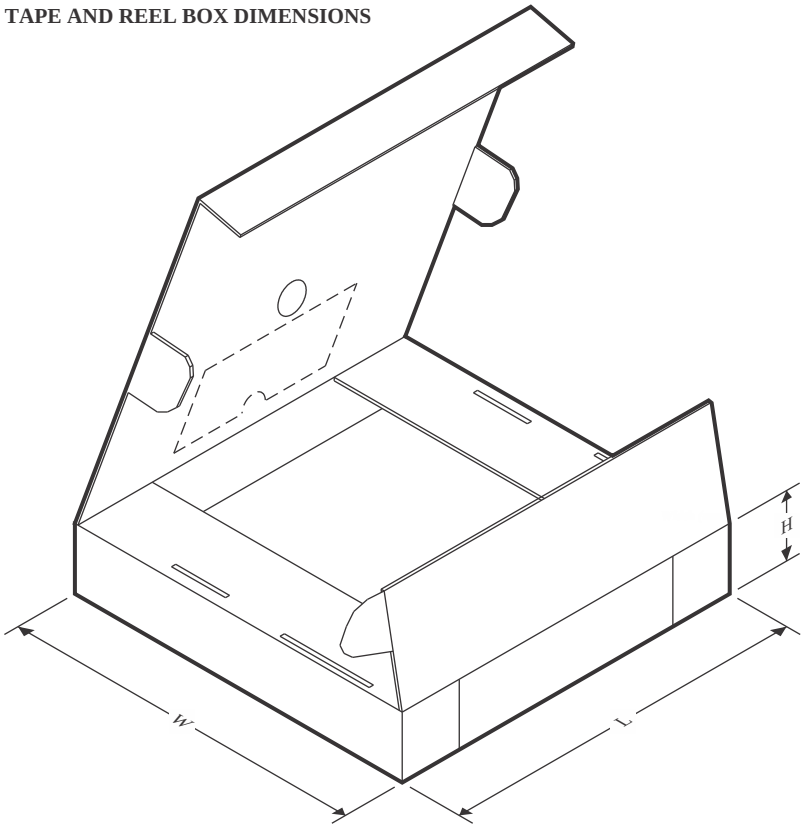
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3212IYZFR	DSBGA	YZF	81	2500	330.0	12.4	5.04	5.07	0.75	8.0	12.0	Q1
TLV320AIC3212IYZFT	DSBGA	YZF	81	250	330.0	12.4	5.04	5.07	0.75	8.0	12.0	Q1

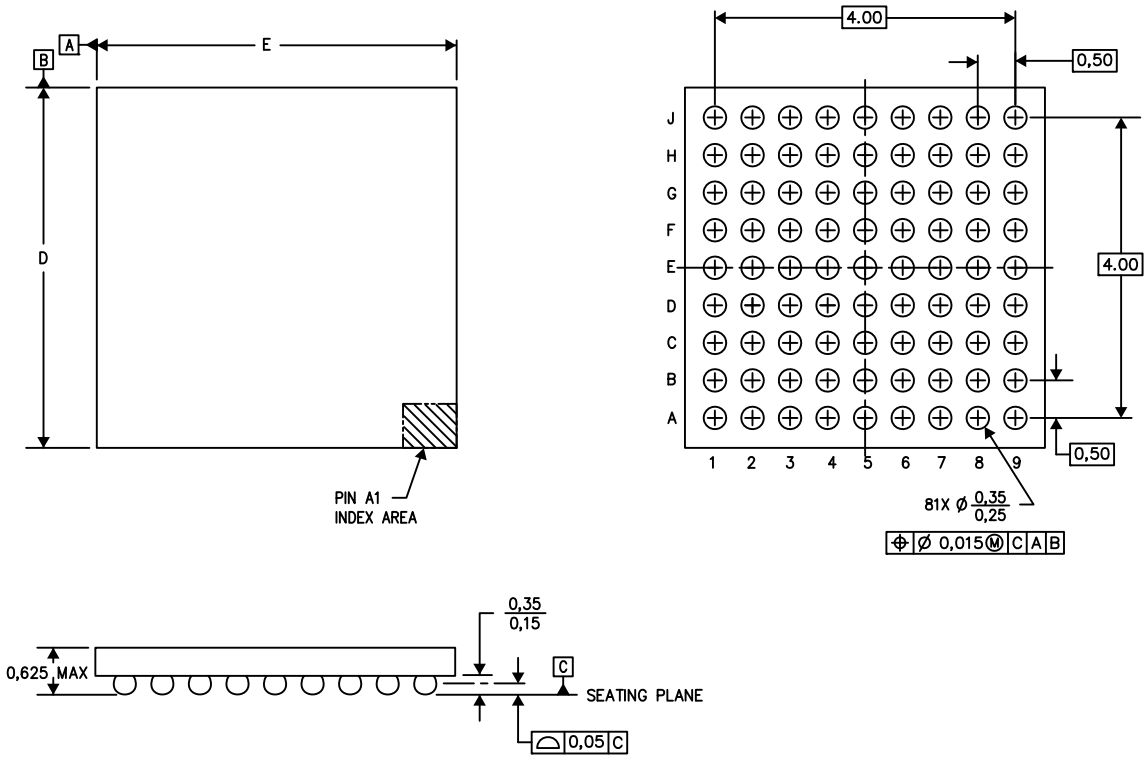
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3212IYZFR	DSBGA	YZF	81	2500	335.0	335.0	25.0
TLV320AIC3212IYZFT	DSBGA	YZF	81	250	335.0	335.0	25.0

YZF (R–XBGA–N81) DIE–SIZE BALL GRID ARRAY



D: Max = 4.84 mm, Min = 4.78 mm

E: Max = 4.84 mm, Min = 4.78 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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