

TLV2711 Advanced, Rail-to-Rail, Micropower, Single, LinCMOS™ Operational Amplifier

1 Features

- Output swing includes both supply rails
- Low noise: $50\text{nV}/\sqrt{\text{Hz}}$ (typ at $f = 1\text{kHz}$)
- Low input bias current: 1pA (typ)
- Very low power: $11\mu\text{A}$ per channel (typ)
- Common-mode input voltage range includes negative rail
- Wide supply voltage range: 2.7V to 10V
- Available in the SOT-23 package

2 Description

The TLV2711 is a single low-voltage operational amplifier available in a 5-pin SOT-23 package. This device consumes only $11\mu\text{A}$ (typ) of supply current, which is useful for battery-powered applications. Looking at the following plot, the TLV2711 has a 3V noise level of $50\text{nV}/\sqrt{\text{Hz}}$ at 1kHz . The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications.

The TLV2711, exhibiting high input impedance and low noise, is an excellent choice for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. As a result of the micropower dissipation levels combined with the 3V operation, these devices work well in hand-held monitoring and remote-sensing applications.

In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of 5.6mm^2 , the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pickup from long PCB traces.

Package Information

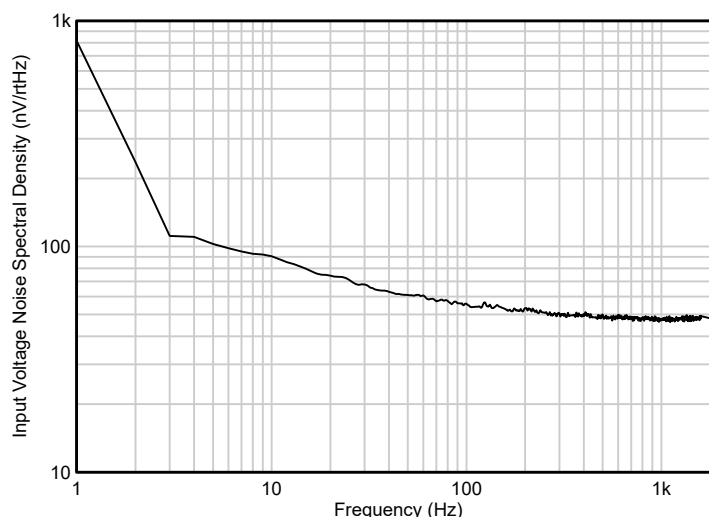
PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TLV2711	DBV (SOT-23, 5)	$2.9\text{mm} \times 2.8\text{mm}$

- (1) For all available packages, see [Section 9](#).
 (2) The package size (length $\times$ width) is a nominal value and includes pins, where applicable.

Device Information

T_A	$V_{IO\text{max}}$ AT 25°C	PACKAGED DEVICES	SYMBOL
		SOT-23 (DBV) ⁽¹⁾	
0°C to 70°C	3mV	TLV2711CDBV	VAJC
-40°C to $+85^\circ\text{C}$	3mV	TLV2711IDBV	VAJI

- (1) DBV package available in tape and reel only.



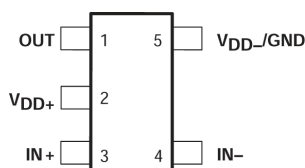
Equivalent Input Noise Voltage vs Frequency



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3 Pin Configuration and Functions



DBV Package (Top View)

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage ⁽²⁾		12	V
V _{ID}	Differential input voltage ⁽³⁾		±V _{DD}	V
V _I	Input voltage range (any input) ⁽²⁾	–0.3	V _{DD}	V
I _I	Input current (each input)		±5	mA
	Duration of short-circuit current at (or less than) 25°C ⁽⁴⁾	Unlimited		
	Continuous total power dissipation	See Dissipation Rating Table		
T _A	Operating free-air temperature range	TLV2711C	0	°C
		TLV2711I	–40	
T _{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package		260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to V_{DD–}.
- (3) Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below V_{DD–} – 0.3 V.
- (4) Short-circuit to ground. Limit temperature, supply voltages, or both to not exceed the maximum dissipation rating.

4.2 Dissipation Rating Table

PACKAGE	T _A ≤ 25 °C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70 °C POWER RATING	T _A = 85 °C POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

4.3 Recommended Operating Conditions

		TLV2711C		TLV2711I		UNIT
		MIN	MAX	MIN	MAX	
V _{DD}	Supply voltage ⁽¹⁾	2.7	10	2.7	10	V
V _I	Input voltage	V _{DD–}	V _{DD+} – 1.3	V _{DD–}	V _{DD+} – 1.3	V
V _{IC}	Common-mode input voltage	V _{DD–}	V _{DD+} – 1.3	V _{DD–}	V _{DD+} – 1.3	V
T _A	Operating free-air temperature	0	70	–40	85	°C

- (1) All voltage values, except differential voltages, are with respect to V_{DD–}.

4.4 Electrical Characteristics, $V_{DD} = 3\text{ V}$

at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A ⁽¹⁾	TLV2711C		TLV2711I		UNIT		
					MIN	TYP	MAX	MIN		TYP	MAX
V _{IO}	Input offset voltage	V _{DD} ± ± 1.5 V, V _O = 0 V, V _{IC} = 0 V, R _S = 50 Ω		Full range	0.4		3	0.4		3	mV
α _{VIO}	Temperature coefficient of input offset voltage				1		1		μV/°C		
I _{IO}	Input offset current ⁽²⁾			25°C	0.5		60	0.5		60	pA
I _{IB}	Input bias current ⁽²⁾			Full range	150		150				
				25°C	60		60				
V _{ICR}	Common-mode input voltage range			Full range	1		150	1		150	
		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V		
V _{OH}	High-level output voltage	I _{OH} = −100 μA		25°C	2.94		2.94			V	
		I _{OH} = −250 μA		25°C	2.85		2.85				
				Full range	2.6		2.6				
V _{OL}	Low-level output voltage	V _{IC} = 1.5 V, I _{OL} = 50 μA		25°C	15		15		mV		
		V _{IC} = 1.5 V, I _{OL} = 500 μA		25°C	150		150				
				Full range	500		500				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 1.5 V, V _O = 1 V to 2 V	R _L = 10 kΩ ⁽³⁾	25°C	3	7	3	7	V/mV		
				Full range	1		1				
			R _L = 1 MΩ ⁽³⁾	25°C	600		600				
r _{i(d)}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
C _{i(c)}	Common-mode input capacitance	f = 10 kHz		25°C	5		5		pF		
z _O	Open-loop output impedance	f = 7 kHz, A _V = 1		25°C	5		5		kΩ		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 1.7 V, R _S = 50 Ω V _O = 1.5 V		25°C	59	83	59	83	dB		
				Full range	58		58				
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 2.7 V to 8 V, no load V _{IC} = V _{DD} / 2,		25°C	70	95	70	95	dB		
				Full range	70		70				
I _{DD}	Supply current	V _O = 1.5 V, no load		25°C	11	25	11	25	μA		
				Full range	30		30				

(1) Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is –40°C to +85°C.

(2) Specified by characterization.

(3) Referenced to 1.5 V.

4.5 Operating Characteristics, $V_{DD} = 3\text{ V}$

at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A ⁽¹⁾	TLV2711C			TLV2711I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.1\text{ V to }1.9\text{ V}$, $R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C	0.01	0.025		0.01	0.025		V/ μ s
			Full range	0.005			0.005			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		80			80		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C		50			50		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		660			660		nV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		880			880		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C		56			56		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C		7			7		kHz
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C		56°			56°		
			25°C		20			20		
	Gain margin		25°C		20			20		dB

(1) Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is – 40°C to +85°C.

(2) Referenced to 1.5 V.

4.6 Electrical Characteristics, $V_{DD} = 5\text{ V}$

at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A ⁽¹⁾	TLV2711C			TLV2711I			UNIT		
					MIN	TYP	MAX	MIN	TYP	MAX			
V _{IO}	Input offset voltage	V _{DD} ± = ±2.5 V, V _O = 0 V, V _{IC} = 0 V, R _S = 50 Ω		Full range	0.45		3	0.45		3	mV		
α _{VIO}	Temperature coefficient of input offset voltage				0.5		0.5		μV/°C				
I _{IO}	Input offset current ⁽²⁾			25°C	0.5		60	0.5		60	pA		
				Full range			150	150					
I _{IB}	Input bias current ⁽²⁾			25°C	1		60	1		60	pA		
				Full range			150	150					
V _{ICR}	Common-mode input voltage range	V _{IO} ≤ 5 mV, R _S = 50 Ω		25°C	0 to 4		-0.3 to 4.2		0 to 4		-0.3 to 4.2		V
				Full range	0 to 3.5				0 to 3.5				
V _{OH}	High-level output voltage	I _{OH} = -100 μA		25°C	4.95				4.95		V		
		I _{OH} = 250 μA		25°C	4.875				4.875				
				Full range	4.6				4.6				
V _{O L}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA		25°C	12				12		mV		
		V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	120				120				
				Full range	500				500				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 10 kΩ ⁽³⁾	25°C	6	12			6	12	V/mV		
			R _L = 1 MΩ ⁽³⁾	Full range	3				3				
				25°C	800				800				

4.6 Electrical Characteristics, $V_{DD} = 5\text{ V}$ (continued)

at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A ⁽¹⁾	TLV2711C			TLV2711I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$r_{i(d)}$	Differential input resistance		25°C		10 ¹²			10 ¹²		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10 ¹²			10 ¹²		Ω
$C_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$	25°C		5			5		pF
Z_O	Open-loop output impedance	$f = 7\text{ kHz}$, $A_V = 1$	25°C		5			5		k Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $R_S = 50\text{ }\Omega$, $V_O = 2.5\text{ V}$	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, no load, $V_{IC} = V_{DD}/2$	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5\text{ V}$, no load	25°C		13	25		13	25	μA
			Full range			30			30	

(1) Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is –40°C to +85°C.

(2) Specified by characterization.

(3) Referenced to 2.5 V.

4.7 Operating Characteristics, $V_{DD} = 5\text{ V}$

at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A ⁽¹⁾	TLV2711C			TLV2711I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}$, $R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C	0.01	0.025		0.01	0.025		V/ μs
			Full range	0.005			0.005			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		72			72		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C		50			50		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		600			600		nV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		800			800		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C		65			65		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C		7			7		kHz
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ ⁽²⁾ , $C_L = 100\text{ pF}$ ⁽²⁾	25°C		60°			60°		
	Gain margin		25°C		22			22		dB

(1) Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is –40°C to +85°C.

(2) Referenced to 2.5 V.

5 Typical Characteristics

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

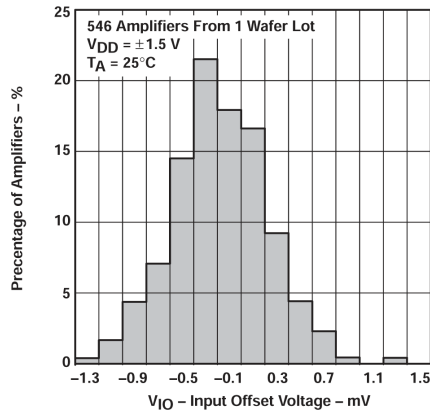


Figure 5-1. Distribution of TLV2711 Input Offset Voltage

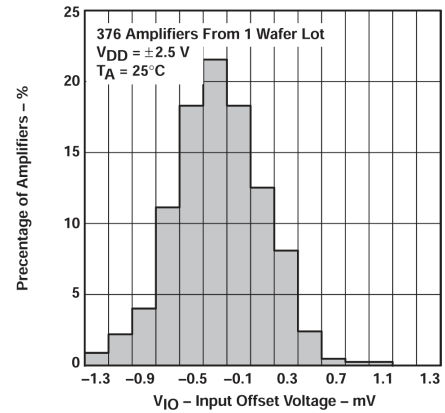


Figure 5-2. Distribution of TLV2711 Input Offset Voltage

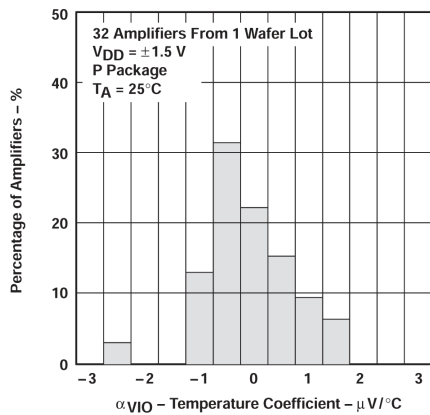


Figure 5-3. Distribution of TLV2711 Input Offset Voltage Temperature Coefficient

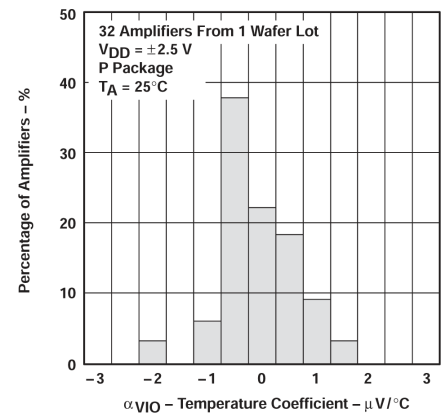


Figure 5-4. Distribution of TLV2711 Input Offset Voltage Temperature Coefficient

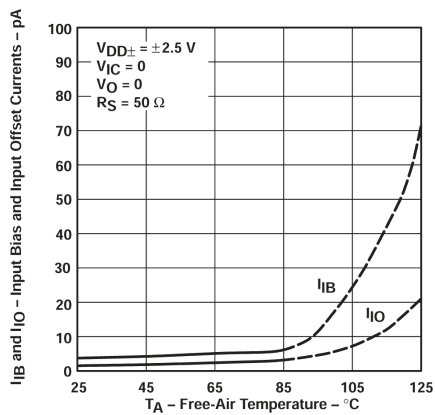


Figure 5-5. Input Bias and Input Offset Currents vs Free-Air Temperature

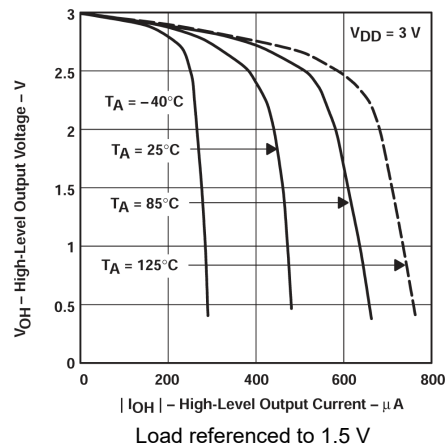


Figure 5-6. High-Level Output Voltage vs High-Level Output Current

5 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

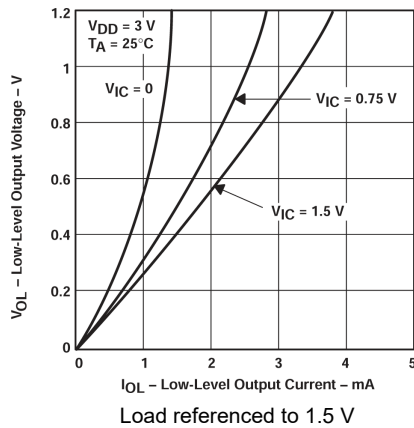


Figure 5-7. Low-Level Output Voltage vs Low-Level Output Current

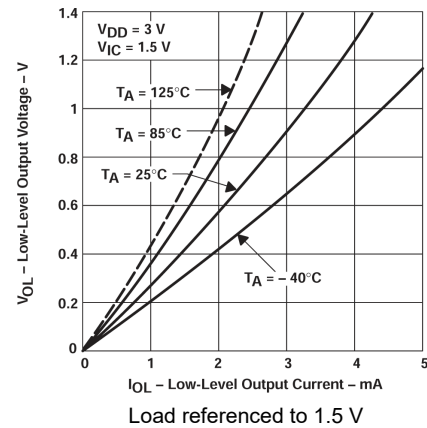


Figure 5-8. Low-Level Output Voltage vs Low-Level Output Current

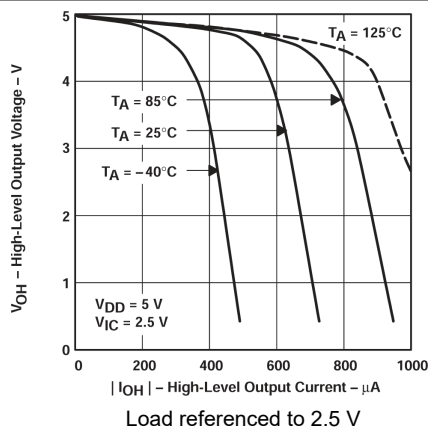


Figure 5-9. High-Level Output Voltage vs High-Level Output Current

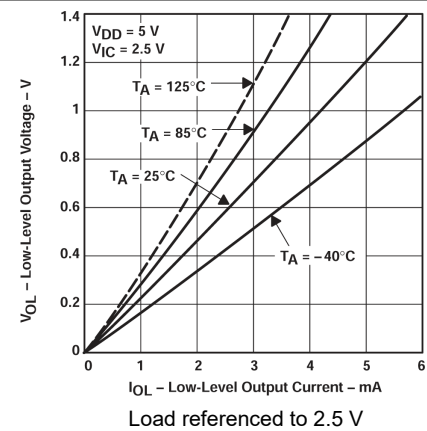
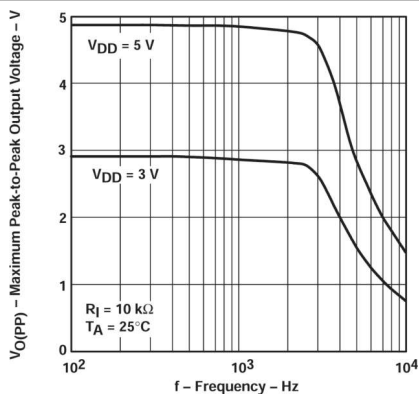


Figure 5-10. Low-Level Output Voltage vs Low-Level Output Current



For $V_{DD} = 3\text{ V}$, load referenced to 1.5 V,
for $V_{DD} = 5\text{ V}$, load referenced to 2.5 V

Figure 5-11. Maximum Peak-to-Peak Output Voltage vs Frequency

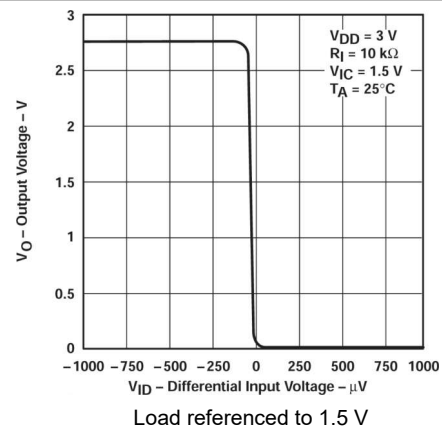


Figure 5-12. Output Voltage vs Differential Input Voltage

5 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

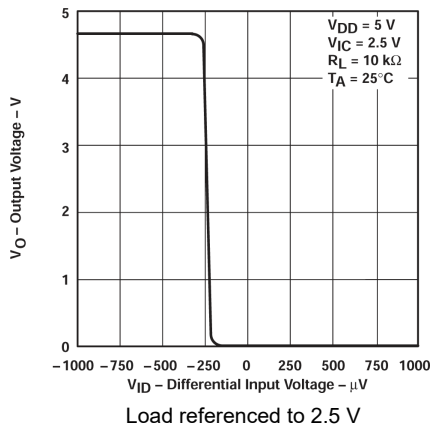


Figure 5-13. Output Voltage vs Differential Input Voltage

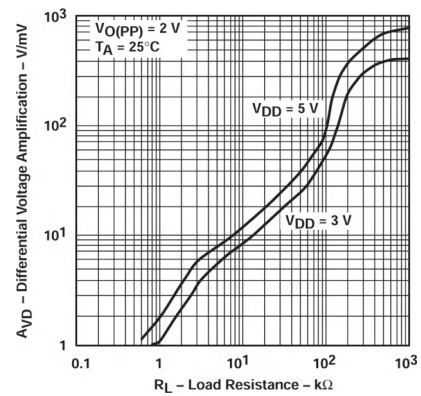


Figure 5-14. Differential Voltage Amplification vs Load Resistance

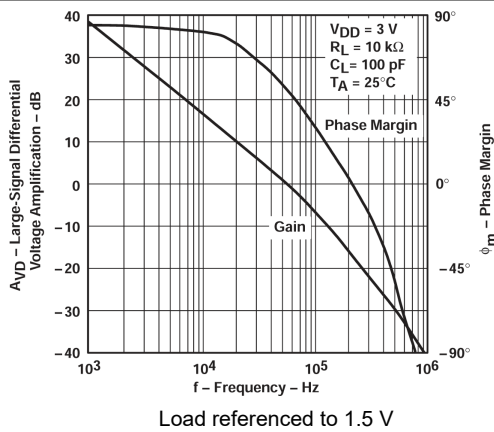


Figure 5-15. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

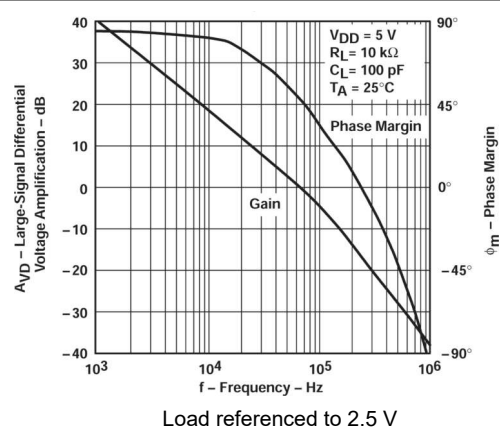


Figure 5-16. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

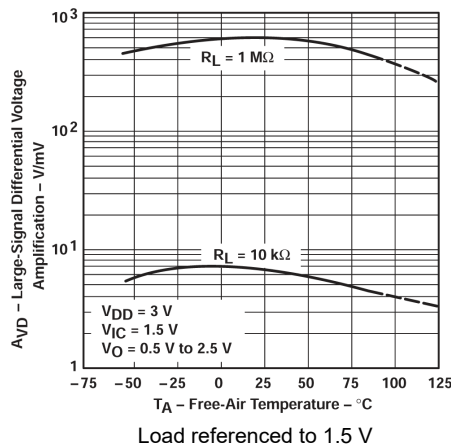


Figure 5-17. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

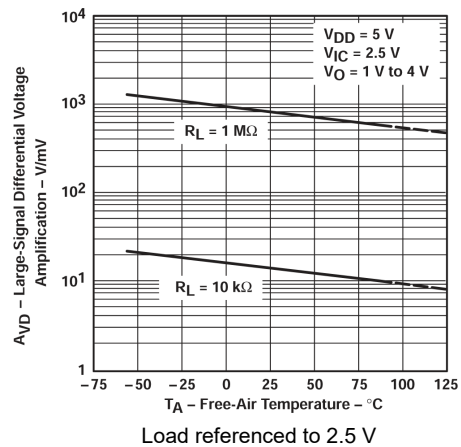


Figure 5-18. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

5 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

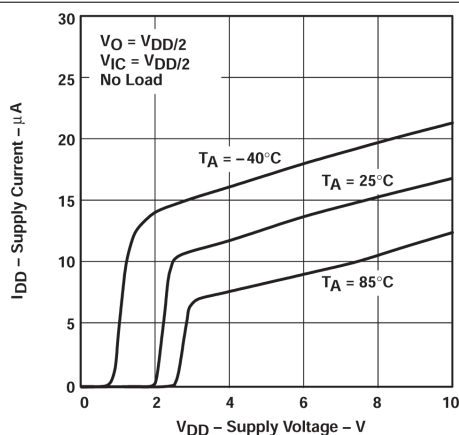


Figure 5-19. Supply Current vs Supply Voltage

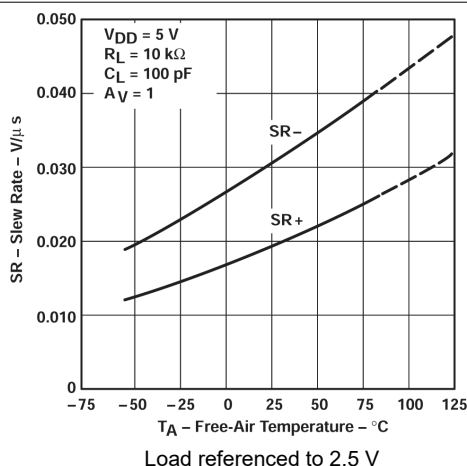


Figure 5-20. Slew Rate vs Free-Air Temperature

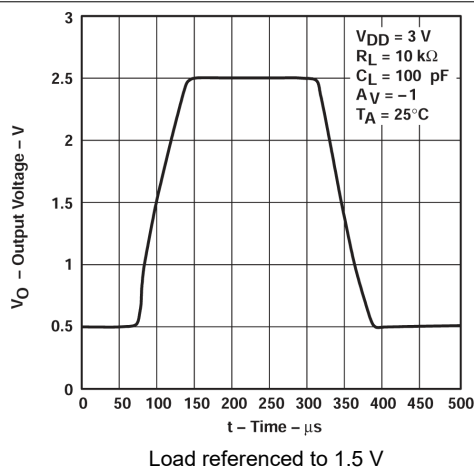


Figure 5-21. Inverting Large-Signal Pulse Response

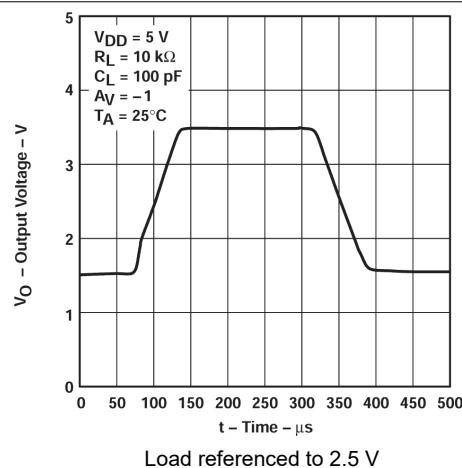


Figure 5-22. Inverting Large-Signal Pulse Response

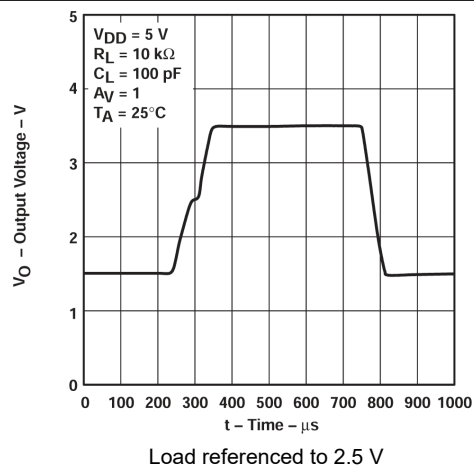


Figure 5-23. Voltage-Follower Large-Signal Pulse Response

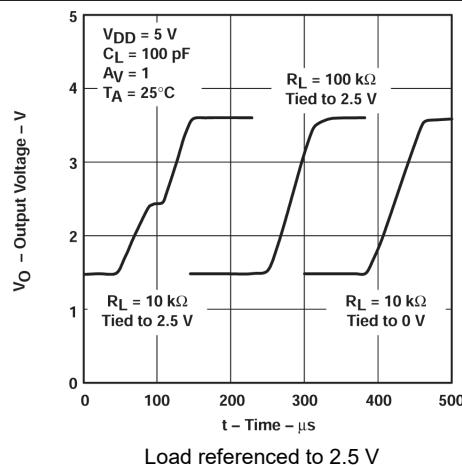


Figure 5-24. Voltage-Follower Large-Signal Pulse Response

5 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

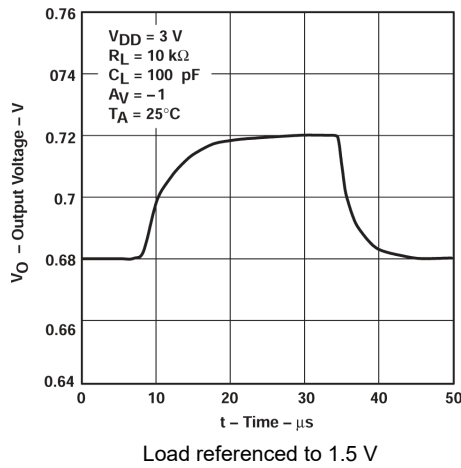


Figure 5-25. Inverting Small-Signal Pulse Response

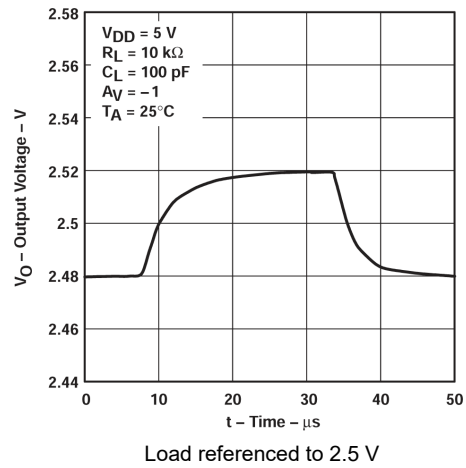


Figure 5-26. Inverting Small-Signal Pulse Response

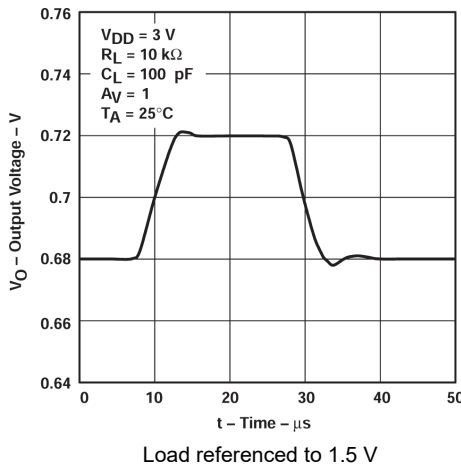


Figure 5-27. Voltage-Follower Small-Signal Pulse Response

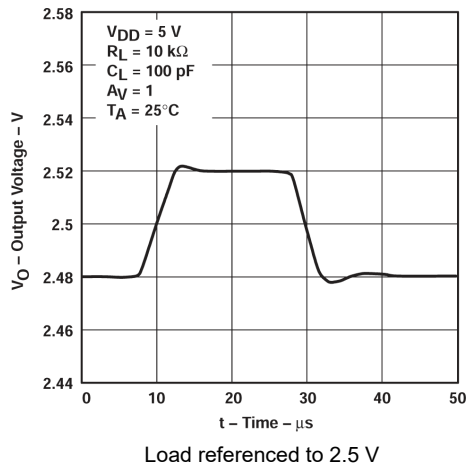


Figure 5-28. Voltage-Follower Small-Signal Pulse Response

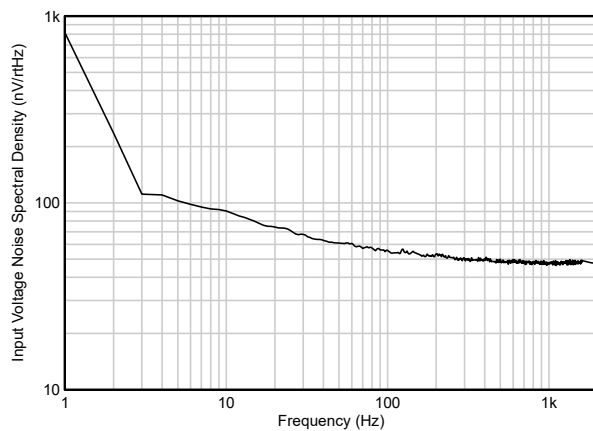


Figure 5-29. Equivalent Input Noise Voltage vs Frequency

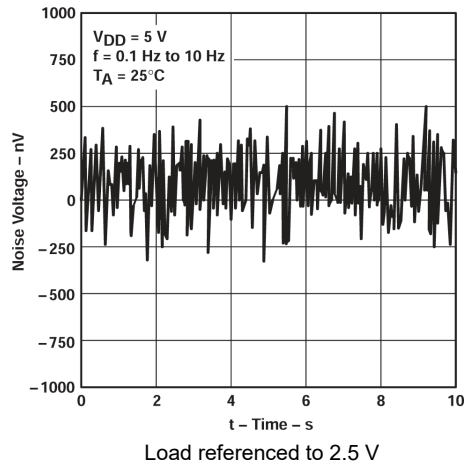


Figure 5-30. Input Noise Voltage Over a 10-Second Period

5 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

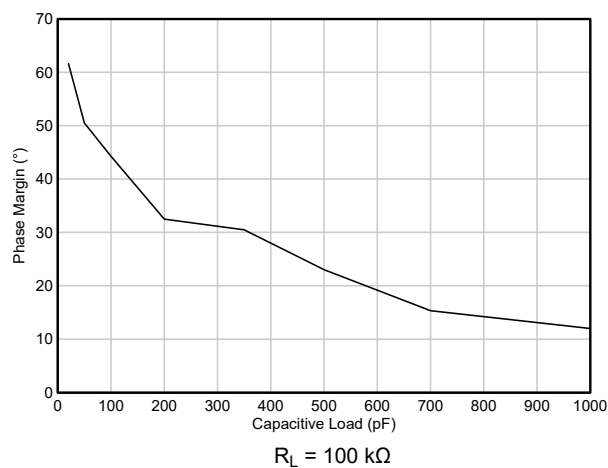


Figure 5-31. Phase Margin vs Load Capacitance

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Driving Large Capacitive Loads

The TLV2711 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 5-31 illustrate the ability to drive loads up to 600 pF while maintaining good phase margins ($R_{null} = 0 \Omega$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 6-1) improves the gain and phase margins when driving large capacitive loads. The addition of this series resistor has two effects. The first effect is that the series resistor adds a zero to the transfer function. The second effect is that the series resistor reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, use Equation 1.

$$\Delta\phi_{m1} = \tan^{-1} (2 \times \pi \times UGBW \times R_{null} \times C_L) \quad (1)$$

where

- $\Delta\phi_{m1}$ = Improvement in phase margin
- UGBW = Unity-gain bandwidth frequency
- R_{null} = Output series resistance
- C_L = Load capacitance

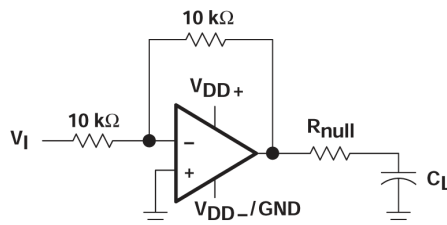


Figure 6-1. Series-Resistance Circuit

6.1.2 Driving Heavy DC Loads

The TLV2711 is designed to provide better sinking and sourcing output currents than previous CMOS rail-to-rail output devices. This device is specified to sink 500 μ A and source 250 μ A at $V_{DD} = 3$ V and $V_{DD} = 5$ V at a maximum quiescent I_{DD} of 25 μ A. These specifications provide a greater than 90% power efficiency.

When driving heavy dc loads, such as 10 k Ω , the positive edge under slewing conditions can experience some distortion; see also Figure 5-23. This condition is affected by three factors:

- *Where the load is referenced.* When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 5-24 illustrates two 10-k Ω load conditions. The first load condition shows the distortion seen for a 10-k Ω load tied to 2.5 V. The third load condition shows no distortion for a 10-k Ω load tied to 0 V.
- *Load resistance.* As the load resistance increases, the distortion seen on the output decreases. Figure 5-24 illustrates the difference seen on the output for a 10-k Ω load and a 100-k Ω load with both tied to 2.5 V.
- *Input signal edge rate.* Faster input edge rates for a step input result in more distortion than with slower input edge rates.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

7.3 Trademarks

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7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2001) to Revision B (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated <i>Features</i>	1
• Deleted references to TLV2711Y chip form device and associated equivalent schematic.....	1
• Deleted Output current, Total current into V_{DD+} and out of V_{DD-} from <i>Absolute Maximum Ratings</i>	3
• Deleted Input offset voltage long term drift and table note 4 from both <i>Electrical Characteristics</i>	4
• Added table note for Input offset current and Input bias current to both <i>Electrical Characteristics</i>	4
• Changed Z_O from 200Ω to 5kΩ in both <i>Electrical Characteristics</i>	4
• Changed CMRR minimum at $T_A = 25^\circ\text{C}$ from 65 dB to 59 dB.....	4
• Changed CMRR minimum at $T_A = \text{Full range}$ from 60 dB to 58 dB.....	4
• Changed kSVR minimum at $T_A = 25^\circ\text{C}$ and $T_A = \text{Full range}$ from 80 dB to 70 dB.....	4
• Changed Equivalent input noise voltage for $f = 1 \text{ kHz}$ from 22 nV/√Hz to 50 nV/√Hz	5
• Updated note 1 to correct temperature ranges for both device versions in both <i>Operating Characteristics</i>	5
• Updated table note 3 to show correct reference voltage.....	5
• Changed Equivalent input noise voltage for $f = 1 \text{ kHz}$ from 21 nV/√Hz to 50 nV/√Hz	6
• Updated table note 2 to show correct reference voltage.....	6
• Deleted Figures 4, 5, 9, 10, 17, 18, 26-32, 34, 45, 47-49, 51, and 52.....	7
• Updated Figure 4-36 and 4-38; previously Figures 44 and 50.....	7
• Updated <i>Applications information</i> on driving large capacitive loads.....	13

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2711CDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	VAJC
TLV2711CDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VAJC
TLV2711CDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-	VAJC
TLV2711CDBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	VAJC
TLV2711IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	VAJI
TLV2711IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	VAJI
TLV2711IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-	VAJI
TLV2711IDBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	VAJI
TLV2711IDBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	-	Call TI	Call TI	See TLV2711IDBVT	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

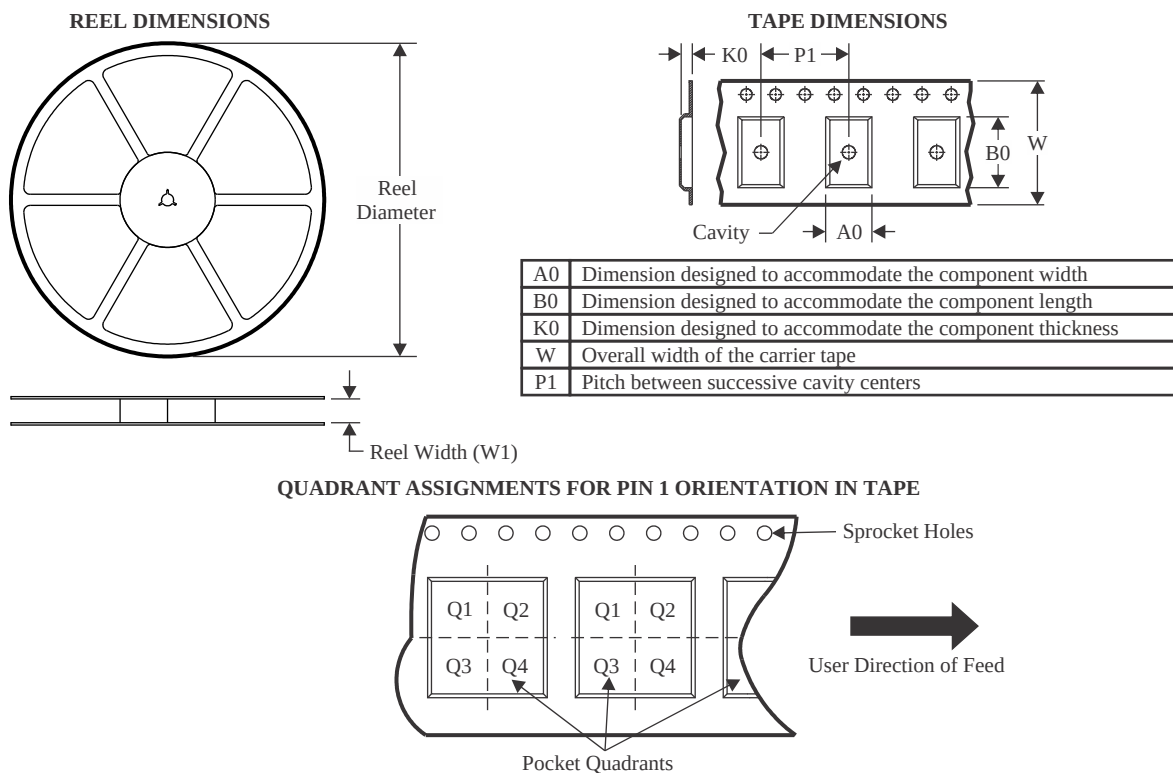
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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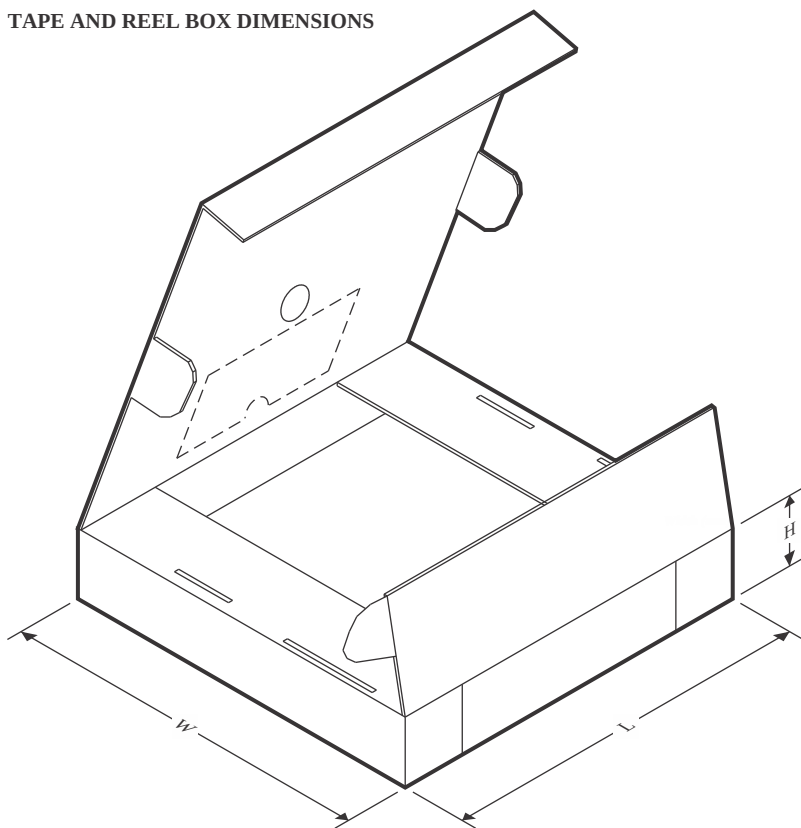
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2711CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2711CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2711IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2711IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

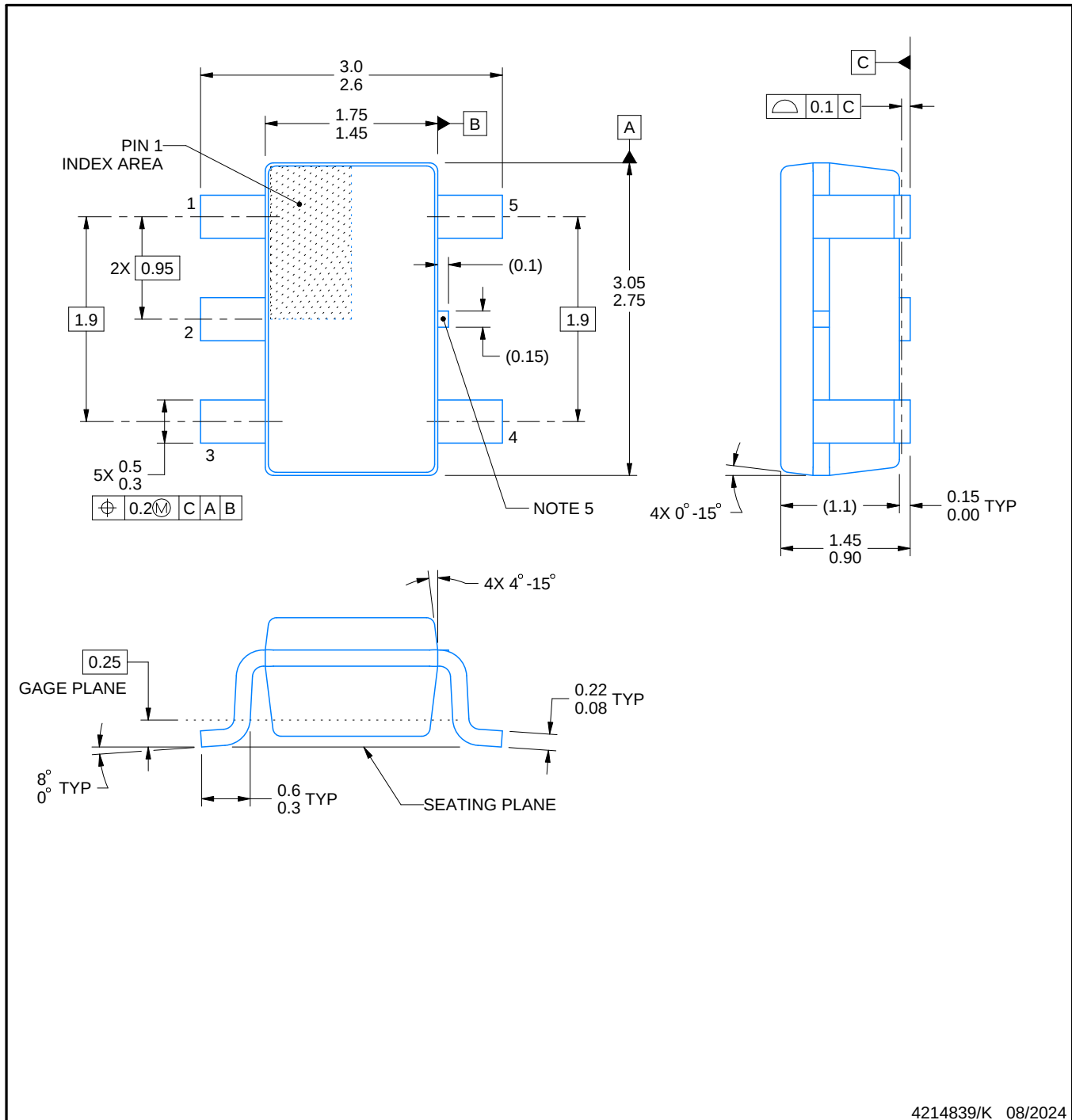


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2711CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2711CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV2711IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2711IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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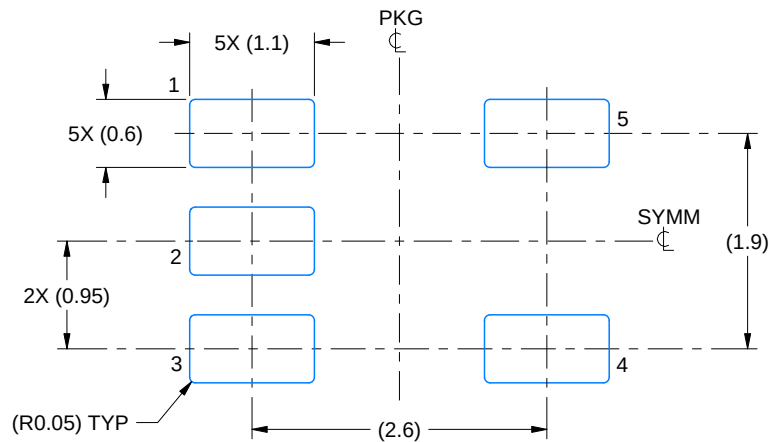
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

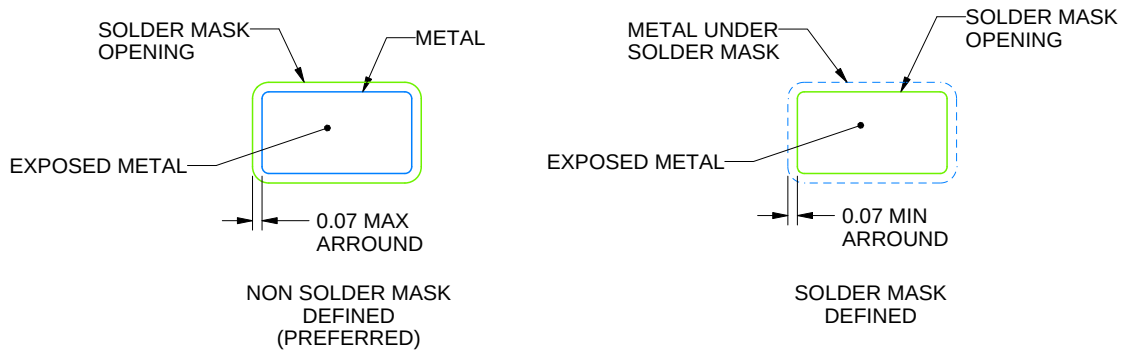
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

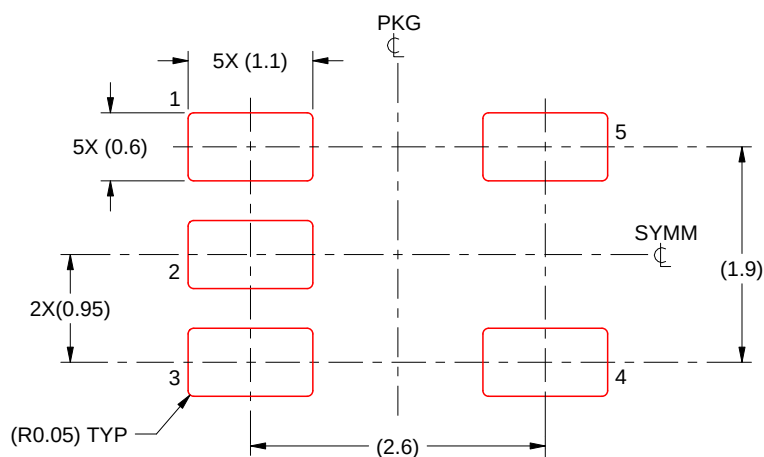
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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