

FAMILY OF NANOPOWER OPERATIONAL AMPLIFIERS AND PUSH-PULL COMPARATORS

FEATURES

- **Micro-Power Operation . . . 1.4 μ A**
- **Input Common-Mode Range Exceeds the Rails . . . -0.1 V to $V_{CC} + 5$ V**
- **Supply Voltage Range . . . 2.5 V to 16 V**
- **Rail-to-Rail Input/Output (Amplifier)**
- **Reverse Battery Protection Up to 18 V**
- **Gain Bandwidth Product . . . 5.5 kHz (Amplifier)**
- **Push-Pull CMOS Output Stage (Comparator)**
- **Specified Temperature Range**
 - $T_A = -40^{\circ}\text{C}$ to 125°C . . . Industrial Grade
- **Ultrasmall Packaging**
 - 8-Pin MSOP (TLV2702)
- **Universal Op-Amp EVM (See the SLOU060 For More Information)**

The TLV270x's low supply current is coupled with extremely low input bias currents enabling them to be used with mega-ohm resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as $390\mu\text{V}$, CMRR of 90 dB, and minimum open loop gain of 130 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V, and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micro-power microcontrollers available today including TI's MSP430.

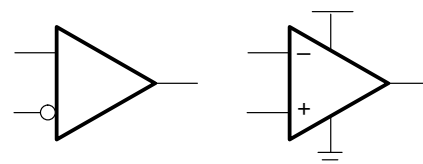
All members are available in PDIP and SOIC with the duals, one op-amp and one comparator, in the small MSOP package and quads, two operational amplifiers and two comparators, in the TSSOP package.

APPLICATIONS

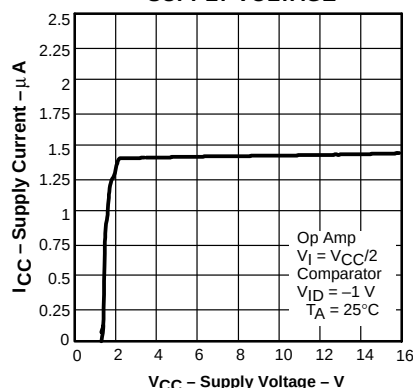
- **Portable Battery Monitoring**
- **Consumer Medical Electronics**
- **Security Detection Systems**

DESCRIPTION

The TLV270x combines sub-micropower operational amplifier and comparator into a single package that produces excellent micropower signal conditioning with only $1.4\mu\text{A}$ of supply current. This combination gives the designer more board space and reduces part counts in systems that require an operational amplifier and comparator. The low supply current makes it an ideal choice for battery powered portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an over-current condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.



**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

A SELECTION OF OUTPUT COMPARATORS†

DEVICE	V _{CC} (V)	V _{IO} (μ V)	I _{CC} /Ch (μ A)	GBW (kHz)	SR (V/ μ s)	t _{PLH} (μ s)	t _{PHL} (μ s)	t _f (μ s)	RAIL-TO-RAIL	OUTPUT STAGE
TLV270x	2.5 – 16	390	1.4‡	5.5	0.0025	56	83	8	I/O	PP
TLV230x	2.5 – 16	390	1.4‡	5.5	0.0025	55	30	5	I/O	OD
TLV240x	2.5 – 16	390	880	5.5	0.0025	—	—	—	I/O	—
TLV224x	2.5 – 12	600	1	5.5	0.002	—	—	—	I/O	—
TLV340x	2.5 – 16	250	0.47	—	—	55	30	5	I	OD
TLV370x	2.5 – 16	250	0.56	—	—	56	83	8	I	PP

† All specifications are typical values measured at 5 V.

‡ ICC is specified as one op-amp and one comparator.

TLV2702 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	MSOP		PLASTIC DIP (P)
			MSOP† (DGK)	SYMBOLS	
–40°C to 125°C	4000 μ V	TLV2702ID	TLV2702IDGK	xxTIAQF	TLV2702IP

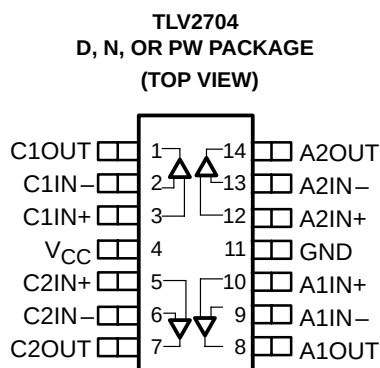
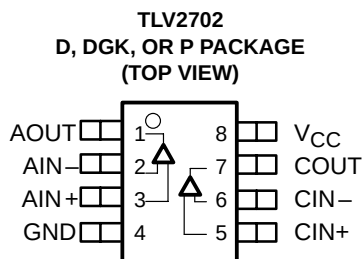
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2702IDR).

TLV2704 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	TSSOP (PW)	PLASTIC DIP (N)
–40°C to 125°C	4000 μ V	TLV2704ID	TLV2704IPW	TLV2704IN

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2704IDR).

TLV270x PACKAGE PINOUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	17 V
Differential input voltage, V_{ID}	V_{CC}
Input voltage range, V_I (see Notes 1 and 2)	0 to $V_{CC} + 5$ V
Input current range, I_I (any input)	± 10 mA
Output current range, I_O	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : I suffix	-40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to GND
2. Input voltage range is limited to 20 V max or $V_{CC} + 5$ V, whichever is smaller.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} ($^{\circ}\text{C}/\text{W}$)	θ_{JA} ($^{\circ}\text{C}/\text{W}$)	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	$T_A = 125^{\circ}\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.3	1022 mW	204.4 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	2.5	16	V
	Split supply	± 1.25	± 8	
Common-mode input voltage range, V_{ICR}	Amplifier and comparator	-0.1	$V_{CC}+5$	V
Operating free-air temperature, T_A		-40	125	$^{\circ}\text{C}$

electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted)

amplifier dc performance

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _O = V _{CC} /2 V, V _{IC} = V _{CC} /2 V, R _S = 50 Ω		25°C		390	4000	μV
				Full range			6000	
αV _{IO}	Offset voltage draft			25°C		3		μV/°C
CMRR	Common-mode rejection ratio	V _{IC} = 0 to V _{CC} , R _S = 50 Ω	V _{CC} = 2.7 V	25°C		55	73	dB
				Full range			52	
			V _{CC} = 5 V	25°C		60	80	
				Full range			55	
			V _{CC} = 15 V	25°C		66	90	
				Full range			60	
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 2.7 V, V _{O(pp)} = 1.5 V, R _L = 500 kΩ		25°C		130	400	V/mV
				Full range			30	
		V _{CC} = 5 V, V _{O(pp)} = 3 V, R _L = 500 kΩ		25°C		300	1000	
				Full range			100	
		V _{CC} = 15 V, V _{O(pp)} = 8 V, R _L = 500 kΩ		25°C		400	1800	
				Full range			120	
PSRR	Power supply rejection ratio (ΔV _{CC} /ΔV _{IO})	V _{IC} = V _{CC} /2 V, No load	V _{CC} = 2.7 to 5 V	25°C		90	120	dB
				Full range			85	
			V _{CC} = 5 to 15 V	25°C		94	120	
				Full range			90	

† Full range is -40°C to 125°C .

amplifier and comparator input characteristics

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
I_{IO}	Input offset current	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$		25°C		25	250	pA
				0 to 70°C			300	
				Full range			700	
I_{IB}	Input bias current			25°C		100	500	pA
				0 to 70°C			550	
				Full range			1700	
$r_{i(d)}$	Differential input resistance			25°C		300		$\text{M}\Omega$
$C_{i(c)}$	Common-mode input capacitance	$f = 100 \text{ kHz}$		25°C		3		pF

† Full range is -40°C to 125°C .

electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted) (continued)

amplifier output characteristics

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$V_{IC} = V_{CC}/2$, $I_{OH} = -50 \mu\text{A}$	$V_{CC} = 2.7 \text{ V}$	25°C	2.55	2.65	V
		Full range		2.5		
		$V_{CC} = 5 \text{ V}$	25°C	4.85	4.95	
		Full range		4.8		
		$V_{CC} = 15 \text{ V}$	25°C	14.8	14.95	
		Full range		14.8		
V_{OL} Low-level output voltage	$V_{IC} = V_{CC}/2$, $I_{OL} = 50 \mu\text{A}$	25°C		180	260	mV
		Full range			300	
I_O Output current	$V_O = 0.5 \text{ V}$ from rail	25°C		± 200		μA
Z_O Closed-loop output impedance	$f = 100 \text{ Hz}$, $A_V = 10$	25°C		1.2		$\text{k}\Omega$

† Full range is -40°C to 125°C .

amplifier dynamic performance

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
UGBW Unity gain bandwidth	$R_L = 500 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C		5.5		kHz
SR Slew rate at unity gain	$V_{O(pp)} = 0.8 \text{ V}$, $R_L = 500 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C		2.5		V/ms
ϕ_M Phase margin	$R_L = 500 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C		60°		
Gain margin				15		dB
t_s Settling time	$V_{CC} = 2.7 \text{ or } 5 \text{ V}$, $V_{(STEP)PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$	25°C		1.84		ms
	$V_{CC} = 15 \text{ V}$, $V_{(STEP)PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$			6.1		
				32		
V_n Equivalent input noise voltage	$f = 0.1 \text{ to } 10 \text{ Hz}$	25°C		5.3		μV_{pp}
	$f = 100 \text{ Hz}$			500		$\text{nV}/\sqrt{\text{Hz}}$
I_n Equivalent input noise current	$f = 100 \text{ Hz}$	25°C		8		$\text{fA}/\sqrt{\text{Hz}}$

supply current

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
I_{CC} Supply current (one op-amp and one comparator)	$V_O = V_{CC}/2$	$V_{CC} = 2.7 \text{ V or } 5 \text{ V}$	25°C	1.4		μA
		$V_{CC} = 15 \text{ V}$	25°C	1.4	1.9	
		Full range			3.7	
Reverse supply current	$V_{CC} = -18 \text{ V}$, $V_I = 0 \text{ V}$, $V_O = \text{open}$	25°C		50		nA

† Full range is -40°C to 125°C .

electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 15 V (unless otherwise noted) (continued)

comparator dc performance

PARAMETER	TEST CONDITIONS†	T_A †	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_{IC} = V_{CC}/2, R_S = 50 \Omega$	25°C		250	5000	μV
		Full range			7000	
α_{VIO} Offset voltage drift		25°C		3		$\mu\text{V}/^\circ\text{C}$
CMRR Common-mode rejection ratio	$V_{IC} = 0 \text{ to } V_{CC}, R_S = 50 \Omega$	$V_{CC} = 2.7 \text{ V}$	25°C	55	72	dB
			Full range	50		
		$V_{CC} = 5 \text{ V}$	25°C	60	76	
			Full range	55		
		$V_{CC} = 15 \text{ V}$	25°C	65	88	
			Full range	60		
A_{VD} Large-signal differential voltage amplification		25°C		1000		V/mV
PSRR Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{IC} = V_{CC}/2 \text{ V}$, No load	$V_{CC} = 2.7 \text{ to } 5 \text{ V}$	25°C	75	100	dB
			Full range	70		
		$V_{CC} = 5 \text{ to } 15 \text{ V}$	25°C	85	105	
			Full range	80		

† Full range is -40°C to 125°C .

comparator output characteristics

PARAMETER	TEST CONDITIONS†	T_A †	MIN	TYP	MAX	UNIT
$r_{i(d)}$ Differential input resistance		25°C		300		$\text{M}\Omega$
V_{OH} High-level output voltage	$V_{IC} = V_{CC}/2, I_{OL} = -50 \mu\text{A}, V_{ID} = 1 \text{ V}$	25°C	$V_{CC}-320$			mV
		Full range	$V_{CC}-450$			
V_{OL} Low-level output voltage	$V_{IC} = V_{CC}/2, I_{OL} = 50 \mu\text{A}, V_{ID} = -1 \text{ V}$	25°C		80	200	mV
		Full range			300	

† Full range is -40°C to 125°C .

switching characteristics at recommended operating conditions, $V_{CC} = 2.7 \text{ V}, 5 \text{ V}, 15 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT
t _(PLH)	Propagation response time, low-to-high-level output	f = 10 kHz, V _{STEP} = 100 mV, C _L = 10 pF, V _{CC} = 2.7 V	Overdrive = 2 mV	25°C	240			μs
			Overdrive = 10 mV		64			
			Overdrive = 50 mV		36			
t _(PHL)	Propagation response time, high-to-low-level output		Overdrive = 2 mV	25°C	167			
			Overdrive = 10 mV		67			
			Overdrive = 50 mV		37			
t _r	Rise time	C _L = 10 pF, V _{CC} = 2.7 V		25°C	7			μs
t _f	Fall time	C _L = 10 pF, V _{CC} = 2.7 V		25°C	9			μs

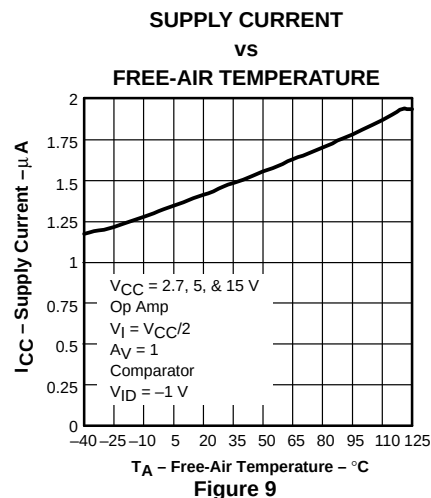
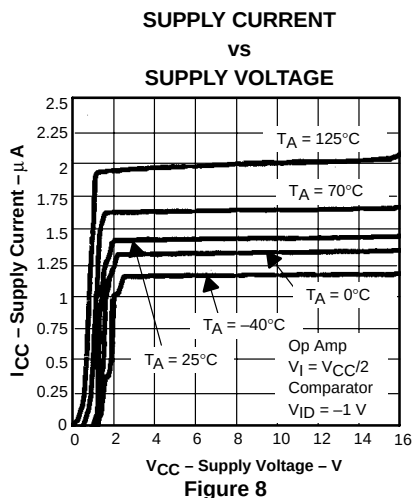
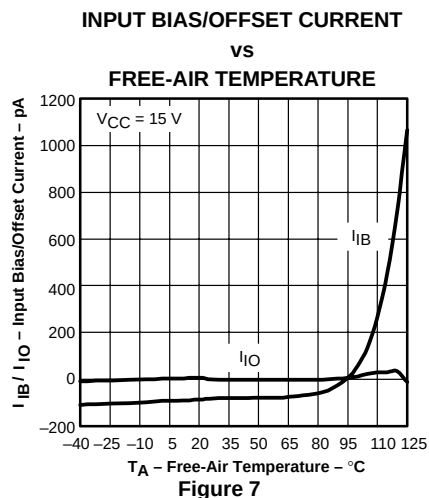
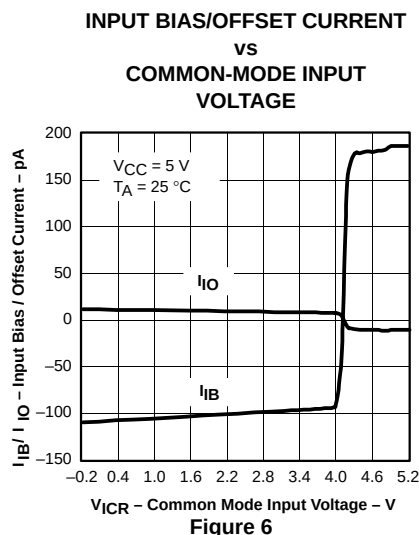
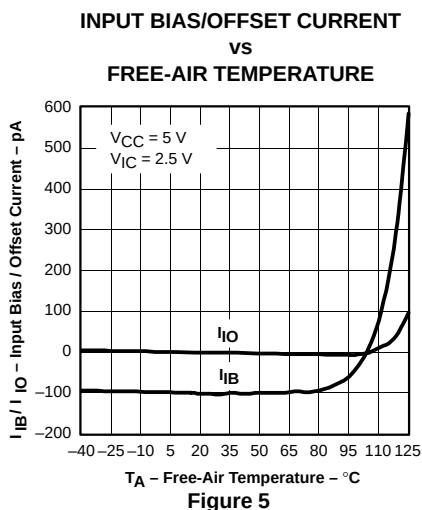
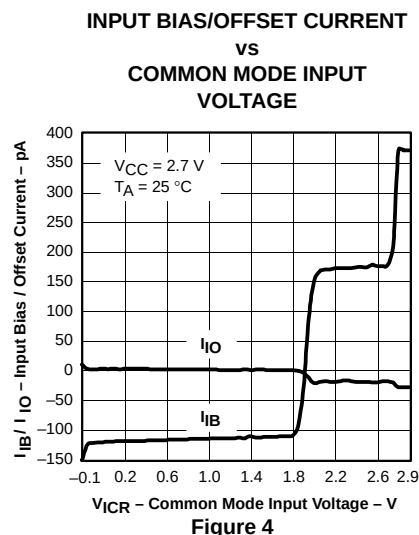
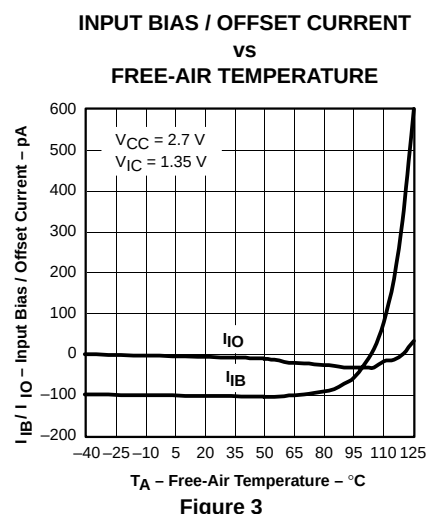
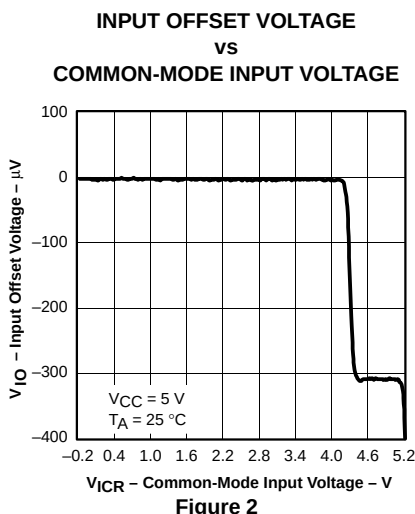
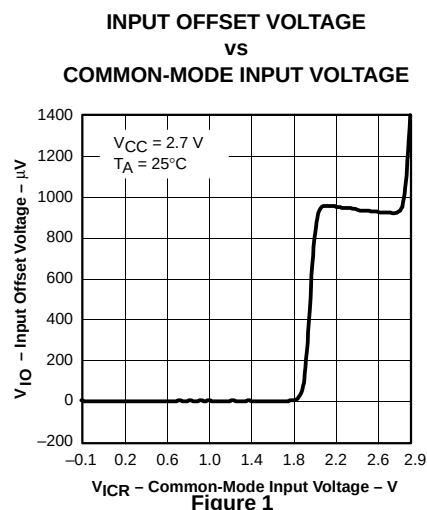
NOTE: The propagation response time specified is the interval between the input step function and the instant when the output crosses 1.4 V. Propagation responses are longer at higher supply voltages, refer to Figure 18 through Figure 36 for further details.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V _{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I _{IB}	Input bias current	vs Free-air temperature	3, 5, 7
		vs Common-mode input voltage	4, 6
I _{IO}	Input offset current	vs Free-air temperature	3, 5, 7
		vs Common-mode input voltage	4, 6
I _{CC}	Supply current	vs Supply voltage	8
		vs Free-air temperature	9
Amplifier			
CMRR	Common-mode rejection ratio	vs Frequency	10
V _{OH}	High-level output voltage	vs High-level output current	11, 13
V _{OL}	Low-level output voltage	vs Low-level output current	12, 14
V _{O(PP)}	Output voltage, peak-to-peak	vs Frequency	15
PSRR	Power supply rejection ratio	vs Frequency	16
	Voltage noise over a 10 Second Period		17
φ _m	Phase margin	vs Capacitive load	18
A _{VD}	Differential voltage gain	vs Frequency	19
	Phase	vs Frequency	19
	Gain-bandwidth product	vs Supply voltage	20
SR	Slew rate	vs Free-air temperature	21
	Large-signal follower pulse response		22
	Small-signal follower pulse response		23
	Large-signal inverting pulse response		24
	Small-signal inverting pulse response		25
Comparator			
V _{OH}	High-level output voltage	vs High-level output current	26, 28
V _{OL}	Low-level output voltage	vs Low-level output current	27, 29
	Output rise/fall time	vs Supply voltage	30
	Low-to-high level output response for various input overdrives		31, 33, 35
	High-to-low level output response for various input overdrives		32, 34, 36

AMPLIFIER AND COMPARATOR TYPICAL CHARACTERISTICS



AMPLIFIER TYPICAL CHARACTERISTICS

**COMMON-MODE REJECTION RATIO
VS
FREQUENCY**

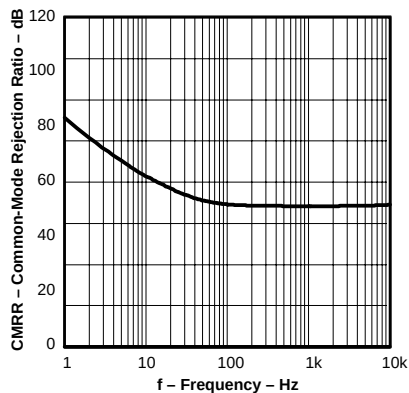


Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

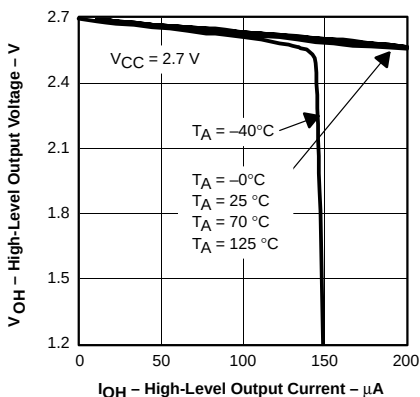


Figure 11

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

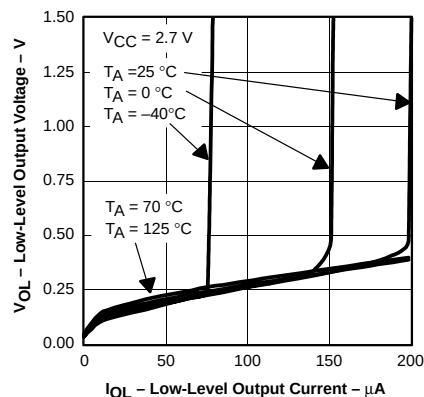


Figure 12

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

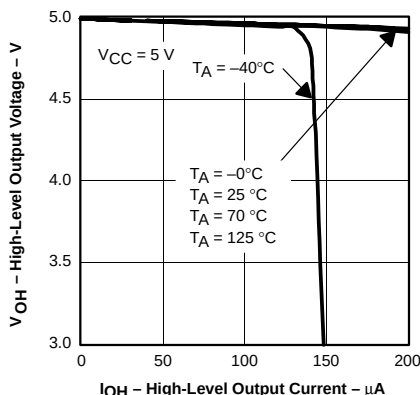


Figure 13

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

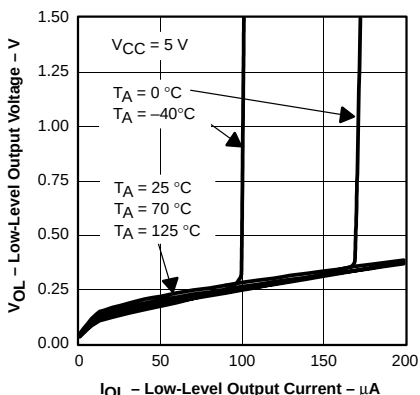


Figure 14

**OUTPUT VOLTAGE
PEAK-TO-PEAK
VS
FREQUENCY**

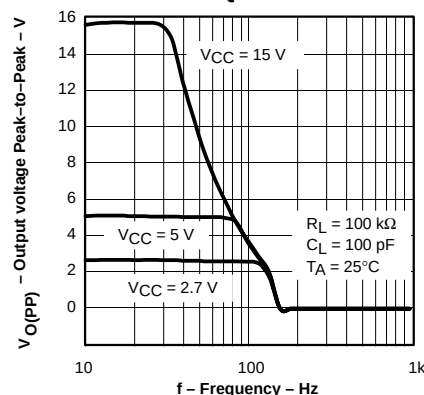


Figure 15

**POWER SUPPLY REJECTION RATIO
VS
FREQUENCY**

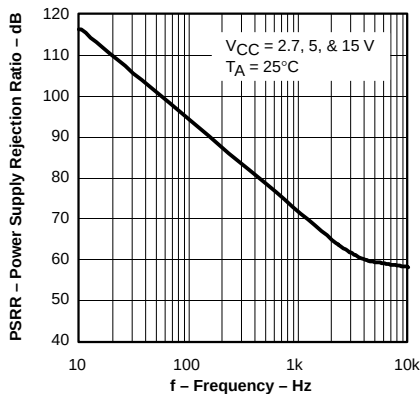


Figure 16

**VOLTAGE NOISE
OVER A 10 SECOND PERIOD**

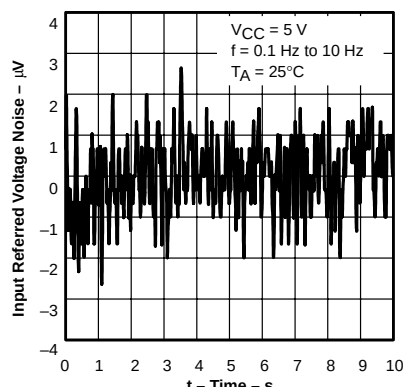


Figure 17

**PHASE MARGIN
VS
CAPACITIVE LOAD**

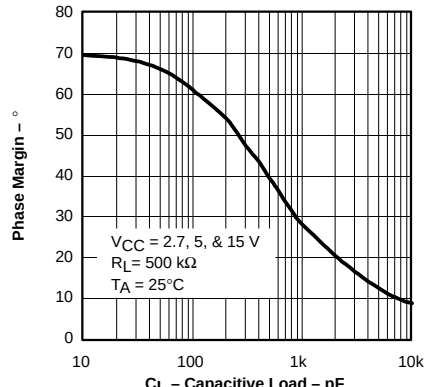
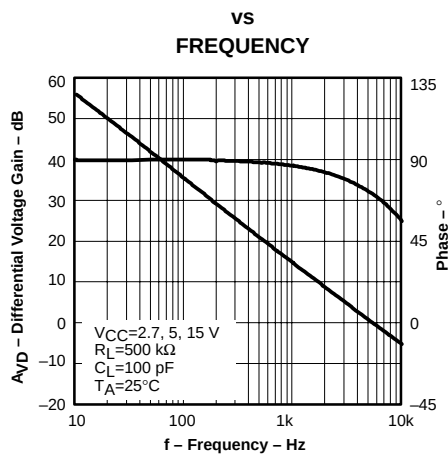


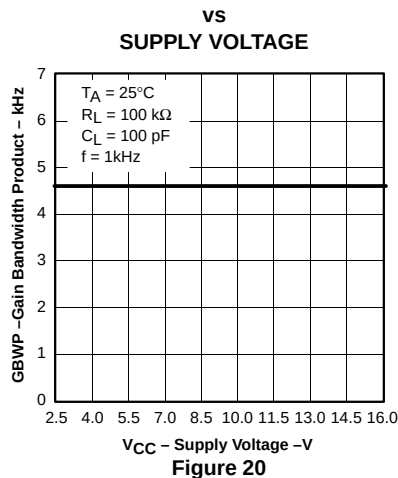
Figure 18

AMPLIFIER TYPICAL CHARACTERISTICS

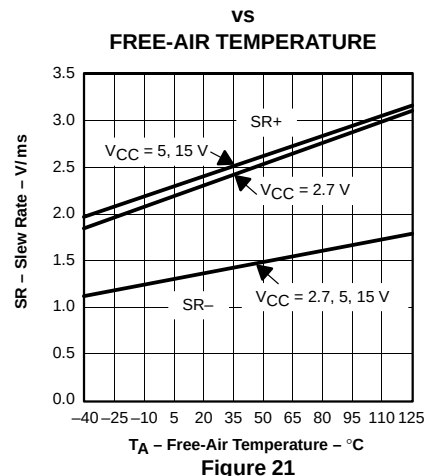
DIFFERENTIAL VOLTAGE GAIN AND PHASE



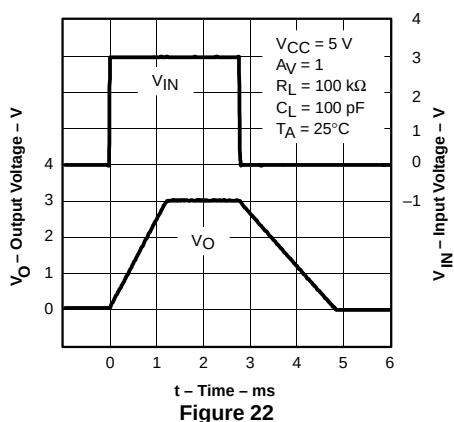
GAIN BANDWIDTH PRODUCT



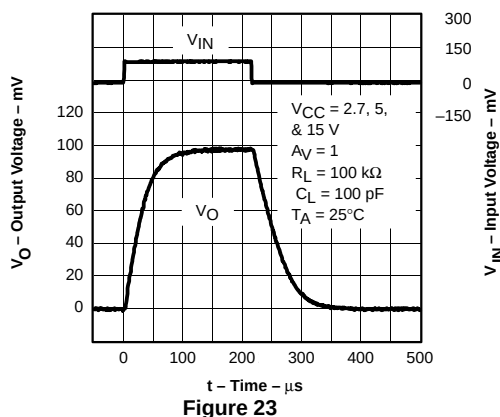
SLEW RATE



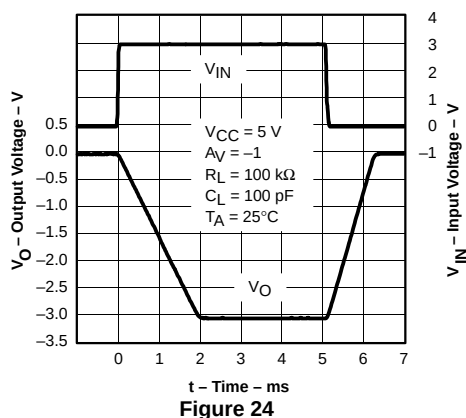
LARGE-SIGNAL FOLLOWER PULSE RESPONSE



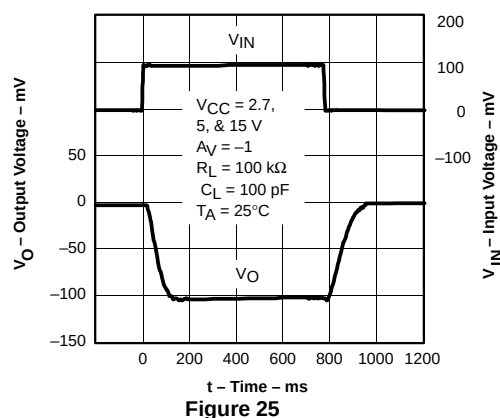
SMALL-SIGNAL FOLLOWER PULSE RESPONSE



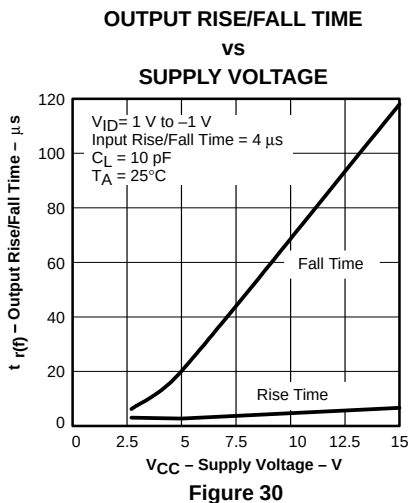
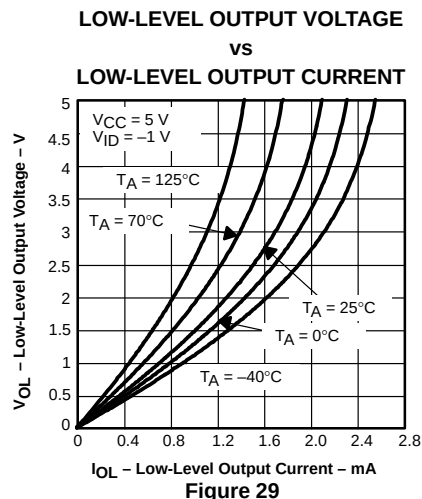
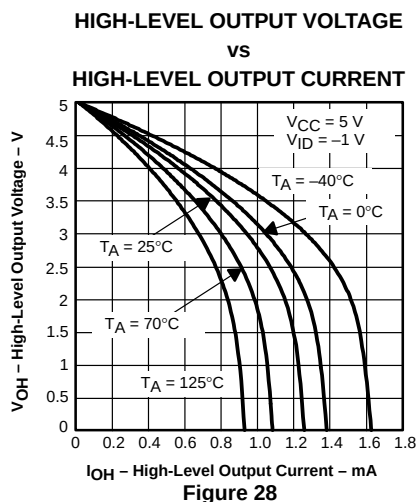
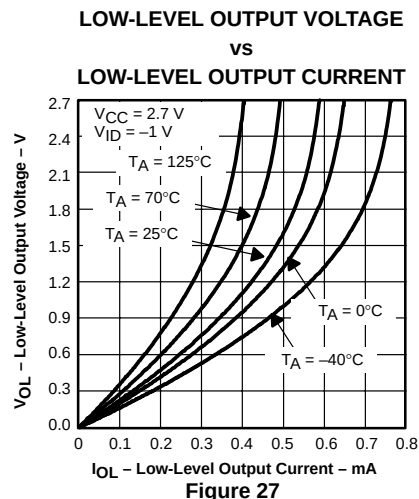
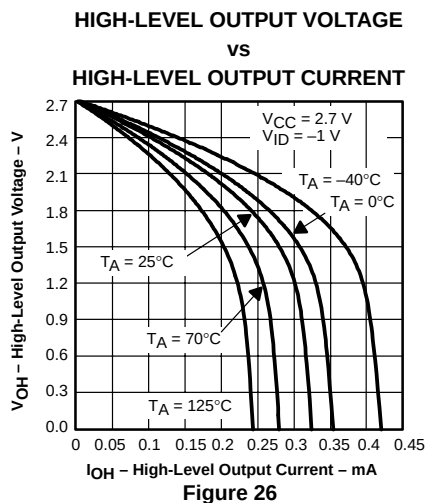
LARGE-SIGNAL INVERTING PULSE RESPONSE



SMALL-SIGNAL INVERTING PULSE RESPONSE



COMPARATOR TYPICAL CHARACTERISTICS



LOW-TO-HIGH OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES



Figure 32

Figure 33

Figure 34

Figure 35

Figure 36

APPLICATION INFORMATION

reverse battery protection

The TLV2702/4 are protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of 6 Schottky diodes and will therefore increase as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure will turn on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

common-mode input range

The TLV2702/4 has rail-rail input and outputs. For common-mode inputs from -0.1 V to $V_{CC} - 0.8$ V a PNP differential pair will provide the gain.

For inputs between $V_{CC} - 0.8$ V and V_{CC} , two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails; because as the inputs go above V_{CC} , the NPNs switch from functioning as transistors to functioning as diodes. This will lead to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC} .

The TLV2702/4 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain will be observed with the ultimate possibility of phase inversion.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage.

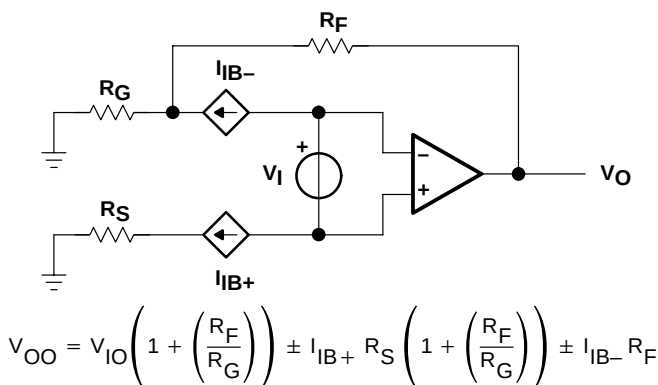


Figure 37. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 38).

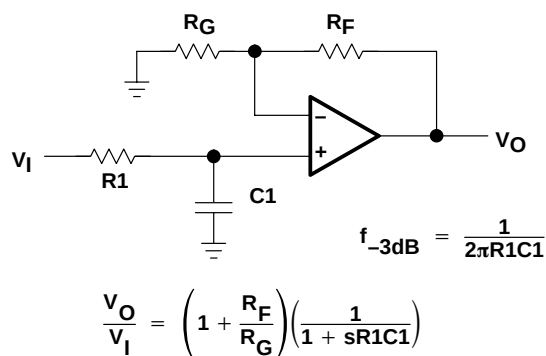


Figure 38. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

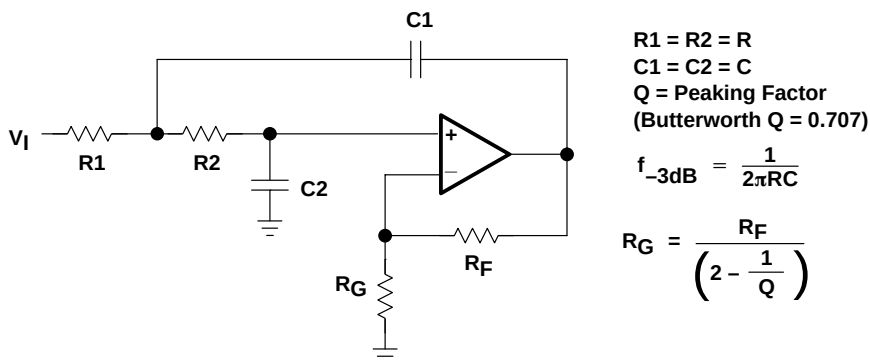


Figure 39. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV270x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes**—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling**—Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- **Sockets**—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs/compact part placements**—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- **Surface-mount passive components**—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 40 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV270x IC (watts)

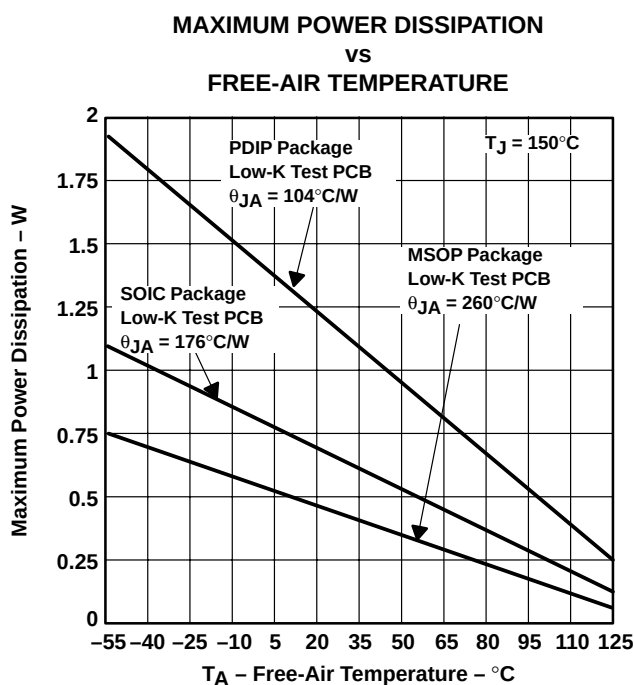
T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Free-ambient air temperature (°C)

θ_{JA} = $\theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 40. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

amplifier macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 41 are generated using the TLV270x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 3: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

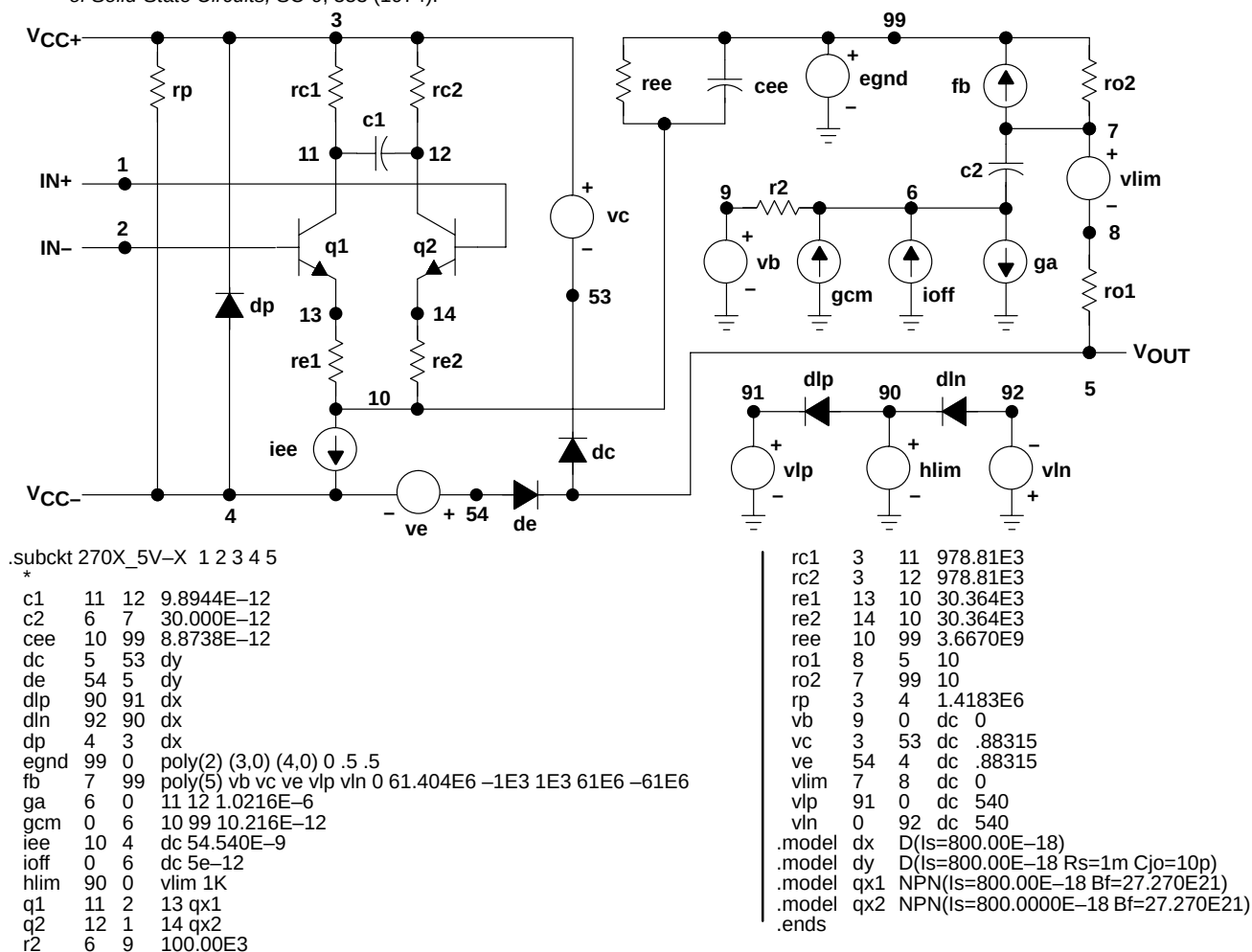


Figure 41. Boyle Macromodels and Subcircuit

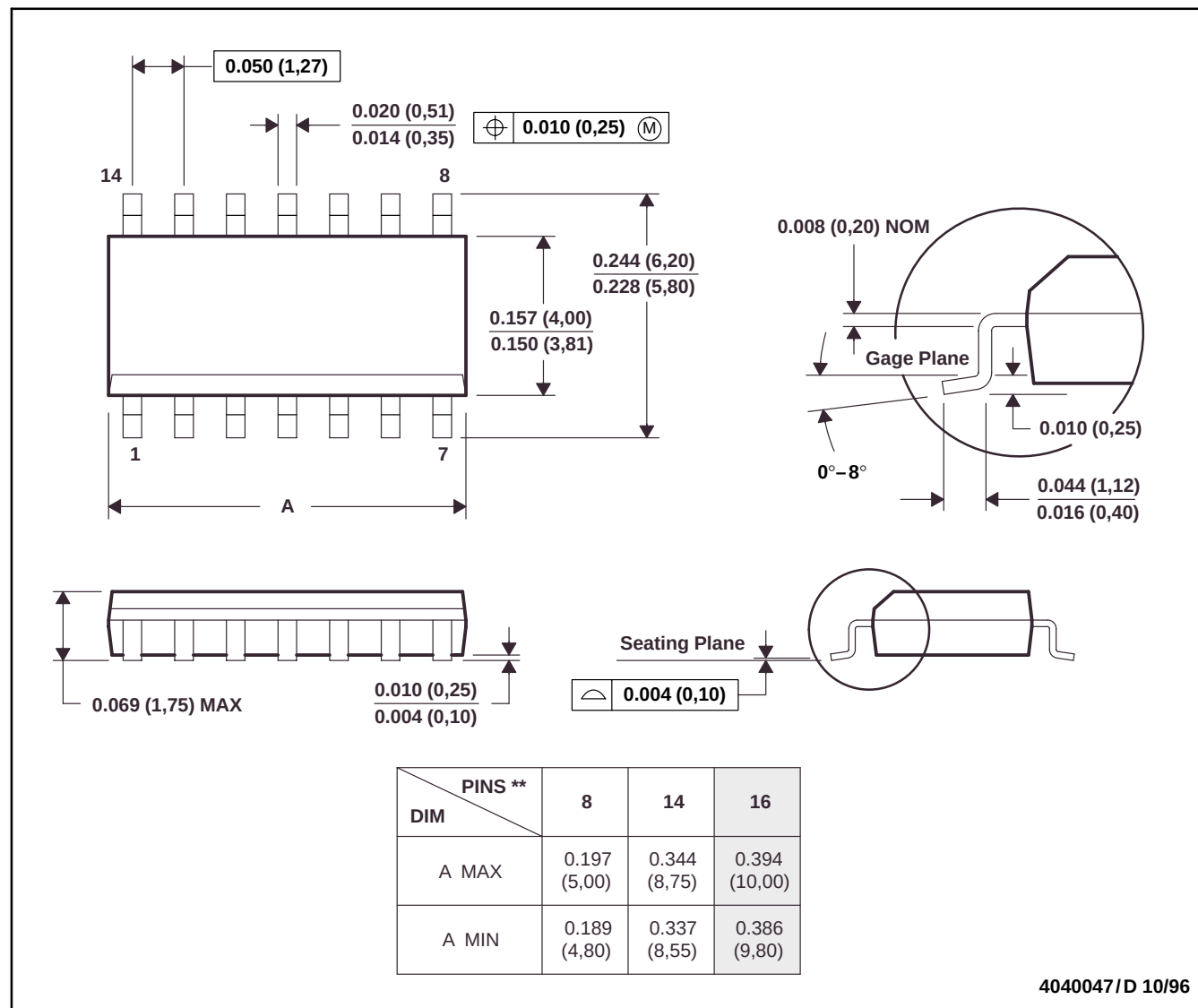
PSpice and *Parts* are trademarks of MicroSim Corporation.

MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

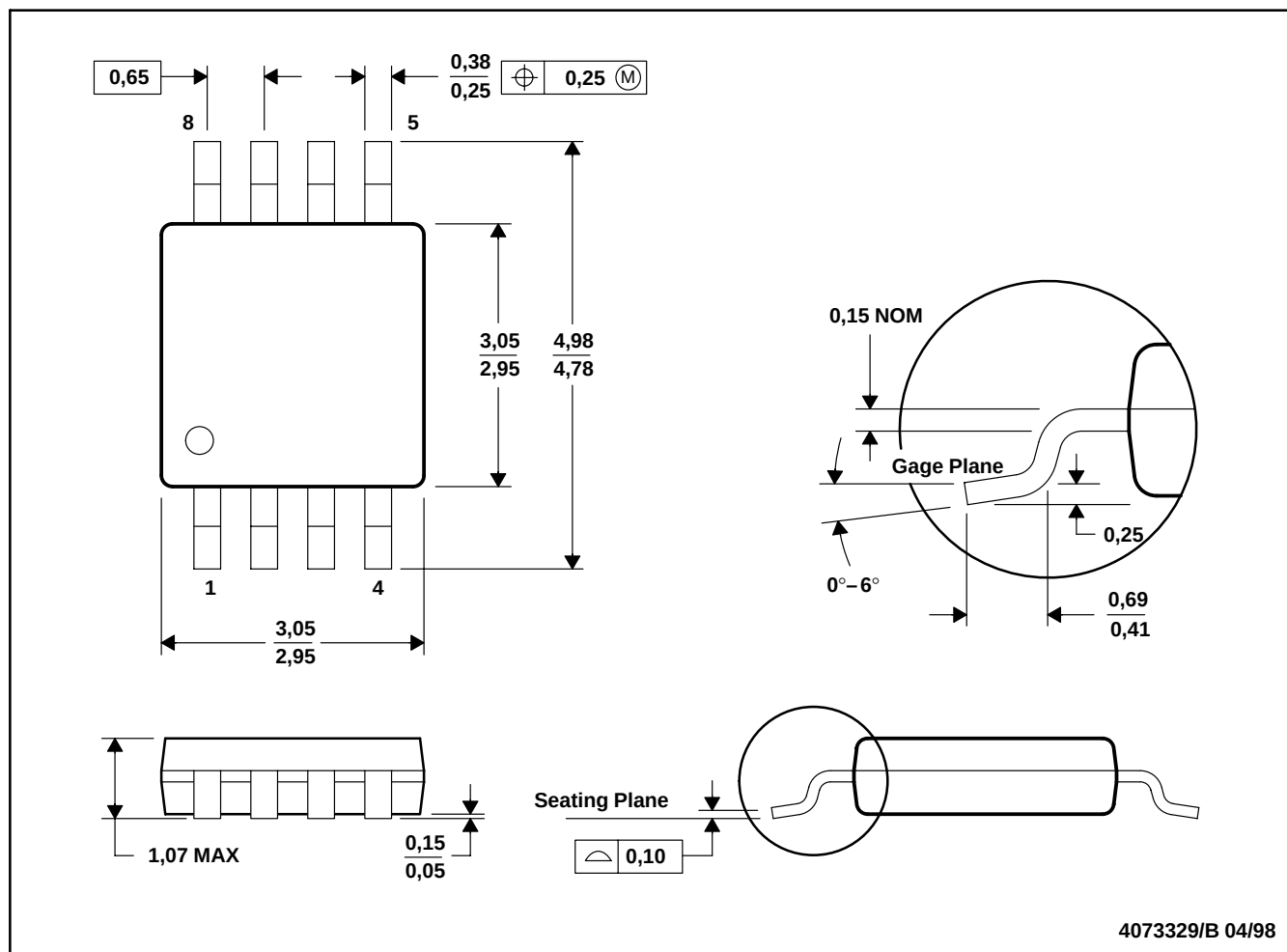


- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

MECHANICAL INFORMATION

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



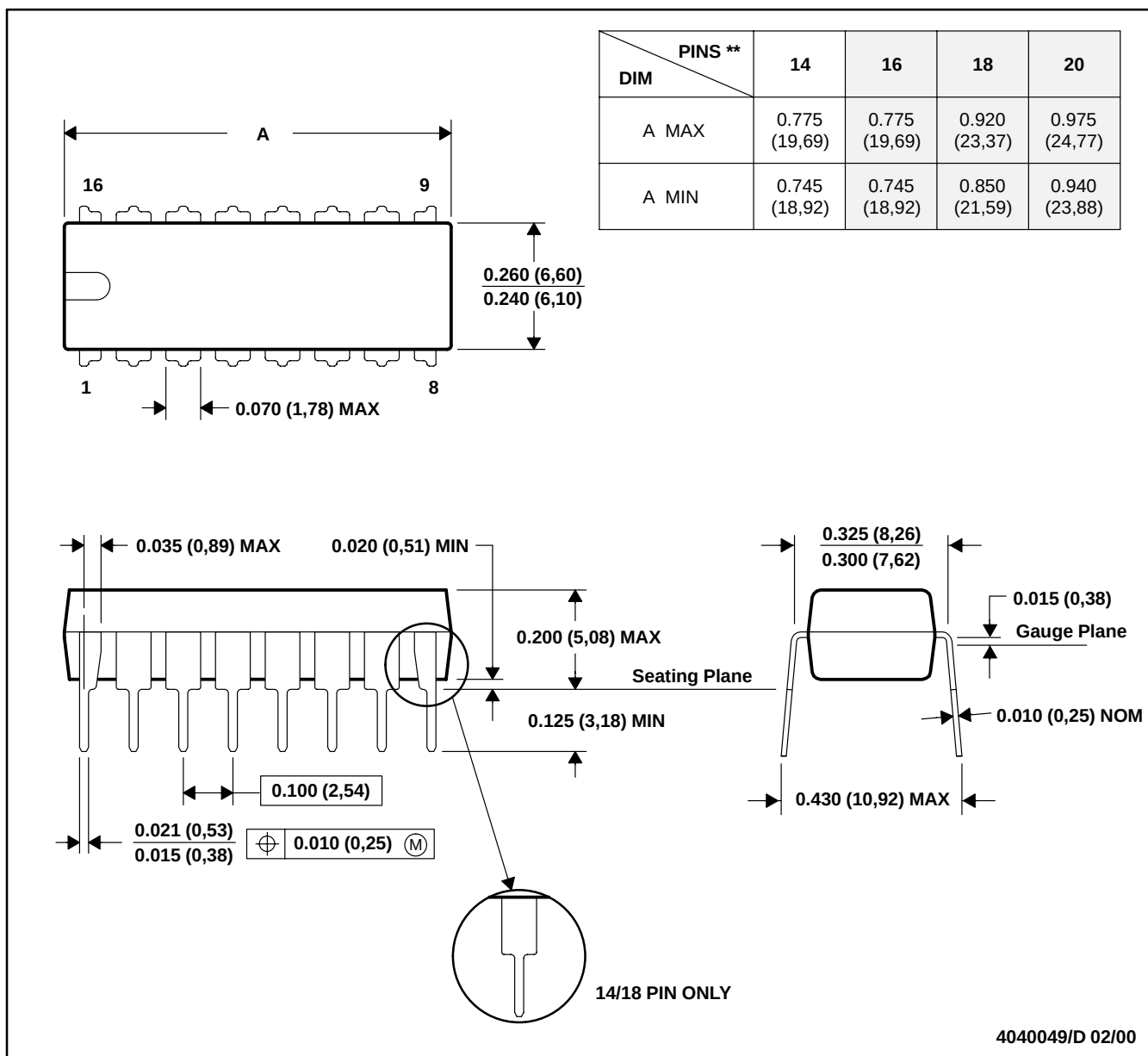
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187

MECHANICAL INFORMATION

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

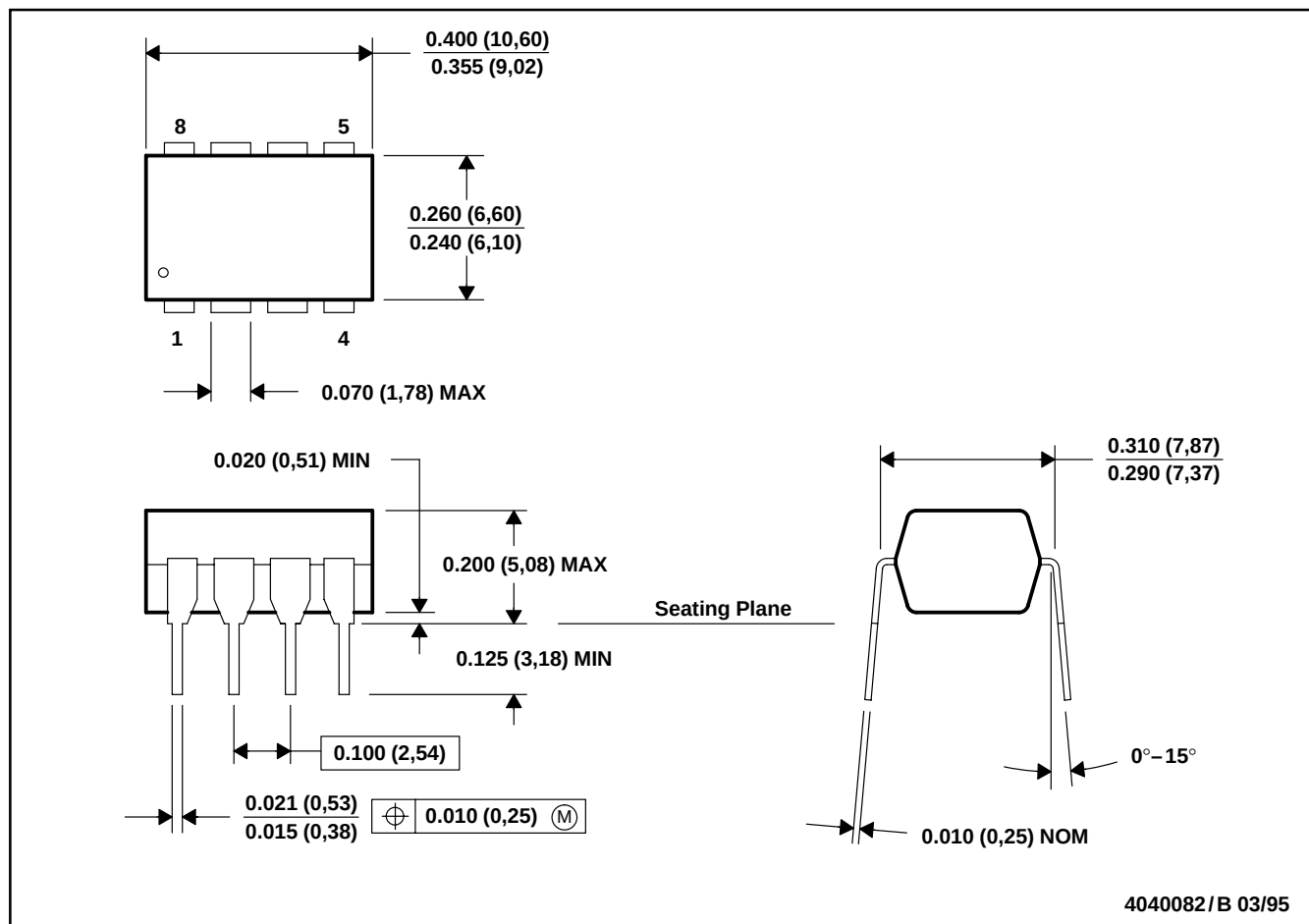


- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



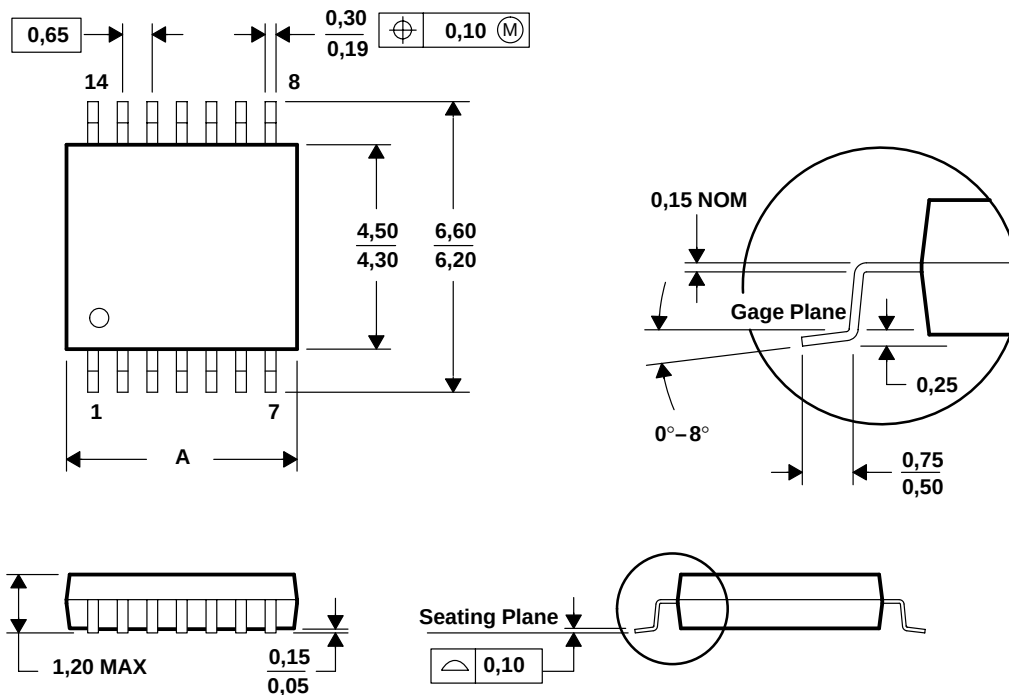
- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2702ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2702I
TLV2702ID.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2702I
TLV2702IDGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQF
TLV2702IDGK.A	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQF
TLV2702IDGKG4	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQF
TLV2702IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2702I
TLV2702IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2702I
TLV2704ID	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2704I
TLV2704ID.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2704I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

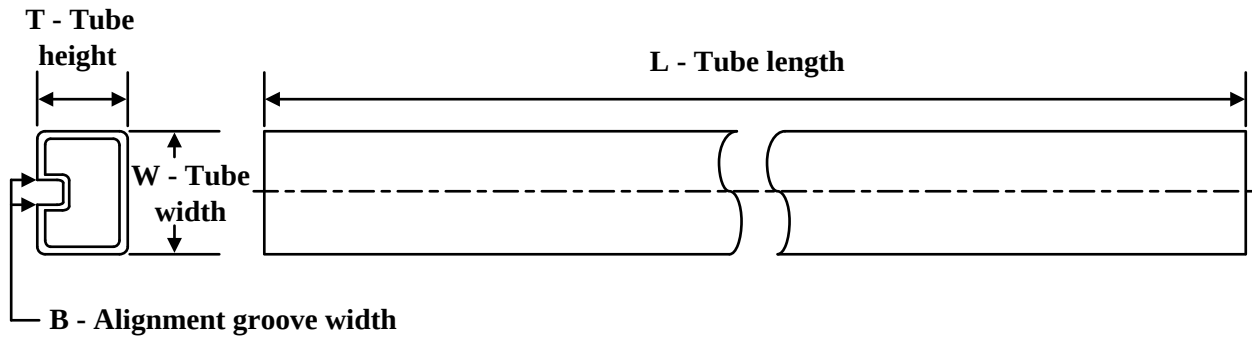
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2702ID	D	SOIC	8	75	507	8	3940	4.32
TLV2702ID.A	D	SOIC	8	75	507	8	3940	4.32
TLV2702IDGK	DGK	VSSOP	8	80	274	6.2	2540	2.5
TLV2702IDGK.A	DGK	VSSOP	8	80	274	6.2	2540	2.5
TLV2702IDGKG4	DGK	VSSOP	8	80	274	6.2	2540	2.5
TLV2702IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2702IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLV2704ID	D	SOIC	14	50	507	8	3940	4.32
TLV2704ID.A	D	SOIC	14	50	507	8	3940	4.32

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