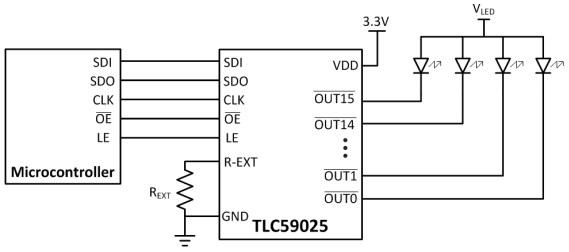
# TLC59025 Low-Power 16-Channel Constant-Current LED Sink Driver

## 1 Features

- 16 constant current output channels
- Matches industry standard IOUT to external resistor ratio
- Constant output current invariant to load voltage change
- Output current accuracy:
  - Between channels: < ±5% (maximum)
  - Between ICs: < ±6% (maximum)
- Constant output current range: 3 mA to 45 mA
- Output current adjusted by external resistor
- Fast response of output current, $\overline{OE}$ (minimum): 100 ns
- 30-MHz clock frequency
- Schmitt-trigger inputs
- 3.0-V to 5.5-V supply voltage
- Thermal shutdown for overtemperature protection
- ESD performance: 1-kV HBM

## 2 Applications

- Gaming machine / entertainment
- General LED applications
- LED display systems
- Signs LED lighting
- White goods




**Typical Application Diagram**

## 3 Description

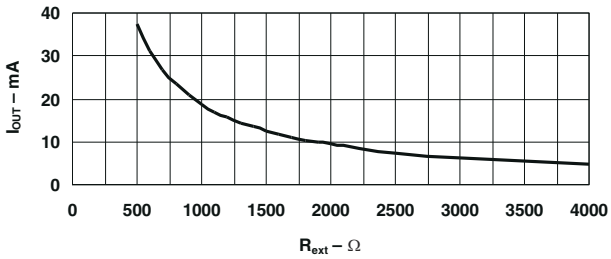
The TLC59025 device is designed for LED displays and LED lighting applications. The TLC59025 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC59025 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (for example, LED panels), the TLC59025 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor, $R_{ext}$, which gives flexibility in controlling the light intensity of LEDs. TLC59025 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The serial data is transferred into TLC59025 through SDI, shifted in the shift register, and transferred out through SDO. LE can latch the serial data in the shift register to the output latch. $\overline{OE}$ enables the output drivers to sink current.

**Device Information** (1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLC59025 | SSOP (24) | 8.65 mm × 3.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**$I_{OUT}$ vs $R_{EXT}$**

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (February 2015) to Revision C (February 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures and cross-references throughout the document | 1 |
| • Updated "$T_J$" to "$T_A$" in *Electrical Characteristics for 3-V Input Voltage* table | 5 |
| • Updated "$T_J$" to "$T_A$" in *Electrical Characteristics for 5.5-V Input Voltage* table | 6 |
| • Added note to *Constant Current* section | 13 |

| Changes from Revision A (March 2013) to Revision B (February 2015) | Page |
|---|---|
| • Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Deleted the *Ordering Information* table | 1 |

## 5 Pin Configuration and Functions

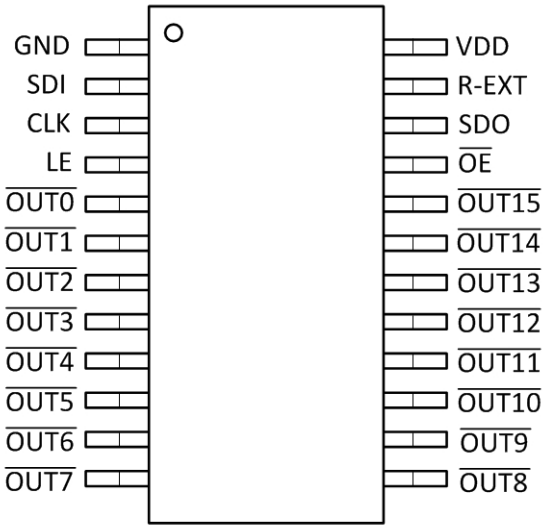



**Figure 5-1. DBQ Package 24-Pin SSOP Top View**

**Table 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CLK | 3 | I | Clock input for data shift on rising edge |
| GND | 1 | — | Ground for control logic and current sink |
| LE | 4 | I | Data strobe input<br>Serial data is transferred to the respective latch when LE is high.<br>The data is latched when LE goes low.<br>LE has an internal pulldown resistor. |
| $\overline{OE}$ | 21 | I | Output enable<br>When $\overline{OE}$ is active (low), the output drivers are enabled.<br>When $\overline{OE}$ is high, all output drivers are turned OFF (blanked).<br>$\overline{OE}$ has an internal pullup resistor. |
| $\overline{OUT0}$ | 5 | O | Constant-current output |
| $\overline{OUT1}$ | 6 | O | Constant-current output |
| $\overline{OUT2}$ | 7 | O | Constant-current output |
| $\overline{OUT3}$ | 8 | O | Constant-current output |
| $\overline{OUT4}$ | 9 | O | Constant-current output |
| $\overline{OUT5}$ | 10 | O | Constant-current output |
| $\overline{OUT6}$ | 11 | O | Constant-current output |
| $\overline{OUT7}$ | 12 | O | Constant-current output |
| $\overline{OUT8}$ | 13 | O | Constant-current output |
| $\overline{OUT9}$ | 14 | O | Constant-current output |
| $\overline{OUT10}$ | 15 | O | Constant-current output |
| $\overline{OUT11}$ | 16 | O | Constant-current output |
| $\overline{OUT12}$ | 17 | O | Constant-current output |
| $\overline{OUT13}$ | 18 | O | Constant-current output |
| $\overline{OUT14}$ | 19 | O | Constant-current output |
| $\overline{OUT15}$ | 20 | O | Constant-current output |
| R-EXT | 23 | I | Input used to connect an external resistor ($R_{ext}$) for setting output currents |
| SDI | 2 | I | Serial-data input to the Shift register |

**Table 5-1. Pin Functions (continued)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SDO | 22 | O | Serial-data output to the following SDI of next driver IC or to the microcontroller |
| VDD | 24 | — | Supply voltage |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 0 | 7 | V |
| $V_I$ | Input voltage | –0.4 | $V_{DD}$ + 0.4 | V |
| $V_O$ | Output voltage | –0.5 | 20 | V |
| $I_{OUT}$ | Output current | | 45 | mA |
| $I_{GND}$ | GND terminal current | | 750 | mA |
| $T_J$ | Operating virtual-junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 3 | 5.5 | V |
| $V_O$ | Output voltage | | | 17 | V |
| $V_{IH}$ | Input voltage | | 0.7 × $V_{DD}$ | $V_{DD}$ + 0.4 | V |
| $V_{IL}$ | Output voltage | | GND | 0.3 × $V_{DD}$ | V |
| $I_{OUT}$ | Output current | $V_O$ ≥ 0.6 V | 3 | | mA |
| | | $V_O$ ≥ 1.0 V | | 45 | mA |
| $I_{OH}$ | High-level output current, source | | –1 | | mA |
| $I_{OL}$ | Low-level output current, sink | | 1 | | mA |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | | TLC59025 DBQ (SSOP) 24 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | Mounted on JEDEC 1-layer board (JESD 51-3), No airflow | 99.8 | °C/W |
| | | Mounted on JEDEC 4-layer board (JESD 51-7), No airflow | 61 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics for 3-V Input Voltage

$V_{DD}$ = 3 V, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{leak}$ | Output leakage current | $V_{OH}$ = 17 V | $T_A$ = 25°C | | | 0.5 | µA |
| | | | $T_A$ = 125°C | | | 2 | |
| $V_{OH}$ | High-level output voltage | SDO, $I_{OL}$ = –1 mA | | $V_{DD}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | SDO, $I_{OH}$ = 1 mA | | | | 0.4 | V |
| $I_{O(1)}$ | Output current 1 | $V_{OUT}$ = 0.6 V, $R_{ext}$ = 1440 Ω | | | 13 | | mA |
| | Output current error, die-die | $I_{OL}$ = 13 mA, $V_O$ = 0.6 V, $R_{ext}$ = 1440 Ω, $T_A$ = 25°C | | | ±3% | ±6% | |
| | Output current error, channel-to-channel | $I_{OL}$ = 13 mA, $V_O$ = 0.6 V, $R_{ext}$ = 1440 Ω, $T_A$ = 25°C | | | ±1.5% | ±5% | |
| $I_{O(2)}$ | Output current 2 | $V_O$ = 0.8 V, $R_{ext}$ = 720 Ω | | | 26 | | mA |
| | Output current error, die-die | $I_{OL}$ = 26 mA, $V_O$ = 0.8 V, $R_{ext}$ = 720 Ω, $T_A$ = 25°C | | | ±3% | ±6% | |
| | Output current error, channel-to-channel | $I_{OL}$ = 26 mA, $V_O$ = 0.8 V, $R_{ext}$ = 720 Ω, $T_A$ = 25°C | | | ±1.5% | ±5% | |
| $I_{OUT}$ vs $V_{OUT}$ | Output current vs output voltage regulation | $V_O$ = 1 V to 3 V, $I_O$ = 13 mA | | | ±0.1 | | %/V |
| | | $V_{DD}$ = 3.0 V to 5.5 V, $I_O$ = 13 mA to 45 mA | | | ±1 | | |
| | Pullup resistance | $\overline{OE}$ | | | 500 | | kΩ |
| | Pulldown resistance | LE | | | 500 | | kΩ |
| $T_{sd}$ | Overtemperature shutdown (1) | | | 150 | 175 | 200 | °C |
| $T_{hys}$ | Restart temperature hysteresis | | | | 15 | | °C |
| $I_{DD}$ | Supply current | $R_{ext}$ = Open | | | 7 | 10 | mA |
| | | $R_{ext}$ = 1440 Ω | | | 9 | 12 | |
| | | $R_{ext}$ = 720 Ω | | | 11 | 13 | |
| $C_{IN}$ | Input capacitance | $V_I$ = $V_{DD}$ or GND, CLK, SDI, SDO, $\overline{OE}$ | | | | 10 | pF |

(1) Specified by design

## 6.6 Electrical Characteristics for 5.5-V Input Voltage

$V_{DD}$ = 5.5 V, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{leak}$ | Output leakage current | $V_{OH}$ = 17 V | $T_A$ = 25°C | | | 0.5 | µA |
| | | | $T_A$ = 125°C | | | 2 | |
| $V_{OH}$ | High-level output voltage | SDO, $I_{OL}$ = –1 mA | | $V_{DD}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | SDO, $I_{OH}$ = 1 mA | | | | 0.4 | V |
| $I_{O(1)}$ | Output current 1 | $V_{OUT}$ = 0.6 V, $R_{ext}$ = 1440 Ω | | | 13 | | mA |
| | Output current error, die-die | $I_{OL}$ = 13 mA, $V_O$ = 0.6 V, $R_{ext}$ = 1440 Ω, $T_A$ = 25°C | | | ±3% | ±6% | |
| | Output current error, channel-to-channel | $I_{OL}$ = 13 mA, $V_O$ = 0.6 V, $R_{ext}$ = 1440 Ω, $T_A$ = 25°C | | | ±1.5% | ±5% | |
| $I_{O(2)}$ | Output current 2 | $V_O$ = 0.8 V, $R_{ext}$ = 720 Ω | | | 26 | | mA |
| | Output current error, die-die | $I_{OL}$ = 26 mA, $V_O$ = 0.8 V, $R_{ext}$ = 720 Ω, $T_A$ = 25°C | | | ±3% | ±6% | |
| | Output current error, channel-to-channel | $I_{OL}$ = 26 mA, $V_O$ = 0.8 V, $R_{ext}$ = 720 Ω, $T_A$ = 25°C | | | ±1.5% | ±5% | |
| $I_{OUT}$ vs $V_{OUT}$ | Output current vs output voltage regulation | $V_O$ = 1 V to 3 V , $I_O$ = 26 mA | | | ±0.1 | | %/V |
| | | $V_{DD}$ = 3.0 V to 5.5 V, $I_O$ = 13 mA to 45 mA | | | ±1 | | |
| | Pullup resistance | $\overline{OE}$ | | | 500 | | kΩ |
| | Pulldown resistance | LE | | | 500 | | kΩ |
| $T_{sd}$ | Overtemperature shutdown (1) | | | 150 | 175 | 200 | °C |
| $T_{hys}$ | Restart temperature hysteresis | | | | 15 | | °C |
| $I_{DD}$ | Supply current | $R_{ext}$ = Open | | | 9 | 11 | mA |
| | | $R_{ext}$ = 1440 Ω | | | 12 | 14 | |
| | | $R_{ext}$ = 720 Ω | | | 14 | 16 | |
| $C_{IN}$ | Input capacitance | $V_I$ = $V_{DD}$ or GND, CLK, SDI, SDO, $\overline{OE}$ | | | | 10 | pF |

(1) Specified by design

## 6.7 Power Dissipation Ratings

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Power dissipation | Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, $T_A$ = 25°C, $T_J$ = 125°C | DBQ package | | 1.6 | W |

## 6.8 Timing Requirements

$V_{DD}$ = 3 V to 5.5 V (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(L)}$ | LE pulse duration | | 15 | | ns |
| $t_{w(CLK)}$ | CLK pulse duration | | 15 | | ns |
| $t_{w(OE)}$ | $\overline{OE}$ pulse duration | | 300 | | ns |
| $t_{su(D)}$ | Setup time for SDI | | 3 | | ns |
| $t_{h(D)}$ | Hold time for SDI | | 2 | | ns |
| $t_{su(L)}$ | Setup time for LE | | 5 | | ns |
| $t_{h(L)}$ | Hold time for LE | | 5 | | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation | | 30 | MHz |

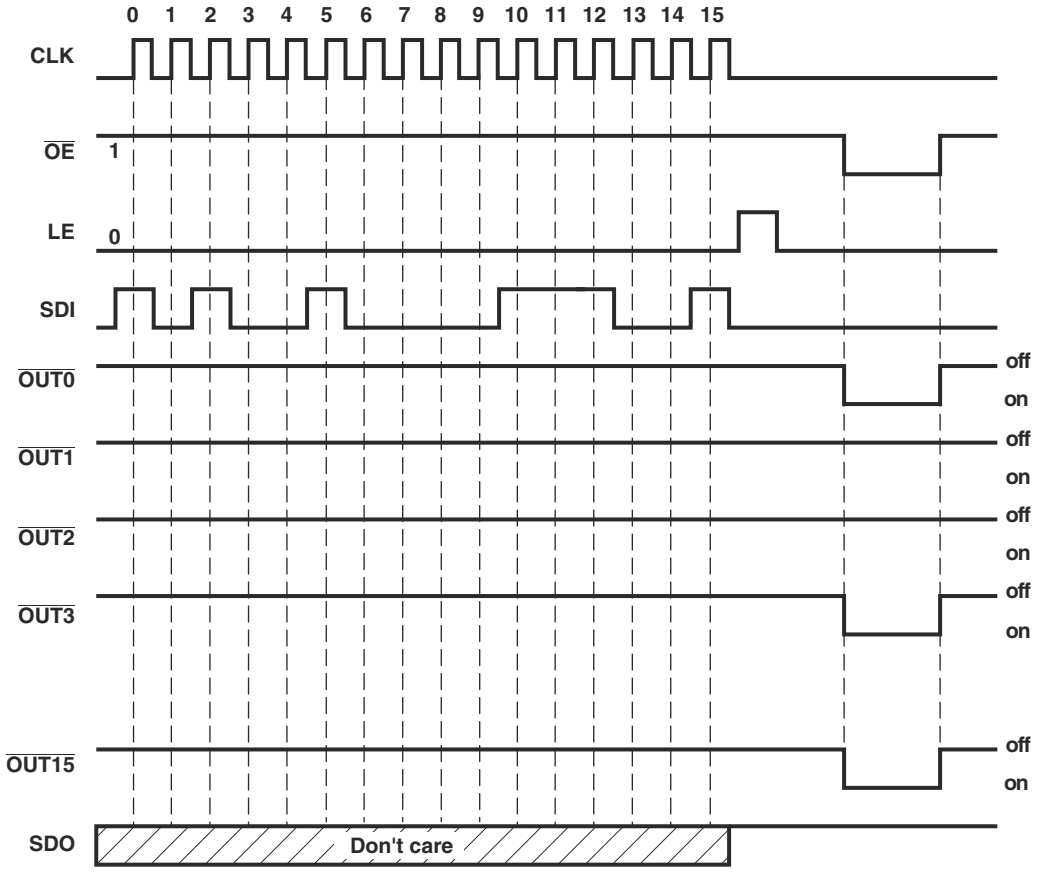



**Figure 6-1. Timing Diagram**

## 6.9 Switching Characteristics for 3-V Input Voltage

$V_{DD}$ = 3 V, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH1}$ | Low-to-high propagation delay time, CLK to $\overline{OUTn}$ | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = GND, $R_{ext}$ = 720 Ω, $V_L$ = 4 V, $R_L$ = 88 Ω, $C_L$ = 10 pF | 30 | 45 | 60 | ns |
| $t_{PLH2}$ | Low-to-high propagation delay time, LE to $\overline{OUTn}$ | | 30 | 45 | 60 | ns |
| $t_{PLH3}$ | Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$ | | 30 | 45 | 60 | ns |
| $t_{PLH4}$ | Low-to-high propagation delay time, CLK to SDO | | | 30 | 40 | ns |
| $t_{PHL1}$ | High-to-low propagation delay time, CLK to $\overline{OUTn}$ | | 40 | 65 | 100 | ns |
| $t_{PHL2}$ | High-to-low propagation delay time, LE to $\overline{OUTn}$ | | 40 | 65 | 100 | ns |
| $t_{PHL3}$ | High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$ | | 40 | 65 | 100 | ns |
| $t_{PHL4}$ | High-to-low propagation delay time, CLK to SDO | | | 30 | 40 | ns |
| $t_{w(CLK)}$ | Pulse duration, CLK | | 15 | | | ns |
| $t_{w(L)}$ | Pulse duration LE | | 15 | | | ns |
| $t_{w(OE)}$ | Pulse duration, $\overline{OE}$ | | 300 | | | ns |
| $t_{h(D)}$ | Hold time, SDI | | 2 | | | ns |
| $t_{su(D)}$ | Setup time, SDI | | 3 | | | ns |
| $t_{h(L)}$ | Hold time, LE | | 5 | | | ns |
| $t_{su(L)}$ | Setup time, LE | | 5 | | | ns |
| $t_r$ | Rise time, CLK (1) | | | | 500 | ns |
| $t_f$ | Fall time, CLK (1) | | | | 500 | ns |
| $t_{or}$ | Rise time, outputs (off) | | 35 | 50 | 70 | ns |
| $t_{of}$ | Rise time, outputs (on) | | 15 | 50 | 120 | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation | | | 30 | MHz |

(1) If the devices are connected in cascade and $t_r$ or $t_f$ is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

## 6.10 Switching Characteristics for 5.5-V Input Voltage

$V_{DD}$ = 5.5 V, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH1}$ | Low-to-high propagation delay time, CLK to $\overline{OUTn}$ | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = GND, $R_{ext}$ = 720 Ω, $V_L$ = 4 V, $R_L$ = 88 Ω, $C_L$ = 10 pF | 20 | 35 | 55 | ns |
| $t_{PLH2}$ | Low-to-high propagation delay time, LE to $\overline{OUTn}$ | | 20 | 35 | 55 | ns |
| $t_{PLH3}$ | Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$ | | 20 | 35 | 55 | ns |
| $t_{PLH4}$ | Low-to-high propagation delay time, CLK to SDO | | | 20 | 30 | ns |
| $t_{PHL1}$ | High-to-low propagation delay time, CLK to $\overline{OUTn}$ | | 15 | 28 | 42 | ns |
| $t_{PHL2}$ | High-to-low propagation delay time, LE to $\overline{OUTn}$ | | 15 | 28 | 42 | ns |
| $t_{PHL3}$ | High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$ | | 15 | 28 | 42 | ns |
| $t_{PHL4}$ | High-to-low propagation delay time, CLK to SDO | | | 20 | 30 | ns |
| $t_{w(CLK)}$ | Pulse duration, CLK | | 10 | | | ns |
| $t_{w(L)}$ | Pulse duration LE | | 10 | | | ns |
| $t_{w(OE)}$ | Pulse duration, $\overline{OE}$ | | 200 | | | ns |
| $t_{h(D)}$ | Hold time, SDI | | 2 | | | ns |
| $t_{su(D)}$ | Setup time, SDI | | 3 | | | ns |
| $t_{h(L)}$ | Hold time, LE | | 5 | | | ns |
| $t_{su(L)}$ | Setup time, LE | | 5 | | | ns |
| $t_r$ | Rise time, CLK (1) | | | | 500 | ns |
| $t_f$ | Fall time, CLK (1) | | | | 500 | ns |
| $t_{or}$ | Rise time, outputs (off) | | 25 | 45 | 65 | ns |
| $t_{of}$ | Rise time, outputs (on) | | 7 | 12 | 20 | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation | | | 30 | MHz |

(1) If the devices are connected in cascade and $t_r$ or $t_f$ is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

## 6.11 Typical Characteristics

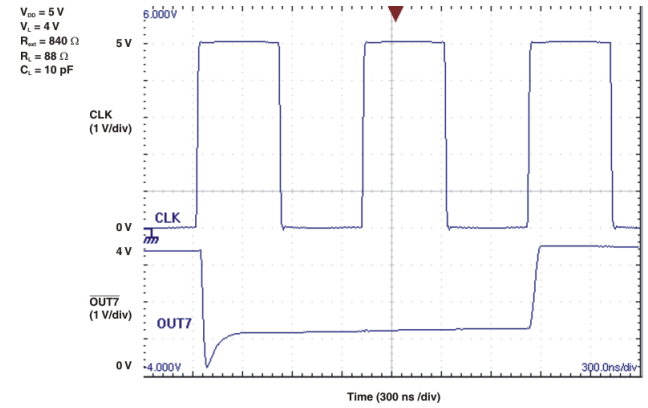



**Figure 6-2. CLK to $\overline{OUT7}$**

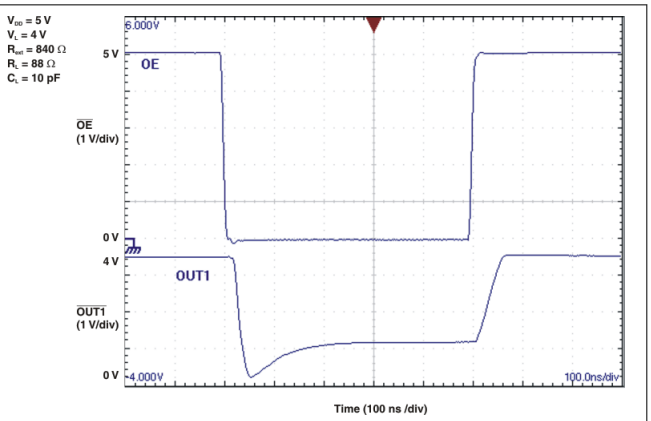



**Figure 6-3. $\overline{OE}$ to $\overline{OUT1}$**

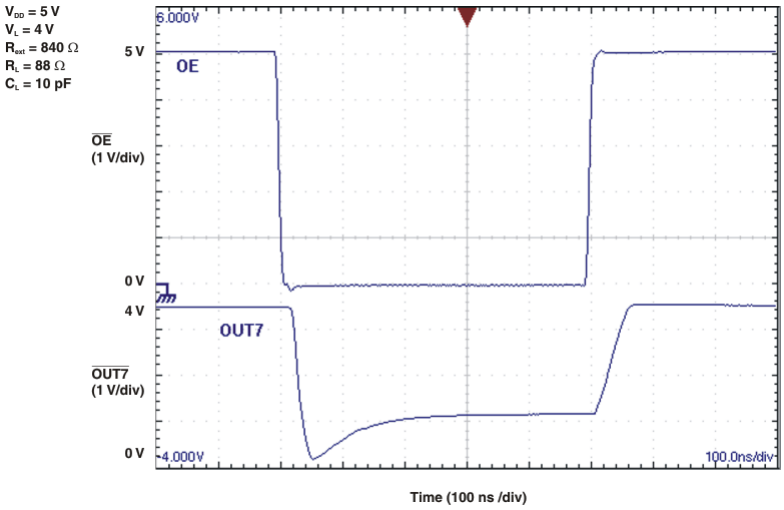



**Figure 6-4. $\overline{OE}$ to $\overline{OUT7}$**

# 7 Parameter Measurement Information

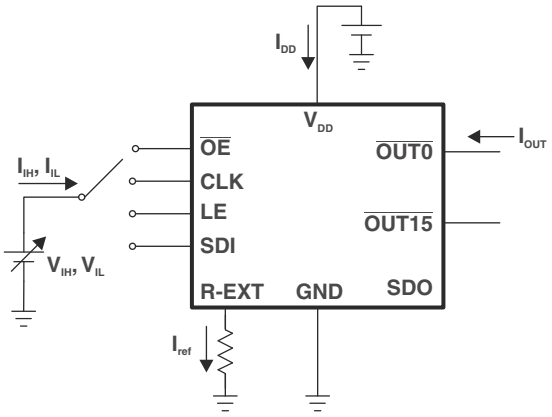



**Figure 7-1. Test Circuit for Electrical Characteristics**

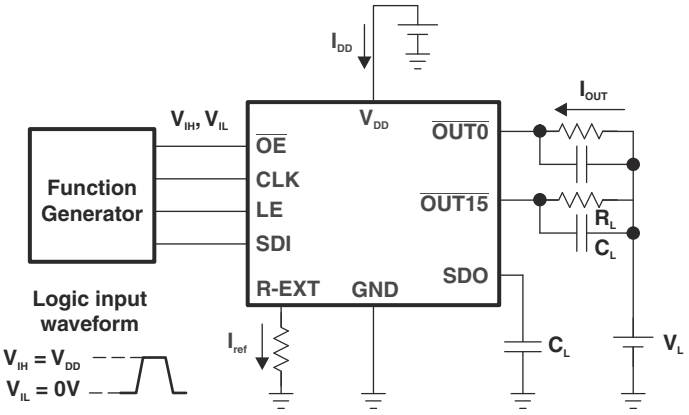



**Figure 7-2. Test Circuit for Switching Characteristics**

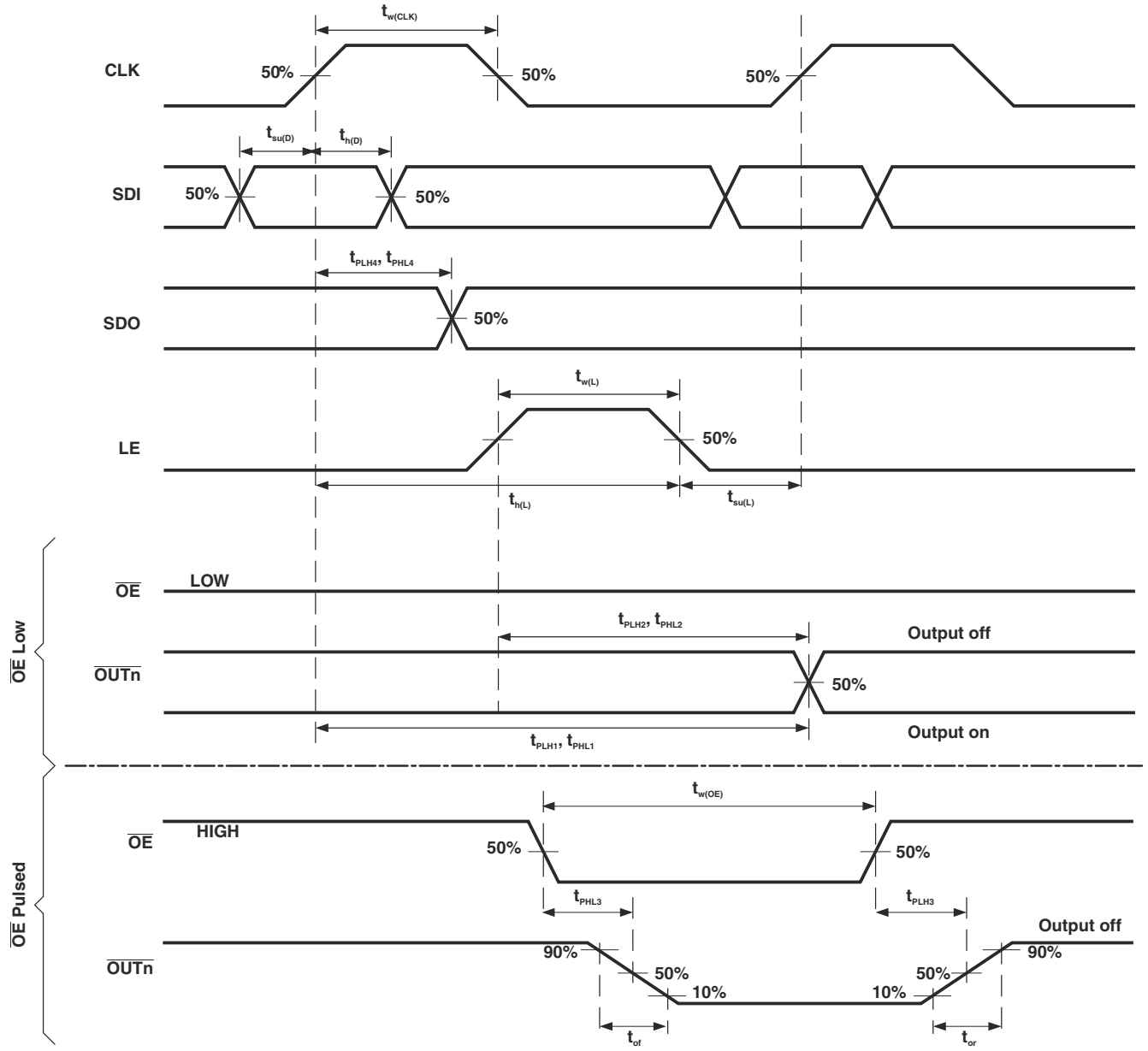


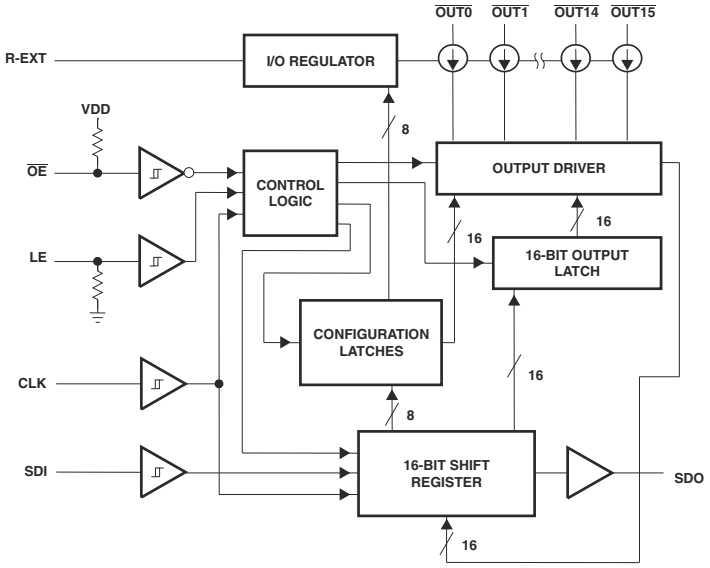

**Figure 7-3. Normal Mode Timing Waveforms**

# 8 Detailed Description

## 8.1 Overview

The TLC59025 is a 16-channel LED driver designed for LED displays and LED lighting applications. The TLC59025 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC59025 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (for example, LED panels), the TLC59025 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor, $R_{EXT}$, which gives flexibility in controlling the light intensity of LEDs. TLC59025 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Constant Current

In LED display applications, TLC59025 provides nearly no current variations from channel to channel and from IC to IC. While $I_{OUT} \leq 45$ mA, the maximum current skew between channels is less than ±5% and between ICs is less than ±6%.

**Note**

When the TLC59025 is used in very low current applications, reduced current accuracy can be expected. For example, current accuracy is estimated to degrade to as much as ±10% when Iout = 1.7 mA.

## 8.4 Device Functional Modes

Table 8-1 lists the functional modes for the TLC59025.

**Table 8-1. Truth Table in Normal Operation**

| CLK | LE | $\overline{OE}$ | SDI | $\overline{OUT0}$... $\overline{OUT15}$... $\overline{OUT15}$ | SDO |
|---|---|---|---|---|---|
| ↑ | H | L | Dn | Dn...Dn – 7...Dn – 15 | Dn – 15 |
| ↑ | L | L | Dn + 1 | No change | Dn – 14 |
| ↑ | H | L | Dn + 2 | Dn + 2...Dn – 5...Dn – 13 | Dn – 13 |
| ↓ | X | L | Dn + 3 | Dn + 2...Dn – 5...Dn – 13 | Dn – 13 |
| ↓ | X | H | Dn + 3 | off | Dn – 13 |

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Turning on the LEDs

To turn on an LED connected to one of the outputs of the device, the output must be pulled low. To do this, the SDI signal must let the device know which outputs should be activated. Using the rising edge of CLK, the logic level of the SDI signal latches the desired state of each output into the shift register. Once this is complete, the LE signal must be toggled from low to high then back to low. Once /OE is pulled down, the corresponding outputs will be pulled low and the LEDs will be turned on. The below diagram shows outputs 0, 3, 4, 5, 10, 13, and 15 being activated.

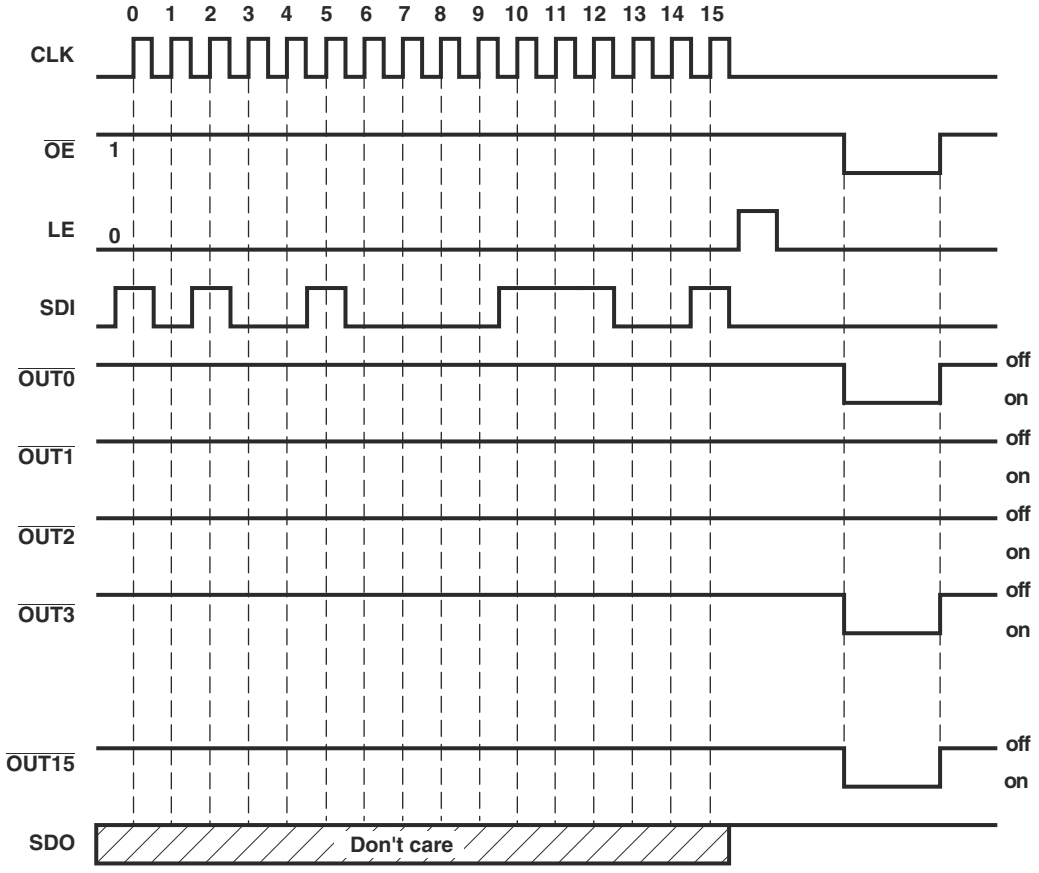



**Figure 9-1. Timing Diagram**

## 9.2 Typical Application

This application shows how to calculate the output current for $\overline{OUT0}$ through $\overline{OUT15}$.

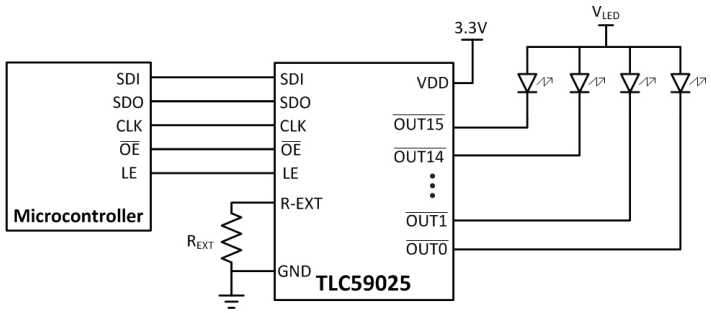



**Figure 9-2. Typical Application Diagram**

### 9.2.1 Design Requirements

For the following design procedure, the input voltage ($V_{DD}$) is between 3 V and 5.5 V.

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Adjusting Output Current*

TLC59025 sets $I_{OUT}$ based on the external resistor $R_{EXT}$. Users can follow the below formula to calculate the target output current $I_{OUT,target}$ in the saturation region:

$I_{OUT,target} = (1.21\ V / R_{EXT}) \times 15.5$

Where $R_{EXT}$ is the external resistance connected between R-EXT and GND. Using this equation, the output current is calculated to be approximately 26 mA at 720 Ω and 13 mA at 1440 Ω.

### 9.2.3 Application Curve

The default relationship after power on between $I_{OUT,target}$ and $R_{EXT}$ is shown in Figure 9-3.

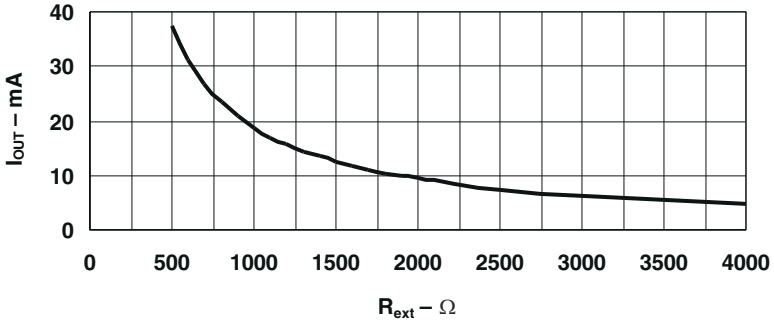



**Figure 9-3. Default Relationship Curve Between $I_{OUT,target}$ and $R_{ext}$ After Power Up**

# 10 Power Supply Recommendations

The TLC59025 is designed to operate with a VDD range between 3 V and 5.5 V.

# 11 Layout

## 11.1 Layout Guidelines

The SDI, CLK, SDO, LE, and $\overline{OE}$ signals should all be kept from potential noise sources.

All traces carrying power through the LEDs should be wide enough to handle necessary currents.

All LED current passes through the device and into the ground node. There must be a strong connection between the device ground and the circuit board ground.

## 11.2 Layout Example

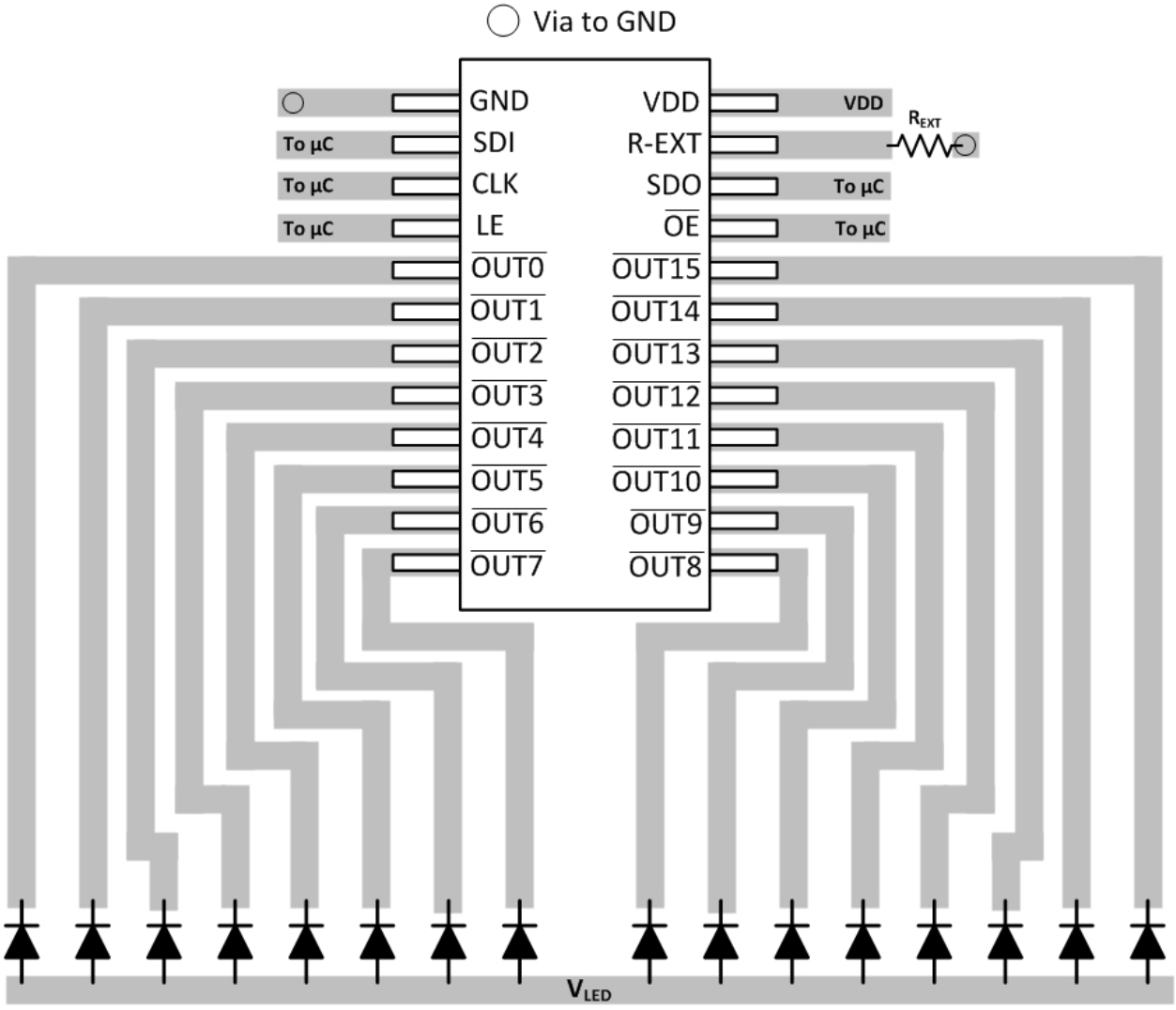



**Figure 11-1. Layout Recommendation**

# 12 Device and Documentation Support

## 12.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.2 Trademarks

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## 12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.4 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLC59025IDBQR | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLC59025I |
| TLC59025IDBQR.B | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLC59025I |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

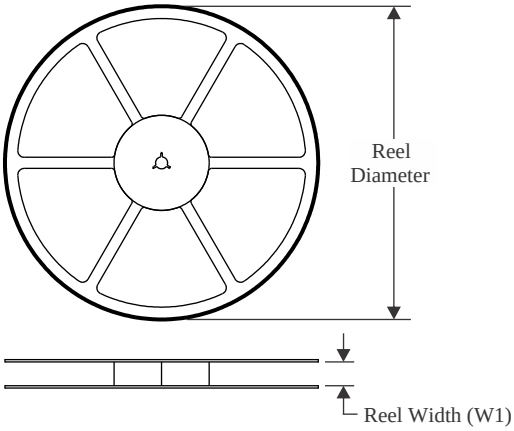
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

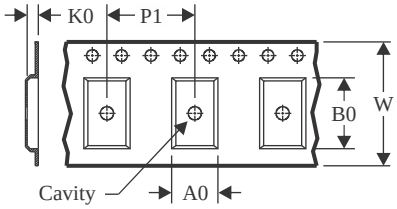
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

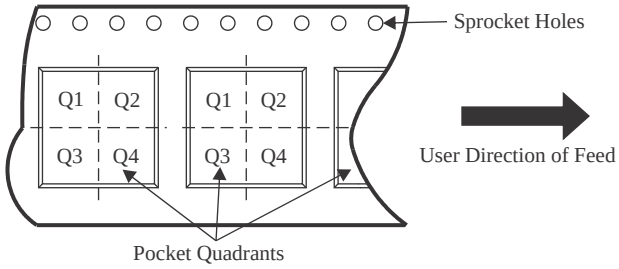



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

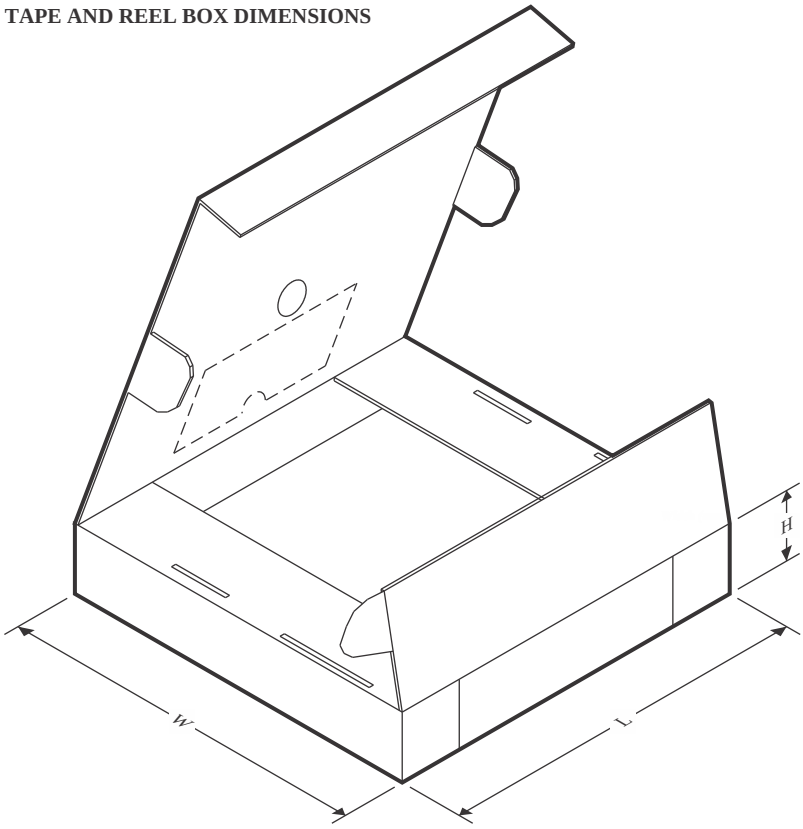
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLC59025IDBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

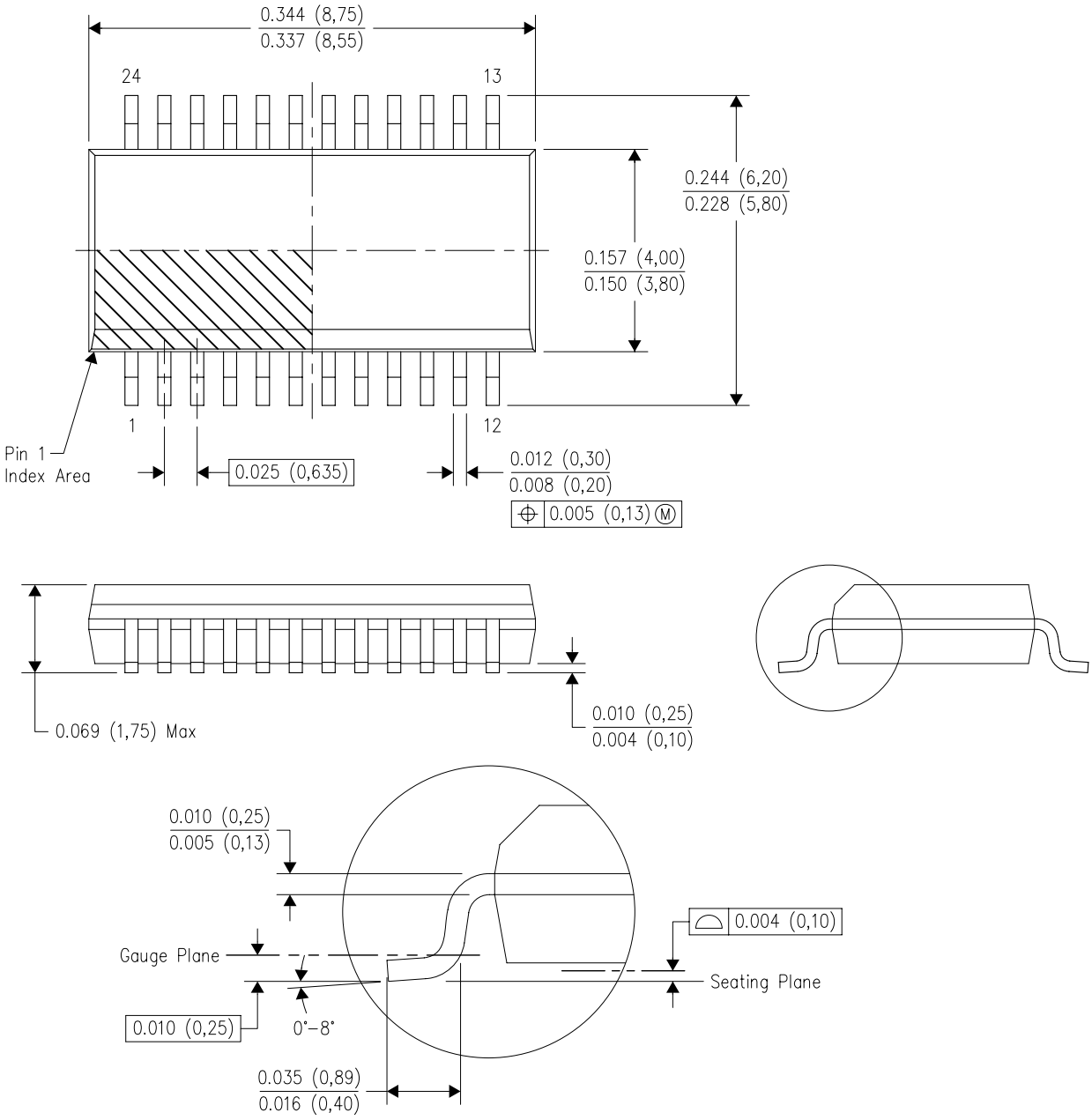
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLC59025IDBQR | SSOP | DBQ | 24 | 2500 | 353.0 | 353.0 | 32.0 |

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

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Last updated 10/2025