TLC556x Dual CMOS Timers

1 Features

- Very low power consumption:
  - 2mW typical at V_{DD} = 5V
- Capable of operation in a stable mode
- CMOS output capable of swinging rail to rail
- High output-current capability
  - Sink: 100mA typical
  - Source: 10mA typical
- Output fully compatible with CMOS, TTL, and MOS
- Low supply current reduces spikes during output transitions
- Single-supply operation from 2V to 15V
- Functionally interchangeable with the NE556; has same pinout

2 Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

3 Description

The TLC556 series are CMOS monolithic timing circuits. The timers are fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2MHz. Because of high input impedance, this device supports smaller timing capacitors than those supported by the NE556. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage pin (CONT). When the trigger input (TRIG) is less than the trigger level, the flip-flop is set and the output goes high. If TRIG is greater than the trigger level and the threshold input (THRES) is greater than the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) overrides all other inputs and is used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge pin (DISCH) and the ground pin (GND). Tie all unused inputs to an appropriate logic level to prevent false triggering.

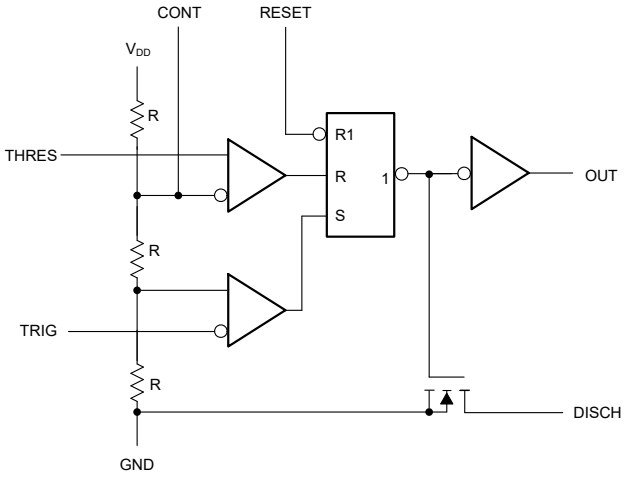
Although the CMOS output is capable of sinking over 100mA and sourcing over 10mA, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This feature minimizes the need for the large decoupling capacitors required by the NE556.

The TLC556C is characterized for operation from 0°C to 70°C. The TLC556I is characterized for operation from −40°C to +85°C. The TLC556M is characterized for operation over the full military temperature range of −55°C to +125°C.

Device Information

PART NUMBER	RATING	PACKAGE(1)
TLC556C	Catalog	D (SOIC, 14)
		N (PDIP, 14)
TLC556I	Industrial	D (SOIC, 14)
		N (PDIP, 14)
TLC556M	Military	D (SOIC, 14)
		FK (LCCC, 20)
		J (CDIP, 14)
		N (PDIP, 14)

(1) For more information, see Section 10.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

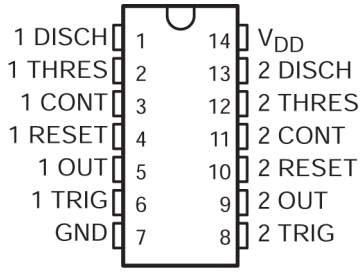

Figure 4-1. D, J, or N Package (Top View)

Table 4-1. Pin Functions: D, J, and N Packages

PIN		TYPE	DESCRIPTION
NAME	NO.		
CONT	3, 11	Input	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	1, 13	Output	Open collector output to discharge timing capacitor.
GND	7	—	Ground.
OUT	5, 9	Output	High current timer output signal.
RESET	4, 10	Input	Active low reset input forces output and discharge low.
THRES	2, 12	Input	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	6, 8	Input	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V_{DD}	14	—	Power-supply voltage.

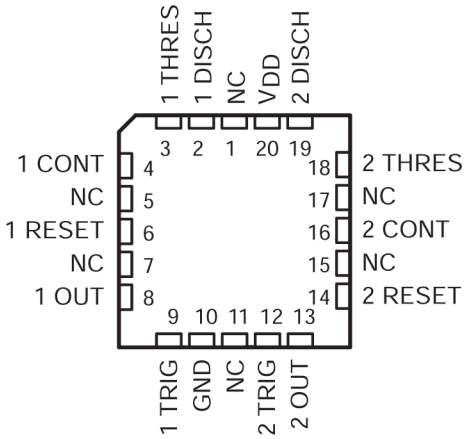

Figure 4-2. FK Package (Top View)

Table 4-2. Pin Functions: FK Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
CONT	4, 16	Input	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	2, 19	Output	Open-collector output to discharge timing capacitor.
GND	10	—	Ground.
NC	1, 5, 7, 11, 15, 17	—	No internal connection.
OUT	8, 13	Output	High current timer output signal.
RESET	6, 14	Input	Active low reset input forces output and discharge low.
THRES	3, 18	Input	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	9, 12	Input	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V_{DD}	20	—	Power-supply voltage.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Voltage	Supply voltage, V_{DD} (2)	–0.3	18	V
		Input, any input	–0.3	V_{DD}	
	Current	Sink, discharge or output		150	mA
		Source, output		15	
T_A	Operating free-air temperature	C-suffix	0	70	°C
		I-suffix	–40	85	
		M-suffix	–55	125	
	Case temperature for 60 seconds	FK package		260	°C
	Lead temperature 1.6mm (1/16 inch) from case	J package, 60 seconds		300	°C
		D or N package, 10 seconds		260	
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(3)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) See Section 7.1.1 for application guidance on protecting the device against ESD.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2	15	V
T_A	Operating free-air temperature	TLC556C	0	70	°C
		TLC556I	−40	85	
		TLC556M	−55	125	

5.4 Thermal Information

THERMAL METRIC(1)		TLC556				UNIT
		D (SOIC)	FK (LCCC)	J (CDIP)	N (PDIP)	
		14 PINS	20 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.1	63.8	80.6	75.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	39.1	33.5	54.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.2	38.5	68.2	50.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	33.3	26.9	31.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.6	38.3	63.2	49.4	°C/W

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5.4 Thermal Information (continued)

THERMAL METRIC[1]		TLC556				UNIT
		D (SOIC)	FK (LCCC)	J (CDIP)	N (PDIP)	
		14 PINS	20 PINS	14 PINS	14 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.7	15.2	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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5.5 Electrical Characteristics: V_{DD} = 2V for TLC556C, V_{DD} = 3V for TLC556I

at specified free-air temperature, V_{DD} = 2V for TLC556C, AND V_{DD} = 3V for TLC556I (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage	25°C	TLC556C	0.95	1.33	1.65	V
			TLC556I	1.6	2	2.4	
		Full range[1]	TLC556C	0.85		1.75	
			TLC556I	1.5		2.5	
	Threshold current	25°C			10		pA
		Full range[1]	TLC556C		75		
			TLC556I		150		
$V_{(trigger)}$	Trigger voltage	25°C	TLC556C	0.4	0.67	0.95	V
			TLC556I	0.71	1	1.29	
		Full range[1]	TLC556C	0.3		1.05	
			TLC556I	0.61		1.39	
$I_{(trigger)}$	Trigger current	25°C			10		pA
		Full range[1]	TLC556C		75		
			TLC556I		150		
$V_{(reset)}$	Reset voltage	25°C		0.4	1.1	1.5	V
		Full range[1]		0.3		1.8	
$I_{(reset)}$	Reset current	25°C			10		pA
		Full range[1]	TLC556C		75		
			TLC556I		150		
	Control voltage (open circuit) as a percentage of supply voltage	Full range[1]			66.7%		
	Discharge switch on-state voltage	I_{OL} = 1mA, 25°C	TLC556C		0.04	0.2	V
			TLC556I		0.03	0.2	
		I_{OL} = 1mA, Full range[1]	TLC556C			0.25	
			TLC556I			0.375	
	Discharge switch off-state current	25°C			0.33		nA
		Full range[1]	TLC556C		11		
			TLC556I		30		
V_{OH}	High-level output voltage	I_{OH} = –300µA, 25°C		1.5	1.9		V
		I_{OH} = –300µA, full range[1]	TLC556C	1.5			
			TLC556I	2.5			
V_{OL}	Low-level output voltage	I_{OL} = 1mA, 25°C			0.07	0.3	V
		I_{OL} = 1mA, full range[1]	TLC556C			0.35	
			TLC556I			0.4	
I_{DD}	Supply current[2]	25°C			275	500	mA
		Full range[1]	TLC556C			800	
			TLC556I			1000	

(1) Full range is 0°C to 70°C for TLC556C and −40°C to +85°C for TLC556I.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

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5.6 Electrical Characteristics: V_{DD} = 5V

at specified free-air temperature and V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage	25°C		2.8	3.3	3.8	V
		Full range		2.7		3.9	
	Threshold current	25°C			10		pA
		Full range[1]	TLC556C		75		
			TLC556I		150		
			TLC556M		5000		
$V_{(trigger)}$	Trigger voltage	25°C		1.36	1.66	1.96	V
		Full range		1.26		2.06	
$I_{(trigger)}$	Trigger current	25°C			10		pA
		Full range[1]	TLC556C		75		
			TLC556I		150		
			TLC556M		5000		
$V_{(reset)}$	Reset voltage	25°C		0.4	1.1	1.5	V
		Full range		0.3		1.8	
$I_{(reset)}$	Reset current	25°C			10		pA
		Full range[1]	TLC556C		75		
			TLC556I		150		
			TLC556M		5000		
	Control voltage (open circuit) as a percentage of supply voltage	Full range[1]			66.7%		
	Discharge switch on-state voltage	I_{OL} = 10mA, 25°C	TLC556C, TLC556I		0.06	0.5	V
			TLC556M		0.15	0.5	
		I_{OL} = 10mA, full range[1]	TLC556C, TLC556I			0.6	
			TLC556M		0.6		
	Discharge switch off-state current	25°C	TLC556C, TLC556I		0.3		nA
			TLC556M		0.1		
		Full range[1]	TLC556C		11		
			TLC556I		30		
			TLC556M		120		
V_{OH}	High-level output voltage	I_{OH} = –1mA	25°C	4.1	4.8		V
			Full range[1]	4.1			

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5.6 Electrical Characteristics: V_{DD} = 5V (continued)

at specified free-air temperature and V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 8mA, 25°C			0.21	0.4	V
		I_{OL} = 8mA, full range(1)	TLC556C, TLC556I			0.5	
			TLC556M			0.6	
		I_{OL} = 5mA, 25°C			0.13	0.3	
		I_{OL} = 5mA, full range(1)	TLC556C, TLC556I			0.4	
			TLC556M			0.45	
		I_{OL} = 3.2mA, 25°C			0.08	0.3	
		I_{OL} = 3.2mA, full range(1)	TLC556C, TLC556I			0.35	
			TLC556M			0.4	
I_{DD}	Supply current(2)	25°C			360	700	µA
		Full range(1)	TLC556C			1000	
			TLC556I			1200	
			TLC556M			1400	

(1) Full range is 0°C to 70°C for TLC556C, −40°C to +85°C for TLC556I, and −55°C to +125°C for TLC556M.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

5.7 Electrical Characteristics: V_{DD} = 15V

at specified free-air temperature and V_{DD} = 15V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage	25°C		9.45	10	10.55	V
		Full range(1)		9.35		10.65	
	Threshold current	25°C			10		pA
		Full range(1)	TLC556C		75		
			TLC556I		150		
			TLC556M		5000		
$V_{(trigger)}$	Trigger voltage	25°C		4.65	5	5.35	V
		Full range(1)		4.55		5.45	
$I_{(trigger)}$	Trigger current	25°C			10		pA
		Full range(1)	TLC556C		75		
			TLC556I		150		
			TLC556M		5000		
$V_{(reset)}$	Reset voltage	25°C		0.4	1.1	1.5	V
		Full range(1)		0.3		1.8	
$I_{(reset)}$	Reset current	25°C			10		pA
		Full range(1)	TLC556C		75		
			TLC556I		150		
			TLC556M		5000		
	Control voltage (open circuit) as a percentage of supply voltage	Full range(1)			66.7%		

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5.7 Electrical Characteristics: V_{DD} = 15V (continued)

at specified free-air temperature and V_{DD} = 15V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Discharge switch on-state voltage	I_{OL} = 100mA	25°C		0.8	1.7	V
			Full range[1]			1.8	
	Discharge switch off-state current	25°C	TLC556C, TLC556I		0.75		nA
			TLC556M		0.1		
		Full range[1]	TLC556C		13		
			TLC556I		30		
			TLC556M		120		
V_{OH}	High-level output voltage	I_{OH} = –10mA	25°C	12.5	14.2		V
			Full range[1]	12.5			
		I_{OH} = –5mA	25°C	13.5	14.6		
			Full range[1]	13.5			
		I_{OH} = –1mA	25°C	14.2	14.9		
			Full range[1]	14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100mA, 25°C			1.28	3.2	V
		I_{OL} = 100mA, full range[1]	TLC556C			3.6	
			TLC556I			3.7	
			TLC556M			3.8	
		I_{OL} = 50mA, 25°C			0.63	1	
		I_{OL} = 50mA, full range[1]	TLC556C			1.3	
			TLC556I			1.4	
			TLC556M			1.5	
		I_{OL} = 10mA, 25°C			0.12	0.3	
		I_{OL} = 10mA, full range[1]	TLC556C, TLC556I			0.4	
			TLC556M			0.45	
I_{DD}	Supply current[2]	25°C	TLC556C, TLC556I		0.47	1.2	mA
			TLC556M		0.72	1.2	
		Full range[1]	TLC556C			1.6	
			TLC556I			1.8	
			TLC556M			2	

(1) Full range is 0°C to 70°C for TLC556C, –40°C to +85°C for TLC556I, and –55°C to +125°C for TLC556M.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

5.8 Switching Characteristics

at V_{DD} = 5V and T_A = 25°C (unless otherwise noted); characteristic values are specified by design, characterization, or both

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Supply voltage sensitivity of timing interval	V_{DD} = 5V to 15V, R_A = R_B = 1kΩ to 100kΩ, C_T = 0.1µF[1]		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10MΩ, C_L = 10pF		20	75	ns
t_f	Output pulse fall time	R_L = 10MΩ, C_L = 10pF		15	60	ns
f_{max}	Maximum frequency in astable mode	R_A = 470Ω, C_T = 200pF, R_B = 200Ω[1]	1.2	2.1		MHz

(1) R_A, R_B, and C_T are as defined in Figure 6-2.

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5.9 Typical Characteristics: TLC556C and TLC556I

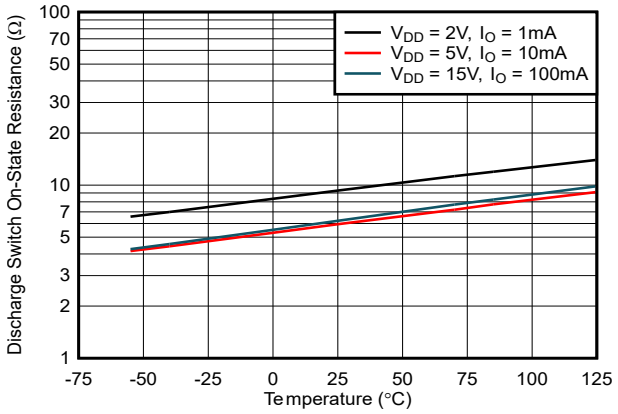

Figure 5-1. Discharge Switch On-State Resistance vs Free-Air Temperature

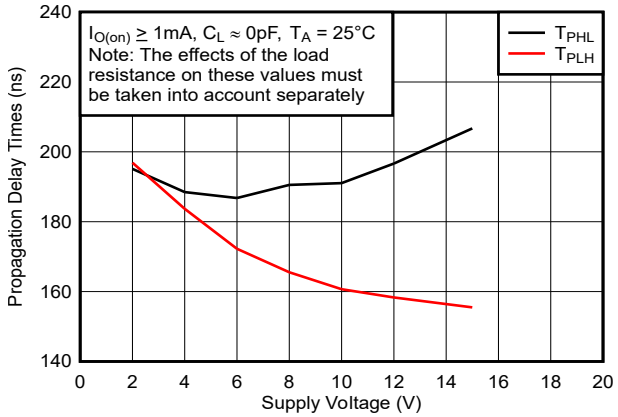

Figure 5-2. Propagation Delay Times (to Discharge Output From Trigger and Threshold Shorted Together) vs Supply Voltage

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5.10 Typical Characteristics: TLC556M

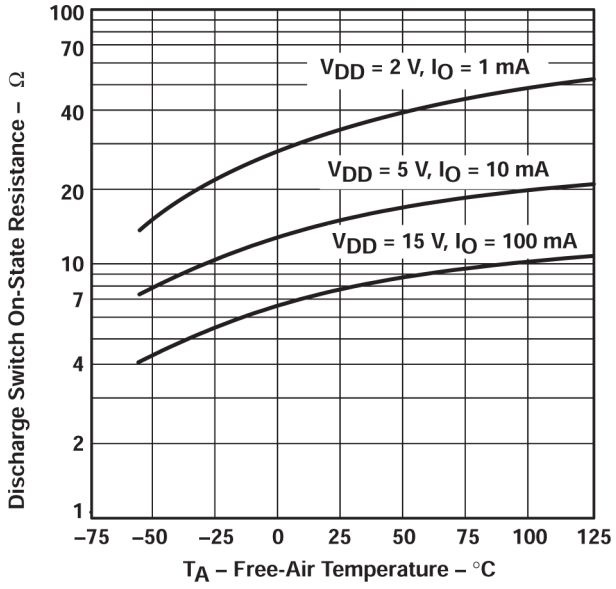
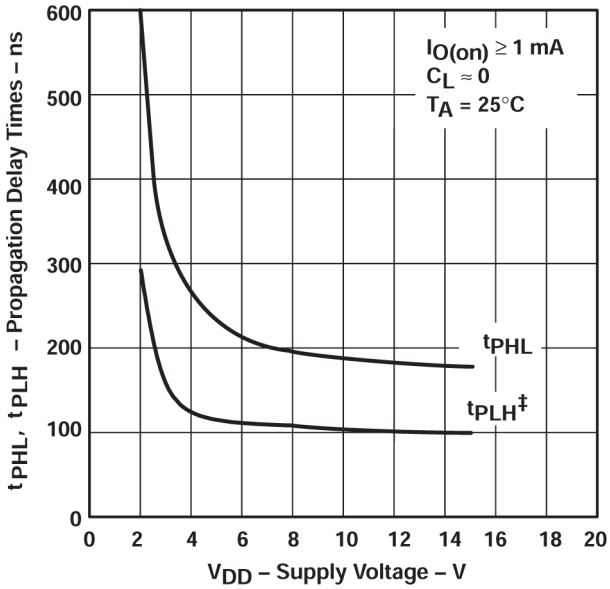


Figure 5-3. Discharge Switch On-State Resistance vs Free-Air Temperature



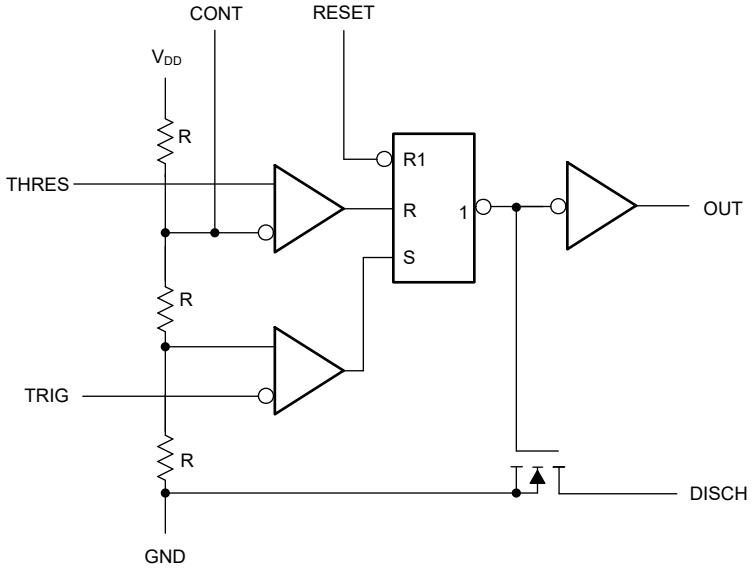
Take the effects of the load resistance on these values into account separately.

Figure 5-4. Propagation Delay Times (to Discharge Output From Trigger and Threshold Shorted Together) vs Supply Voltage

6 Detailed Description

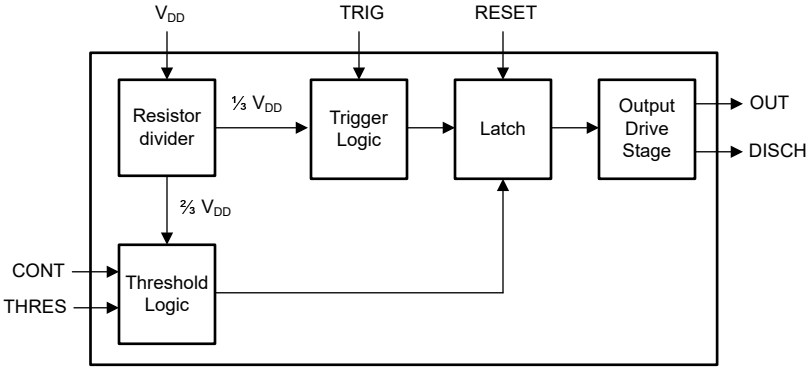
6.1 Overview

The TLC556 is a precision timing device used for general-purpose timing applications up to 2.1MHz. All inputs are level sensitive, not edge-triggered inputs. RESET overrides TRIG, which overrides THRES (when CONT pin is 2/3 V_{DD}). The resistance of R resistors vary with V_{DD} and temperature. The resistors match each other very well across V_{DD} and temperature for a temperature-stable control-voltage ratio.



Simplified Schematic

6.2 Functional Block Diagram (Each Timer)



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6.3 Feature Description

6.3.1 Monostable Operation

For monostable operation, Figure 6-1 shows how either of the timers can be connected. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal latch; the output goes high, and discharge pin (DISCH) becomes open drain. Capacitor C_T then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the internal latch, the output goes low, the discharge pin goes low, which quickly discharges capacitor C_T.

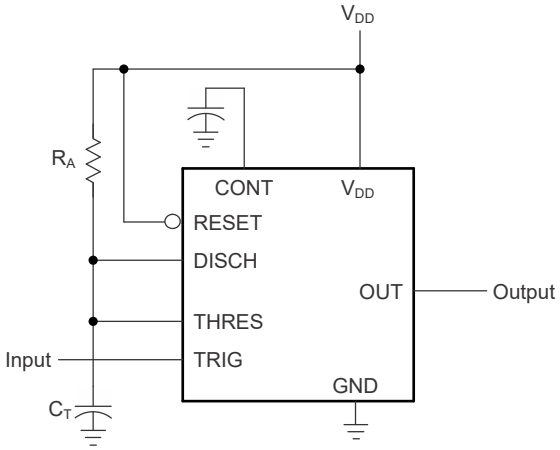

Figure 6-1. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage is less than the trigger threshold. If initiated, the sequence ends only if TRIG is high for at least 1µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 1µs, which limits the minimum monostable pulse duration to 1µs. The output pulse duration is approximately $t_w = 1.1 \times R_A C_T$. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{DD}. The timing interval is, therefore, independent of the supply voltage, as long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges capacitor C_T and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not asserted low, connect RESET to V_{DD}. If the RESET function is required and the pin is driven by external logic or a microcontroller, use a pullup resistor to V_{DD} (such as 10kΩ) to prevent the RESET pin from floating. If the RESET function is not required, short the RESET pin directly to the V_{DD} pin.

In monostable applications, set the trip point of the trigger input by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage, from a resistor divider with at least 500µA bias, provides good results.

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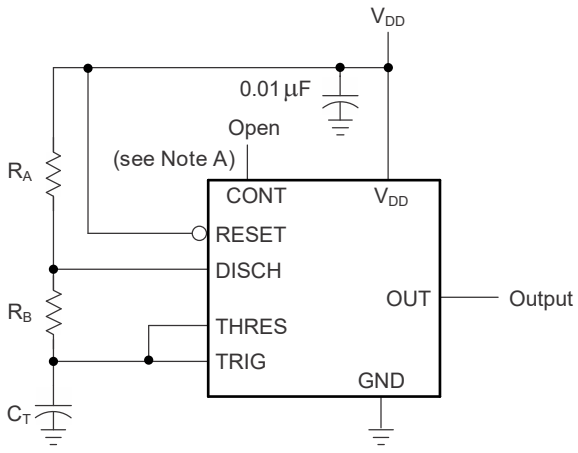
6.3.2 Astable Operation

As shown in Figure 6-2, adding a second resistor, R_B, to the circuit of Figure 6-1 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C_T charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C_T charging and discharging between the threshold-voltage level ($\cong 0.67 \times V_{DD}$) and the trigger-voltage level ($\cong 0.33 \times V_{DD}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



A. Decouple CONT voltage to ground with a capacitor to improve operation. Reevaluate for individual applications.

Figure 6-2. Circuit for Astable Operation

$$t_H \cong 0.693 \times (R_A + R_B) \times C_T \quad (1)$$

$$t_L \cong 0.693 \times R_B \times C_T \quad (2)$$

Other useful relationships for period, frequency, and driver-referred and waveform-referred duty cycle are shown as follows:

$$T = t_H + t_L \cong 0.693 \times (R_A + 2R_B) \times C_T \quad (3)$$

$$f = \frac{1}{T} \cong \frac{1.44}{(R_A + 2R_B) \times C_T} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{T} \cong \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{T} \cong 1 - \frac{R_B}{R_A + 2R_B} = \frac{R_A + R_B}{R_A + 2R_B} \quad (6)$$

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These equations do not account for any propagation delay times from the TRIG and THRES inputs to DISCH output. These delay times add directly to the period and overcharge the capacitor, which creates differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance, r_{on}, during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low. The following equations provide better agreement with measured values. Equation 7 and Equation 8 represent the actual low and high times when used at higher frequencies (beyond 100kHz) because propagation delay and discharge on resistance is added to the formulas. The value of C_T includes both the nominal or deliberate timing capacitance, as well as parasitic capacitance on the PCB. Decoupling capacitance on CONT also affects the duty cycle, with an error contribution that depends on the capacitor leakage resistance. For additional discussion, see the *Design low-duty-cycle timer circuits* article.

$$t_{c(H)} = C_T \times (R_A + R_B) \times \ln\left(3 - e\left(\frac{-t_{PD\ rising}}{C_T \times (R_B + r_{on})}\right)\right) + t_{PD\ falling} \quad (7)$$

$$t_{c(L)} = C_T \times (R_B + r_{on}) \times \ln\left(3 - e\left(\frac{-t_{PD\ falling}}{C_T \times (R_A + R_B)}\right)\right) + t_{PD\ rising} \quad (8)$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln(2) at low frequencies, and ln(3) at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Output waveform duty cycles less than 50% require that $t_{c(H)} / t_{c(L)} < 1$ and possibly that $R_A \leq r_{on}$. These conditions can be difficult to obtain.

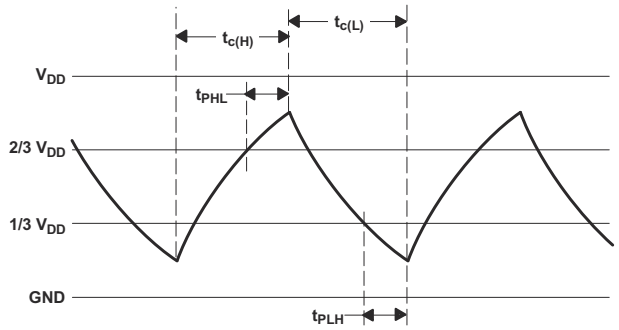

Figure 6-3. Trigger and Threshold Voltage Waveform

6.4 Device Functional Modes

Table 6-1 shows the device truth table. For a valid reset voltage condition, use an external pullup resistor to V_{DD} (if using the RESET functionality), or short the RESET pin directly to V_{DD} (if the RESET functionality is not used).

Table 6-1. Function Table

RESET VOLTAGE(1)	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
< MIN	Irrelevant	Irrelevant	L	On
> MAX	< MIN	Irrelevant(2)	H	Off
> MAX	> MAX	> MAX	L	On
> MAX	> MAX	< MIN	As previously established	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under Section 5.5.
(2) CONT pin open or 2/3 V_{DD}.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLC556 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. *Section 7.2* presents a simplified discussion of the design process. Reset mode forces output and discharge low and provides a small reduction in supply current.

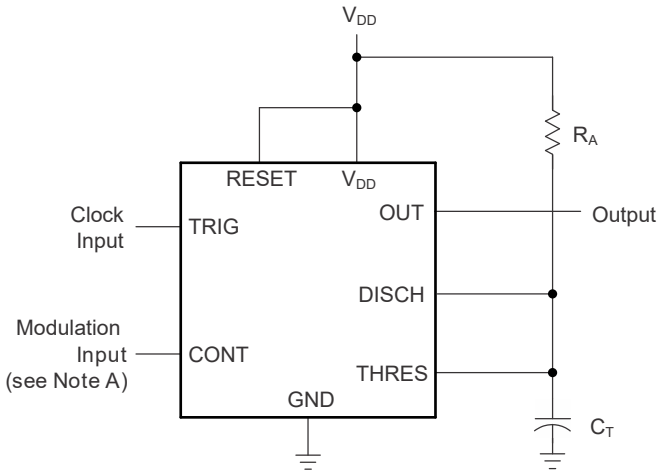
7.1.1 Designing for Improved ESD Performance

The TLC556 internal HBM and CDM protection allows for safe assembly in ESD-controlled environments. In applications that expose the pins of the TLC556 to ESD, additional protection is highly recommended. Use bypass capacitors, current-limiting resistors, and voltage-clamping TVS diodes as necessary to provide additional protection for commonly exposed pins (RESET, TRIG, and OUPUT) against ESD.

7.2 Typical Applications

7.2.1 Pulse-Width Modulation

To modify timer operation, apply an external voltage (or current) to CONT to modulate the internal threshold and trigger voltages. Figure 7-1 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 7-2 shows the resulting duty cycle versus control voltage transfer function. Attempting to run under 10% duty cycle can result in inconsistent output pulses. Attempting to run close to 100% duty cycle results in frequency division by 2, then 3, then 4.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

Figure 7-1. Circuit for Pulse-Width Modulation

7.2.1.1 Design Requirements

The clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 V_{DD}, respectively. Clock input V_{OL} time must be less than minimum output high time; therefore, a high (positive) duty cycle clock is recommended. Minimum recommended modulation voltage is 1V. Lower CONT voltage can greatly increase threshold comparator propagation delay and storage time. The application must be tolerant of a nonlinear

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transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC-based with an negative exponential curve.

7.2.1.2 Detailed Design Procedure

Choose R_A and C_T so that $R_A \times C_T$ is same or less than clock input period. Figure 7-2 shows the non linear relationship between control voltage and output duty cycle. Duty cycle is function of control voltage and clock period relative to RC time constant.

7.2.1.3 Application Curve

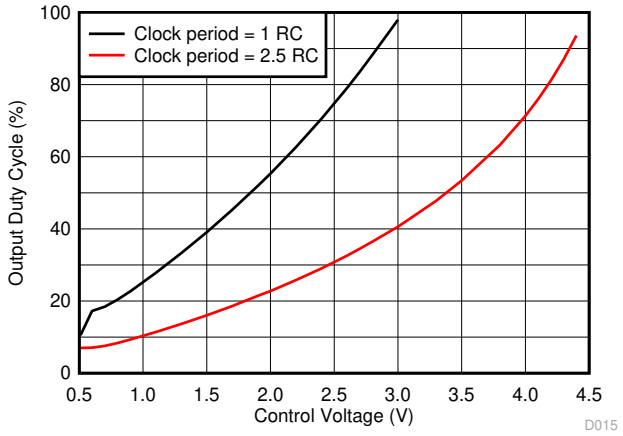
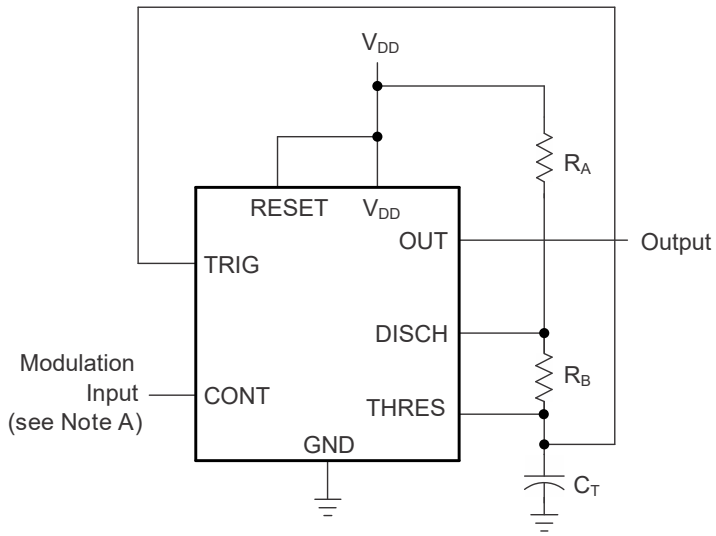


Figure 7-2. Pulse-Width-Modulation vs Control Voltage
Clock Duty Cycle 98%, V_{DD} = 5V

7.2.2 Pulse-Position Modulation

As shown in Figure 7-3, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and thereby the time delay of a free-running oscillator. Figure 7-4 and Figure 7-5 shows the output frequency and duty cycle versus control voltage.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

Figure 7-3. Circuit for Pulse-Position Modulation

7.2.2.1 Design Requirements

Both dc- and ac-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage. Control voltage less than 1V can result in output glitches instead of a steady-output pulse stream. Table 7-1 gives example design requirements.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_A	3kΩ
R_B	309Ω
C_T	1nF

7.2.2.2 Detailed Design Procedure

The nominal output frequency and duty cycle for control voltage set to 2/3 of V_{DD} can be determined using formulas in *Section 6.3.2*.

7.2.2.3 Application Curves

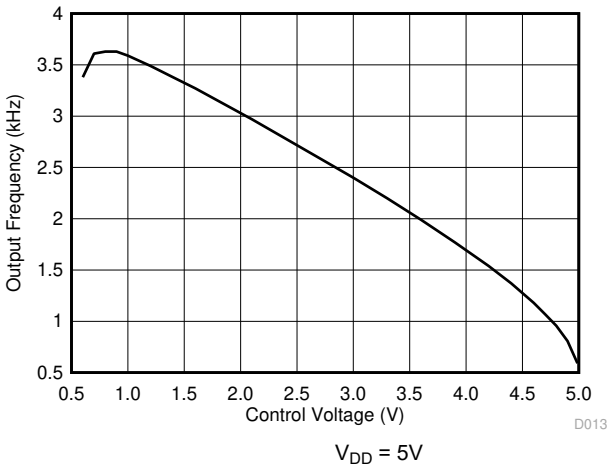


Figure 7-4. Pulse-Position-Modulation Frequency vs Control Voltage

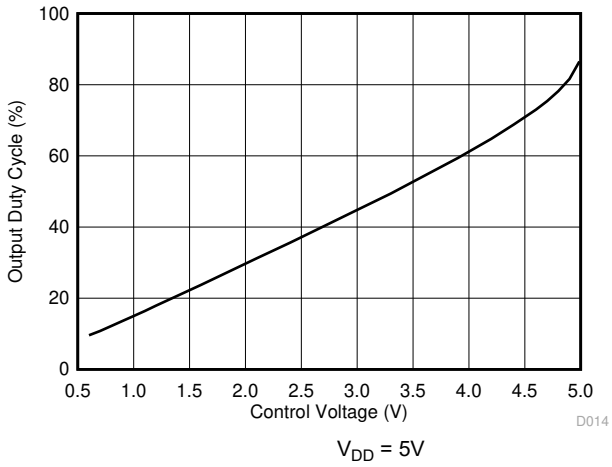


Figure 7-5. Pulse-Position-Modulation Duty Cycle vs Control Voltage

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2024) to Revision D (March 2026)	Page
• Removed LinCMOS™ terminology from data sheet	0
• The specifications for the TLC55M devices are unchanged under revision D	1
• Removed the test condition of V_{RESET} = V_{DD} from reset current ($I_{(reset)}$) in *Electrical Characteristics: V_{DD} = 2V for TLC556C, V_{DD} = 3V for TLC556I*, *Electrical Characteristics: V_{DD} = 5V*, and *Electrical Characteristics: V_{DD} = 15V*	6
• Changed the discharge switch off-stage current typical value at 25°C from 0.1nA to 0.33nA in *Electrical Characteristics: V_{DD} = 2V for TLC556C, V_{DD} = 3V for TLC556I*	6
• Changes the discharge switch off-stage current typical value for TLC556C across temperature from 0.5nA to 11nA in *Electrical Characteristics: V_{DD} = 2V for TLC556C, V_{DD} = 3V for TLC556I*	6
• Changes the discharge switch off-stage current typical value for TLC556I across temperature from 120nA to 30nA in *Electrical Characteristics: V_{DD} = 2V for TLC556C, V_{DD} = 3V for TLC556I*	6
• Removed reset current (I_{RESET}) typical specification with test condition V_{RESET} = 0V in *Electrical Characteristics: V_{DD} = 5V* and *Electrical Characteristics: VDD = 15V*	7
• Changed the typical value of discharge switch off-stage current at 25°C for TLC556C and TLC556I from 0.1nA to 0.3nA in *Electrical Characteristics: V_{DD} = 5V*	7
• Changed the typical value of discharge switch off-stage current for TLC556C at max temperature range from 0.5nA to 11nA in *Electrical Characteristics: V_{DD} = 5V*	7
• Changed the typical value of discharge switch off-stage current for TLC556I at max temperature range from 2nA to 30nA in *Electrical Characteristics: V_{DD} = 5V*	7

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- Changed the typical value of discharge switch on-stage voltage at 25°C for TLC556C and TLC556I from 0.15V to 0.06V in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed the typical value of discarge switch off-stage current at 25°C for TLC556C and TLC556I from 0.1nA to 0.75nA in *Electrical Characteristics: VDD = 15V* 8
- Changed the typical value of discarge switch off-stage current for TLC556C at max temperature range from 0.5nA to 13nA in *Electrical Characteristics: VDD = 15V* 8
- Added a typical value of 30nA to the discarge switch off-stage current for TLC556I at max temperature range in *Electrical Characteristics: VDD = 15V* 8
- Changed the typical value of supply current at 25°C for TLC556C and TLC556I from 0.72mA to 0.47mA in *Electrical Characteristics: VDD = 15V* 8
- Added the *Typical Characteristics* section with updated typical characterstic curves for TLC556C and TLC556I 10

Changes from Revision B (September 1997) to Revision C (December 2024) **Page**

- Added *Applications* section 1
- Added *Package Information* table and *Simplified Schematic* figure to *Description* 1
- Deleted paragraph regarding ESD ratings under MIL-STD-883C, Method 3015 in *Description* 1
- Added *Pin Functions* tables to *Pin Configuration and Functions* 3
- Deleted *TLC556Y Chip Information* section 3
- Deleted continuous total power dissipation specification from *Absolute Maximum Ratings* and restructured table for clarity 4
- Added *ESD Ratings* table and HBM and CDM specifications 4
- Changed *Power Dissipation Ratings* table to *Thermal Information*, and updated per-package thermal specifications 4
- Changed reset current ($I_{(reset)}$) test conditions to V_{RESET} = V_{DD}, in *Electrical Characteristics: V_{DD} = 2V for TLC556C, V_{DD} = 3V for TLC556I*, *Electrical Characteristics: V_{DD} = 5V*, and *Electrical Characteristics: V_{DD} = 15V* 6
- Changed supply current (I_{DD}) typical value from 130µA to 275µA in *Electrical Characteristics: V_{DD} = 2V for TLC556C, V_{DD} = 3V for TLC556I* 6
- Added new reset current ($I_{(reset)}$) typical specification, for test condition V_{RESET} = 0V, to *Electrical Characteristics: V_{DD} = 5V* and *Electrical Characteristics: V_{DD} = 15V* 7
- Changed supply current (I_{DD}) typical value from 340µA to 360µA in *Electrical Characteristics: V_{DD} = 5V* 7
- Changed title of *Operating Characteristics* section to *Switching Characteristics* and clarified that values are specified by design or characterization 9
- Deleted initial error of timing interval specification in *Timing Characteristics* 9
- Updated *Application Information* section and renamed to *Astable Operation* 14
- Updated equations for output driver duty cycle and output waveform duty cycle in *Astable Operation* 14
- Added *Application and Implementation* section with pulse-width modulation and pulse-position modulation applications 16
- Added *Designing for Improved ESD Performance* section to *Application Information* 16

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-89503022A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89503022A TLC556MFKB
5962-8950302CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950302CA TLC556MJB
TLC556CD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC556C
TLC556CD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC556C
TLC556CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC556C
TLC556CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC556C
TLC556CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC556CN
TLC556CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	TLC556CN
TLC556ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC556I
TLC556ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC556I
TLC556IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC556I
TLC556IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC556I
TLC556IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC556IN
TLC556IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	TLC556IN
TLC556MD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC556M
TLC556MD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC556M
TLC556MDG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC556M
TLC556MDG4.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC556M
TLC556MDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC556M
TLC556MDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC556M
TLC556MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89503022A TLC556MFKB
TLC556MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89503022A TLC556MFKB
TLC556MJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC556MJ
TLC556MJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC556MJ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC556MJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950302CA TLC556MJB
TLC556MJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950302CA TLC556MJB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC556, TLC556M :

- Catalog : TLC556

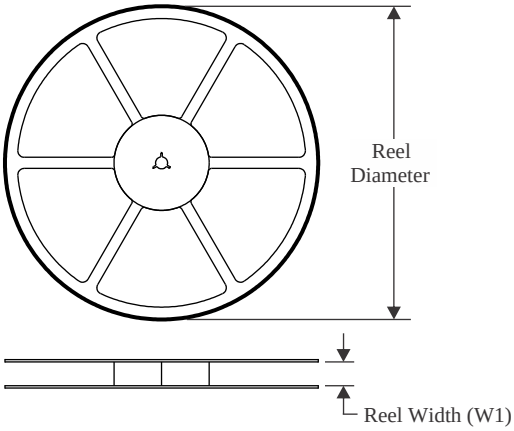
- Military : TLC556M

NOTE: Qualified Version Definitions:

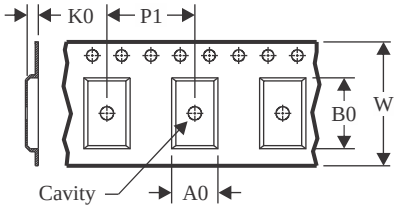
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

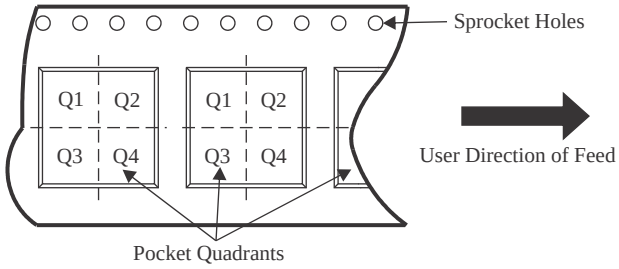


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

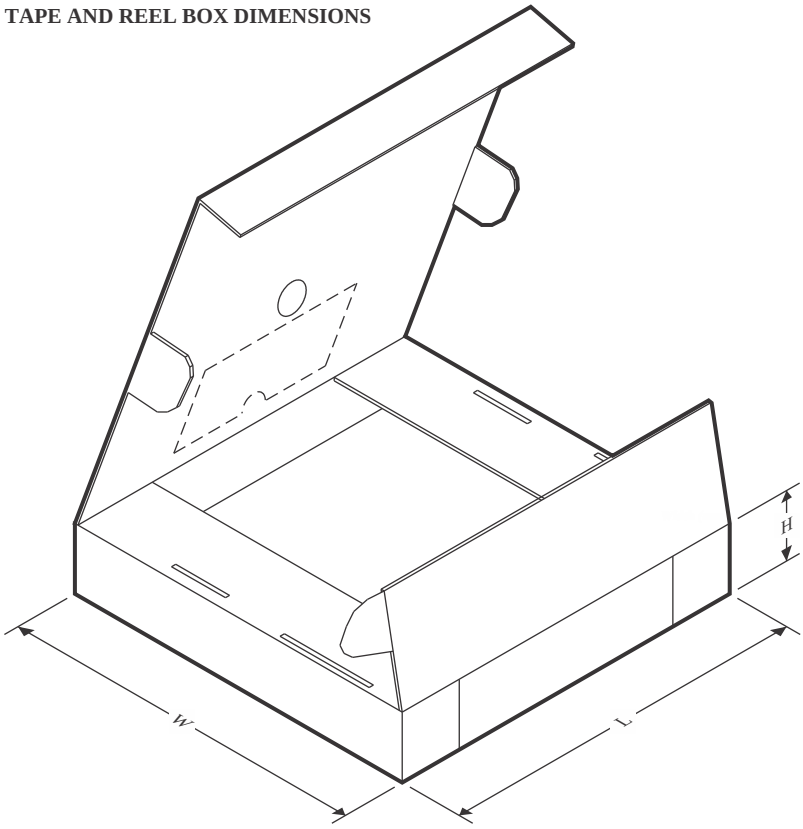
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC556CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC556CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC556CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC556IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

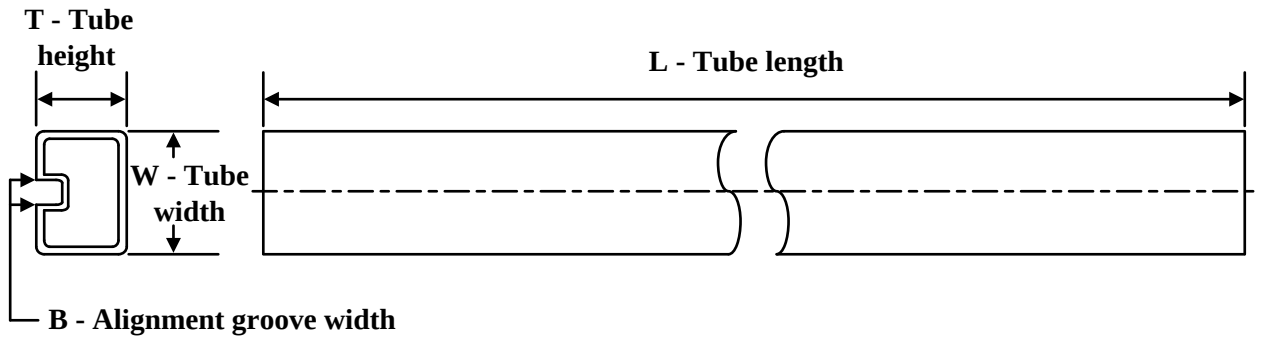
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC556CDR	SOIC	D	14	2500	353.0	353.0	32.0
TLC556CDR	SOIC	D	14	2500	353.0	353.0	32.0
TLC556CDR	SOIC	D	14	2500	353.0	353.0	32.0
TLC556IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE



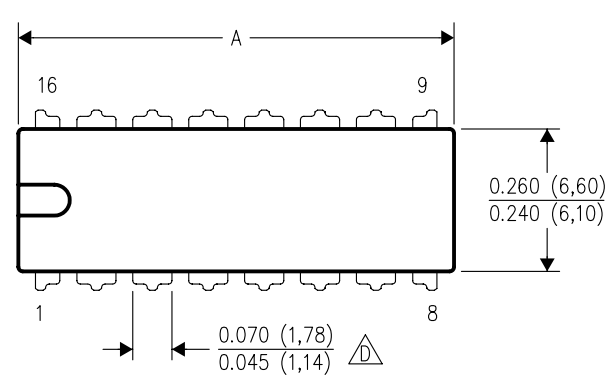
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-89503022A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC556CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC556CD	D	SOIC	14	50	507	8	3940	4.32
TLC556CD.A	D	SOIC	14	50	507	8	3940	4.32
TLC556CD.A	D	SOIC	14	50	505.46	6.76	3810	4
TLC556CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC556CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC556ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC556ID.A	D	SOIC	14	50	505.46	6.76	3810	4
TLC556IN	N	PDIP	14	25	506	13.97	11230	4.32
TLC556IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC556MD	D	SOIC	14	50	505.46	6.76	3810	4
TLC556MD.A	D	SOIC	14	50	505.46	6.76	3810	4
TLC556MDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC556MDG4.A	D	SOIC	14	50	505.46	6.76	3810	4
TLC556MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC556MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA

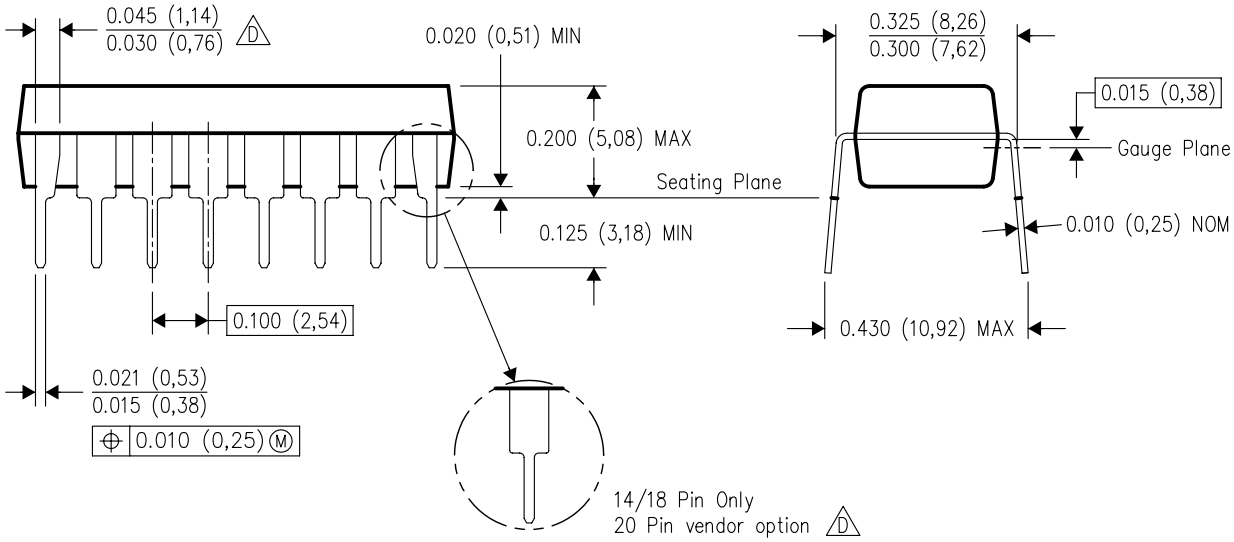
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

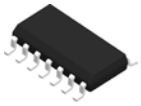


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

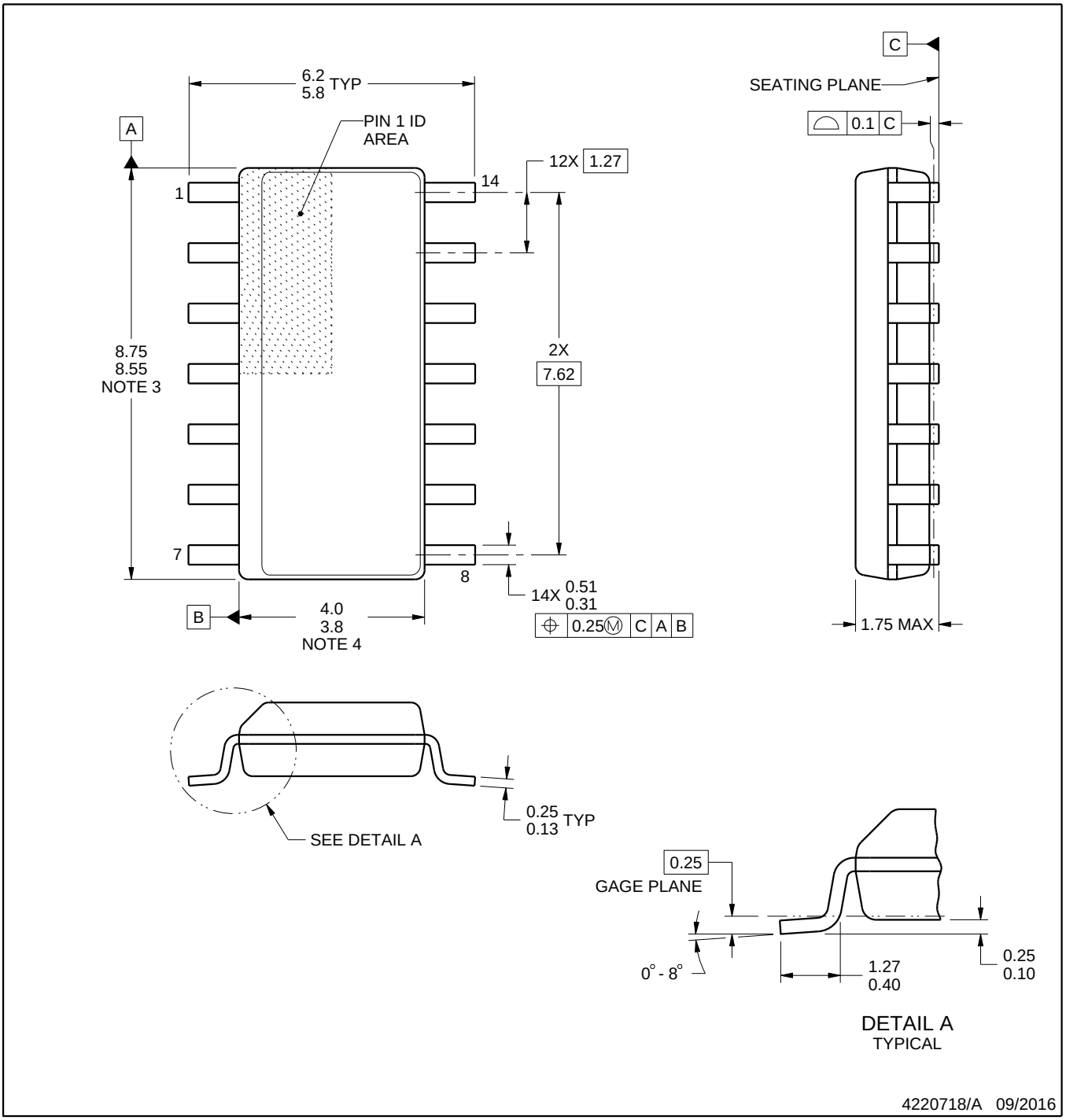


PACKAGE OUTLINE

D0014A

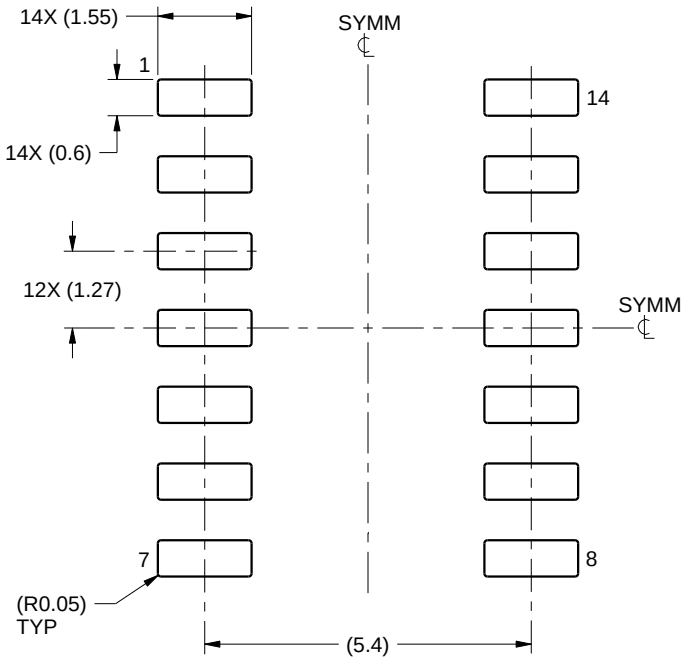
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

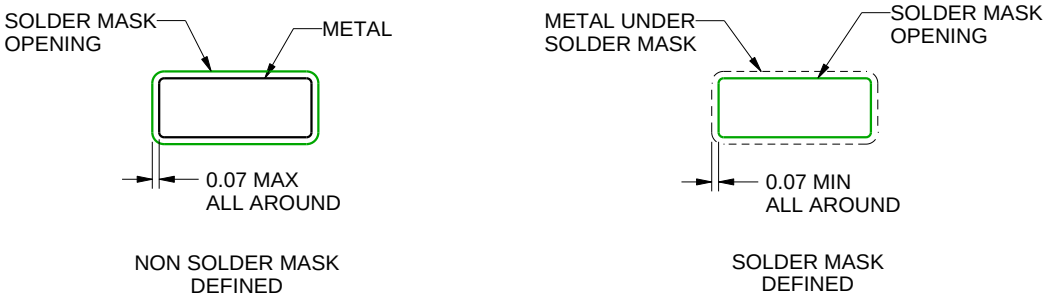


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

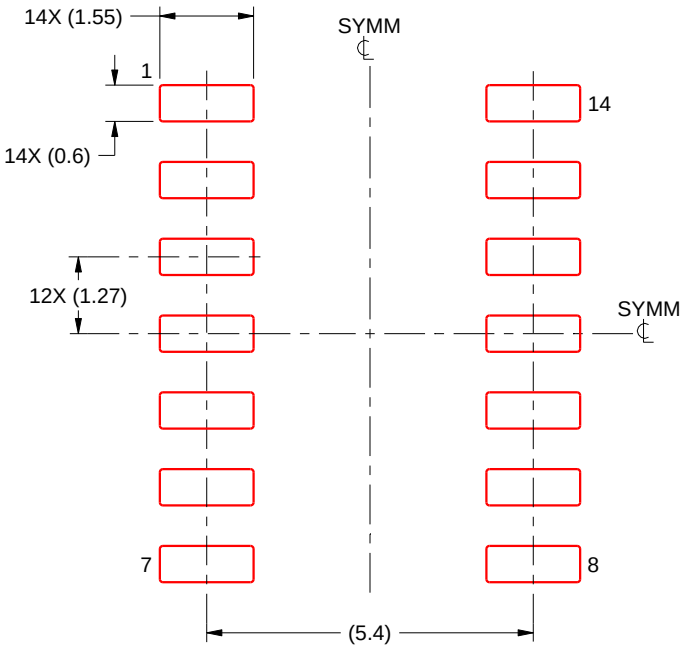
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

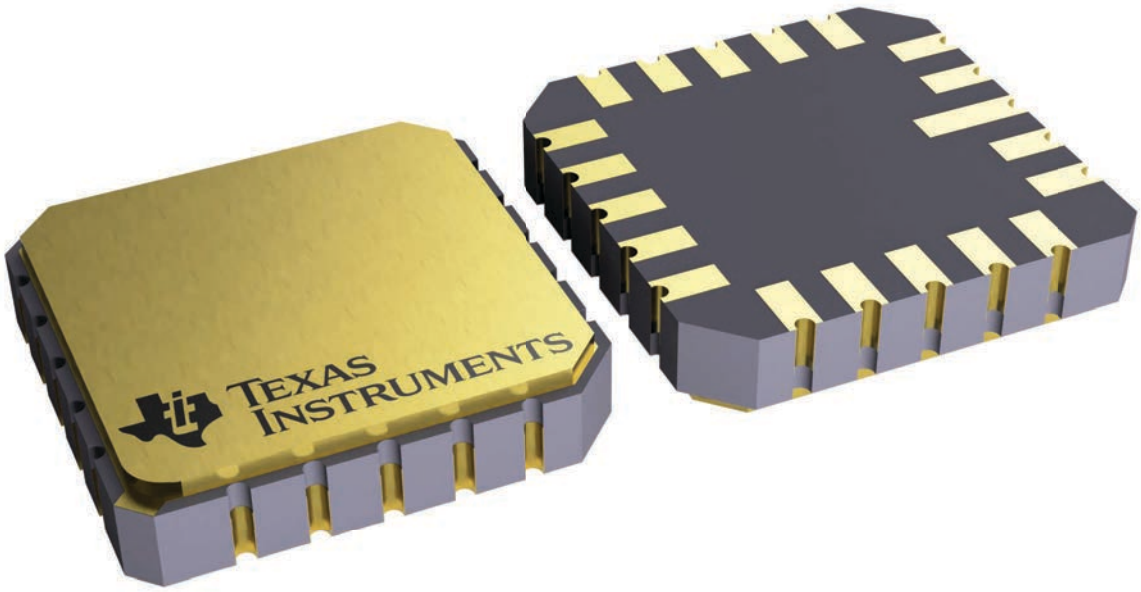
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

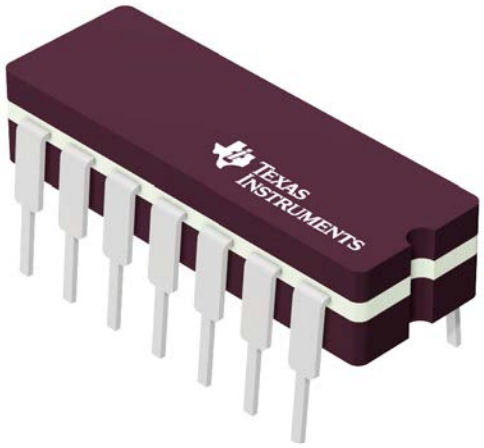


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

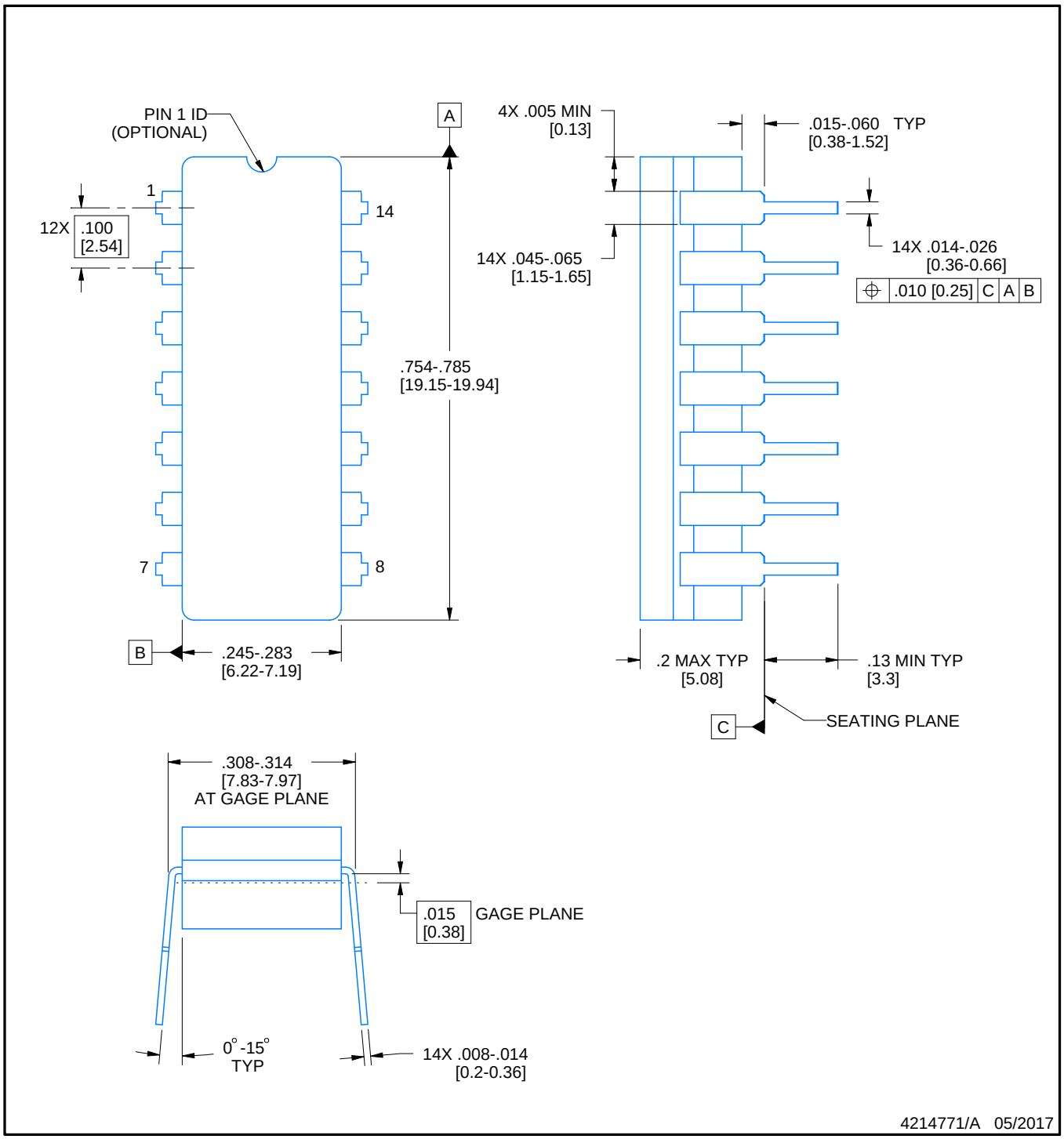
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

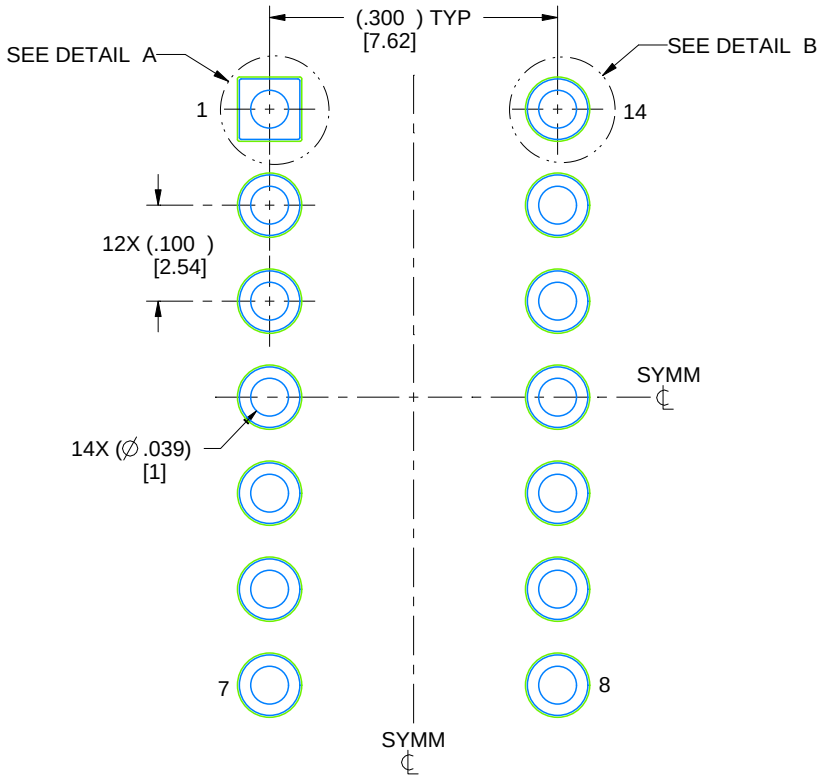
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

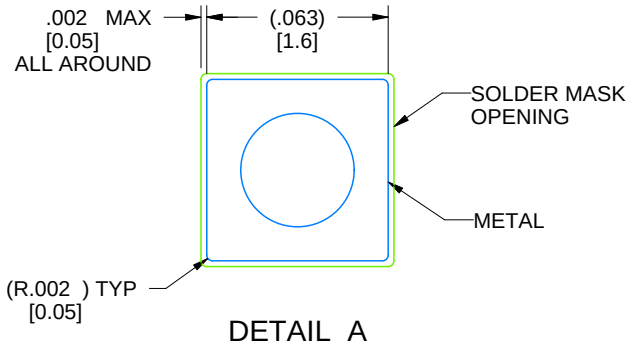
J0014A

CDIP - 5.08 mm max height

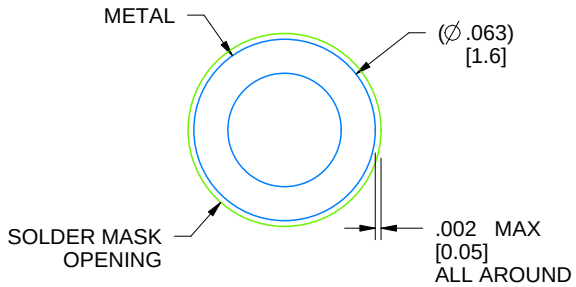
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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