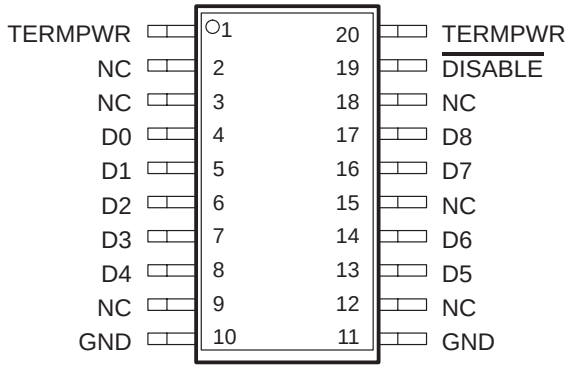
available features

- **Fully Integrated 9-Channel SCSI Termination**
- **No External Components Required**
- **Maximum Allowed Current Applied at First High-Level Step**
- **6-pF Typical Power-Down Output Capacitance**
- **Wide V_{term}† (Termination Voltage) Operating Range, 3.5 V to 5.5 V**
- **TTL-Compatible Disable Feature**
- **Compatible With Active Negation**
- **Thermal Regulation**

PW PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TL2218-285 is a current-mode 9-channel monolithic terminator specially designed for single-ended small-computer-systems-interface (SCSI) bus termination. A user-controlled disable function is provided to reduce standby power. No impedance-matching resistors or other external components are required for its operation as a complete terminator.

The device operates over a wide termination-voltage (V_{term}†) range of 3.5 V to 5.5 V, offering an extra 0.5 V of operating range when compared to the minimum termination voltage of 4 V required by other integrated active terminators. The TL2218-285 functions as a current-sourcing terminator and supplies a constant output current of 23 mA into each asserted line. When a line is deasserted, the device senses the rising voltage level and begins to function as a voltage source, supplying a fixed output voltage of 2.85 V. The TL2218-285 features compatibility with active negation drivers and has a typical sink current capability of 20 mA.

The TL2218-285 is able to ensure that maximum current is applied at the first high-level step. This performance means that the device should provide a first high-level step exceeding 2 V even at a 10-MHz rate. Therefore, noise margins are improved considerably above those provided by resistive terminators.

A key difference between the TL2218-285 current-mode terminator and a Boulay terminator is that the TL2218-285 does not incorporate a low dropout regulator to set the output voltage to 2.85 V. In contrast with the Boulay termination concept, the accuracy of the 2.85 V is not critical with the current-mode method used in the TL2218-285 because this voltage does not determine the driver current. Therefore, the primary device specifications are not the same as with a voltage regulator but are more concerned with output current.

The $\overline{\text{DISABLE}}$ terminal is TTL compatible and must be taken low to shut down the outputs. The device is normally active, even when $\overline{\text{DISABLE}}$ is left floating. In the disable mode, only the device startup circuits remain active, thereby reducing the supply current to just 500 μA. Output capacitance in the shutdown mode is typically 6 pF.

The TL2218-285 has on-board thermal regulation and current limiting, thus eliminating the need for external protection circuitry. A thermal regulation circuit that is designed to provide current limiting, rather than an actual thermal shutdown, is included in the individual channels of the TL2218-285. When a system fault occurs that leads to excessive power dissipation by the terminator, the thermal regulation circuit causes a reduction in the asserted-line output current sufficient to maintain operation. This feature allows the bus to remain active during a fault condition, which permits data transfer immediately upon removal of the fault. A terminator with thermal shutdown does not allow for data transfer until sufficient cooling has occurred. Another advantage offered by the TL2218-285 is a design that does not require costly laser trimming in the manufacturing process.

The TL2218-285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

† This symbol is not presently listed within EIA/JEDEC standards for letter symbols.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1995, Texas Instruments Incorporated

AVAILABLE OPTIONS

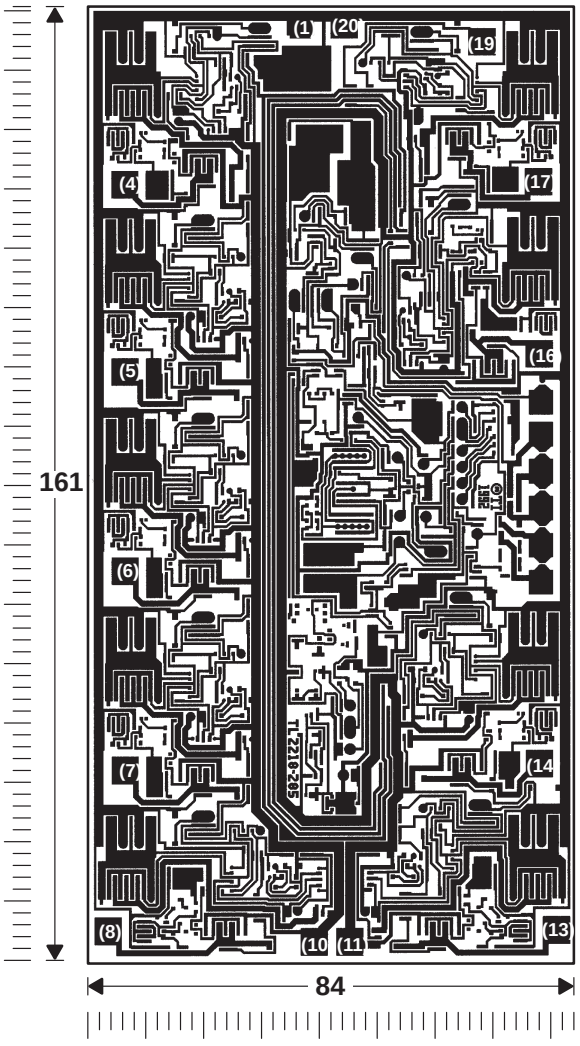
T_J	SURFACE MOUNT (PW)†	CHIP FORM (Y)
0°C to 125°C	TL2218-285PWLE	TL2218-285Y

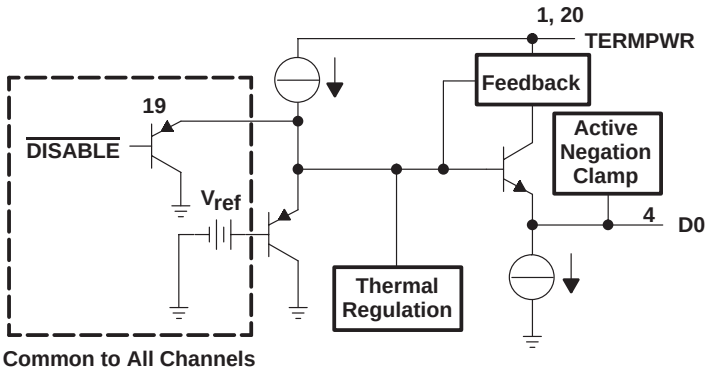
† The PW package is only available left-end taped and reeled.

TL2218-285Y chip information

This chip, when properly assembled, displays characteristics similar to the TL2218-285. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

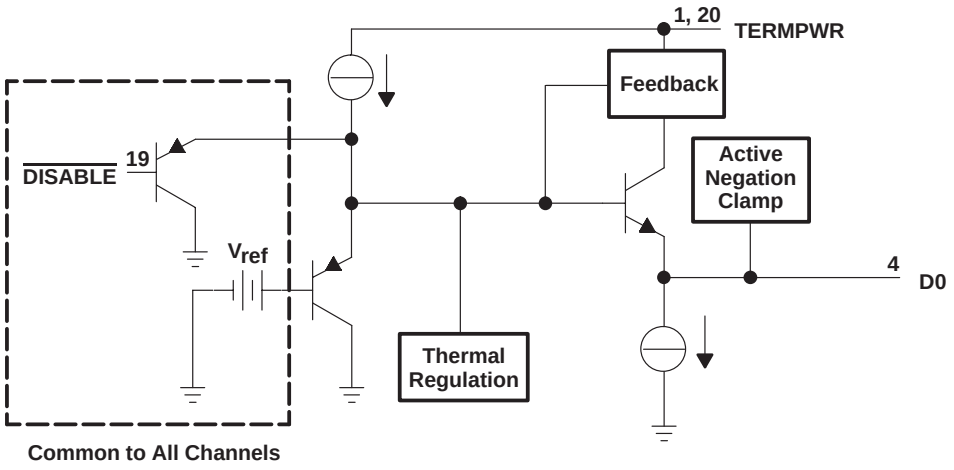
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS
77251−1443

functional block diagram (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Figures 1, 2, and 3)†

Continuous termination voltage . . . . . 10 V
Continuous output voltage range . . . . . 0 V to 5.5 V
Continuous disable voltage range . . . . . 0 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . −55°C to 150°C
Storage temperature range, T_{stg} . . . . . −60°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
PW	T_A	828 mW	6.62 mW/°C	530 mW	430 mW	166 mW
	T_C	4032 mW	32.2 mW/°C	2583 mW	2100 mW	812 mW
	T_L‡	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

‡ $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

**FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE**

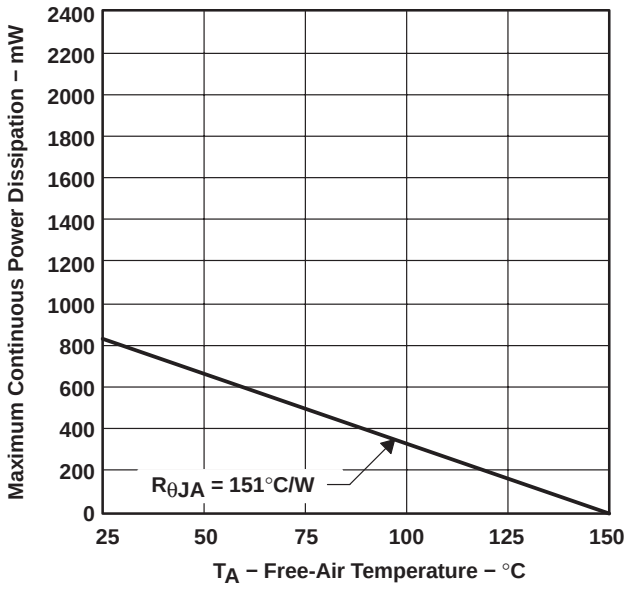


Figure 1

**CASE TEMPERATURE
DISSIPATION DERATING CURVE**

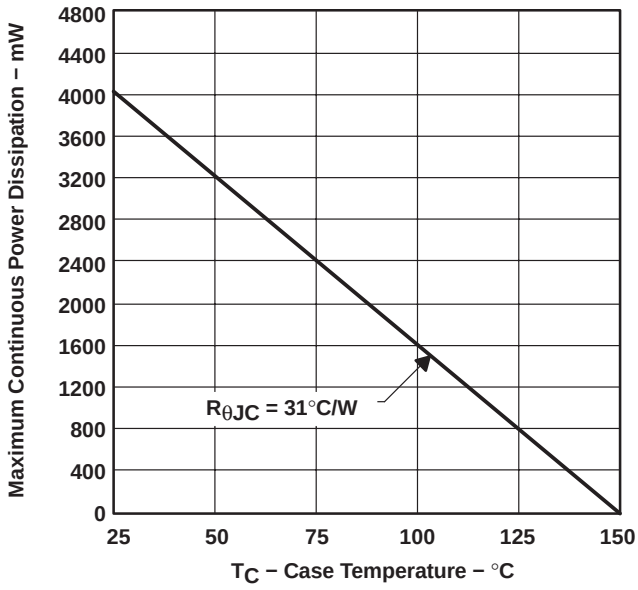


Figure 2

**LEAD TEMPERATURE
DISSIPATION DERATING CURVE**

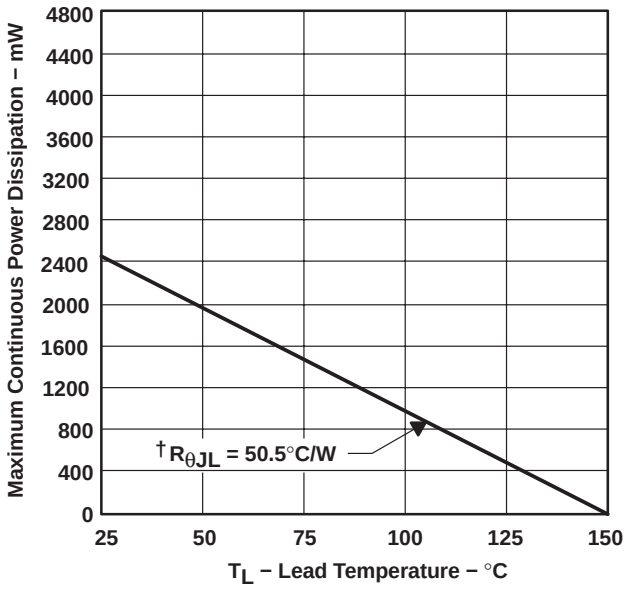


Figure 3

† $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device, and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS
77251−1443

recommended operating conditions

	MIN	MAX	UNIT
Termination voltage	3.5	5.5	V
High-level disable input voltage, V_{IH}	2	V_{term}	V
Low-level disable input voltage, V_{IL}	0	0.8	V
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics, V_{term} = 4.75 V, V_O = 0.5 V, T_J = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage		2.5	2.85		V
TERMPWR supply current	All data lines open		9		mA
	All data lines = 0.5 V		228		
	$\overline{\text{DISABLE}}$ = 0 V		500		µA
Output current		−20.5	−23	−24	mA
Disable input current (see Note 1)	$\overline{\text{DISABLE}}$ = 4.75 V			1	µA
	$\overline{\text{DISABLE}}$ = 0 V			600	
Output leakage current	$\overline{\text{DISABLE}}$ = 0 V		100		nA
Output capacitance, device disabled	V_O = 0 V, 1 MHz		6		pF
Termination sink current, total	V_O = 4 V		20		mA

NOTE 1: When $\overline{\text{DISABLE}}$ is open or high, the terminator is active.

THERMAL INFORMATION

The need for smaller surface-mount packages for use on compact printed-wiring boards (PWB) causes an increasingly difficult problem in the area of thermal dissipation. In order to provide the systems designer with a better approximation of the junction temperature rise in the thin-shrink small-outline package (TSSOP), the junction-to-lead thermal resistance ($R_{\theta JL}$) is provided along with the more typical values of junction-to-ambient and junction-to-case thermal resistances, $R_{\theta JA}$ and $R_{\theta JC}$.

$R_{\theta JL}$ is used to calculate the device junction temperature rise measured from the leads of the unit. Consequently, the junction temperature is dependent upon the board temperature at the leads, $R_{\theta JL}$, and the internal power dissipation of the device. The board temperature is contingent upon several variables, including device packing density, thickness, material, area, and number of interconnects. The $R_{\theta JL}$ value depends on the number of leads connecting to the die-mount pad, the lead-frame alloy, area of the die, mount material, and mold compound. Since the power level at which the TSSOP can be used is highly dependent upon both the temperature rise of the PWB and the device itself, the systems designer can maximize this level by optimizing the circuit board. The junction temperature of the device can be calculated using the equation $T_J = (P_D \times R_{\theta JL}) + T_L$ where T_J = junction temperature, P_D = power dissipation, $R_{\theta JL}$ = junction-to-lead thermal resistance, and T_L = board temperature at the leads of the unit.

The values of thermal resistance for the TL2218-285 PW are as follows:

Thermal Resistance	Typical Junction Rise
$R_{\theta JA}$	151°C/W
$R_{\theta JC}$	31 °C/W
$R_{\theta JL}$	50.5°C/W

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_O	Output current	vs Input voltage	4
V_O	Output voltage	vs Input voltage	5
I_O	Output current	vs Junction temperature	6
V_O	Output voltage	vs Junction temperature	7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs INPUT VOLTAGE

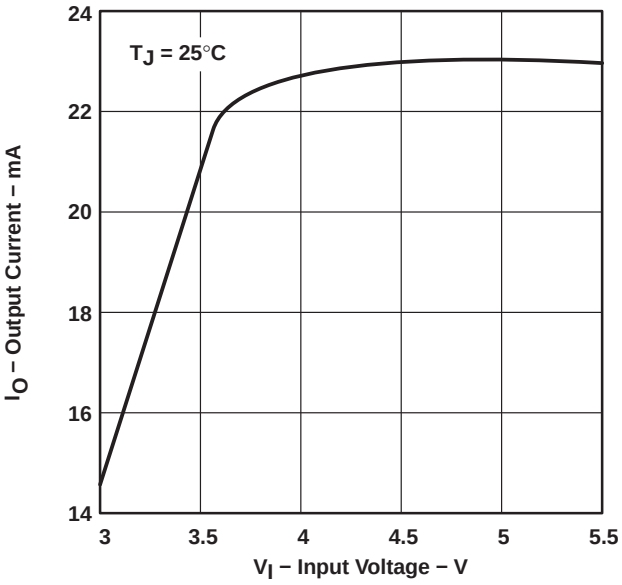


Figure 4

OUTPUT VOLTAGE vs INPUT VOLTAGE

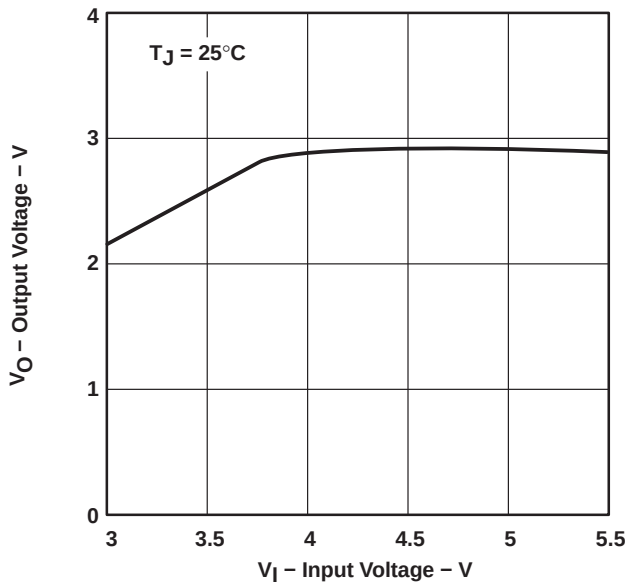


Figure 5

OUTPUT CURRENT vs JUNCTION TEMPERATURE

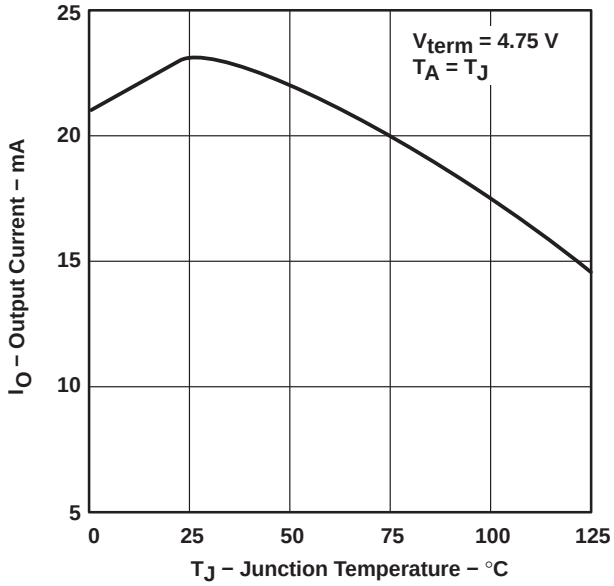


Figure 6

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

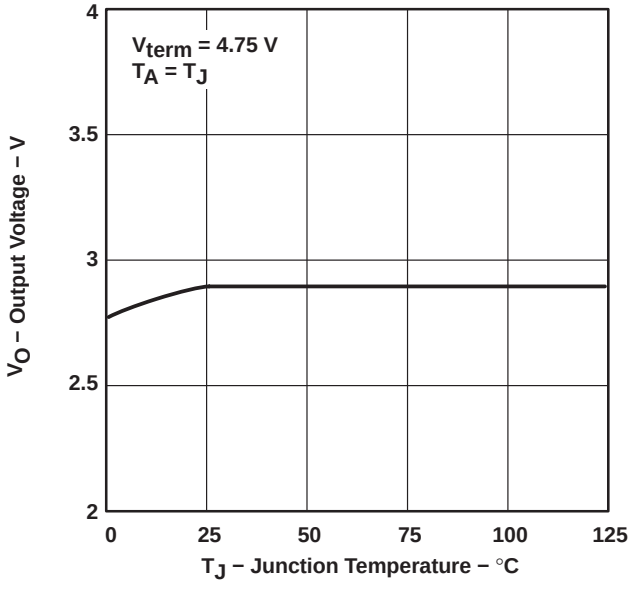


Figure 7

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL2218-285PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	0 to 125	2218285
TL2218-285PWR	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	0 to 125	2218285

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025