TL08xx FET-Input Operational Amplifiers

1 Features

- High slew rate: 20V/µs (TL08xH, typ)
- Low offset voltage: 1mV (TL08xH, typ)
- Low offset voltage drift: 2µV/°C
- Low power consumption: 940µA/ch (TL08xH, typ)
- Wide common-mode and differential voltage ranges
  - Common-mode input voltage range includes V_{CC+}
- Low input bias and offset currents
- Low noise: V_n = 37nV/√Hz (typ) at f = 1kHz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage: ±2.25V to ±20V, 4.5V to 40V

2 Applications

- Solar energy: string and central inverter
- Motor drives: AC and servo drive control and power stage modules
- Single phase online UPS
- Three phase UPS
- Pro audio mixers
- Battery test equipment

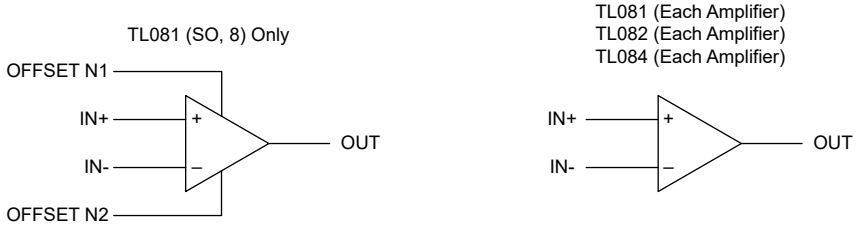
3 Description

The TL08xH (TL081H, TL082H, and TL084H) family of devices are the next-generation versions of the industry-standard TL08x (TL081, TL082, and TL084) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1mV, typical), high slew rate (20V/µs), and common-mode input to the positive supply. High ESD (1.5kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL08xH devices to be used in the most rugged and demanding applications.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
TL081x	Single	P (PDIP, 8)
		DCK (SC70, 5)
		PS (SO, 8)
		D (SOIC, 8)
		DBV (SOT-23, 5)
TL082x	Dual	P (PDIP, 8)
		PS (SO, 8)
		D (SOIC, 8)
		DDF (SOT-23, 8)
		PW (TSSOP, 8)
TL082M	Dual	JG (CDIP, 8)
		FK (LCCC, 20)
TL084x	Quad	N (PDIP, 14)
		D (SOIC, 14)
		DYY (SOT-23, 14)
		PW (TSSOP, 14)
TL084M	Quad	J (CDIP, 14)
		FK (LCCC, 20)

(1) For more information, see Section 11.



Logic Symbols

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

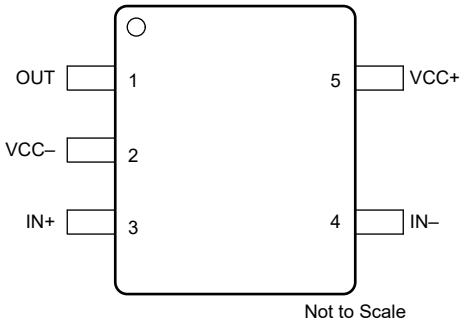


Figure 4-1. TL081H: DBV Package, 5-Pin SOT-23 (Top View)

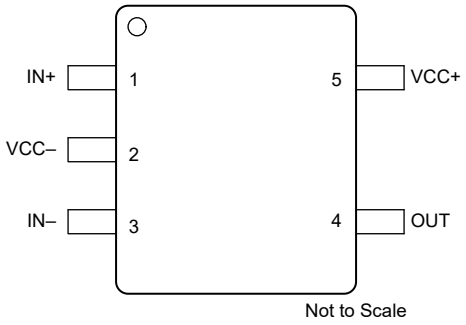


Figure 4-2. TL081H: DCK Package, 5-Pin SC70 (Top View)

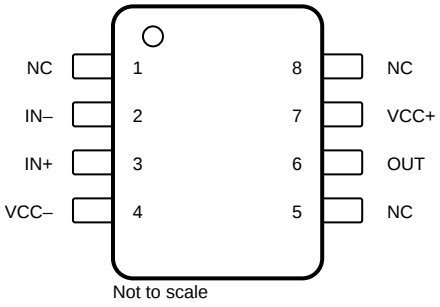


Figure 4-3. TL081x: D Package, 8-Pin SOIC, P Package, 8-Pin PDIP (Top View)

Table 4-1. Pin Functions: TL081x

PIN					TYPE[1]	DESCRIPTION
NAME	NO.					
	D	DBV	DCK	P		
NC	1	—	—	1	—	Do not connect
IN–	2	4	3	2	I	Inverting input
IN+	3	3	1	3	I	Non inverting input
VCC–	4	2	2	4	—	Power supply
NC	5	—	—	5	—	Do not connect
OUT	6	1	4	6	O	Output
VCC+	7	5	5	7	—	Power supply
NC	8	—	—	8	—	Do not connect

(1) I = input, O = output.

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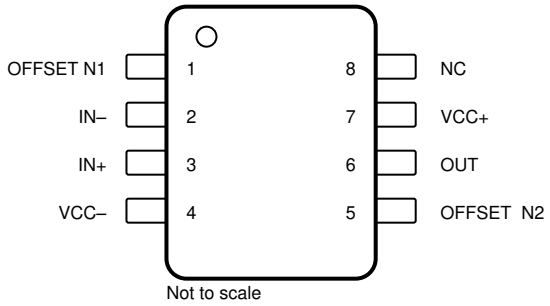


Figure 4-4. TL081C PS Package, 8-Pin SO (Top View)

Table 4-2. Pin Functions: TL081C

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OFFSET N1	1	—	Input offset adjustment
IN–	2	I	Inverting input
IN+	3	I	Non inverting input
VCC–	4	—	Power supply
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC+	7	—	Power supply
NC	8	—	Do not connect

(1) I = input, O = output.

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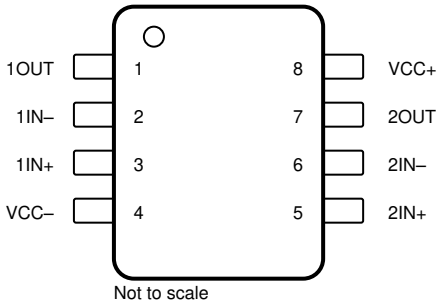


Figure 4-5. TL082x D, DDF, DGK, JG, P, PS, and PW Packages, 8-Pin SOIC, SOT-23 (8), VSSOP, CDIP, PDIP, SO, and TSSOP (Top View)

Table 4-3. Pin Functions: TL082x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1OUT	1	O	Output
1IN–	2	I	Inverting input
1IN+	3	I	Non inverting input
VCC–	4	—	Power supply
2IN+	5	I	Non inverting input
2IN–	6	I	Inverting input
2OUT	7	O	Output
VCC+	8	—	Power supply

(1) I = input, O = output.

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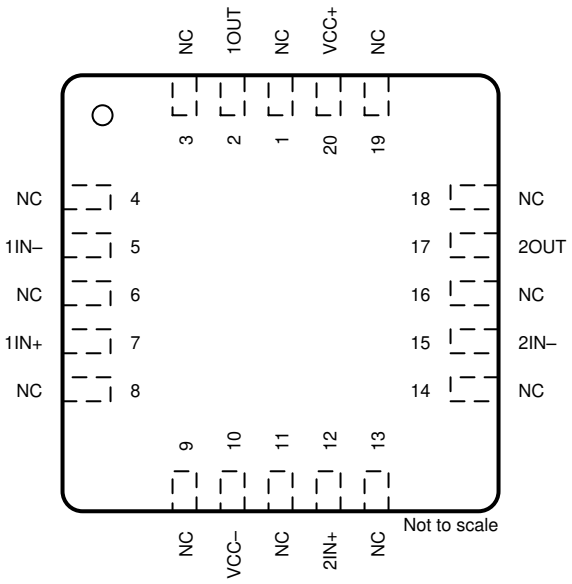


Figure 4-6. TL082 FK Package, 20-Pin LCCC (Top View)

Table 4-4. Pin Functions: TL082x

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1IN–	5	I	Inverting input
1IN+	7	I	Non inverting input
1OUT	2	O	Output
2IN–	15	I	Inverting input
2IN+	12	I	Non inverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC–	10	—	Power supply
VCC+	20	—	Power supply

(1) I = input, O = output.

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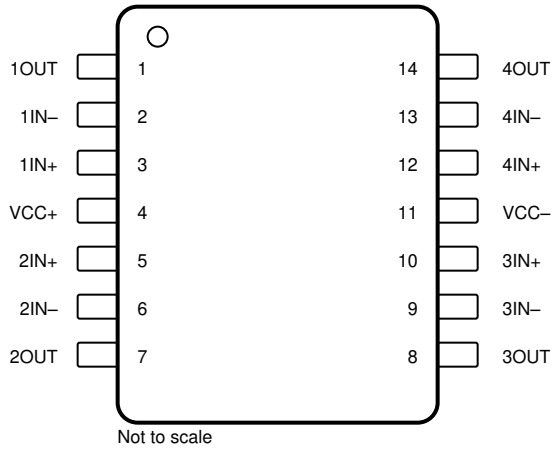


Figure 4-7. TL084x D, N, NS, PW, J, and DYY Package, 14-Pin SOIC, PDIP, SO, TSSOP, CDIP, and SOT-23 (14) (Top View)

Table 4-5. Pin Functions: TL084x

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Non inverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Non inverting input
2OUT	7	O	Output
3IN–	9	I	Inverting input
3IN+	10	I	Non inverting input
3OUT	8	O	Output
4IN–	13	I	Inverting input
4IN+	12	I	Non inverting input
4OUT	14	O	Output
V_{CC-}	11	—	Power supply
V_{CC+}	4	—	Power supply

(1) I = input, O = output.

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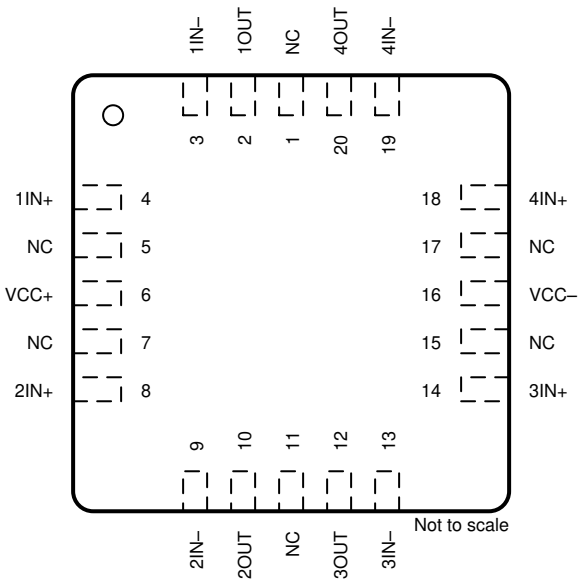


Figure 4-8. TL084 FK Package, 20-Pin LCCC (Top View)

Table 4-6. Pin Functions: TL084x

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Non inverting input
1OUT	2	O	Output
2IN–	9	I	Inverting input
2IN+	8	I	Non inverting input
2OUT	10	O	Output
3IN–	13	I	Inverting input
3IN+	14	I	Non inverting input
3OUT	12	O	Output
4IN–	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC–	16	—	Power supply
VCC+	6	—	Power supply

(1) I = input, O = output.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		All NS and PS packages; All TL08xM devices	–0.3	36	V
		All other devices	0	42	V
Signal input pins	Common-mode voltage (3)	All NS and PS packages; All TL08xM devices	(V–) – 0.3	(V–) + 36	V
		All other devices	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (3)	All NS and PS packages; All TL08xM devices (4)	(V–) – 0.3	(V–) + 36	V
		All other devices		V_S + 0.2	V
	Current (3)	All NS and PS packages; All TL07xM devices		50	mA
		All other devices	–10	10	mA
Output short-circuit (2)			Continuous		
Operating ambient temperature, T_A			–55	150	°C
Junction temperature, T_J				150	°C
Case temperature for 60 seconds - FK package				260	°C
Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds				300	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(4) Differential voltage only limited by input voltage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, (V_{CC}+) – (V_{CC}–)	All NS and PS packages; All TL08xM devices(1)	10	30	V
		All other devices	4.5	40	V
V_I	Input voltage range	All NS and PS packages; All TL08xM devices	(V_{CC}–) + 2	(V_{CC}+) + 0.1	V
		All other devices	(V_{CC}–) + 4	(V_{CC}+) + 0.1	V
T_A	Specified temperature	TL08xM	–55	125	°C
		TL08xH	–40	125	°C
		TL08xI	–40	85	°C
		TL08xC	0	70	°C

(1) V+ and V– are not required to be of equal magnitude, provided that the total V_S (V+ – V–) is between 10 V and 30 V.

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5.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TL081xx					UNIT
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	P (PDIP)	PS (SO)	
		8 PINS	5 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.8	217.5	212.2	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.6	113.1	111.1	–	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.3	63.8	79.4	–	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.8	34.8	51.8	–	–	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.5	63.5	79.0	–	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metric* application report.

5.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TL082xx								UNIT
		D (SOIC)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SO)	PW (TSSOP)	U (CFP)	
		8 PINS	8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.8	181.5	–	–	85	95	200.3	169.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.2	112.5	5.61	15.05	–	–	89.4	62.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.4	98.2	–	–	–	–	131.0	176.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	36.8	17.2	–	–	–	–	22.2	48.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.6	97.6	–	–	–	–	129.3	144.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	N/A	5.4	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metric* application report.

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5.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		TL084xx								UNIT
		D (SOIC)	DYY (SOT-23)	FK (TSSOP)	J (TSSOP)	N (TSSOP)	NS (TSSOP)	PW (TSSOP)	W (TSSOP)	
		14 PINS	14 PINS	20 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	153.2	–	–	80	76	–	128.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	88.7	5.61	14.5	–	–	14.5	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.2	65.4	–	–	–	–	–	127.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.8	9.5	–	–	–	–	–	29	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.8	65.0	–	–	–	–	–	106.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	–	0.5	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metric* application report.

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5.7 Electrical Characteristics: TL08xH

For $V_S = (V_{CC+}) – (V_{CC–}) = 4.5$ V to 40 V (±2.25 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{out} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±4	mV
			T_A = –40°C to +125°C			±5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +125°C		±2		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 5V to 40V, $V_{CM} = V_S/2$	T_A = –40°C to +125°C		±1	±10	µV/V
	Channel separation	f = 0 Hz			10		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±120	pA
			DCK and DBV packages		±1	±300	pA
			T_A = –40°C to +125°C (1)			±5	nA
I_{OS}	Input offset current				±0.5	±120	pA
			DCK and DBV packages		±0.5	±250	pA
			T_A = –40°C to +125°C (1)			±5	nA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			37		nV/√Hz
		f = 10 kHz			21		
i_N	Input current noise	f = 1 kHz			80		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			$(V_{CC–}) + 1.5$		(V_{CC+})	V
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < $(V_{CC+}) – 1.5$ V		100	105		dB
			T_A = –40°C to +125°C	95			dB
		V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < (V_{CC+})		90	105		dB
			T_A = –40°C to +125°C	80			dB
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 2		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, $(V_{CC–}) + 0.3$ V < V_O < $(V_{CC+}) – 0.3$ V	T_A = –40°C to +125°C	118	125		dB
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, R_L = 2 kΩ, $(V_{CC–}) + 1.2$ V < V_O < $(V_{CC+}) – 1.2$ V	T_A = –40°C to +125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			20		V/µs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, C_L = 20 pF			0.63		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, C_L = 20 pF			0.56		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, C_L = 20 pF			0.91		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, C_L = 20 pF			0.48		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20 pF			56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz			0.00012		%
EMIRR	EMI rejection ratio	f = 1 GHz			53		dB

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5.7 Electrical Characteristics: TL08xH (continued)

For $V_S = (V_{CC+}) – (V_{CC–}) = 4.5$ V to 40 V (±2.25 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{out} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	$V_S = 40$ V, $R_L = 10$ kΩ		115	210	mV
			$V_S = 40$ V, $R_L = 2$ kΩ		520	965	
		Negative rail headroom	$V_S = 40$ V, $R_L = 10$ kΩ		105	215	
			$V_S = 40$ V, $R_L = 2$ kΩ		500	1030	
I_{SC}	Short-circuit current				±26		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1 MHz, $I_O = 0$ A			125		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$I_O = 0$ A			937.5	1125	µA
		$I_O = 0$ A, (TL081H)			960	1156	
		$I_O = 0$ A	$T_A = –40°C$ to $+125°C$			1130	
		$I_O = 0$ A, (TL082H)				1143	
		$I_O = 0$ A, (TL071H)				1160	
	Turn-On time	At $T_A = 25°C$, $V_S = 40V$, V_S ramp rate > 0.3V/µs			60		µs

(1) Max I_B and I_{os} data is specified based on characterization results.

5.8 Electrical Characteristics (DC): TL08xC, TL08xAC, TL08xBC, TL08xI, TL08xM

For $V_S = (V_{CC+}) – (V_{CC–}) = ±15$ V at $T_A = 25°C$, unless otherwise noted

PARAMETER		TEST CONDITIONS[1] [2]			MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	$V_O = 0$ V $R_S = 50$ Ω	TL08xC			3	10	mV
				T_A = Full range			13	
			TL08xAC			3	6	
				T_A = Full range			7.5	
			TL08xBC			2	3	
				T_A = Full range			5	
			TL08xI			3	6	
				T_A = Full range			8	
			TL081M, TL082M			3	6	
				T_A = Full range			9	
			TL084M			3	9	
				T_A = Full range			15	
dV_{OS}/dT	Input offset voltage drift	$V_O = 0$ V, $R_S = 50$ Ω	T_A = Full range			±18		µV/°C
I_{OS}	Input offset current	$V_O = 0$ V	TL08xC			5	100	pA
				T_A = Full range			10	nA
			TL08xAC, TL08xBC, TL08xI			5	100	pA
				T_A = Full range			2	nA
			TL08xM			5	100	pA
				T_A = Full range			20	nA
I_B	Input bias current	$V_O = 0$ V	TL08xC, TL08xAC, TL08xBC, TL08xI			65	200	pA
				T_A = Full range			7	nA
			TL081M, TL082M			65	200	pA
				T_A = Full range			50	nA
			TL084M			65	200	pA
				T_A = Full range			20	nA
V_{CM}	Common-mode voltage range				±11	–12 to 15		V
VOM	Maximum peak output voltage swing	$R_L = 10$ kΩ			±12	±13.5		V
		$R_L ≥ 10$ kΩ	T_A = Full range		±12			
		$R_L ≥ 2$ kΩ			±10			
A_{OL}	Open-loop voltage gain	$V_O = 0$ V	TL08xC		25	200		V/mV
				T_A = Full range	15			
			TL08xAC, TL08xBC, TL08xI		50	200		
				T_A = Full range	25			
			TL08xM		35	200		
				T_A = Full range	15			
GBW	Gain-bandwidth product	All NS and PS packages; All TL08xM devices				3		MHz
		All other devices				5.25		
R_{ID}	Common-mode input resistance					1		TΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$ $V_O = 0$ V $R_S = 50$ Ω	TL08xC		70	100		dB
			TL08xAC, TL08xBC, TL08xI		75	100		
			TL08xM		80	86		
PSRR	Input offset voltage versus power supply	$V_S = ±9$ V to ± 18 V $V_O = 0$ V $R_S = 50$ Ω	TL08xC		70	100		dB
			TL08xAC, TL08xBC, TL08xI		80	100		
			TL08xM		80	86		

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5.8 Electrical Characteristics (DC): TL08xC, TL08xAC, TL08xBC, TL08xI, TL08xM (continued)

For $V_S = (V_{CC+}) – (V_{CC–}) = ±15$ V at $T_A = 25°C$, unless otherwise noted

PARAMETER		TEST CONDITIONS(1) (2)	MIN	TYP	MAX	UNIT
I_Q	Quiescent current per amplifier	$V_O = 0$ V; no load		1.4	2.5	mA
	Channel separation	f = 0 Hz		1		µV/V

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is $T_A = 0°C$ to 70°C for the TL07xC, TL07xAC, and TL07xBC; $T_A = –40°C$ to 85°C for the TL07xI; and $T_A = –55°C$ to 125°C for the TL07xM.

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5.9 Electrical Characteristics (AC): TL08xC, TL08xAC, TL08xBC, TL08xI, TL08xM

For $V_S = (V_{CC+}) – (V_{CC–}) = ±15$ V at $T_A = 25°C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate	V_I = 10 V, C_L = 100 pF, R_L = 2 kΩ	TL08xM	5	20		V/µs
			TL08xC, TL08xAC, TL08xBC, TL08xI	8	20		V/µs
t_S	Settling time	V_I = 20 V, C_L = 100 pF, R_L = 2 kΩ			0.1		µs
					20%		
e_N	Input voltage noise density	All PS and NS packages; All TL08xM devices	R_S = 20 Ω, f = 1 kHz		18		nV/√Hz
		All other devices	f = 1 kHz		37		nV/√Hz
			f = 10 kHz		21		
E_N	Input voltage noise	All PS and NS packages; All TL08xM devices	R_S = 20 Ω, f = 10 Hz to 10 kHz		4		$µV_{RMS}$
		All other devices	f = 0.1 Hz to 10 Hz		1.4		$µV_{RMS}$
i_N	Input current noise	R_S = 20 Ω, f = 1 kHz			10		fA/√Hz
	Phase margin	TL08xC, TL08xAC, TL08xBC, TL08xI	G = +1, R_L = 10kΩ, C_L = 20 pF		56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	All PS and NS packages; All TL08xM devices	V_O = 6 V_{RMS}, R_L ≥ 2 kΩ, f = 1 kHz, G = +1, R_S ≤ 1 kΩ		0.003		%
		All other devices	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz		0.00012		%
EMIRR	EMI rejection ratio	TL08xC, TL08xAC, TL08xBC, TL08xI	f = 1 GHz		53		dB
Z_O	Open-loop output impedance	TL07xC, TL07xAC, TL07xBC, TL07xI	f = 1 MHz, I_O = 0 A		125		Ω

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5.10 Typical Characteristics: TL08xH

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

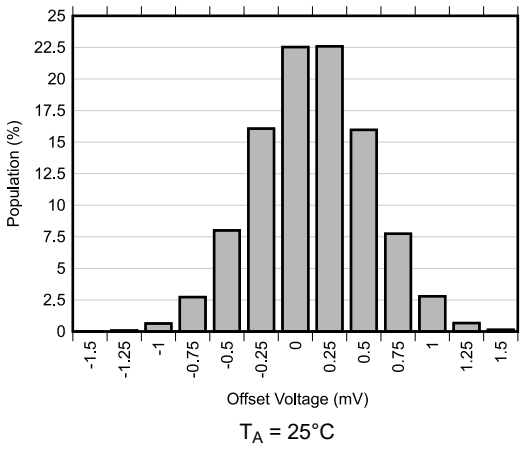


Figure 5-1. Offset Voltage Production Distribution

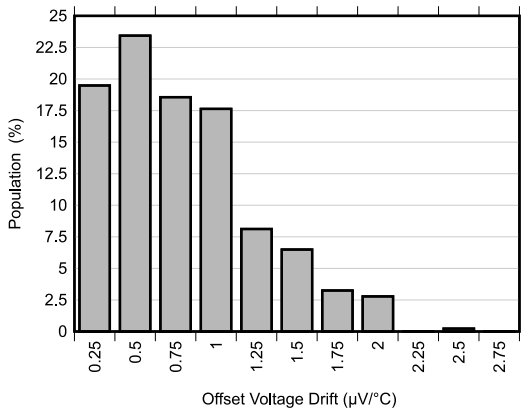


Figure 5-2. Offset Voltage Drift Distribution

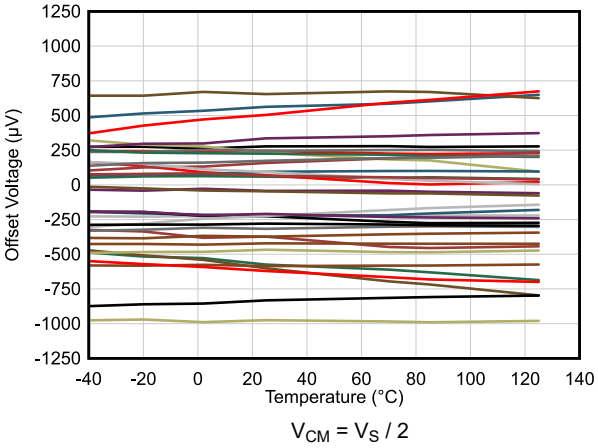


Figure 5-3. Offset Voltage vs Temperature

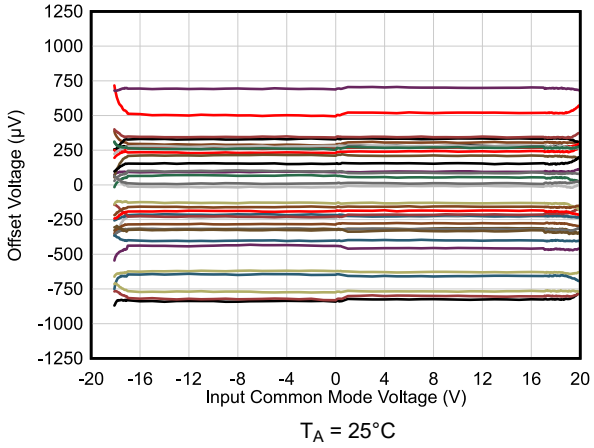


Figure 5-4. Offset Voltage vs Common-Mode Voltage

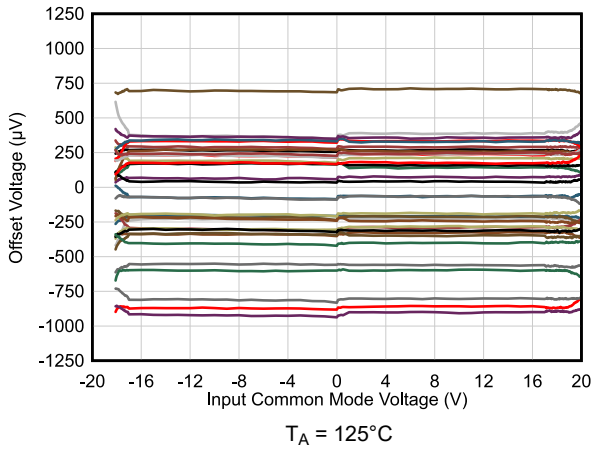


Figure 5-5. Offset Voltage vs Common-Mode Voltage

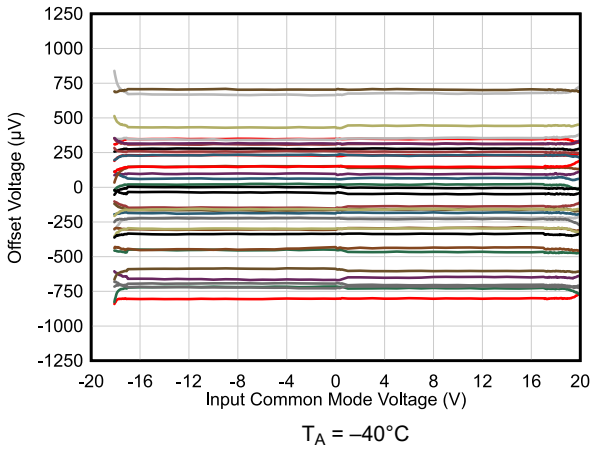


Figure 5-6. Offset Voltage vs Common-Mode Voltage

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5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

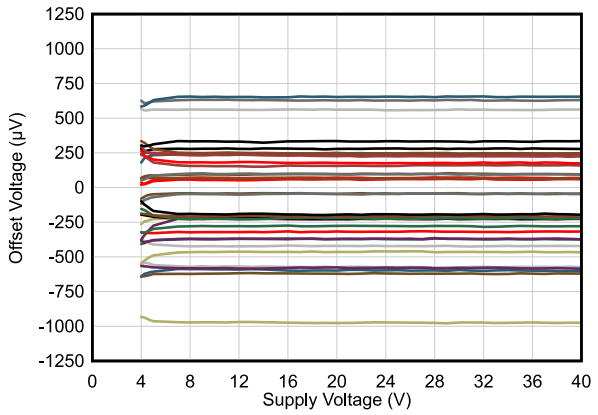


Figure 5-7. Offset Voltage vs Power Supply

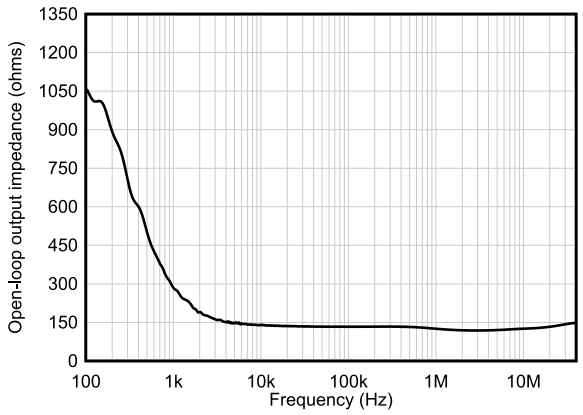


Figure 5-8. Open-Loop Output Impedance vs Frequency

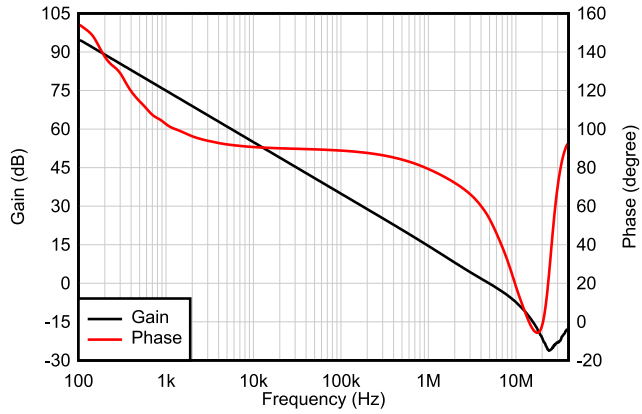


Figure 5-9. Open-Loop Gain and Phase vs Frequency

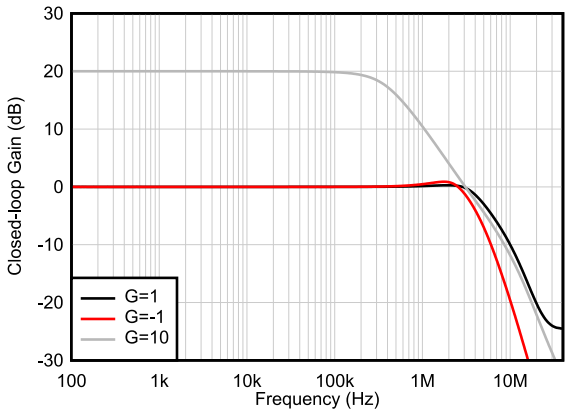


Figure 5-10. Closed-Loop Gain vs Frequency

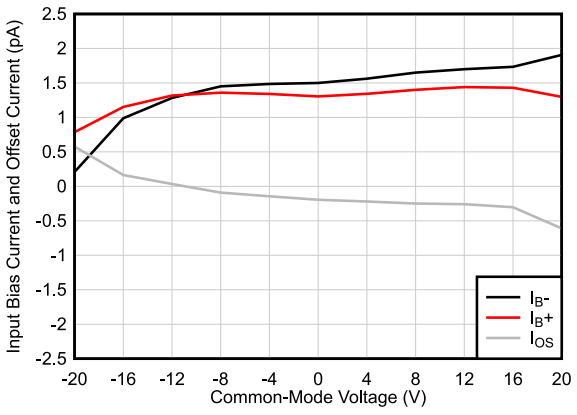


Figure 5-11. Input Bias Current vs Common-Mode Voltage

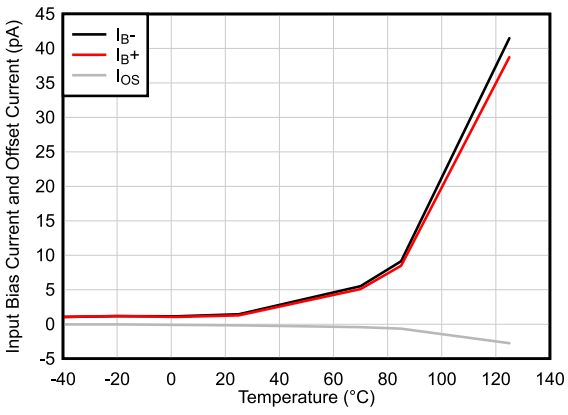


Figure 5-12. Input Bias Current vs Temperature

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5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

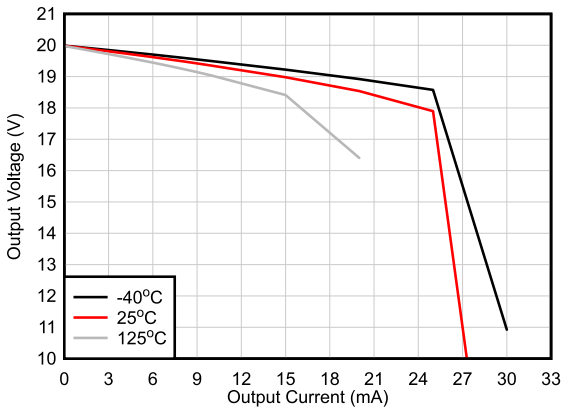


Figure 5-13. Output Voltage Swing vs Output Current (Sourcing)

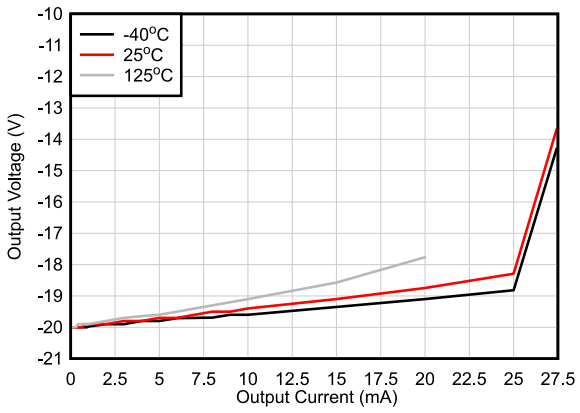
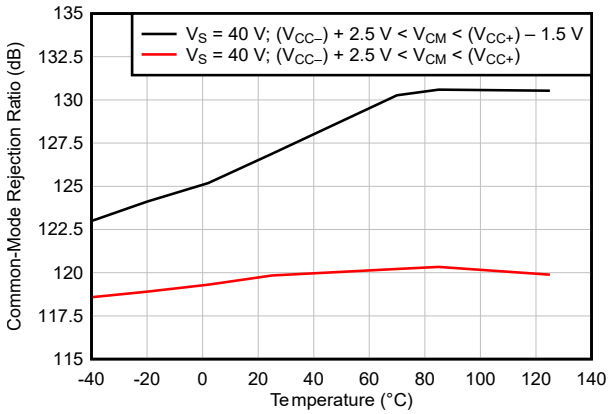
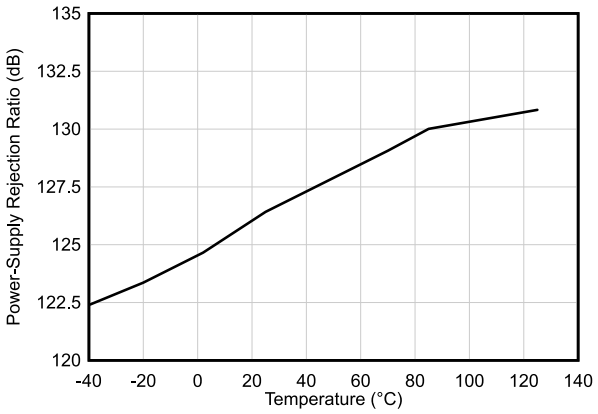


Figure 5-14. Output Voltage Swing vs Output Current (Sinking)



f = 0Hz

Figure 5-15. CMRR vs Temperature (dB)



f = 0Hz

Figure 5-16. PSRR vs Temperature (dB)

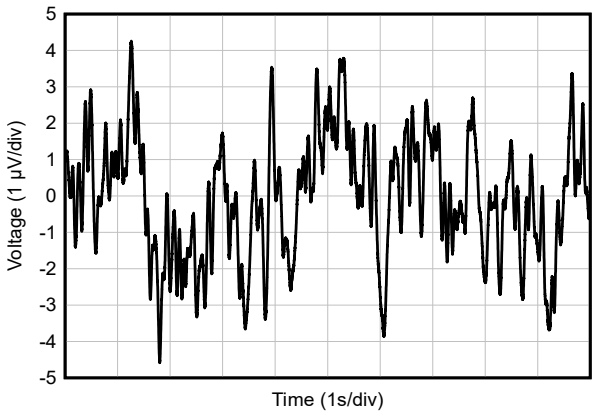


Figure 5-17. 0.1Hz to 10Hz Noise

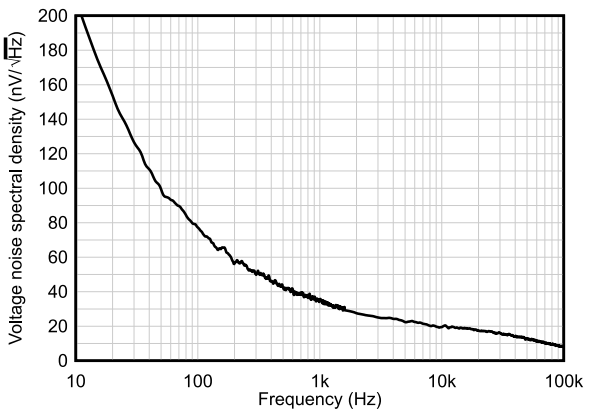


Figure 5-18. Input Voltage Noise Spectral Density vs Frequency

5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

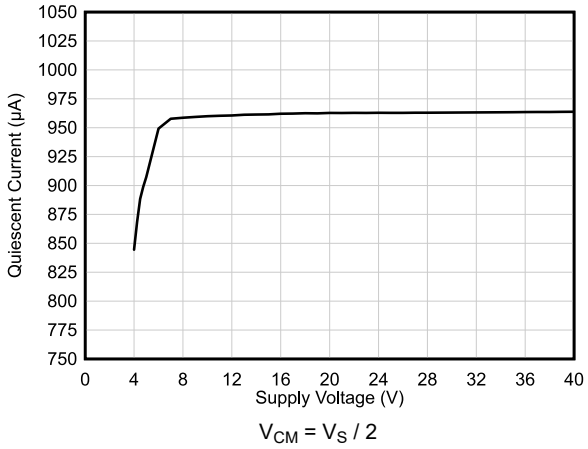


Figure 5-19. Quiescent Current vs Supply Voltage

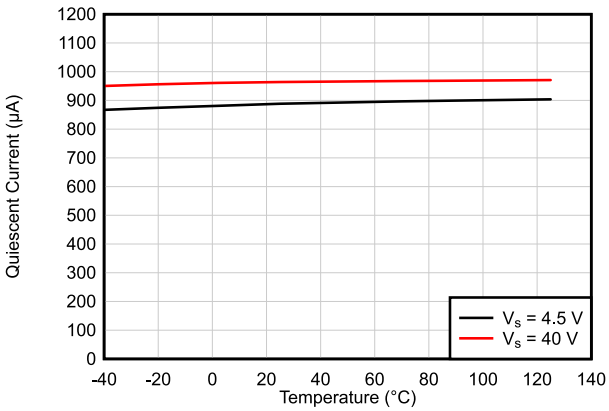


Figure 5-20. Quiescent Current vs Temperature

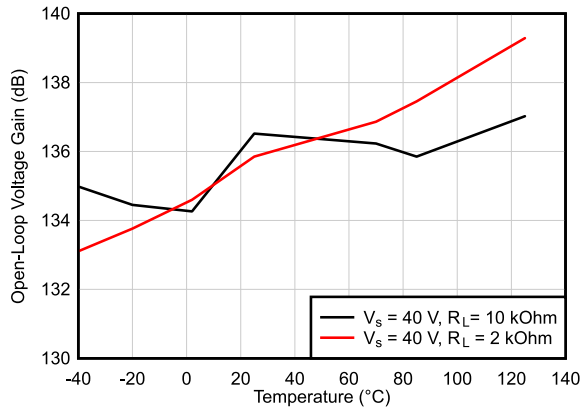


Figure 5-21. Open-Loop Voltage Gain vs Temperature (dB)

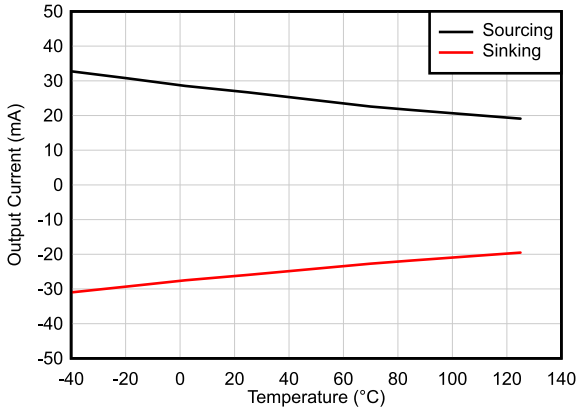


Figure 5-22. Short-Circuit Current vs Temperature

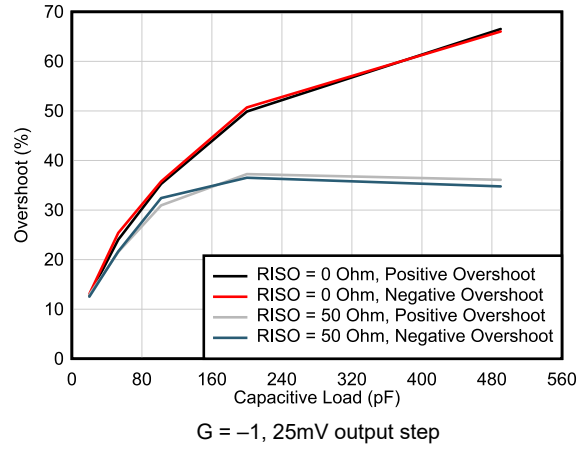


Figure 5-23. Small-Signal Overshoot vs Capacitive Load

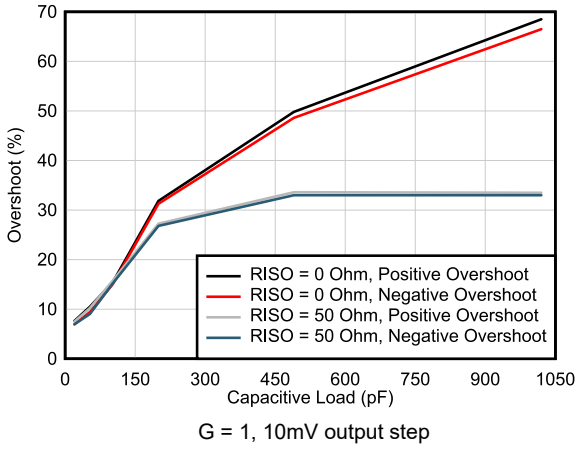


Figure 5-24. Small-Signal Overshoot vs Capacitive Load

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5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

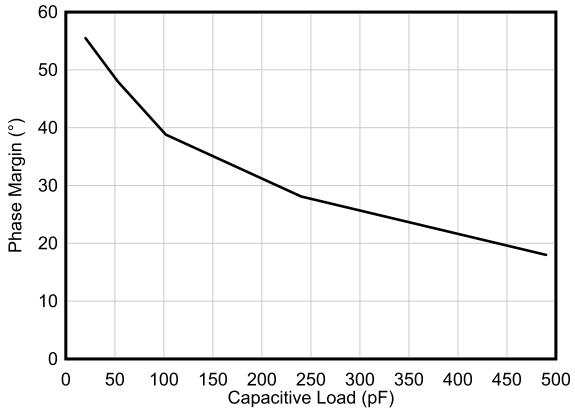
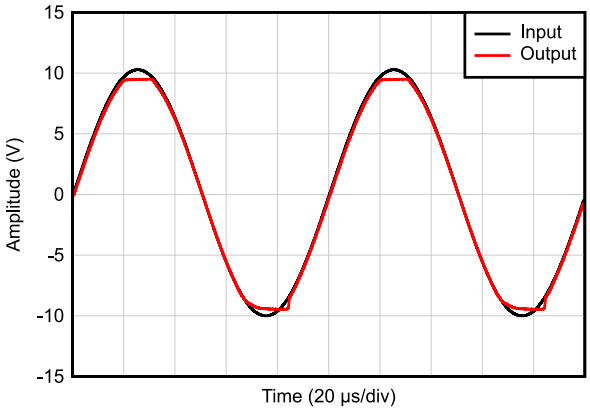
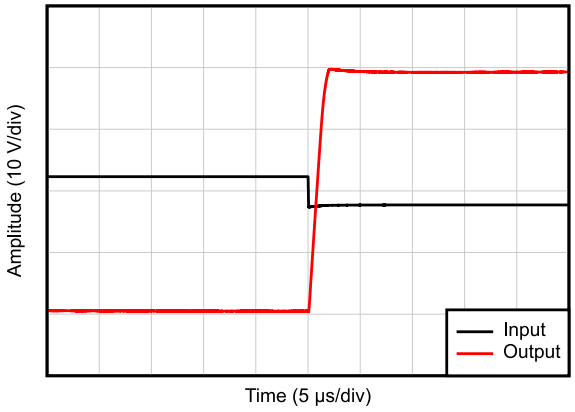


Figure 5-25. Phase Margin vs Capacitive Load



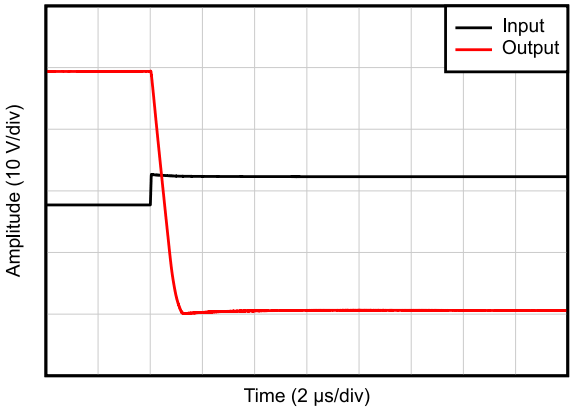
V_S = ±10V, V_{IN} = V_{OUT}

Figure 5-26. No Phase Reversal



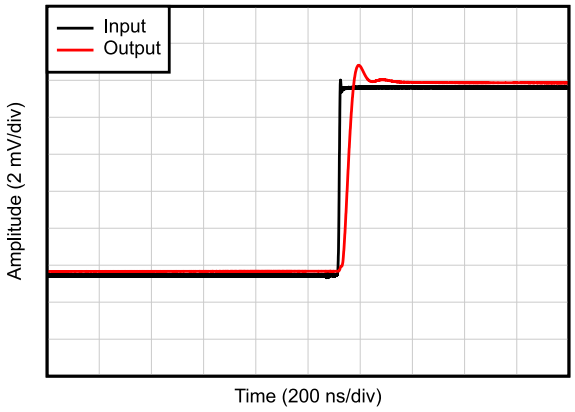
G = –10

Figure 5-27. Positive Overload Recovery



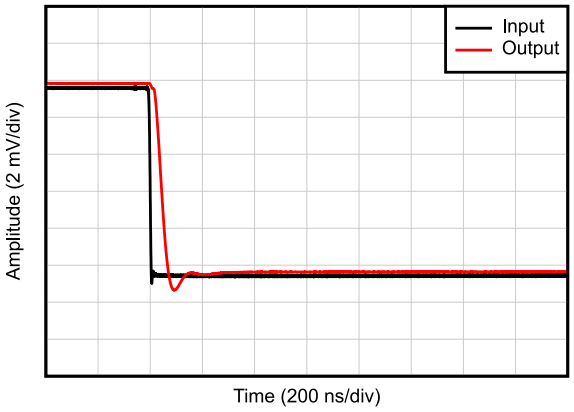
G = –10

Figure 5-28. Negative Overload Recovery



C_L = 20pF, G = 1, 10mV step response

Figure 5-29. Small-Signal Step Response, Rising



C_L = 20pF, G = 1, 10mV step response

Figure 5-30. Small-Signal Step Response, Falling

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5.10 Typical Characteristics: TL08xH (continued)

at T_A = 25°C, V_S = 40V (±20V), V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 20pF (unless otherwise noted)

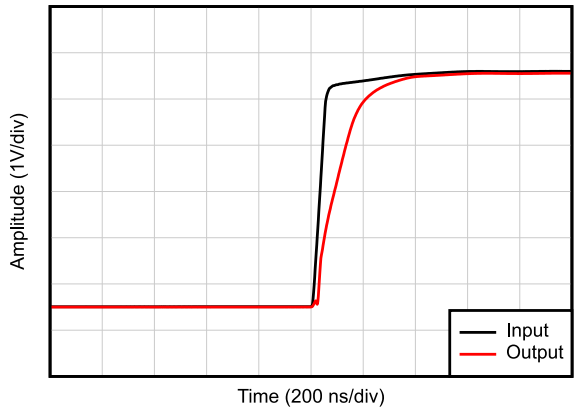


Figure 5-31. Large-Signal Step Response (Rising)

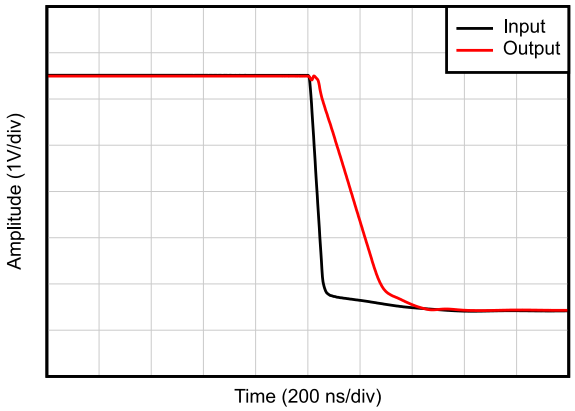


Figure 5-32. Large-Signal Step Response (Falling)

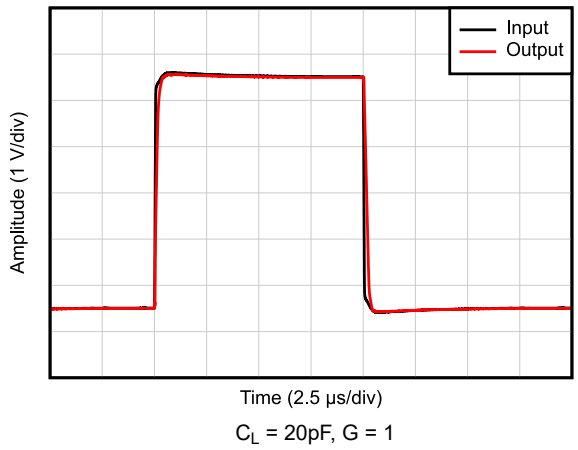


Figure 5-33. Large-Signal Step Response

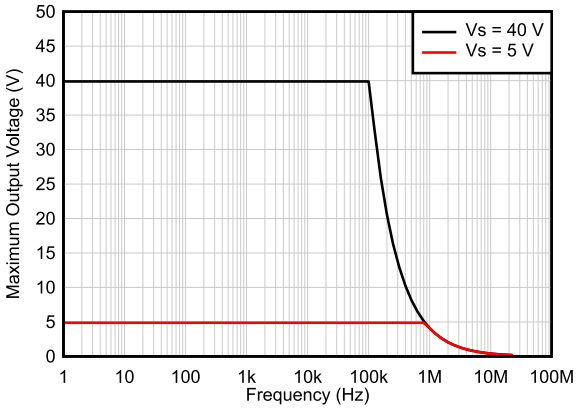


Figure 5-34. Maximum Output Voltage vs Frequency

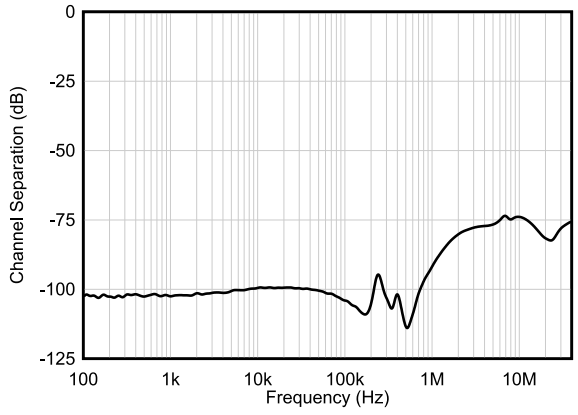


Figure 5-35. Channel Separation vs Frequency

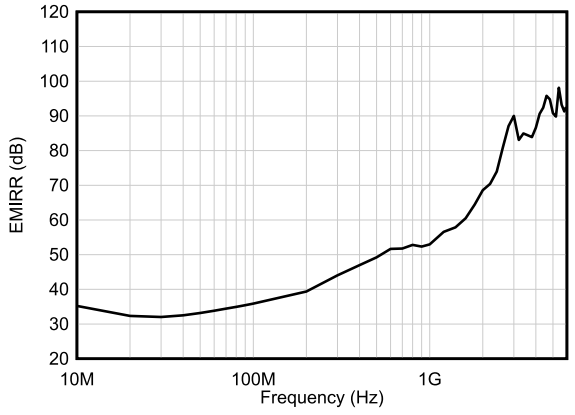


Figure 5-36. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

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6 Parameter Measurement Information

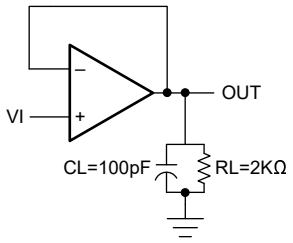


Figure 6-1. Test Figure 1

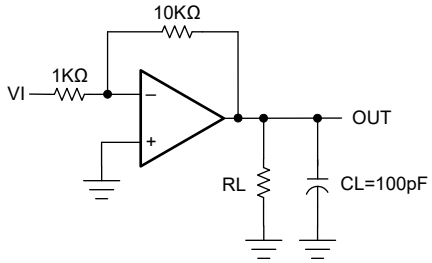


Figure 6-2. Test Figure 2

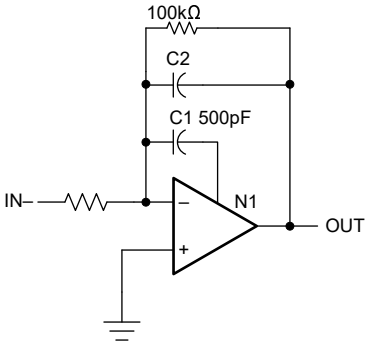


Figure 6-3. Test Figure 3

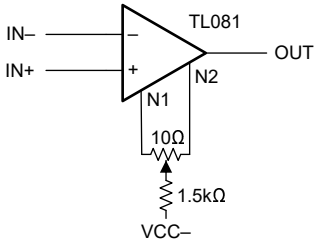


Figure 6-4. Test Figure 4 (for SO Package Only)

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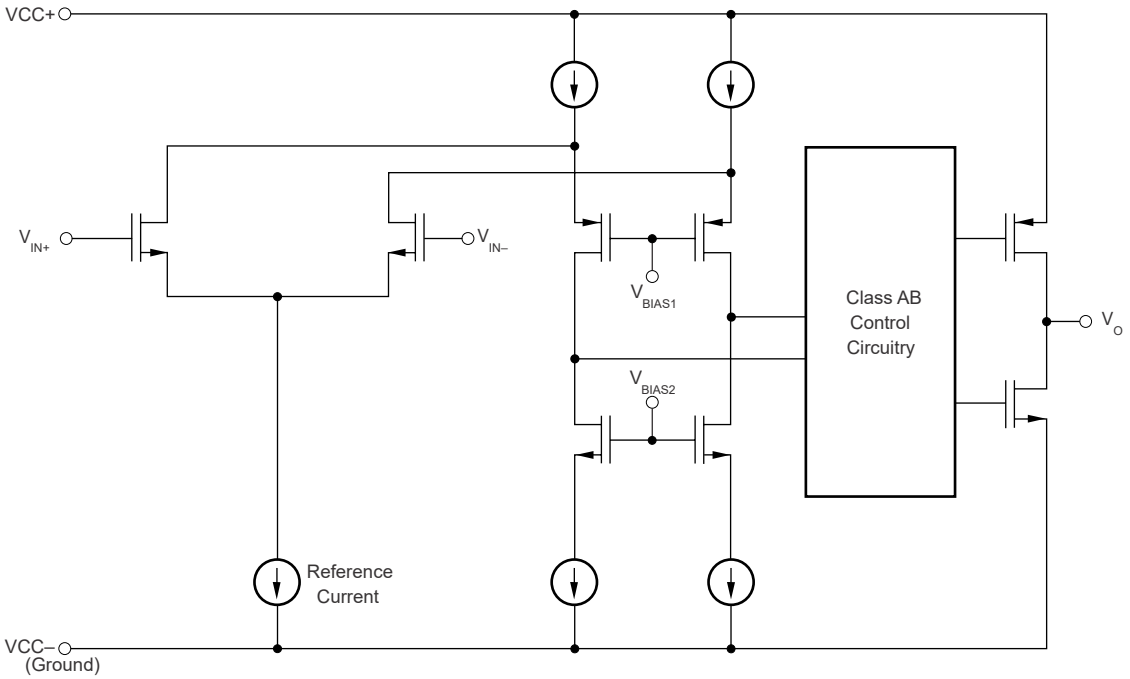
7 Detailed Description

7.1 Overview

The TL08xH family (TL081H, TL082H, and TL084H) is the next-generation family of the industry standard TL08x (TL081, TL082, and TL084) high-voltage general purpose amplifiers. These devices provide outstanding value for cost-sensitive applications requiring high slew rate with high voltage signals, such as motor drive and inverter systems.

A robust MUX-friendly input stage enhances flexibility in design, with common-mode voltage range extending to the positive rail as well as improved settling time in multi-channel applications. Low offset voltage (1mV, typ) and low offset voltage drift (2µV/°C) allows the TL08xH family to be used in rugged applications requiring precision current and voltage sensing. High voltage operation (up to 40V) and high slew rate (20V/µs) make the TL08xH family a premier choice for high-voltage applications with fast transients.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Total Harmonic Distortion

Electronic components within a circuit generate harmonic distortion in the audio signal. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices generate little harmonic distortion when used in audio signal applications.

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier changes the output when there is a change on the input. These devices have a 20V/µs slew rate.

7.4 Device Functional Modes

These devices are powered on when the supply is connected. This device operates as a single-supply operational amplifier or dual-supply amplifier depending on the application.

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8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

8.2 Typical Applications

8.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes positive voltage as a negative voltage of the same magnitude. In the same manner, amplifier also makes negative voltages positive.

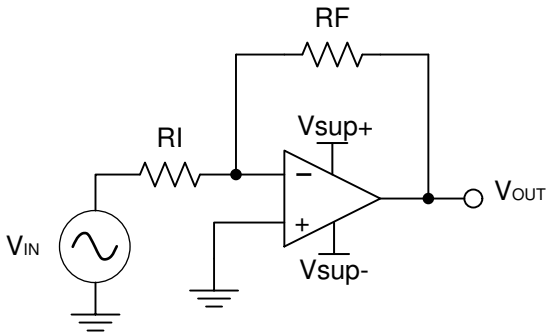


Figure 8-1. Schematic for Inverting Amplifier Application

8.2.1.1 Design Requirements

Choose the supply voltage higher than input and output ranges. For instance, this application scales a signal of ±0.5V to ±1.8V. Setting the supply at ±12V is sufficient to accommodate this application.

8.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

After the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit uses currents in the milliampere range. This example chooses 10kΩ for RI, which means that 36kΩ is used for RF. RF value is determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

8.2.1.3 Application Curve

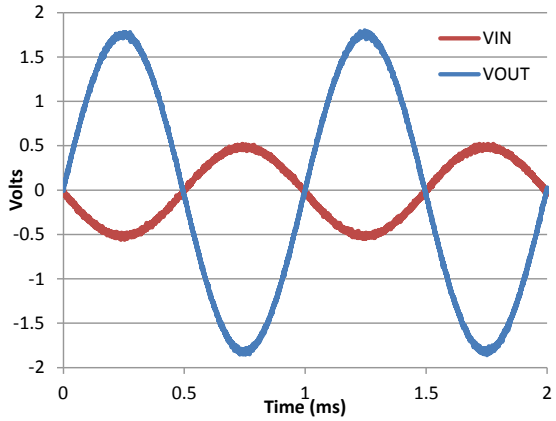


Figure 8-2. Input and Output Voltages of the Inverting Amplifier

8.3 Power Supply Recommendations

CAUTION

Supply voltages larger than 36V for a single-supply or outside the range of ±18V for a dual-supply can permanently damage the device (see Section 5.1).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see Section 8.4.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCB are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Keep digital and analog grounds physically separate, and pay attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible to keep them separate, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Section 8.4.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring significantly helps reduce leakage currents from nearby traces that are at different potentials.

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8.4.2 Layout Examples

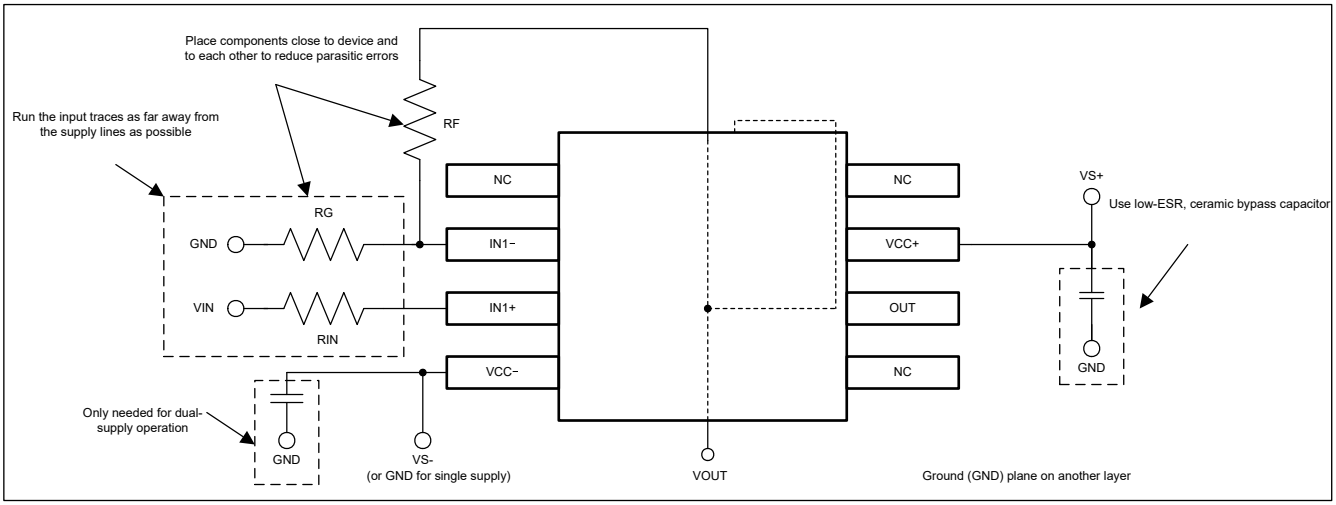


Figure 8-3. Operational Amplifier Board Layout for Non-inverting Configuration

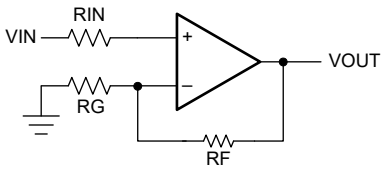


Figure 8-4. Operational Amplifier Schematic for Non-inverting Configuration

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature

PART NUMBER	DEFINITION
TL08*xyzzzzzz*	*x* is the channel count
	If *y* = H, the die is manufactured on the latest flow (CSO: RFB). Section 5.7 and Section 5.10 describe the performance of the new die.
	If *y* ≠ H and *y* ≠ M, the die is manufactured on the legacy flow (CSO: SFAB) or the latest flow (CSO: RFB). Section 5.8 and Section 5.9 describe the performance of the original die.
	If *y* = M, the device is specified for the extended temperature range of –55°C to +125°C. The die is manufactured on the legacy flow (CSO:SFAB). The letters and numbers represented by *z* are grade-out and package options described in Section 5.8 and the *Package Option Addendum* at the end of this data sheet.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (June 2024) to Revision O (September 2025)	Page
• Changed V_n = 18nV/√Hz to V_n = 37nV/√Hz in *Features*	1
• Updated *Device Information* table	1
• Changed TL081 to TL081 SOIC only in figure1 and TL081 (Each Amplifier) in figure2 of *Logic Symbols*	1
• Updated pin name from V– to VCC– and V+ to VCC+ in Figure 4-1 and Figure 4-2	3
• Updated caption for Figure 4-3	3
• Updated caption for Figure 4-4	3

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- Changed TL081x to TL081C in Table 4-2 ... 3
- Updated HBM value from 2000V to 1500V ... 9
- Deleted plots for *THD+N Ratio vs Frequency*, *THD+N vs Output Amplitude*, and *CMRR and PSRR vs Frequency* ... 17
- Added "(for SO Package Only)" to Figure 6-4, *Test Figure 4* ... 23
- Deleted *System Examples* section ... 26
- Updated 2nd bullet in *Layout Guidelines* ... 26
- Added *Device Nomenclature* table ... 28

Changes from Revision M (December 2021) to Revision N (June 2024) **Page**

- Changed Absolute Maximum Ratings, ESD Ratings, Recommended Operating Conditions, and Thermal Information sections by merging TL08xH and TL08xx specifications ... 9
- Changed Electrical Characteristics tables by merging TL08xC, TL08xAC, TL08xBC, TL08xI, and TL08xM specifications ... 14
- Increased gain bandwidth of all non-NS/non-PS packages and non-TL08xM devices from 3 MHz to 5.25 MHz ... 14
- Merged TL08xC, TL08xAC, TL08xBC, TL08xI, and TL08xM Switching Characteristics tables and renamed to Electrical Characteristics (AC) ... 16
- Changed input voltage noise density at 1 kHz for all non-PS/non-NS packages and all non-TL08xM devices to 37 nV/√Hz ... 16
- Changed THD+N for all non-PS/non-NS packages and all non-TL08xM devices to 0.00012% ... 16
- Updated *Functional Block Diagram* and *Feature Description* sections ... 24

Changes from Revision L (July 2021) to Revision M (December 2021) **Page**

- Corrected DCK pinout diagram and table in *Pin Configurations and Functions* section ... 3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9851501Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB
5962-9851501QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9851501QPA TL082M
5962-9851503Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB
5962-9851503QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503QCA TL084MJB
TL081ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	081AC
TL081ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC
TL081ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC
TL081ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081ACP
TL081ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081ACP
TL081BCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	081BC
TL081BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC
TL081BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC
TL081BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081BCP
TL081BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081BCP
TL081CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	TL081C
TL081CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C
TL081CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C
TL081CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081CP
TL081CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081CP
TL081CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL081CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T081
TL081CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T081
TL081HIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T81V

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL081HIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T81V
TL081HIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IP
TL081HIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IP
TL081HIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL081D
TL081HIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL081D
TL081IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I
TL081IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I
TL081IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL081IP
TL081IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL081IP
TL082ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	082AC
TL082ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC
TL082ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC
TL082ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082ACP
TL082ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082ACP
TL082ACPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A
TL082ACPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A
TL082BCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	082BC
TL082BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082BCP
TL082BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082BCP
TL082BCPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL082CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C
TL082CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C
TL082CDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082CP
TL082CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082CP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL082CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPSRG4	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082HIDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082F
TL082HIDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082F
TL082HIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082D
TL082HIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082D
TL082HIPWR	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082HPW
TL082HIPWR.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082HPW
TL082IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082IDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL082IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL082IP
TL082IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL082IP
TL082IPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	-40 to 85	
TL082IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082
TL082IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082
TL082MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB
TL082MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB
TL082MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL082MJG
TL082MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL082MJG
TL082MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9851501QPA TL082M
TL082MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9851501QPA TL082M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL084ACD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL084AC
TL084ACDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC
TL084ACDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC
TL084ACN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084ACN
TL084ACN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084ACN
TL084ACNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A
TL084ACNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A
TL084BCDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDR1G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDR1G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL084BCN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084BCN
TL084BCN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084BCN
TL084BCNE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	0 to 70	
TL084CD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL084C
TL084CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C
TL084CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C
TL084CDRG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL084C
TL084CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084CN
TL084CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084CN
TL084CNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084
TL084CNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084
TL084CPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	T084
TL084CPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	T084
TL084CPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084
TL084CPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084
TL084HIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084HID
TL084HIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084HID
TL084HIDYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL084HIDYYR.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY
TL084HIDYYRG4	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY
TL084HIDYYRG4.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY
TL084HIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TL084PW
TL084HIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084PW
TL084IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I
TL084IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I
TL084IDR1G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084I
TL084IDR1G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084I
TL084IDRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL084IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL084IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL084IN
TL084IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL084IN
TL084ING4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL084IN
TL084ING4.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL084IN
TL084MFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MFK
TL084MFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MFK
TL084MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB
TL084MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB
TL084MJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MJ
TL084MJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MJ
TL084MJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503QCA TL084MJB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL084MJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB
TL084QD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	TL084Q
TL084QDG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	TL084Q
TL084QDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q
TL084QDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q
TL084QDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q
TL084QDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

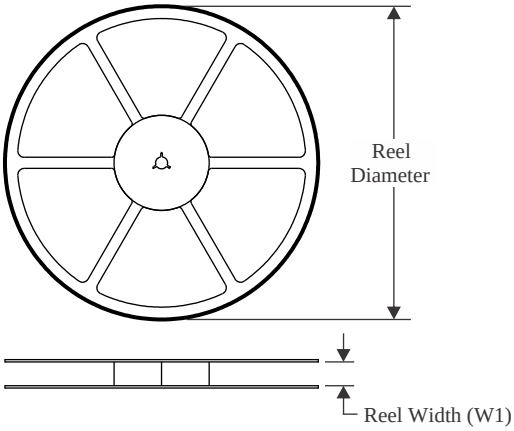
- Catalog : TL082, TL084
- Automotive : TL082-Q1, TL082-Q1
- Military : TL082M, TL084M

NOTE: Qualified Version Definitions:

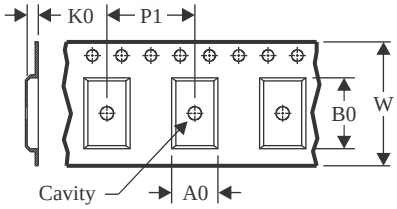
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

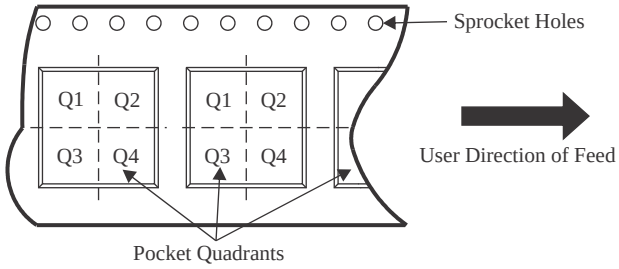


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

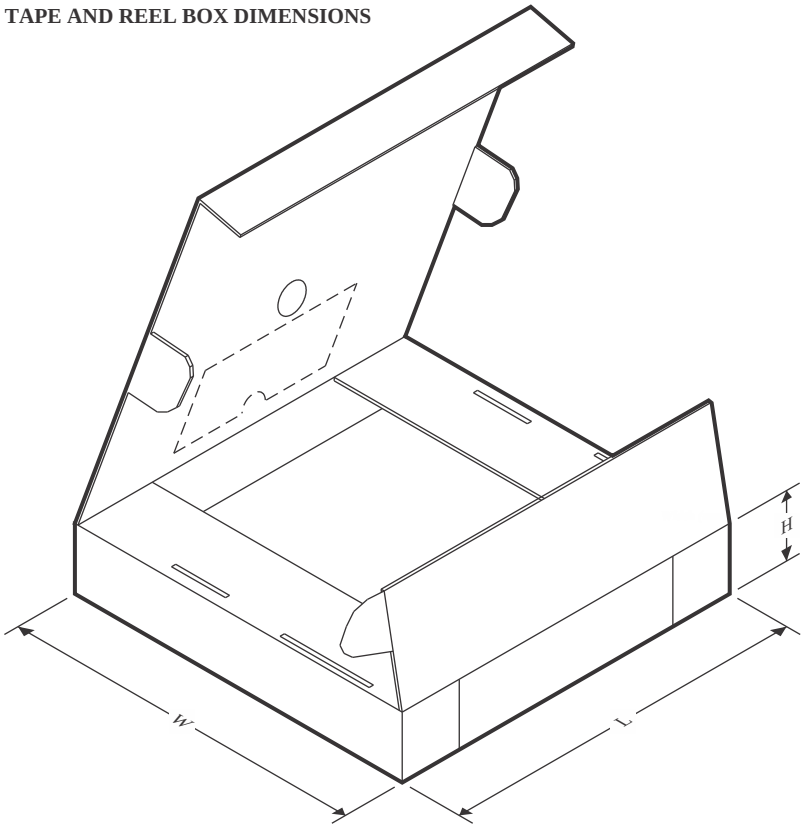


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL081HIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL081HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL081HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082BCDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL082HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084BCDR1G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL084HIDYYRG4	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL084HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084IDR1G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

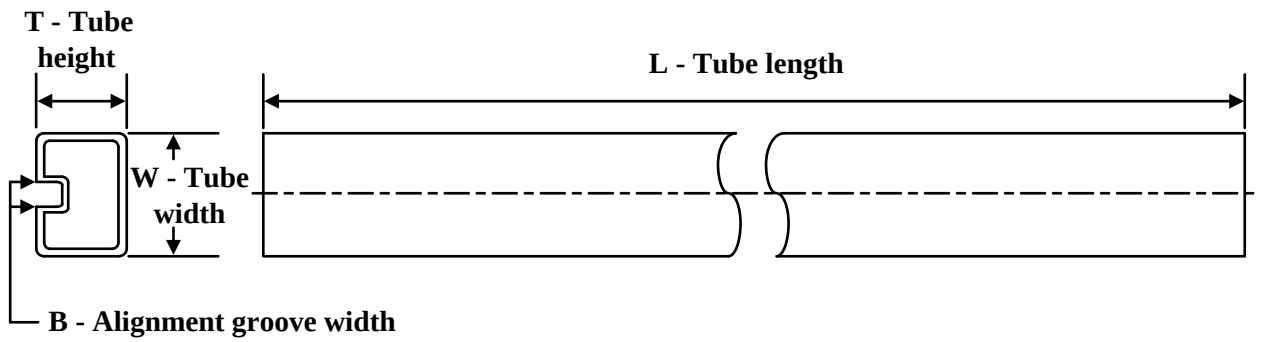


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL081HIDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TL081HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL081HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL081IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACPSR	SO	PS	8	2000	353.0	353.0	32.0
TL082BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082BCDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL082CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL082CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082HIDR	SOIC	D	8	3000	367.0	367.0	35.0
TL082HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL082HIPWR	TSSOP	PW	8	3000	353.0	353.0	32.0
TL082IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL084ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084ACNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL084BCDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084BCDR1G4	SOIC	D	14	2500	353.0	353.0	32.0
TL084CDR	SOIC	D	14	2500	367.0	367.0	35.0
TL084CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084CNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL084CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084CPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084CPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084HIDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL084HIDYYRG4	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL084HIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084HIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084IDR	SOIC	D	14	2500	367.0	367.0	35.0
TL084IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084IDR1G4	SOIC	D	14	2500	353.0	353.0	32.0
TL084QDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084QDRG4	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9851501Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9851503Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL081ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL081ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL081BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL081BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL081CP	P	PDIP	8	50	506	13.97	11230	4.32
TL081CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL081IP	P	PDIP	8	50	506	13.97	11230	4.32
TL081IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL082ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL082BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082CP	P	PDIP	8	50	506	13.97	11230	4.32
TL082CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL082MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN.A	N	PDIP	14	25	506	13.97	11230	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL084BCN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084CN	N	PDIP	14	25	506	13.97	11230	4.32
TL084CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084IN	N	PDIP	14	25	506	13.97	11230	4.32
TL084IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084ING4	N	PDIP	14	25	506	13.97	11230	4.32
TL084ING4.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084MFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA

GENERIC PACKAGE VIEW

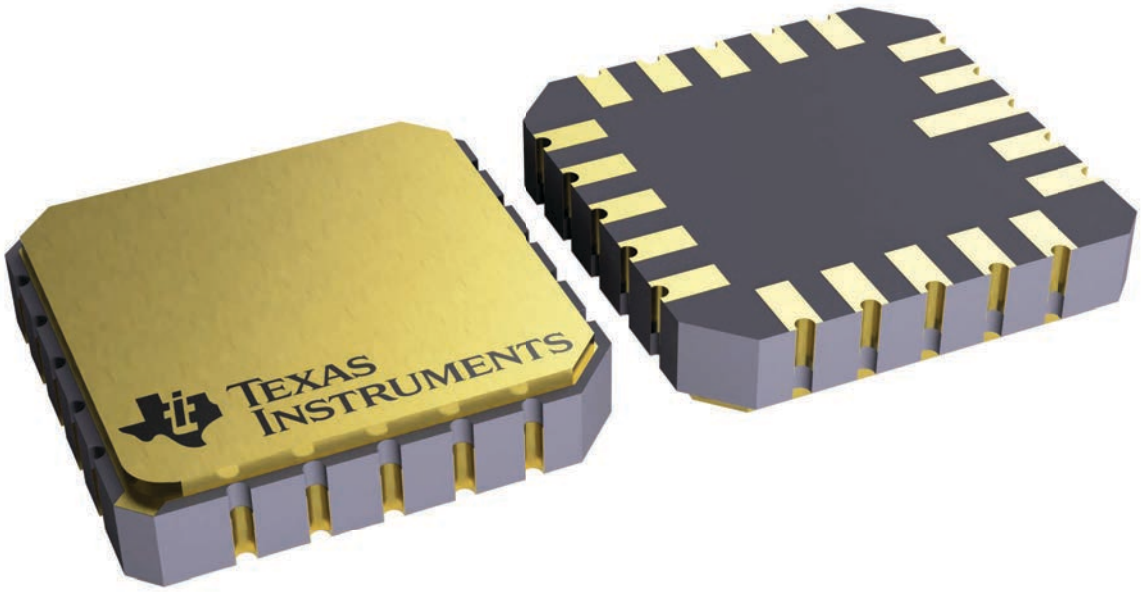
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

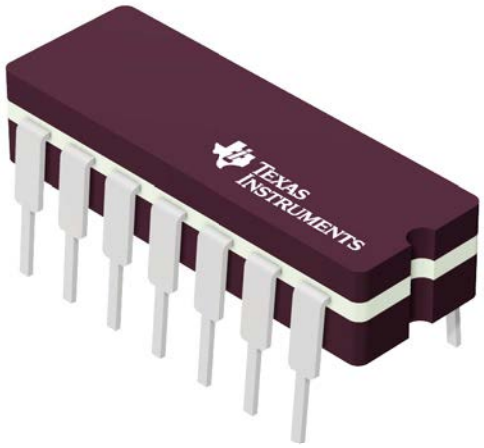


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

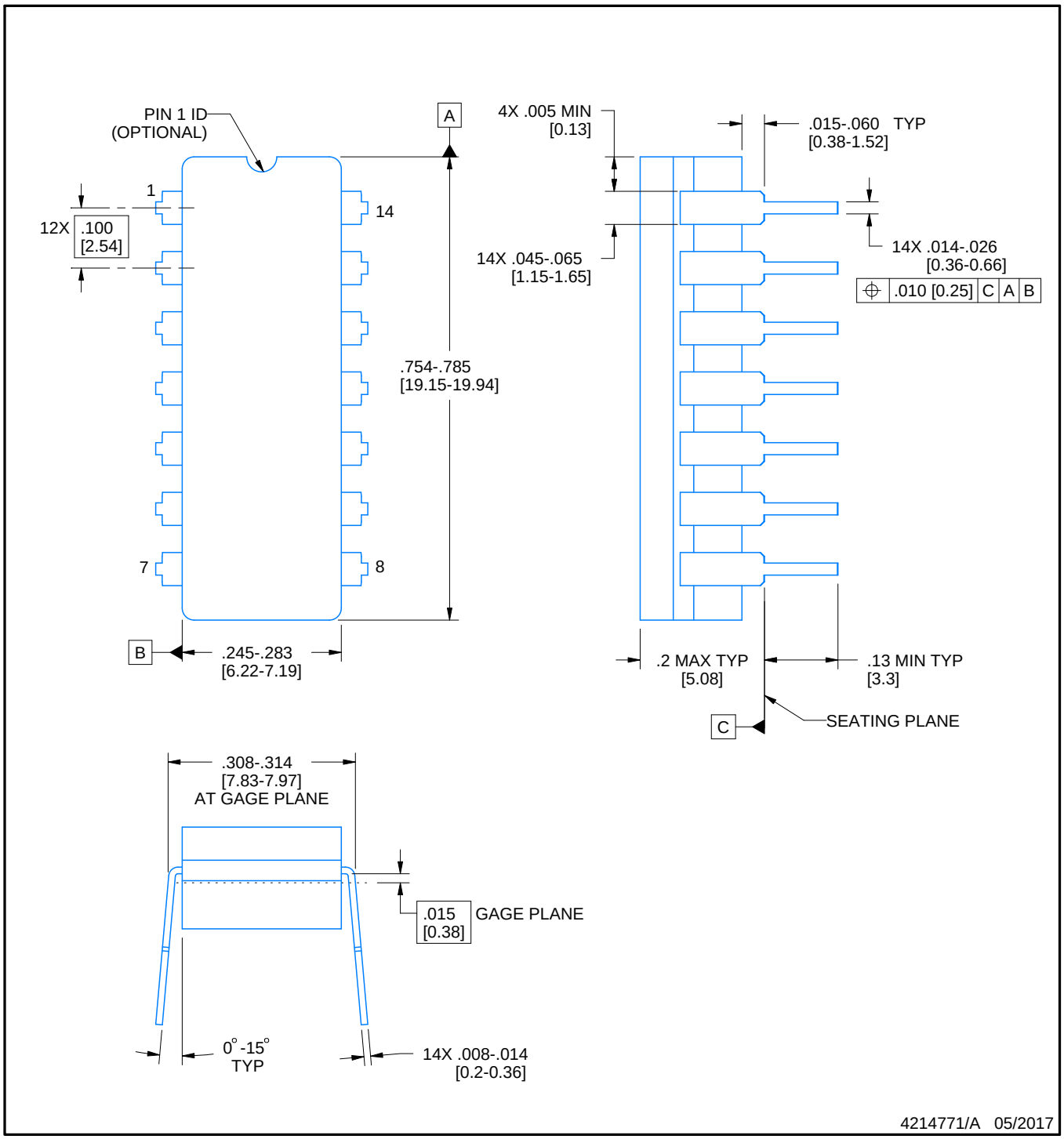


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

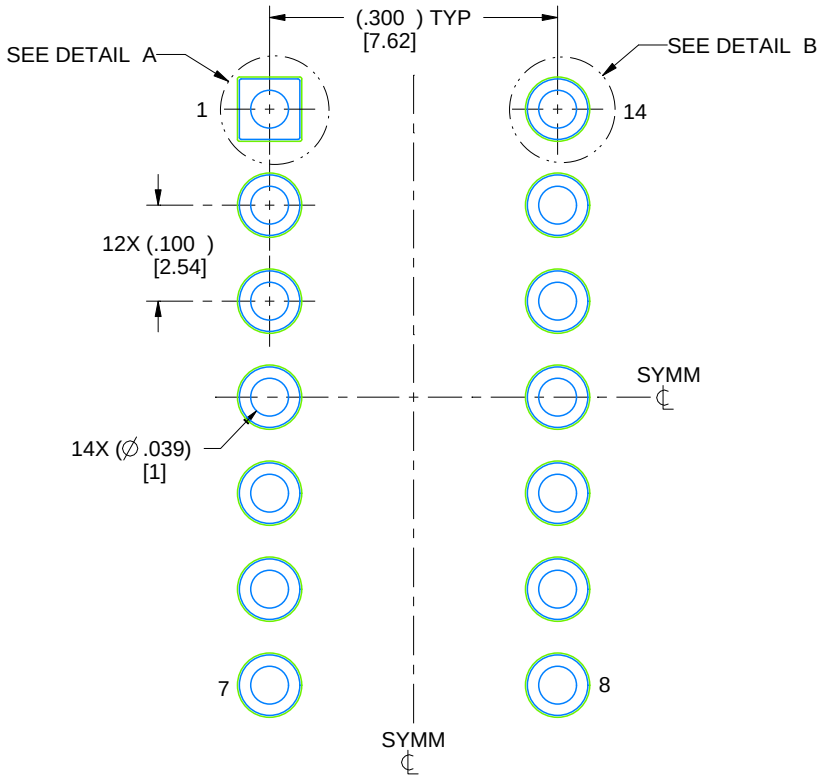
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

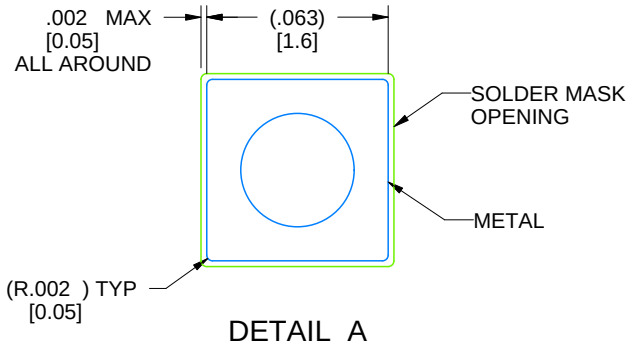
J0014A

CDIP - 5.08 mm max height

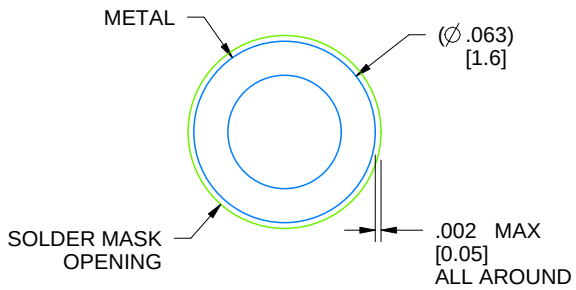
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

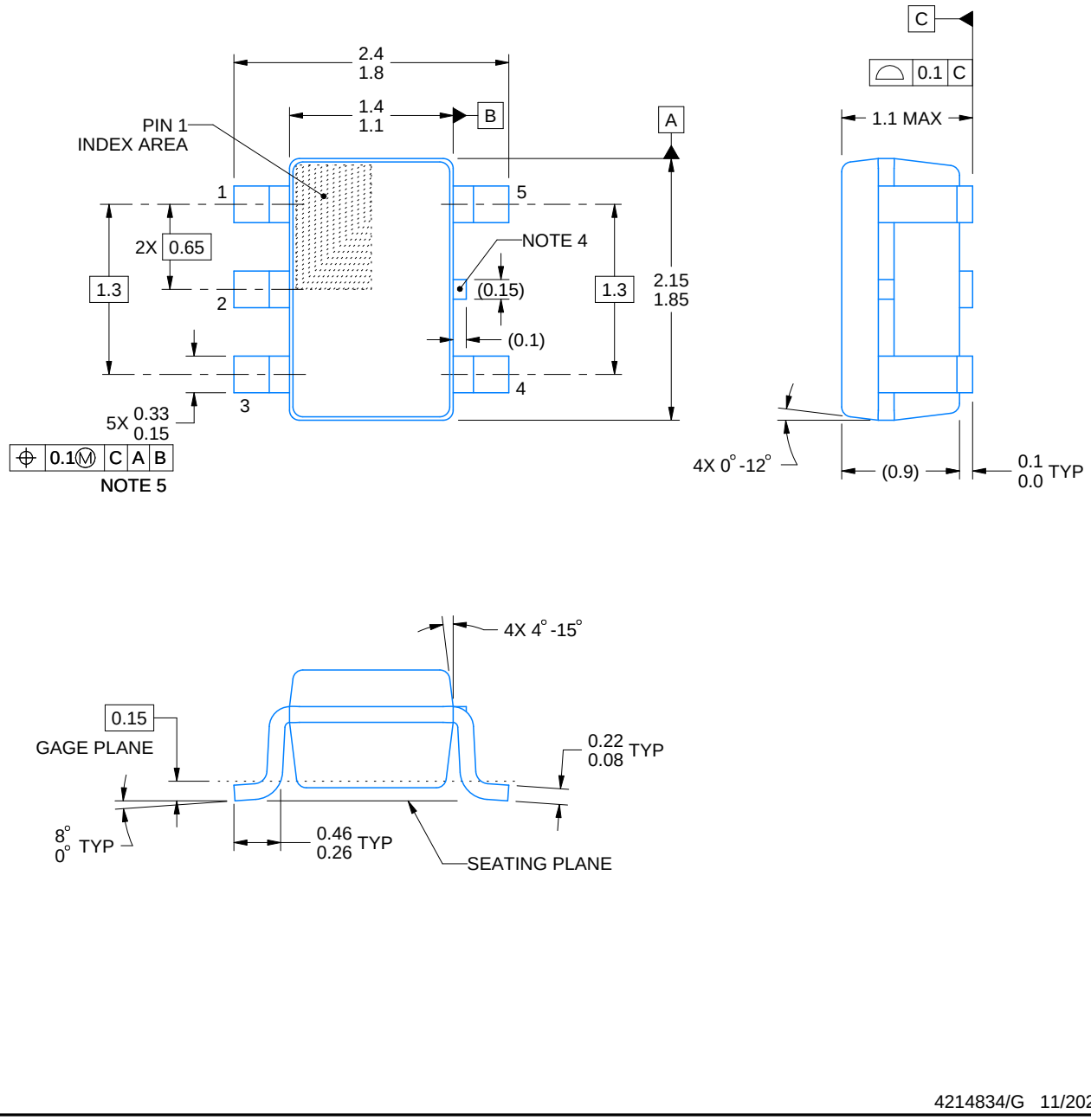
4214771/A 05/2017

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

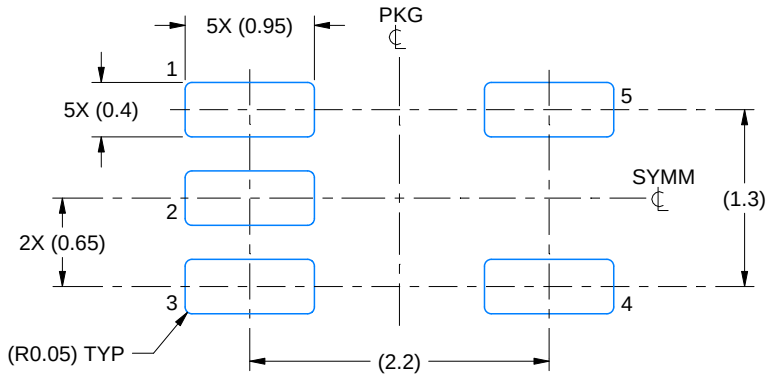
SMALL OUTLINE TRANSISTOR



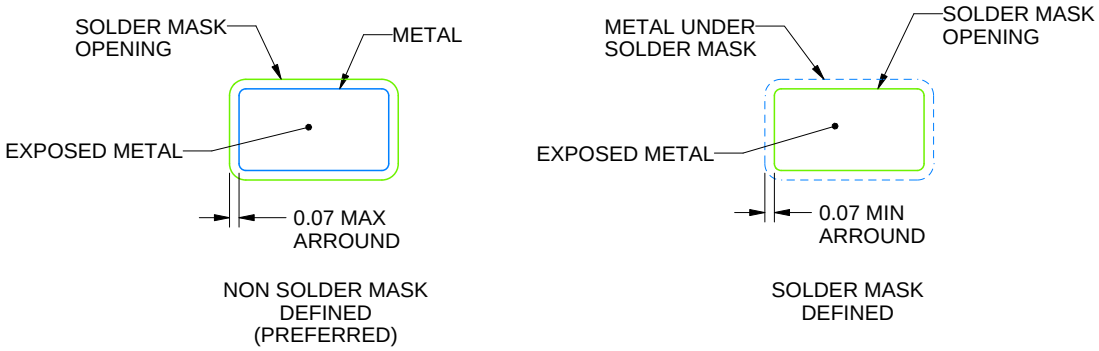
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

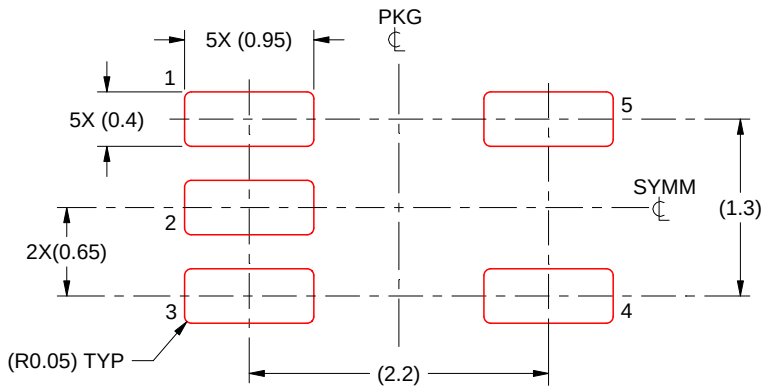


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

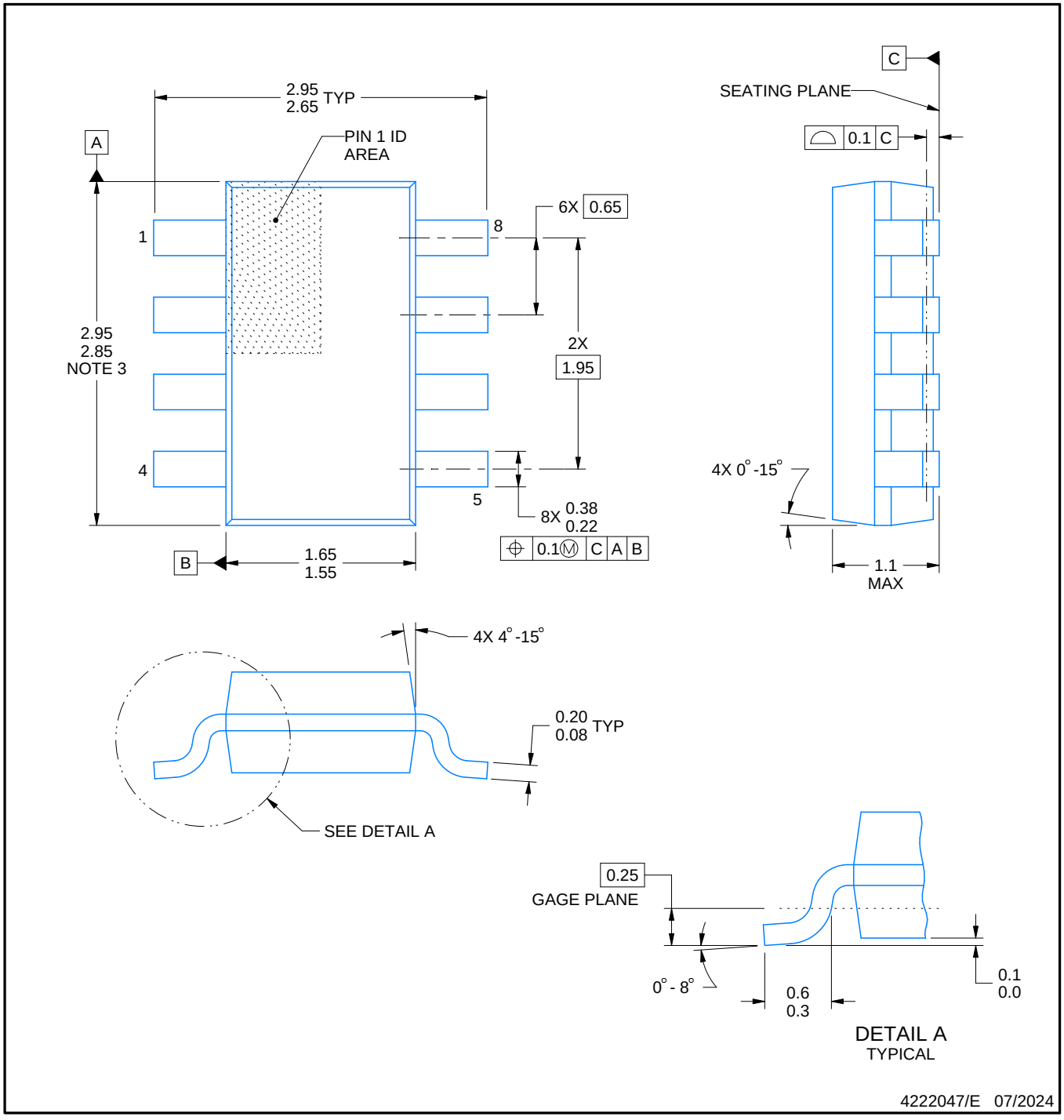
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

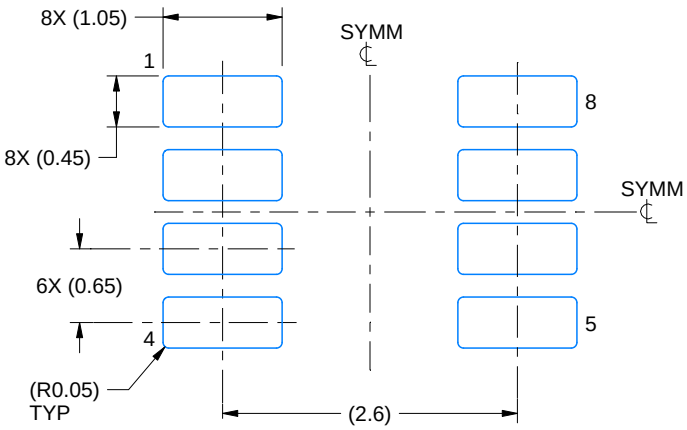
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

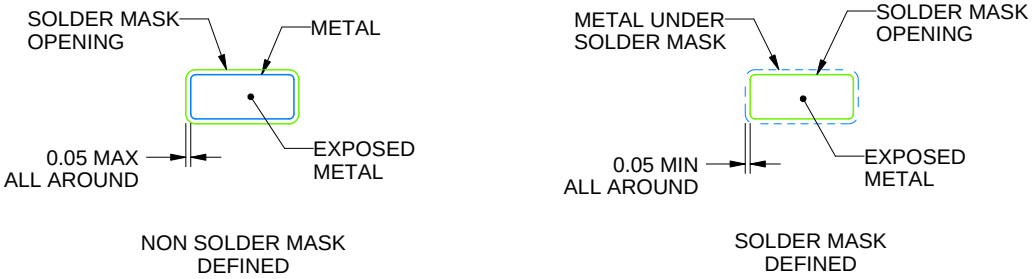


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

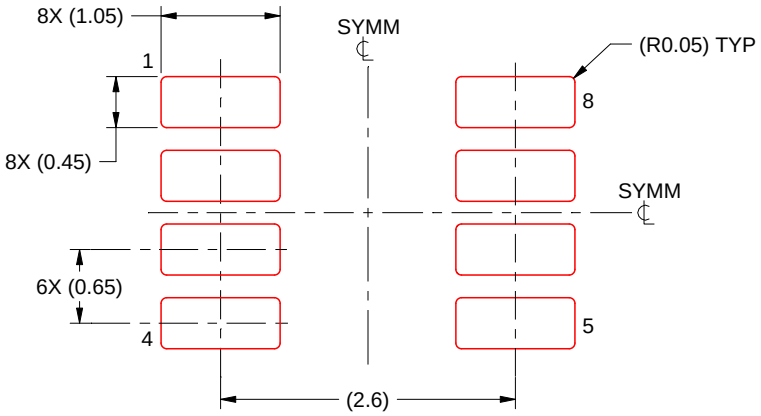
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

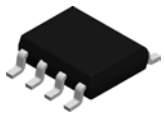


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

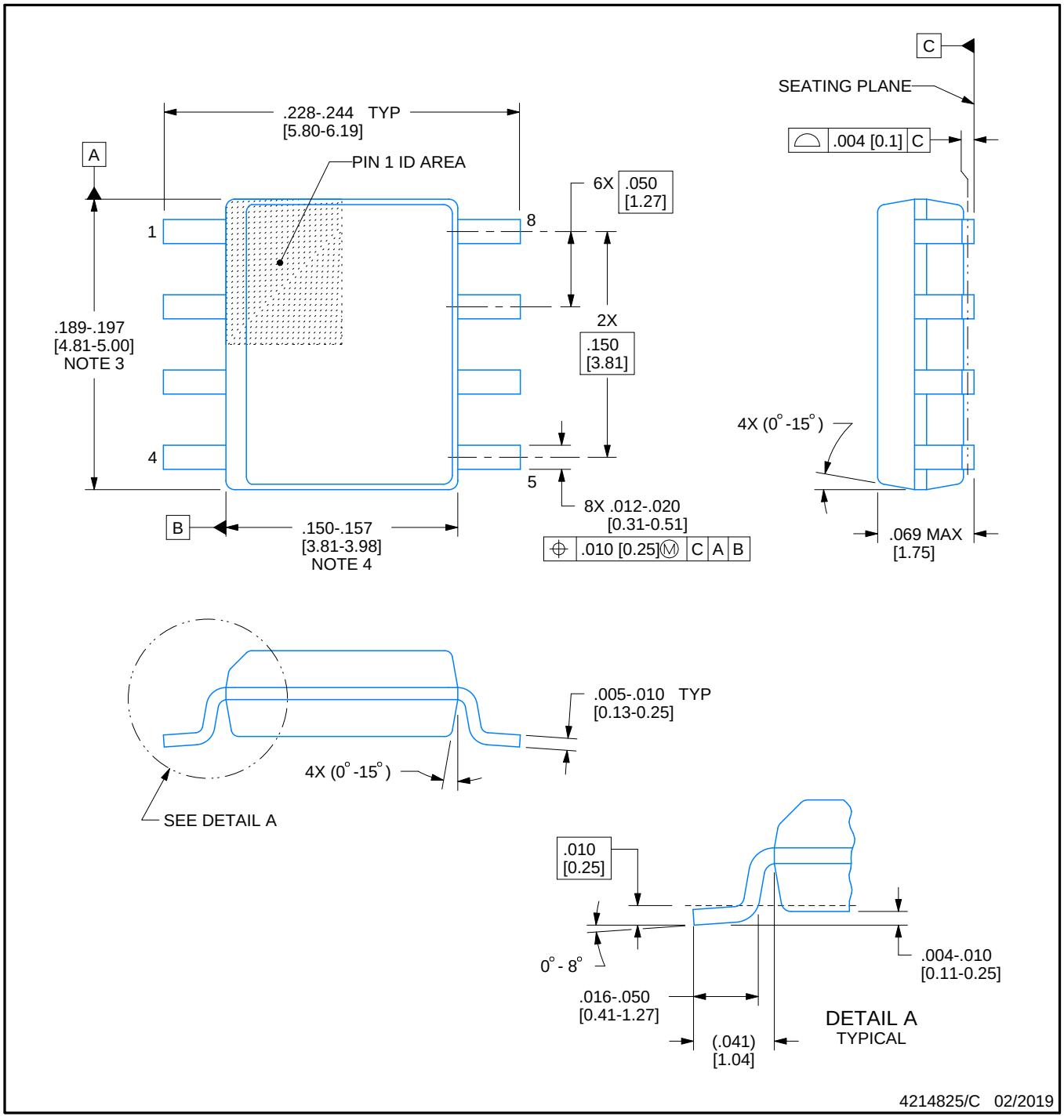


PACKAGE OUTLINE

D0008A

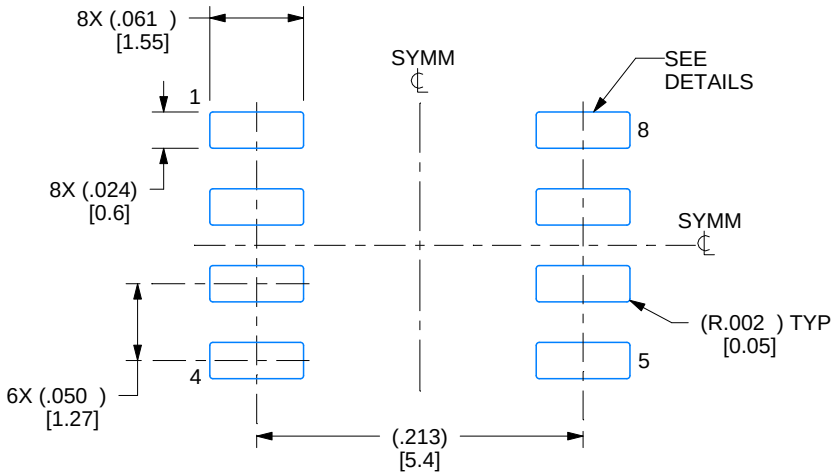
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

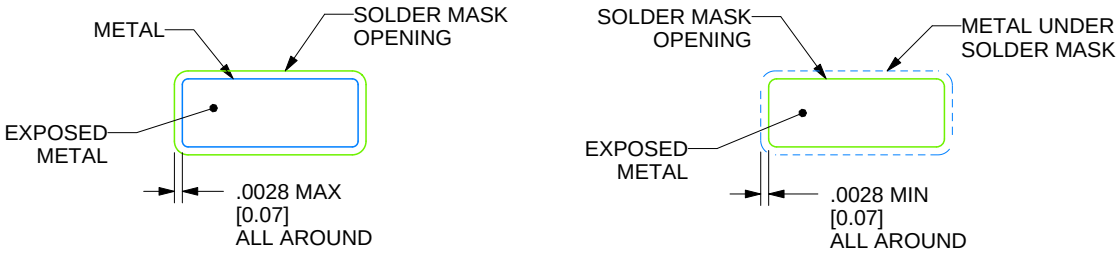


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

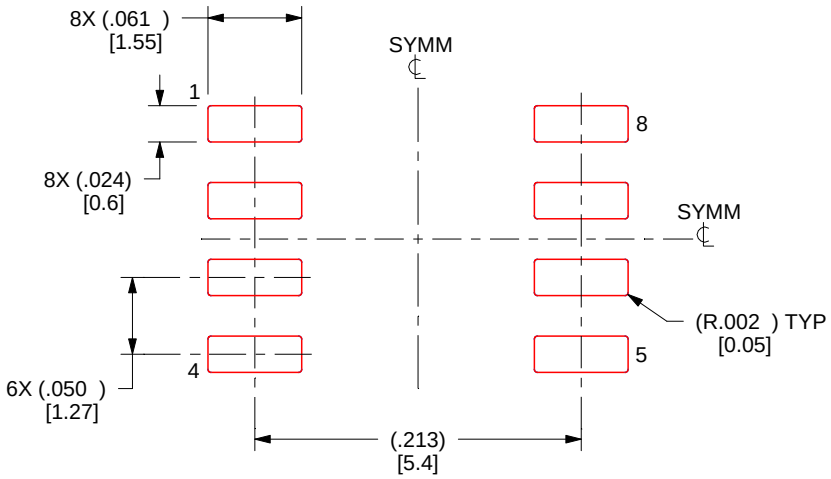
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

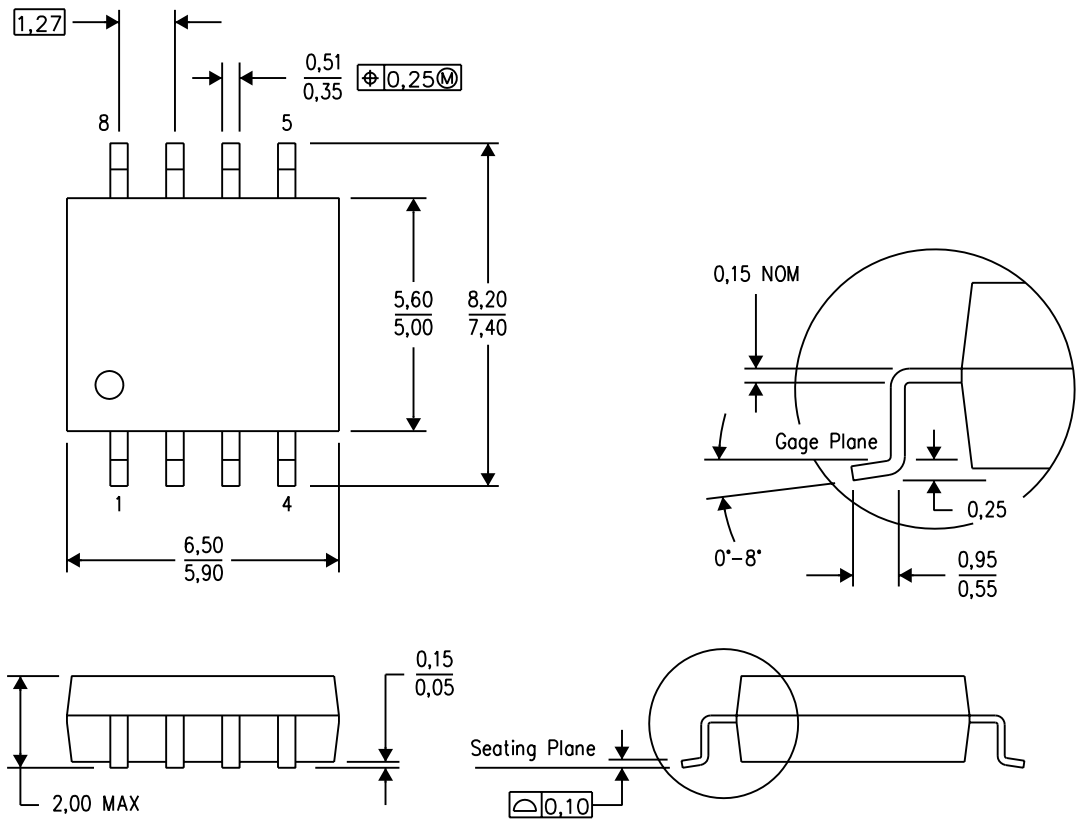
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

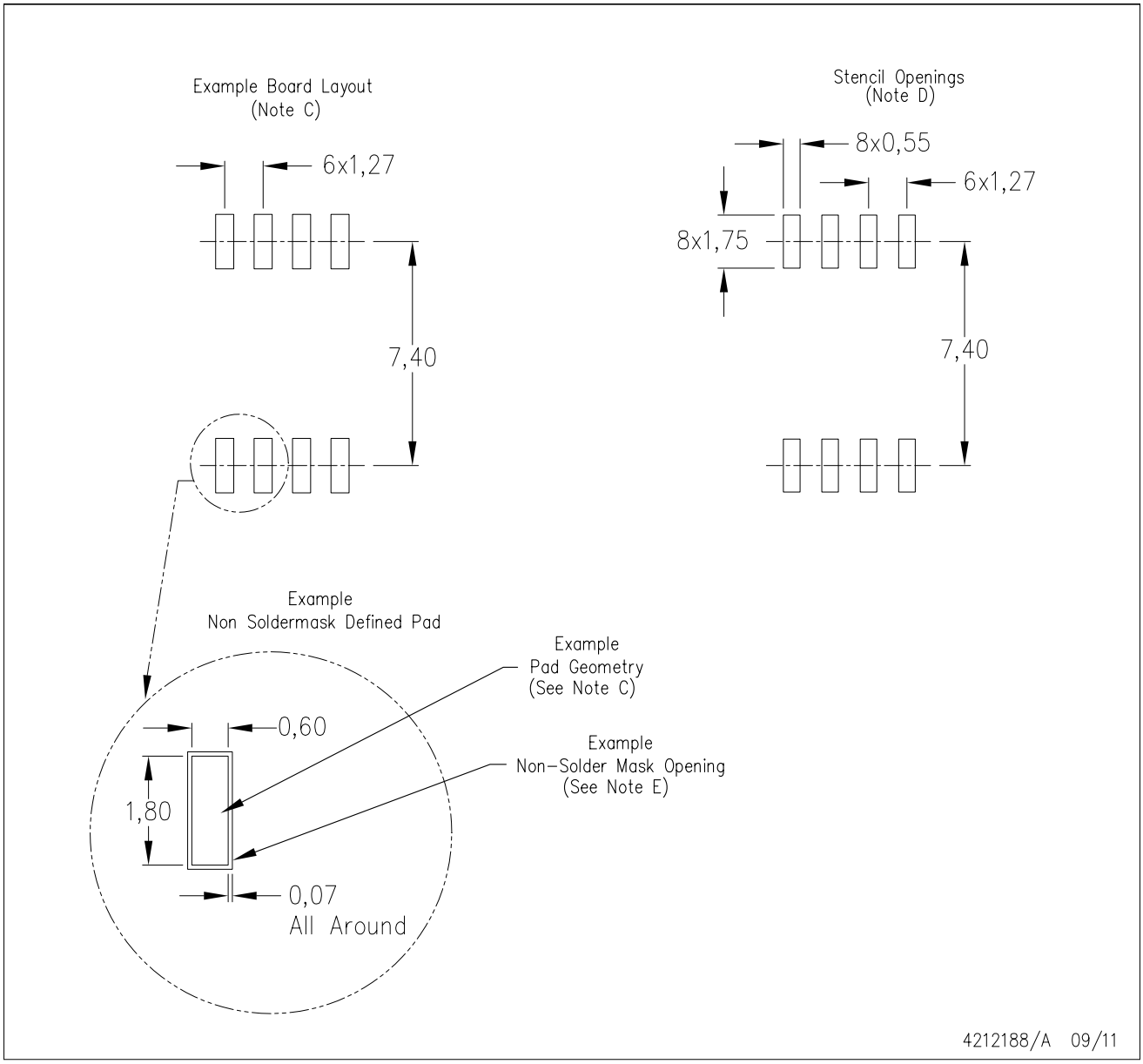
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

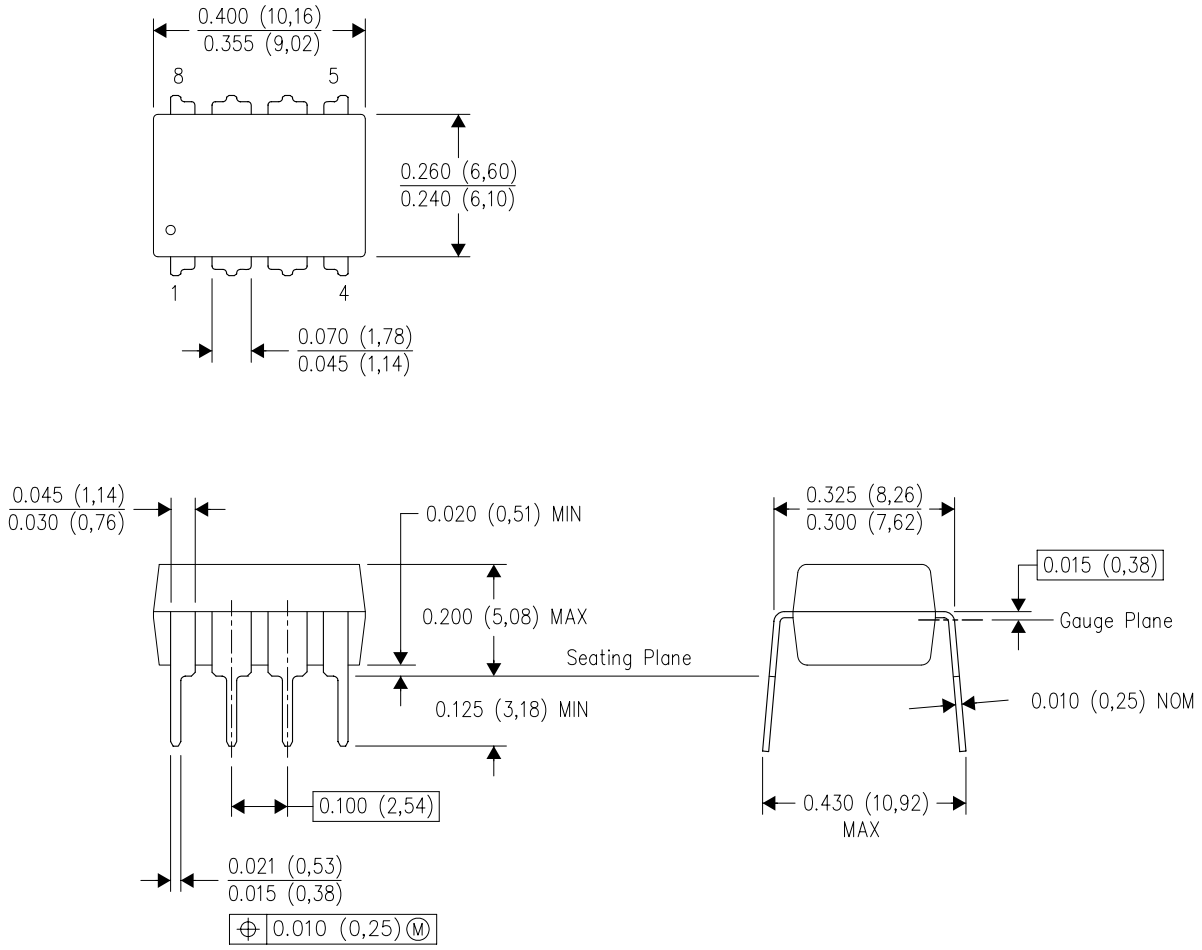
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

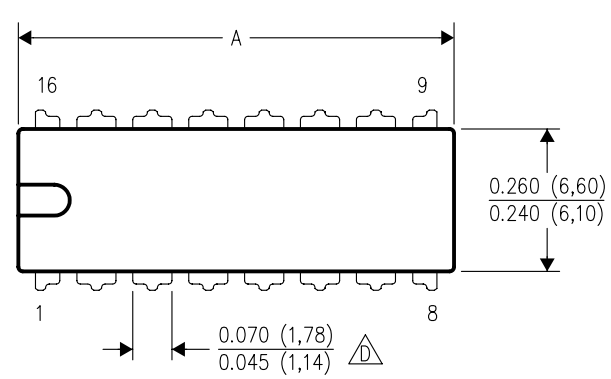


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

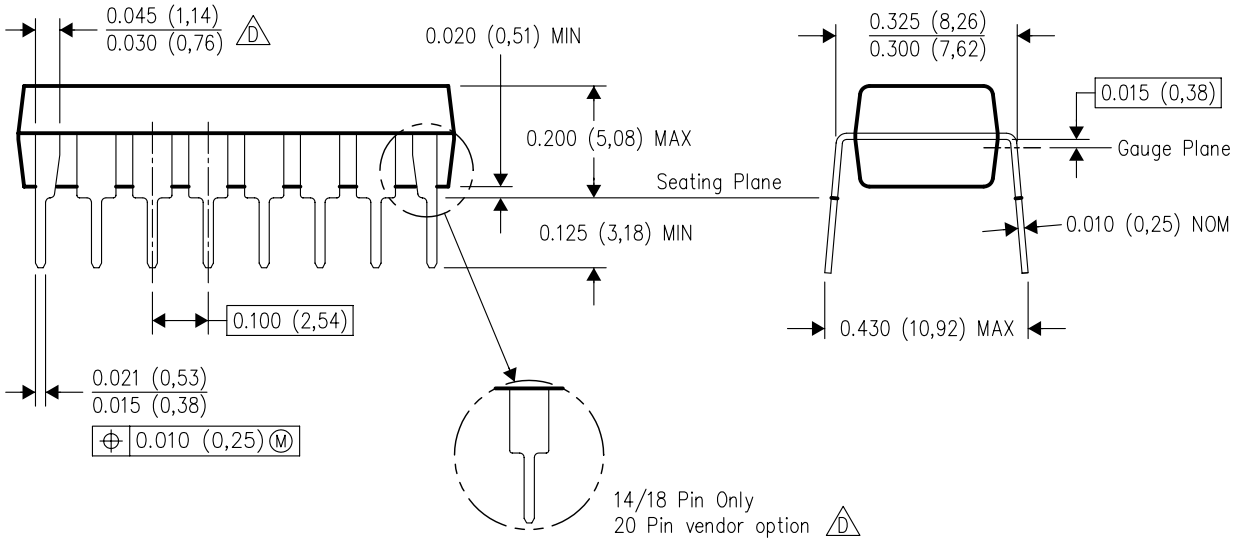
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

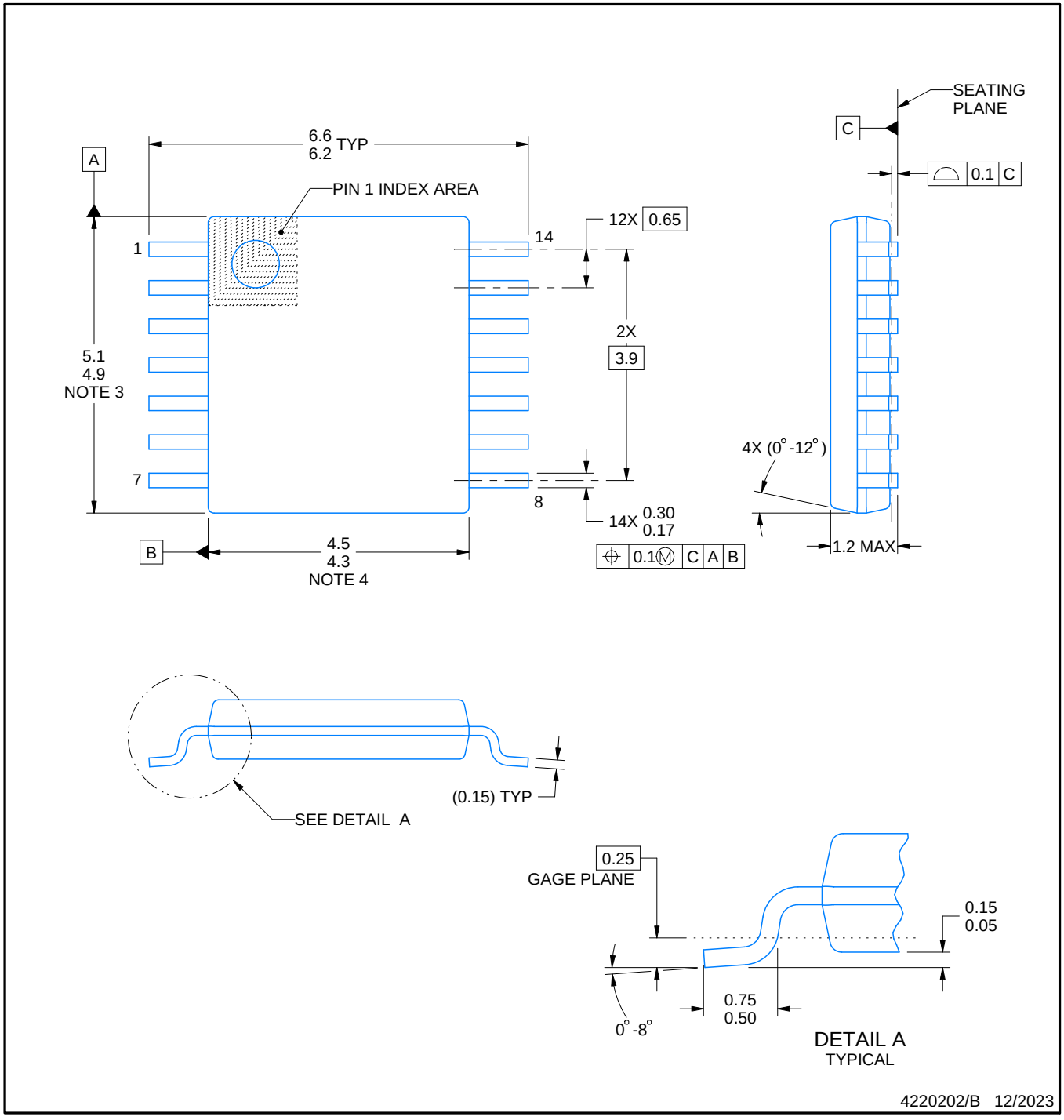
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

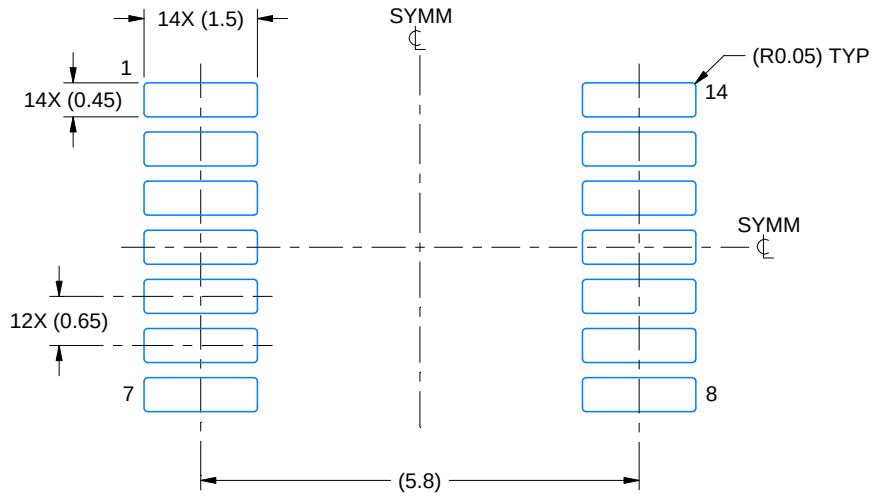
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

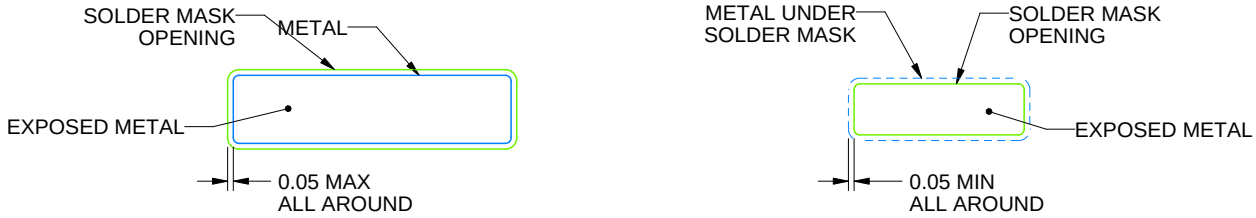


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

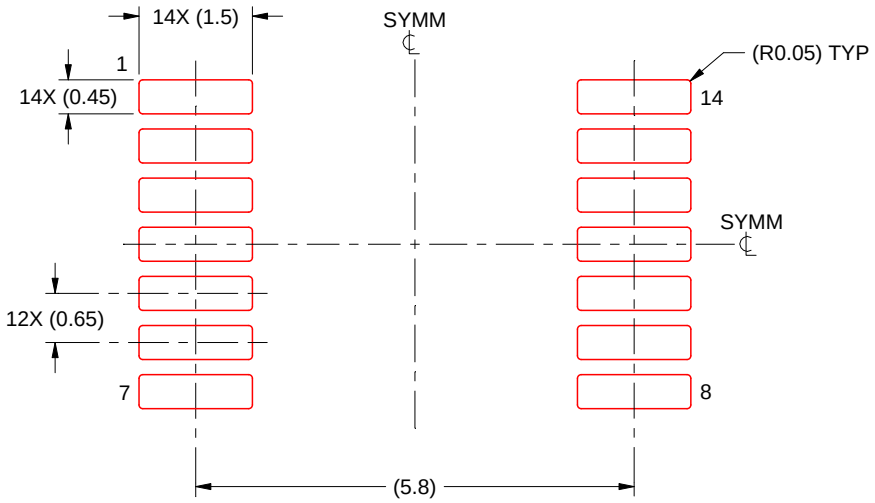


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

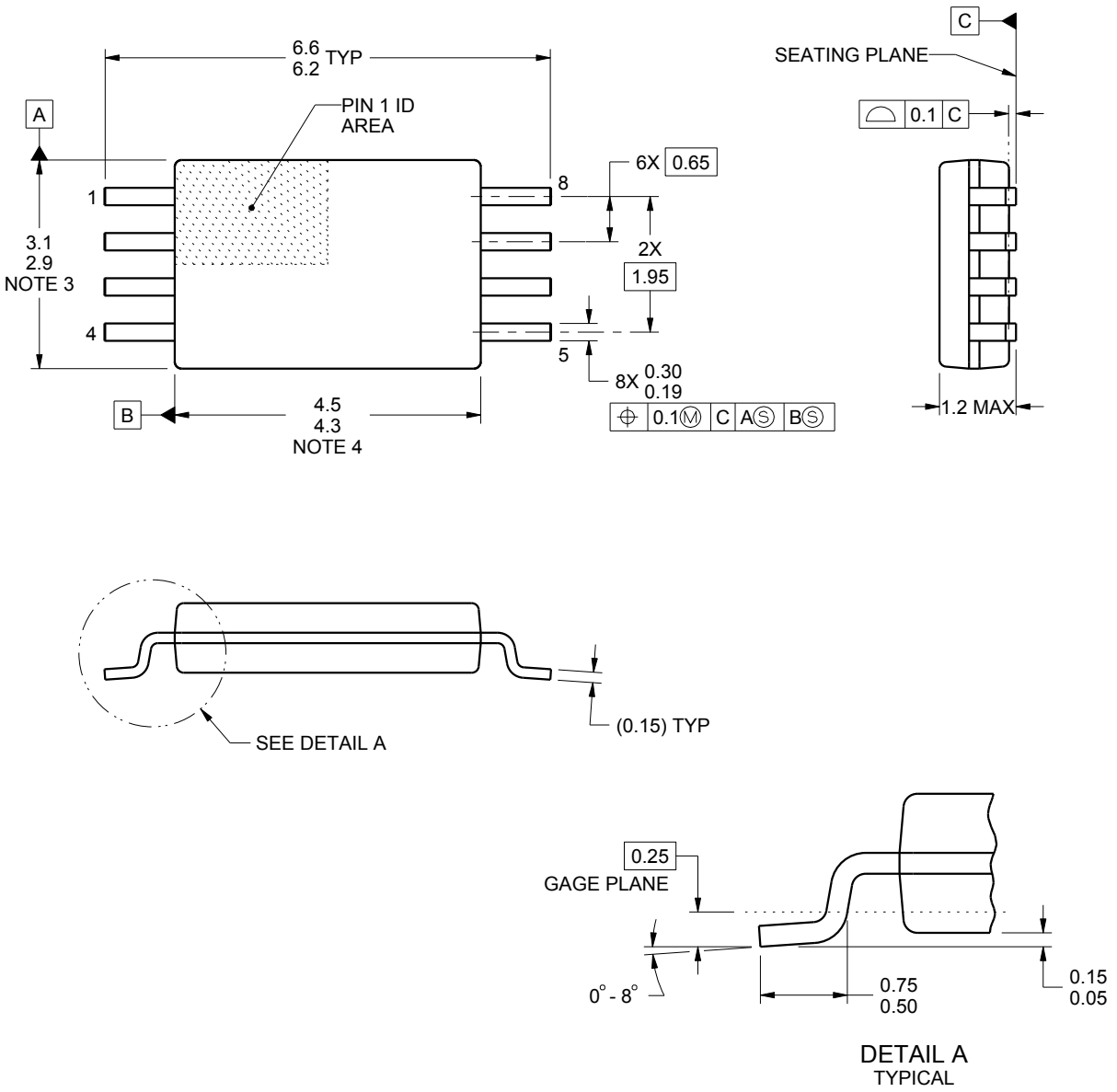
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

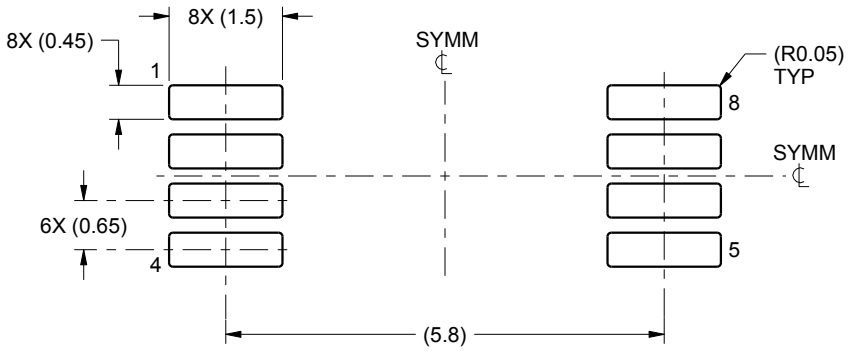
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

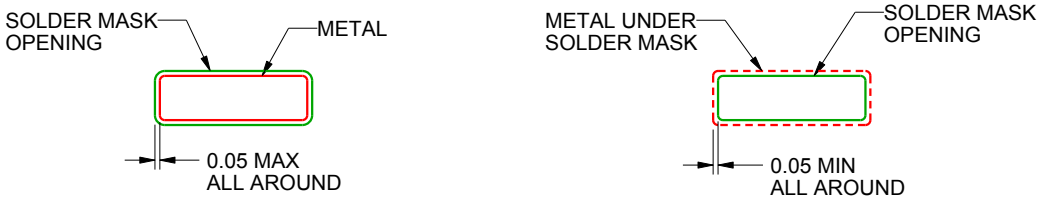


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

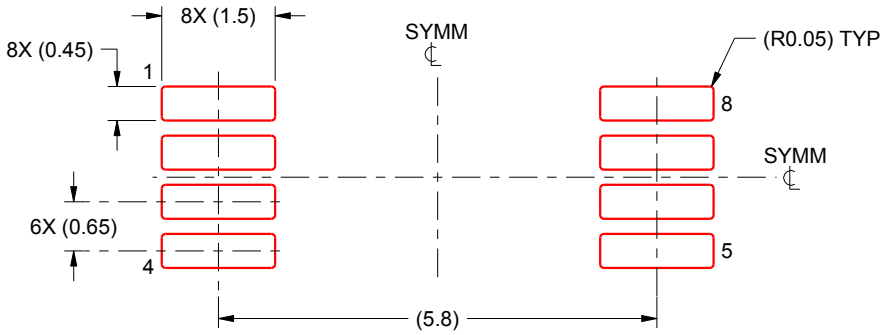


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

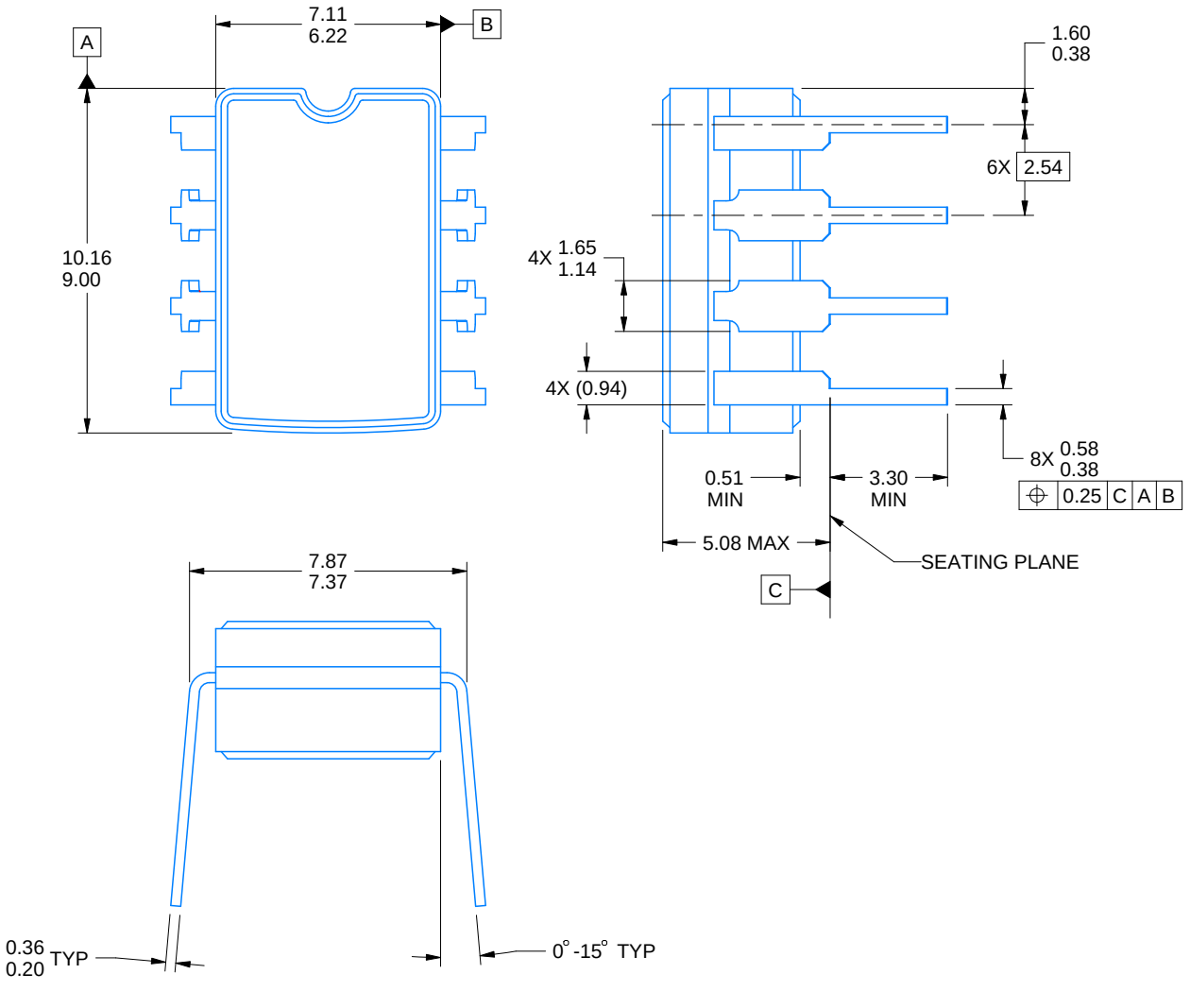
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

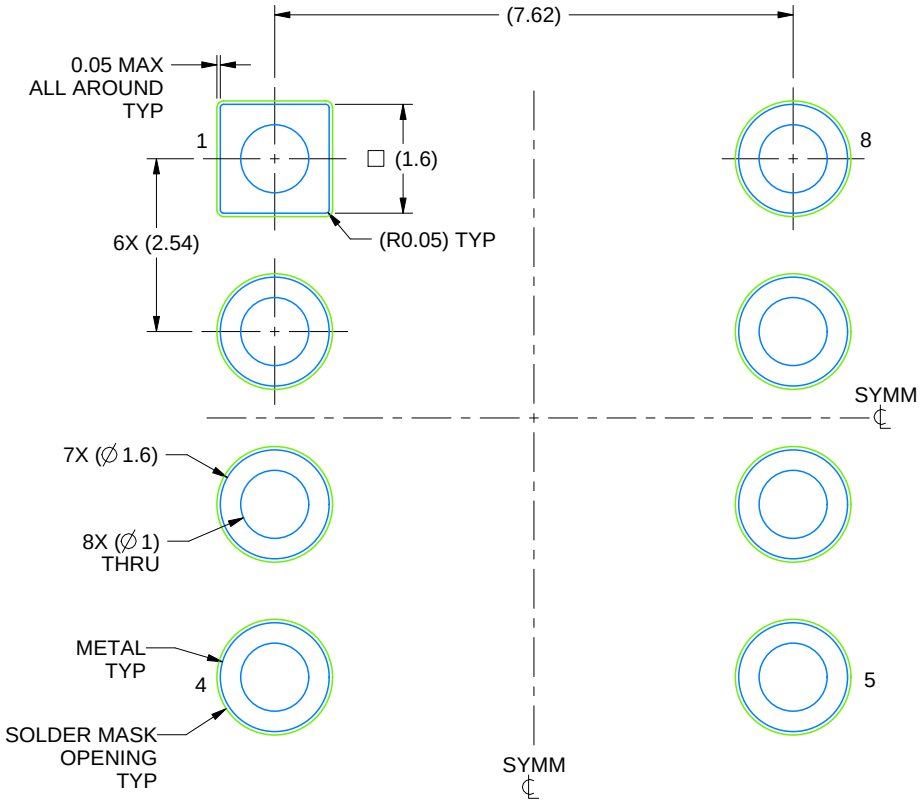
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

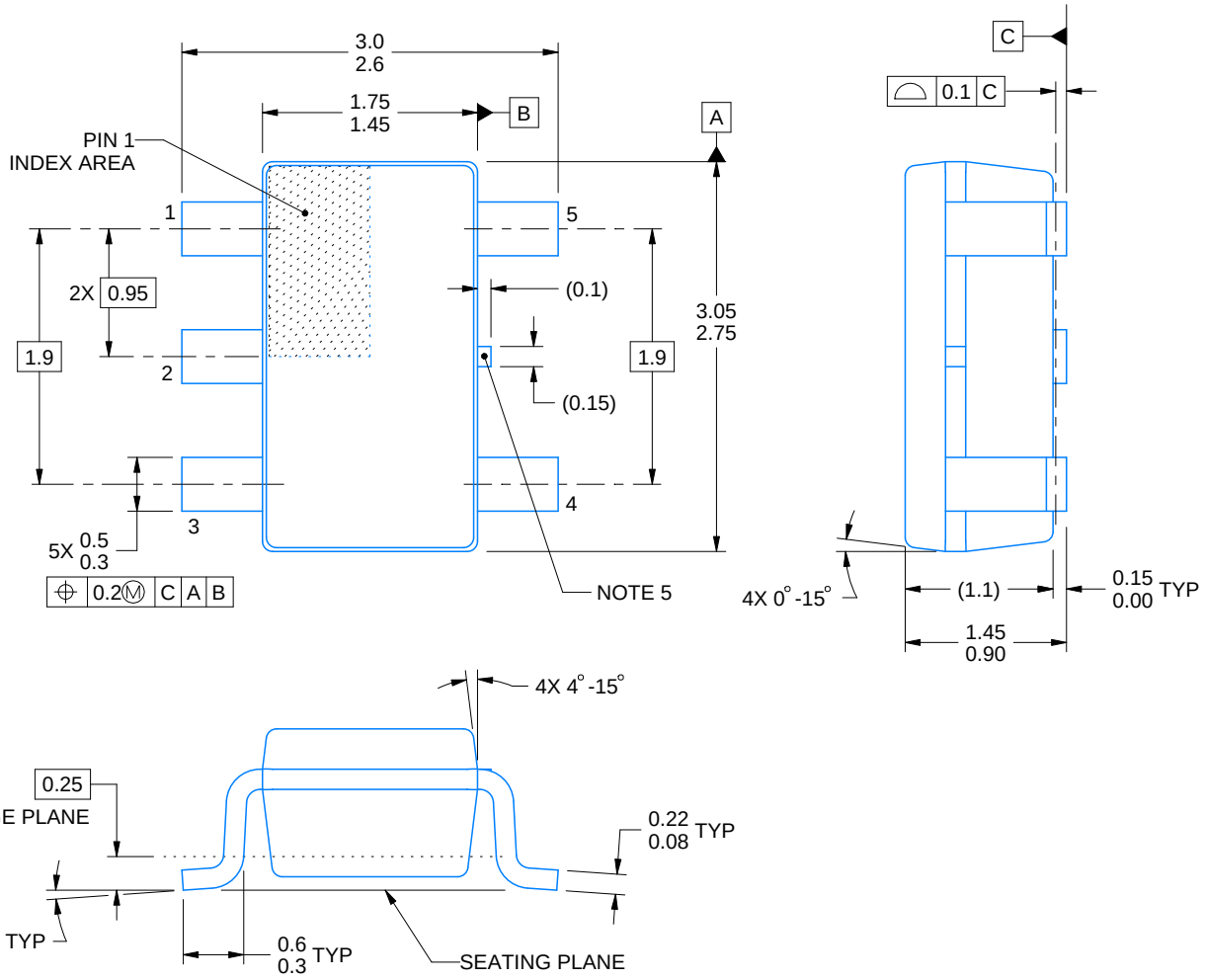
4230036/A 09/2023

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

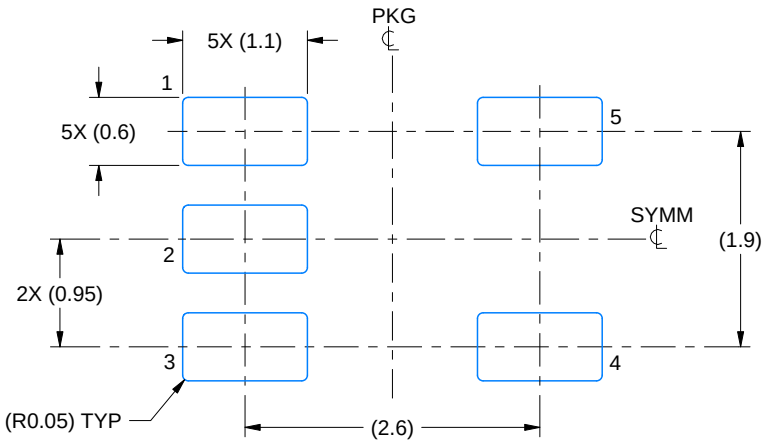
SMALL OUTLINE TRANSISTOR



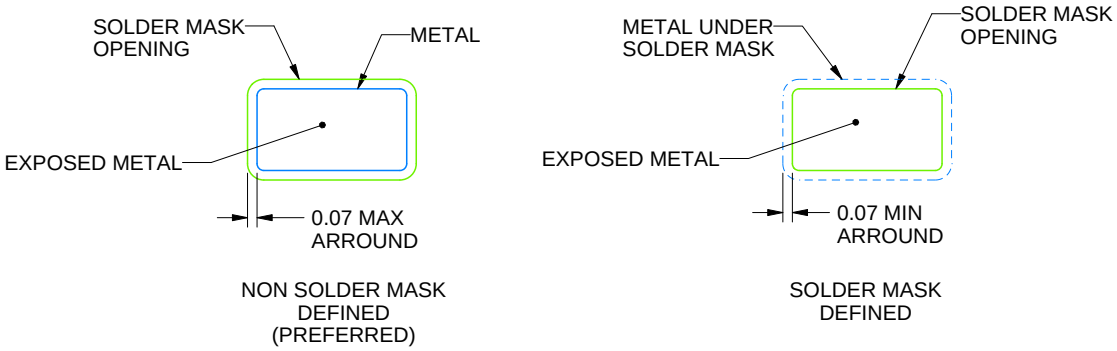
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

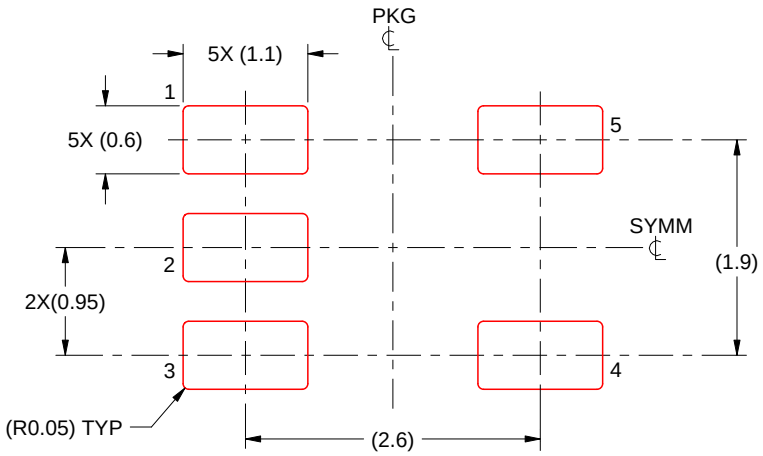


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

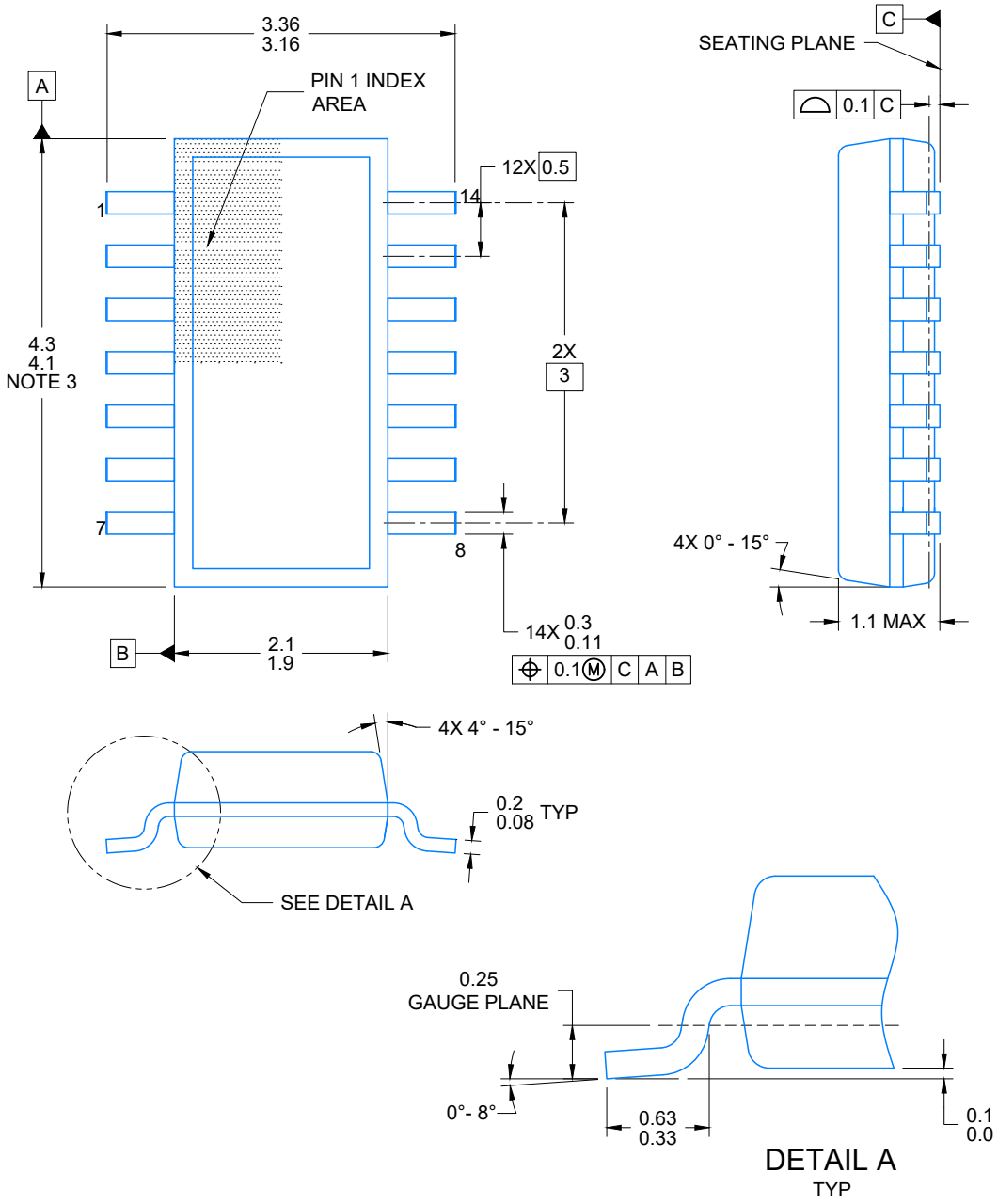
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

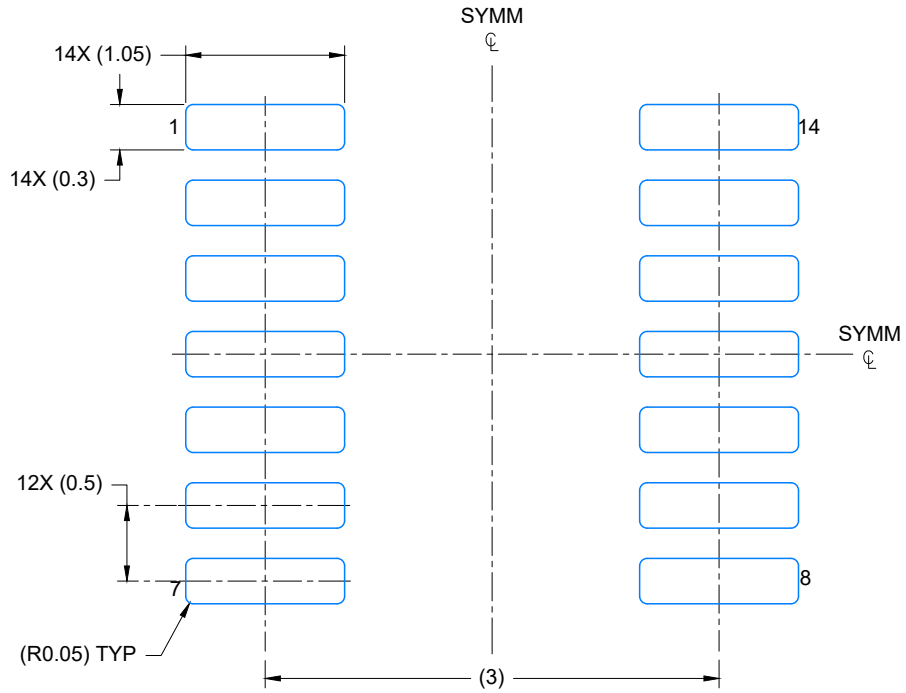
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

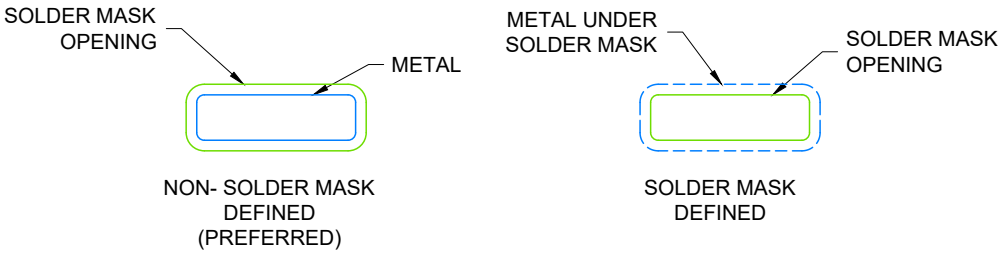


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

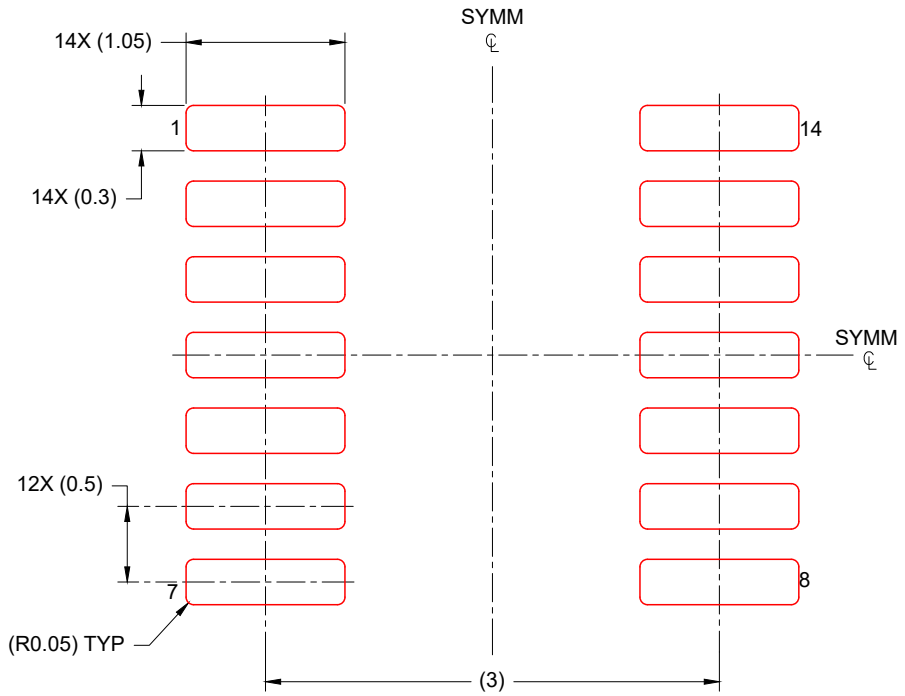


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

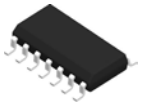


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

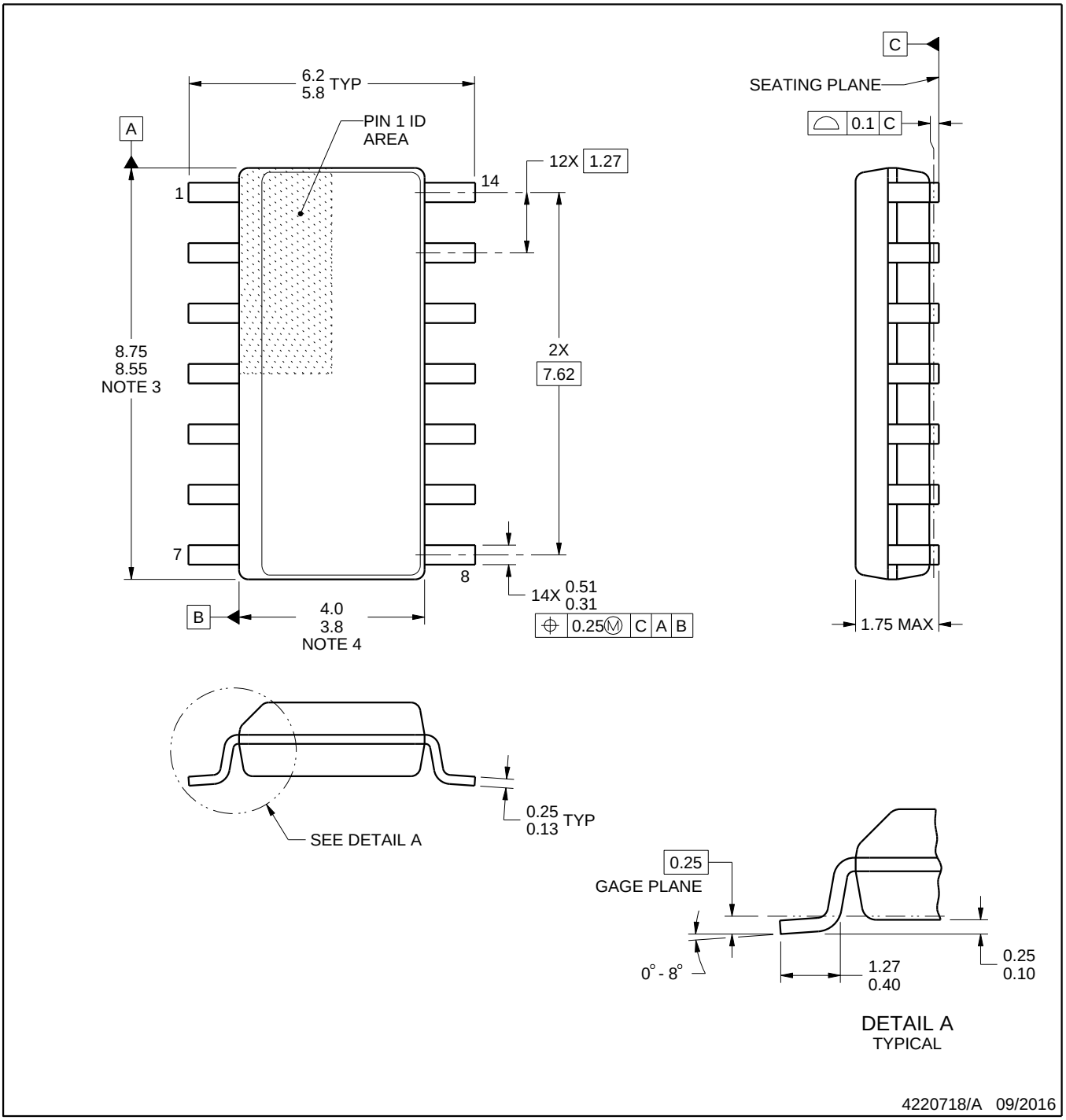


PACKAGE OUTLINE

D0014A

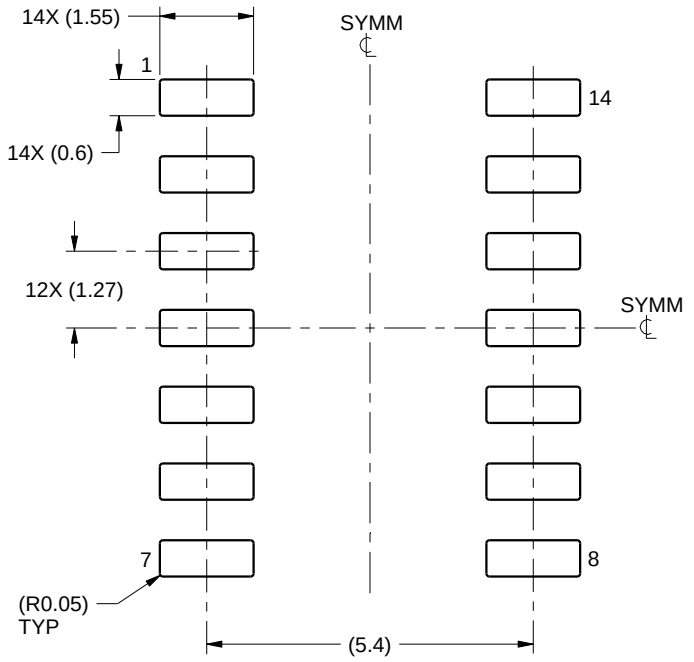
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

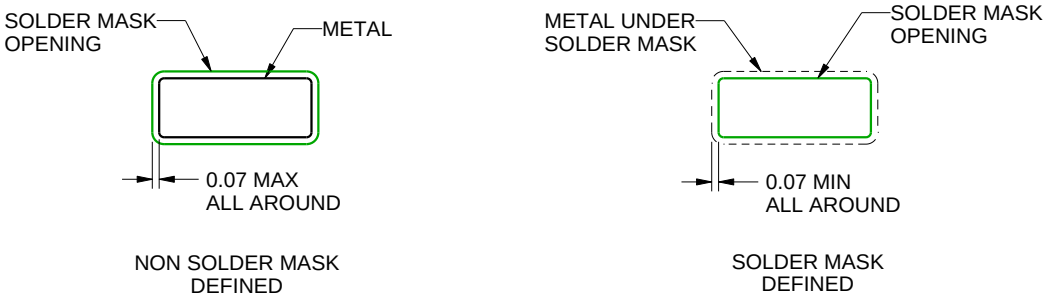


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

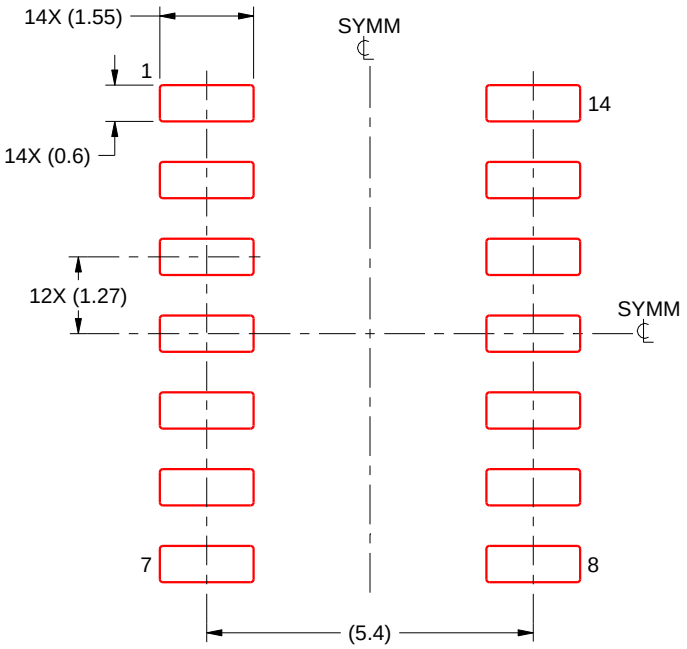
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

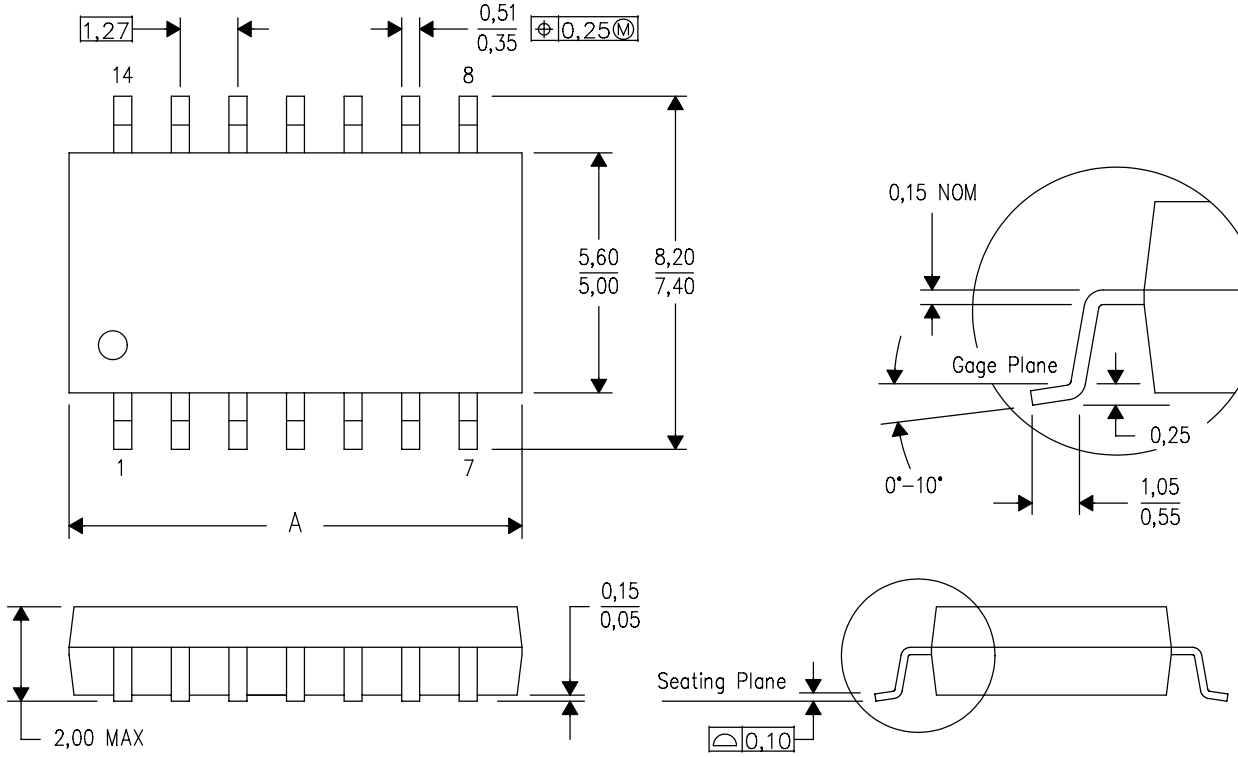
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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