

## LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIER

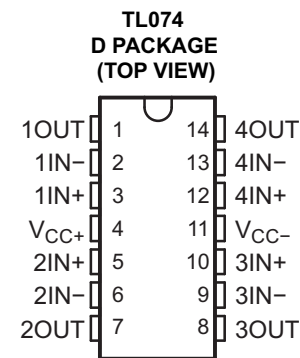
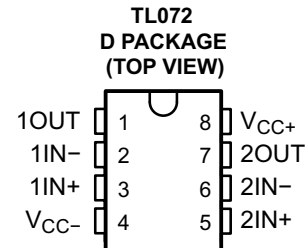
Check for Samples: [TL072-EP](#), [TL074-EP](#)

### FEATURES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typ
- Low Noise  
 $V_n = 18 \text{ nV}/\sqrt{\text{Hz}}$  Typ at  $f = 1 \text{ kHz}$
- High Input Impedance: JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate: 13 V/ $\mu\text{s}$  Typ
- Common-Mode Input Voltage Range Includes  $V_{CC+}$

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Extended ( $-40^\circ\text{C}$  to  $125^\circ\text{C}$ ) or Military ( $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



### DESCRIPTION/ORDERING INFORMATION

The JFET-input operational amplifiers in the TL07x is similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The TL07x is characterized for operation over the extended temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  or military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

### ORDERING INFORMATION<sup>(1)</sup>

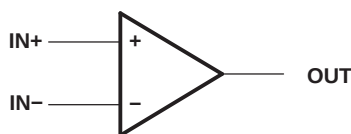
| $T_A$                                      | $V_{IO\text{mA}X}$<br>AT $25^\circ\text{C}$ | PACKAGE  |              | ORDERABLE<br>PART NUMBER | TOP-SIDE<br>MARKING | VID NUMBER       |
|--------------------------------------------|---------------------------------------------|----------|--------------|--------------------------|---------------------|------------------|
| $-40^\circ\text{C}$ to $125^\circ\text{C}$ | 6 mV                                        | SOIC – D | Reel of 2500 | TL072QDREP               | TL072Q              | V62/12604-01XE   |
|                                            |                                             |          |              | TL074QDREP               | TL074Q              | V62/11621-01XE   |
| $-55^\circ\text{C}$ to $125^\circ\text{C}$ | 6 mV                                        | SOIC – D | Reel of 2500 | TL074MDREP               | TL074M              | V62/11621-02XE   |
|                                            |                                             |          | Tube of 75   | TL074MDEP                | TL074M              | V62/11621-02XE-T |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](#).

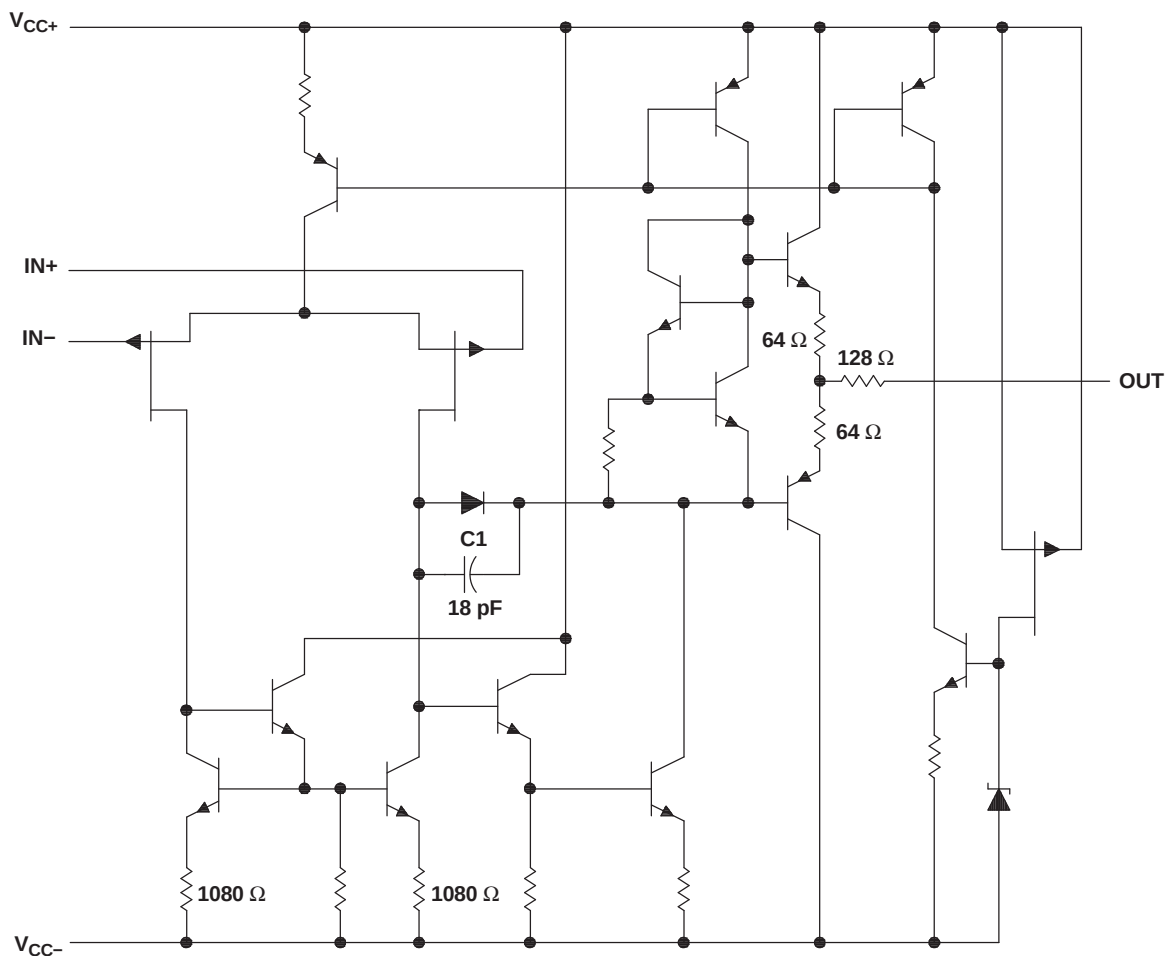


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## TL072 and TL074 SYMBOL (EACH AMPLIFIER)



## SCHEMATIC (EACH AMPLIFIER)



All component values shown are nominal.

| COMPONENT COUNT <sup>(1)</sup> |       |       |
|--------------------------------|-------|-------|
| COMPONENT TYPE                 | TL072 | TL074 |
| Resistors                      | 22    | 44    |
| Transistors                    | 28    | 56    |
| JFET                           | 4     | 6     |
| Diodes                         | 2     | 4     |
| Capacitors                     | 2     | 4     |
| epi-FET                        | 2     | 4     |

(1) Includes bias and trim circuitry

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |                                                            | MIN   | MAX       | UNIT |
|------------------|------------------------------------------------------------|-------|-----------|------|
| V <sub>CC+</sub> | Supply voltage <sup>(2)</sup>                              |       | 18        | V    |
| V <sub>CC-</sub> |                                                            |       | 18        |      |
| V <sub>ID</sub>  | Differential input voltage <sup>(3)</sup>                  |       | ±30       | V    |
| V <sub>I</sub>   | Input voltage <sup>(2) (4)</sup>                           |       | ±15       | V    |
|                  | Duration of output short circuit <sup>(5)</sup>            |       | Unlimited |      |
| $\theta_{JA}$    | Thermal resistance, junction-to-ambient <sup>(6) (7)</sup> | TL072 | 97.5      | °C/W |
|                  |                                                            | TL074 | 86        |      |
| $\theta_{JC}$    | Thermal resistance, junction-to-case <sup>(7)</sup>        | TL072 | 38.3      | °C/W |
|                  |                                                            | TL074 | 51.5      |      |
| T <sub>J</sub>   | Operating virtual junction temperature                     |       | 150       | °C   |
| T <sub>stg</sub> | Storage temperature range                                  | -65   | 150       | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
- (3) Differential voltages are at IN+, with respect to IN-.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
- (6) Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

## ELECTRICAL CHARACTERISTICS

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

| PARAMETER                        |                                                                       | TEST CONDITIONS <sup>(1)</sup>                                                       | T <sub>A</sub> <sup>(2)</sup> | TL072            |           |     | TL074            |           |       | UNIT |
|----------------------------------|-----------------------------------------------------------------------|--------------------------------------------------------------------------------------|-------------------------------|------------------|-----------|-----|------------------|-----------|-------|------|
|                                  |                                                                       |                                                                                      |                               | MIN              | TYP       | MAX | MIN              | TYP       | MAX   |      |
| V <sub>IO</sub>                  | Input offset voltage                                                  | V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω                                            | 25°C                          | 3                |           | 6   | 3                |           | 6     | mV   |
|                                  |                                                                       |                                                                                      | Full range                    | 8                |           |     | 8                |           |       |      |
| α <sub>VIO</sub>                 | Temperature coefficient of input offset voltage                       | V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω                                            | Full range                    | 18               |           |     | 18               |           | μV/°C |      |
| I <sub>IO</sub>                  | Input offset current                                                  | V <sub>O</sub> = 0                                                                   | 25°C                          | 5                | 100       |     | 5                | 100       |       | pA   |
|                                  |                                                                       |                                                                                      | 125°C                         | 2                |           |     | 2                |           | nA    |      |
| I <sub>IB</sub>                  | Input bias current                                                    | V <sub>O</sub> = 0                                                                   | 25°C                          | 65               | 200       |     | 65               | 200       |       | pA   |
|                                  |                                                                       |                                                                                      | 125°C                         | 20               |           |     | 20               |           | nA    |      |
| V <sub>ICR</sub>                 | Common-mode input voltage range                                       |                                                                                      | 25°C                          | ±11              | –12 to 15 |     | ±11              | –12 to 15 |       | V    |
| V <sub>OM</sub>                  | Maximum peak output voltage swing                                     | R <sub>L</sub> = 10 kΩ                                                               | 25°C                          | ±12              | ±13.5     |     | ±12              | ±13.5     |       | V    |
|                                  |                                                                       | R <sub>L</sub> ≥ 10 kΩ                                                               | Full range                    | ±12              |           |     | ±12              |           |       |      |
|                                  |                                                                       | R <sub>L</sub> ≥ 2 kΩ                                                                |                               | ±10              |           |     | ±10              |           |       |      |
| A <sub>VD</sub>                  | Large-signal differential voltage amplification                       | V <sub>O</sub> = ±10 V, R <sub>L</sub> ≥ 2 kΩ                                        | 25°C                          | 35               | 200       |     | 35               | 200       |       | V/mV |
|                                  |                                                                       |                                                                                      | Full range                    | 15               |           |     | 15               |           |       |      |
| B <sub>1</sub>                   | Unity-gain bandwidth                                                  |                                                                                      | 25°C                          | 3                |           |     | 3                |           |       | MHz  |
| r <sub>i</sub>                   | Input resistance                                                      |                                                                                      | 25°C                          | 10 <sup>12</sup> |           |     | 10 <sup>12</sup> |           |       | Ω    |
| CMRR                             | Common-mode rejection ratio                                           | V <sub>IC</sub> = V <sub>ICRmin</sub> ,<br>V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω | 25°C                          | 80               | 86        |     | 80               | 86        |       | dB   |
| k <sub>SVR</sub>                 | Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> ) | V <sub>CC</sub> = ±9 V to ±15 V,<br>V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω        | 25°C                          | 80               | 86        |     | 80               | 86        |       | dB   |
| I <sub>CC</sub>                  | Supply current (each amplifier)                                       | V <sub>O</sub> = 0, No load                                                          | 25°C                          | 1.4              | 2.5       |     | 1.4              | 2.5       |       | mA   |
| V <sub>O1</sub> /V <sub>O2</sub> | Crosstalk attenuation                                                 | A <sub>VD</sub> = 100                                                                | 25°C                          | 120              |           |     | 120              |           |       | dB   |

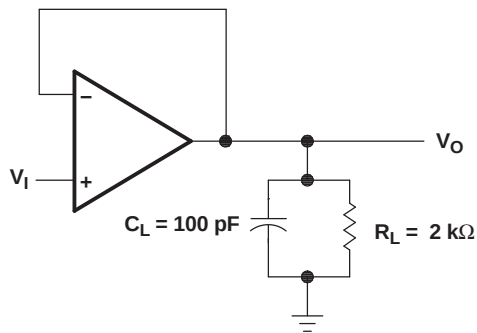
- Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 3](#). Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.
- All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  for TL07xQ and  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for TL07xM.

## OPERATING CHARACTERISTICS

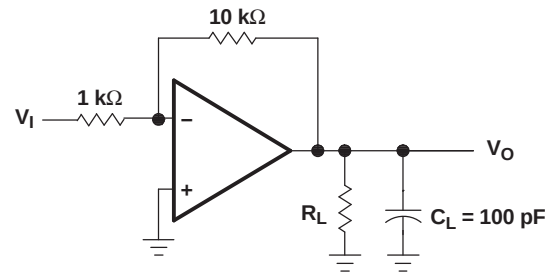
 $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

| PARAMETER | TEST CONDITIONS                |                                                                                                                                              | TL072 |       |     | TL074 |       |     | UNIT                         |
|-----------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-----|-------|-------|-----|------------------------------|
|           |                                |                                                                                                                                              | MIN   | TYP   | MAX | MIN   | TYP   | MAX |                              |
| SR        | Slew rate at unity gain        | $V_I = 10\text{ V}$ ,<br>$C_L = 100\ \text{pF}$ ,<br>$R_L = 2\ \text{k}\Omega$ ,<br>See <a href="#">Figure 1</a>                             | 8     | 13    |     | 8     | 13    |     | V/ $\mu\text{s}$             |
| $t_r$     | Rise-time overshoot factor     | $V_I = 20\text{ V}$ ,<br>$C_L = 100\ \text{pF}$ ,<br>$R_L = 2\ \text{k}\Omega$ ,<br>See <a href="#">Figure 1</a>                             |       | 0.1   |     |       | 0.1   |     | $\mu\text{s}$                |
|           |                                |                                                                                                                                              |       | 20    |     |       | 20    |     | %                            |
| $V_n$     | Equivalent input noise voltage | $R_S = 20\ \Omega$                                                                                                                           |       | 18    |     |       | 18    |     | $\text{nV}/\sqrt{\text{Hz}}$ |
|           |                                | $f = 10\text{ Hz}$ to $10\text{ kHz}$                                                                                                        |       | 4     |     |       | 4     |     | $\mu\text{V}$                |
| $I_n$     | Equivalent input noise current | $R_S = 20\ \Omega$ ,<br>$f = 1\text{ kHz}$                                                                                                   |       | 0.01  |     |       | 0.01  |     | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD       | Total harmonic distortion      | $V_{I\text{rms}} = 6\text{ V}$ ,<br>$R_L \geq 2\ \text{k}\Omega$ ,<br>$f = 1\text{ kHz}$ ,<br>$A_{VD} = 1$ ,<br>$R_S \leq 1\ \text{k}\Omega$ |       | 0.003 |     |       | 0.003 |     | %                            |

## PARAMETER MEASUREMENT INFORMATION



**Figure 1. Unity-Gain Amplifier**



**Figure 2. Gain-of-10 Inverting Amplifier**

## TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

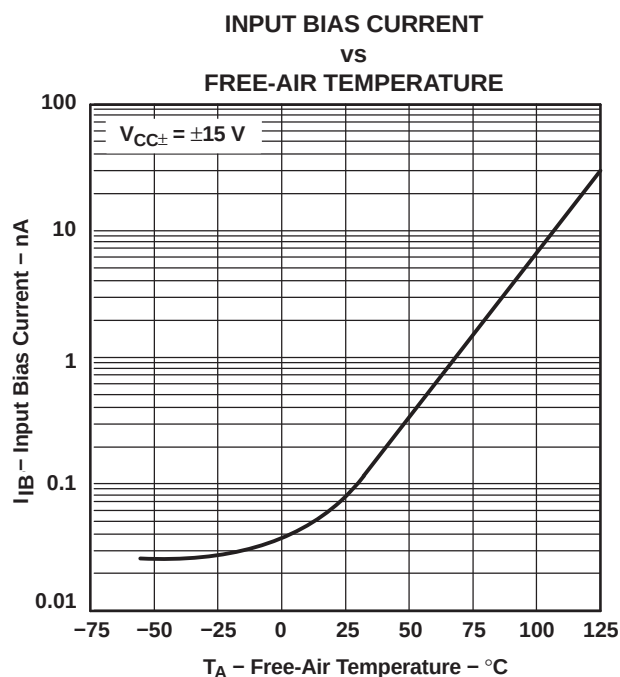


Figure 3.

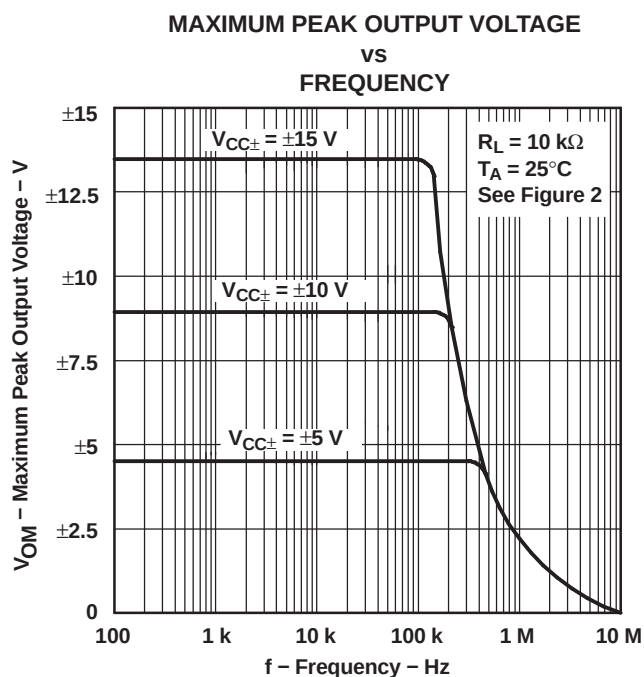


Figure 4.

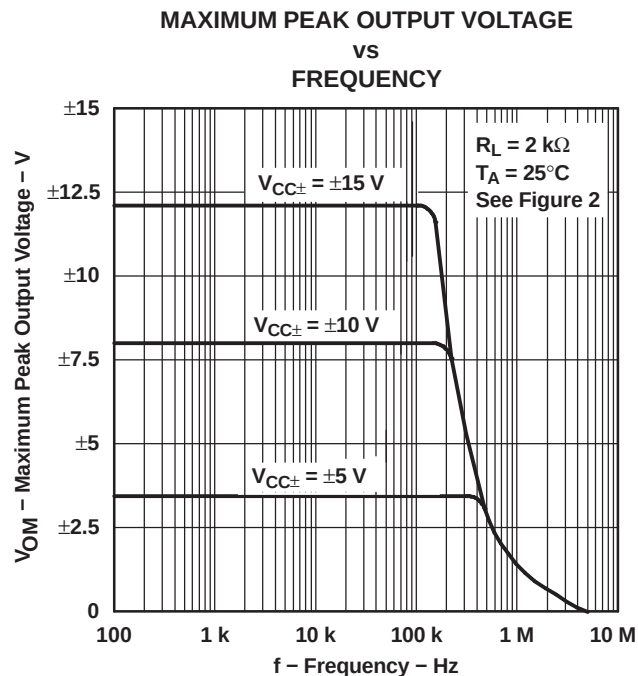


Figure 5.

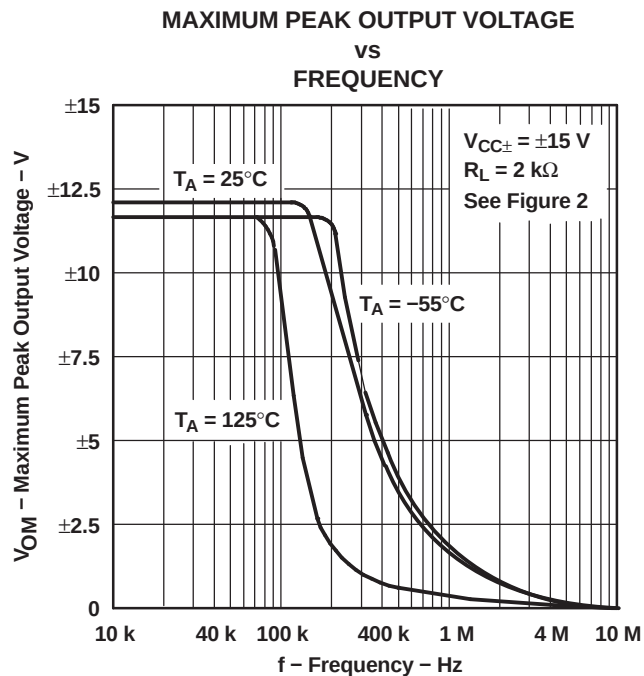
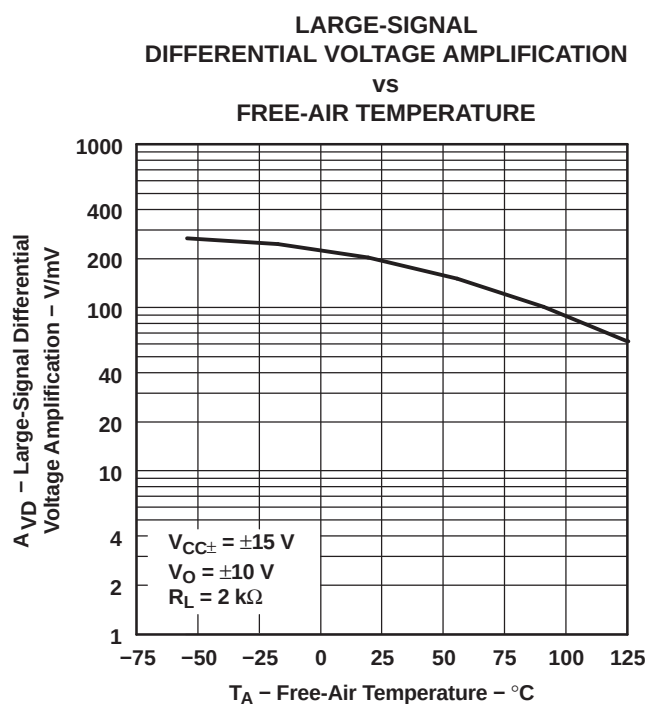
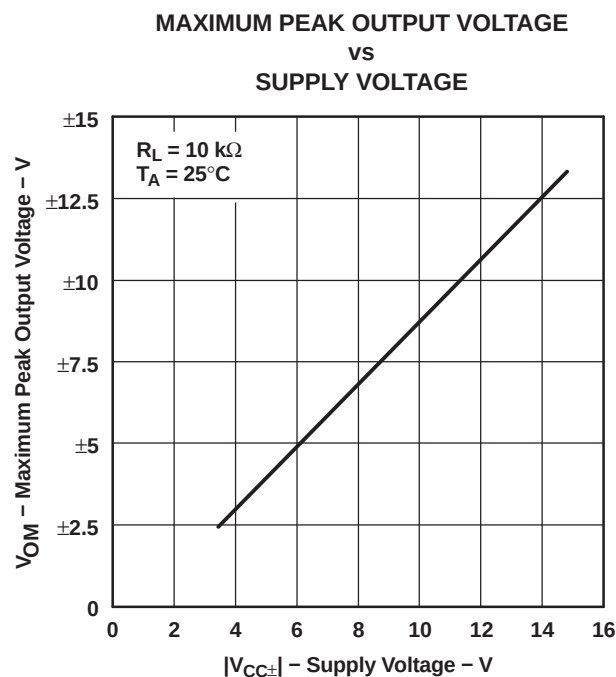
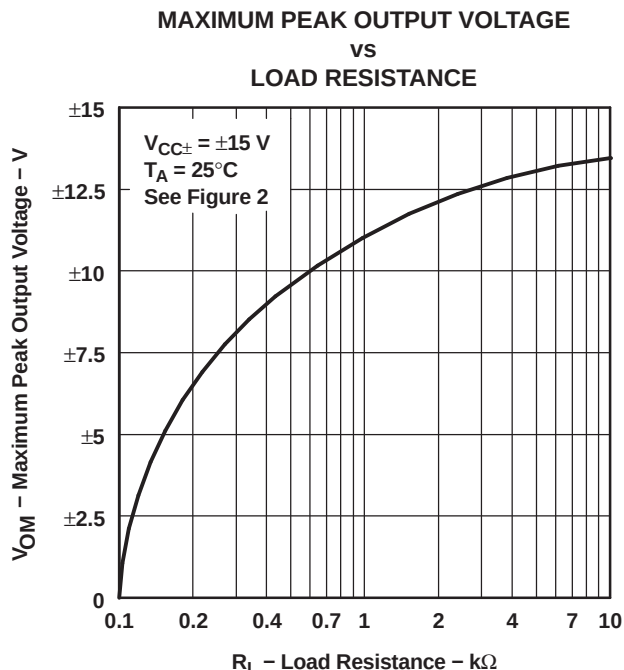
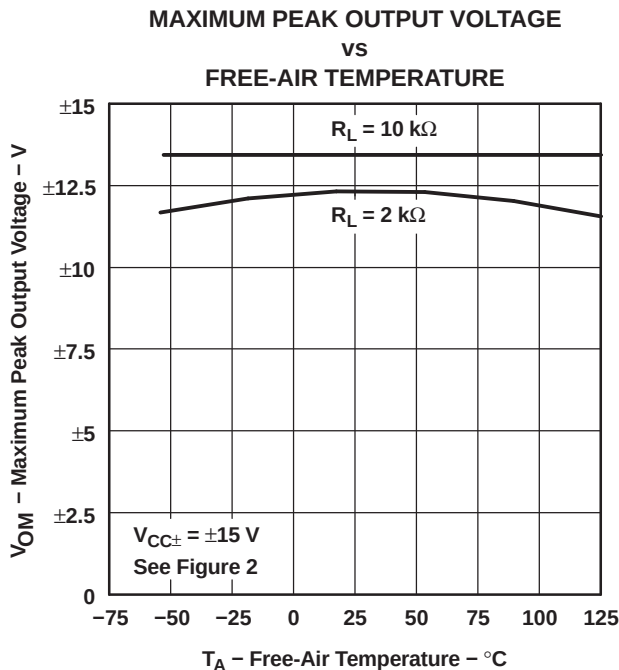


Figure 6.

## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

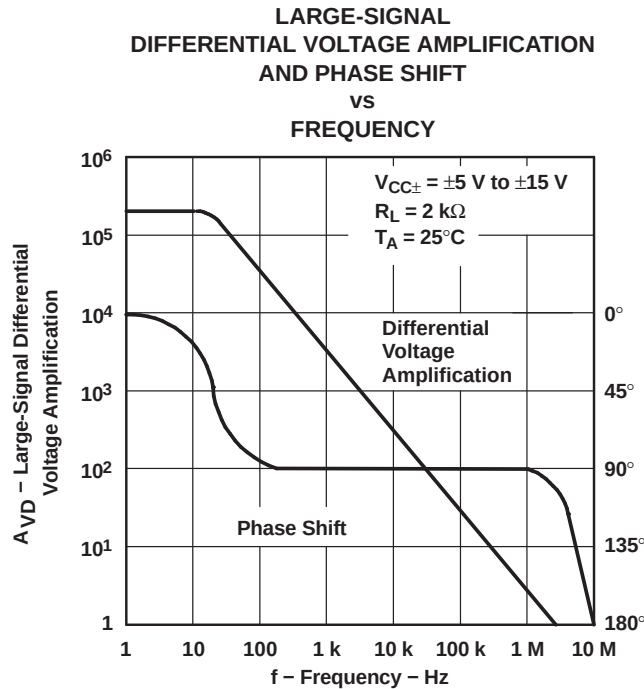


Figure 11.

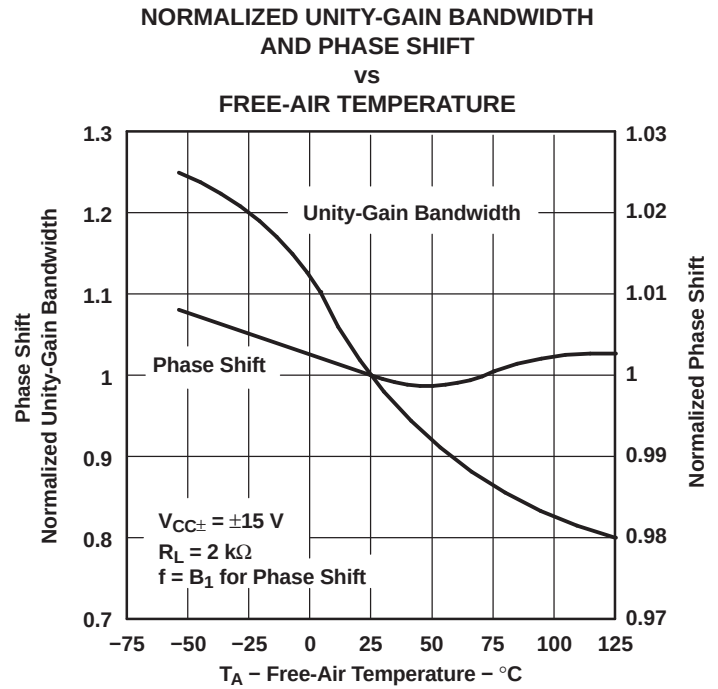


Figure 12.

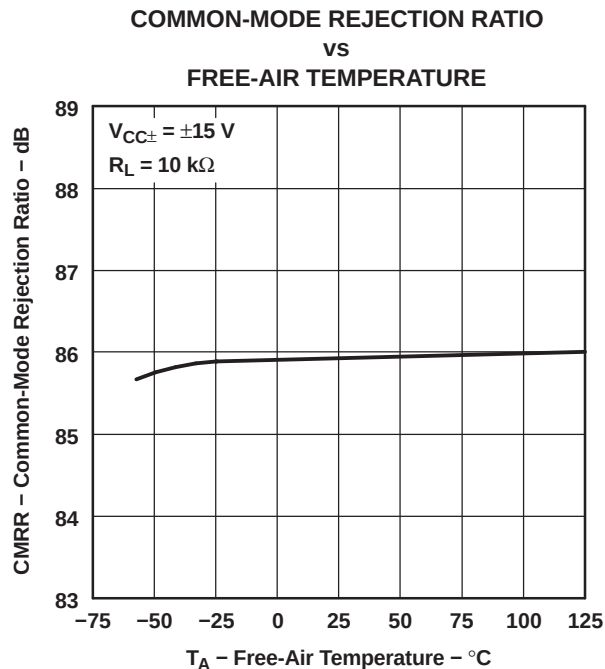


Figure 13.

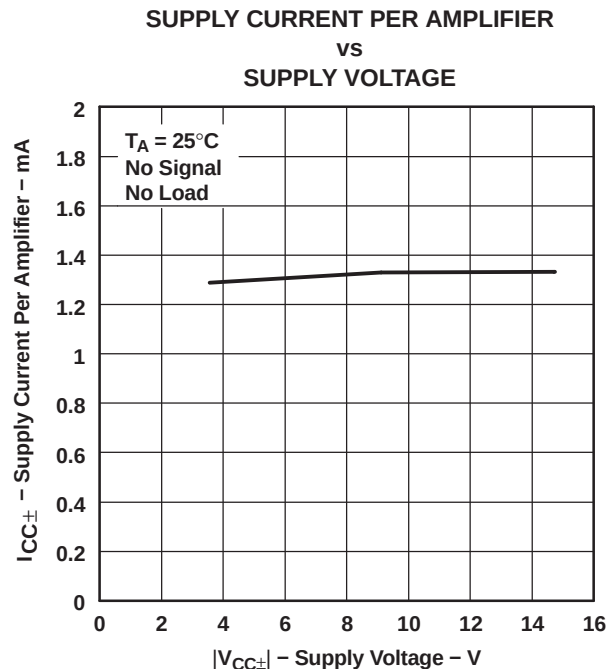


Figure 14.



## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

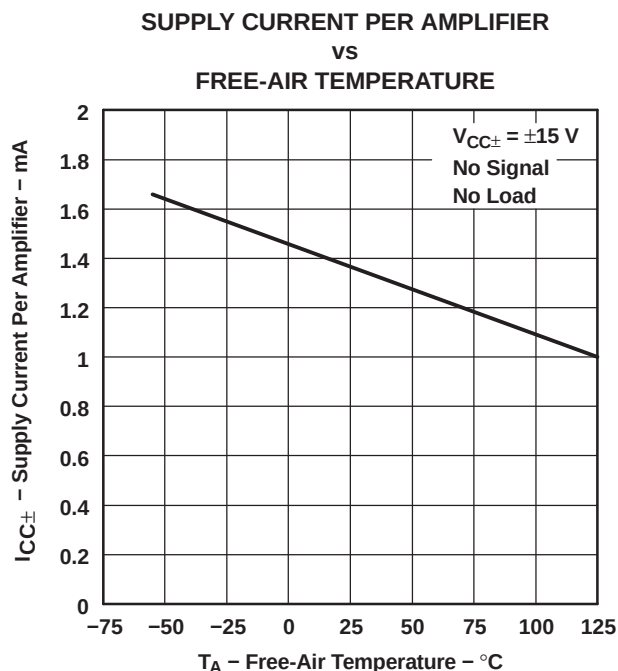


Figure 15.

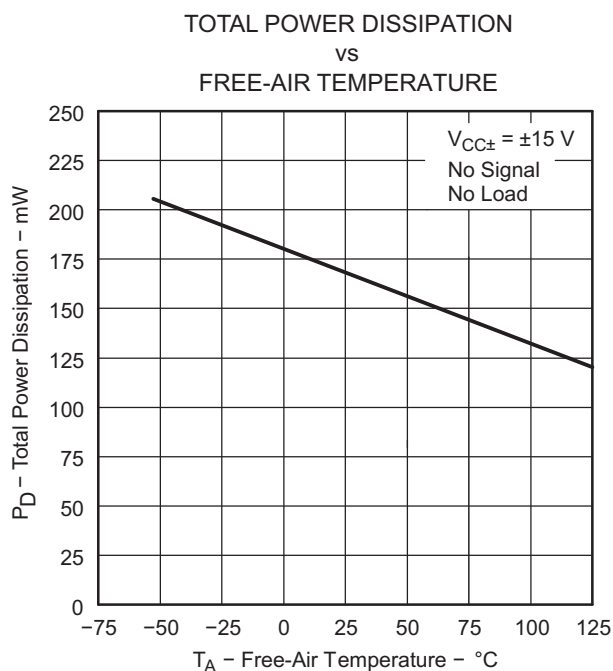


Figure 16.

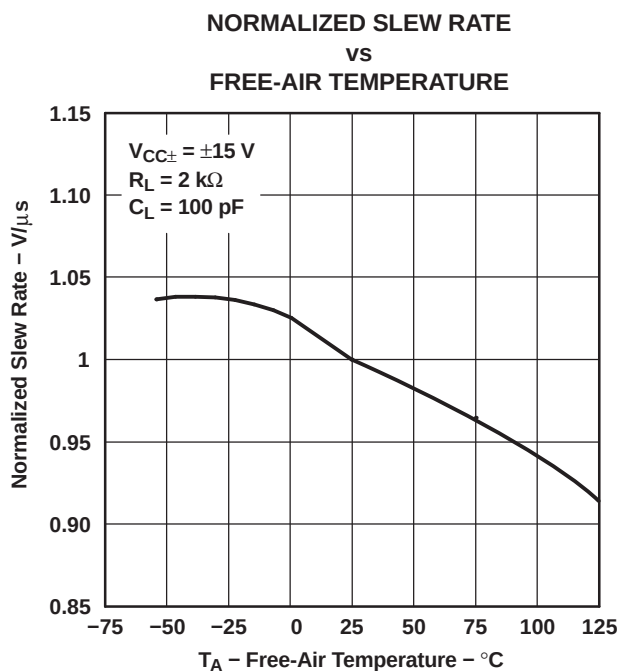


Figure 17.

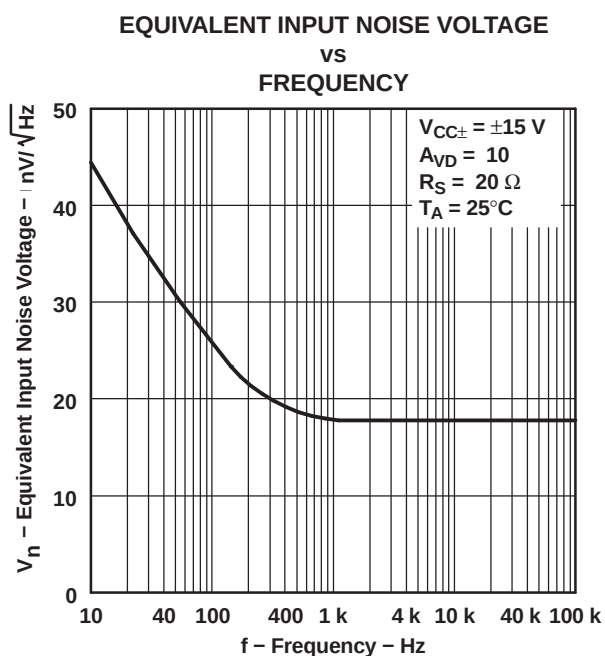


Figure 18.

## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

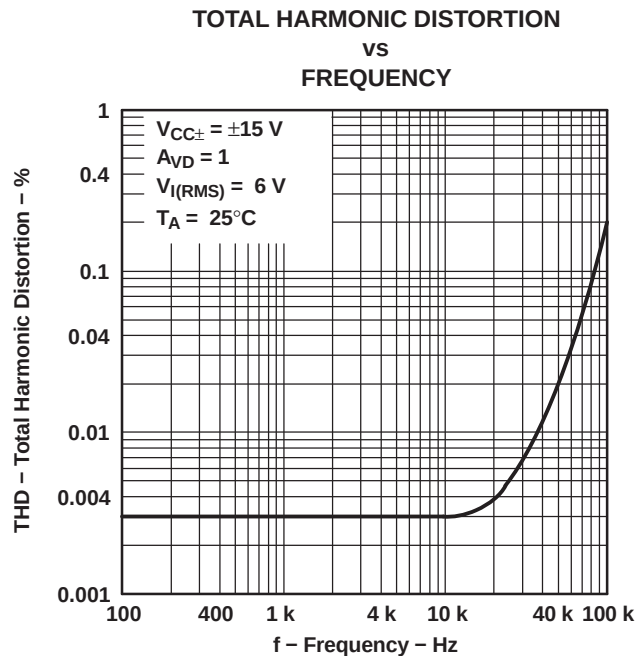


Figure 19.

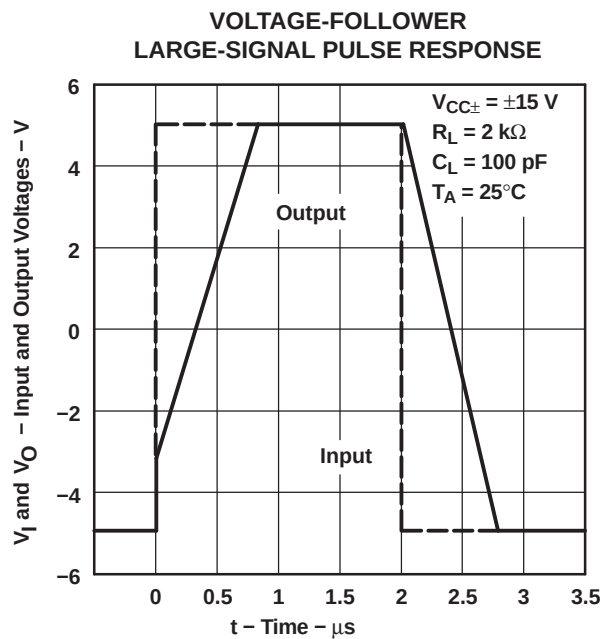


Figure 20.

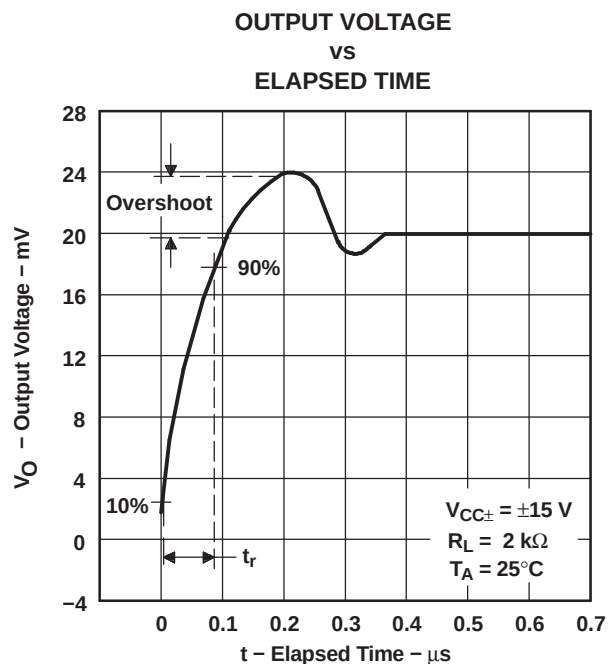
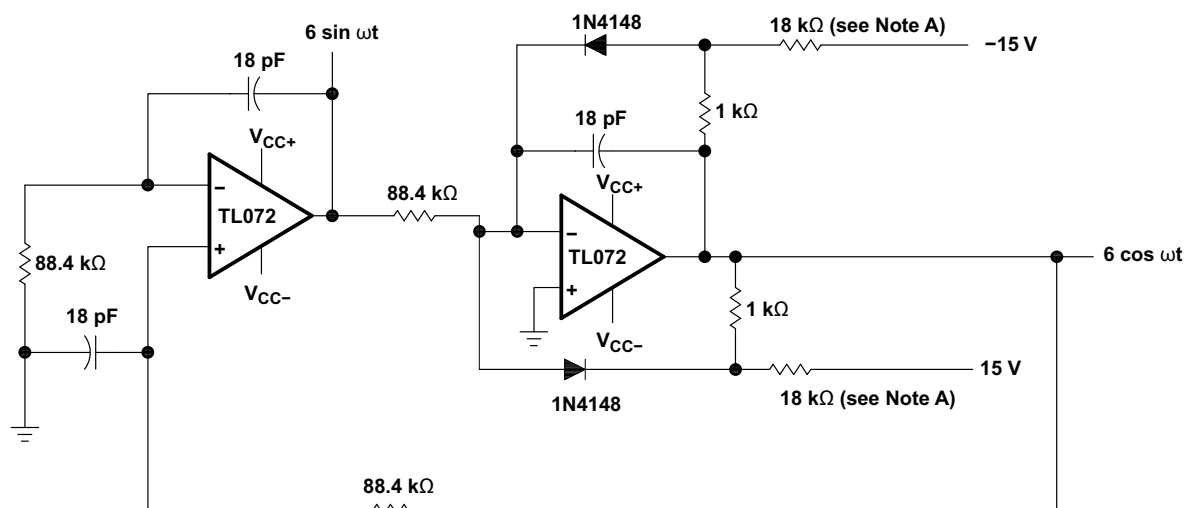


Figure 21.

## APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 22. 100-kHz Quadrature Oscillator

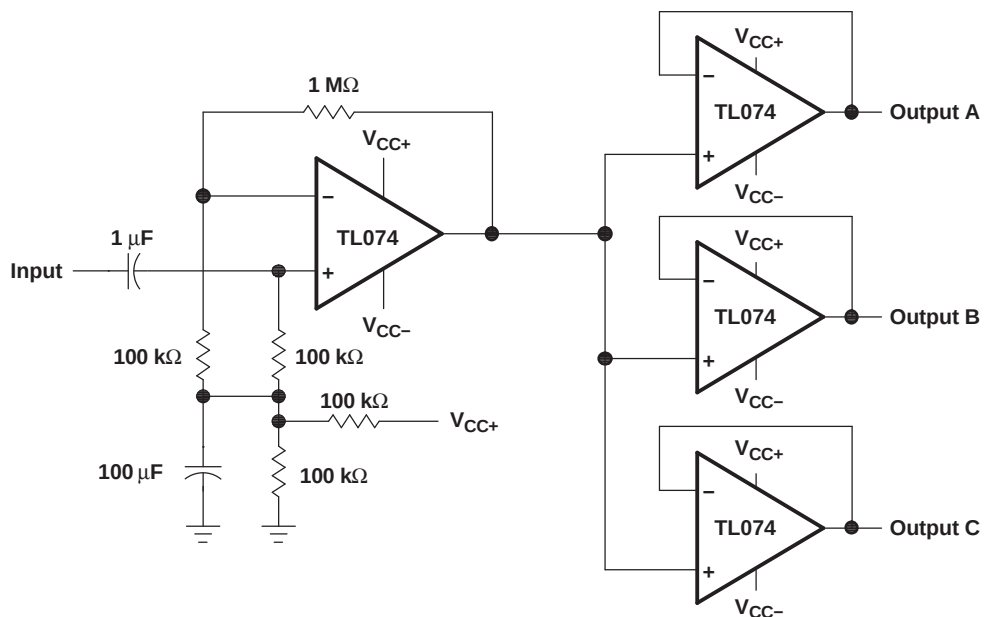


Figure 23. Audio-Distribution Amplifier

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TL072QDREP</a>       | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | TL072Q              |
| TL072QDREP.A                     | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | TL072Q              |
| <a href="#">TL074MDEP</a>        | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TL074M              |
| TL074MDEP.A                      | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TL074M              |
| <a href="#">TL074MDREP</a>       | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TL074M              |
| TL074MDREP.A                     | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TL074M              |
| <a href="#">TL074QDREP</a>       | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | TL074Q              |
| TL074QDREP.A                     | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | TL074Q              |
| <a href="#">V62/11621-01XE</a>   | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | TL074Q              |
| <a href="#">V62/11621-02XE</a>   | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TL074M              |
| <a href="#">V62/11621-02XE-T</a> | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TL074M              |
| <a href="#">V62/12604-01XE</a>   | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | TL072Q              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL072-EP, TL074-EP :**

- Catalog : [TL072](#), [TL074](#)
- Military : [TL072M](#), [TL074M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

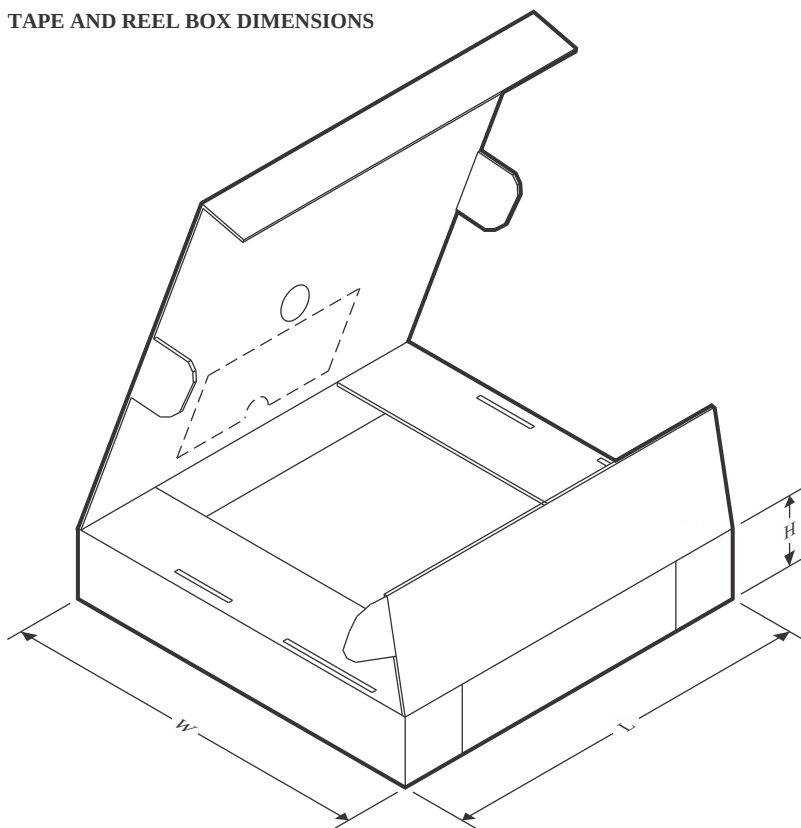
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL072QDREP | SOIC         | D               | 8    | 2500 | 330.0              | 12.5               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL074MDREP | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL074QDREP | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

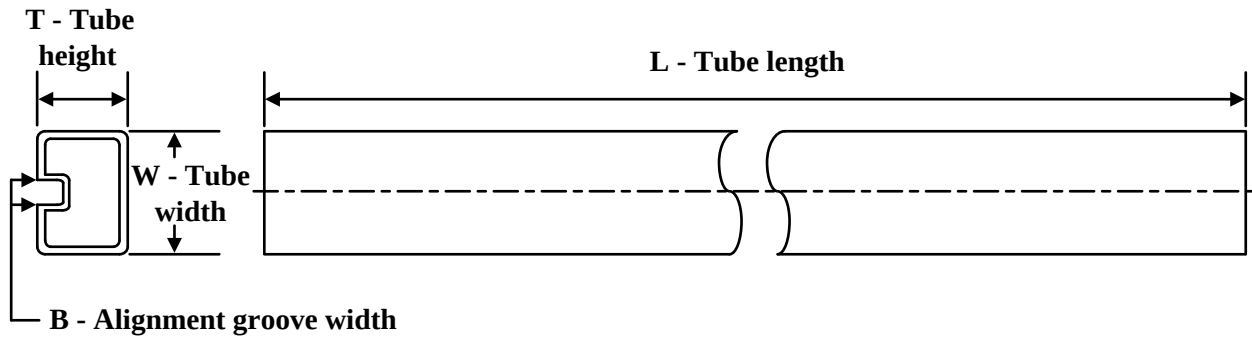
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL072QDREP | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL074MDREP | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| TL074QDREP | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |

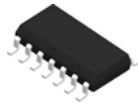
## TUBE



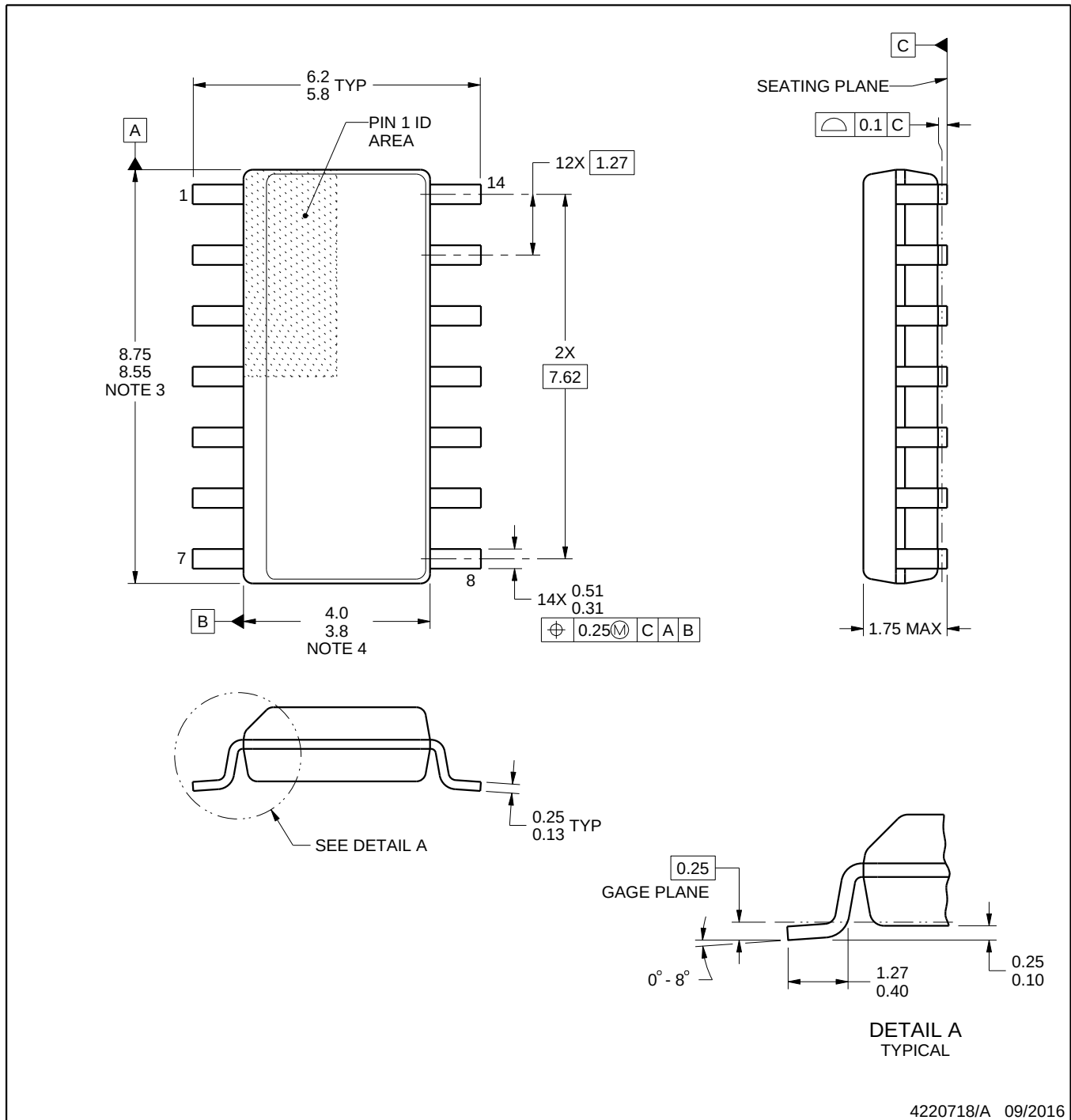
\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TL074MDEP        | D            | SOIC         | 14   | 50  | 507    | 8      | 3940   | 4.32   |
| TL074MDEP.A      | D            | SOIC         | 14   | 50  | 507    | 8      | 3940   | 4.32   |
| V62/11621-02XE-T | D            | SOIC         | 14   | 50  | 507    | 8      | 3940   | 4.32   |



**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

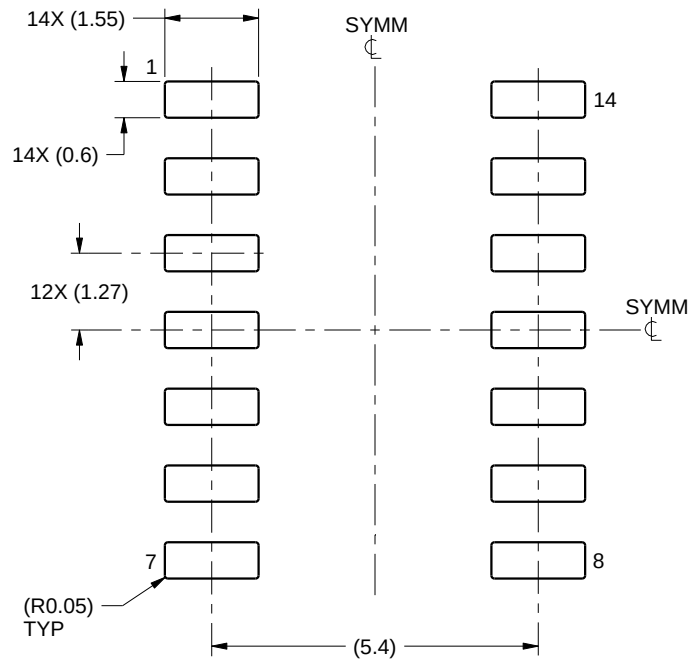
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

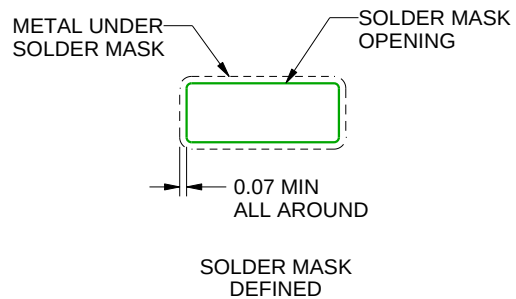
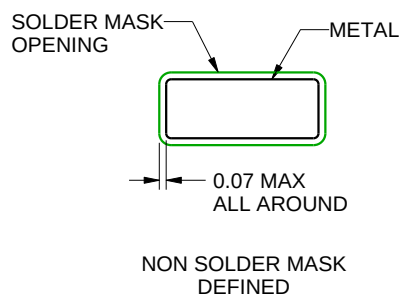
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

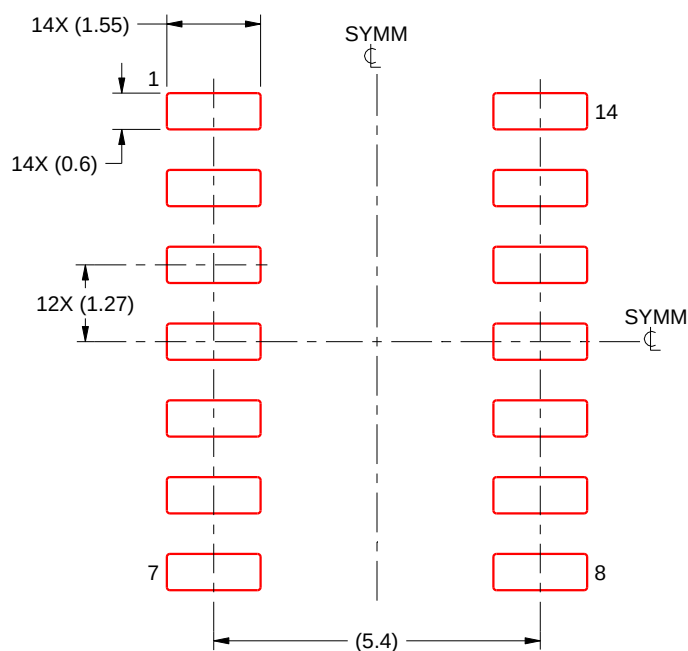
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

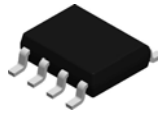


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

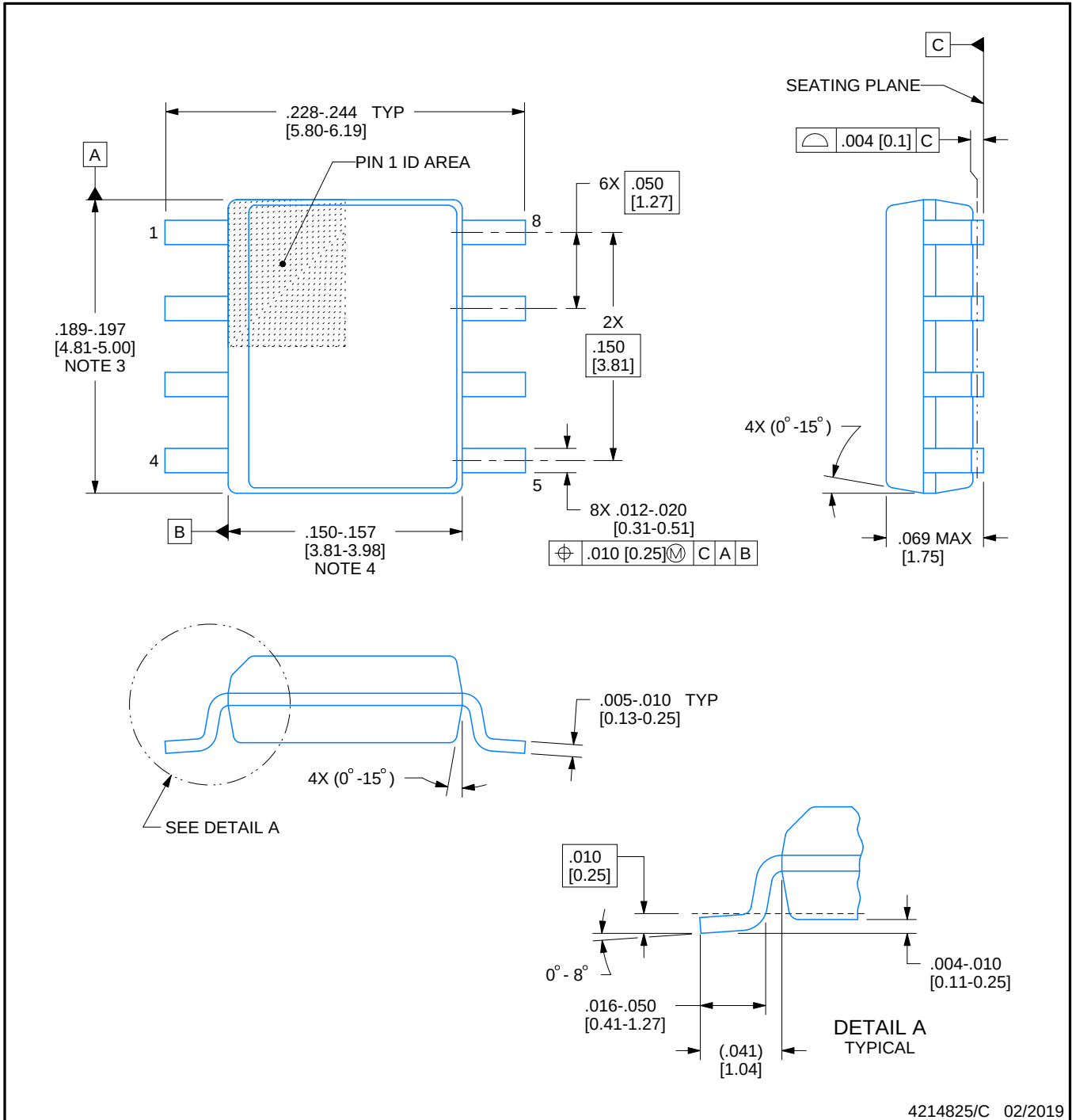


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

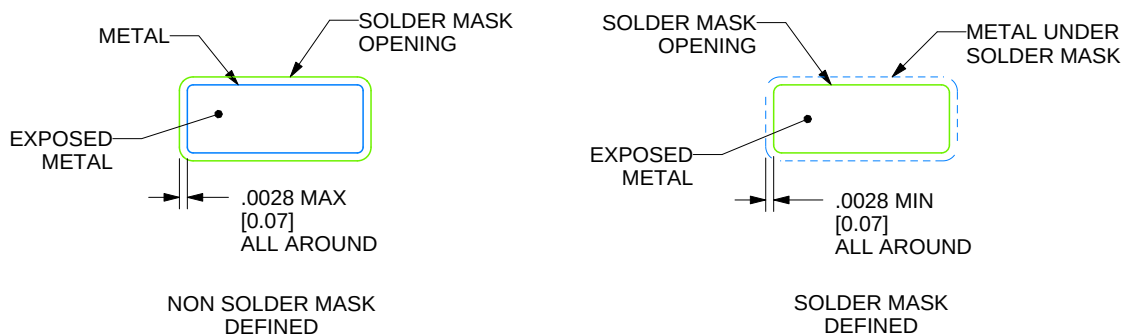
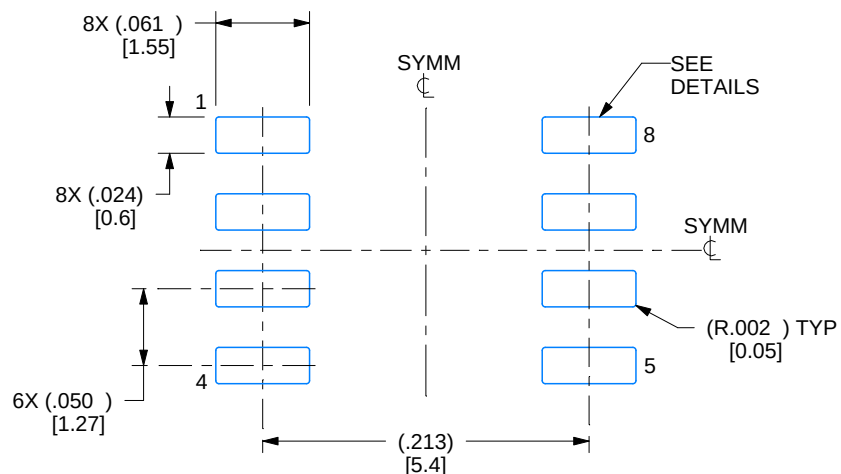
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

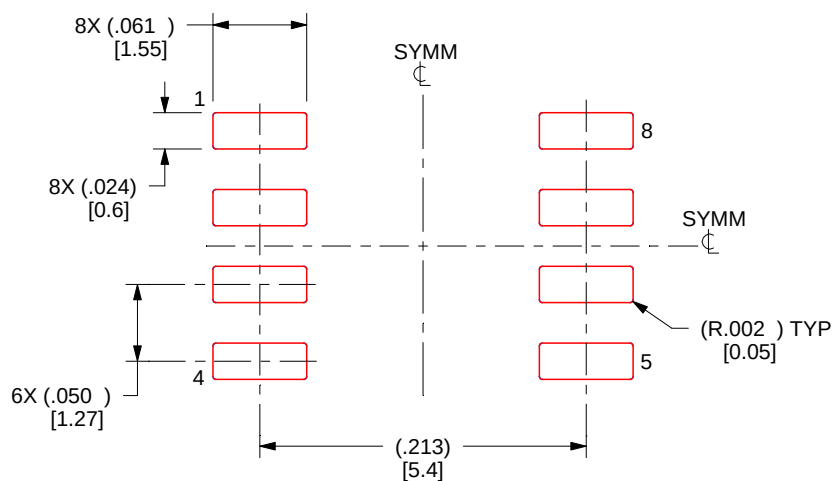
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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