

# TL07xx Low-Noise, FET-Input Operational Amplifiers

## 1 Features

- High slew rate: 20V/μs (TL07xH, typ)
- Low offset voltage: 1mV (TL07xH, typ)
- Low offset voltage drift: 2μV/°C
- Low power consumption: 940μA/ch (TL07xH, typ)
- Wide common-mode and differential voltage ranges
  - Common-mode input voltage range includes V<sub>CC+</sub>
- Low input bias and offset currents
- Low noise:
  - V<sub>n</sub> = 37nV/√Hz (typ) at f = 1kHz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage:
  - ±2.25V to ±20V, 4.5V to 40V

## 2 Applications

- [Solar energy: string and central inverter](#)
- [Motor drives: ac and servo drive control and power-stage modules](#)
- [Single-phase online UPS](#)
- [Three-phase UPS](#)
- [Pro audio mixers](#)
- [Battery test equipment](#)

## 3 Description

The TL071H, TL072H, and TL074H (TL07xH) family of devices are next-generation versions of the industry-standard TL071, TL072, and TL074 (TL07x) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1mV, typical), high slew rate (20V/μs), and common-mode input to the positive supply.

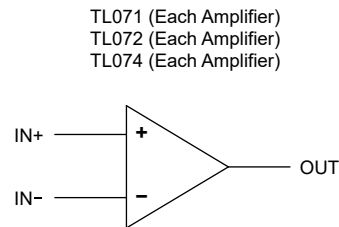
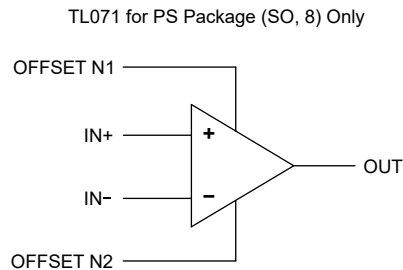
High ESD (1.5kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to +125°C range enable the TL07xH devices for use in the most rugged and demanding applications.

### Device Information

PART NUMBER <sup>(1)</sup>	CHANNEL COUNT	PACKAGE
TL071x	Single	D (SOIC, 8)
		DBV (SOT-23, 5)
		DCK (SC70, 5)
		P (PDIP, 8)
		PS (SO, 8)
TL072x	Dual	D (SOIC, 8)
		DDF (SOT-23-THIN, 8)
		P (PDIP, 8)
		PS (SO, 8)
TL072M <sup>(2)</sup>	Dual	FK (LCCC, 20)
		JG (CDIP, 8)
		U (CFP, 10)
TL074x	Quad	D (SOIC, 14)
		DB (SSOP, 14)
		DYY (SOT-23-THIN, 14)
		N (PDIP, 14)
		NS (SOP, 14)
TL074M <sup>(2)</sup>	Quad	FK (LCCC, 20)
		J (CDIP, 14)
		W (CFP, 14)

(1) For more information, see [Section 11](#).

(2) Devices with M suffix have an extended temperature range of –55°C to +125°C.



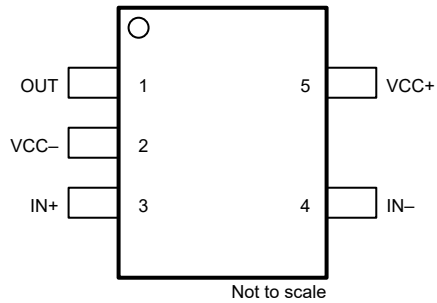
### Logic Symbols



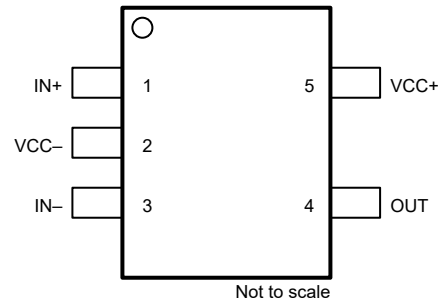
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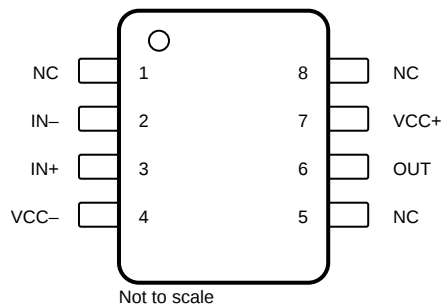
## 4 Pin Configuration and Functions



**Figure 4-1. TL071H DBV Package, 5-Pin SOT-23 (Top View)**



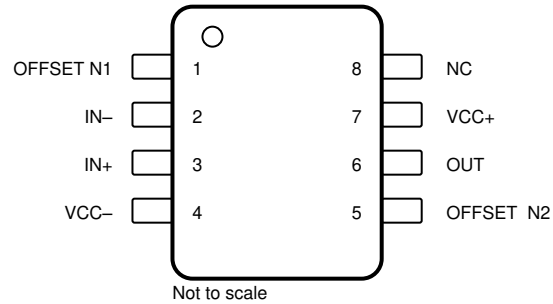
**Figure 4-2. TL071H DCK Package, 5-Pin SC70 (Top View)**



**Figure 4-3. TL071x D Package, 8-Pin SOIC and P Package, 8-pin PDIP (Top View)**

**Table 4-1. Pin Functions: TL071x**

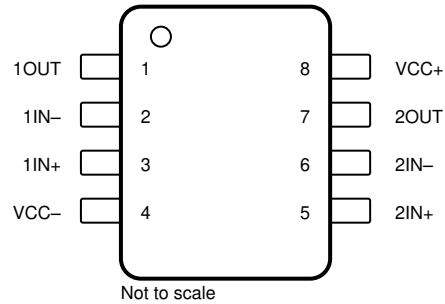
NAME	PIN NO.				TYPE	DESCRIPTION
	DBV (SOT-23)	DCK (SC70)	D (SOIC)	P (PDIP)		
IN-	4	3	2	2	Input	Inverting input
IN+	3	1	3	3	Input	Noninverting input
NC	—	—	8	8	—	Do not connect
NC	—	—	1	1	—	Do not connect
NC	—	—	5	5	—	Do not connect
OUT	1	4	6	6	Output	Output
VCC-	2	2	4	4	—	Power supply
VCC+	5	5	7	7	—	Power supply



**Figure 4-4. TL071C PS Package, 8-Pin SO  
(Top View)**

**Table 4-2. Pin Functions: TL071C**

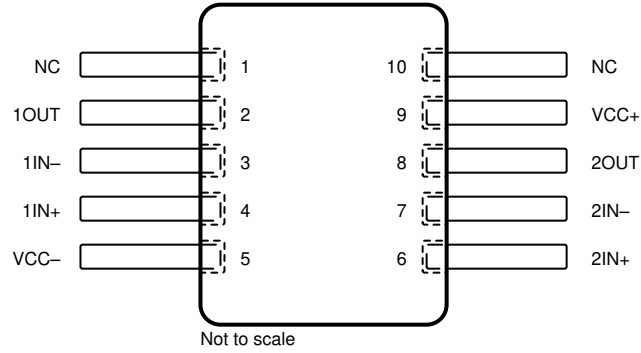
PIN		TYPE	DESCRIPTION
NAME	NO.		
IN-	2	Input	Inverting input
IN+	3	Input	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	Output	Output
VCC-	4	—	Power supply
VCC+	7	—	Power supply



**Figure 4-5. TL072x D, DDF, JG, P, PS, and PW Packages,  
8-Pin SOIC, SOT-23-THIN, CDIP, PDIP, SO, and TSSOP  
(Top View)**

**Table 4-3. Pin Functions: TL072x**

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN-	2	Input	Inverting input
1IN+	3	Input	Noninverting input
1OUT	1	Output	Output
2IN-	6	Input	Inverting input
2IN+	5	Input	Noninverting input
2OUT	7	Output	Output
VCC-	4	—	Power supply
VCC+	8	—	Power supply



**Figure 4-6. TL072M U Package, 10-Pin CFP  
(Top View)**

**Table 4-4. Pin Functions: TL072M**

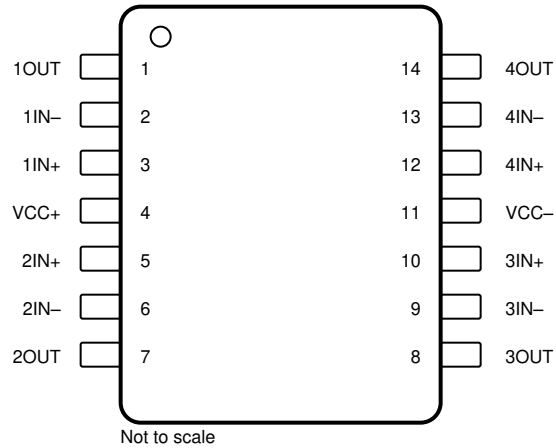
PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN-	3	Input	Inverting input
1IN+	4	Input	Noninverting input
1OUT	2	Output	Output
2IN-	7	Input	Inverting input
2IN+	6	Input	Noninverting input
2OUT	8	Output	Output
NC	1, 10	—	Do not connect
VCC-	5	—	Power supply
VCC+	9	—	Power supply



**Figure 4-7. TL072M FK Package, 20-Pin LCCC (Top View)**

**Table 4-5. Pin Functions: TL072M**

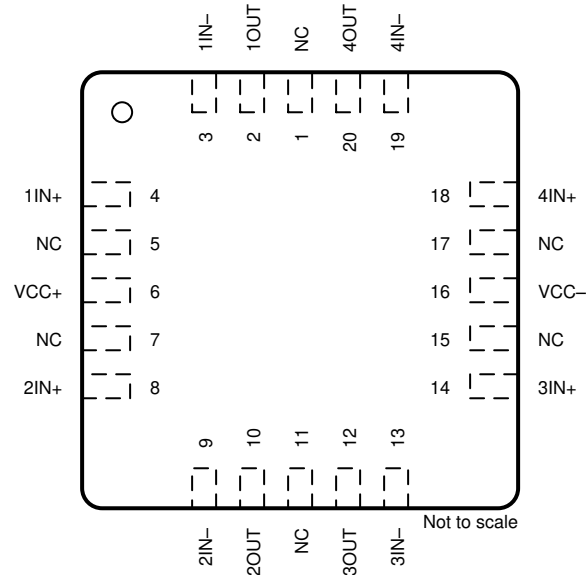
PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN-	5	Input	Inverting input
1IN+	7	Input	Noninverting input
1OUT	2	Output	Output
2IN-	15	Input	Inverting input
2IN+	12	Input	Noninverting input
2OUT	17	Output	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC-	10	—	Power supply
VCC+	20	—	Power supply



**Figure 4-8. TL074x D, DYY, J, N, NS, PW and W Packages,  
 14-Pin SOIC, SOT-23-THIN, CDIP, PDIP, SOP, TSSOP, and CFP  
 (Top View)**

**Table 4-6. Pin Functions: TL074x**

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN-	2	Input	Inverting input
1IN+	3	Input	Noninverting input
1OUT	1	Output	Output
2IN-	6	Input	Inverting input
2IN+	5	Input	Noninverting input
2OUT	7	Output	Output
3IN-	9	Input	Inverting input
3IN+	10	Input	Noninverting input
3OUT	8	Output	Output
4IN-	13	Input	Inverting input
4IN+	12	Input	Noninverting input
4OUT	14	Output	Output
VCC-	11	—	Power supply
VCC+	4	—	Power supply



**Figure 4-9. TL074M FK Package, 20-Pin LCCC (Top View)**

**Table 4-7. Pin Functions: TL074M**

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN-	3	Input	Inverting input
1IN+	4	Input	Noninverting input
1OUT	2	Output	Output
2IN-	9	Input	Inverting input
2IN+	8	Input	Noninverting input
2OUT	10	Output	Output
3IN-	13	Input	Inverting input
3IN+	14	Input	Noninverting input
3OUT	12	Output	Output
4IN-	19	Input	Inverting input
4IN+	18	Input	Noninverting input
4OUT	20	Output	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC-	16	—	Power supply
VCC+	6	—	Power supply

## 5 Specifications

### Note

The TLV07xx series has transitioned new die fabrication into a modern process.

This new die is available with an H suffix.

A die with a different suffix is either older or newer; see also [Section 9.1.1](#).

[Section 5.7](#) and [Section 5.10](#) describe the performance of the new die.

[Section 5.8](#), [Section 5.9](#), and [Section 5.11](#) describe the performance of the old die.

### 5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		All NS and PS packages; All TL07xM devices	-0.3	36	V
		All other devices	0	42	
Signal input pins	Common-mode voltage <sup>(2)</sup>	All NS and PS packages; All TL07xM devices	$(V_{CC-}) - 0.3$	$(V_{CC-}) + 36$	V
		All other devices	$(V_{CC-}) - 0.5$	$(V_{CC+}) + 0.5$	
	Differential voltage <sup>(2)</sup>	All NS and PS packages; All TL07xM devices <sup>(3)</sup>	$(V_{CC-}) - 0.3$	$(V_{CC-}) + 36$	V
		All other devices		$V_S + 0.2$	
Current <sup>(2)</sup>	All NS and PS packages; All TL07xM devices		50	mA	
	All other devices	-10	10		
Output short-circuit <sup>(4)</sup>			Continuous		
Operating ambient temperature, $T_A$			-55	150	°C
Junction temperature, $T_J$				150	°C
Case temperature for 60 seconds - FK package				260	°C
Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds				300	°C
Storage temperature, $T_{stg}$			-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to both power-supply rails on all new die. Current limit input signals that swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Differential voltage only limited by input voltage.
- (4) Short-circuit to ground, one amplifier per package.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage, (V <sub>CC+</sub> ) – (V <sub>CC-</sub> )	All NS and PS packages; All TL07xM devices <sup>(1)</sup>	10	30	V
		All other devices	4.5	40	
V <sub>I</sub>	Input voltage	All NS and PS packages; All TL07xM devices	(V <sub>CC-</sub> ) + 2	(V <sub>CC+</sub> ) + 0.1	V
		All other devices	(V <sub>CC-</sub> ) + 4	(V <sub>CC+</sub> ) + 0.1	
T <sub>A</sub>	Specified temperature <sup>(2)</sup>	TL07xM	-55	125	°C
		TL07xH	-40	125	
		TL07xI	-40	85	
		TL07xC	0	70	

- (1) V<sub>CC+</sub> and V<sub>CC-</sub> are not required to be of equal magnitude, provided that the total V<sub>S</sub> ((V<sub>CC+</sub>) – (V<sub>CC-</sub>)) is between 10 V and 30 V.  
(2) See also [Section 9.1.1](#).

### 5.4 Thermal Information for Single Channel

THERMAL METRIC <sup>(1)</sup>		TL071xx					UNIT
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	P (PDIP)	PS (SO)	
		8 PINS	5 PINS	5 PINS	8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	158.8	217.5	212.2	85	95	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	98.6	113.1	111.1	–	–	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	102.3	63.8	79.4	–	–	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	45.8	34.8	51.8	–	–	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	101.5	63.5	79.0	–	–	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.5 Thermal Information for Dual Channel

THERMAL METRIC <sup>(1)</sup>		TL072xx								UNIT
		D (SOIC)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SO)	PW (TSSOP)	U (CFP)	
		8 PINS	8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	147.8	181.5	–	–	85	95	200.3	169.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	88.2	112.5	5.61	15.05	–	–	89.4	62.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	91.4	98.2	–	–	–	–	131.0	176.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	36.8	17.2	–	–	–	–	22.2	48.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	90.6	97.6	–	–	–	–	129.3	144.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	N/A	5.4	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.6 Thermal Information for Quad Channel

THERMAL METRIC <sup>(1)</sup>		TL074xx								UNIT
		D (SOIC)	DYY (SOT-23)	FK (TSSOP)	J (TSSOP)	N (TSSOP)	NS (TSSOP)	PW (TSSOP)	W (TSSOP)	
		14 PINS	14 PINS	20 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	114.2	153.2	–	–	80	76	–	128.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	70.3	88.7	5.61	14.5	–	–	14.5	56.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	70.2	65.4	–	–	–	–	–	127.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	28.8	9.5	–	–	–	–	–	29	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	69.8	65.0	–	–	–	–	–	106.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	–	0.5	°C/W

(1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.7 Electrical Characteristics for TL07xH

at  $V_S = (V_{CC+}) - (V_{CC-}) = 4.5\text{ V to }40\text{ V}$  ( $\pm 2.25\text{ V to } \pm 20\text{ V}$ ),  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage				$\pm 1$	$\pm 4$	mV	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			$\pm 5$		
$dV_{OS}/dT$	Input offset voltage drift		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		$\pm 2$		$\mu\text{V}/^\circ\text{C}$	
PSRR	Input offset voltage versus power supply	$V_S = 5\text{ V to }40\text{ V}$ , $V_{CM} = V_S / 2$	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		$\pm 1$	$\pm 10$	$\mu\text{V}/\text{V}$	
	Channel separation	$f = 0\text{ Hz}$			10		$\mu\text{V}/\text{V}$	
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current				$\pm 1$	$\pm 120$	pA	
			DCK and DBV packages		$\pm 1$	$\pm 300$	pA	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}^{(1)}$			$\pm 5$	nA	
$I_{OS}$	Input offset current				$\pm 0.5$	$\pm 120$	pA	
			DCK and DBV packages		$\pm 0.5$	$\pm 250$	pA	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}^{(1)}$			$\pm 5$	nA	
<b>NOISE</b>								
$E_N$	Input voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$			9.2		$\mu\text{V}_{PP}$	
					1.4		$\mu\text{V}_{RMS}$	
$e_N$	Input voltage noise density	$f = 1\text{ kHz}$			37		$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 10\text{ kHz}$			21			
$i_N$	Input current noise	$f = 1\text{ kHz}$			80		$\text{fA}/\sqrt{\text{Hz}}$	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage			$(V_{CC-}) + 1.5$		$(V_{CC+})$	V	
CMRR	Common-mode rejection ratio	$V_S = 40\text{ V}$ , $(V_{CC-}) + 2.5\text{ V} < V_{CM} < (V_{CC+}) - 1.5\text{ V}$			100	105	dB	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			95		dB
		$V_S = 40\text{ V}$ , $(V_{CC-}) + 2.5\text{ V} < V_{CM} < (V_{CC+})$				90	105	dB
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			80		dB
<b>INPUT CAPACITANCE</b>								
$Z_{ID}$	Differential				$100 \parallel 2$		$\text{M}\Omega \parallel \text{pF}$	
$Z_{ICM}$	Common-mode				$6 \parallel 1$		$\text{T}\Omega \parallel \text{pF}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 40\text{ V}$ , $V_{CM} = V_S / 2$ , $(V_{CC-}) + 0.3\text{ V} < V_O < (V_{CC+}) - 0.3\text{ V}$	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		118	125	dB	
$A_{OL}$	Open-loop voltage gain	$V_S = 40\text{ V}$ , $V_{CM} = V_S / 2$ , $R_L = 2\text{ k}\Omega$ , $(V_{CC-}) + 1.2\text{ V} < V_O < (V_{CC+}) - 1.2\text{ V}$	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		115	120	dB	
<b>FREQUENCY RESPONSE</b>								
GBW	Gain-bandwidth product				5.25		MHz	
SR	Slew rate	$V_S = 40\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			20		$\text{V}/\mu\text{s}$	
$t_s$	Settling time	$\text{To } 0.1\%$ , $V_S = 40\text{ V}$ , $V_{STEP} = 10\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			0.63		$\mu\text{s}$	
		$\text{To } 0.1\%$ , $V_S = 40\text{ V}$ , $V_{STEP} = 2\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			0.56			
		$\text{To } 0.01\%$ , $V_S = 40\text{ V}$ , $V_{STEP} = 10\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			0.91			
		$\text{To } 0.01\%$ , $V_S = 40\text{ V}$ , $V_{STEP} = 2\text{ V}$ , $G = +1$ , $C_L = 20\text{ pF}$			0.48			
	Phase margin	$G = +1$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$			56		$^\circ$	
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			300		ns	
THD+N	Total harmonic distortion + noise	$V_S = 40\text{ V}$ , $V_O = 6\text{ V}_{RMS}$ , $G = +1$ , $f = 1\text{ kHz}$			0.00012		%	
EMIRR	EMI rejection ratio	$f = 1\text{ GHz}$			53		dB	

## 5.7 Electrical Characteristics for TL07xH (continued)

at  $V_S = (V_{CC+}) - (V_{CC-}) = 4.5\text{ V to }40\text{ V}$  ( $\pm 2.25\text{ V to } \pm 20\text{ V}$ ),  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
Voltage output swing from rail	Positive rail headroom	$V_S = 40\text{ V}, R_L = 10\text{ k}\Omega$		115	210	mV
		$V_S = 40\text{ V}, R_L = 2\text{ k}\Omega$		520	965	
	Negative rail headroom	$V_S = 40\text{ V}, R_L = 10\text{ k}\Omega$		105	215	
		$V_S = 40\text{ V}, R_L = 2\text{ k}\Omega$		500	1030	
$I_{SC}$	Short-circuit current			$\pm 26$		mA
$C_{LOAD}$	Capacitive load drive			300		pF
$Z_O$	Open-loop output impedance	$f = 1\text{ MHz}, I_O = 0\text{ A}$		125		$\Omega$
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current per amplifier	$I_O = 0\text{ A}$	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	937.5	1125	$\mu\text{A}$
		$I_O = 0\text{ A}, (\text{TL071H})$		960	1156	
		$I_O = 0\text{ A}$			1130	
		$I_O = 0\text{ A}, (\text{TL072H})$			1143	
		$I_O = 0\text{ A}, (\text{TL071H})$			1160	
	Turn-on time	At $T_A = 25^\circ\text{C}, V_S = 40\text{ V}, V_S$ ramp rate $> 0.3\text{ V}/\mu\text{s}$		60		$\mu\text{s}$

(1) Maximum  $I_B$  and  $I_{OS}$  data are specified based on characterization results.

### 5.8 Electrical Characteristics (DC) for TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM

at  $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1) (2)</sup>		MIN	TYP	MAX	UNIT
<b>DC</b>							
$V_{OS}$	Input offset voltage	$V_O = 0\text{ V}$ $R_S = 50\ \Omega$	TL07xC		3	10	mV
				$T_A = \text{Full range}$		13	
			TL07xAC		3	6	
				$T_A = \text{Full range}$		7.5	
			TL07xBC		2	3	
				$T_A = \text{Full range}$		5	
			TL07xI	$T_A = \text{Full range}$	3	6	
TL071M, TL072M	$T_A = \text{Full range}$	3	6				
TL074M	$T_A = \text{Full range}$	3	9				
			$T_A = \text{Full range}$			15	
$dV_{OS}/dT$	Input offset voltage drift	$V_O = 0\text{ V}$ , $R_S = 50\ \Omega$	$T_A = \text{Full range}$		$\pm 18$		$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input offset current	$V_O = 0\text{ V}$	TL07xC		5	100	pA
				$T_A = \text{Full range}$		10	nA
			TL07xAC, TL07xBC, TL07xI		5	100	pA
				$T_A = \text{Full range}$		2	nA
TL07xM		5	100	pA			
$T_A = \text{Full range}$			20	nA			
$I_B$	Input bias current	$V_O = 0\text{ V}$	TL07xC, TL07xAC, TL07xBC, TL07xI		65	200	pA
				$T_A = \text{Full range}$		7	nA
			TL071M, TL072M		65	200	pA
				$T_A = \text{Full range}$		50	nA
			TL074M		65	200	pA
				$T_A = \text{Full range}$		20	nA
$V_{CM}$	Common-mode voltage			$\pm 11$	-12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$	$T_A = \text{Full range}$	$\pm 12$	$\pm 13.5$	V	
		$R_L \geq 10\text{ k}\Omega$		$\pm 12$			
		$R_L \geq 2\text{ k}\Omega$		$\pm 10$			
$A_{OL}$	Open-loop voltage gain	$V_O = 0\text{ V}$	TL07xC		25	200	V/mV
				$T_A = \text{Full range}$		15	
			TL07xAC, TL07xBC, TL07xI		50	200	
				$T_A = \text{Full range}$		25	
			TL07xM		35	200	
$T_A = \text{Full range}$		15					
GBW	Gain-bandwidth product	All NS and PS packages; All TL07xM devices		3		MHz	
		All other devices		5.25			
$R_{ID}$	Common-mode input resistance			1		T $\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$ $V_O = 0\text{ V}$ $R_S = 50\ \Omega$	TL07xC	70	100	dB	
			TL07xAC, TL07xBC, TL07xI	75	100		
			TL07xM	80	86		
PSRR	Input offset voltage versus power supply	$V_S = \pm 9\text{ V to } \pm 18\text{ V}$ $V_O = 0\text{ V}$ $R_S = 50\ \Omega$	TL07xC	70	100	dB	
			TL07xAC, TL07xBC, TL07xI	80	100		
			TL07xM	80	86		

## 5.8 Electrical Characteristics (DC) for TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM (continued)

at  $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1) (2)</sup>	MIN	TYP	MAX	UNIT
$I_Q$	Quiescent current per amplifier	$V_O = 0\text{ V}$ , no load		1.4	2.5	mA
	Channel separation	$f = 0\text{ Hz}$		1		$\mu\text{V/V}$

- (1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.  
 (2) Full range is  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for the TL07xC, TL07xAC, and TL07xBC;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the TL07xI; and  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the TL07xM.

## 5.9 Electrical Characteristics (AC) for TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM

at  $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

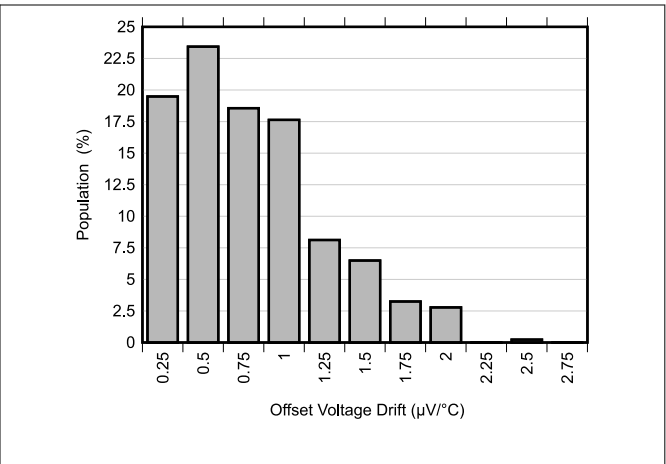
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>AC</b>							
SR	Slew rate	$V_I = 10\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$	TL07xM	5	20		$\text{V}/\mu\text{s}$
			TL07xC, TL07xAC, TL07xBC, TL07xI	8	20		$\text{V}/\mu\text{s}$
$t_s$	Settling time	$V_I = 20\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$			0.1		$\mu\text{s}$
					20%		
$e_N$	Input voltage noise density	All PS and NS packages, all TL07xM devices	$R_S = 20\ \Omega$ , $f = 1\text{ kHz}$		18		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$		37		$\text{nV}/\sqrt{\text{Hz}}$
				$f = 10\text{ kHz}$		21	
$E_N$	Input voltage noise	All PS and NS packages, all TL07xM devices	$R_S = 20\ \Omega$ , $f = 10\text{ Hz}$ to $10\text{ kHz}$		4		$\mu\text{V}_{\text{RMS}}$
			All other devices	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		1.4	
$i_N$	Input current noise	$R_S = 20\ \Omega$ , $f = 1\text{ kHz}$			10		$\text{fA}/\sqrt{\text{Hz}}$
	Phase margin	TL07xC, TL07xAC, TL07xBC, TL07xI	$G = +1$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$		56		$^\circ$
	Overload recovery time	$V_{\text{IN}} \times \text{gain} > V_S$			300		ns
THD+N	Total harmonic distortion + noise	All PS and NS packages, all TL07xM devices	$V_O = 6\text{ V}_{\text{RMS}}$ , $R_L \geq 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $G = +1$ , $R_S \leq 1\text{ k}\Omega$		0.003		%
			All other devices	$V_S = 40\text{ V}$ , $V_O = 6\text{ V}_{\text{RMS}}$ , $G = +1$ , $f = 1\text{ kHz}$		0.00012	
EMIRR	EMI rejection ratio	TL07xC, TL07xAC, TL07xBC, TL07xI	$f = 1\text{ GHz}$		53		dB
$Z_O$	Open-loop output impedance	TL07xC, TL07xAC, TL07xBC, TL07xI	$f = 1\text{ MHz}$ , $I_O = 0\text{ A}$		125		$\Omega$

### 5.10 Typical Characteristics: TL07xH

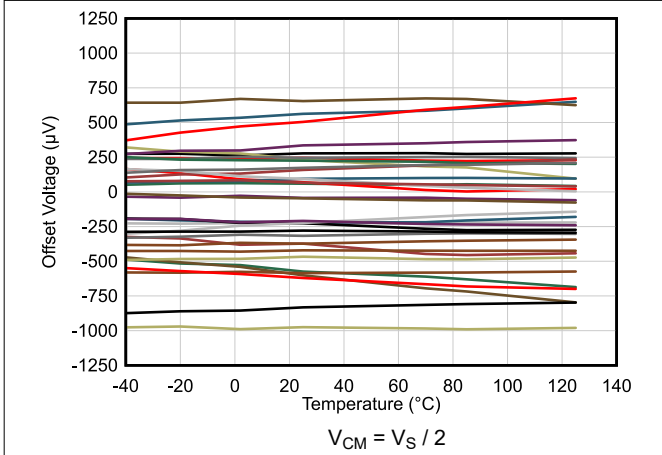
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 40\text{ V}$  ( $\pm 20\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 20\text{ pF}$  (unless otherwise noted)



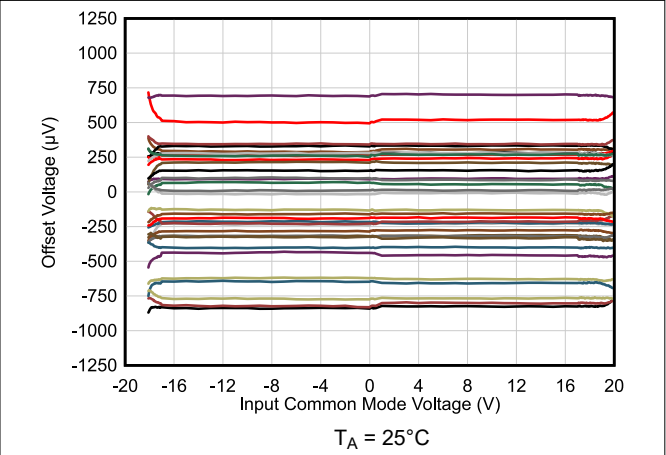
**Figure 5-1. Offset Voltage Production Distribution**



**Figure 5-2. Offset Voltage Drift Distribution**



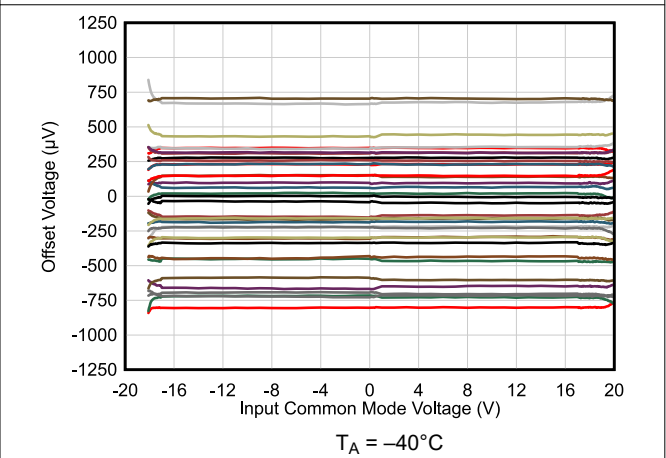
**Figure 5-3. Offset Voltage vs Temperature**



**Figure 5-4. Offset Voltage vs Common-Mode Voltage**



**Figure 5-5. Offset Voltage vs Common-Mode Voltage**



**Figure 5-6. Offset Voltage vs Common-Mode Voltage**

## 5.10 Typical Characteristics: TL07xH (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 40\text{ V}$  ( $\pm 20\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 20\text{ pF}$  (unless otherwise noted)

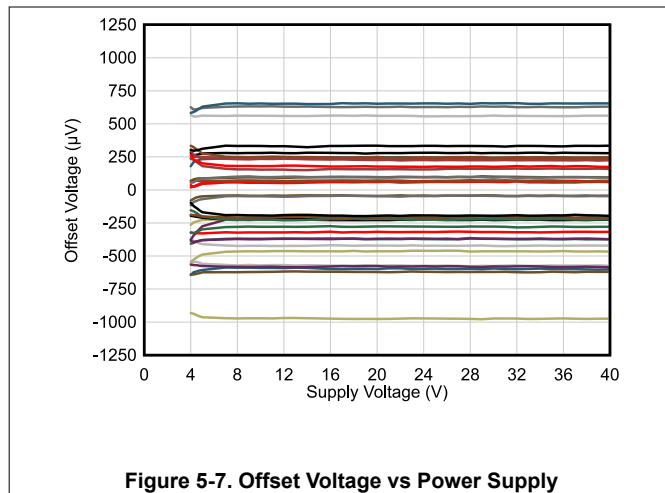


Figure 5-7. Offset Voltage vs Power Supply

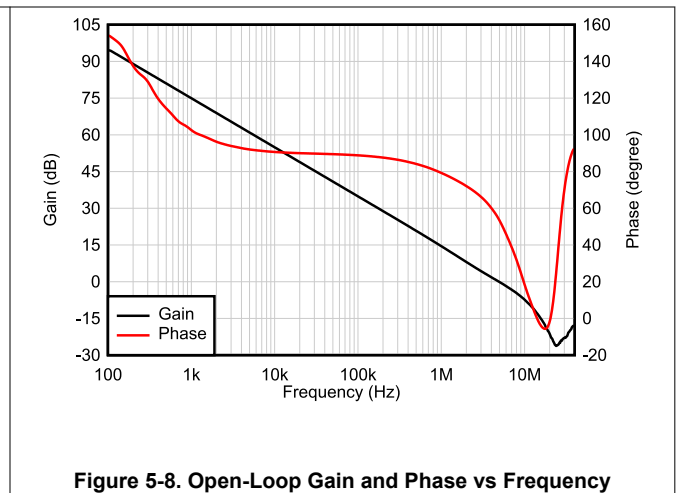


Figure 5-8. Open-Loop Gain and Phase vs Frequency

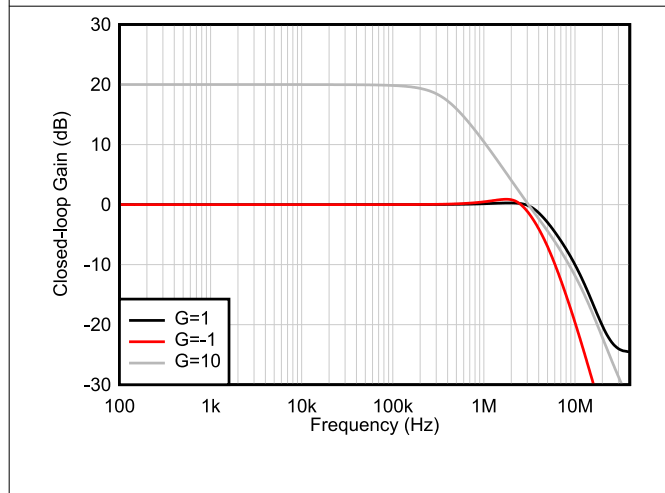


Figure 5-9. Closed-Loop Gain vs Frequency

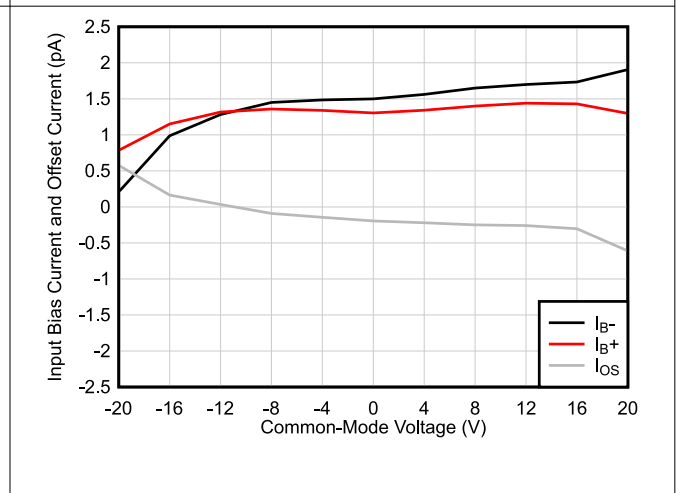


Figure 5-10. Input Bias Current vs Common-Mode Voltage

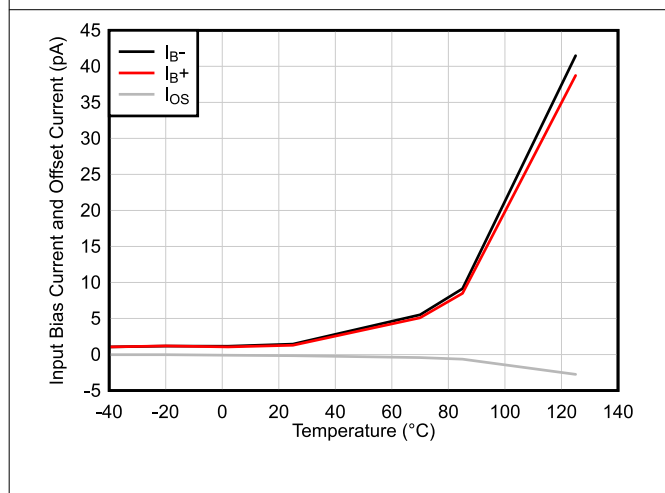


Figure 5-11. Input Bias Current vs Temperature

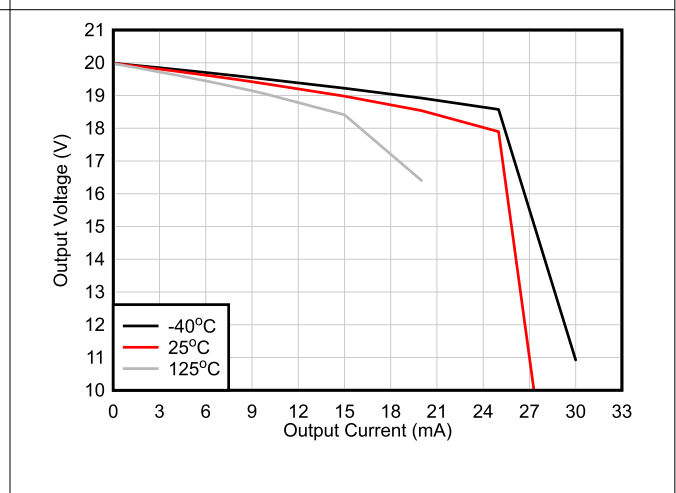
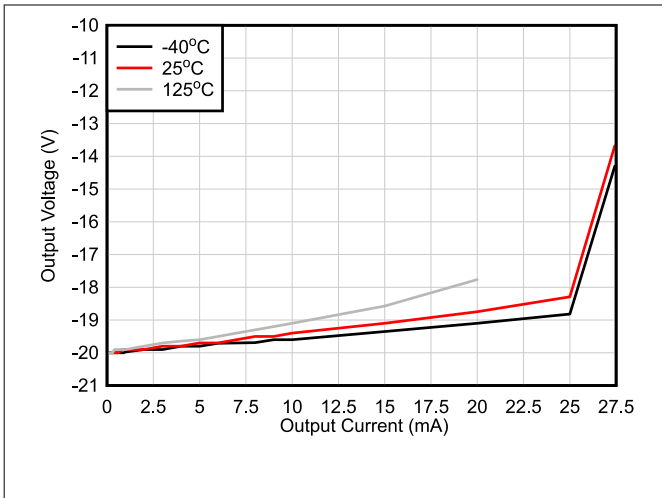


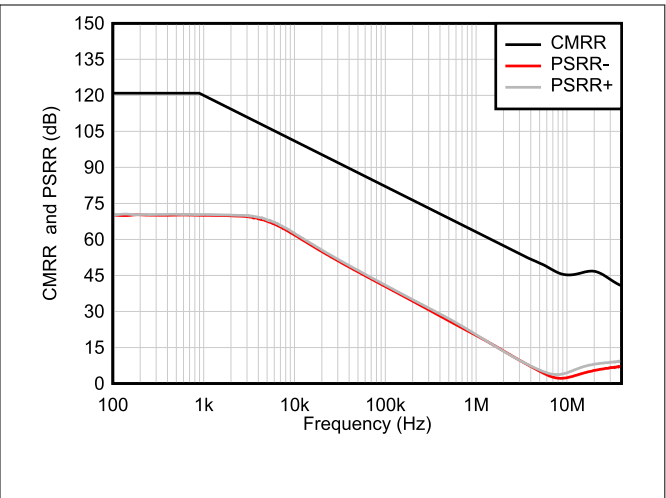
Figure 5-12. Output Voltage Swing vs Output Current (Sourcing)

### 5.10 Typical Characteristics: TL07xH (continued)

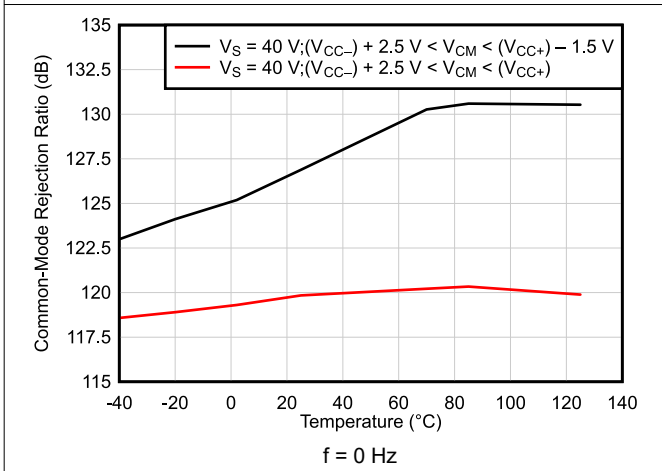
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 40\text{ V}$  ( $\pm 20\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 20\text{ pF}$  (unless otherwise noted)



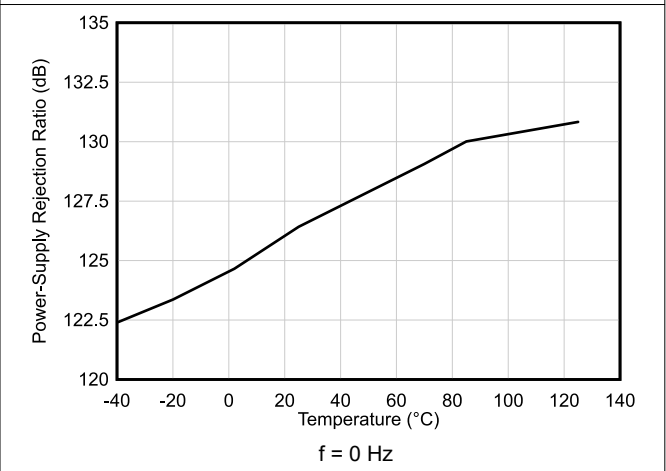
**Figure 5-13. Output Voltage Swing vs Output Current (Sinking)**



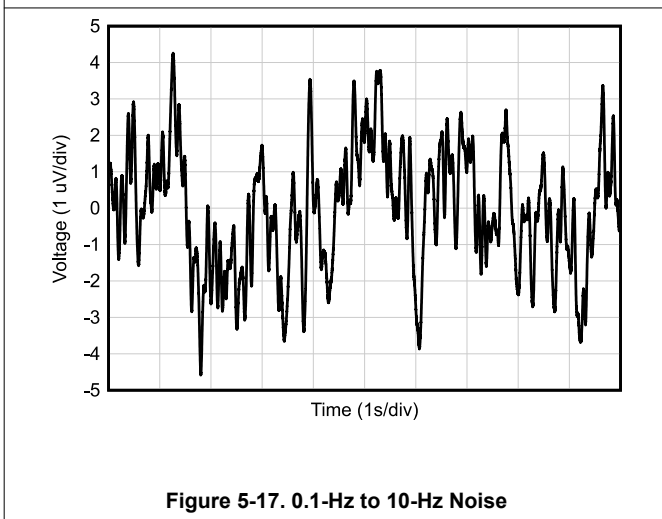
**Figure 5-14. CMRR and PSRR vs Frequency**



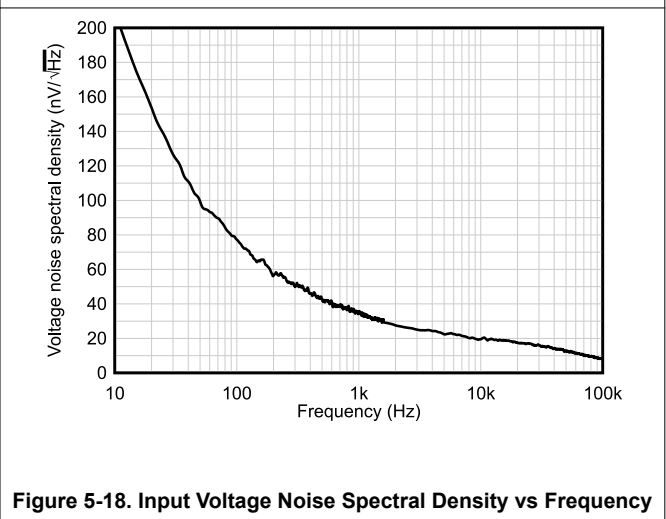
**Figure 5-15. CMRR vs Temperature (dB)**



**Figure 5-16. PSRR vs Temperature (dB)**



**Figure 5-17. 0.1-Hz to 10-Hz Noise**



**Figure 5-18. Input Voltage Noise Spectral Density vs Frequency**

### 5.10 Typical Characteristics: TL07xH (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 40\text{ V}$  ( $\pm 20\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 20\text{ pF}$  (unless otherwise noted)

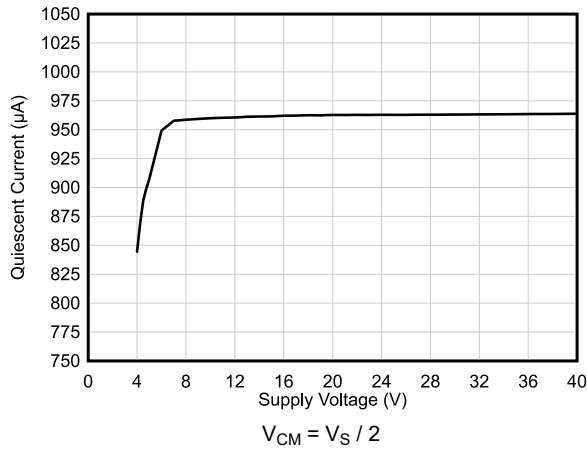


Figure 5-19. Quiescent Current vs Supply Voltage

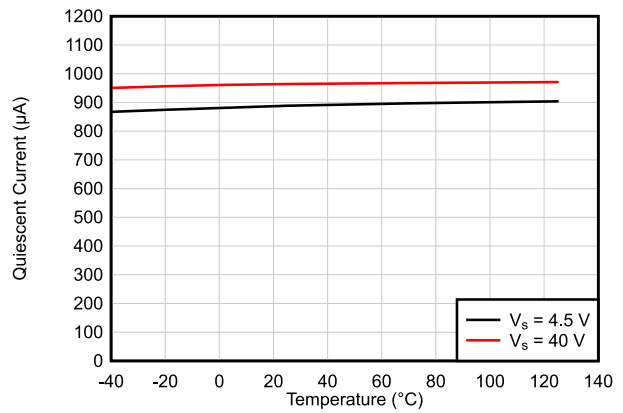


Figure 5-20. Quiescent Current vs Temperature

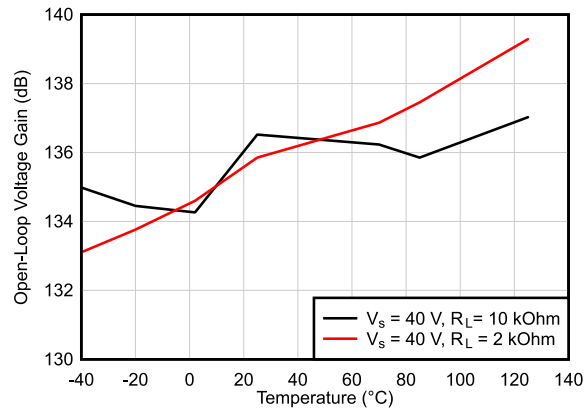


Figure 5-21. Open-Loop Voltage Gain vs Temperature

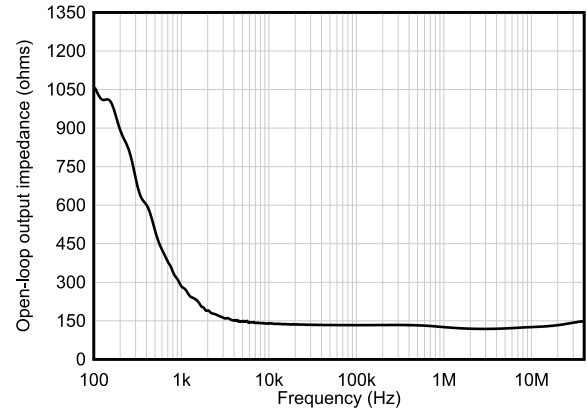


Figure 5-22. Open-Loop Output Impedance vs Frequency

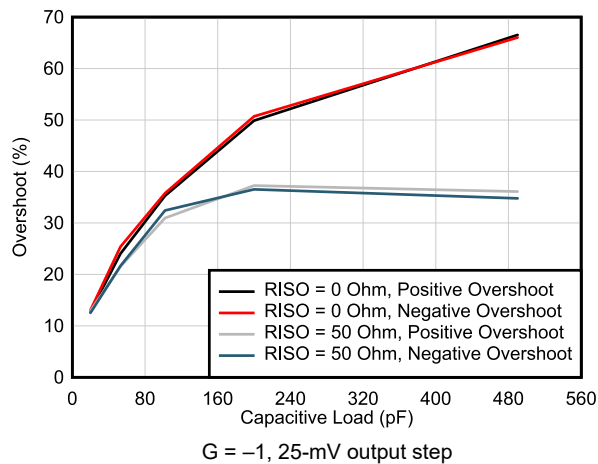


Figure 5-23. Small-Signal Overshoot vs Capacitive Load

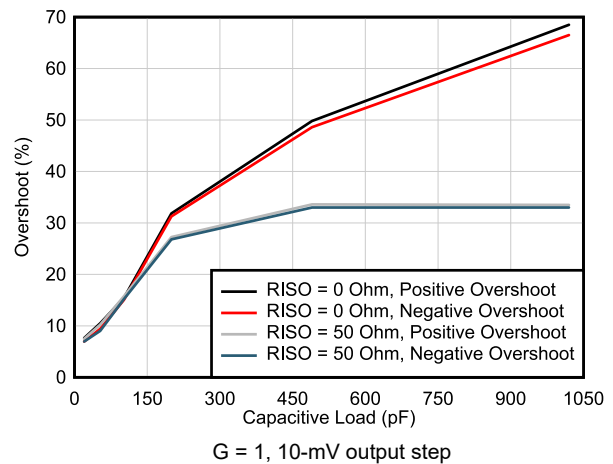
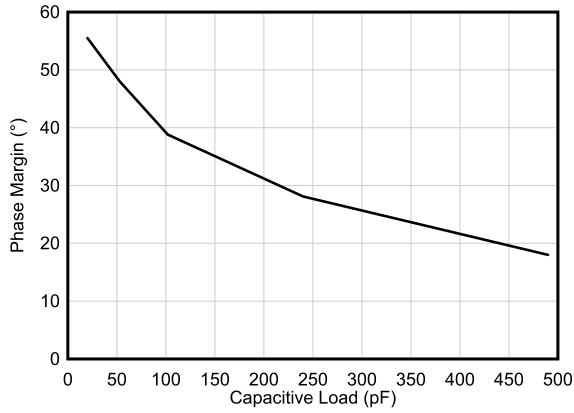


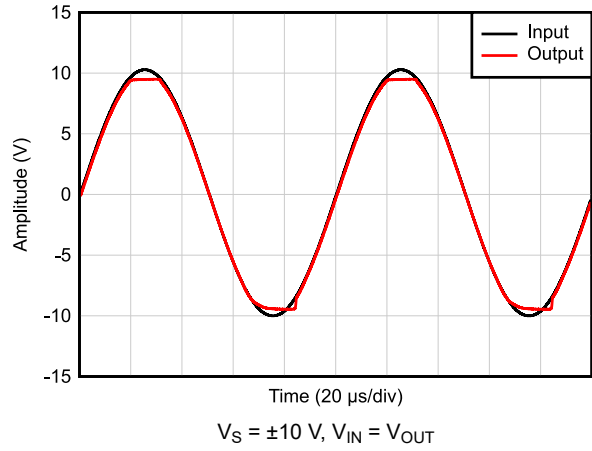
Figure 5-24. Small-Signal Overshoot vs Capacitive Load

### 5.10 Typical Characteristics: TL07xH (continued)

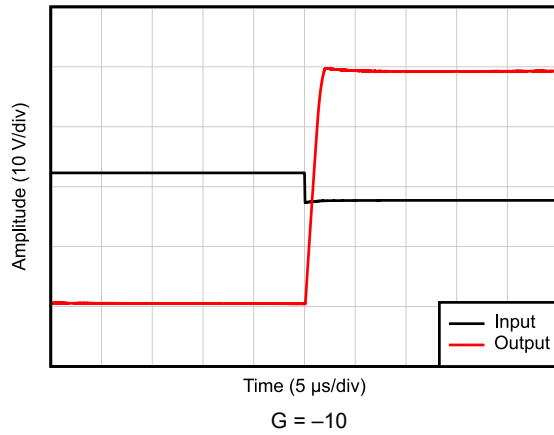
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 40\text{ V}$  ( $\pm 20\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 20\text{ pF}$  (unless otherwise noted)



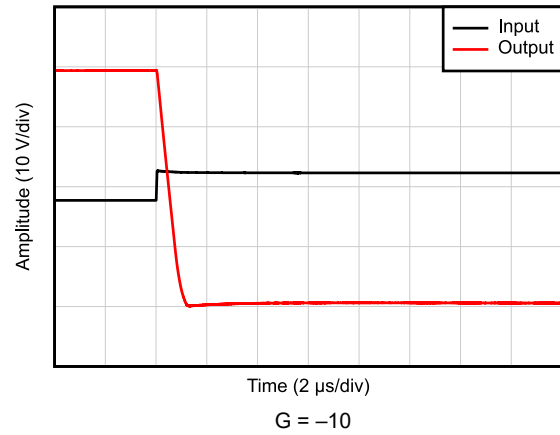
**Figure 5-25. Phase Margin vs Capacitive Load**



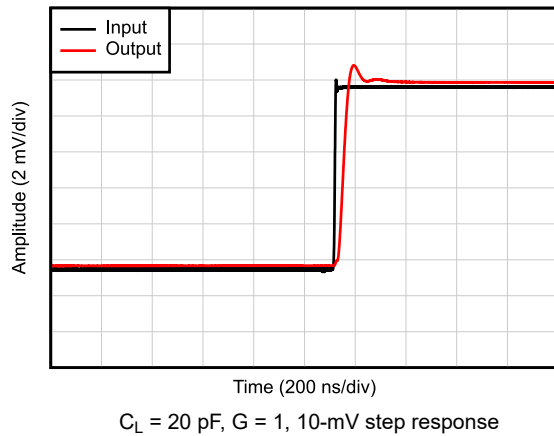
**Figure 5-26. No Phase Reversal**



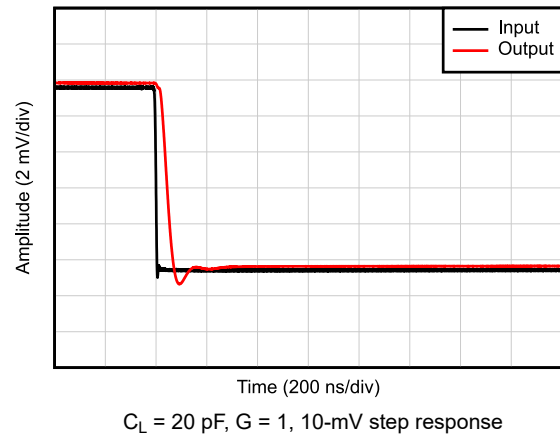
**Figure 5-27. Positive Overload Recovery**



**Figure 5-28. Negative Overload Recovery**



**Figure 5-29. Small-Signal Step Response, Rising**



**Figure 5-30. Small-Signal Step Response, Falling**

## 5.10 Typical Characteristics: TL07xH (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 40\text{ V}$  ( $\pm 20\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 20\text{ pF}$  (unless otherwise noted)

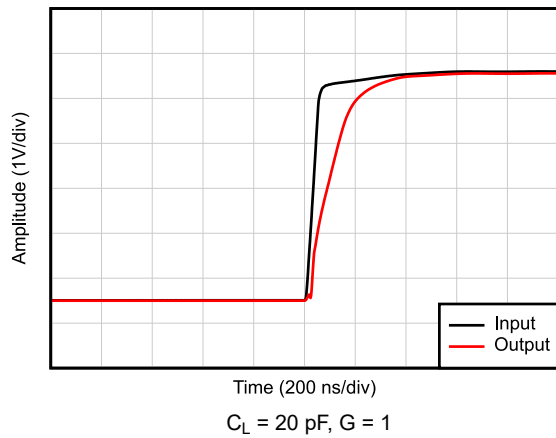


Figure 5-31. Large-Signal Step Response (Rising)

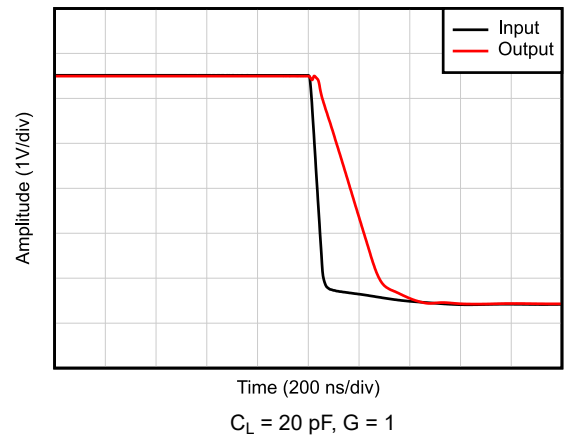


Figure 5-32. Large-Signal Step Response (Falling)

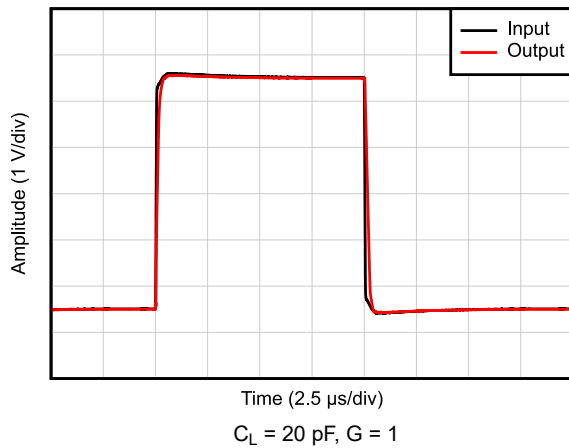


Figure 5-33. Large-Signal Step Response

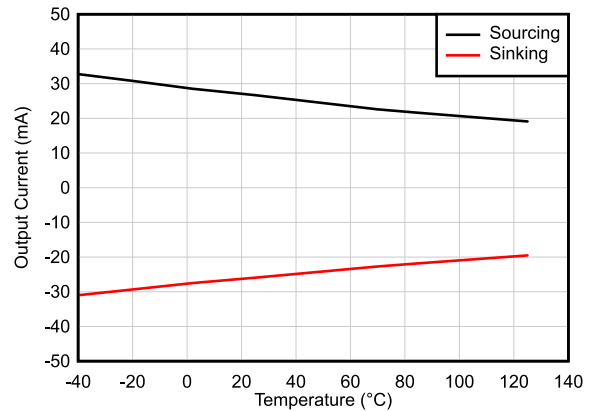


Figure 5-34. Short-Circuit Current vs Temperature

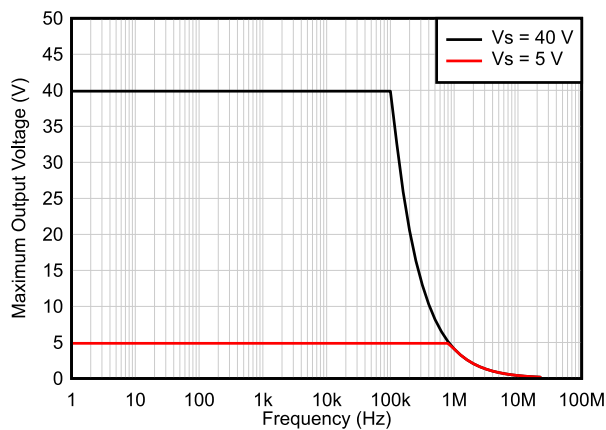


Figure 5-35. Maximum Output Voltage vs Frequency

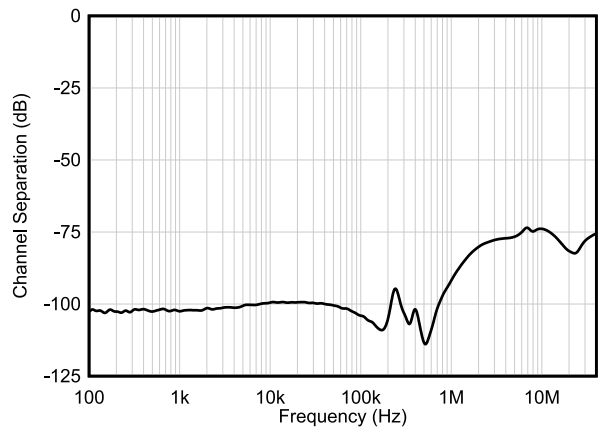


Figure 5-36. Channel Separation vs Frequency

### 5.10 Typical Characteristics: TL07xH (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 40\text{ V}$  ( $\pm 20\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 20\text{ pF}$  (unless otherwise noted)

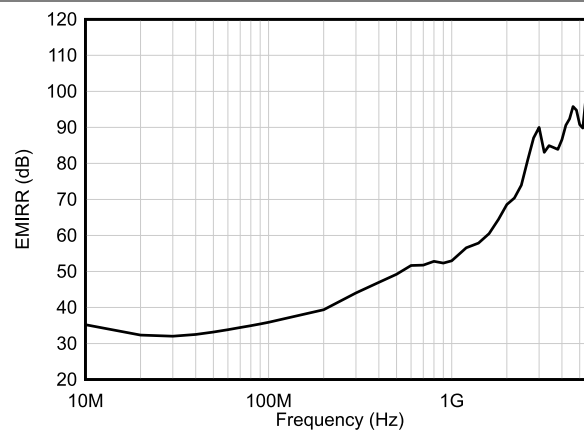


Figure 5-37. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

### 5.11 Typical Characteristics: All Devices Except TL07xH

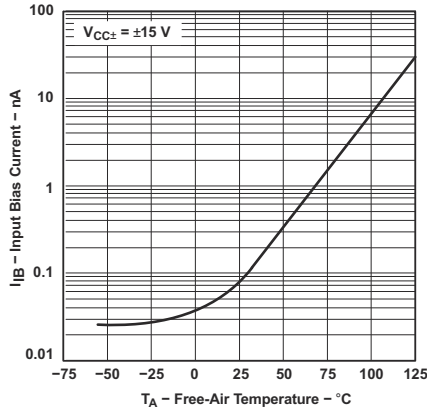


Figure 5-38. Input Bias Current vs Free-Air Temperature

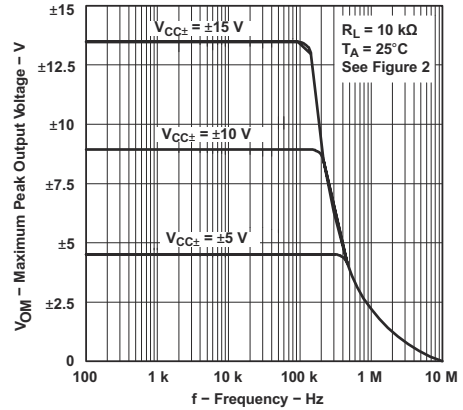


Figure 5-39. Maximum Peak Output Voltage vs Frequency

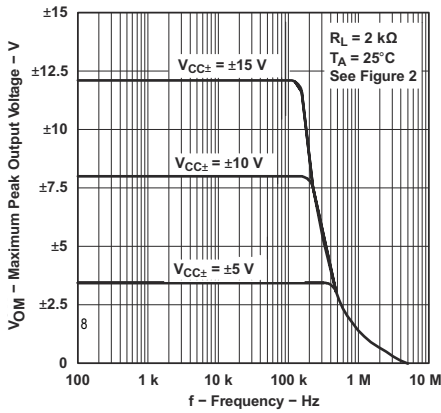


Figure 5-40. Maximum Peak Output Voltage vs Frequency

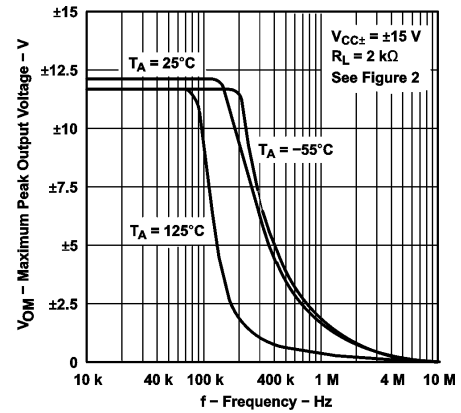


Figure 5-41. Maximum Peak Output Voltage vs Frequency

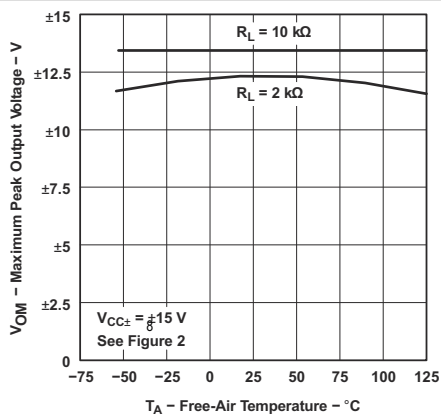


Figure 5-42. Maximum Peak Output Voltage vs Free-Air Temperature

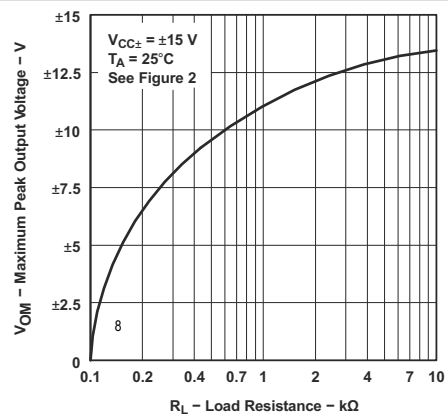


Figure 5-43. Maximum Peak Output Voltage vs Load Resistance

### 5.11 Typical Characteristics: All Devices Except TL07xH (continued)

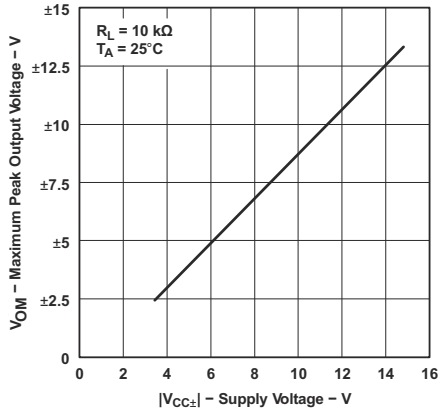


Figure 5-44. Maximum Peak Output Voltage vs Supply Voltage

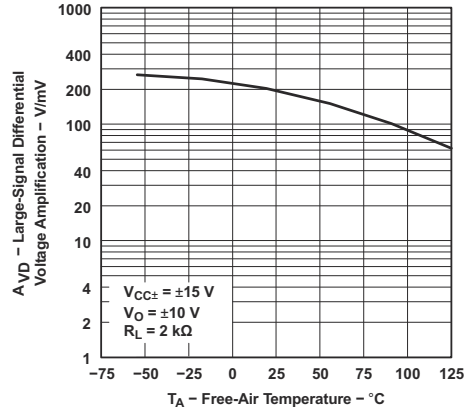


Figure 5-45. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

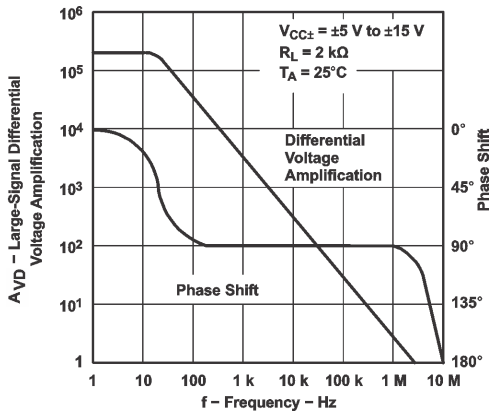


Figure 5-46. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

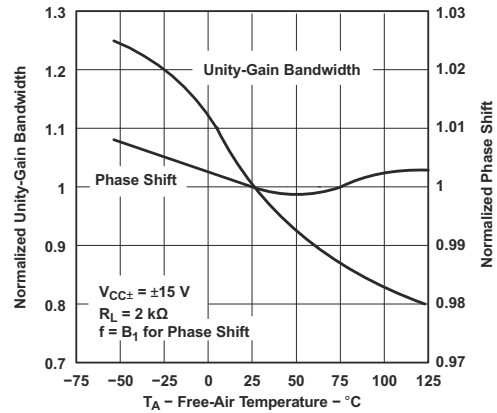


Figure 5-47. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

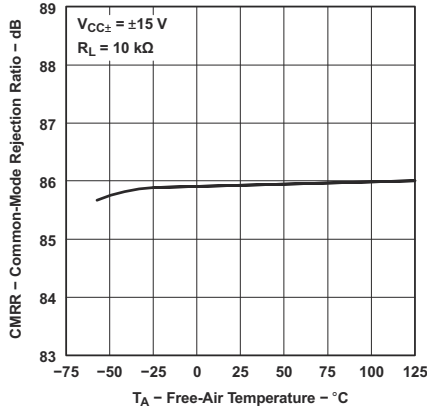


Figure 5-48. Common-Mode Rejection Ratio vs Free-Air Temperature

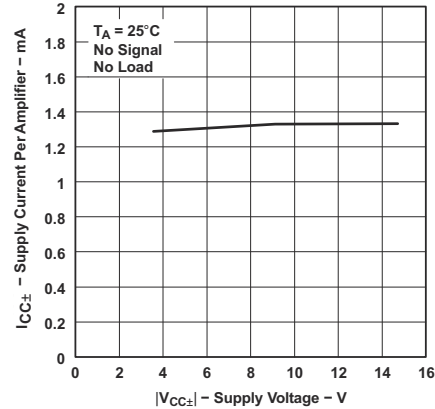


Figure 5-49. Supply Current Per Amplifier vs Supply Voltage

### 5.11 Typical Characteristics: All Devices Except TL07xH (continued)

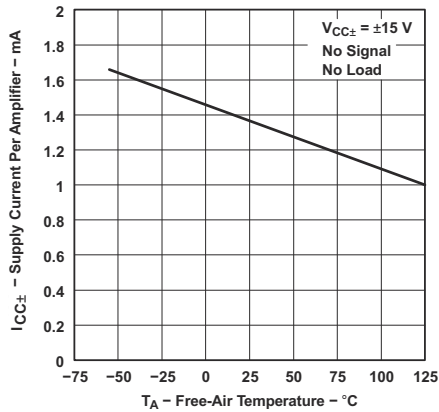


Figure 5-50. Supply Current Per Amplifier vs Free-Air Temperature

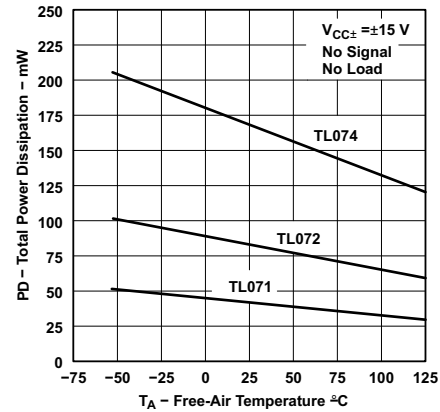


Figure 5-51. Total Power Dissipation vs Free-Air Temperature

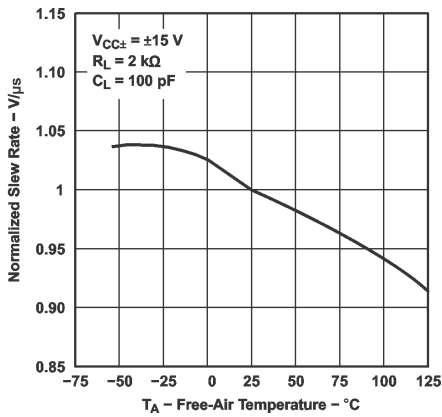


Figure 5-52. Normalized Slew Rate vs Free-Air Temperature

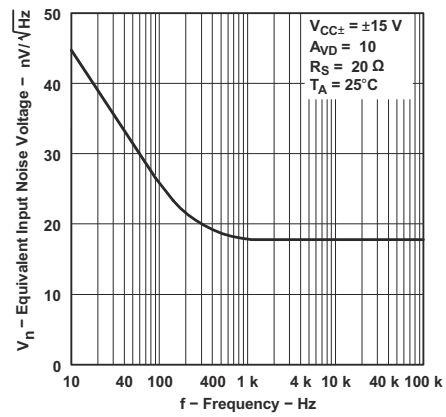


Figure 5-53. Equivalent Input Noise Voltage vs Frequency

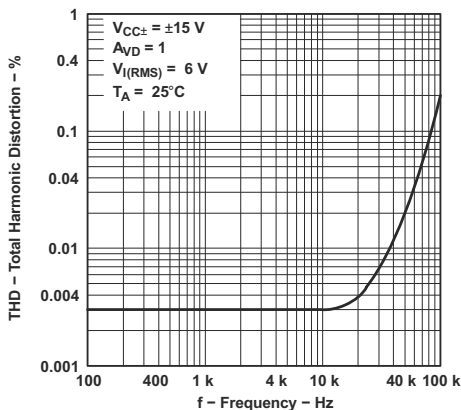


Figure 5-54. Total Harmonic Distortion vs Frequency

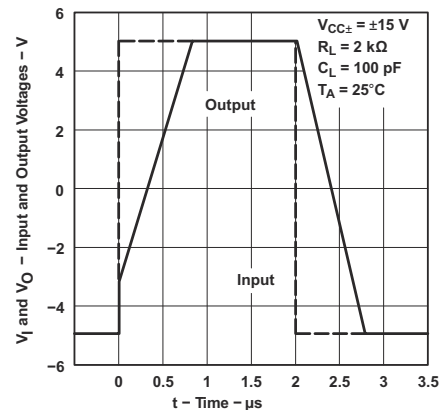


Figure 5-55. Voltage-Follower Large-Signal Pulse Response

### 5.11 Typical Characteristics: All Devices Except TL07xH (continued)

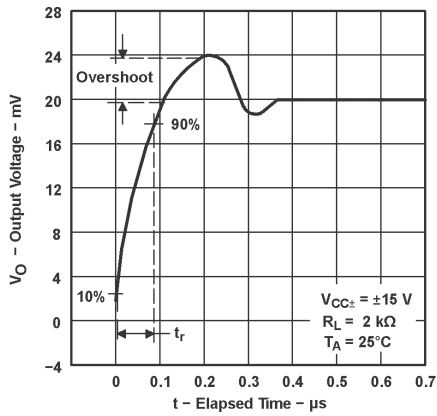


Figure 5-56. Output Voltage vs Elapsed Time

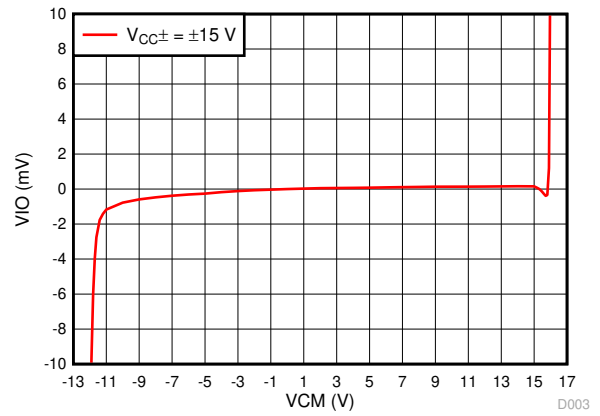
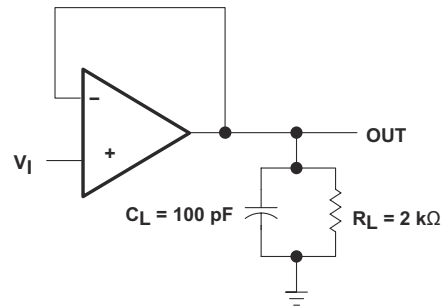
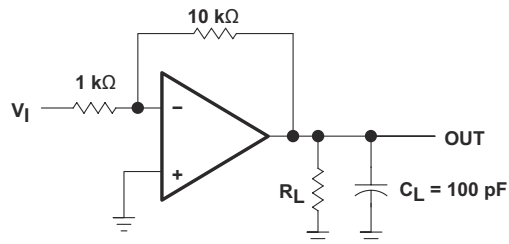


Figure 5-57.  $V_{IO}$  vs  $V_{CM}$

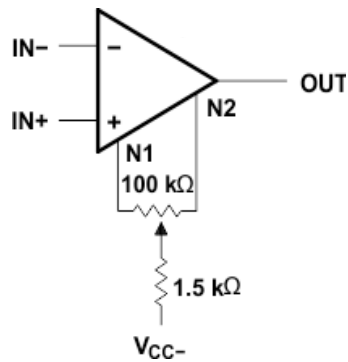
## 6 Parameter Measurement Information



**Figure 6-1. Unity-Gain Amplifier**



**Figure 6-2. Gain-of-10 Inverting Amplifier**



**Figure 6-3. Input Offset-Voltage Null Circuit  
for PS Package (SO, 8) Only**



## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier makes negative voltages positive.

### 8.2 Typical Applications

#### 8.2.1 Inverting Amplifier

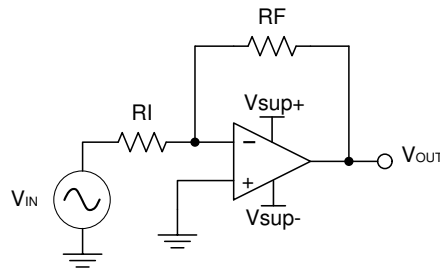


Figure 8-1. Inverting Amplifier

##### 8.2.1.1 Design Requirements

The supply voltage must be selected so the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

##### 8.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

After the desired gain is determined, select a value for  $R_I$  or  $R_F$ . Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamp range. This example uses  $10$  k $\Omega$  for  $R_I$ , which means  $36$  k $\Omega$  is used for  $R_F$ . The gain is determined by [Equation 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

### 8.2.1.3 Application Curve

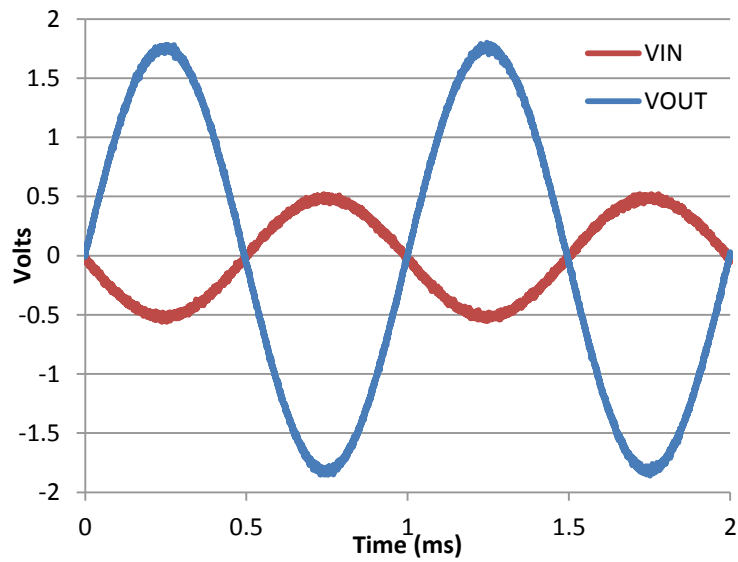


Figure 8-2. Input and Output Voltages of the Inverting Amplifier

## 8.3 Power Supply Recommendations

### CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of  $\pm 18$  V for a dual-supply can permanently damage the device (see [Section 5.1](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Section 8.4](#).

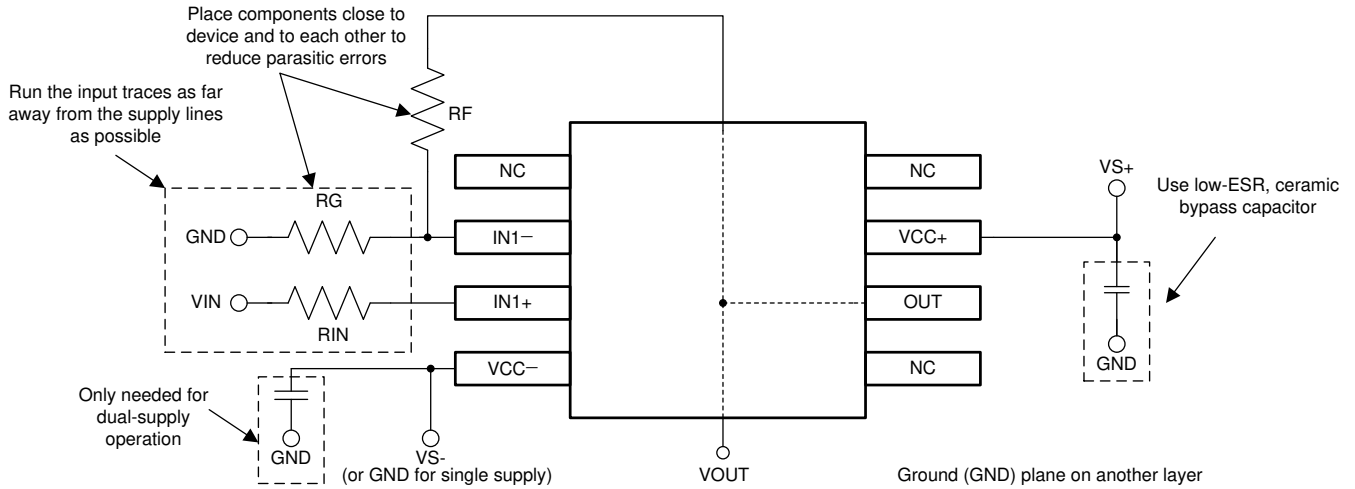
## 8.4 Layout

### 8.4.1 Layout Guidelines

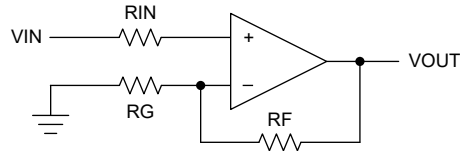
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V_{CC+}$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible, then better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance; see also [Section 8.4.2](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 8.4.2 Layout Example



**Figure 8-3. Operational Amplifier Board Layout for Noninverting Configuration**



**Figure 8-4. Operational Amplifier Schematic for Noninverting Configuration**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Device Nomenclature

**Table 9-1. Device Nomenclature**

PART NUMBER	DEFINITION
TL07xyzzzzzz	x is the channel count
	If y = H, the die is manufactured on the latest flow (CSO: RFB). Section 5.7 and Section 5.10 describe the performance of the new die.
	If y ≠ H and y ≠ M, the die is manufactured on the legacy flow (CSO: SFAB) or the latest flow (CSO: RFB). Section 5.8, Section 5.9, and Section 5.11 describe the performance of the original die. Section 5.7 and Section 5.10 describe the performance of the new die.
	If y = M, the device is specified for the extended temperature range of –55°C to +125°C. The die is manufactured on the legacy flow (CSO:SFAB). The letters and numbers represented by z are grade-out and package options described in Section 5.8 and the <i>Package Option Addendum</i> at the end of this data sheet.

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
 All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision V (April 2023) to Revision W (July 2025)	Page
• Deleted references to trim function from all packages except PS (SO, 8) package.....	1
• Changed $V_n$ from $18nV/\sqrt{Hz}$ to $37nV/\sqrt{Hz}$ in <i>Features</i> .....	1
• Updated <i>Device Information</i> table to match <i>Package Option Addendum</i> .....	1
• Updated front page image to show which device uses the PS package only.....	1
• Updated <i>Pin Configuration and Functions</i> to show that only PS package (PDIP, 8) has trim function.....	3

• Added note regarding old and new dies.....	10
• Deleted Figure 5-19, <i>THD+N Ratio vs Frequency</i> and Figure 5-20, <i>THD+N vs Output Amplitude</i> .....	17
• Added "for PS Package (SO, 8) Only" to Figure 7-3 caption.....	28
• Deleted <i>Unity Gain Buffer</i> and <i>System Examples</i> sections.....	30
• Deleted Equation 1 from <i>Detailed Design Procedure</i> .....	30
• Deleted "This ensures the part does not draw too much current." from <i>Detailed Design Procedure</i> .....	30
• Added <i>Device Nomenclature</i> table.....	34

<b>Changes from Revision U (December 2022) to Revision V (April 2023)</b>	<b>Page</b>
• Updated <i>Overview</i> , <i>Functional Block Diagram</i> , and <i>Feature Description</i> sections .....	29

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">81023052A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023052A TL072MFKB
<a href="#">8102305HA</a>	Active	Production	CFP (U)   10	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305HA TL072M
<a href="#">8102305PA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305PA TL072M
<a href="#">81023062A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023062A TL074MFKB
<a href="#">8102306CA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306CA TL074MJB
<a href="#">8102306DA</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306DA TL074MWB
<a href="#">JM38510/11905BPA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11905BPA
JM38510/11905BPA.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11905BPA
<a href="#">M38510/11905BPA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11905BPA
<a href="#">TL071ACDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC
TL071ACDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC
<a href="#">TL071ACP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071ACP
TL071ACP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071ACP
<a href="#">TL071BCDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC
TL071BCDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC
<a href="#">TL071BCP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071BCP
TL071BCP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071BCP
<a href="#">TL071CDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C
TL071CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C
TL071CDRE4	Active	Production	SOIC (D)   8	2500   LARGE T&R	-	Call TI	Call TI	0 to 70	
TL071CDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	-	Call TI	Call TI	0 to 70	
<a href="#">TL071CP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071CP

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL071CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071CP
TL071CPE4	Active	Production	PDIP (P)   8	50   TUBE	-	Call TI	Call TI	0 to 70	
<a href="#">TL071CPSR</a>	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071
TL071CPSR.A	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071
<a href="#">TL071HIDBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V
<a href="#">TL071HIDCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IO
TL071HIDCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IO
<a href="#">TL071HIDR</a>	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL071D
TL071HIDR.A	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL071D
<a href="#">TL071IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDR1G4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDR1G4.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	-	Call TI	Call TI	-40 to 85	
<a href="#">TL071IP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL071IP
TL071IP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL071IP
<a href="#">TL072ACDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDRE4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
<a href="#">TL072ACP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072ACP
TL072ACP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072ACP
TL072ACPE4	Active	Production	PDIP (P)   8	50   TUBE	-	Call TI	Call TI	0 to 70	
TL072ACPS	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072A
TL072ACPS.A	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072A
<a href="#">TL072BCD</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	0 to 70	072BC
<a href="#">TL072BCDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC
TL072BCDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TL072BCP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072BCP
TL072BCP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072BCP
<a href="#">TL072CDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
<a href="#">TL072CP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072CP
TL072CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072CP
<a href="#">TL072CPS</a>	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPS.A	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
<a href="#">TL072CPSR</a>	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSR.A	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSRG4	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
<a href="#">TL072CPWR</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWR.A	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWRE4	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	-	Call TI	Call TI	0 to 70	
TL072CPWRG4	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	-	Call TI	Call TI	0 to 70	
<a href="#">TL072HIDDFR</a>	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F
TL072HIDDFR.A	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F
<a href="#">TL072HIDR</a>	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072D
TL072HIDR.A	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072D
<a href="#">TL072HIPWR</a>	Active	Production	TSSOP (PW)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	072HPW
TL072HIPWR.A	Active	Production	TSSOP (PW)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	072HPW
<a href="#">TL072IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
TL072IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
<a href="#">TL072IP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL072IP
TL072IP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL072IP
TL072IPE4	Active	Production	PDIP (P)   8	50   TUBE	-	Call TI	Call TI	-40 to 85	
<a href="#">TL072MFKB</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023052A TL072MFKB
TL072MFKB.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023052A TL072MFKB
<a href="#">TL072MJG</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL072MJG

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL072MJG.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL072MJG
<a href="#">TL072MJGB</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305PA TL072M
TL072MJGB.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305PA TL072M
<a href="#">TL072MUB</a>	Active	Production	CFP (U)   10	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305HA TL072M
TL072MUB.A	Active	Production	CFP (U)   10	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305HA TL072M
<a href="#">TL074ACD</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	TL074AC
<a href="#">TL074ACDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
<a href="#">TL074ACN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074ACN
TL074ACN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074ACN
<a href="#">TL074ACNSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A
TL074ACNSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A
<a href="#">TL074BCD</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	TL074BC
<a href="#">TL074BCDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDRE4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
<a href="#">TL074BCN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074BCN
TL074BCN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074BCN
<a href="#">TL074CD</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	TL074C
<a href="#">TL074CDBR</a>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CDBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
<a href="#">TL074CDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
<a href="#">TL074CDRG4</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
<a href="#">TL074CN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074CN
TL074CN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074CN

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TL074CNSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074
TL074CNSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074
<a href="#">TL074CPW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	0 to 70	T074
<a href="#">TL074CPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWRE4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
<a href="#">TL074HIDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
<a href="#">TL074HIDYYR</a>	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY
TL074HIDYYR.A	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY
<a href="#">TL074HIPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074PW
TL074HIPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074PW
<a href="#">TL074ID</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	TL074I
<a href="#">TL074IDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDRE4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
<a href="#">TL074IN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN
TL074IN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN
TL074ING4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN
TL074ING4.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN
<a href="#">TL074MFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MFK
TL074MFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MFK
TL074MFKB	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023062A TL074MFKB
TL074MFKB.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023062A TL074MFKB

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TL074MJ</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MJ
TL074MJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MJ
<a href="#">TL074MJB</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306CA TL074MJB
TL074MJB.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306CA TL074MJB
<a href="#">TL074MWB</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306DA TL074MWB
TL074MWB.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306DA TL074MWB

**(1) Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

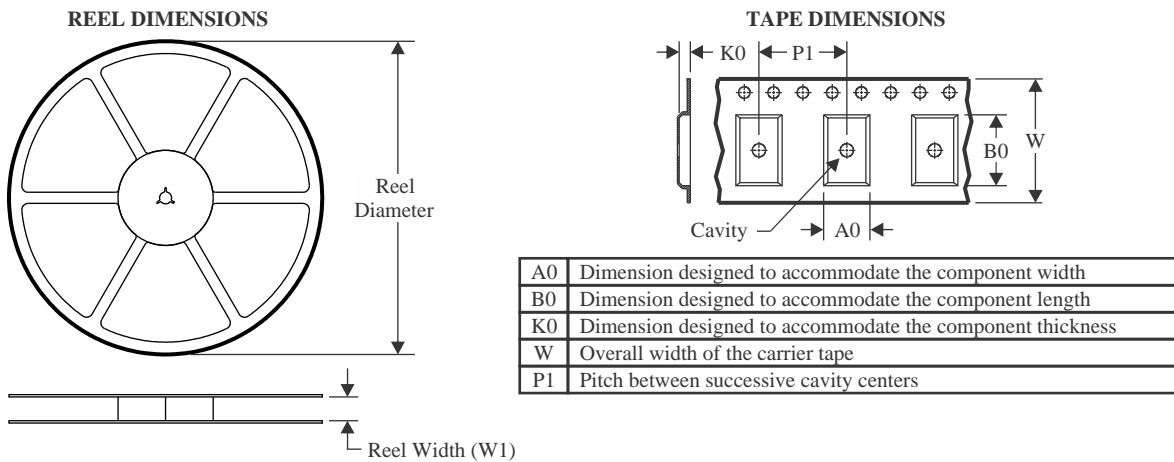
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :**

- Catalog : [TL072](#), [TL074](#)
- Enhanced Product : [TL072-EP](#), [TL072-EP](#), [TL074-EP](#), [TL074-EP](#)
- Military : [TL072M](#), [TL074M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL071HIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL071HIDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL071HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL071HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

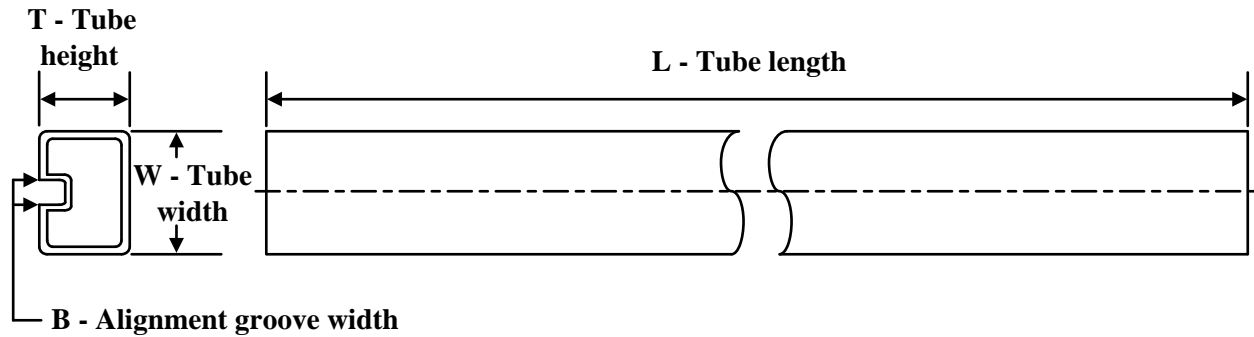
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL072HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072HIDR	SOIC	D	8	3000	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
TL072HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
TL074HIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL074HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL071CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL071HIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL071HIDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL071HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL071HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL071IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL071IDR1G4	SOIC	D	8	2500	353.0	353.0	32.0
TL072ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL072CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL072HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL072HIDR	SOIC	D	8	3000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL072HIPWR	TSSOP	PW	8	3000	353.0	353.0	32.0
TL072IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL074ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074ACNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL074BCDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074CDBR	SSOP	DB	14	2000	353.0	353.0	32.0
TL074CDR	SOIC	D	14	2500	367.0	367.0	35.0
TL074CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074CDRG4	SOIC	D	14	2500	340.5	336.1	32.0
TL074CNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL074CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL074CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL074HIDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074HIDR	SOIC	D	14	2500	367.0	367.0	35.0
TL074HIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL074HIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL074IDR	SOIC	D	14	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
81023052A	FK	LCCC	20	55	506.98	12.06	2030	NA
8102305HA	U	CFP	10	25	506.98	26.16	6220	NA
81023062A	FK	LCCC	20	55	506.98	12.06	2030	NA
8102306DA	W	CFP	14	25	506.98	26.16	6220	NA
TL071ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL071ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL071CP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL071IP	P	PDIP	8	50	506	13.97	11230	4.32
TL071IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072ACPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TL072BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL072BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072CP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TL072IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL072MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL072MUB	U	CFP	10	25	506.98	26.16	6220	NA
TL072MUB.A	U	CFP	10	25	506.98	26.16	6220	NA
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32

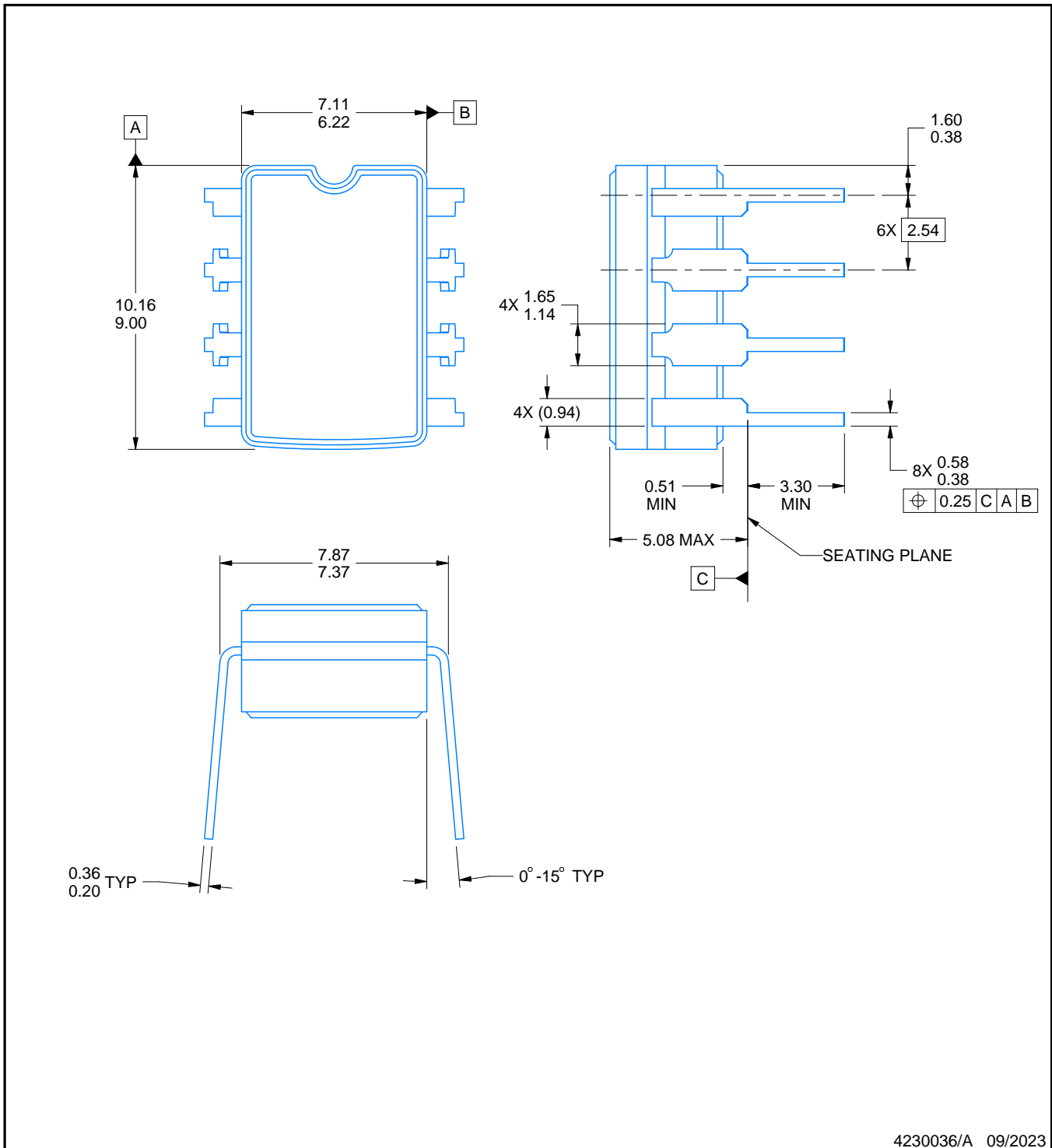
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074IN	N	PDIP	14	25	506	13.97	11230	4.32
TL074IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074ING4	N	PDIP	14	25	506	13.97	11230	4.32
TL074ING4.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MWB	W	CFP	14	25	506.98	26.16	6220	NA
TL074MWB.A	W	CFP	14	25	506.98	26.16	6220	NA

# PACKAGE OUTLINE

## JG0008A

### CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



#### NOTES:

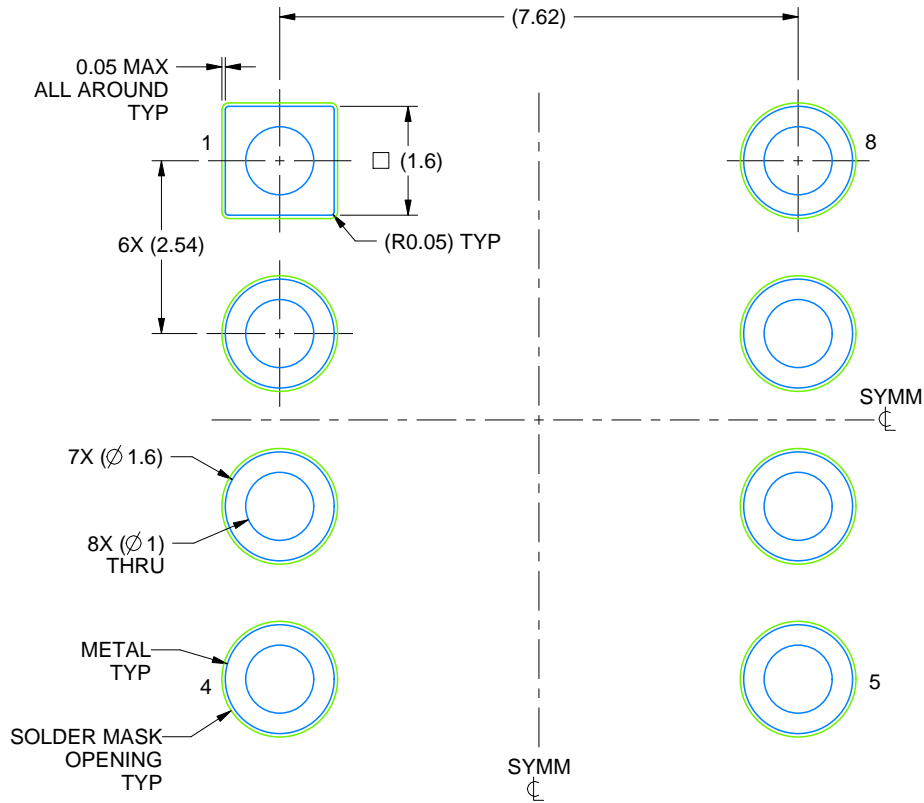
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

# EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE  
NON SOLDER MASK DEFINED  
SCALE: 9X

4230036/A 09/2023







# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

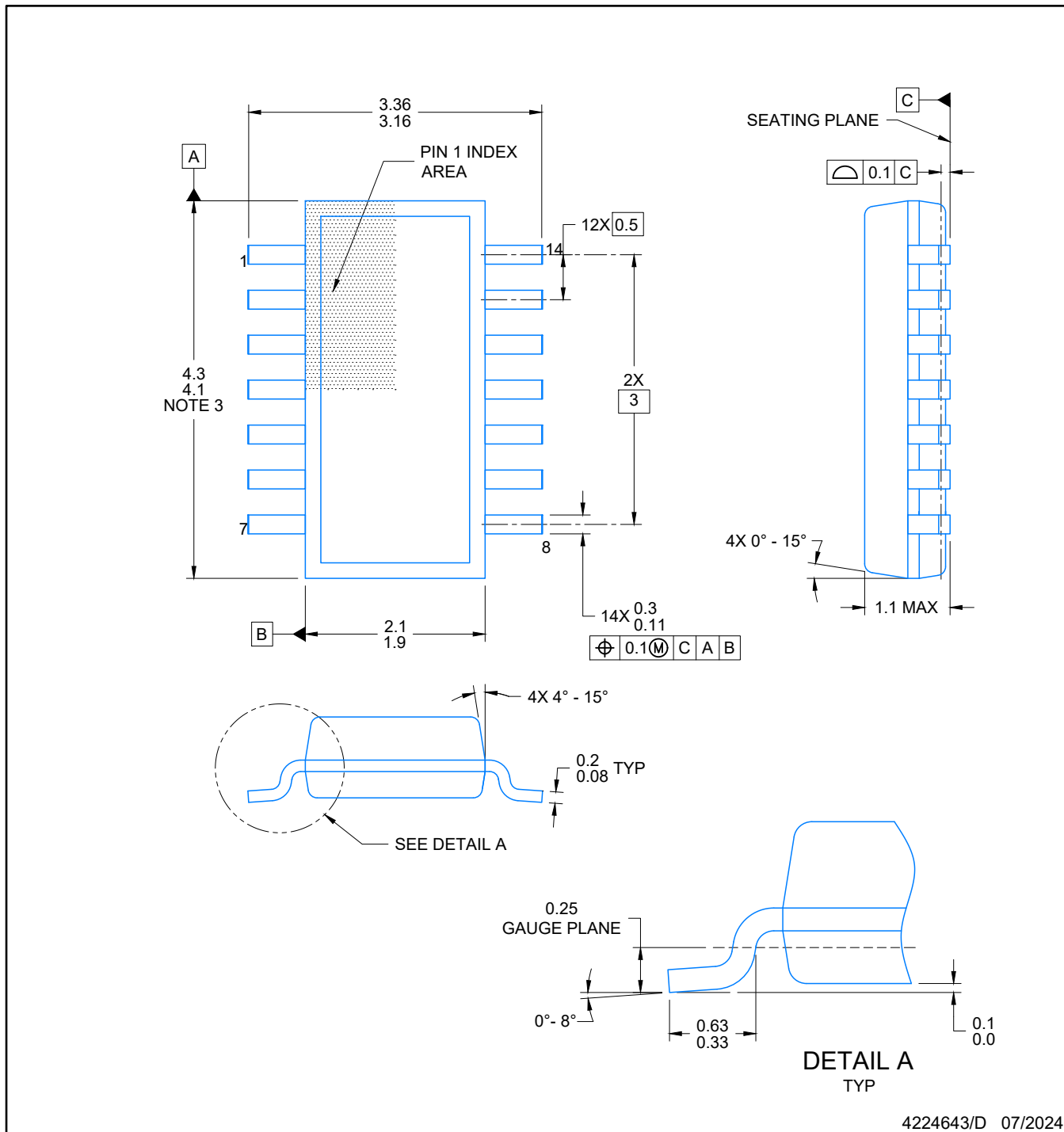


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

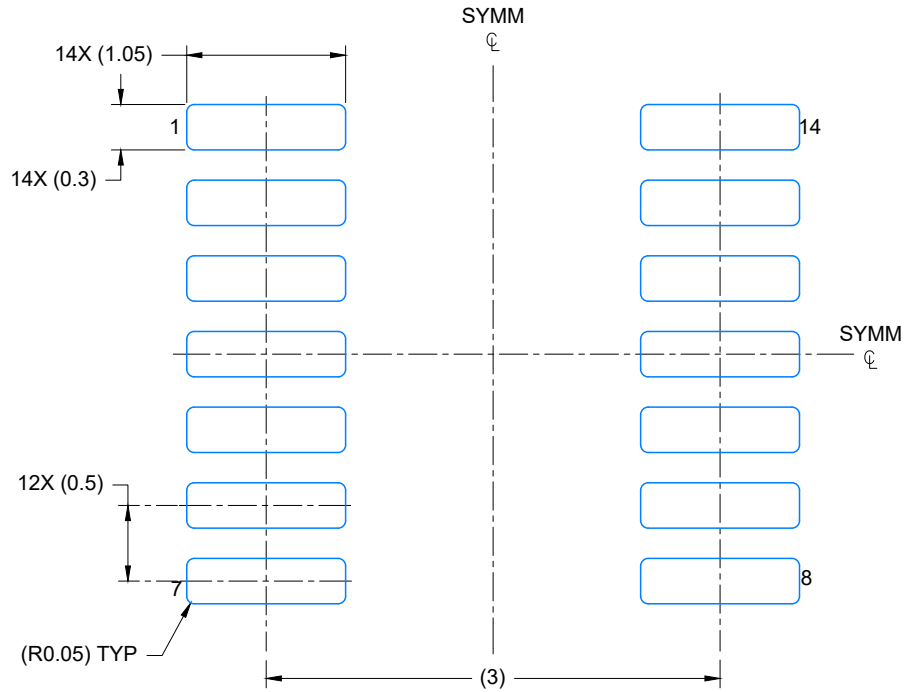
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



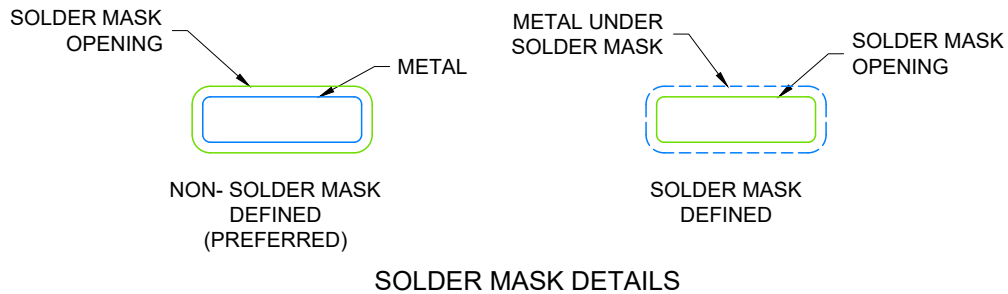
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



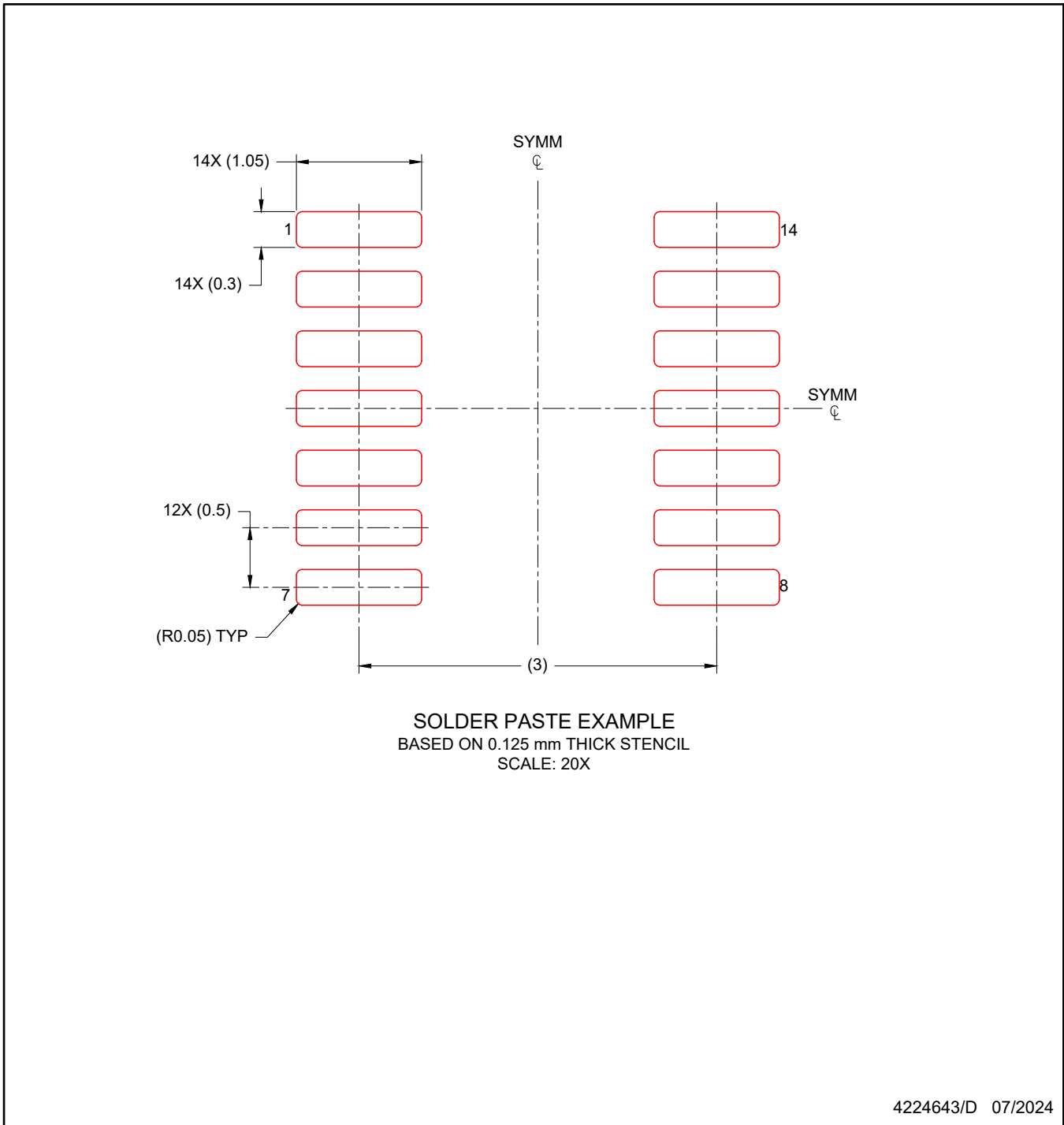
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224643/D 07/2024

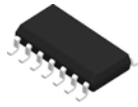
NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

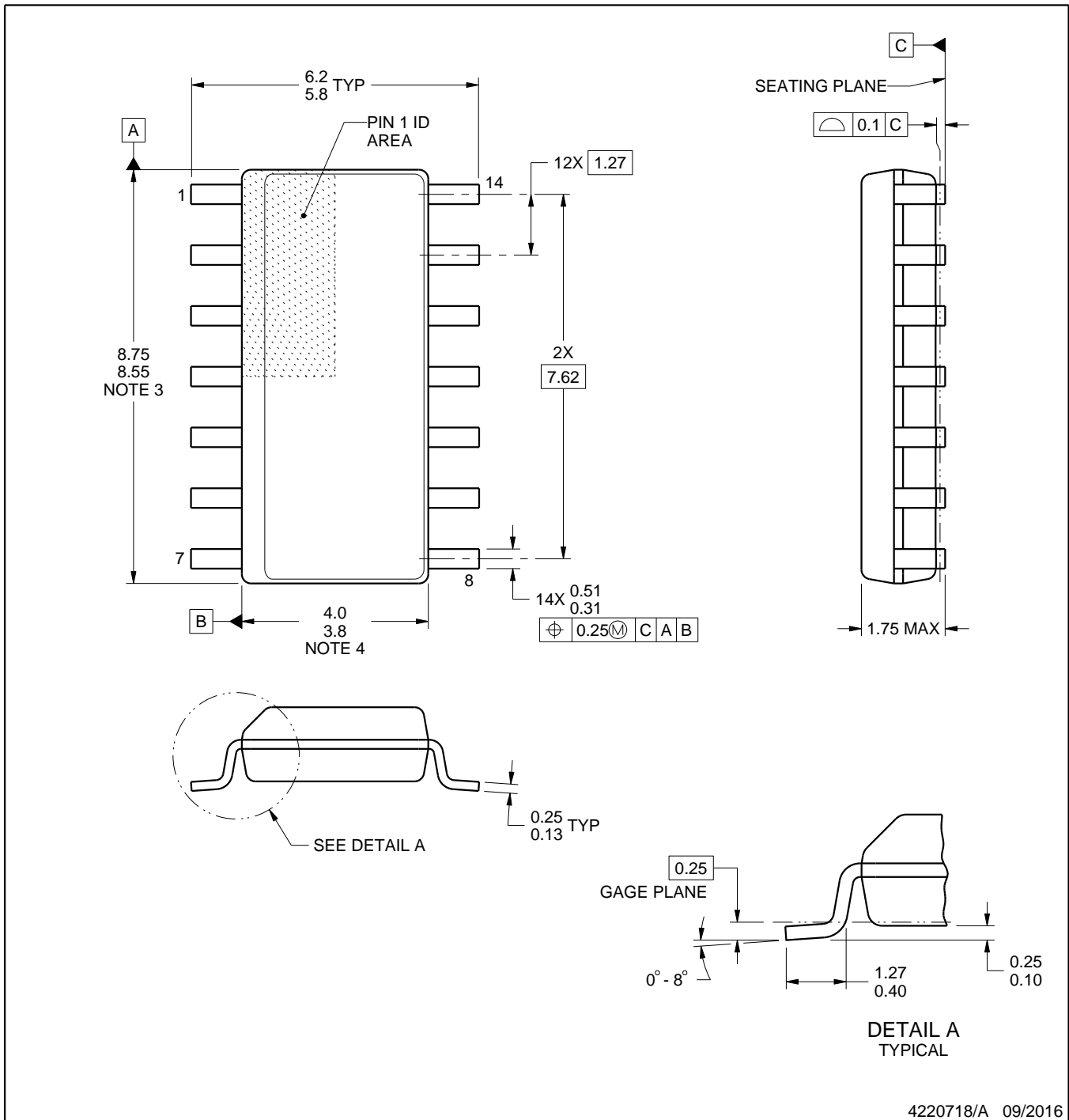


# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

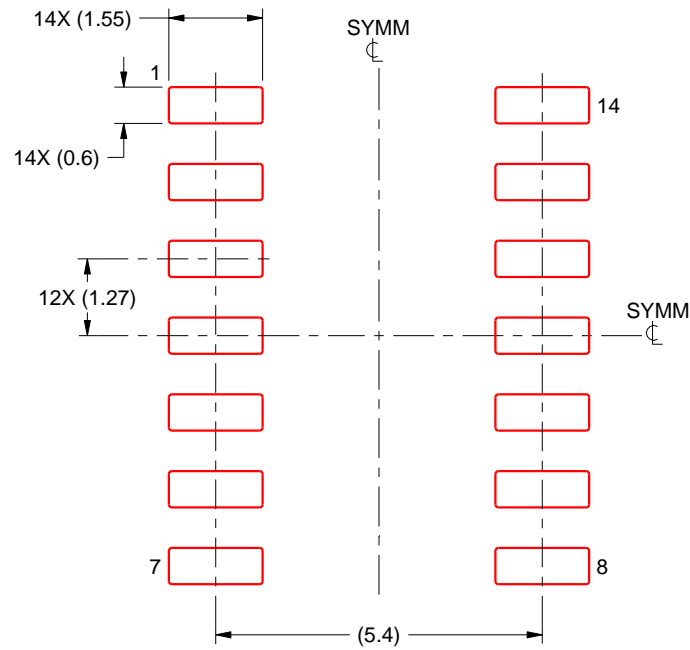
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

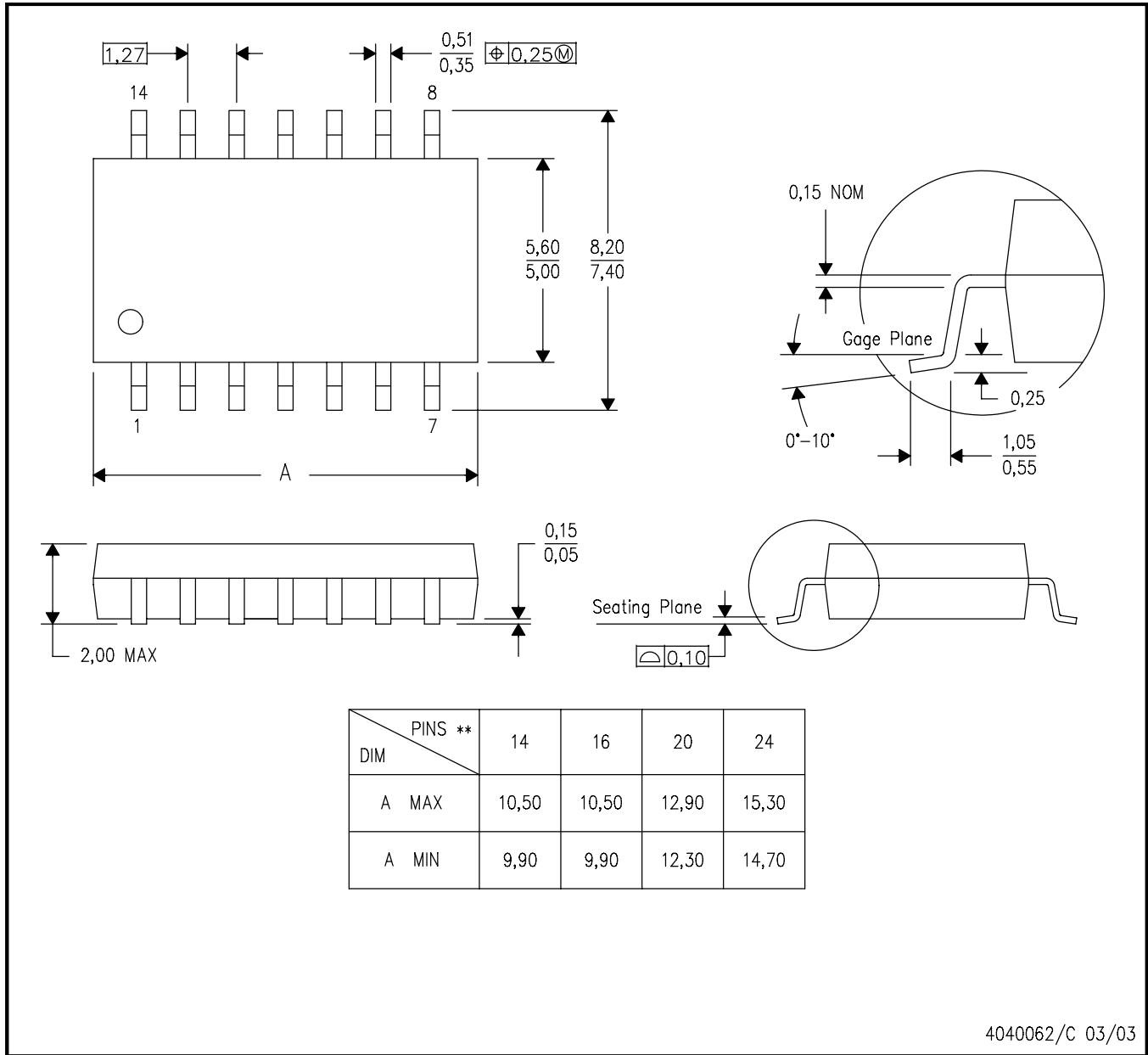
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

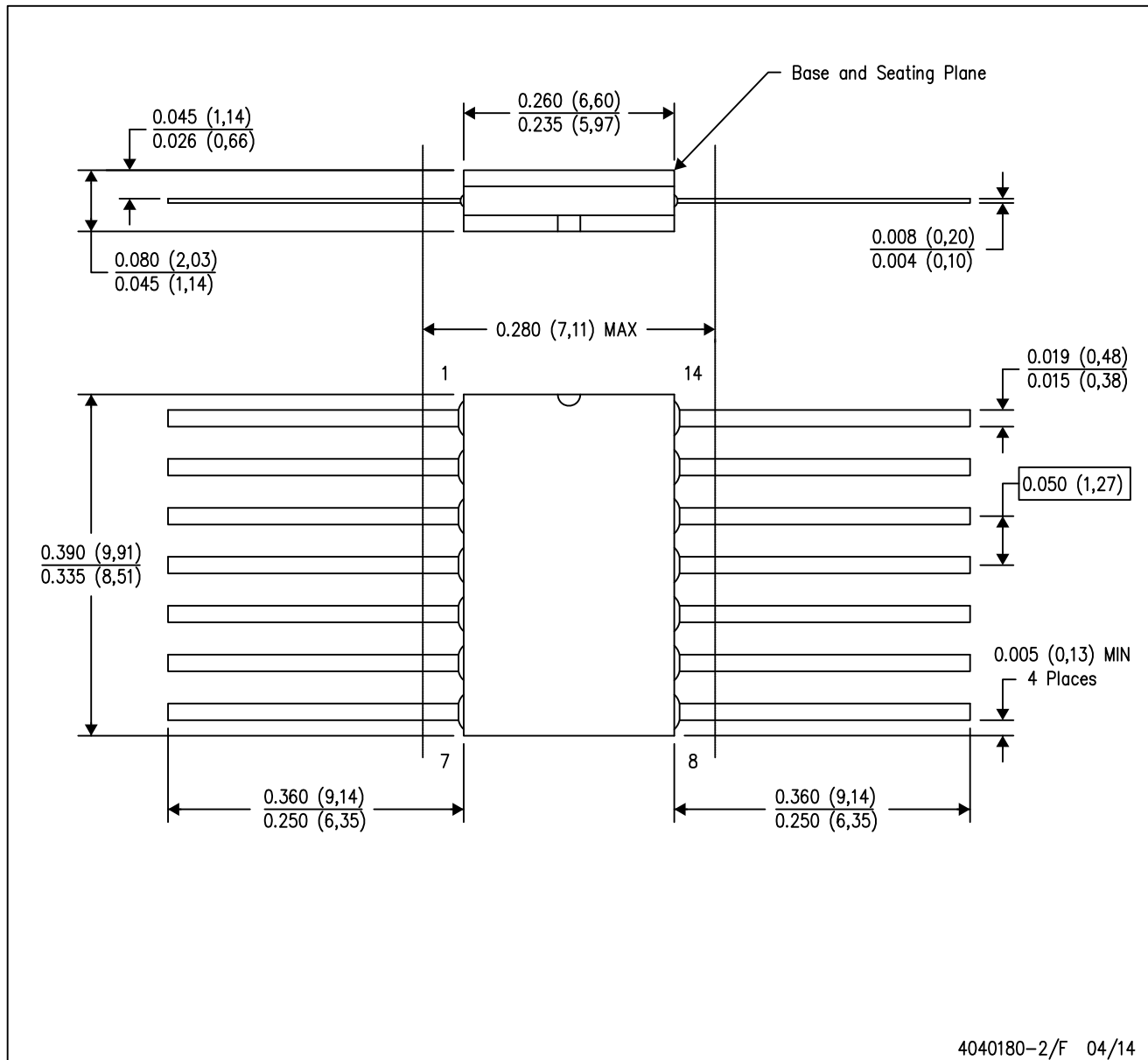
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

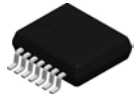
W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

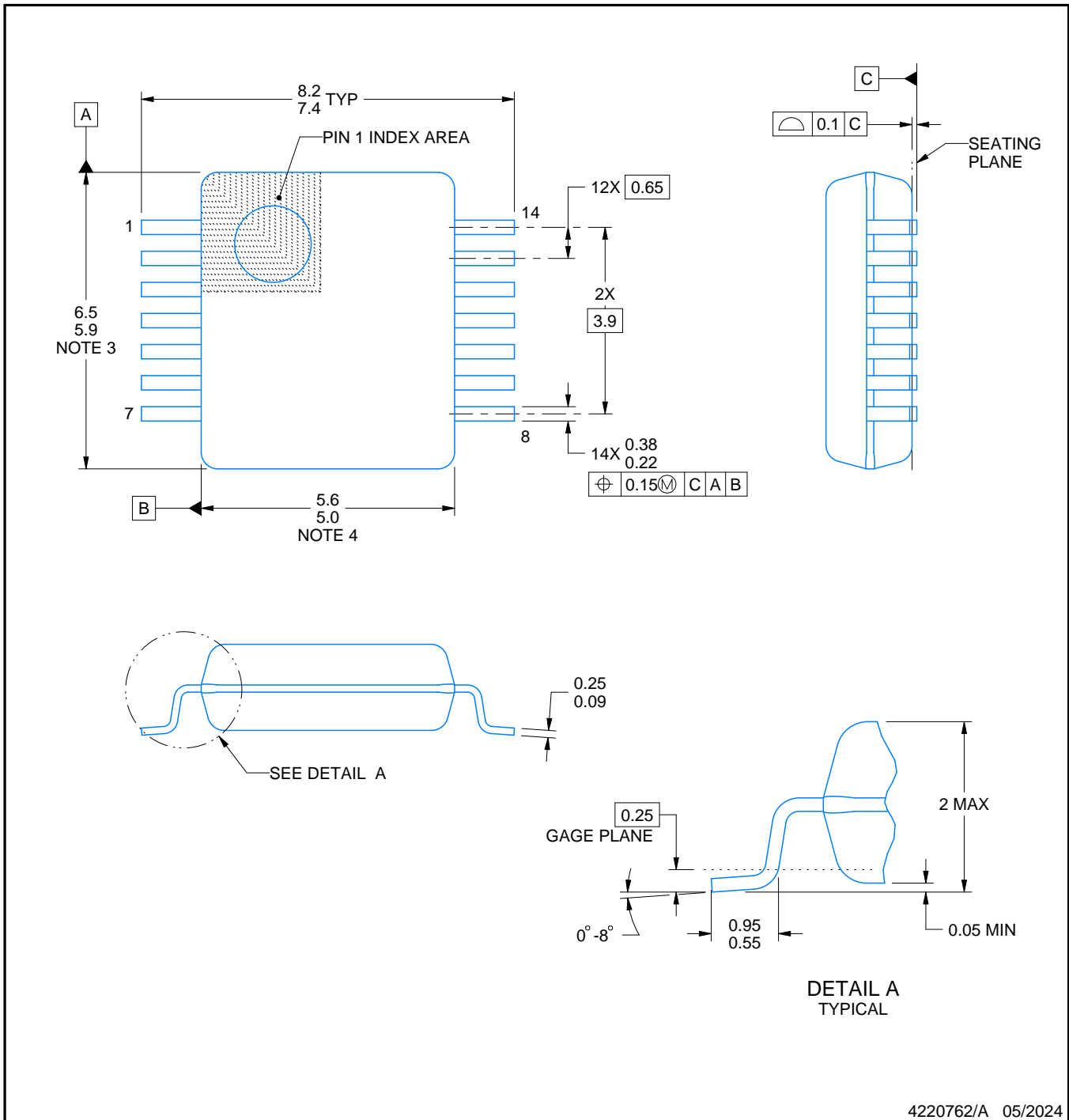
# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

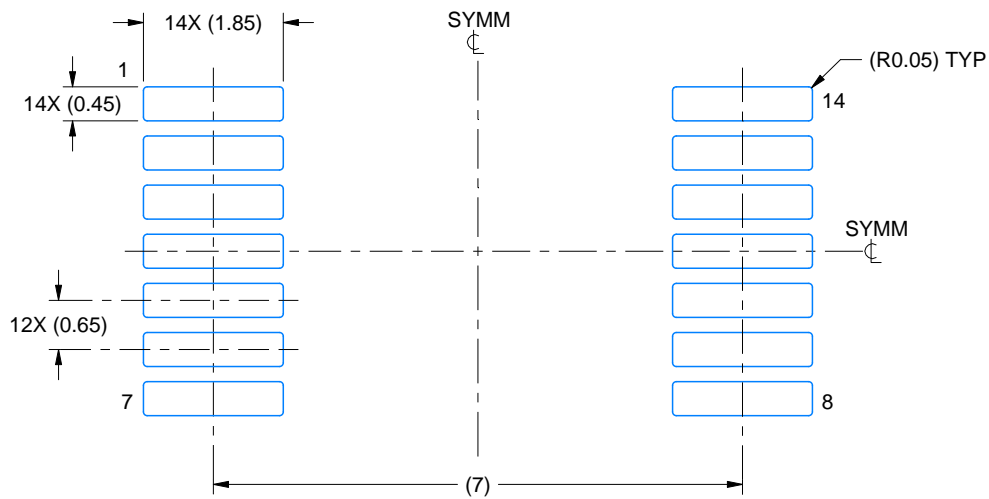
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

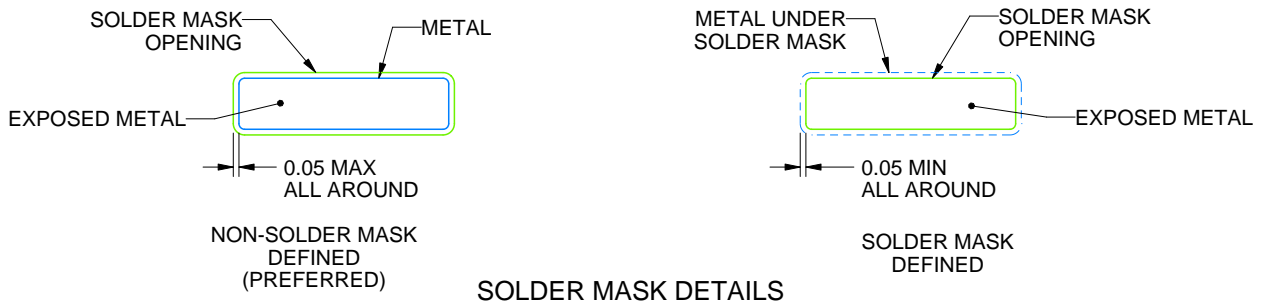
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

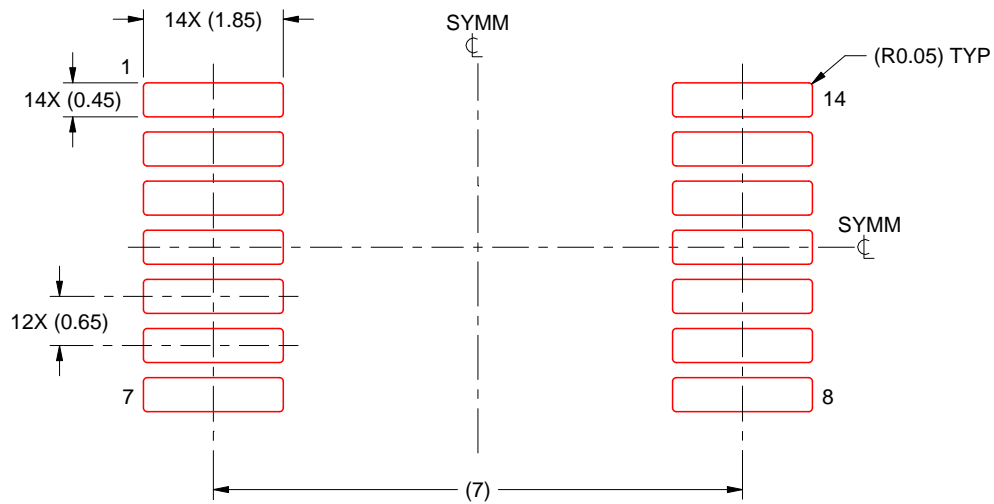
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

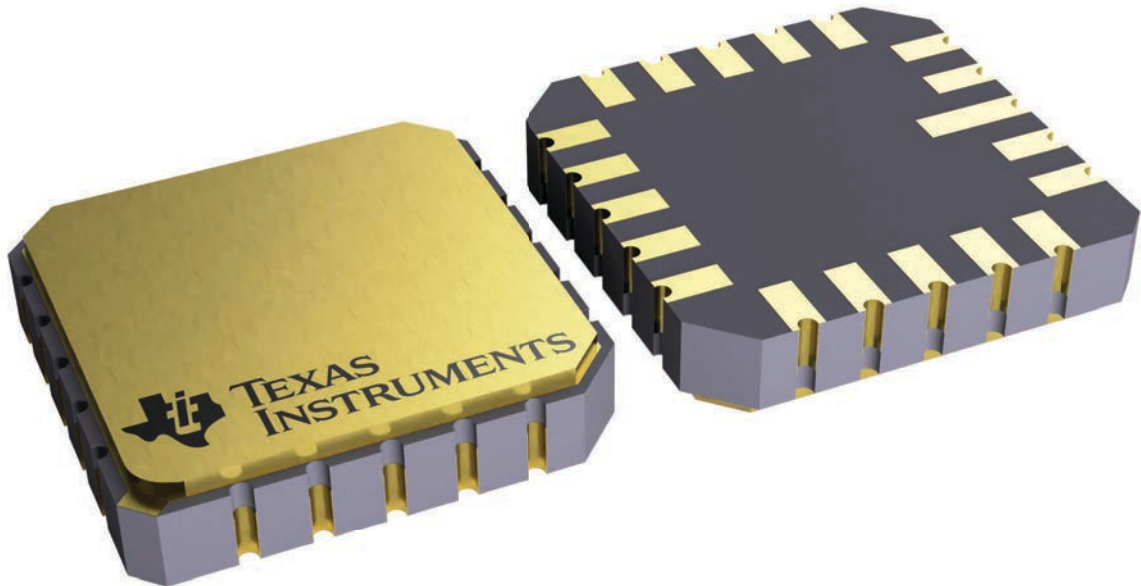
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

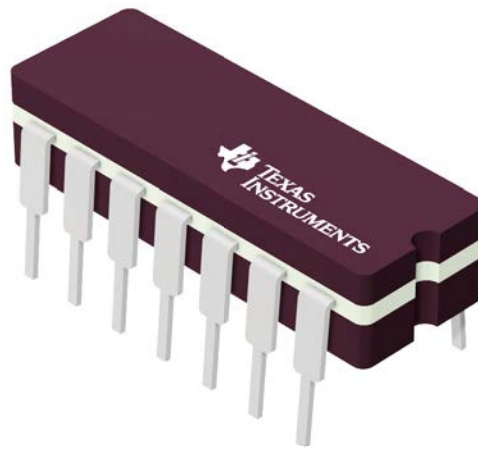
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

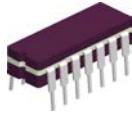
**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

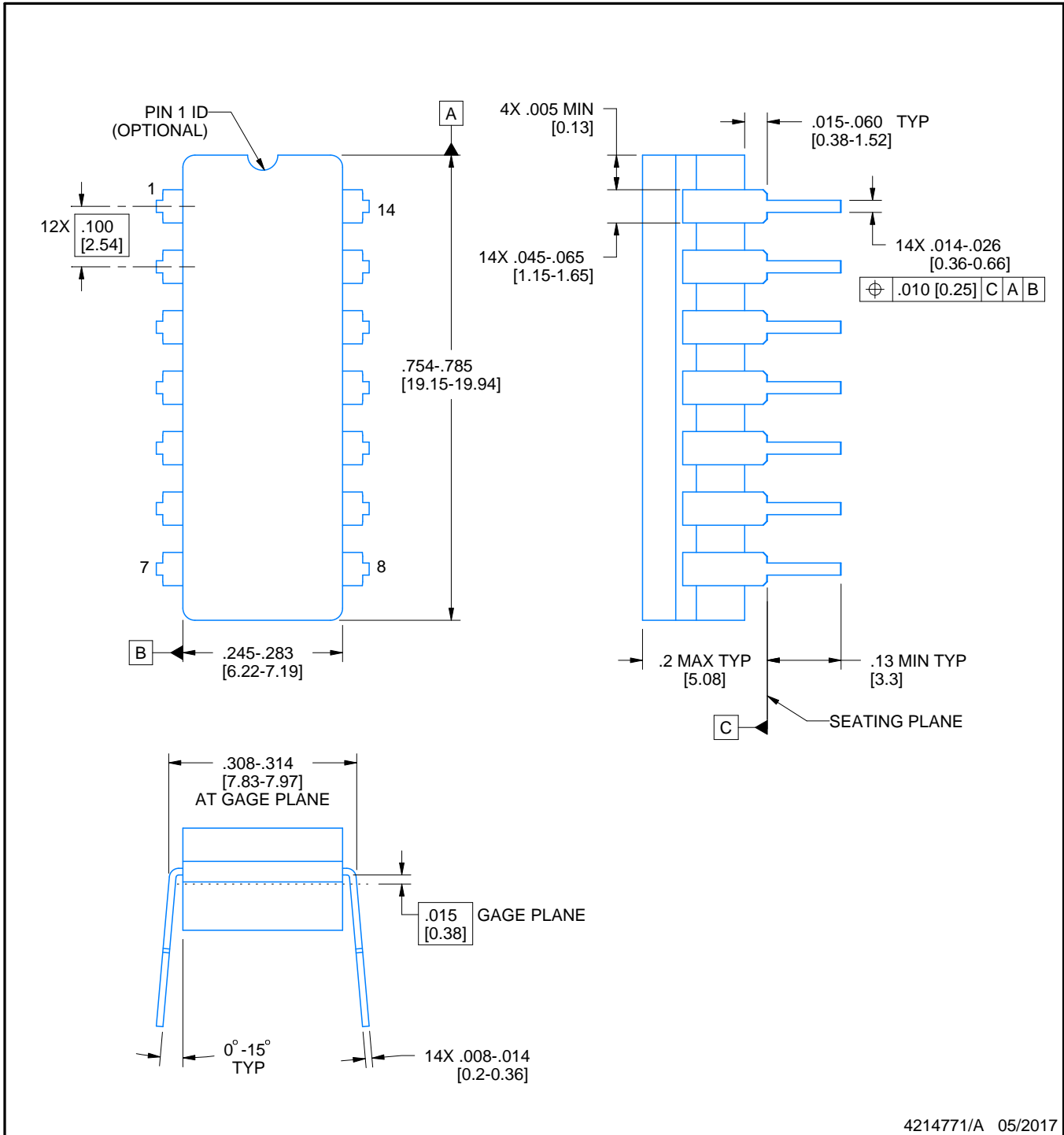
J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

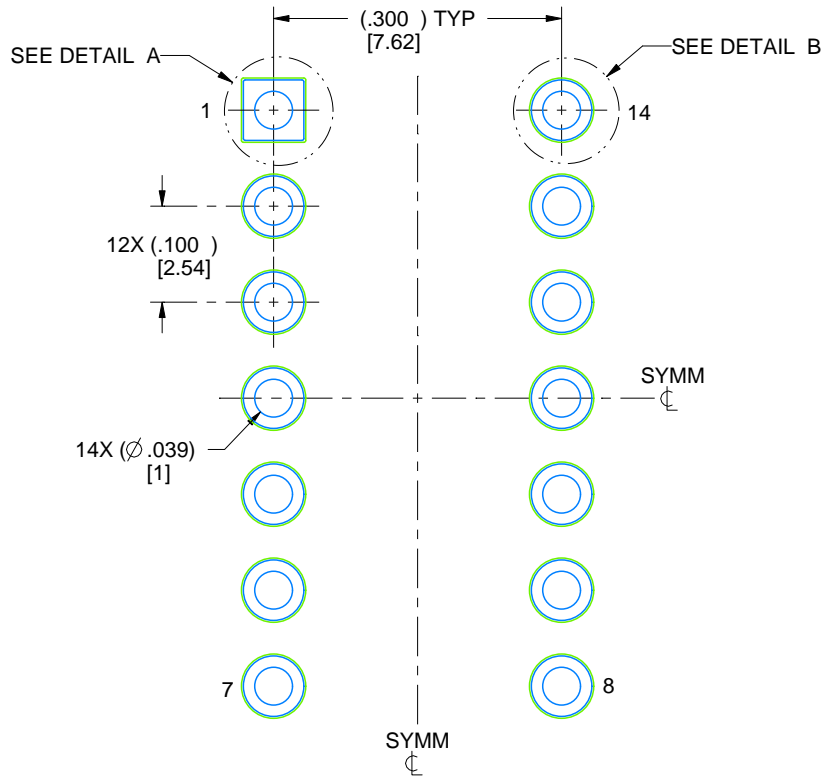
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

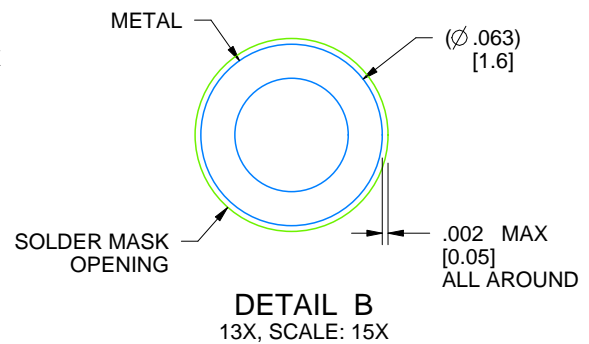
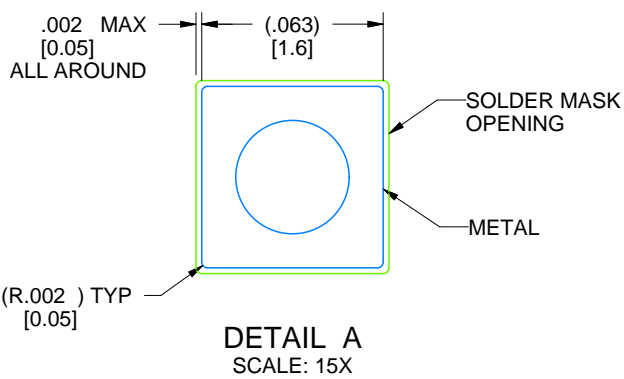
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

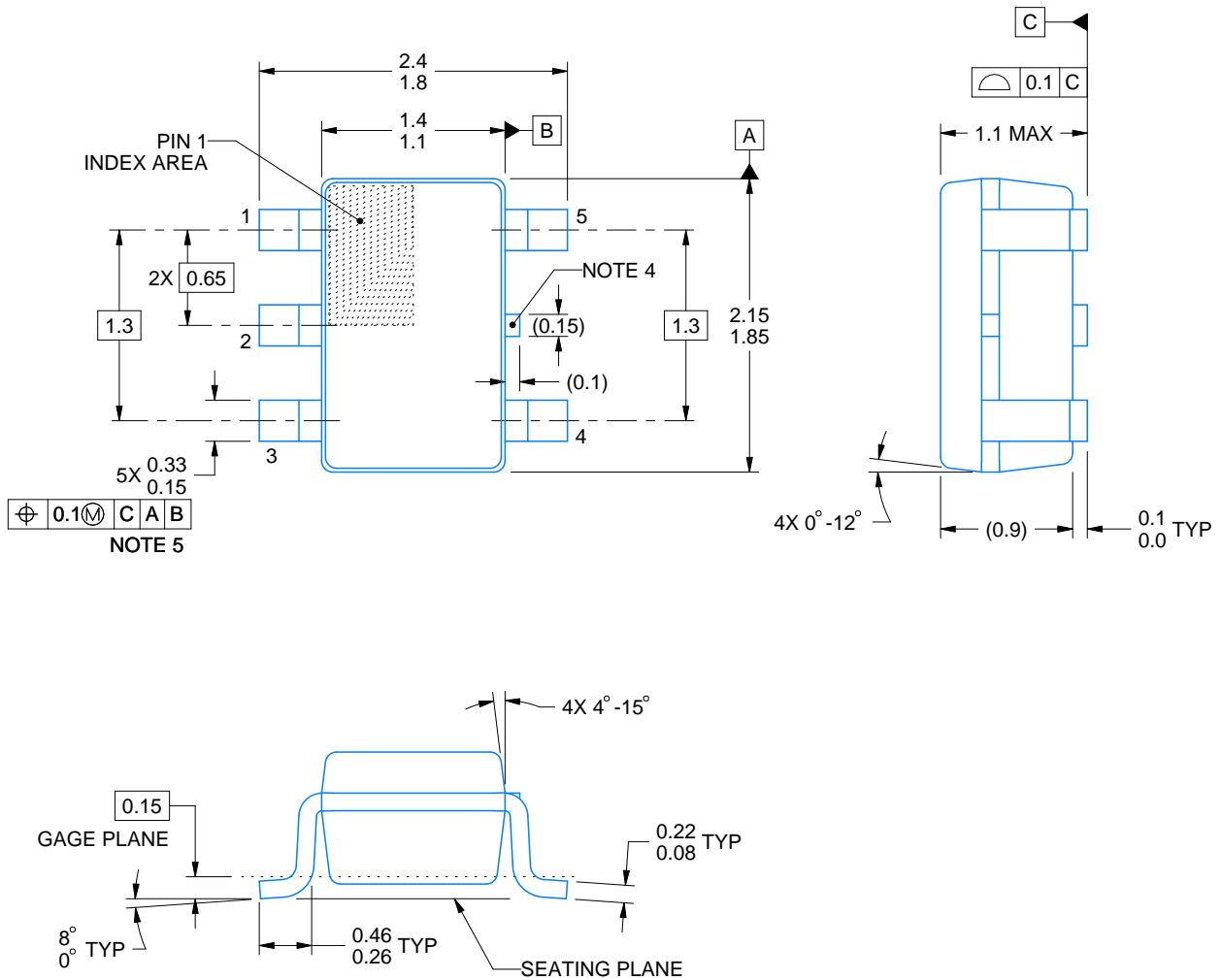
# DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

## NOTES:

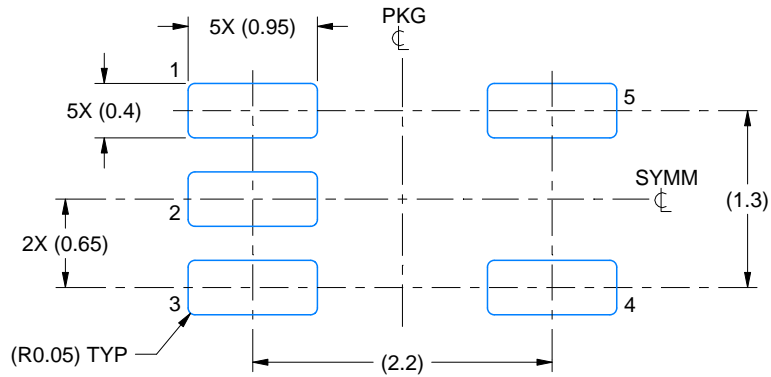
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

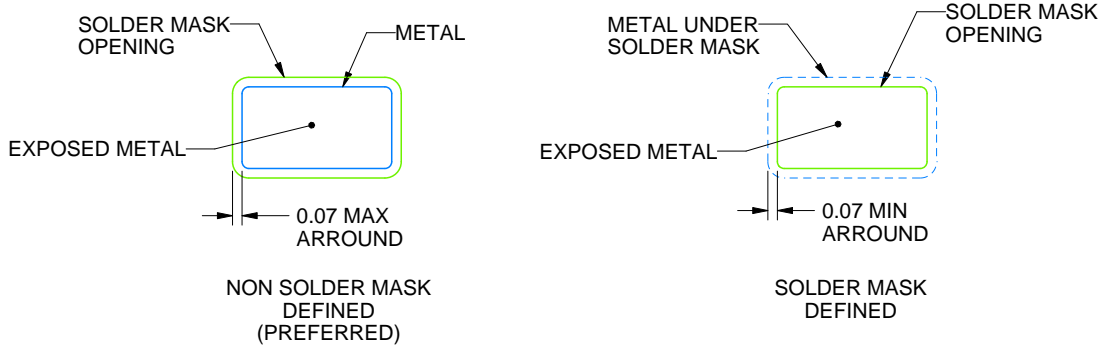
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

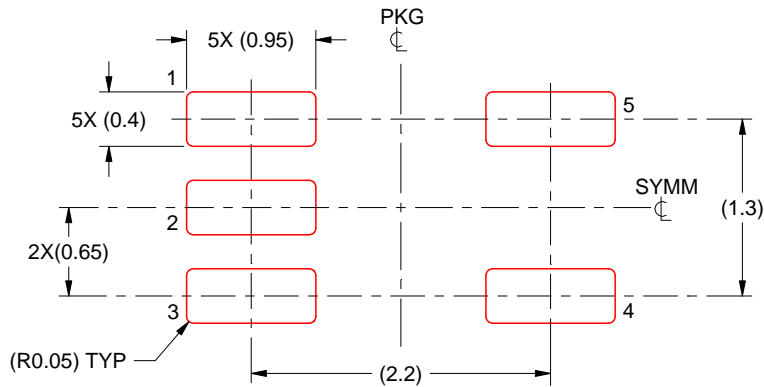
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

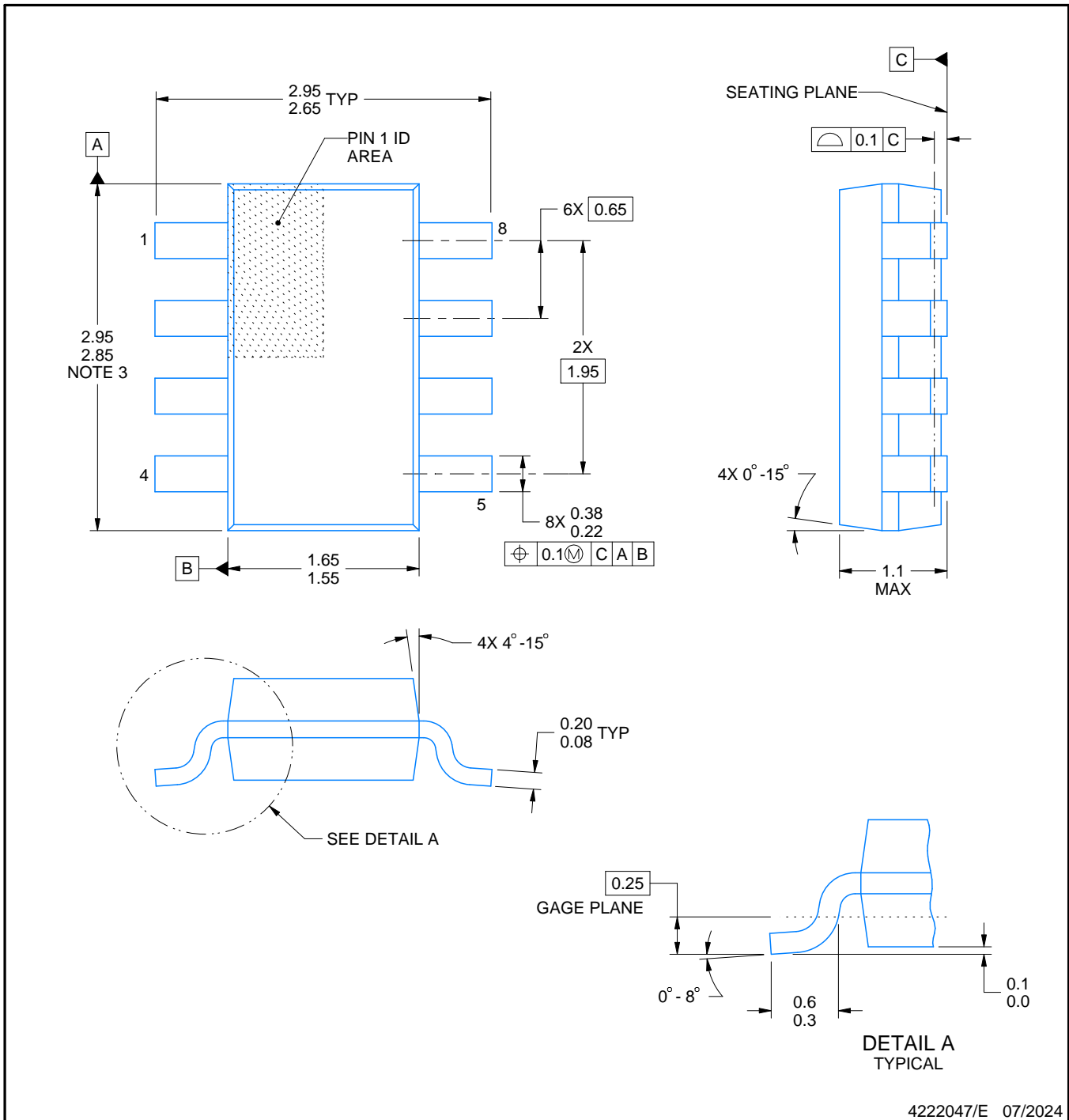
# DDF0008A



# PACKAGE OUTLINE

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



### NOTES:

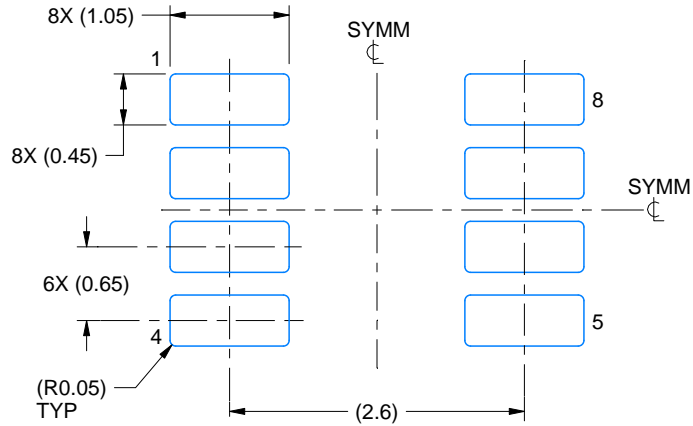
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

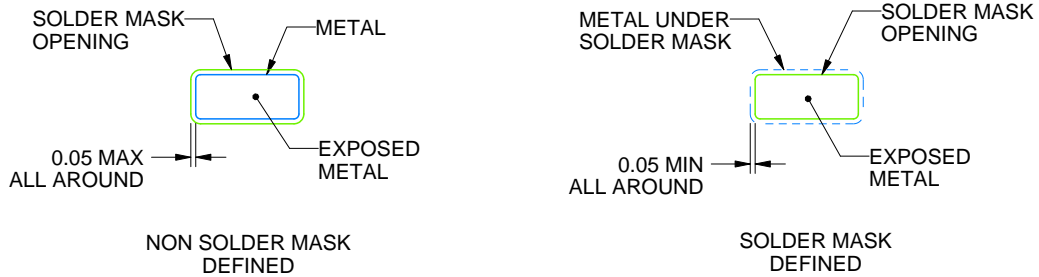
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

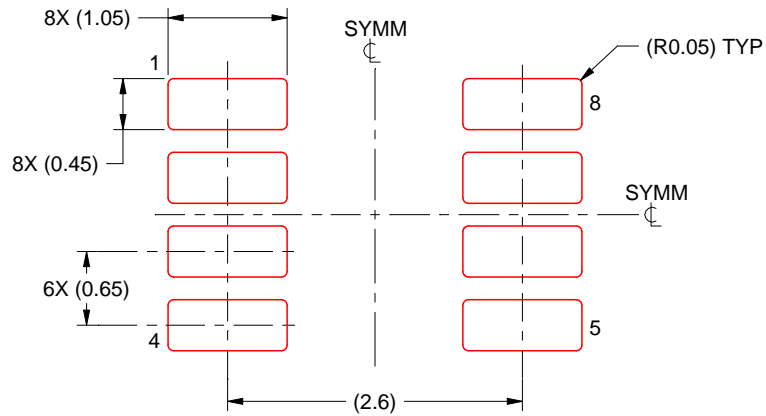
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

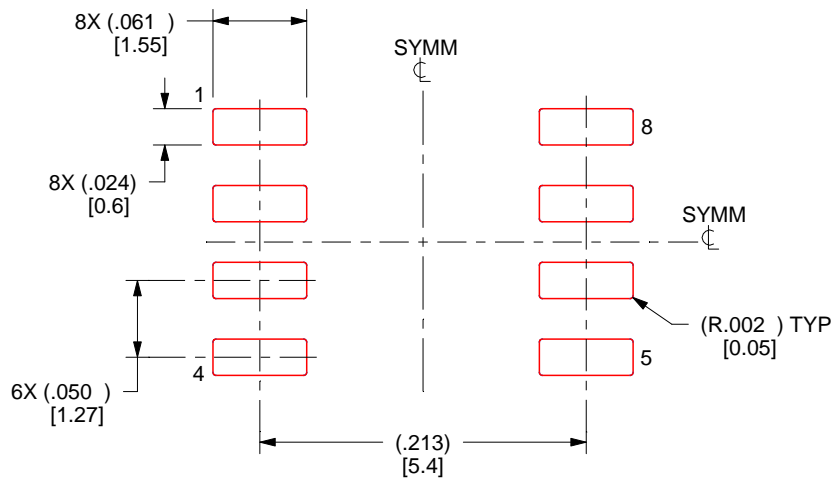
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

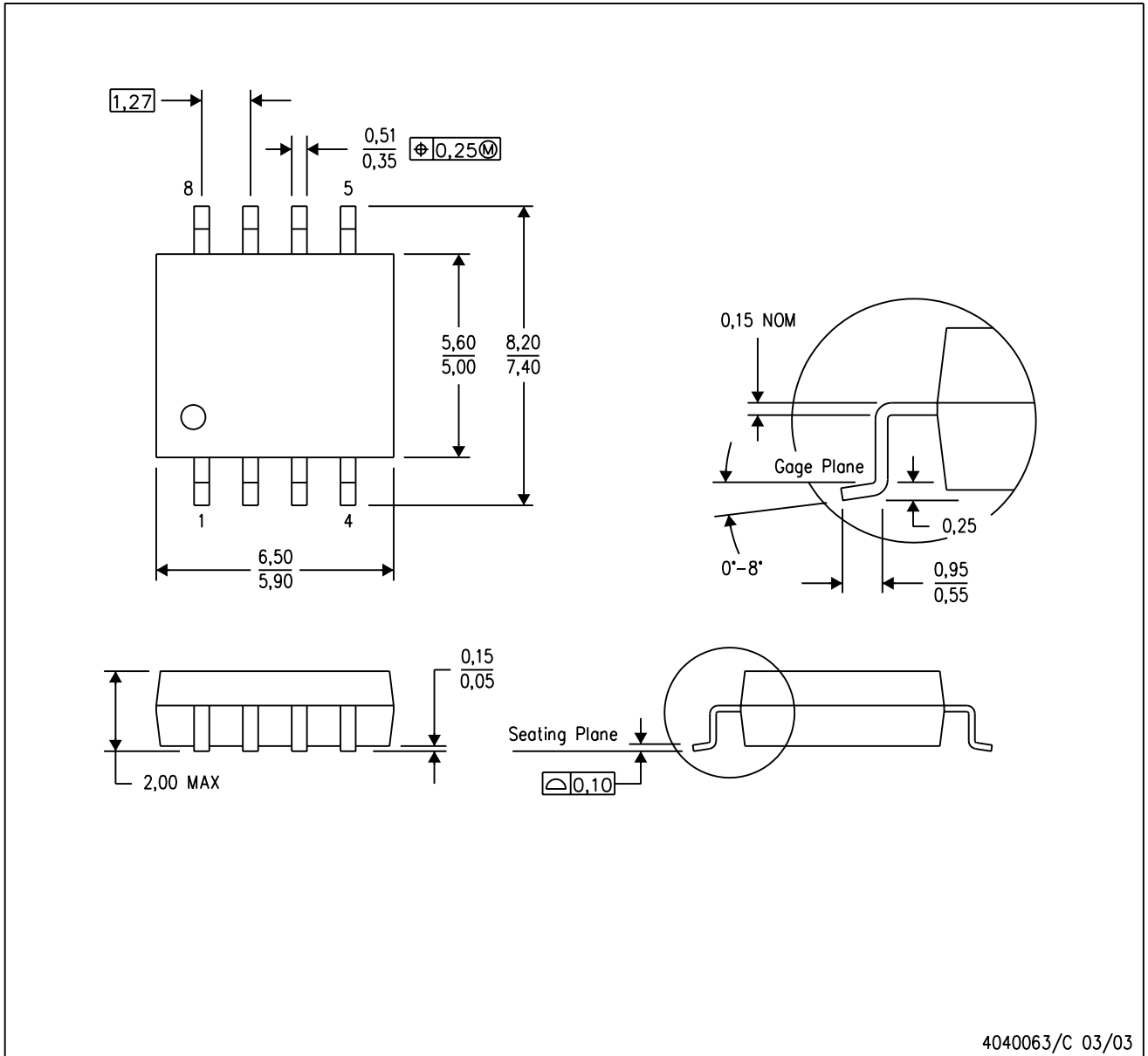
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

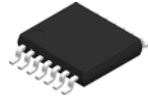
16 PINS SHOWN



4040049/E 12/2002

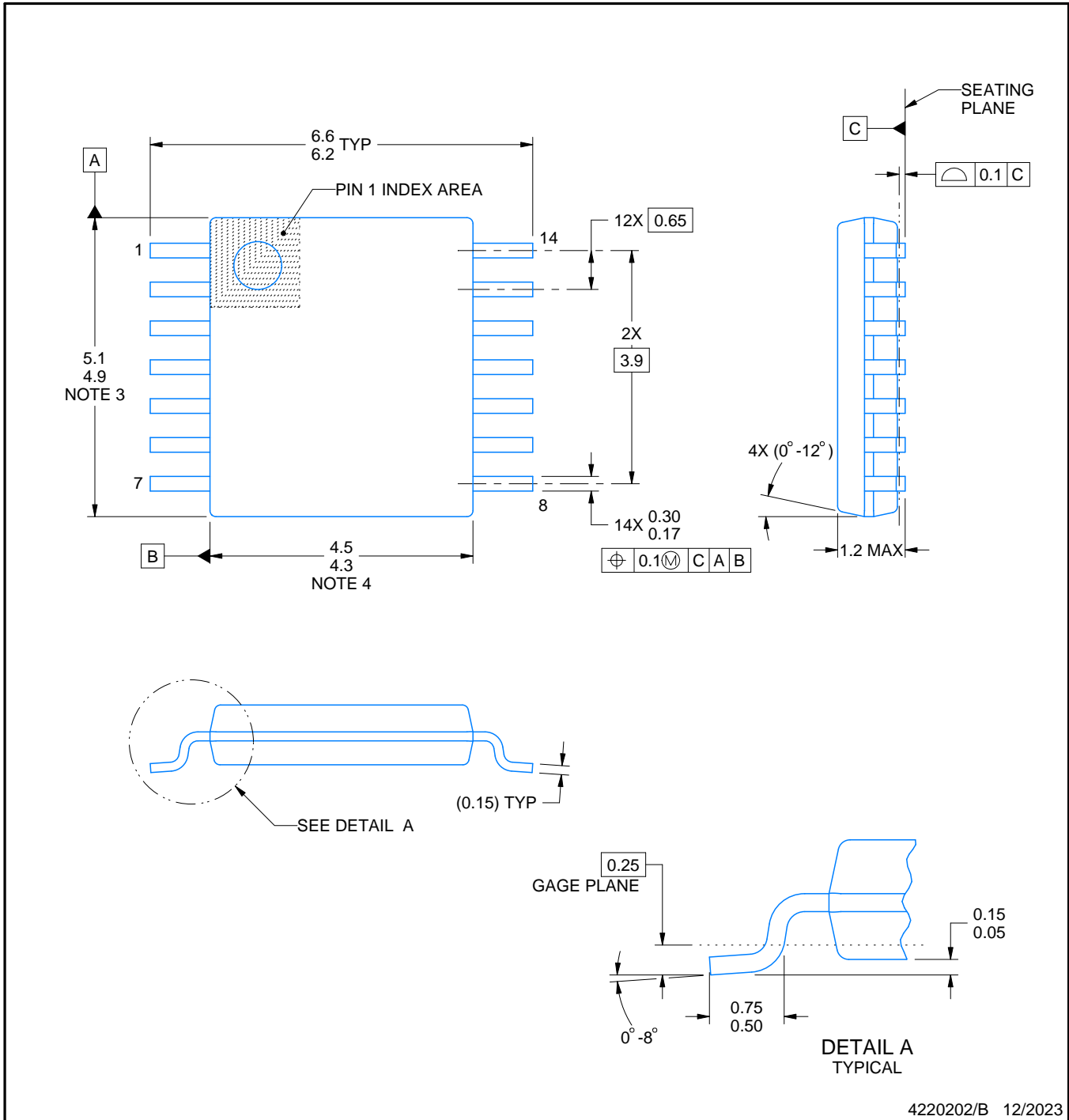
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

**NOTES:**

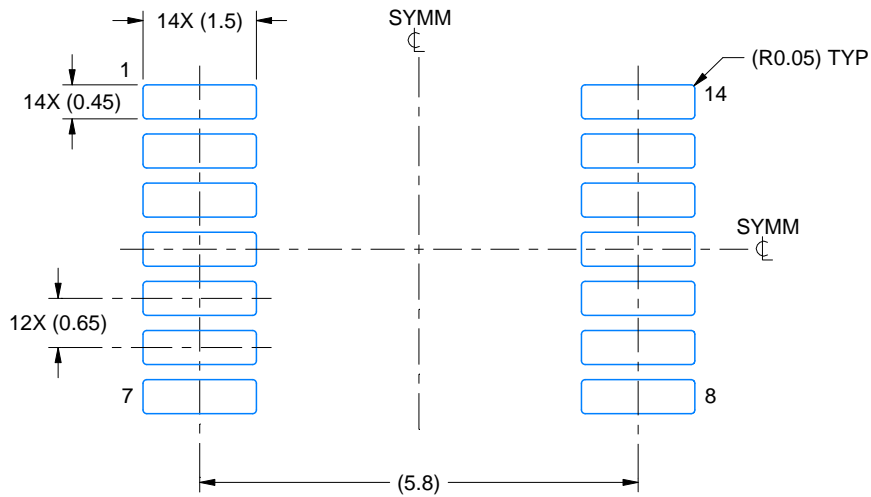
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

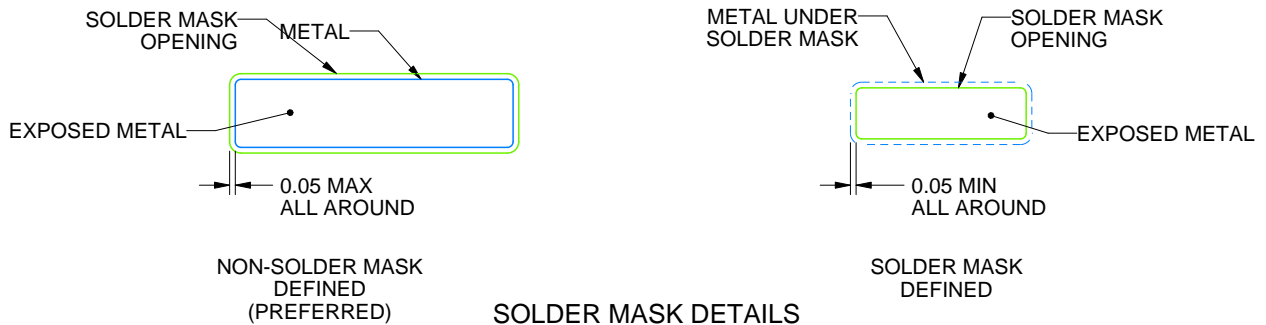
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

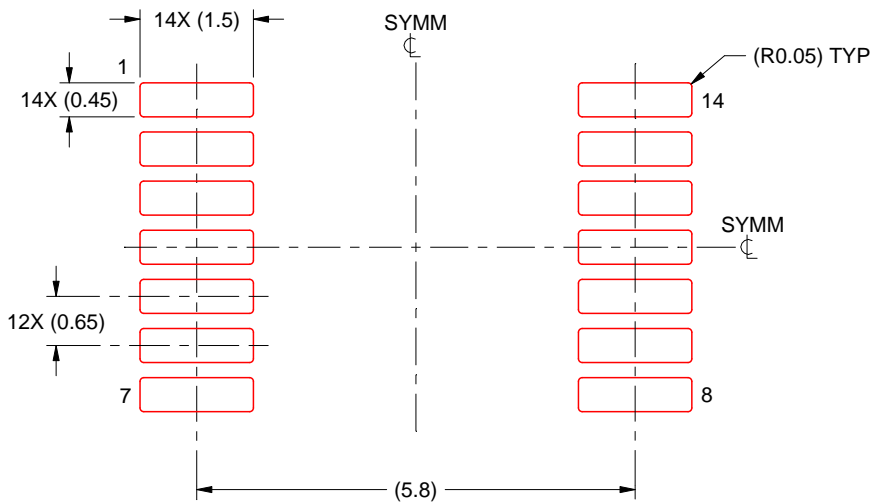
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

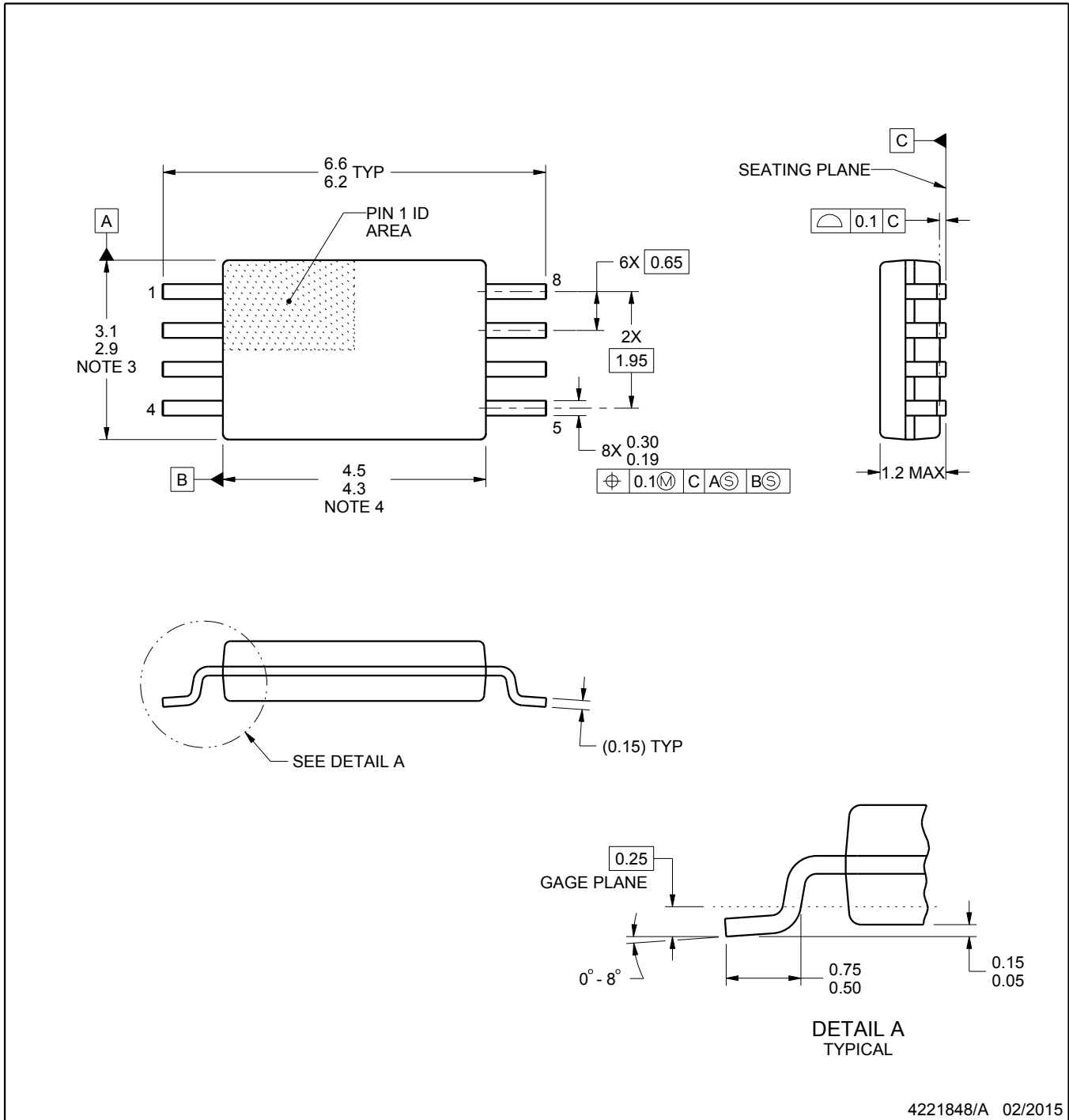
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

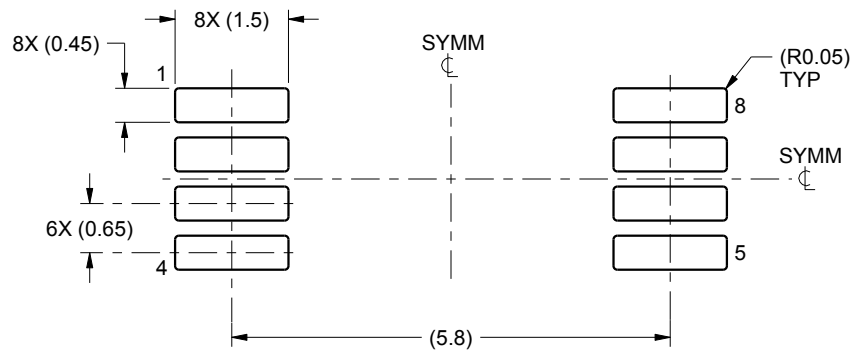
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

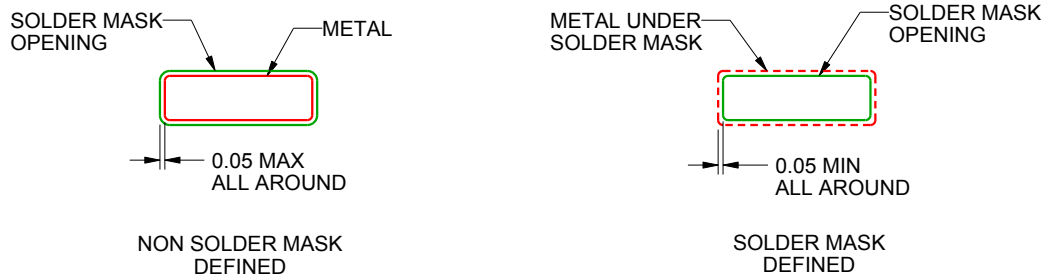
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

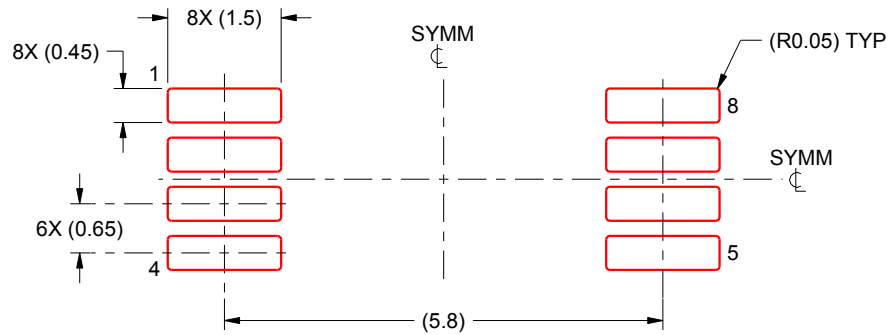
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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