

## TRIPLE 10-BIT 180-MSPS GRAPHICS AND VIDEO DAC

Check for Samples: [THS8136](#)

### FEATURES

- Triple 10-Bit Digital-to-Analog Converters (DACs)
- 180-MSPS Operation
- Direct Drive of Double-Terminated 75-Ω Load Into Standard Video Levels
- Bi-Level Sync and Blank Level Generation
- Internal Voltage Reference
- Low-Power Operation From 3.3-V Analog and 1.8-V Digital Supply Levels
- 1.8-V Compatible Inputs
- Qualified for Automotive Applications (AEC-Q100 Rev G – THS8136IPHPQ1, THS8136IPHPRQ1)

### APPLICATIONS

- Graphics and Video Generation
- High-Resolution Image Processing
- Generic Triple D/A Converter

### DESCRIPTION

The THS8136 is a general-purpose triple high-speed digital-to-analog (D/A) converter optimized for use in video/graphics applications. The device operates from 3.3-V analog and 1.8-V digital supplies with D/A converter performance assured at sampling rates up to 180 MHz. The THS8136 consists of three 10-bit D/A converters and additional circuitry for bi-level sync and blanking level generation. The current-steering DACs have been specifically designed to produce standard video output levels when directly connected to a single-ended double-terminated 75-Ω coaxial cable.

By providing a dc offset in sync insertion mode, the THS8136 can generate a bi-level sync on the AG DAC output without sacrificing DAC resolution. Support is also provided for insertion of RGB or YPbPr reference or blanking levels, irrespective of the DAC input codes. A generic DAC mode is provided for applications not requiring sync generation. All digital inputs are 1.8-V compatible.

### ORDERING INFORMATION<sup>(1)</sup>

| T <sub>A</sub> | PACKAGED DEVICES <sup>(2)</sup><br>PowerPAD™ TQFP-48 – PHP | PACKAGE OPTION |
|----------------|------------------------------------------------------------|----------------|
| 0°C to 70°C    | THS8136PHP                                                 | Tray           |
|                | THS8136PHPR                                                | Tape and reel  |
| –40°C to 85°C  | THS8136IPHP                                                | Tray           |
|                | THS8136IPHPR                                               | Tape and reel  |
|                | THS8136IPHPQ1 <sup>(3)</sup>                               | Tray           |
|                | THS8136IPHPRQ1 <sup>(3)</sup>                              | Tape and reel  |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) AEC-Q100 Rev G certified



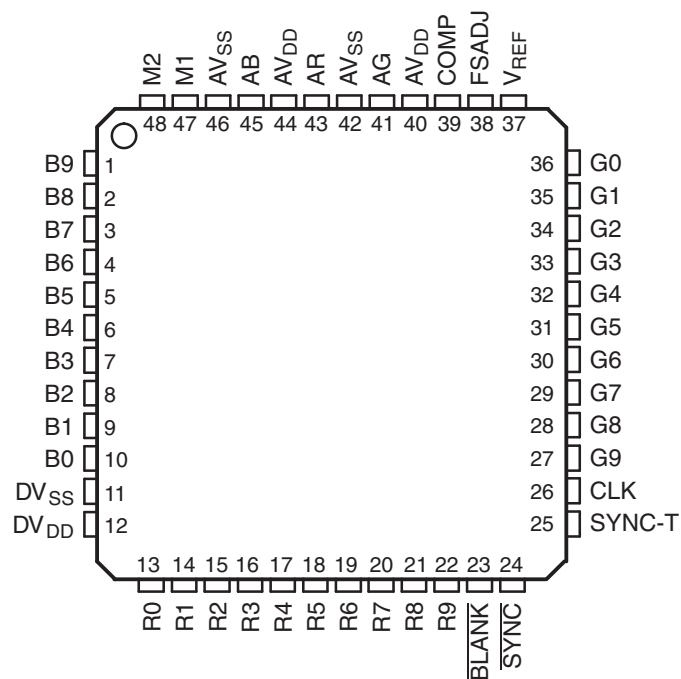
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**PHP (TQFP-48) PowerPAD PACKAGE  
(TOP VIEW)**



**TERMINAL FUNCTIONS**

| TERMINAL                                                 |                                                          | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------------------------|----------------------------------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                     | NO.                                                      |     |                                                                                                                                                                                                                                                                                                                                                                    |
| AB                                                       | 45                                                       | O   | Analog blue current output, capable of directly driving a double terminated 75-Ω coaxial cable                                                                                                                                                                                                                                                                     |
| AG                                                       | 41                                                       | O   | Analog green current output, capable of directly driving a double terminated 75-Ω coaxial cable                                                                                                                                                                                                                                                                    |
| AR                                                       | 43                                                       | O   | Analog red current output, capable of directly driving a double terminated 75-Ω coaxial cable                                                                                                                                                                                                                                                                      |
| AV <sub>DD</sub>                                         | 40, 44                                                   | I   | Analog power supply (3.3 V). All AV <sub>DD</sub> pins must be connected.                                                                                                                                                                                                                                                                                          |
| AV <sub>SS</sub>                                         | 42, 46                                                   | I   | Analog ground                                                                                                                                                                                                                                                                                                                                                      |
| $\overline{\text{SYNC}}$                                 | 24                                                       | I   | Sync insertion input. Active low. When asserted, the G output is forced to the bottom sync tip level.                                                                                                                                                                                                                                                              |
| SYNC-T                                                   | 25                                                       | I   | Connect to DV <sub>SS</sub> (GND) or logic low to enable bi-level sync insertion. Connect to DV <sub>DD</sub> (1.8 V) or logic high for generic DAC applications not requiring sync insertion.                                                                                                                                                                     |
| M2                                                       | 48                                                       | I   | Connect to DV <sub>SS</sub> (GND) or logic 0 for RGB blanking level operation. Connect to the $\overline{\text{SYNC}}$ control input for YPbPr video operation.                                                                                                                                                                                                    |
| M1                                                       | 47                                                       | I   | Must be tied to DV <sub>SS</sub> (GND) or logic 0 for normal operation.                                                                                                                                                                                                                                                                                            |
| B0<br>B1<br>B2<br>B3<br>B4<br>B5<br>B6<br>B7<br>B8<br>B9 | 10<br>9<br>8<br>7<br>6<br>5<br>4<br>3<br>2<br>1          | I   | Blue or (Pb) pixel data input. Signals with index 0 denote the least significant bit. Unused inputs should be connected to DV <sub>SS</sub> (GND).                                                                                                                                                                                                                 |
| $\overline{\text{BLANK}}$                                | 23                                                       | I   | Blanking control input, active low. A rising edge on CLK latches BLANK. When asserted, the AR, AG, and AB outputs are driven to the reference blanking level, regardless of the value on the data inputs.                                                                                                                                                          |
| CLK                                                      | 26                                                       | I   | Clock input. A rising edge on CLK latches R0–R9, G0–G9, B0–B9, and BLANK.                                                                                                                                                                                                                                                                                          |
| COMP                                                     | 39                                                       | O   | Compensation terminal. A 0.1-μF capacitor must be connected between COMP and AV <sub>DD</sub> .                                                                                                                                                                                                                                                                    |
| DV <sub>DD</sub>                                         | 12                                                       | I   | Digital power supply (1.8 V)                                                                                                                                                                                                                                                                                                                                       |
| DV <sub>SS</sub>                                         | 11                                                       | I   | Digital ground                                                                                                                                                                                                                                                                                                                                                     |
| FSADJ                                                    | 38                                                       | I   | Full-scale adjust control. The full-scale current drive on each of the output channels is determined by the value of a resistor R <sub>FS</sub> connected between this terminal and AV <sub>SS</sub> . <a href="#">Figure 3</a> shows the relationship between full-scale output voltage compliance and R <sub>FS</sub> for the nominal DAC termination of 37.5 Ω. |
| G0<br>G1<br>G2<br>G3<br>G4<br>G5<br>G6<br>G7<br>G8<br>G9 | 36<br>35<br>34<br>33<br>32<br>31<br>30<br>29<br>28<br>27 | I   | Green (or Y) pixel data input. Signals with index 0 denote the least significant bit. Unused inputs should be connected to DV <sub>SS</sub> (GND).                                                                                                                                                                                                                 |
| R0<br>R1<br>R2<br>R3<br>R4<br>R5<br>R6<br>R7<br>R8<br>R9 | 13<br>14<br>15<br>16<br>17<br>18<br>19<br>20<br>21<br>22 | I   | Red (or Pr) pixel data input. Signals with index 0 denote the least significant bit. Unused inputs should be connected to DV <sub>SS</sub> (GND).                                                                                                                                                                                                                  |
| V <sub>REF</sub>                                         | 37                                                       | O   | Voltage reference for DACs. An internal voltage reference of nominally 1.2 V is provided, which requires an external 0.1-μF ceramic capacitor between V <sub>REF</sub> and AV <sub>SS</sub> .                                                                                                                                                                      |

## DETAILED DESCRIPTION

The THS8136 is a fast well-matched triple DAC with current outputs optimized for graphics and video applications without sacrificing its usefulness as a generic DAC. The DAC output stages are designed to provide direct drive of doubly-terminated 75-Ω loads (37.5 Ω). The full-scale output current of all three DACs is determined by a single resistor connecting the FSADJ pin to AV<sub>SS</sub> (GND). A 3.8-kΩ resistor is suitable for most applications requiring 700-mV output levels. Additional circuitry and digital input controls for analog sync and blank level generation are provided for both RGB and YPbPr color spaces. A generic mode of operation is provided for applications not requiring sync insertion. [Figure 1](#) shows a block diagram of the device.

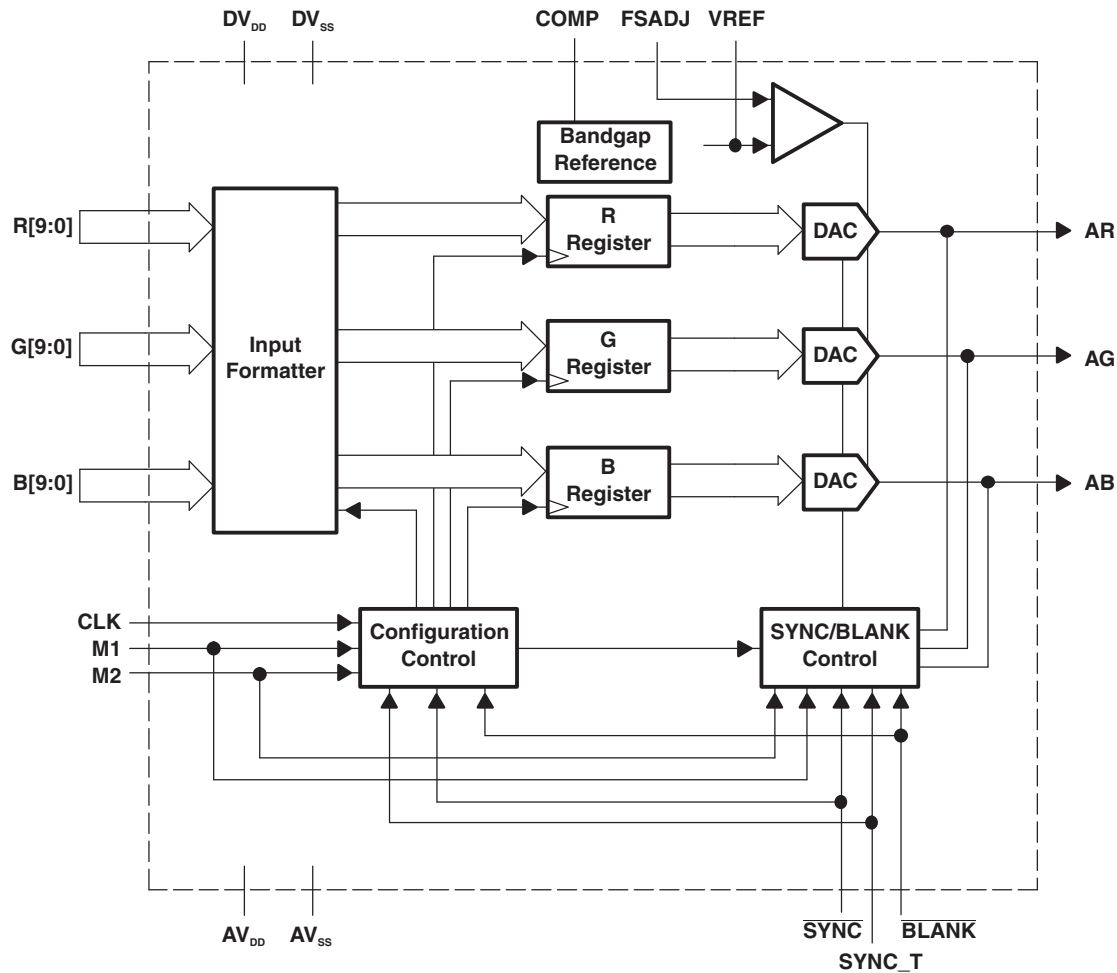


Figure 1. Functional Block Diagram

### Generic DAC Mode Versus Sync Insertion Mode

When configured for sync insertion, the THS8136 provides additional dc bias on the DAC outputs to provide headroom for negative bi-level sync insertion. Such bias might be undesirable in applications where no analog sync insertion is required, since it results in additional power consumption and might prevent dc coupling of the DAC outputs. In such cases, only triple DAC operation without dc bias (i.e., DAC input code 0 corresponding to 0-V output) might be preferred. Generic DAC mode is easily selected by connecting the SYNC and SYNC\_T pins to DV<sub>DD</sub> (or logic 1) and the M1 and M2 pins to DV<sub>SS</sub> (or logic 0). BLANK is functional in both generic mode and sync insertion mode.

## Blanking Generation

The  $\overline{\text{BLANK}}$  control input forces the output amplitude on all channels to the blanking or reference level, irrespective of the value on the data input ports. The output blanking level on each channel and its relation to active video varies depending on the mode of operation. In generic DAC mode, the output blank level for each DAC is at 0 V and corresponds to a DAC input code of 0. When sync insertion is enabled a 350-mV dc bias ( $R_{FS}$  selected for 700-mV output) is applied to provide room for bi-level sync insertion. When RGB sync insertion is enabled, the output blank level of each DAC will be at 350 mV and will correspond to a DAC input code of 0. In YPbPr video mode, the blank level of each DAC is 350 mV, but the AR and AB blank levels correspond to a DAC input code of 512 to accommodate mid-level UV blank levels. A video to blank level amplitude ratio of 2:1 is maintained for various  $R_{FS}$  values, provided the maximum DAC output compliance is not exceeded.

## Sync Generation

The  $\overline{\text{SYNC}}$  and SYNC\_T control inputs can be used to enable the superposition of a bi-level sync on the AG DAC output. Correctly timed assertion of the  $\overline{\text{SYNC}}$  input (active low) allows insertion of an analog composite sync on the AG DAC output consisting of horizontal sync and vertical sync. The video to sync amplitude ratio is 7:3 providing a 300 mV sync tip, when FSADJ is selected to provide 700 mV full-scale graphics or video. This 7:3 video to sync amplitude ratio is maintained for various  $R_{FS}$  values, provided the maximum DAC output compliance is not exceeded. The SYNC-T input pin must be connected to DV<sub>SS</sub> (or logic low) to enable sync insertion.

## Device Configuration

The THS8136 operating mode is determined from the state of the  $\overline{\text{SYNC}}$ , SYNC-T, M1, and M2 control terminals. Generic DAC mode is easily selected by connecting  $\overline{\text{SYNC}}$  and SYNC\_T to DV<sub>DD</sub> (or logic high) and M1 and M2 to DV<sub>SS</sub> (logic low). To enable sync insertion, the SYNC\_T terminal must be connected to DV<sub>SS</sub> (or logic low). YPbPr video mode can be selected for support of mid-level PbPr blanking by connecting the sync control input to both the  $\overline{\text{SYNC}}$  and M2 input terminals. The M1 terminal must be connected to DV<sub>SS</sub> (logic 0) for all operating modes. See [Table 1](#) and [Figure 4](#), [Figure 5](#), and [Figure 6](#) for additional information on configuring the THS8136.

**Table 1. Table 1. Device Configuration**

| OPERATING MODE       | M1 | M2                       | SYNC_T | $\overline{\text{SYNC}}$ | DESCRIPTION                                                                                             |
|----------------------|----|--------------------------|--------|--------------------------|---------------------------------------------------------------------------------------------------------|
| Generic DAC          | 0  | 0                        | 1      | 1                        | Sync insertion disabled. The blank level on all DAC outputs corresponds to 0-V and DAC input code 0.    |
| RGB Sync Insertion   | 0  | 0                        | 0      | $\overline{\text{SYNC}}$ | DC bias and sync insertion enabled. The blank level on all DAC outputs corresponds to DAC input code 0. |
| YPbPr Sync Insertion | 0  | $\overline{\text{SYNC}}$ | 0      | $\overline{\text{SYNC}}$ | DC bias and sync insertion enabled. AB and AR mid-level blanking corresponds to DAC input code 512.     |

## DAC Operation

The DAC output drivers generate a current with a drive level that can be user-modified by choosing an appropriate resistor value  $R_{FS}$  connected between the FSADJ terminal and AV<sub>SS</sub> (GND). All current source amplitudes (graphics/video, blanking, and sync on AG) are derived from  $R_{FS}$  and an internal voltage reference such that the relative amplitudes of sync, blank, and graphics/video are always equal to their nominal relationships. The relative amplitudes of these current drivers are maintained without regard to the value of  $R_{FS}$ , as long as the maximum current drive capability is not exceeded. [Figure 3](#) shows the relationship between  $R_{FS}$  and the current drive level on each channel for full-range DAC input. The voltage compliance outputs in [Figure 3](#) assume termination with a 37.5-Ω resistor. When sync insertion is enabled, an additional current source is enabled providing a DC bias and head-room for negative sync insertion. A fixed  $R_{FS}$  value of 3.8 kΩ ( $R_{FS(nom)}$ ) is suitable for most applications requiring 700-mV output levels.

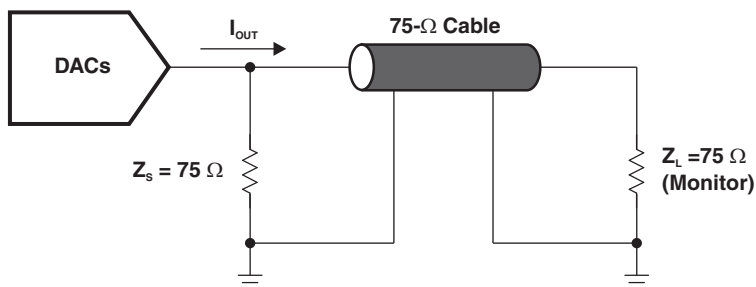


Figure 2. DAC Output Termination

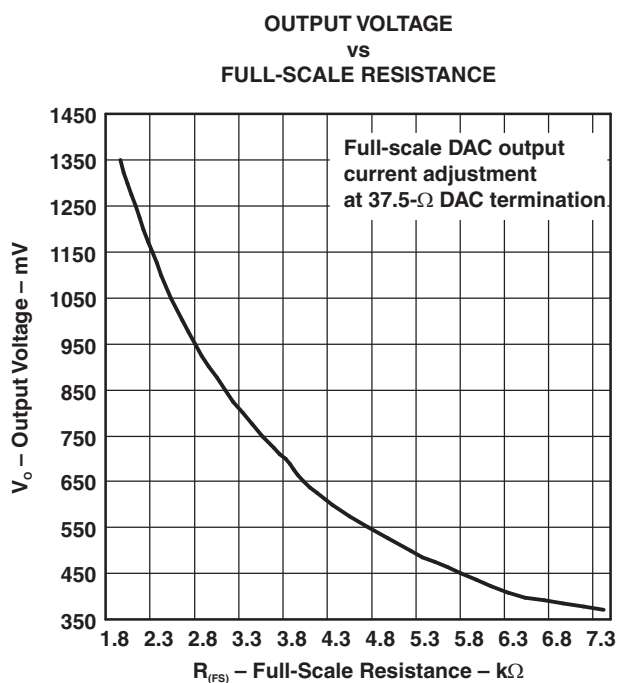
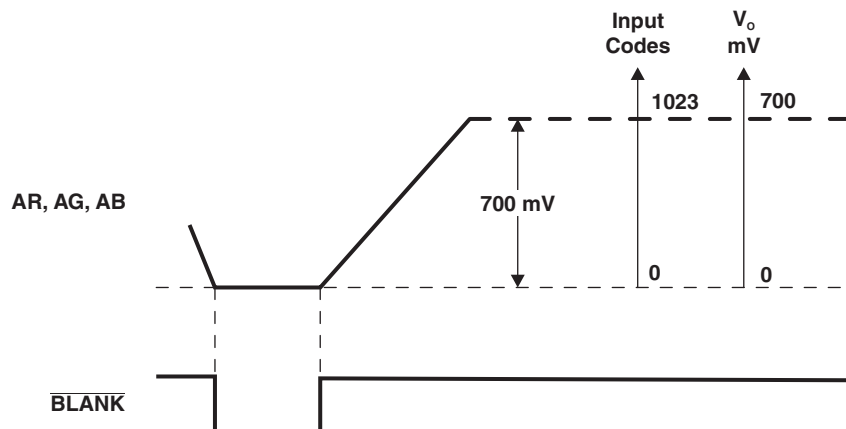


Figure 3. Output Voltage vs Full-Scale Resistance

The user is free to connect another resistor value, but care should be taken not to exceed the maximum current level on each of the DAC outputs as shown in the specifications section. Additionally, DAC output linearity will degrade if the 1.2-V maximum output compliance is exceeded.

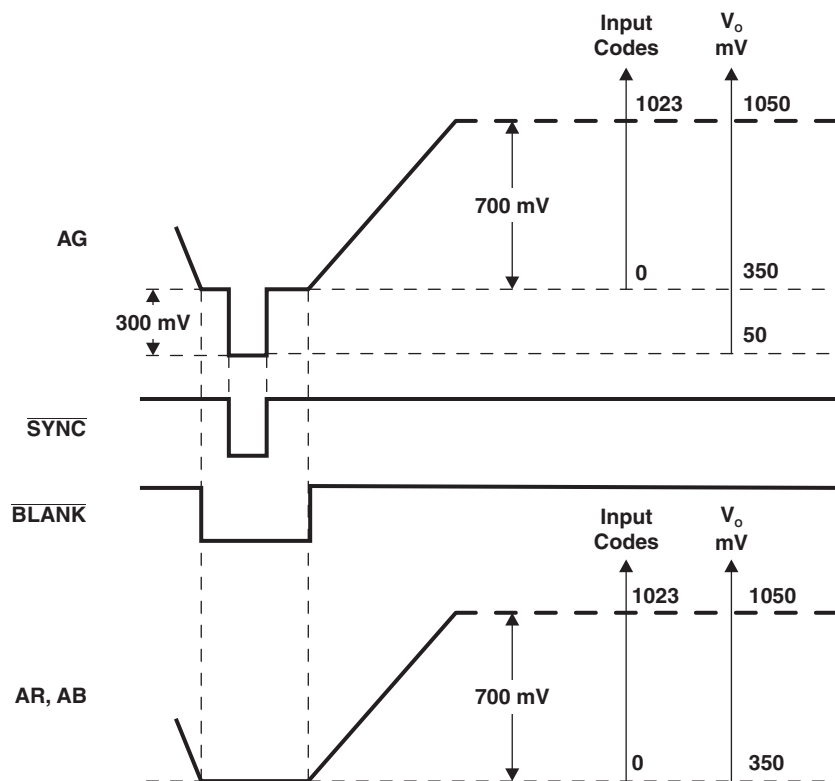


NOTE:  $\overline{\text{BLANK}}$  = High in applications not requiring a forced blank level.

$R_{FS}$  chosen for 700-mV output.

$R_{LOAD} = 37.5 \Omega$

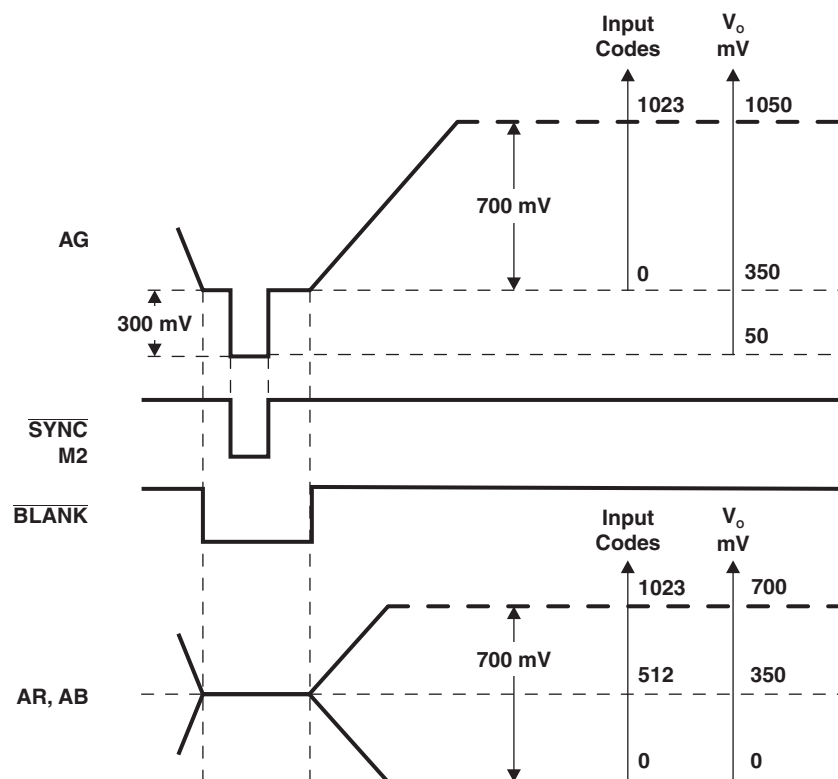
**Figure 4. Generic DAC Mode (M1 = Low, M2 = Low,  $\overline{\text{SYNC}}$  = High, SYNC\_T = High)**



NOTE:  $R_{FS}$  chosen for 700-mV output.

$R_{LOAD} = 37.5 \Omega$

**Figure 5. RGB Sync-on-G (M1 = Low, M2 = Low, SYNC\_T = Low)**



NOTE:  $R_{FS}$  chosen for 700-mV output.  
 $R_{LOAD} = 37.5 \Omega$

**Figure 6. YPbPr Sync-on-Y (M1 = Low, M2 =  $\overline{\text{SYNC}}$ , SYNC\_T = Low)**

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                 |                                      |                                                      |
|-------------------------------------------------|--------------------------------------|------------------------------------------------------|
| Supply voltage                                  | AV <sub>DD</sub> to AV <sub>SS</sub> | –0.5 V to 3.6 V                                      |
|                                                 | DV <sub>DD</sub> to DV <sub>SS</sub> | –0.5 V to 1.95 V                                     |
|                                                 | AV <sub>SS</sub> to DV <sub>SS</sub> | –0.5 to 0.5 V                                        |
| Digital input voltage range to DV <sub>SS</sub> |                                      | –0.5 V to (DV <sub>DD</sub> + 0.5) V                 |
| T <sub>A</sub>                                  | Operating free-air temperature range | –40°C to 85°C                                        |
| T <sub>stg</sub>                                | Storage temperature range            | –55°C to 150°C                                       |
| V <sub>ESD</sub>                                | ESD stress voltage <sup>(2)</sup>    | Human-body model (HBM) <sup>(3)</sup> , All pins     |
|                                                 |                                      | Charged-device model (CDM) <sup>(4)</sup> , All pins |
|                                                 |                                      | >2000 V                                              |
|                                                 |                                      | >500 V                                               |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
- (3) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001-2010 and AEC Q100-002 rev D. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible if necessary precautions are taken. Pins listed as 2000 V may actually have higher performance.
- (4) Level listed is the passing level per EIA-JEDEC JESD22-C101E and AEC Q100-011 rev B. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance. Corner pins meet the AEC Q100-011 rev B 750-V requirement.

## THERMAL SPECIFICATIONS

| PARAMETER           |                                                     | TEST CONDITIONS <sup>(1)</sup>             | MIN | TYP   | MAX | UNIT |
|---------------------|-----------------------------------------------------|--------------------------------------------|-----|-------|-----|------|
| $\theta_{JA}$       | Junction-to-ambient thermal resistance, still air   | Thermal PAD soldered to 4-layer High-K PCB |     | 29.11 |     | °C/W |
|                     |                                                     | Low-K PCB, Thermal PAD not soldered        |     | 64.42 |     | °C/W |
| $\theta_{JC}$       | Junction-to-case thermal resistance, still air      |                                            |     | 0.12  |     |      |
| T <sub>J(MAX)</sub> | Maximum junction temperature for reliable operation |                                            |     |       | 105 | °C   |

- (1) When split ground planes are used, attach the thermal pad to the analog ground plane.

## RECOMMENDED OPERATING CONDITIONS

|                                     |                               | MIN              | NOM | MAX              | UNIT       |
|-------------------------------------|-------------------------------|------------------|-----|------------------|------------|
| <b>Power Supply</b>                 |                               |                  |     |                  |            |
| AV <sub>DD</sub>                    |                               | 3                | 3.3 | 3.6              | V          |
| DV <sub>DD</sub>                    |                               | 1.65             | 1.8 | 1.95             | V          |
| <b>Digital and Reference Inputs</b> |                               |                  |     |                  |            |
| V <sub>IH</sub>                     | High-level input voltage      | 1.2              |     | DV <sub>DD</sub> | V          |
| V <sub>IL</sub>                     | Low-level input voltage       | DV <sub>SS</sub> |     | 0.7              | V          |
| f <sub>CLK</sub>                    | Clock frequency               | 0                |     | 180              | MHz        |
| t <sub>w(CLKH)</sub>                | Pulse duration, clock high    | 40%              |     | 60%              | CLK period |
| t <sub>w(CLKL)</sub>                | Pulse duration, clock low     | 40%              |     | 60%              | CLK period |
| R <sub>FS(nom)</sub>                | FSADJ resistor <sup>(1)</sup> |                  | 3.8 |                  | kΩ         |

- (1) R<sub>FS</sub> should be chosen such that the maximum full-scale DAC output current (I<sub>FS</sub>) does not exceed the maximum stated level. This yields the nominal output voltage compliance at the nominal load termination of 37.5 Ω.

## POWER SUPPLY ELECTRICAL CHARACTERISTICS

over recommended operating conditions,  $f_{CLK} = 180$  MHz, use of internal reference voltage  $V_{REF}$ ,  $R_{FS} = R_{FS(nom)}$ , 37.5- $\Omega$  load termination (unless otherwise noted)

| PARAMETER  |                                   | TEST CONDITIONS <sup>(1)</sup> | MIN                            | TYP <sup>(2)</sup> | MAX <sup>(3)</sup> | UNIT |
|------------|-----------------------------------|--------------------------------|--------------------------------|--------------------|--------------------|------|
| $I_{AVDD}$ | Operating supply current, analog  | CLK = 80 MSPS                  | Generic (700 mV)               | 65                 | 72                 | mA   |
|            |                                   | CLK = 180 MSPS                 |                                | 65                 | 72                 |      |
|            |                                   | CLK = 80 MSPS                  | Generic (1.2 mV)               | 110                | 112                |      |
|            |                                   | CLK = 180 MSPS                 |                                | 110                | 112                |      |
|            |                                   | CLK = 80 MSPS                  | Sync Insertion (700 mV + Sync) | 94                 | 102                |      |
|            |                                   | CLK = 180 MSPS                 |                                | 94                 | 103                |      |
| $I_{DVDD}$ | Operating supply current, digital | CLK = 80 MSPS                  | Generic (700 mV)               | 13                 | 16                 | mA   |
|            |                                   | CLK = 180 MSPS                 |                                | 31                 | 36                 |      |
|            |                                   | CLK = 80 MSPS                  | Generic (1.2 mV)               | 14                 | 16                 |      |
|            |                                   | CLK = 180 MSPS                 |                                | 31                 | 37                 |      |
|            |                                   | CLK = 80 MSPS                  | Sync Insertion (700 mV + Sync) | 13                 | 16                 |      |
|            |                                   | CLK = 180 MSPS                 |                                | 31                 | 36                 |      |
| $P_D$      | Power dissipation                 | CLK = 80 MSPS                  | Generic (700 mV)               | 238                | 290                | mW   |
|            |                                   | CLK = 180 MSPS                 |                                | 270                | 329                |      |
|            |                                   | CLK = 80 MSPS                  | Generic (1.2 mV)               | 388                | 434                |      |
|            |                                   | CLK = 180 MSPS                 |                                | 419                | 475                |      |
|            |                                   | CLK = 80 MSPS                  | Sync Insertion (700 mV + Sync) | 334                | 398                |      |
|            |                                   | CLK = 180 MSPS                 |                                | 366                | 441                |      |

(1) A multiburst RGB input test pattern was used in all cases.

(2) TYP current and  $P_D$  measured at  $AV_{DD} = 3.3$  V and  $DV_{DD} = 1.8$  V.

(3) MAX current and  $P_D$  measured at  $AV_{DD} = 3.6$  V and  $DV_{DD} = 1.95$  V.

## DIGITAL INPUTS – DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions,  $f_{CLK} = 180$  MHz, use of internal reference voltage  $V_{REF}$ ,  $R_{FS} = R_{FS(nom)}$ , 37.5- $\Omega$  load termination (unless otherwise noted)

| PARAMETER     |                                                                                          | TEST CONDITIONS                                                | MIN | TYP | MAX | UNIT        |
|---------------|------------------------------------------------------------------------------------------|----------------------------------------------------------------|-----|-----|-----|-------------|
| $I_{IH}$      | High-level input current                                                                 | $AV_{DD} = 3.3$ V, $DV_{DD} = 1.8$ V, Digital inputs at 1.95 V |     |     | 1   | $\mu$ A     |
| $I_{IL}$      | Low-level input current                                                                  | $AV_{DD} = 3.3$ V, $DV_{DD} = 1.8$ V, Digital inputs at 0 V    |     |     | –1  | $\mu$ A     |
| $I_{IH(CLK)}$ | High-level input current, CLK                                                            | $AV_{DD} = 3.3$ V, $DV_{DD} = 1.8$ V, CLK at 1.95 V            | –1  |     | 1   | $\mu$ A     |
| $I_{IL(CLK)}$ | Low-level input current, CLK                                                             | $AV_{DD} = 3.3$ V, $DV_{DD} = 1.8$ V, CLK at 0 V               | –1  |     | 1   | $\mu$ A     |
| $C_I$         | Input capacitance                                                                        | $T_A = 25^\circ\text{C}$                                       |     | 5   |     | pF          |
| $t_s$         | Setup time, data and control inputs <sup>(1)</sup>                                       |                                                                | 1.5 |     |     | ns          |
| $t_h$         | Hold time, data and control inputs <sup>(1)</sup>                                        |                                                                | 500 |     |     | ps          |
| $t_{d(D)}$    | Digital process delay time from first registered color component of pixel <sup>(2)</sup> |                                                                |     | 7.5 |     | CLK periods |

(1) Specified by characterization only.

(2) This parameter is specified by design. The digital process delay is defined as the number of CLK cycles required for the first registered color component of a pixel, starting from the time of registering it on the input bus, to propagate through all processing and appear at the DAC output drivers. The remaining delay through the IC is the analog delay  $t_{d(A)}$  of the analog output drivers.

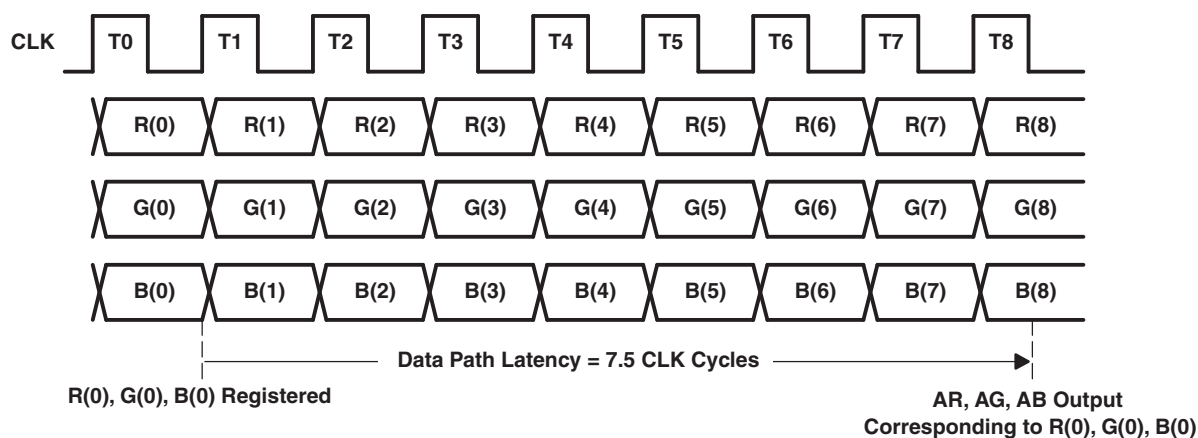
## ANALOG (DAC) OUTPUTS ELECTRICAL CHARACTERISTICS

over recommended operating conditions,  $f_{CLK} = 180 \text{ MHz}$ , use of internal reference voltage  $V_{REF}$ ,  $R_{FS} = R_{FS(nom)}$ , 37.5- $\Omega$  load termination (unless otherwise noted)

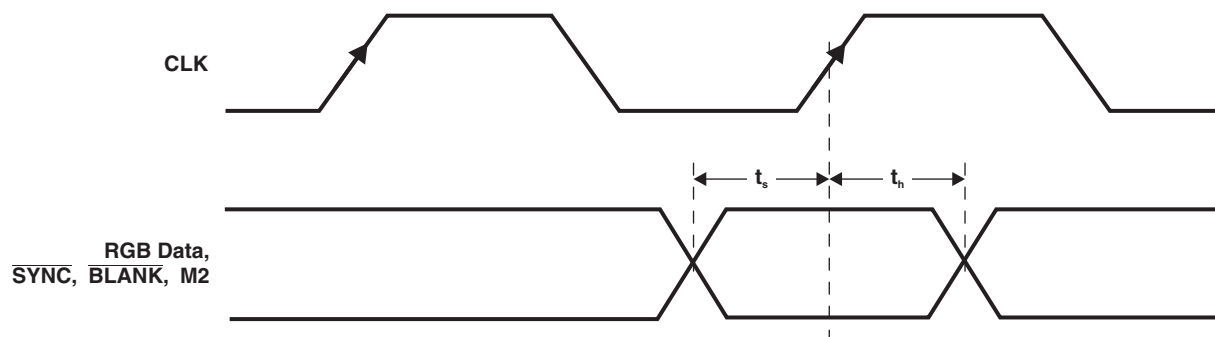
| PARAMETER      |                                                                | TEST CONDITIONS                                                                                   | MIN  | TYP      | MAX      | UNIT     |
|----------------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------|------|----------|----------|----------|
| DAC resolution |                                                                |                                                                                                   |      | 10       |          | Bits     |
| INL            | Integral nonlinearity                                          | Static, best fit, RGB with sync insertion (700 + sync)                                            |      | -1/1     | -2.5/1.5 | LSB      |
|                |                                                                | Static, best fit, generic mode, 1.2 V output range                                                |      | -1/1     |          |          |
| DNL            | Differential nonlinearity                                      | Static, RGB with sync insertion (700 + sync)                                                      |      | -0.4/0.4 | $\pm 1$  | LSB      |
|                |                                                                | Static, generic mode, 1.2 V output range                                                          |      | -0.4/0.4 |          |          |
| PSRR           | Power supply ripple rejection ratio of DAC output (full scale) | $f = DC^{(1)}$                                                                                    |      | 38.5     |          | dB       |
| $V_{refo}$     | Voltage reference output                                       |                                                                                                   | 1.12 | 1.16     | 1.20     | V        |
| $R_R$          | $V_{REF}$ output resistance                                    |                                                                                                   |      | 284      |          | $\Omega$ |
| $K_{IMBAL}$    | Imbalance between DACs <sup>(2)</sup>                          | CLK = 80 MSPS, video mode                                                                         | -2   | 1.8      | 2        | %        |
| $V_{OC}$       | DAC output compliance voltage                                  |                                                                                                   |      | 0.7      | 1.2      | V        |
| $I_{FS}$       | Generic DAC mode                                               | CLK = 80 MSPS <sup>(3)</sup>                                                                      | 18   | 18.67    | 19.5     | mA       |
|                | RGB with sync insertion enabled                                | CLK = 80 MSPS <sup>(3)</sup>                                                                      | 27   | 28       | 29.3     |          |
| $t_{RDAC}$     | DAC output current rise time                                   | CLK = 80 MSPS, 10 to 90% of full scale <sup>(4)</sup>                                             | 2.8  | 3.3      | 3.6      | ns       |
| $t_{FDAC}$     | DAC output current fall time                                   | CLK = 80 MSPS, 10 to 90% of full scale <sup>(4)</sup>                                             | 2.8  | 3.3      | 3.6      | ns       |
| $t_{d(A)}$     | Analog output delay                                            | Measured from CLK = $V_{IH(min)}$ to 50% of full-scale transition <sup>(5)</sup>                  |      | 4.5      |          | ns       |
| $t_S$          | Analog output settling time                                    | Measured from 50% of full scale transition on output to output settling, within 2% <sup>(4)</sup> |      | 15       |          | ns       |

- (1) PSRR is measured with a 0.1- $\mu\text{F}$  capacitor between the COMP and  $AV_{DD}$  pins and with a 0.1- $\mu\text{F}$  capacitor connected between the  $V_{REF}$  and  $AV_{SS}$  pins. The ripple amplitude is within the range 100 mVp-p to 500 mVp-p with the DAC output set to full scale and a double-terminated 75  $\Omega$  (= 37.5  $\Omega$ ) load. PSRR is defined as  $20 \times \log(\text{ripple voltage at DAC output} / \text{ripple voltage at } AV_{DD} \text{ input})$ . Limits are from characterization only.
- (2) The imbalance between DACs applies to all possible pairs of the three DACs.
- (3) Values at  $R_{FS} = R_{FS(nom)}$
- (4) From characterization only. Measured on the AG channel with  $R_{FS} = R_{FS(nom)}$ .
- (5) This value excludes the digital process delay,  $t_{D(D)}$ . Limit are from characterization only.

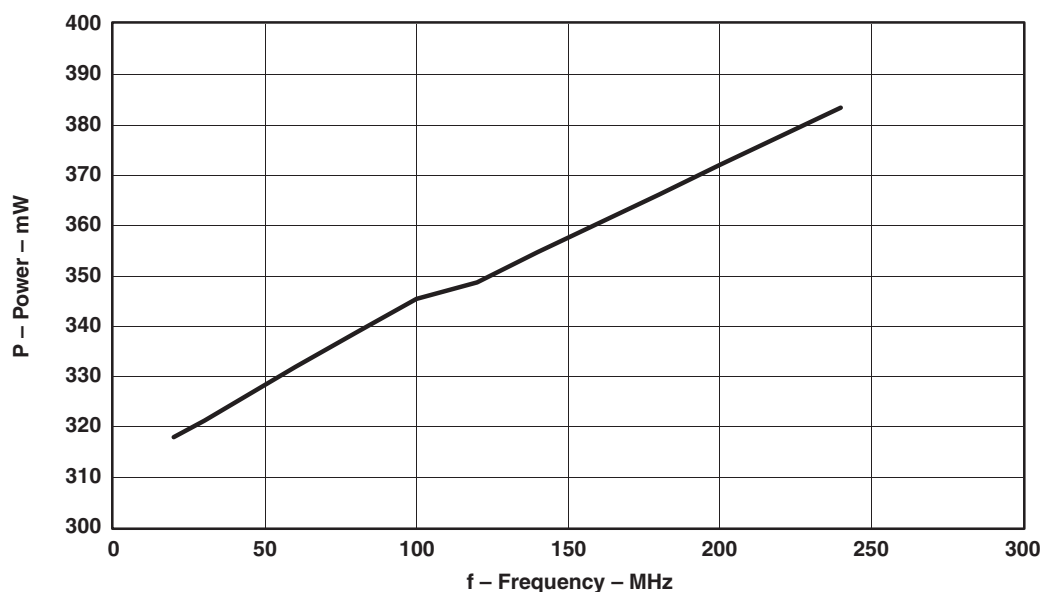
## TYPICAL CHARACTERISTICS



**Figure 7. Input Data Internally Latched on Rising Edge of CLK  
(Data Path Latency is 7.5 CLK Cycles)**

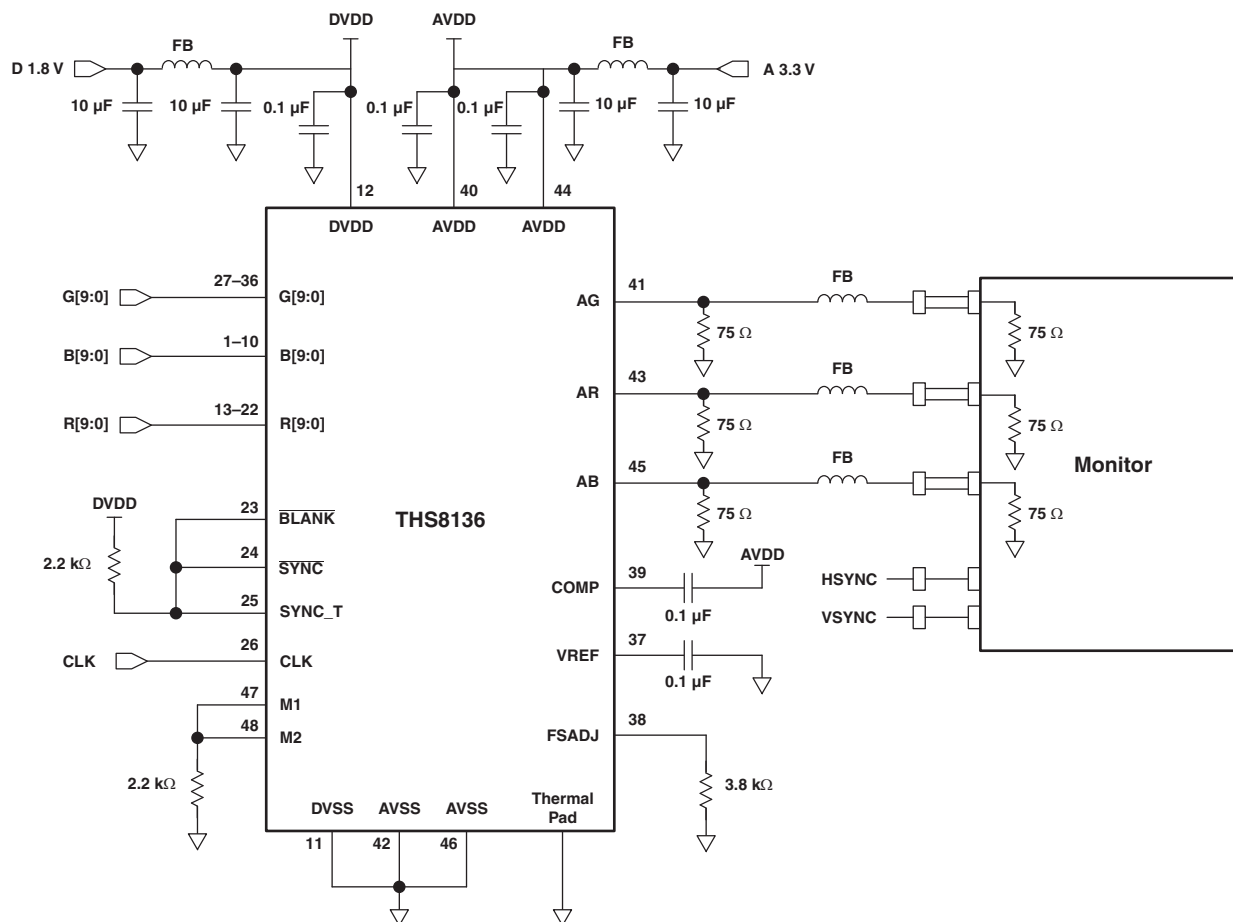


**Figure 8. Input Data Registered on Rising Edge of CLK**



**Figure 9. Power vs Clock Frequency, RGB Sync Insertion, 1-MHz Input Tone on All Channels**

## APPLICATION INFORMATION



NOTE: System level ESD protection is not included in this application circuit, but it is highly recommended on the analog RGB outputs.

**Figure 10. Typical Generic DAC Application Circuit**

## REVISION HISTORY

| REVISION | COMMENTS                                                                                                                                                                                                             |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SLES236  | Initial release                                                                                                                                                                                                      |
| SLES236A | AEC-Q100 qualification added.<br>Added ESD data to Absolute Maximum Ratings table.<br>Power dissipation ratings changed to Thermal specifications.<br>Modified Digital inputs - DC electrical characteristics table. |
| SLES236B | <a href="#">Figure 10</a> , Added note concerning ESD protection.                                                                                                                                                    |

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|------------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">THS8136IPHP</a>  | Active        | Production           | HTQFP (PHP)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | THS8136I            |
| THS8136IPHP.A                | Active        | Production           | HTQFP (PHP)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | THS8136I            |
| <a href="#">THS8136IPHPR</a> | Active        | Production           | HTQFP (PHP)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | THS8136I            |
| THS8136IPHPR.A               | Active        | Production           | HTQFP (PHP)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | THS8136I            |
| <a href="#">THS8136PHP</a>   | Active        | Production           | HTQFP (PHP)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | THS8136             |
| THS8136PHP.A                 | Active        | Production           | HTQFP (PHP)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | THS8136             |
| <a href="#">THS8136PHPR</a>  | Active        | Production           | HTQFP (PHP)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | THS8136             |
| THS8136PHPR.A                | Active        | Production           | HTQFP (PHP)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | THS8136             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

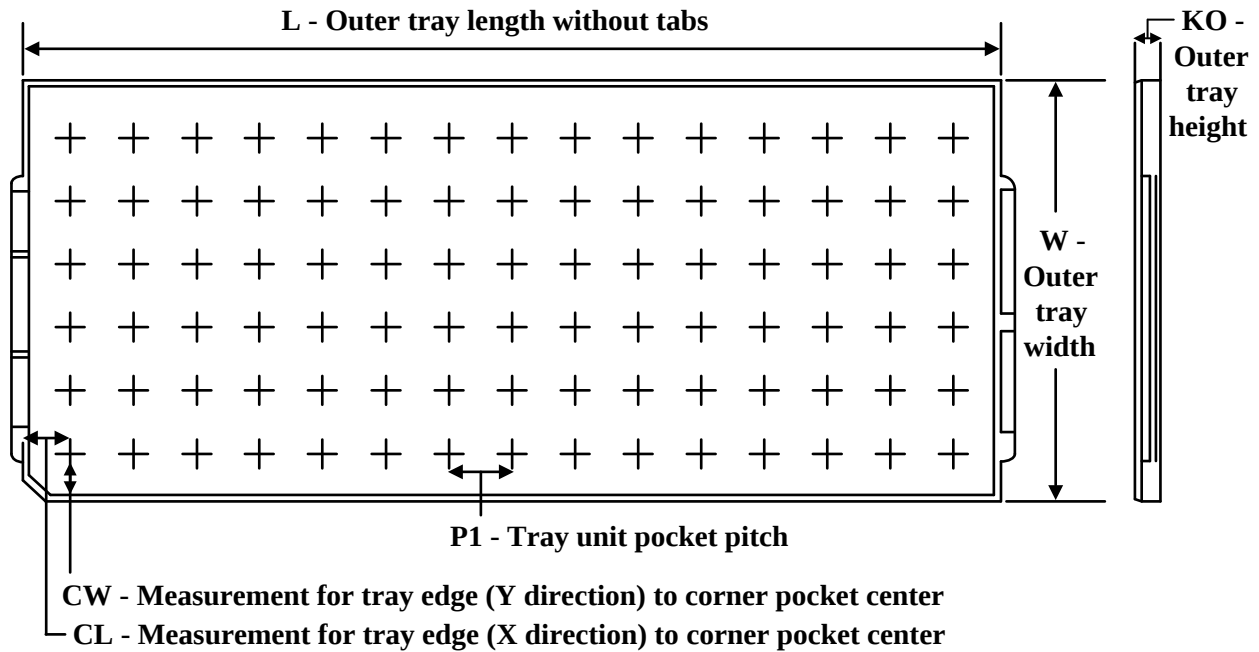
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|---------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| THS8136IPHP   | PHP          | HTQFP        | 48   | 250 | 10 x 25           | 150                  | 315    | 135.9  | 7620    | 12.2    | 11.1    | 11.25   |
| THS8136IPHP.A | PHP          | HTQFP        | 48   | 250 | 10 x 25           | 150                  | 315    | 135.9  | 7620    | 12.2    | 11.1    | 11.25   |
| THS8136PHP    | PHP          | HTQFP        | 48   | 250 | 10 x 25           | 150                  | 315    | 135.9  | 7620    | 12.2    | 11.1    | 11.25   |
| THS8136PHP.A  | PHP          | HTQFP        | 48   | 250 | 10 x 25           | 150                  | 315    | 135.9  | 7620    | 12.2    | 11.1    | 11.25   |

## GENERIC PACKAGE VIEW

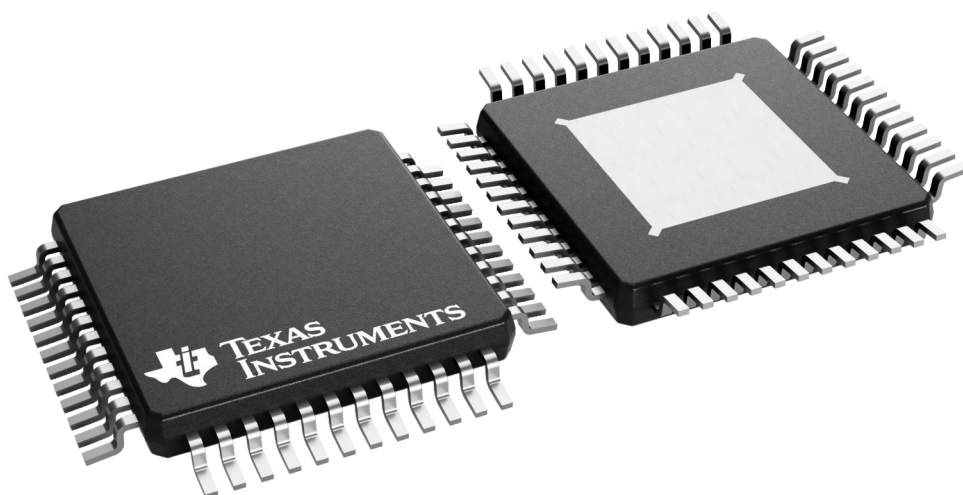
**PHP 48**

**TQFP - 1.2 mm max height**

7 x 7, 0.5 mm pitch

QUAD FLATPACK

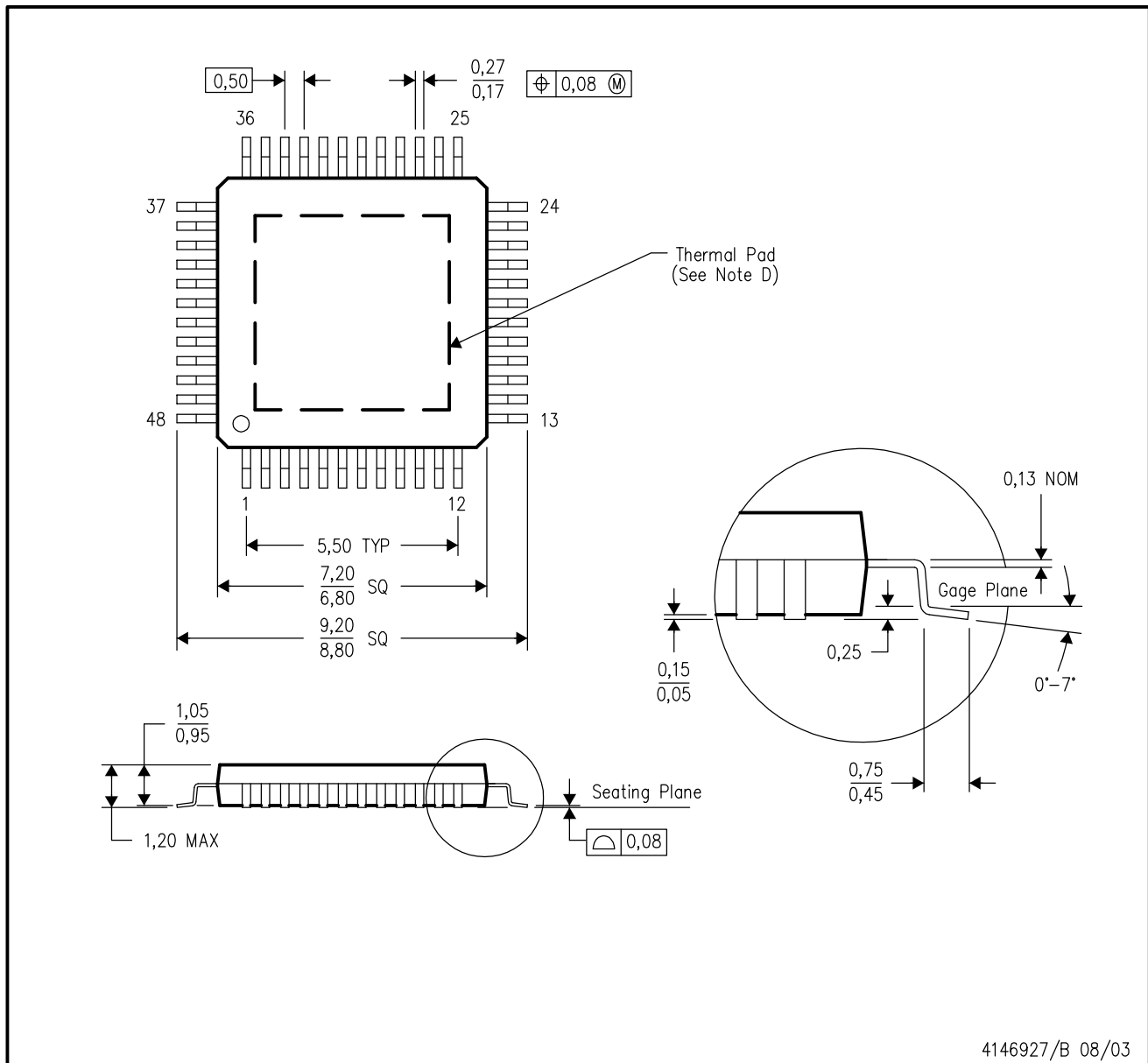
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226443/A

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

PHP (S-PQFP-G48)

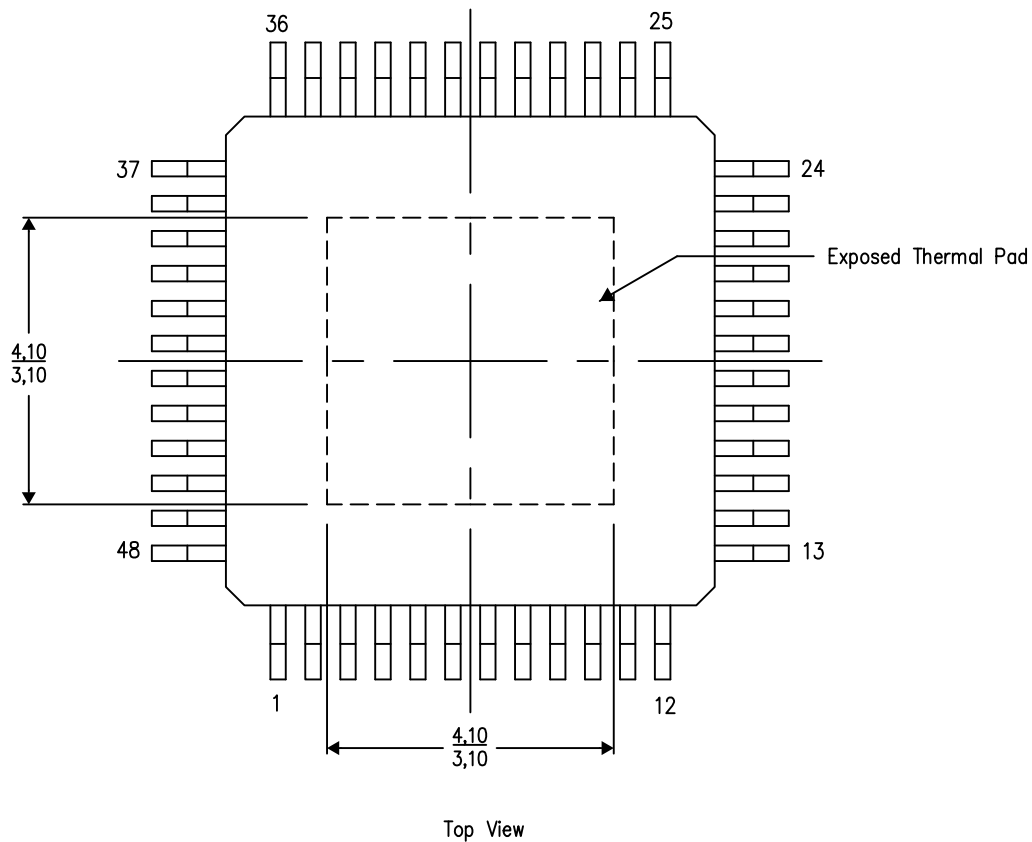
PowerPAD™ PLASTIC QUAD FLATPACK

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

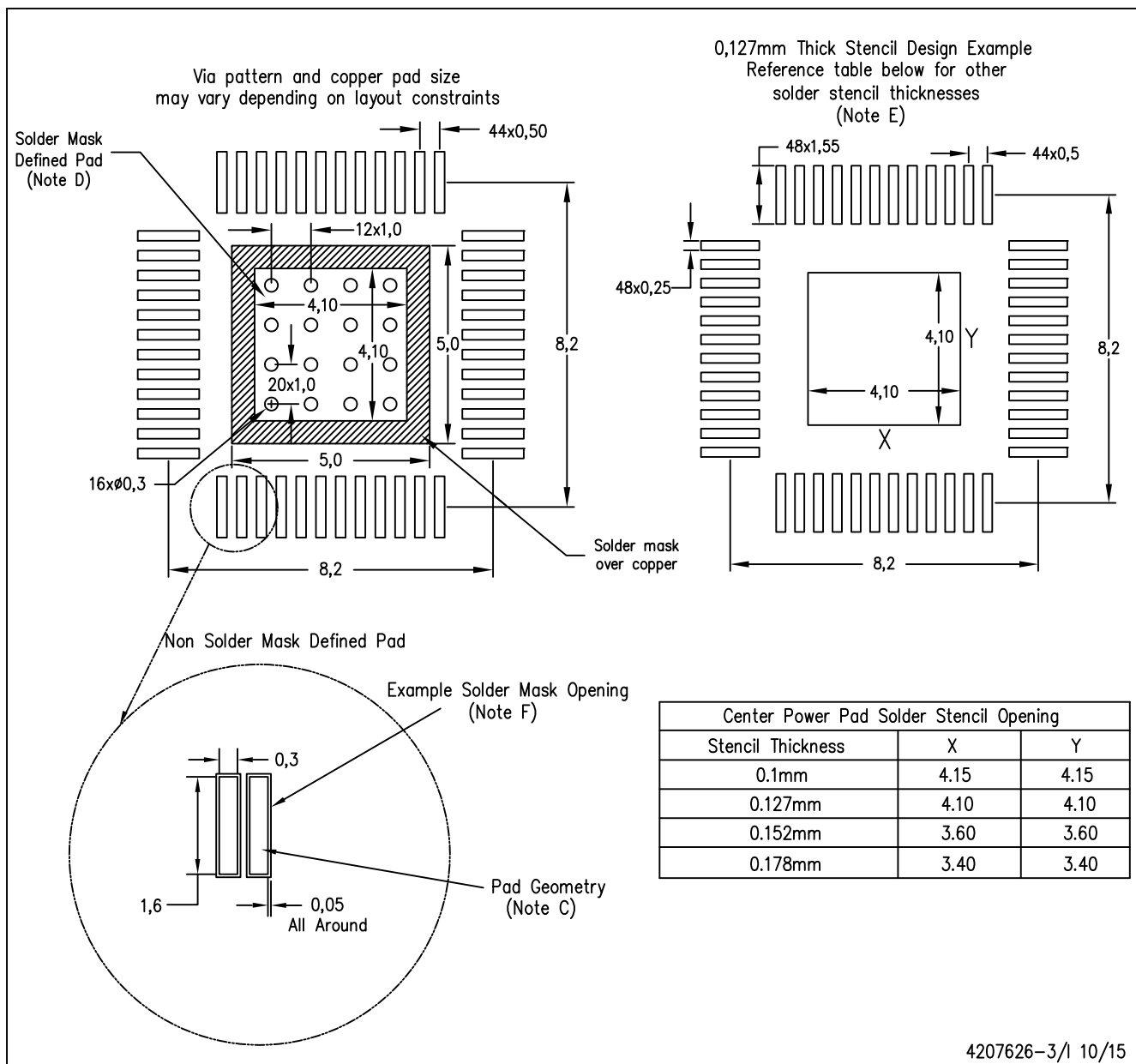


Exposed Thermal Pad Dimensions

4206329-3/P 03/15

NOTE: A. All linear dimensions are in millimeters

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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

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