THS6222 8V to 32V, Differential HPLC Line Driver With Common-Mode Buffer

1 Features

- Supply range (V_S): 8V to 32V
- Integrated midsupply common-mode buffer
- Large-signal bandwidth: 195MHz (V_O = 16V_{PP})
- Slew rate (16V step): 5500V/µs
- Low distortion (V_S = 12V, 50Ω load):
  - HD2: –80dBc (1MHz)
  - HD3: –90dBc (1MHz)
- Output current: 338mA (V_S = 12V, 25Ω load)
- Wide output swing (V_S = 12V):
  - 19.4V_{PP} (100Ω load)
  - 18.6V_{PP} (50Ω load)
- Adjustable power modes:
  - Full-bias mode: 19.5mA
  - Mid-bias mode: 15mA
  - Low-bias mode: 10.4mA
  - Low-power shutdown mode
  - IADJ pin for variable bias
- Integrated overtemperature protection
- High performance upgrade to the THS6212

2 Applications

- SGCC HPLC line drivers, IEEE 1901.1
- PLC Standards: G.hn, PRIME BPL, G3, PRIME
- HomePlug GreenPHY (HPGP), ISO 15118
- Smart meters
- Data concentrators
- Power line communications gateways
- Home networking PLC
- Differential DSL line drivers

3 Description

The THS6222 is a differential line-driver amplifier with a current-feedback architecture manufactured using Texas Instruments' proprietary, high-speed, silicon-germanium (SiGe) process. The device is targeted for use in broadband, high-speed, power line communications (HPLC, IEEE 1901.1) line driver applications that require high linearity when driving heavy line loads. The THS6222 supports PLC standards including G3, PRIME, ISO 15118 (HPGP), G.hn and PRIME BPL. Common modulation schema: OOK, FSK, OFDM.

The unique architecture of the THS6222 uses minimal quiescent current while achieving very high linearity. The amplifier has an adjustable current pin (IADJ) that sets the nominal current consumption along with the multiple bias modes that allow for enhanced power savings where the full performance of the amplifier is not required. Shutdown bias mode provides further power savings during receive mode in time division multiplexed (TDM) systems while maintaining high output impedance. The integrated midsupply common-mode buffer eliminates external components, reducing system cost and board space.

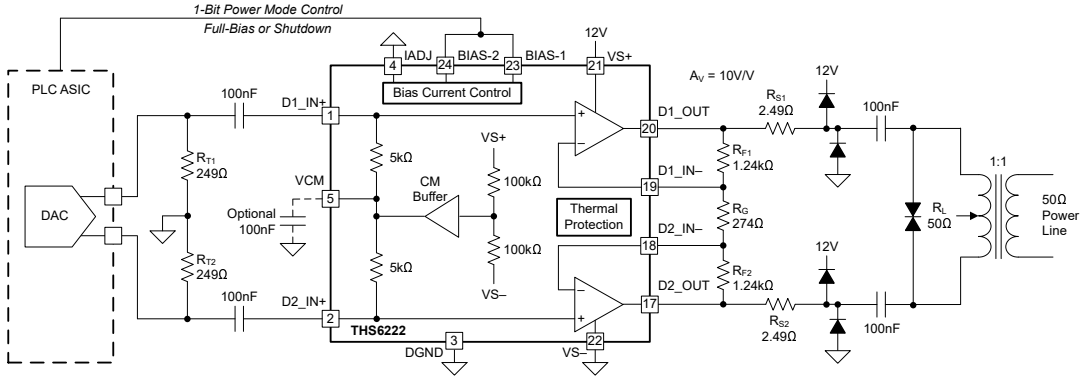
The wide output swing of 57V_{PP} (100Ω load) with 32V power supplies, coupled with over 650mA of current drive (25Ω load), allows for wide dynamic range that keeps distortion minimal.

The THS6222 is available in 16-pin and 24-pin VQFN packages with exposed thermal pad, and is specified for operation from –40°C to +85°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
THS6222	RGT (VQFN, 16)	3mm × 3mm
	RHF (VQFN, 24)	5mm × 4mm
	YS die (wafer sale, 19)	1261.00µm × 1641.00µm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Line-Driver Circuit Using the THS6222

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

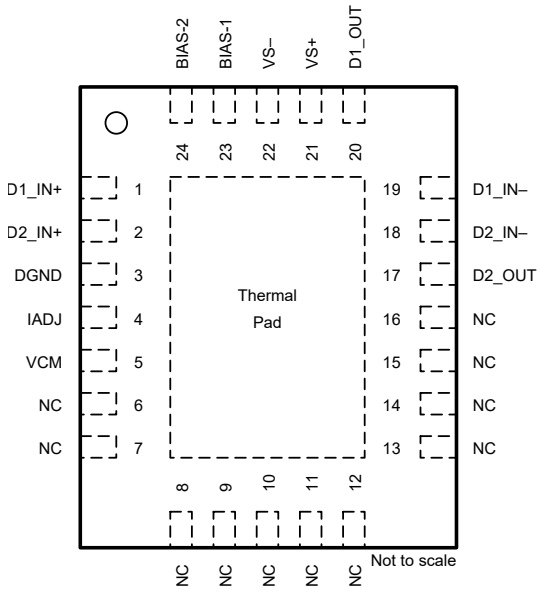


Figure 4-1. RHF Package, 24-Pin VQFN With Exposed Thermal Pad (Top View)

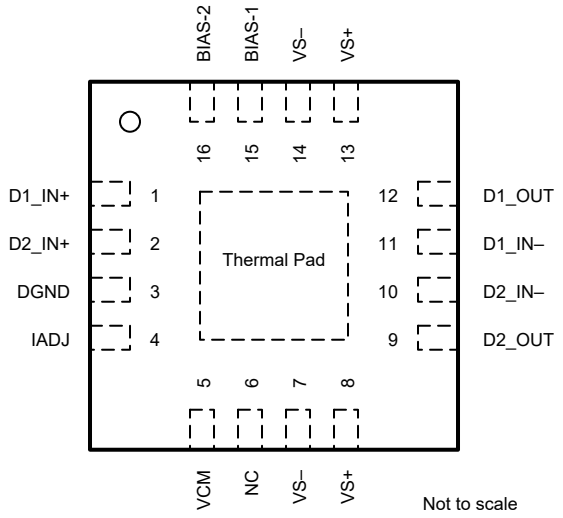


Figure 4-2. RGT Package, 16-Pin VQFN With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	RHF (VQFN)	RGT (VQFN)		
BIAS-1(1)	23	15	Input	Bias mode control, LSB
BIAS-2(1)	24	16	Input	Bias mode control, MSB
D1_IN–	19	11	Input	Amplifier D1 inverting input
D1_IN+	1	1	Input	Amplifier D1 noninverting input
D1_OUT	20	12	Output	Amplifier D1 output
D2_IN–	18	10	Input	Amplifier D2 inverting input
D2_IN+	2	2	Input	Amplifier D2 noninverting input
D2_OUT	17	9	Output	Amplifier D2 output
DGND(2)	3	3	Input	Ground reference for bias control pins
IADJ	4	4	Input	Bias current adjustment pin
NC	6-16	6	—	No internal connection
VCM	5	5	Output	Common-mode buffer output
VS–	22	7, 14	Power	Negative power-supply connection
VS+	21	8, 13	Power	Positive power-supply connection
Thermal Pad	Pad	Pad	Power	Electrically connected to die substrate and VS–. Connect to VS– on the printed circuit board (PCB) for best performance.

(1) The THS6222 defaults to the shutdown (disable) state if a signal is not present on the bias pins.
(2) The DGND pin ranges from VS– to (VS+) – 5V.

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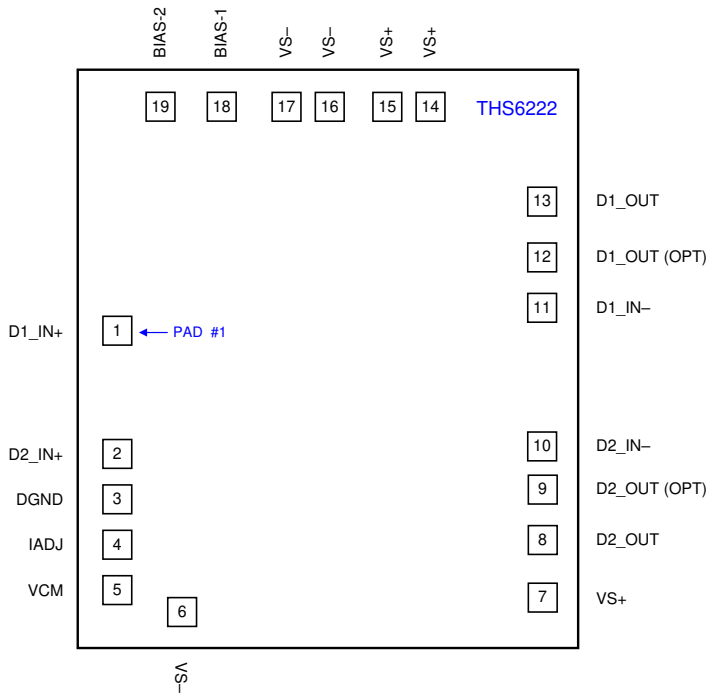


**Figure 4-3. YS Die,
19-Pad Wafer Sale
(Top View)**

Table 4-2. Bond Pad Functions

PAD		TYPE	DESCRIPTION
NAME	NO.		
BIAS-1(1)	18	Input	Bias mode parallel control, LSB
BIAS-2(1)	19	Input	Bias mode parallel control, MSB
D1_IN–	11	Input	Amplifier D1 inverting input
D1_IN+	1	Input	Amplifier D1 noninverting input
D1_OUT	13	Output	Amplifier D1 output (must be used for D1 output)
D1_OUT (OPT)	12	Output	Optional amplifier D1 output (pad can be left unconnected or connected to pad 13)
D2_IN–	10	Input	Amplifier D2 inverting input
D2_IN+	2	Input	Amplifier D2 noninverting input
D2_OUT	8	Output	Amplifier D2 output (must be used for D2 output)
D2_OUT (OPT)	9	Output	Optional amplifier D2 output (can be left unconnected or connected to pad 8)
DGND(2)	3	Input	Ground reference for bias control pins
IADJ	4	Input	Bias-current adjustment pin
VCM	5	Output	Common-mode buffer output
VS–	6, 16, 17	Power	Negative power-supply connection
VS+	7, 14, 15	Power	Positive power-supply connection
Backside	—	—	Connect to the lowest voltage potential on the die (generally $V_{S–}$)

(1) The THS6222 defaults to the shutdown (disable) state if a signal is not present on the bias pins.
(2) The DGND pin ranges from VS– to (VS+) – 5V.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, $V_S = (V_{S+}) – (V_{S–})$(2)		33	V
V_{BIAS}	Bias control pin voltage, referenced to DGND	0	16.5	V
V_{CM}	Common-mode voltage	See *Common-Mode Buffer*		V
$V_{IN/OUT/IADJ}$	All pins except VS+, VS–, VCM, and BIAS control	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
T_J	Maximum junction temperature (under any condition)		150	°C
T_{stg}	Storage temperature	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Refer to *Breakdown Supply Voltage* for breakdown test results.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, $V_S = (V_{S+}) – (V_{S–})$	8		32	V
DGND	DGND pin voltage	$V_{S–}$		$V_{S+} – 5$	V
T_A	Ambient operating air temperature	–40	25	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		THS6222		UNIT
		RHF (VQFN)	RGT (VQFN)	
		24 PINS	16 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	43.4	48.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	35	55.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	21.3	22.6	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	1.3	1.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	21.2	22.6	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	8.6	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics V_S = 12 V

at T_A ≈ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, VCM = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	A_V = 5 V/V, R_F = 1.5 kΩ, V_O = 2 V_{PP}			250		MHz
		A_V = 10 V/V, R_F = 1.24 kΩ, V_O = 2 V_{PP}			180		
		A_V = 15 V/V, R_F = 1 kΩ, V_O = 2 V_{PP}			165		
	0.1-dB bandwidth flatness				17		MHz
LSBW	Large-signal bandwidth	V_O = 16 V_{PP}			195		MHz
SR	Slew rate (20% to 80%)	V_O = 16-V step			5500		V/µs
	Rise and fall time (10% to 90%)	V_O = 2 V_{PP}			2.1		ns
HD2	2nd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 50 Ω	Full bias, f = 1 MHz		–80		dBc
			Mid bias, f = 1 MHz		–78		
			Low bias, f = 1 MHz		–78		
			Full bias, f = 10 MHz		–61		
			Mid bias, f = 10 MHz		–61		
			Low bias, f = 10 MHz		–61		
HD3	3rd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 50 Ω	Full bias, f = 1 MHz		–90		dBc
			Mid bias, f = 1 MHz		–86		
			Low bias, f = 1 MHz		–83		
			Full bias, f = 10 MHz		–69		
			Mid bias, f = 10 MHz		–65		
			Low bias, f = 10 MHz		–62		
e_n	Differential input voltage noise	f ≥ 1 MHz, input-referred, with and without 100 nF noise-decoupling capacitor on VCM pin			2.5		nV/√Hz
i_{n+}	Noninverting input current noise	f ≥ 1 MHz, each amplifier			1.4		pA/√Hz
i_{n-}	Inverting input current noise	f ≥ 1 MHz, each amplifier			18		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain				1300		kΩ
	Input offset voltage (each amplifier)				±12		mV
		T_A = –40°C			±16		
		T_A = 85°C			±11		
	Noninverting input bias current				±1		µA
		T_A = –40°C			±1		
		T_A = 85°C			±1		
	Inverting input bias current				±8		µA
		T_A = –40°C			±7		
		T_A = 85°C			±4		

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5.5 Electrical Characteristics V_S = 12 V (continued)

at T_A ≈ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, VCM = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
	Common-mode input voltage	Each input with respect to midsupply			±3.0		V
CMRR	Common-mode rejection ratio	Each input			64		dB
		T_A = –40°C			67		
		T_A = 85°C			62		
	Noninverting differential input resistance				10 || 2		kΩ || pF
	Inverting input resistance				43		Ω
COMMON-MODE BUFFER CHARACTERISTICS							
V_{CM-OS}	Common-mode offset voltage	Voltage at V_{CM} with respect to midsupply			±2.5		mV
		T_A = –40°C			±5		
		T_A = 85°C			±1		
	Common-mode voltage noise	With and without 100-nF V_{CM} noise-decoupling capacitor, f ≥ 50 kHz			20		nV/√Hz
	Common-mode output resistance	f = DC	AC-coupled inputs		650		Ω
			DC-coupled inputs		520		Ω
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	R_L = 100 Ω, R_S = 0 Ω			±9.7		V
		R_L = 50 Ω, R_S = 0 Ω			±9.3		
		R_L = 25 Ω, R_S = 0 Ω			±8.4		
I_O	Output current (sourcing and sinking)	R_L = 25 Ω, R_S = 0 Ω, based on V_O specification			±338		mA
	Short-circuit output current				±0.81		A
Z_O	Closed-loop output impedance	f = 1 MHz, differential			0.03		Ω
POWER SUPPLY							
DGND	DGND pin voltage			$V_{S–}$	0	V_{S+} – 5	V
I_{S+}	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)			19.5		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)			15		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)			10.4		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)			1.1		
$I_{S–}$	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)			18.8		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)			14.4		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)			9.8		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)			0.4		
	Current through DGND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)			0.8		mA
+PSRR	Positive power-supply rejection ratio	Differential			83		dB
–PSRR	Negative power-supply rejection ratio	Differential			83		dB

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5.5 Electrical Characteristics V_S = 12 V (continued)

at T_A ≈ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, VCM = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CONTROL						
	Bias control pin voltage	With respect to DGND, T_A = –40°C to +85°C	0	3.3	12	V
	Bias control pin logic threshold	Logic 1, with respect to DGND, T_A = –40°C to +85°C	2.1			V
		Logic 0, with respect to DGND, T_A = –40°C to +85°C			0.8	
	Bias control pin current(1)	BIAS-1, BIAS-2 = 0.5 V (logic 0)		–9.6		µA
		BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.3	1	
	Open-loop output impedance	Off bias (BIAS-1 = 1, BIAS-2 = 1)		70 || 5		MΩ || pF

(1) Current is considered positive out of the pin.

5.6 Electrical Characteristics V_S = 32 V

at T_A ≈ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 100 Ω, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_{CM} = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth, –3 dB	A_V = 5 V/V, R_F = 1.5 kΩ, V_O = 2 V_{PP}			285		MHz
		A_V = 10 V/V, R_F = 1.24 kΩ, V_O = 2 V_{PP}			205		
	0.1-dB bandwidth flatness				13		MHz
LSBW	Large-signal bandwidth	V_O = 40 V_{PP}			170		MHz
SR	Slew rate (20% to 80% level)	V_O = 40-V step			11,000		V/µs
	Rise and fall time	V_O = 2 V_{PP}			2		ns
HD2	2nd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 100 Ω	Full bias, f = 1 MHz		–86		dBc
			Low bias, f = 1 MHz		–79		
			Full bias, f = 10 MHz		–71		
			Low bias, f = 10 MHz		–63		
HD3	3rd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 100 Ω	Full bias, f = 1 MHz		–101		dBc
			Low bias, f = 1 MHz		–88		
			Full bias, f = 10 MHz		–80		
			Low bias, f = 10 MHz		–65		
e_n	Differential input voltage noise	f ≥ 1 MHz, input-referred			2.5		nV/√Hz
i_{n+}	Noninverting input current noise (each amplifier)	f ≥ 1 MHz			1.7		pA/√Hz
i_{n-}	Inverting input current noise (each amplifier)	f ≥ 1 MHz			18		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain				1500		kΩ
	Input offset voltage				±12		mV
	Input offset voltage drift	T_A = –40°C to +85°C			–40		µV/°C
	Input offset voltage matching	Amplifier A to B			±0.5		mV
	Noninverting input bias current				±1		µA
	Inverting input bias current				±6		µA
	Inverting input bias current matching				±8		µA

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5.6 Electrical Characteristics V_S = 32 V (continued)

at T_A ≈ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 100 Ω, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_{CM} = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
	Common-mode input voltage	Each input	±11	±12		V
CMRR	Common-mode rejection ratio	Each input	53	65		dB
	Noninverting input resistance			10 || 2		kΩ || pF
	Inverting input resistance			38		Ω
COMMON-MODE BUFFER CHARACTERISTICS						
V_{CM-OS}	Common-mode offset voltage	Voltage at V_{CM} with respect to midsupply		±3.9		mV
	Common-mode voltage noise	With and without 100-nF V_{CM} noise-decoupling capacitor, f ≥ 50 kHz		21		nV/√Hz
	Common-mode output resistance	f = DC		520		Ω
OUTPUT CHARACTERISTICS						
V_O	Output voltage swing(1)	R_L = 100 Ω		±28.5		V
		R_L = 25 Ω		±16.3		
I_O	Output current (sourcing and sinking) (1)	R_L = 25 Ω, based on V_O specification	±580	±665		mA
	Short-circuit output current			1		A
Z_O	Output impedance	f = 1 MHz, differential		0.01		Ω
POWER SUPPLY						
I_{S+}	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		23		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		17.7		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		12.2		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		1.5	1.8	
$I_{S–}$	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		22		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		16.7		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		11.2		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.5	0.8	
	Current through GND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)		1		mA
+PSRR	Positive power-supply rejection ratio	Differential		83		dB
–PSRR	Negative power-supply rejection ratio	Differential		77		dB
BIAS CONTROL						
	Bias control pin voltage	With respect to DGND, T_A = –40°C to +85°C	0	3.3	16.5	V
	Bias control pin logic threshold	Logic 1, with respect to DGND, T_A = –40°C to +85°C	1.9			V
		Logic 0, with respect to DGND, T_A = –40°C to +85°C			0.8	
	Bias control pin current(2)	BIAS-1, BIAS-2 = 0.5 V (logic 0)	–15	–10		µA
		BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.1	1	

(1) See *Output Voltage and Current Drive* and *Figure 5-51* for output voltage vs output current characteristics.
(2) Current is considered positive out of the pin.

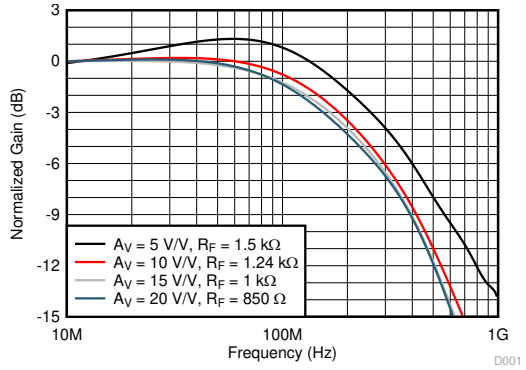
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5.7 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON}	Turn-on time delay: time for output to start tracking the input		25		ns
t_{OFF}	Turn-off time delay: time for output to stop tracking the input		275		ns

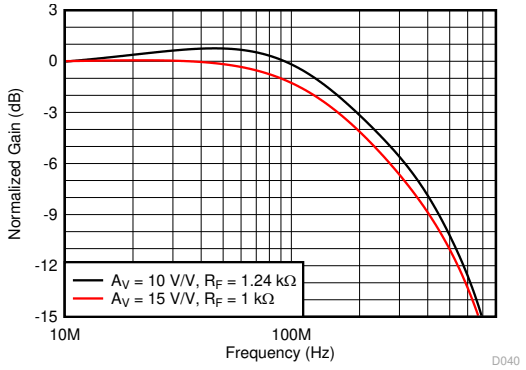
5.8 Typical Characteristics: V_S = 12 V

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



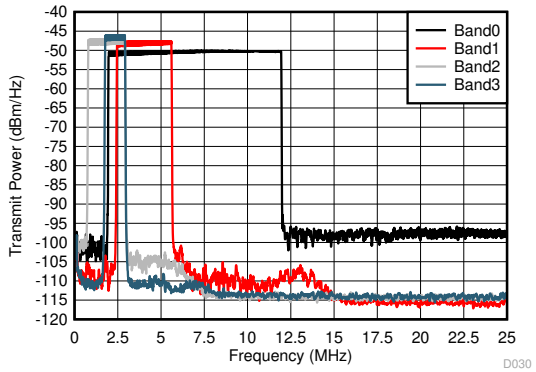
V_O = 2 V_{PP}

Figure 5-1. Small-Signal Frequency Response



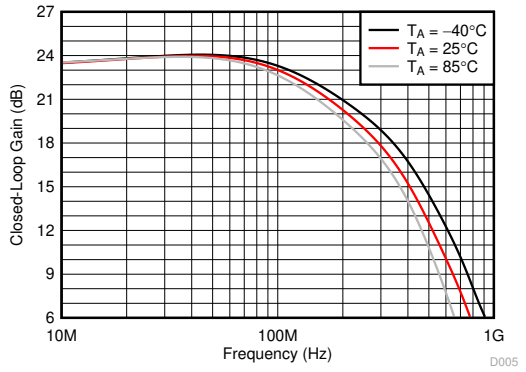
V_O = 16 V_{PP}

Figure 5-2. Large-Signal Frequency Response



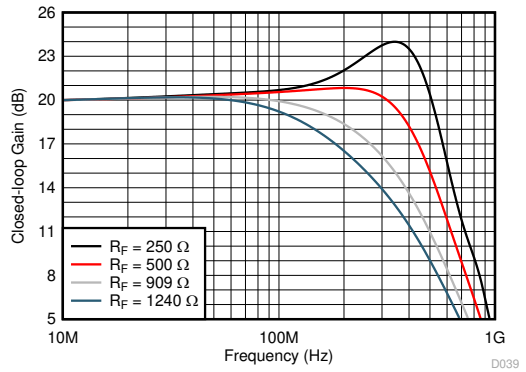
SGCC HPLC profiles, crest factor = 5 V/V, see the *Broadband PLC Line Driving* section for more details.

Figure 5-3. Out-of-Band Suppression



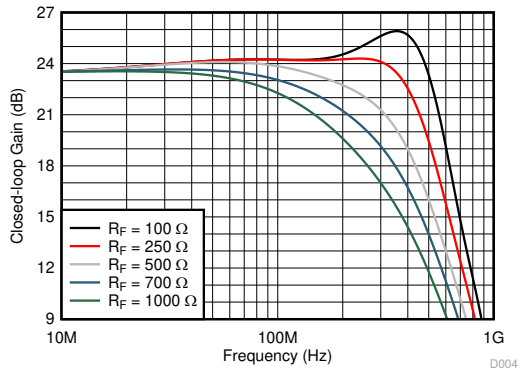
A_V = 15 V/V, V_O = 2 V_{PP}

Figure 5-4. Small-Signal Frequency Response vs Temperature



A_V = 10 V/V, V_O = 2 V_{PP}

Figure 5-5. Small-Signal Frequency Response vs R_F



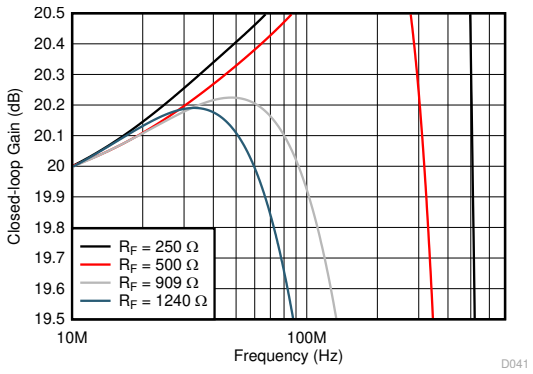
A_V = 15 V/V, V_O = 2 V_{PP}

Figure 5-6. Small-Signal Frequency Response vs R_F

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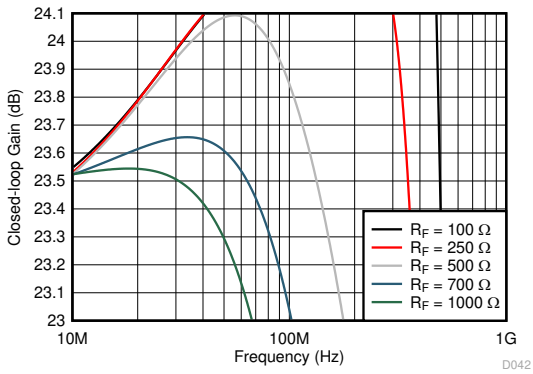
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



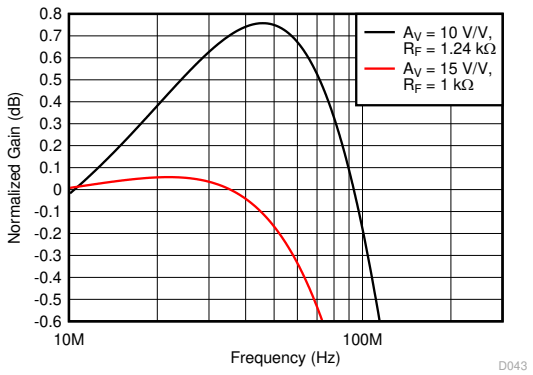
A_V = 10 V/V, V_O = 2 V_{PP}

Figure 5-7. Small-Signal Gain Flatness vs R_F



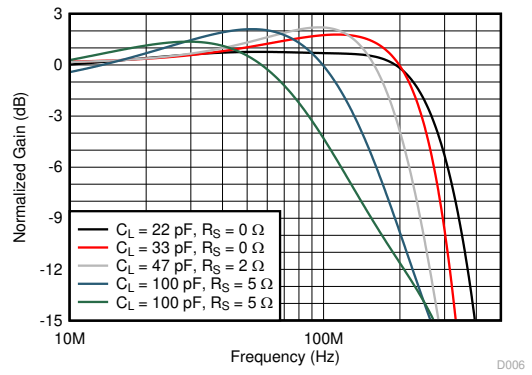
A_V = 15 V/V, V_O = 2 V_{PP}

Figure 5-8. Small-Signal Gain Flatness vs R_F



V_O = 16 V_{PP}

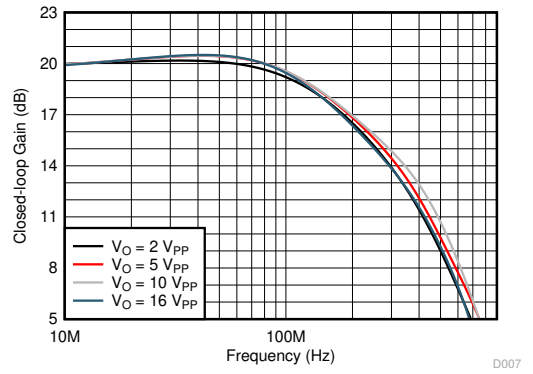
Figure 5-9. Large-Signal Gain Flatness



V_O = 100 mV_{PP}

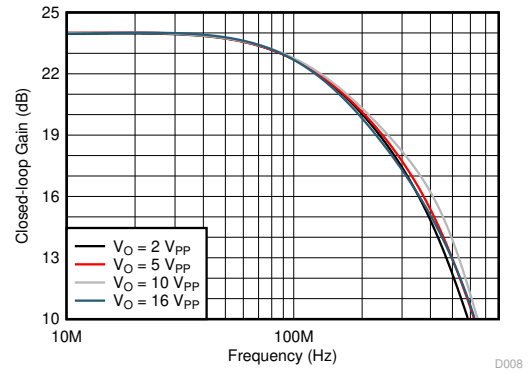
Frequency response is measured at the device output pin before the isolation resistor.

Figure 5-10. Small-Signal Frequency Response vs C_{LOAD}



A_V = 10 V/V

Figure 5-11. Large-Signal Frequency Response vs V_O



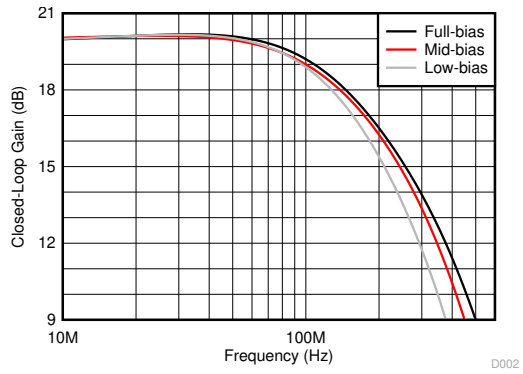
A_V = 15 V/V

Figure 5-12. Large-Signal Frequency Response vs V_O

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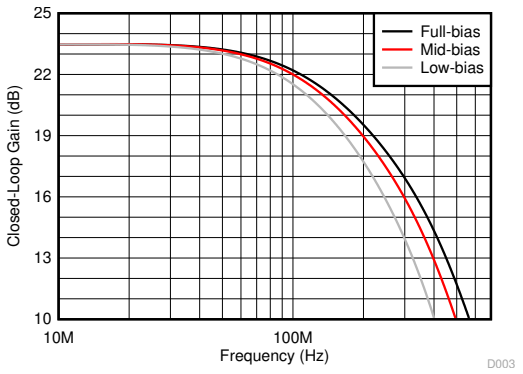
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



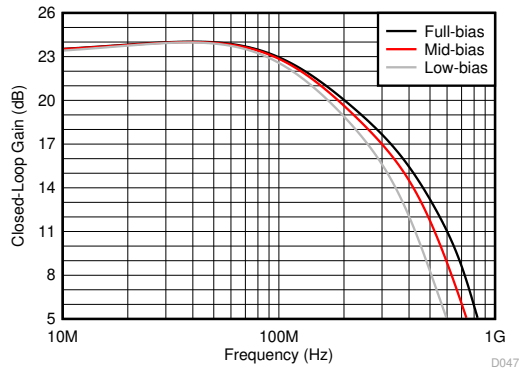
A_V = 10 V/V, V_O = 2 V_{PP}

Figure 5-13. Small-Signal Frequency Response vs Bias Modes



A_V = 15 V/V, V_O = 2 V_{PP}

Figure 5-14. Small-Signal Frequency Response vs Bias Modes



A_V = 15 V/V, V_O = 16 V_{PP}

Figure 5-15. Large-Signal Frequency Response vs Bias Modes

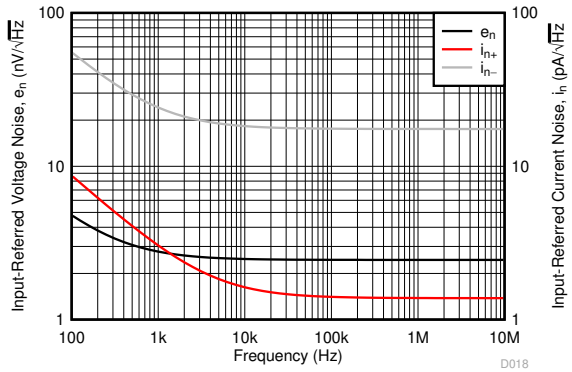
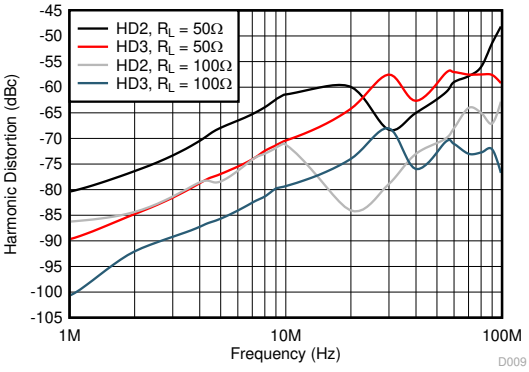
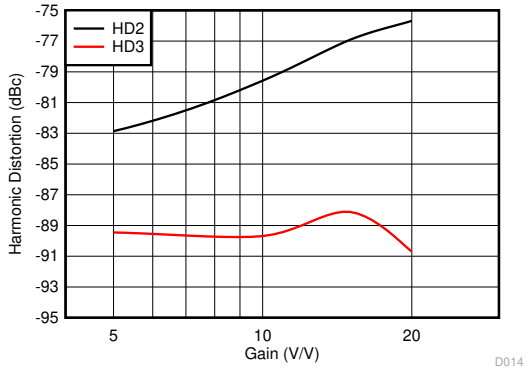


Figure 5-16. Input Voltage and Current Noise Density vs Frequency



V_O = 2 V_{PP}

Figure 5-17. Harmonic Distortion vs Frequency



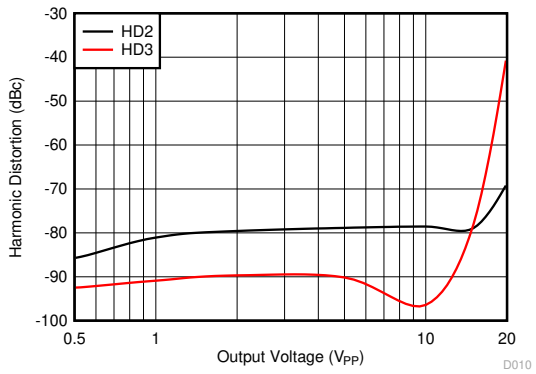
f = 1 MHz, V_O = 2 V_{PP}

Figure 5-18. Harmonic Distortion vs Gain

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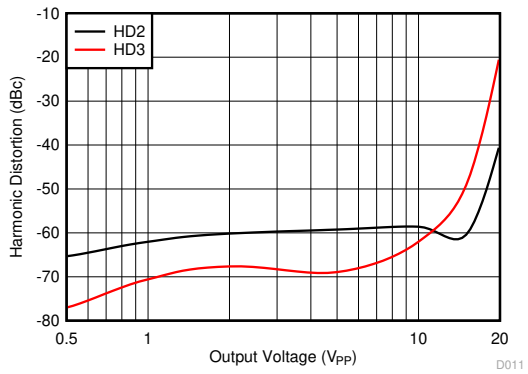
5.8 Typical Characteristics: V_S = 12 V (continued)

at T_A ≈ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



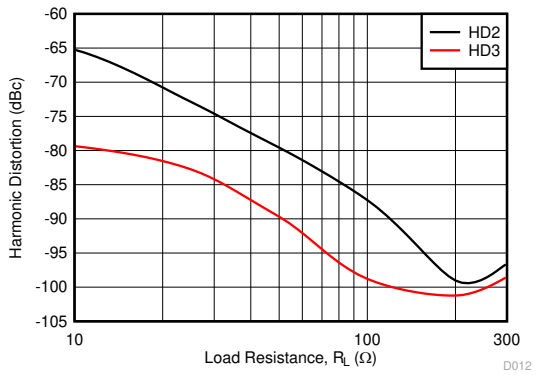
f = 1 MHz, A_V = 10 V/V

Figure 5-19. Harmonic Distortion vs V_O



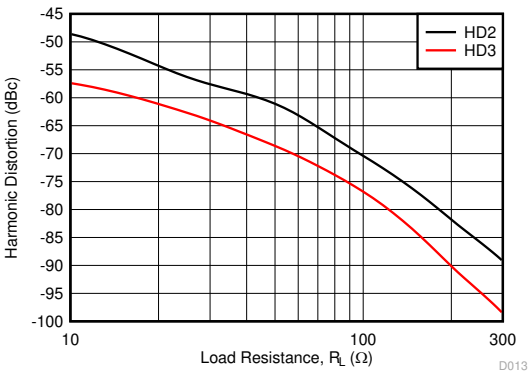
f = 10 MHz, A_V = 10 V/V

Figure 5-20. Harmonic Distortion vs V_O



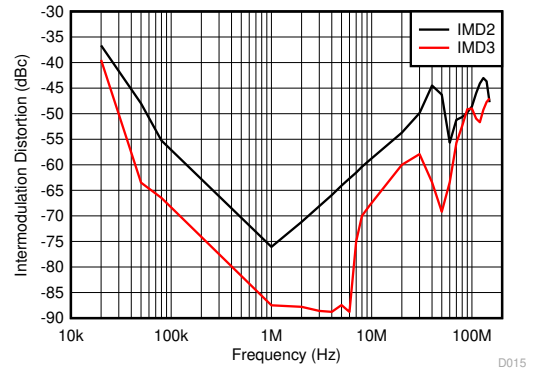
f = 1 MHz, V_O = 2 V_{PP}, A_V = 10 V/V

Figure 5-21. Harmonic Distortion vs R_L



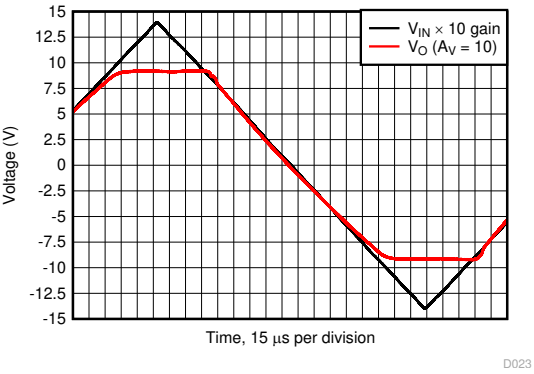
f = 10 MHz, V_O = 2 V_{PP}, A_V = 10 V/V

Figure 5-22. Harmonic Distortion vs R_L



±12.2 kHz tone spacing, V_O = 2 V_{PP} per tone

Figure 5-23. Intermodulation Distortion vs Frequency



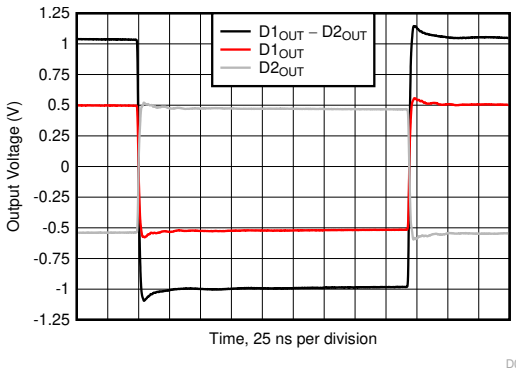
V_{IN} = 2.8-V_{PP} triangular waveform

Figure 5-24. Overdrive Recovery

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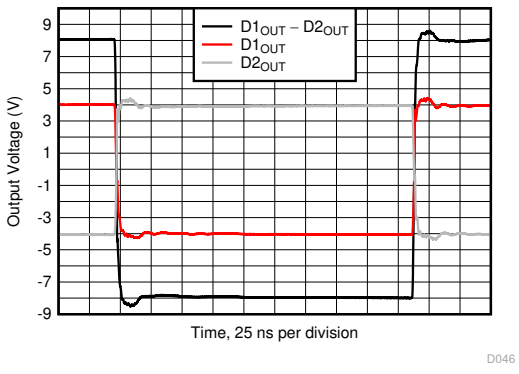
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



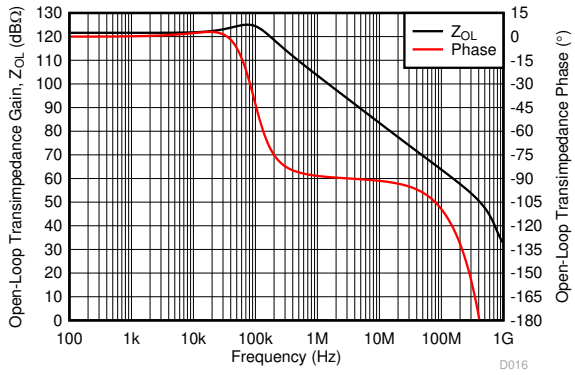
V_O step = 2 V_{PP}

Figure 5-25. Small-Signal Pulse Response



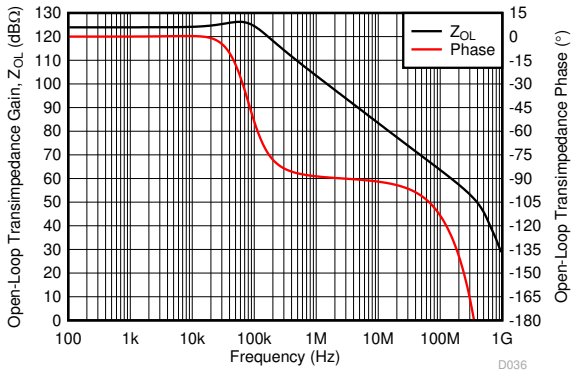
V_O step = 16 V_{PP}

Figure 5-26. Large-Signal Pulse Response



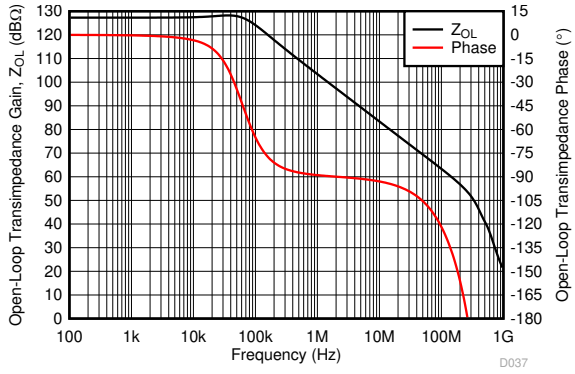
Full-bias simulation

Figure 5-27. Open-Loop Transimpedance Gain and Phase vs Frequency



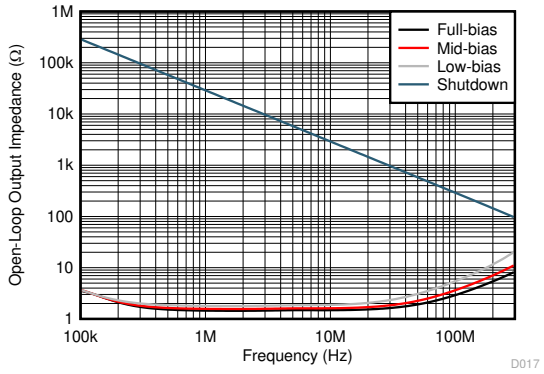
Mid-bias simulation

Figure 5-28. Open-Loop Transimpedance Gain and Phase vs Frequency



Low-bias simulation

Figure 5-29. Open-Loop Transimpedance Gain and Phase vs Frequency



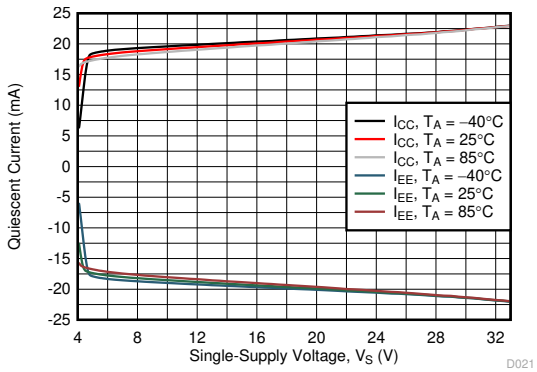
Simulation

Figure 5-30. Open-Loop Output Impedance vs Frequency

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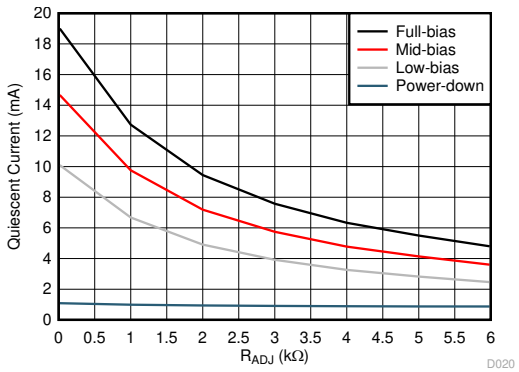
5.8 Typical Characteristics: V_S = 12 V (continued)

at T_A ≈ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



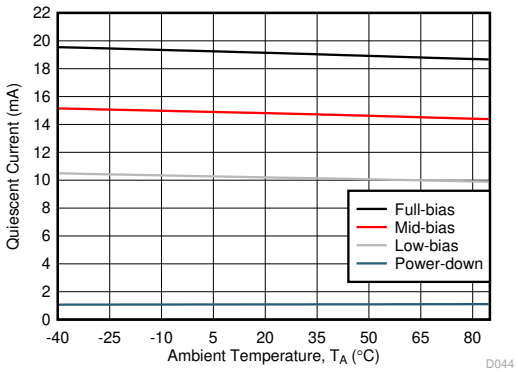
R_L = no load, average of 30 devices

Figure 5-31. Quiescent Current vs Single-Supply Voltage



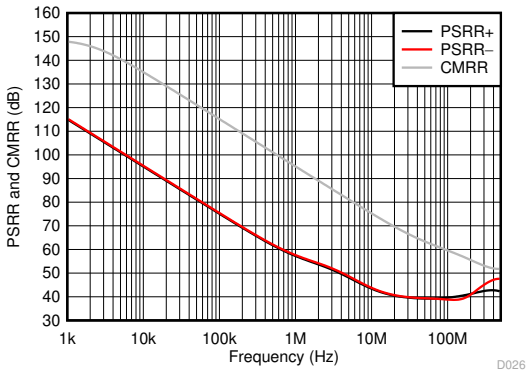
Average of 30 devices

Figure 5-32. Quiescent Current vs R_{ADJ}



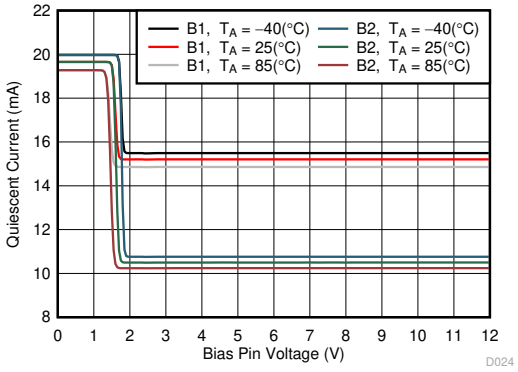
R_L = no load, average of 30 devices

Figure 5-33. Quiescent Current vs Temperature



T_J = 50°C, simulation

Figure 5-34. PSRR and CMRR vs Frequency



B1 = full-bias to mid-bias transition with B2 = DGND, B2 = full-bias to low-bias transition with B1 = DGND, DGND = $V_{S–}$

Figure 5-35. Mode Transition Voltage Threshold

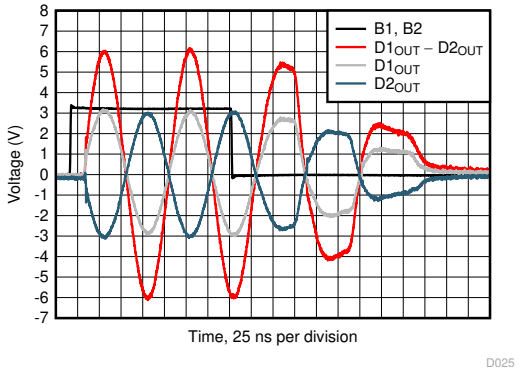
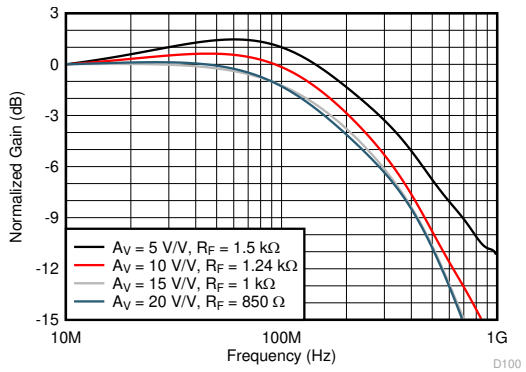


Figure 5-36. Full-Bias and Shutdown Mode Transition Timing

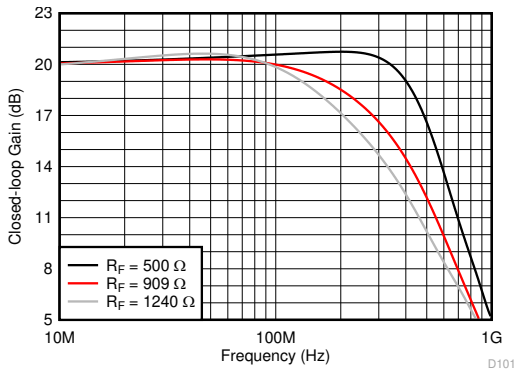
5.9 Typical Characteristics: V_S = 32 V

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



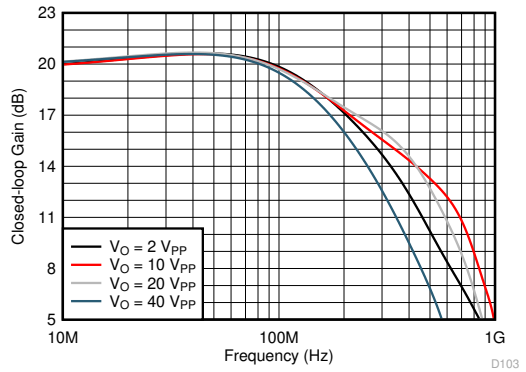
V_O = 2 V_{PP}

Figure 5-37. Small-Signal Frequency Response



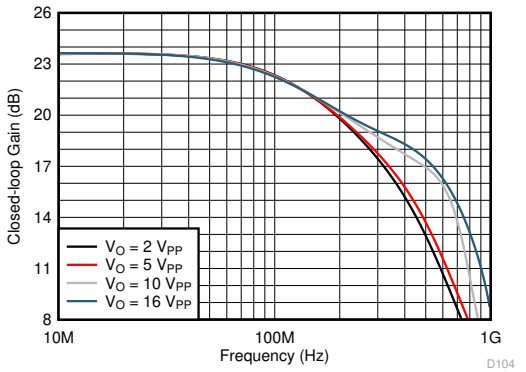
V_O = 2 V_{PP}

Figure 5-38. Small-Signal Frequency Response vs R_F



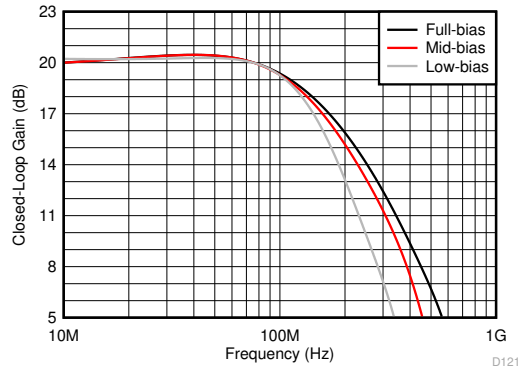
A_V = 10 V/V

Figure 5-39. Large-Signal Frequency Response vs V_O



A_V = 15 V/V

Figure 5-40. Large-Signal Frequency Response vs V_O



V_O = 40 V_{PP}

Figure 5-41. Large-Signal Frequency Response vs Bias Modes

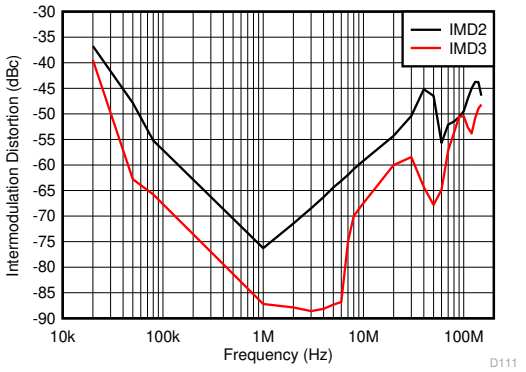
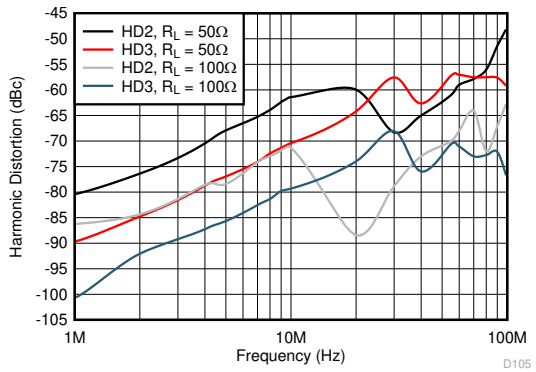


Figure 5-42. Intermodulation Distortion vs Frequency

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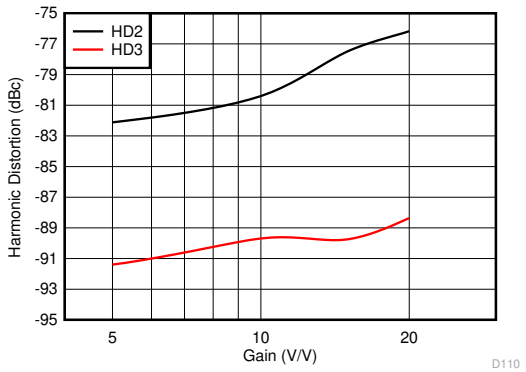
5.9 Typical Characteristics: V_S = 32 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



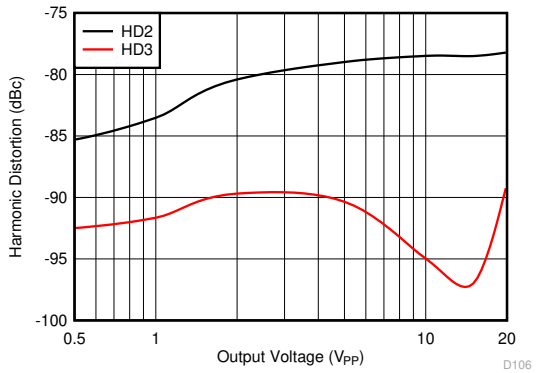
V_O = 2 V_{PP}

Figure 5-43. Harmonic Distortion vs Frequency



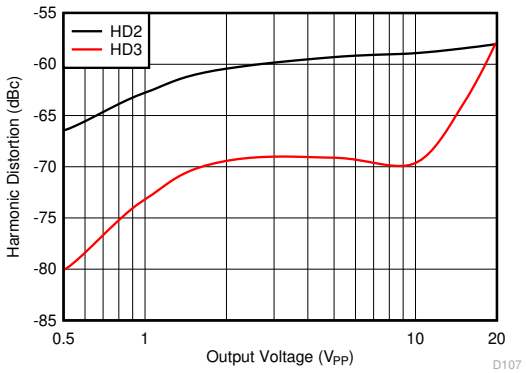
f = 1 MHz, V_O = 2 V_{PP} R_L = 50 Ω

Figure 5-44. Harmonic Distortion vs Gain



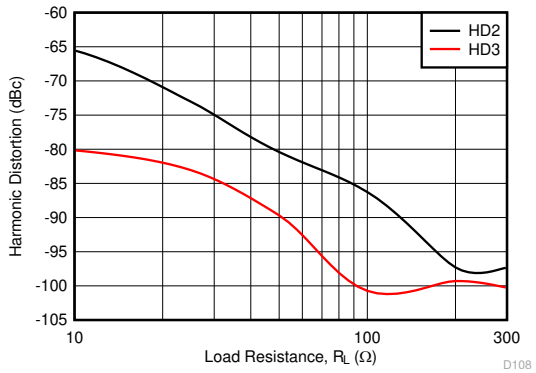
f = 1 MHz, R_L = 50 Ω

Figure 5-45. Harmonic Distortion vs V_O



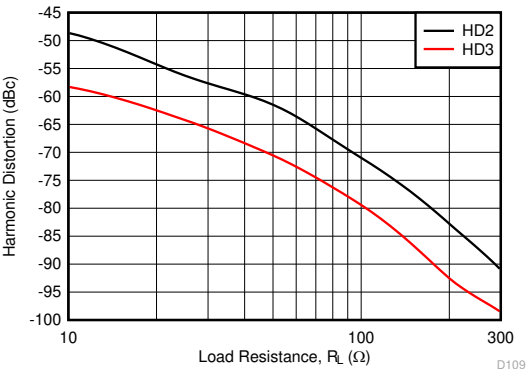
f = 10 MHz, R_L = 50 Ω

Figure 5-46. Harmonic Distortion vs V_O



f = 1 MHz, V_O = 2 V_{PP}

Figure 5-47. Harmonic Distortion vs R_L

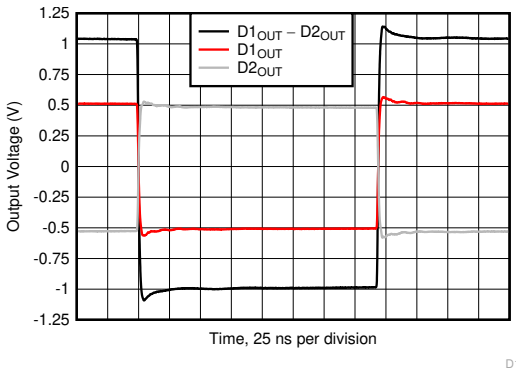


f = 10 MHz, V_O = 2 V_{PP}

Figure 5-48. Harmonic Distortion vs R_L

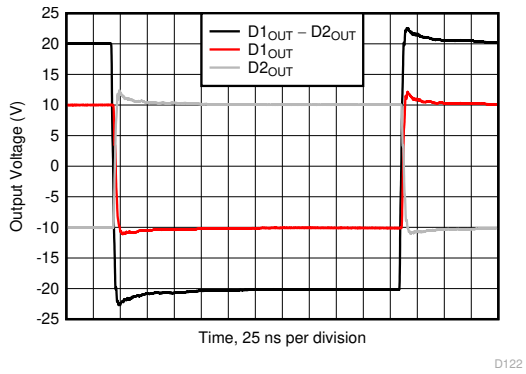
5.9 Typical Characteristics: V_S = 32 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



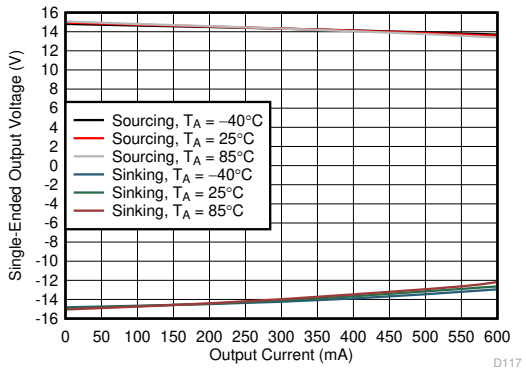
V_O step = 2 V_{PP}

Figure 5-49. Small-Signal Pulse Response



V_O step = 40 V_{PP}

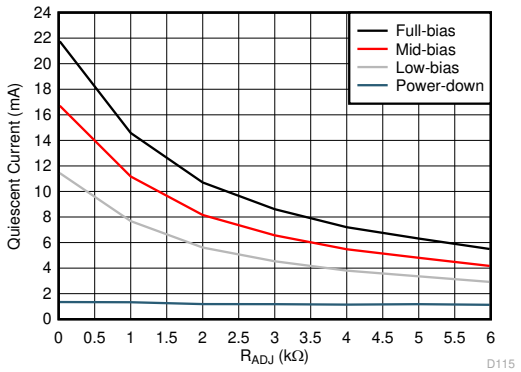
Figure 5-50. Large-Signal Pulse Response



Average of 30 devices

Output voltage was slammed and I_O was pulsed to maintain T_J as close to T_A as possible.

Figure 5-51. Single-Ended Output Voltage vs I_O and Temperature



Average of 30 devices

Figure 5-52. Quiescent Current vs R_{ADJ}

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6 Detailed Description

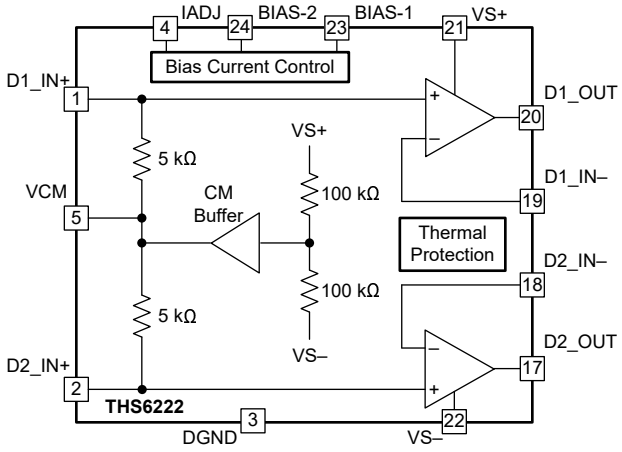
6.1 Overview

The THS6222 is a differential line-driver amplifier with a current-feedback architecture. The device is targeted for use in line-driver applications such as narrow-band and broadband power-line communications (PLC) that are often found in smart-metering and home-networking applications.

The THS6222 is designed as a single-port differential line driver. For the THS6222 to function as a drop-in replacement for the THS6212, tie the thermal pad to VS–. The integrated common-mode buffer featured in the THS6222 reduces the number of external components required for level shifting the input common-mode voltage in PLC applications that are often ac coupled, resulting in space savings on the circuit board and reducing the overall system cost. As a result of the THS6222 architecture, the two current-feedback amplifiers (D1 and D2) cannot be used independently; therefore, always drive these amplifiers differentially.

The architecture of the THS6222 is designed to provide maximum flexibility with adjustable power modes that are selectable based on application performance requirements, and also provide an external current adjustment pin (IADJ) to further optimize the quiescent power of the device. The wide output swing (18.6 V_{PP}) into 50-Ω differential loads with 12-V power supplies and high current drive of the THS6222 make the device an excellent choice for high-power, line-driving applications. By using 32-V power supplies and with good thermal design that keep the device within the safe operating temperature, the THS6222 is capable of swinging 57 V_{PP} into 100-Ω loads.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Common-Mode Buffer

The THS6222 is a differential line driver that features an integrated common-mode buffer. Figure 7-2 shows that the most-common line-driving applications for the THS6222 are ac-coupled applications. Therefore, common-mode shift the inputs to confirm the input signals are within the common-mode specifications of the device. To maximize the dynamic range, the common-mode voltage is shifted to midsupply in most ac-coupled applications. With the integrated common-mode buffer, no external components are required to shift the input common-mode voltage. Engineers often choose to connect a noise-decoupling capacitor to the VCM pin. However, as shown in Figure 6-1, assuming the circuit is reasonably shielded from external noise sources, no difference in common-mode noise is observed with the 100-nF capacitor or without the capacitor.

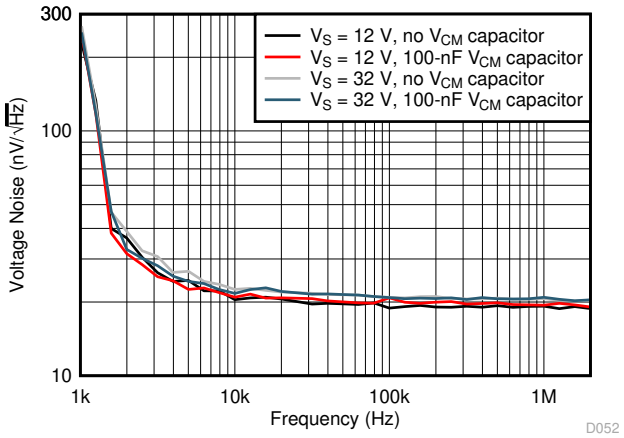


Figure 6-1. Common-Mode Voltage Noise Density vs Frequency

There are ESD protection diodes in series directly at the output of the common-mode buffer between the internal 520-Ω resistor and the common-mode buffer output. These diodes are referenced to midsupply. Any voltage that is 1.4 V greater or less than the midsupply applied to the VCM pin forward biases the protection diodes. This biasing results in either current flowing into or out of the VCM pin. The current is limited by the 520-Ω resistor in series, but to prevent permanent damage to the device, limit the current to the specifications in the *Absolute Maximum Ratings*.

6.3.2 Thermal Protection and Package Power Dissipation

The THS6222 is designed with thermal protection that automatically puts the device in shutdown mode when the junction temperature reaches approximately 175°C. In this mode, the device behavior is the same as if the bias pins are used to power-down the device. The device resumes normal operation when the junction temperature reaches approximately 145°C. In general, the thermal shutdown condition must be avoided. If and when the thermal protection triggers, thermal cycling occurs where the device repeatedly goes in and out of thermal shutdown until the junction temperature stabilizes to a value that prevents thermal shutdown.

A common technique to calculate the maximum power dissipation that a device can withstand is by using the junction-to-ambient thermal resistance ($R_{\theta JA}$), provided in the *Thermal Information* table. Using the equation power dissipation = (junction temperature, T_J – ambient temperature, T_A) / $R_{\theta JA}$, the amount of power a package can dissipate can be estimated. Figure 6-2 illustrates the package power dissipation based on this equation to reach junction temperatures of 125°C and 150°C at various ambient temperatures. The $R_{\theta JA}$ value is determined using industry standard JEDEC specifications and allows ease of comparing various packages. Power greater than that in Figure 6-2 can be dissipated in a package by good printed circuit board (PCB) thermal design, using heat sinks, and or active cooling techniques. See the *Thermal Design By Insight, Not Hindsight* application report for an in-depth discussion on thermal design.

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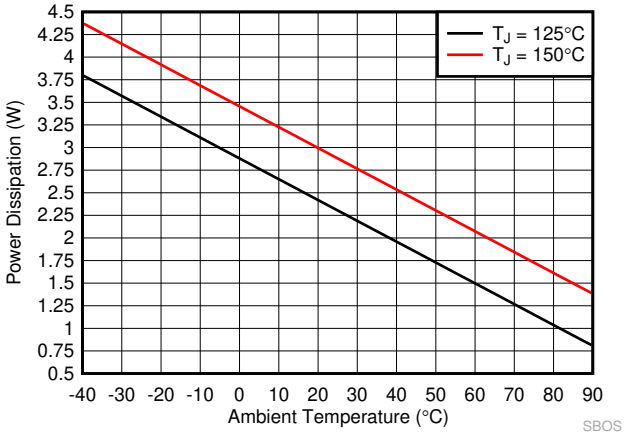
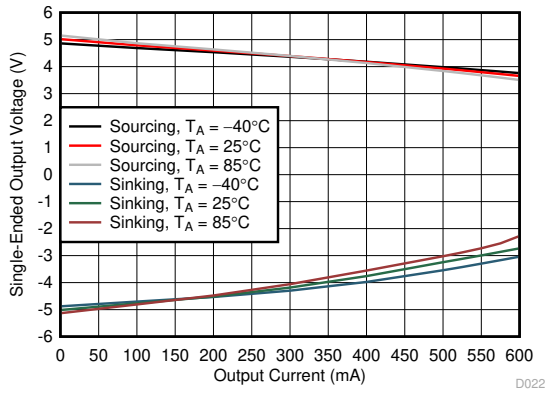


Figure 6-2. Package Power Dissipation vs Ambient Temperature

6.3.3 Output Voltage and Current Drive

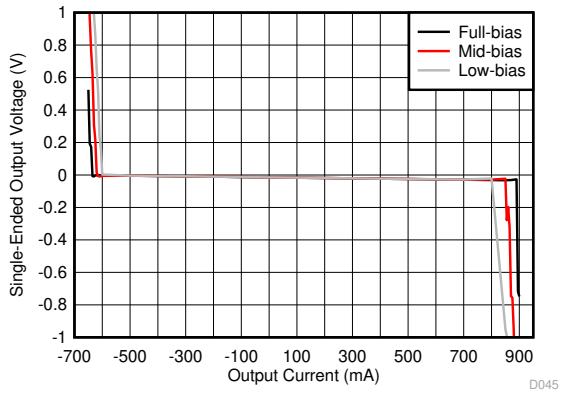
The THS6222 provides output voltage and current capabilities that are unsurpassed in a low-cost, monolithic op amp. Under no load at room temperature, the output voltage typically swings closer than 1.1 V to either supply rail and typically swings to within 1.1 V of either supply with a 100-Ω differential load. The THS6222 can deliver over 350 mA of current with a 25-Ω load.

Good thermal design of the system is important (including use of heat sinks and active cooling methods) if the THS6222 is pushed to the limits of the output drive capabilities. Figure 6-3 and Figure 6-4 show the output drive of the THS6222 under two different sets of conditions where T_A is approximately equal to T_J. In practical applications, T_J is often much higher than T_A and highly depends on the device configuration, signal parameters, and PCB thermal design. To represent the full output-drive capability of the THS6222 in Figure 6-3 and Figure 6-4, $T_J \approx T_A$ is achieved by pulsing or sweeping the output current for a duration of less than 100 ms.



V_S = 12 V, $T_J \approx T_A$

Figure 6-3. Slammed Single-Ended Output Voltage vs I_O and Temperature



V_S = 12 V, $T_J \approx T_A \approx$ 25°C

Figure 6-4. Linear Single-Ended Output Voltage vs I_O and Temperature

In Figure 6-3, the output voltages are differentially slammed to the rail and the output current is single-endedly sourced or sunk using a source measure unit (SMU) for less than 100 ms. The single-ended output voltage of each output is then measured prior to removing the load current. After removing the load current, the outputs are brought back to mid-supply before repeating the measurement for different load currents. This entire process is repeated for each ambient temperature. Under the slammed output voltage condition of Figure 6-3, the output transistors are in saturation and the transistors start going into linear operation as the output swing is backed off for a given I_O,

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In Figure 6-4, the inputs are floated and the output voltages are allowed to settle to the mid-supply voltage. The load current is then single-endedly swept for sourcing (greater than 0 mA) and sinking (less than 0 mA) conditions and the single-ended output voltage is measured at each current-forcing condition. The current sweep is completed in a few seconds (approximately 3 s to 4 s) so as not to significantly raise the junction temperature (T_J) of the device from the ambient temperature (T_A). The output is not swinging and the output transistors are in linear operation in Figure 6-4 until the current drawn exceeds the device capabilities, at which point the output voltage starts to deviate quickly from the no load output voltage.

To maintain maximum output stage linearity, output short-circuit protection is not provided. This absence of short-circuit protection is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin, in most cases, permanently damages the amplifier.

6.3.4 Breakdown Supply Voltage

To estimate the margin beyond the maximum supply voltage specified in the *Absolute Maximum Ratings* table and exercise the robustness of the device, several typical units were tested beyond the specifications in the *Absolute Maximum Ratings* table. Figure 6-5 shows the configuration used for the test. The supply voltage, V_S, was swept manually and quiescent current was recorded at each 0.5-V supply voltage increment. Figure 6-6 shows the results of the single-supply voltage where the typical units started breaking. Under a similar configuration as the one shown in Figure 6-5, a unit was subjected to V_S = 42 V for 168 hours and tested for quiescent current at the beginning and at the end of the test. There was no notable difference in the quiescent current before and after the 168 hours of testing and the device did not show any signs of damage or abnormality.

The primary objective of these tests was to estimate the margins of robustness for typical devices and does not imply performance or maximum limits beyond those specified in the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables.

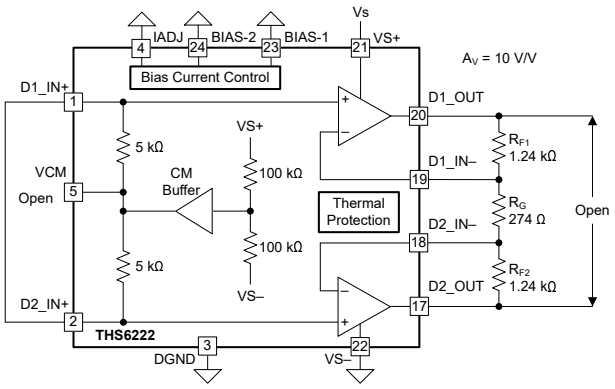


Figure 6-5. Breakdown Supply Voltage Test Configuration

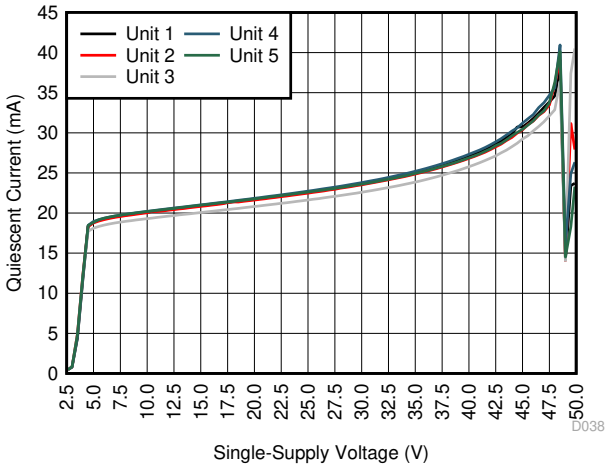


Figure 6-6. Typical Device Breakdown Supply Voltage (T_A = 27°C)

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6.3.5 Surge Test Results

Line drivers such as the THS6222 often directly interface with power lines through a transformer and various protection components in high-speed power line communications (HPLC) smart-meters and digital subscriber line (DSL) applications. Surge testing is an important requirement for such applications. To validate the performance and surge survivability of the THS6222, the THS6222 circuit configuration shown in Figure 6-7 was subjected to a ±4-kV common-mode surge and a ±2-kV differential-mode surge. The common-mode and differential-mode surge voltages were applied at V_{CM} and V_{DIFF}, respectively, in Figure 6-7. The 1.2/50-µs surge profile was used per the IEC 61000-4-5 test with R_{EQ} = 42 Ω, as explained in the *TI's IEC 61000-4-x Tests and Procedures* application report. Five devices were tested in full-bias and shutdown modes, and were subjected to the surge five times for each polarity. No device showed any discernible change in quiescent current after being subjected to the surge test, and the out-of-band suppression tests did not show any performance deterioration either; see Figure 6-8 through Figure 6-11 for the state grid corporation of China (SGCC) HPLC bands.

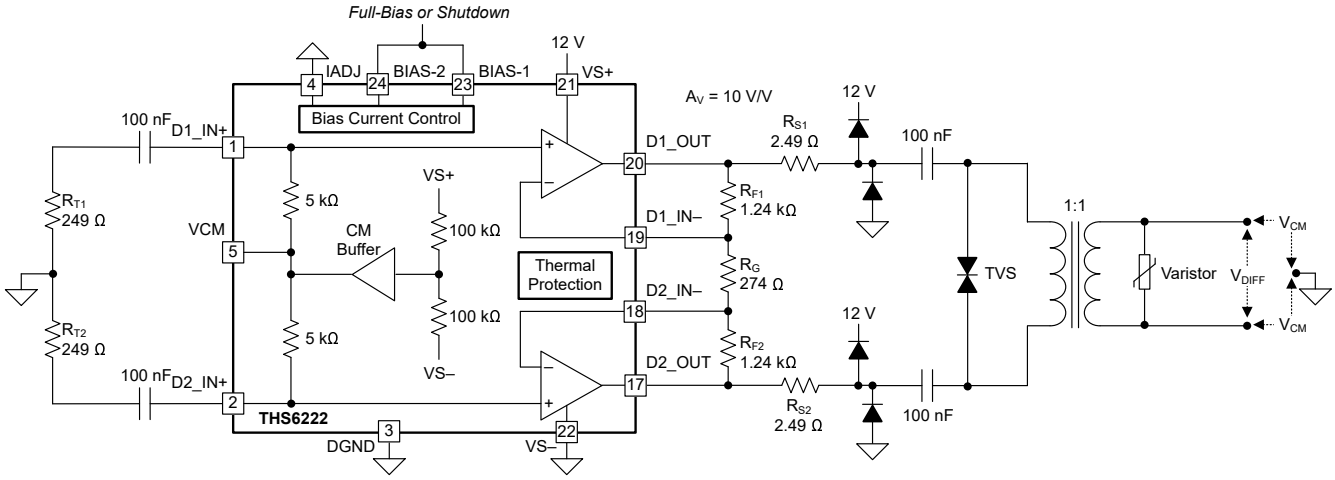


Figure 6-7. Surge Test Configuration

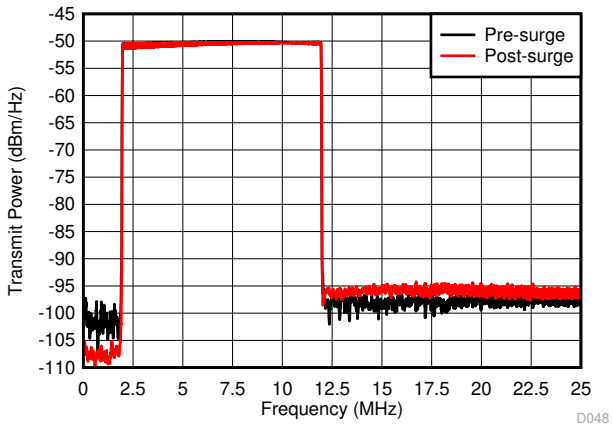


Figure 6-8. China SGCC HPLC Band0 Pre-Surge and Post-Surge

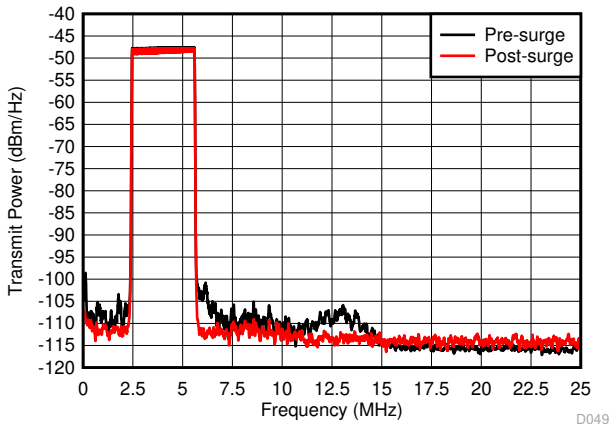


Figure 6-9. China SGCC HPLC Band1 Pre-Surge and Post-Surge

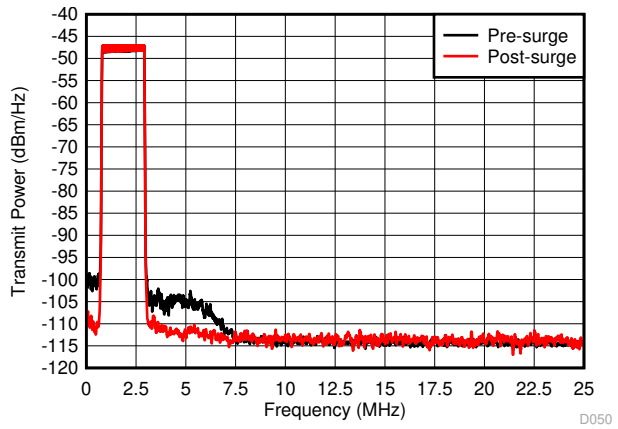


Figure 6-10. China SGCC HPLC Band2 Pre-Surge and Post-Surge

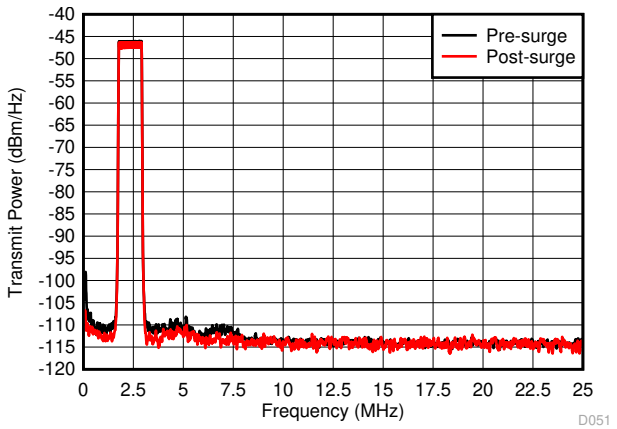


Figure 6-11. China SGCC HPLC Band3 Pre-Surge and Post-Surge

6.4 Device Functional Modes

The THS6222 has four different functional modes set by the BIAS-1 and BIAS-2 pins. Table 6-1 shows the truth table for the device mode pin configuration and the associated description of each mode.

Table 6-1. BIAS-1 and BIAS-2 Logic Table

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full-bias mode (100%)	Amplifiers on with lowest distortion possible
1	0	Mid-bias mode (75%)	Amplifiers on with power savings and a reduction in distortion performance
0	1	Low-bias mode (50%)	Amplifiers on with enhanced power savings and a reduction of overall performance
1	1	Shutdown mode	Amplifiers off and output is high impedance

If the PLC application requires switching the line driver between all four power modes and if the PLC application-specific integrated circuit (ASIC) has two control bits, then the two control bits can be connected to the bias pins BIAS-1 and BIAS-2 for switching between any of the four power modes. Most PLC applications, however, only require the line driver to switch between one of the three active power modes and the shutdown mode. This type of 1-bit power mode control is illustrated in Figure 7-1, where the line driver can be switched between the full-bias and shutdown modes using just one control bit from the PLC ASIC. If switching between the mid-bias or low-bias modes and the shutdown mode is required for the application, then either the BIAS-1 or BIAS-2 pin can be connected to ground and the control pin from the PLC ASIC can be connected to the non-grounded BIAS pin.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The THS6222 is typically used for high output power line-driving applications with various load conditions, as is often the case in power line communications (PLC) applications. In the *Typical Applications* section, the amplifier is presented in a typical, broadband, current-feedback configuration driving a 50 Ω line load; however, the amplifier is also applicable for many different general-purpose and specific line-driving applications beyond what is shown in the *Typical Applications* section.

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7.2 Typical Applications

7.2.1 Broadband PLC Line Driving

The THS6222 provides the exceptional ac performance of a wideband current-feedback op amp with a highly linear, high-power output stage. The low output headroom requirement and high output current drive capability makes the THS6222 an excellent choice for 12 V PLC applications. The primary advantage of a current-feedback op amp such as the THS6222 over a voltage-feedback op amp is that the ac performance (bandwidth and distortion) is relatively independent of signal gain. Figure 7-1 shows a typical ac-coupled broadband PLC application circuit where a current-output digital-to-analog converter (DAC) of the PLC application-specific integrated circuit (ASIC) drives the inputs of the THS6222. Though Figure 7-1 shows the THS6222 interfacing with a current-output DAC, the THS6222 can just as easily be interfaced with a voltage-output DAC by using much larger terminating resistors, R_{T1} and R_{T2}.

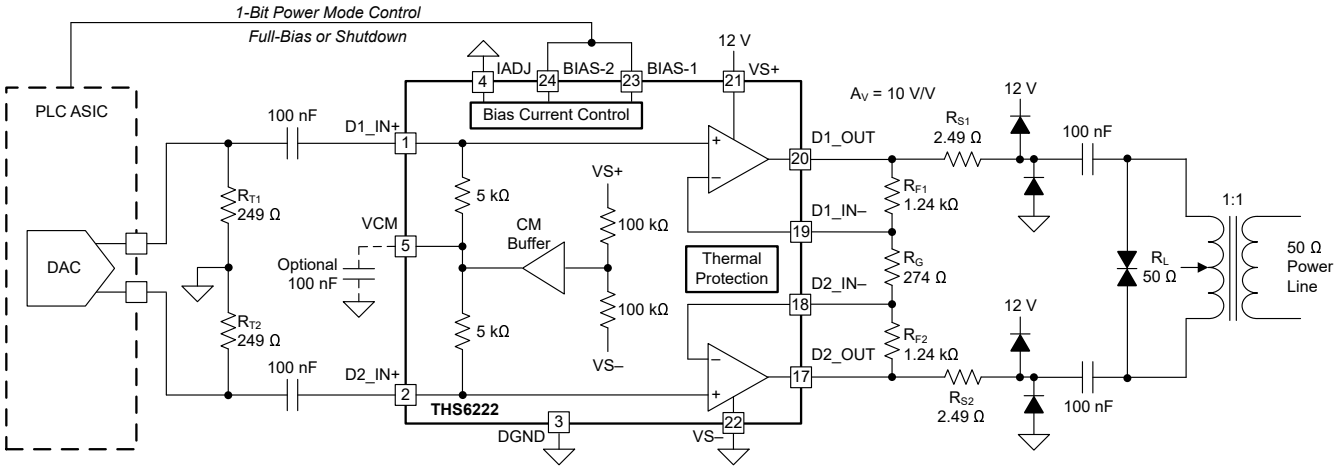


Figure 7-1. Typical Broadband PLC Configuration

7.2.1.1 Design Requirements

The main design requirements for an ac-coupled wideband current-feedback operation are to choose power supplies that satisfy the output voltage requirement, and also to use a feedback resistor value that allows for the proper bandwidth while maintaining stability. Use the design requirements shown in Table 7-1 to design a broadband PLC application circuit.

Table 7-1. Design Requirements

DESIGN PARAMETER	VALUE
Power supply	12 V, single-supply
Differential gain, A_V	10 V/V
Spectrum profile	China SGCC HPLC band0, band1, band2, and band3
In-band power spectral density	–50 dBm/Hz
Minimum out-of-band suppression	35 dB

7.2.1.2 Detailed Design Procedure

The closed-loop gain equation for a differential line driver such as the THS6222 is given as $A_V = 1 + 2 \times (R_F / R_G)$, where $R_F = R_{F1} = R_{F2}$. The THS6222 is a current-feedback amplifier and thus the bandwidth of the closed-loop configuration is set by the value of the R_F resistor. This advantage of the current-feedback architecture allows for flexibility in setting the differential gain by choosing the value of the R_G resistor without reducing the bandwidth as is the case with voltage-feedback amplifiers. The THS6222 is designed to provide excellent bandwidth performance with $R_{F1} = R_{F2} = 1.24$ kΩ. To configure the device in a gain of 10 V/V, the R_G resistor is chosen to be 274 Ω. See the TI Precision Labs for more details on how to choose the R_F resistor to optimize the performance of a current-feedback amplifier.

Often, a key requirement for PLC applications is the out-of-band suppression specifications. The in-band frequencies carry the encoded data with a certain power level. The line driver must not generate any spurs beyond a certain power level outside the in-band spectrum. In the design requirements of this application example, the minimum out-of-band suppression specification of 35 dB means there must be no frequency spurs in the out-of-band spectrum beyond the –80 dBm/Hz power spectral density, considering the in-band power spectral density is –50 dBm/Hz.

The circuit shown in Figure 7-2 measures the out-of-band suppression specification. The minor difference in components between the circuits of Figure 7-1 and Figure 7-2 does not have any significant impact on the out-of-band suppression results.

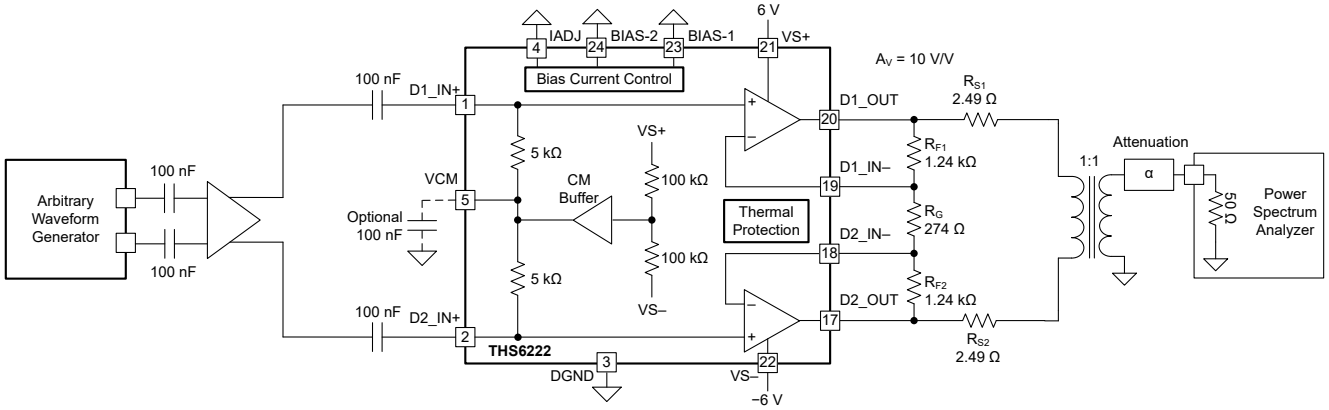


Figure 7-2. Measurement Test Circuit for Out-of-Band Suppression

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7.2.1.3 Application Curve

Figure 7-3 shows the out-of-band suppression measurement results of the circuit. Out-of-band suppression is a good indicator of the linearity performance of the device. The results in Figure 7-3 show over 40 dB of out-of-band suppression, which is well beyond the 35 dB requirement and indicative of the excellent linearity performance of the THS6222.

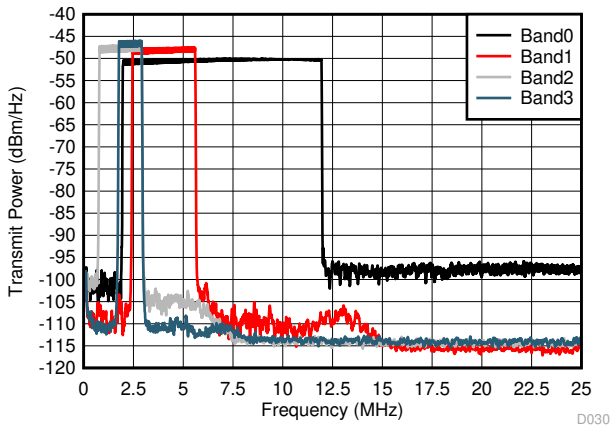


Figure 7-3. Out-of-Band Suppression

7.3 Best Design Practices

7.3.1 Do

- Include a thermal design at the beginning of the project.
- Use well-terminated transmission lines for all signals.
- Use solid metal layers for the power supplies.
- Keep signal lines as straight as possible.
- Keep the traces carrying differential signals of the same length.

7.3.2 Do Not

- Do not use a lower supply voltage than necessary.
- Do not use thin metal traces to supply power.
- Do not treat the D1 and D2 amplifiers as independent single-ended amplifiers.

7.4 Power Supply Recommendations

The THS6222 supports single-supply and split-supply power supplies, as well as balanced and unbalanced bipolar supplies. The device has a wide supply range of 8 V (–3 V to +5 V) to 32 V (±16 V). Choose power-supply voltages that allow for adequate swing on both the inputs and outputs of the amplifier to prevent affecting device performance. Operating from a single supply can have numerous advantages. With the negative supply at ground, the errors resulting from the –PSRR term can be minimized. The DGND pin provides the ground reference for the bias control pins. For applications that use split bipolar supplies, care must be taken to design within the DGND voltage specifications and must be within $V_{S–}$ to (V_{S+} – 5 V); the DGND pin must be a minimum bias of 5 V. Thus, the minimum positive supply that can be used in split-supply applications is V_{S+} = 5 V. The negative supply, $V_{S–}$, can then be set to a voltage anywhere in between –3 V and –27 V, as per the *Recommended Operating Conditions* specifications.

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7.5 Layout

7.5.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6222 requires careful attention to board layout parasitic and external component types. The THS6222RHFEVM can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Parasitic capacitance, particularly on the output and inverting input pins, can cause instability; on the noninverting input, this capacitance can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all ground and power planes around these pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. Minimize the distance (less than 0.25 in, or 6.35 mm) from the power-supply pins to high-frequency 0.1 µF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequencies, must also be used on the main supply pins. These capacitors can be placed somewhat farther from the device and can be shared among several devices in the same area of the PCB.
3. Careful selection and placement of external components preserves the high-frequency performance of the THS6222. Resistors must be of a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition, axially-leaded resistors can also provide good high-frequency performance.

   Again, keep leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Where double-side component mounting is required, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value, as described in *Section 7.2.1*. Increasing the value reduces the bandwidth, whereas decreasing the value leads to a more peaked frequency response. The 1.24 kΩ feedback resistor used in *Section 5.8* is a good starting point for a gain of 10 V/V design.
4. Connections to other wideband devices on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50-mils to 100-mils, 0.050-in to 0.100-in, or 1.27-mm to 2.54-mm) must be used, preferably with ground and power planes opened up around them.
5. Socketing a high-speed part such as the THS6222 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, and can make achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the THS6222 directly onto the board.
6. Use the $V_{S–}$ plane to conduct the heat out of the package. The package attaches the die directly to an exposed thermal pad on the bottom, and must be soldered to the board. This pad must be connected electrically to the same voltage plane as the most negative supply voltage ($V_{S–}$) applied to the THS6222. Place as many vias as possible on the thermal pad connection and connect the vias to a heat spreading plane that is at the same potential as $V_{S–}$ on the bottom side of the PCB.

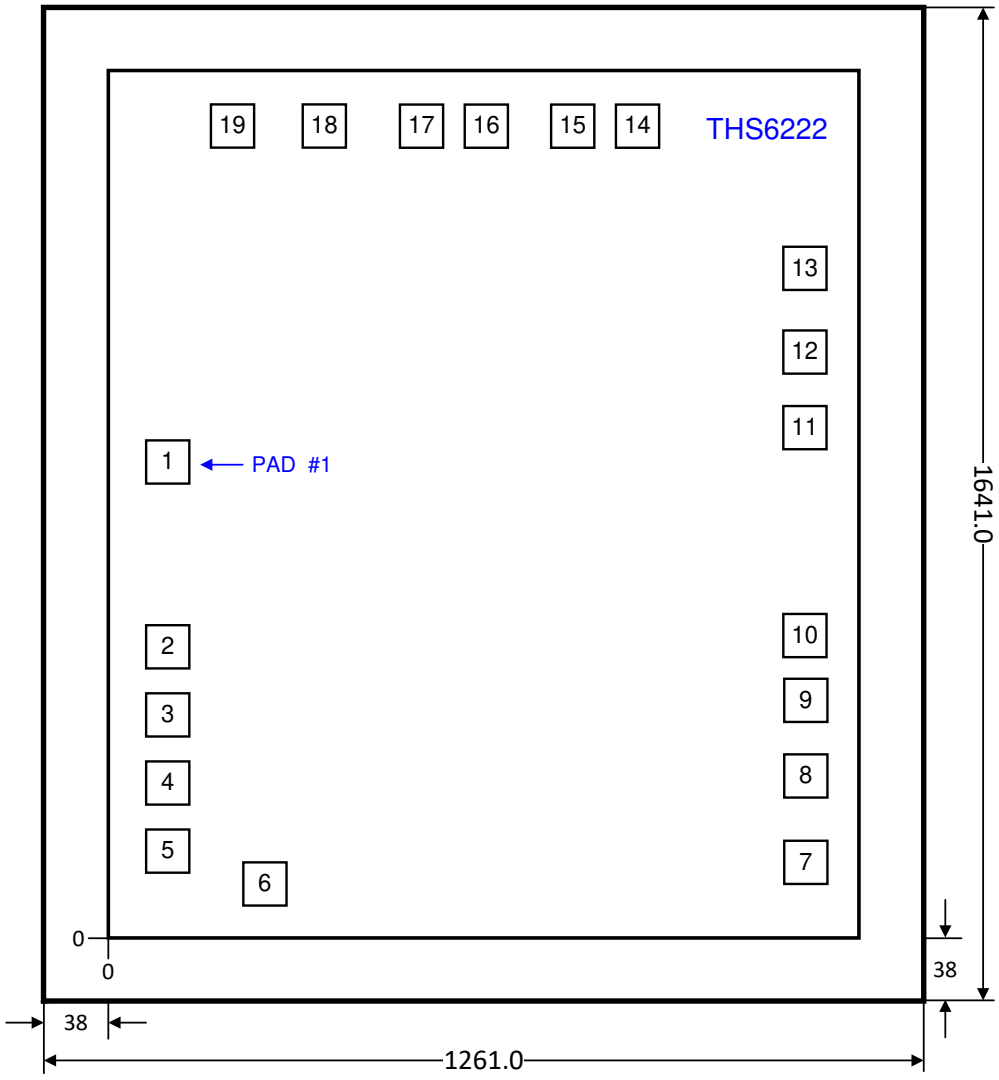
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7.5.1.1 Wafer and Die Information

Table 7-2 lists wafer and bond pad information for the YS package.

Table 7-2. Wafer and Bond Pad Information

WAFER BACKSIDE FINISH	WAFER THICKNESS	BACKSIDE POTENTIAL	BOND PAD METALLIZATION	BOND PAD DIMENSIONS (X × Y)
Silicon without backgrind	25 mils	Must be connected to the lowest voltage potential on the die (generally V_{S-})	Al	76.0 µm × 76.0 µm



All dimensions are in micrometers (µm).

Figure 7-4. Die Dimensions

Table 7-3 lists the bond pad locations for the YS package. All dimensions are in micrometers (µm).

Table 7-3. Bond Pad Locations

PAD NUMBER	PAD NAME	X MIN	Y MIN	X MAX	Y MAX	DESCRIPTION
1	D1_IN+	71.050	878.875	147.050	954.875	Amplifier D1 noninverting input
2	D2_IN+	71.050	525.125	147.050	601.125	Amplifier D2 noninverting input
3	DGND	71.050	384.025	147.050	460.025	Ground reference for bias control pins
4	IADJ	71.050	267.025	147.050	343.025	Bias current adjustment pin
5	VCM	71.050	150.025	147.050	226.025	Common-mode buffer output
6	VS–	209.175	85.925	285.175	161.925	Negative power-supply connection
7	VS+	1007.475	95.500	1083.475	171.500	Positive power-supply connection
8	D2_OUT	1007.475	222.500	1083.475	298.500	Amplifier D2 output (must be used for D2 output)
9	D2_OUT (OPT)	1007.475	369.900	1083.475	445.900	Optional amplifier D2 output (can be left unconnected or connected to pad 8)
10	D2_IN–	1007.475	487.375	1083.475	563.375	Amplifier D2 inverting input
11	D1_IN–	1007.450	919.375	1083.450	995.375	Amplifier D1 inverting input
12	D1_OUT (OPT)	1007.475	1034.100	1083.475	1110.100	Optional amplifier D1 output (pad can be left unconnected or connected to pad 13)
13	D1_OUT	1007.475	1181.500	1083.475	1257.500	Amplifier D1 output (must be used for D1 output)
14	VS+	851.675	1417.950	927.675	1493.950	Positive power-supply connection
15	VS+	718.900	1417.950	794.900	1493.950	Positive power-supply connection
16	VS–	557.375	1417.950	633.375	1493.950	Negative power-supply connection
17	VS–	424.600	1417.950	500.600	1493.950	Negative power-supply connection
18	BIAS-1	293.075	1417.750	369.075	1493.750	Bias mode parallel control, LSB
19	BIAS-2	159.250	1417.750	235.250	1493.750	Bias mode parallel control, MSB

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7.5.2 Layout Examples

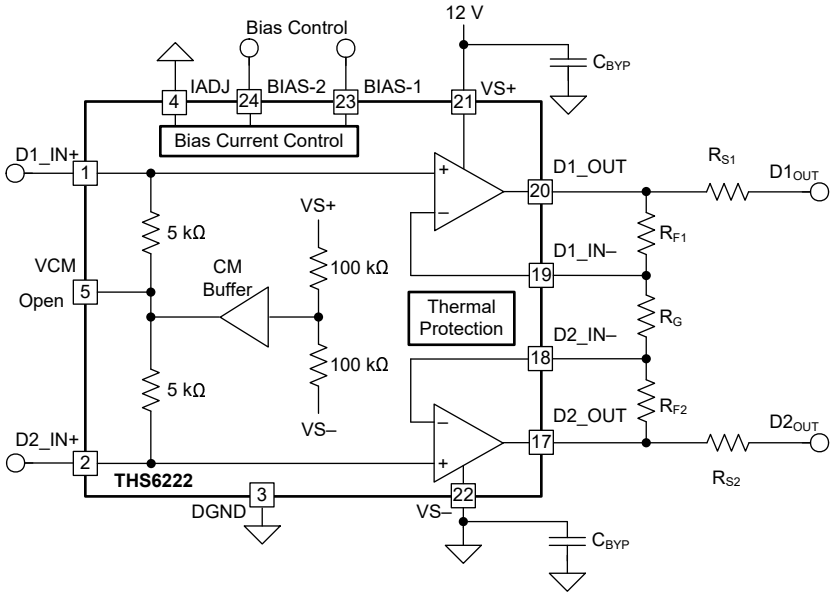


Figure 7-5. Representative Schematic for the Layout in Figure 7-6

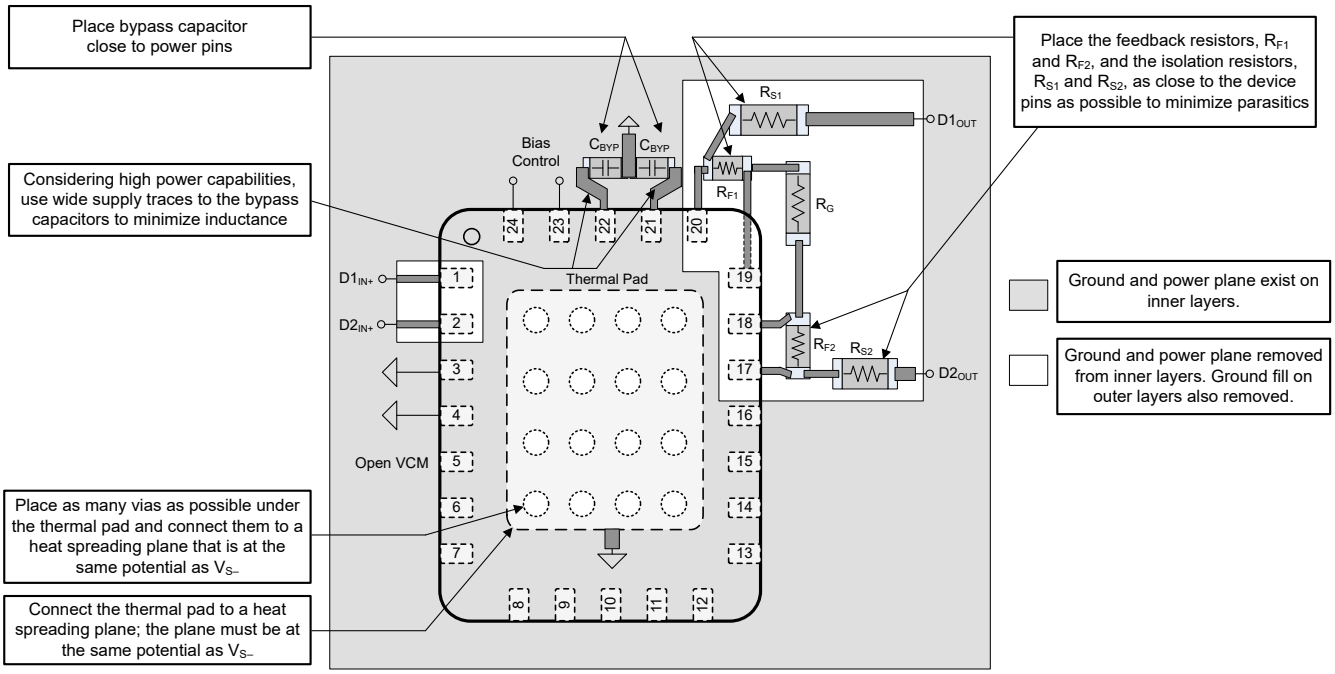


Figure 7-6. Layout Recommendations

8 Device and Documentation Support

8.1 Development Support

TI Precision Labs

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *THS6212 Differential Broadband PLC Line Driver Amplifier* data sheet
- Texas Instruments, *THS6214 Dual-Port, Differential, VDSL2 Line Driver Amplifiers* data sheet
- Texas Instruments, *Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *TI's IEC 61000-4-x Tests and Procedures* application report
- Texas Instruments, *THS6222 Evaluation Module* user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2024) to Revision F (December 2024)	Page
• Added language for PLC standards for SEO in *Applications*	1
• Added language for PLC standards for SEO in *Description*	1
• Updated front page image, *Functional Block Diagram*, and Figures 6-5, 6-7, 7-1, 7-2, and 7-5 to fix incorrect pin swap and labels	1

Changes from Revision D (April 2021) to Revision E (October 2024)	Page
• Updated last *Features* bullet to clarify compatibility with THS6212	1

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- Deleted maximum junction temperature continuous operation, long-term reliability from *Absolute Maximum Ratings* 5
- Updated drop-in replacement text in *Overview* section..... 19

Changes from Revision C (November 2020) to Revision D (April 2021) **Page**

- Updated the wrong pin diagram image that was tagged incorrectly during system migration.....3

Changes from Revision B (April 2020) to Revision C (November 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Added VQFN (16) package to the *Device Information* table..... 1
- Updated the RHF package in the *Pin Configuration and Functions* section.....3
- Added the RGT package in the *Pin Configuration and Functions* section.....3

Changes from Revision A (December 2019) to Revision B (April 2020) **Page**

- Added wafer sale package and BODY SIZE (NOM) to the *Device Information* table 1
- Added the YS die bondpad and functions..... 3
- Updated Table 1 BIAS-1 and BIAS-2 Logic Table..... 24
- Added Wafer and Die Information section..... 29

Changes from Revision * (August 2019) to Revision A (December 2019) **Page**

- Changed device status from advance information to production data 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS6222IRGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TH6222
THS6222IRGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TH6222
THS6222IRGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TH6222
THS6222IRHFR	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222IRHFR.B	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222IRHFT	Active	Production	VQFN (RHF) | 24	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222IRHFT.B	Active	Production	VQFN (RHF) | 24	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222YS	Active	Production	WAFERSALE (YS) | 0	1 | OTHER	-	Call TI	Call TI	-40 to 85	
THS6222YS.B	Active	Production	WAFERSALE (YS) | 0	1 | OTHER	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

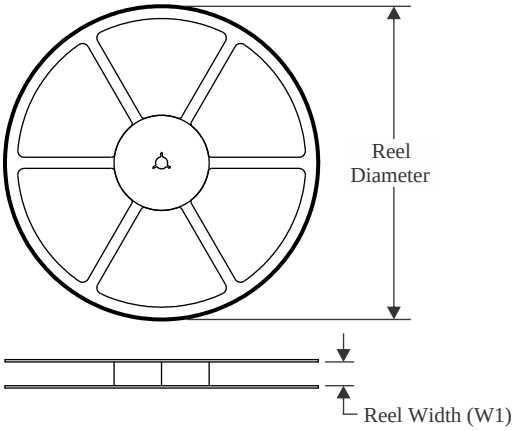
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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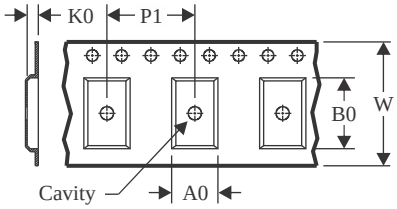
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

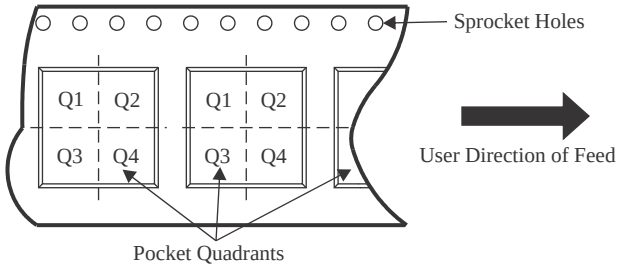


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

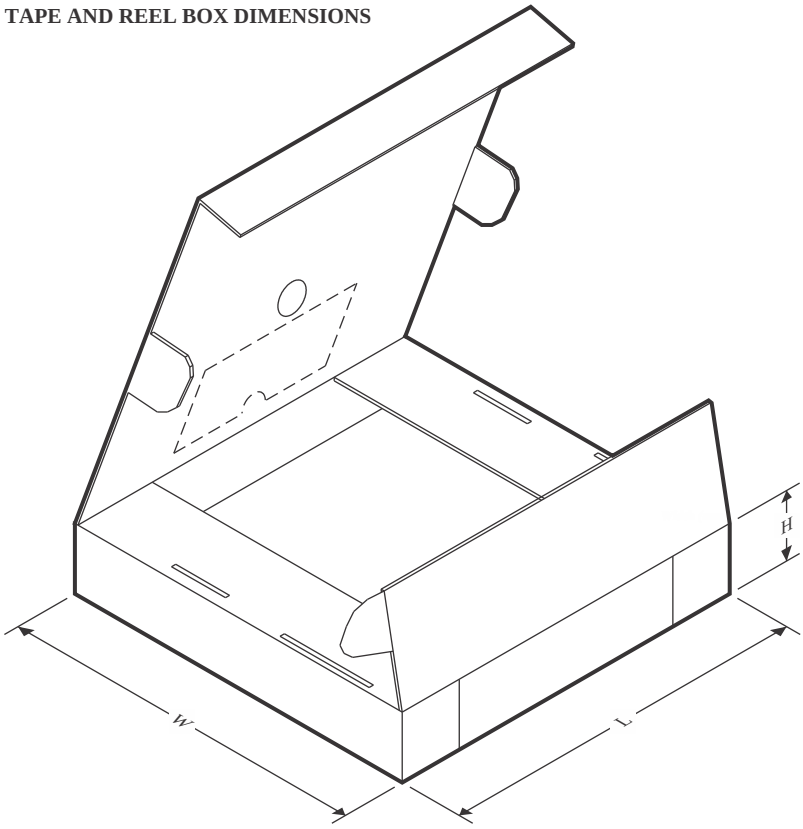
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6222IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS6222IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6222IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

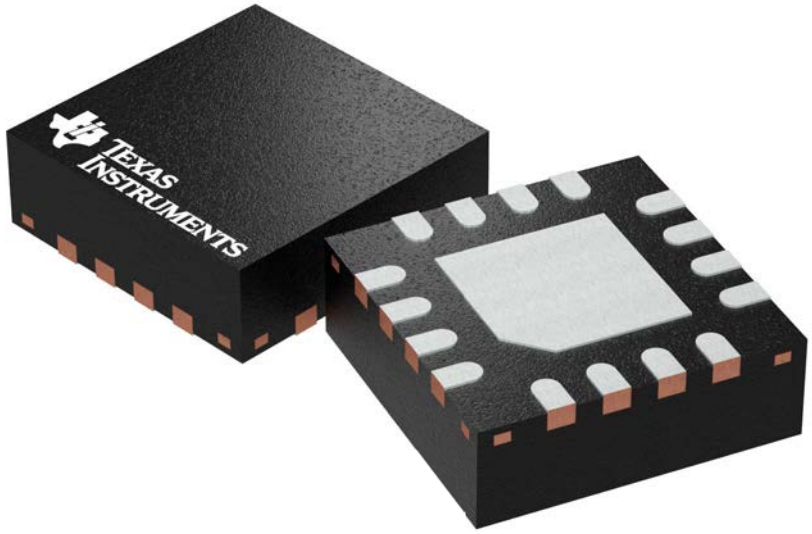


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6222IRGTR	VQFN	RGT	16	3000	360.0	360.0	36.0
THS6222IRHFR	VQFN	RHF	24	3000	356.0	356.0	36.0
THS6222IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



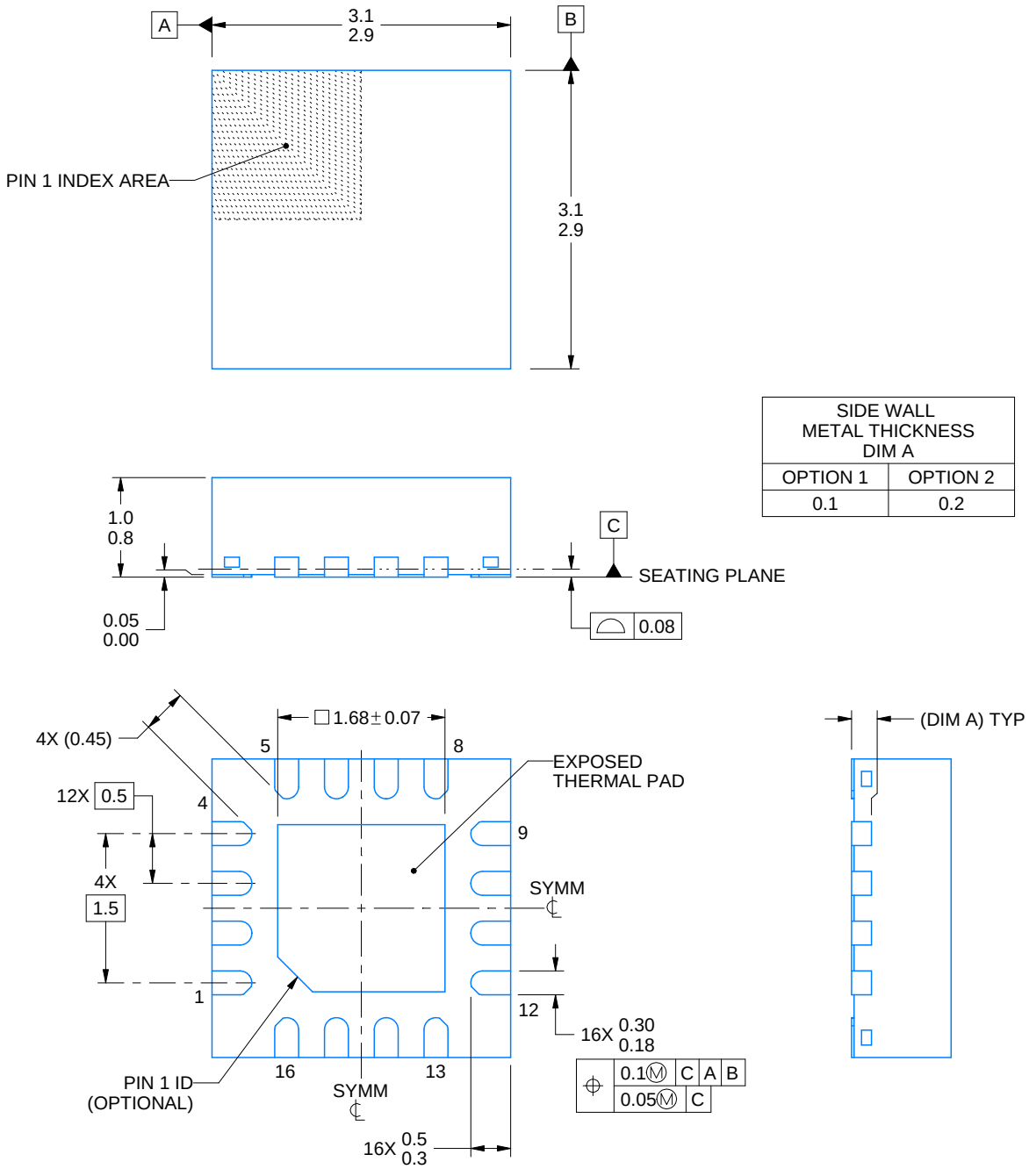
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

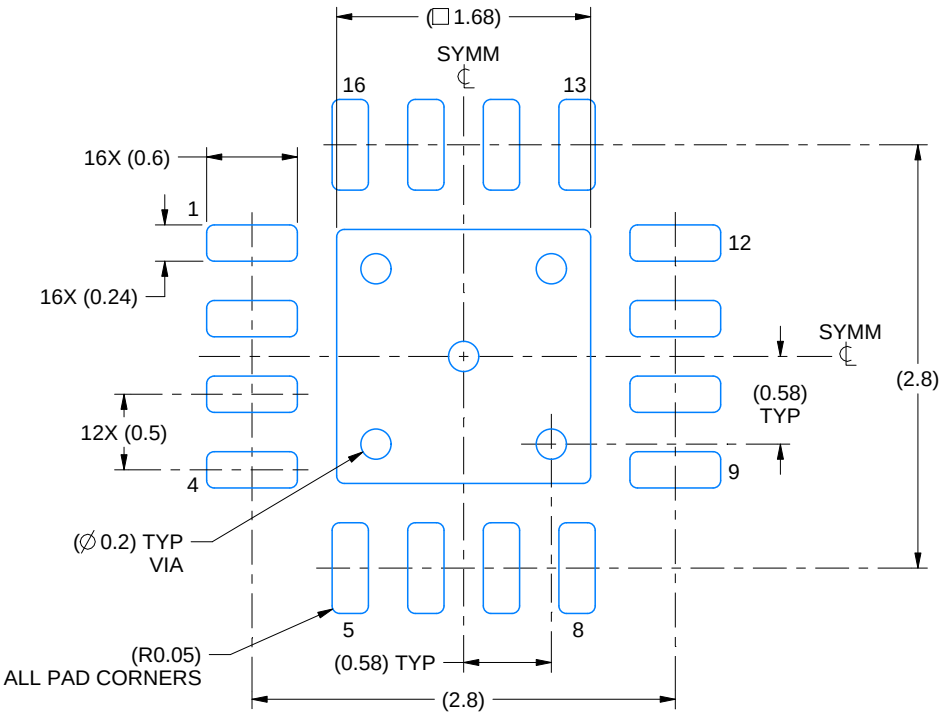
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

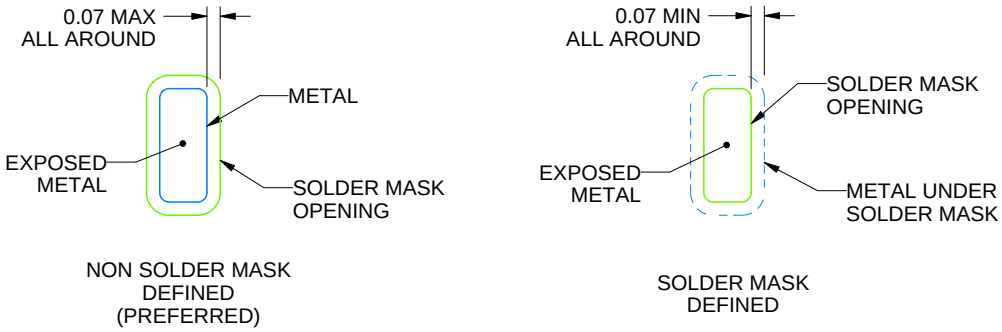


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

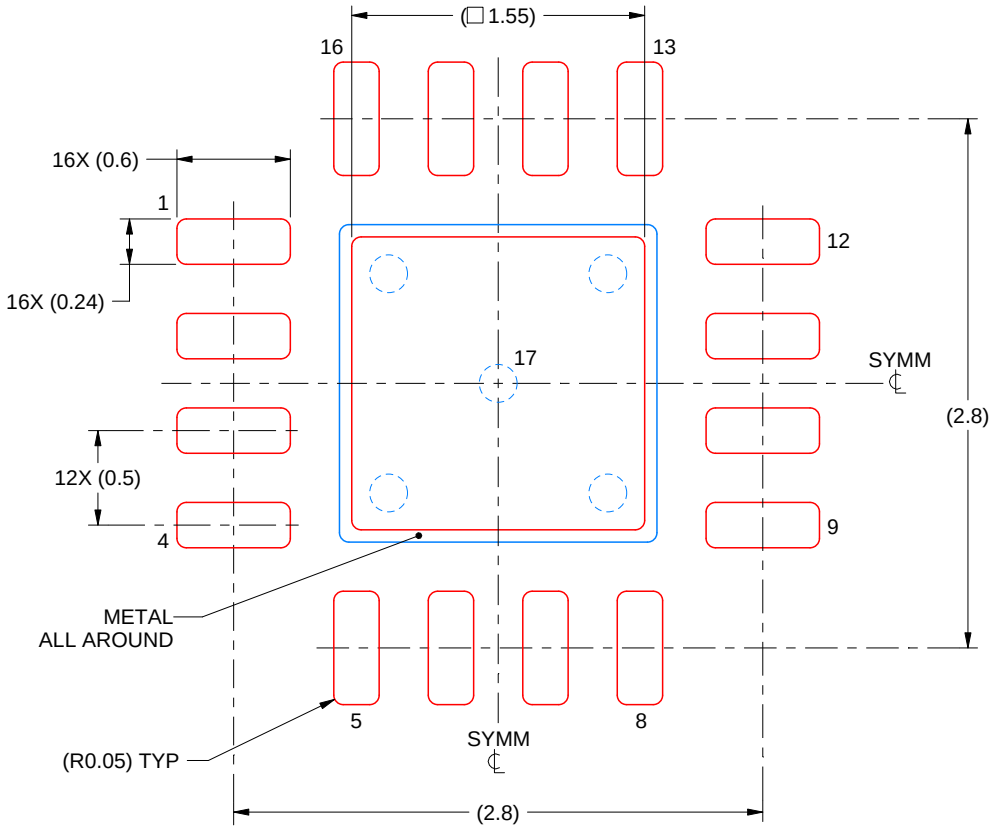


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

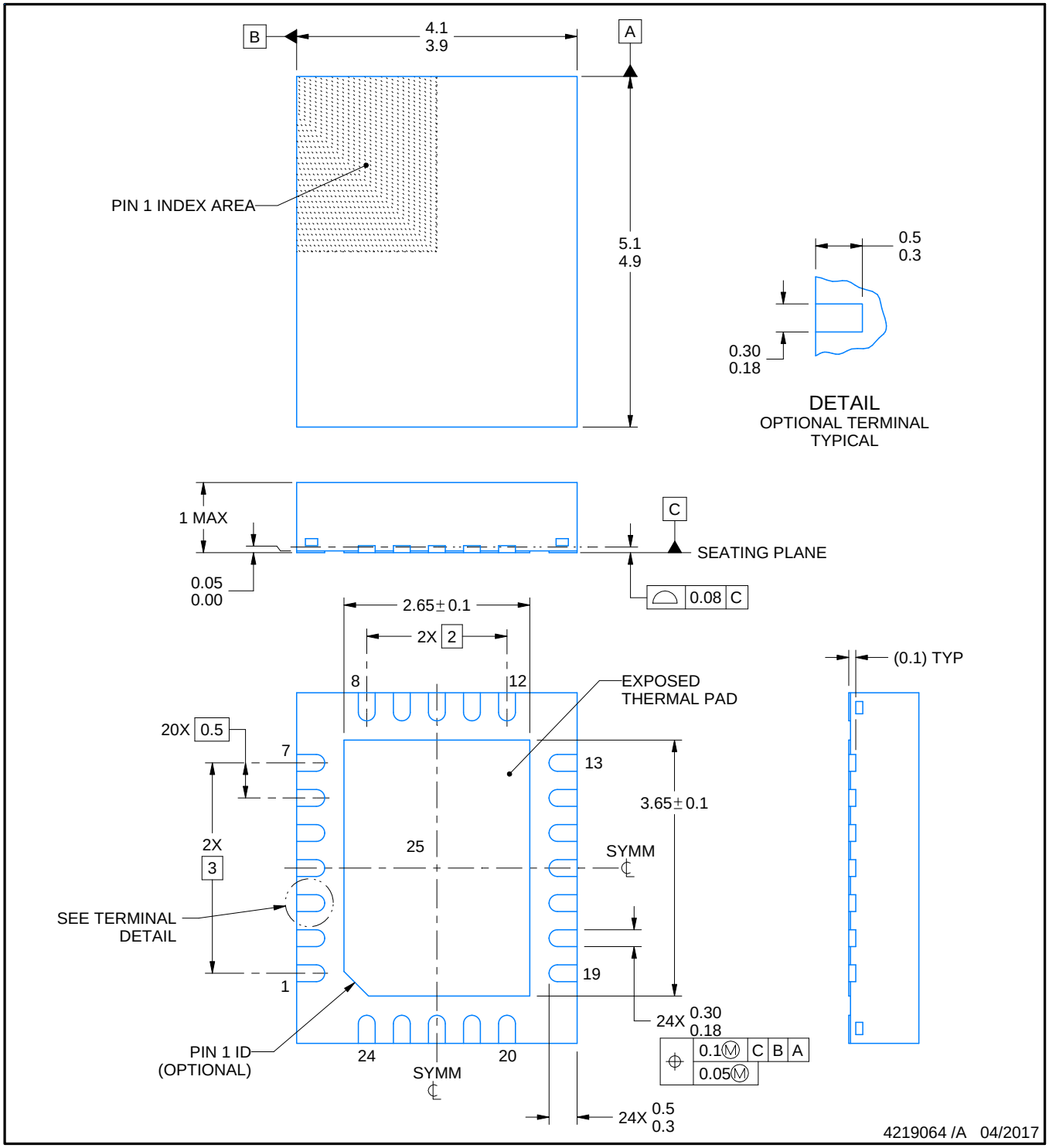
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

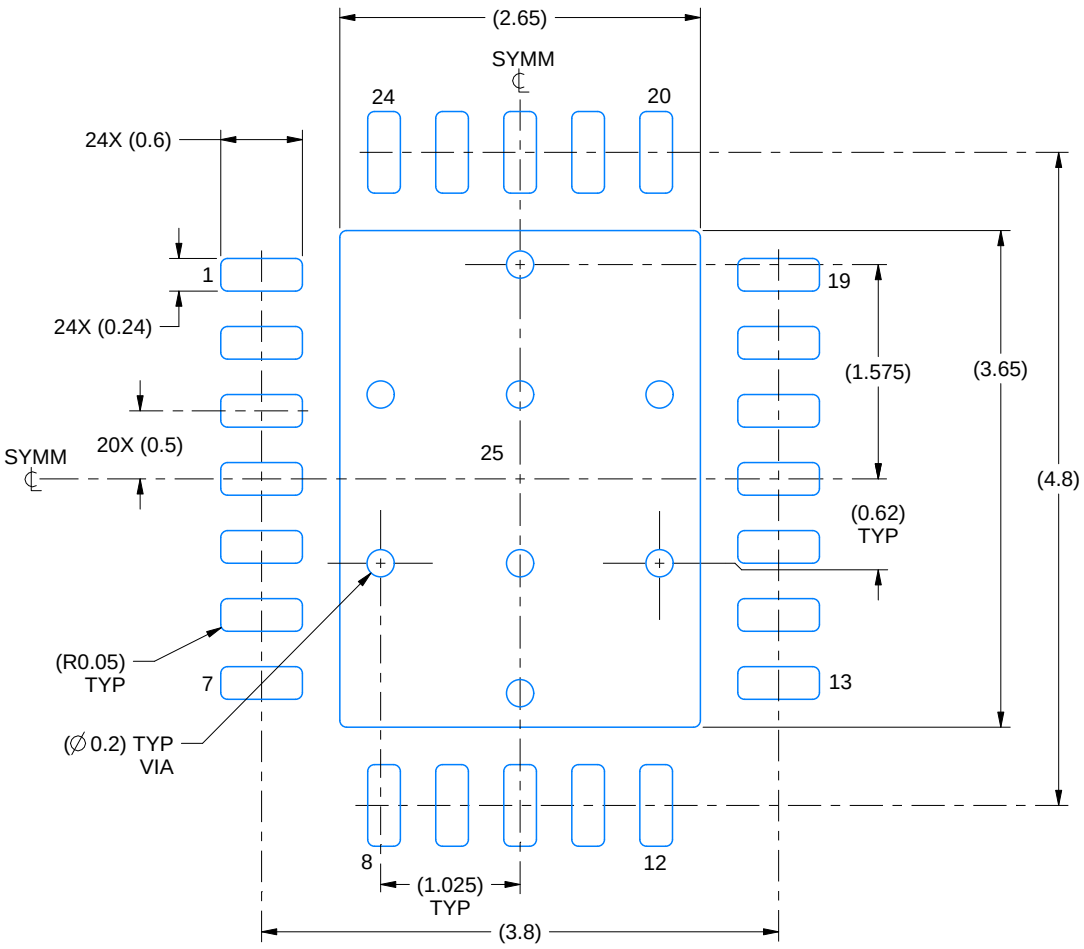
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

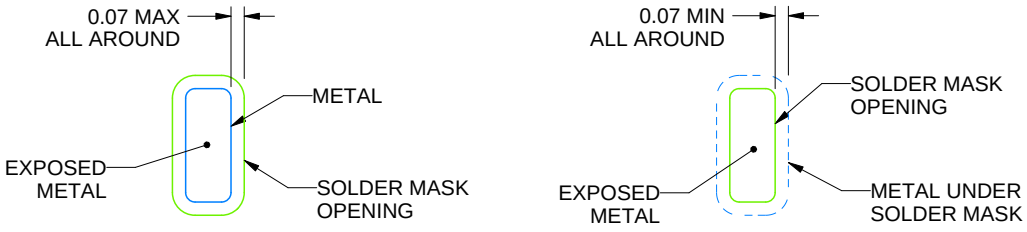
RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

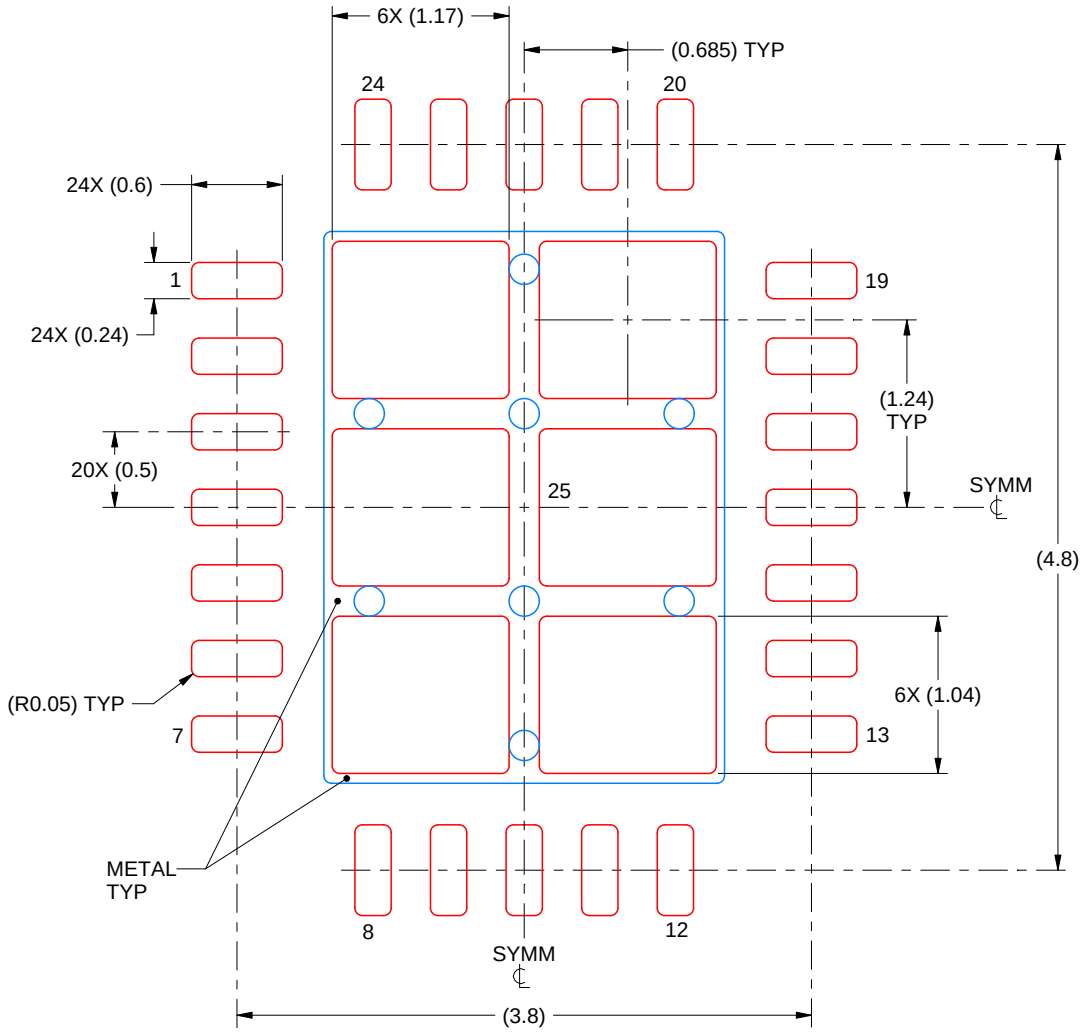


SOLDER MASK DETAILS

4219064 /A 04/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219064 /A 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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