THS3470 60V, 1A, 70MHz, 6500V/µs, High-Speed Power Amplifier

1 Features

- Bandwidth (V_S = ±20V, R_{FB} = 1.2kΩ):
  - Small-signal: 70MHz (V_O = $2V_{PP}$)
  - Large-signal: 45MHz (V_O = $20V_{PP}$)
  - Large-signal: 22MHz (V_S = ±30V, V_O = $50V_{PP}$, R_F = 2kΩ)
- Slew rate (20-80%):
  - 3000V/µs (R_F = 1.2kΩ, C_L = 300pF)
  - 2000V/µs (R_F = 2kΩ, C_L = 1nF)
  - 6500V/µs (Peak, R_F = 1.2kΩ, R_L = 100Ω)
- Output current:
  - Linear output current: ±1.35A
  - Peak output current: 2A
  - 250mV V_{OUT} swing in linear range (I_{OUT} = ±1A, V_O = ±25V, V_S = ±30V)
- Diagnostic features:
  - Programmable current limit (200mA to 1.5A, separate source and sink)
  - Die temperature and current output monitoring
  - Diagnostic flags (temperature, current source, current sink)

2 Applications

- Pattern generators for LCD/OLED testers
- CCD panel drivers
- Power SMUs
- High capacitive-load piezo element driver
- Power FET drivers
- Semiconductor test
- Line Drivers
- Arbitrary waveform generators

3 Description

The THS3470 is a high-speed current-feedback amplifier (CFA) with a high linear-output current drive (1.35A), high slew rate (6500V/µs peak), and wide supply range (60V). The device is stable over a wide range of capacitive loads and supports up to 2A of peak output current that these applications require. The THS3470 has a bandwidth of 70MHz with low-noise and distortion providing great large-signal performance for heavy resistive loads as well.

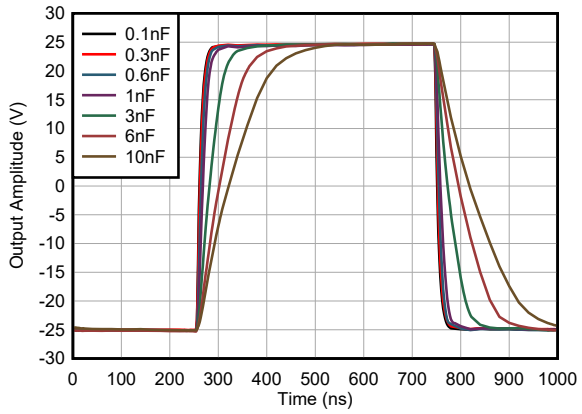
In addition to high speed and power performance, the THS3470 features a number of useful features such as temperature monitoring, output current monitoring, output current limiting, and output current protection. The output current features of the device can be manually enabled or driven by various flag outputs from the device providing even greater modularity in the use case of the device.

The THS3470 is available in a VQFN-42 (REB) package, providing small-size with an exposed top-side thermal pad for direct heat transfer to a heat sink. The THS3470 is characterized for operation over the wide temperature range of –40°C to +125°C.

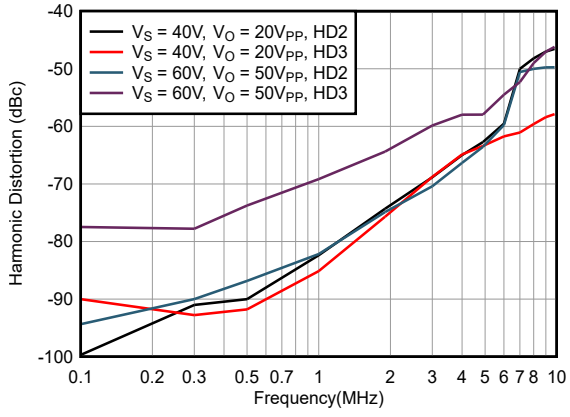
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
THS3470	REB (VQFN, 42)	7mm × 7mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



THS3470 Driving Capacitive Load



Harmonic Distortion vs Frequency (R_{LOAD} = 100Ω)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....5
5.1 Absolute Maximum Ratings....5
5.2 ESD Ratings....5
5.3 Recommended Operating Conditions....5
5.4 Thermal Information....5
5.5 Electrical Characteristics $\pm V_S$ = ±30V....7
5.6 Electrical Characteristics $\pm V_S$ = ±20V....10
5.7 Typical Characteristics....12
6 Detailed Description....20
6.1 Overview....20
6.2 Functional Block Diagram....20
6.3 Feature Description....21
6.4 Device Functional Modes....29
7 Application and Implementation....33
7.1 Application Information....33
7.2 Typical Application....33
7.3 Short Circuit Protection....40
7.4 Power Supply Recommendations....42
7.5 Layout....42
8 Device and Documentation Support....49
8.1 Documentation Support....49
8.2 Receiving Notification of Documentation Updates....49
8.3 Support Resources....49
8.4 Trademarks....49
8.5 Electrostatic Discharge Caution....49
8.6 Glossary....49
9 Revision History....49
10 Mechanical, Packaging, and Orderable Information....49
10.1 TAPE AND REEL INFORMATION....50

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4 Pin Configuration and Functions

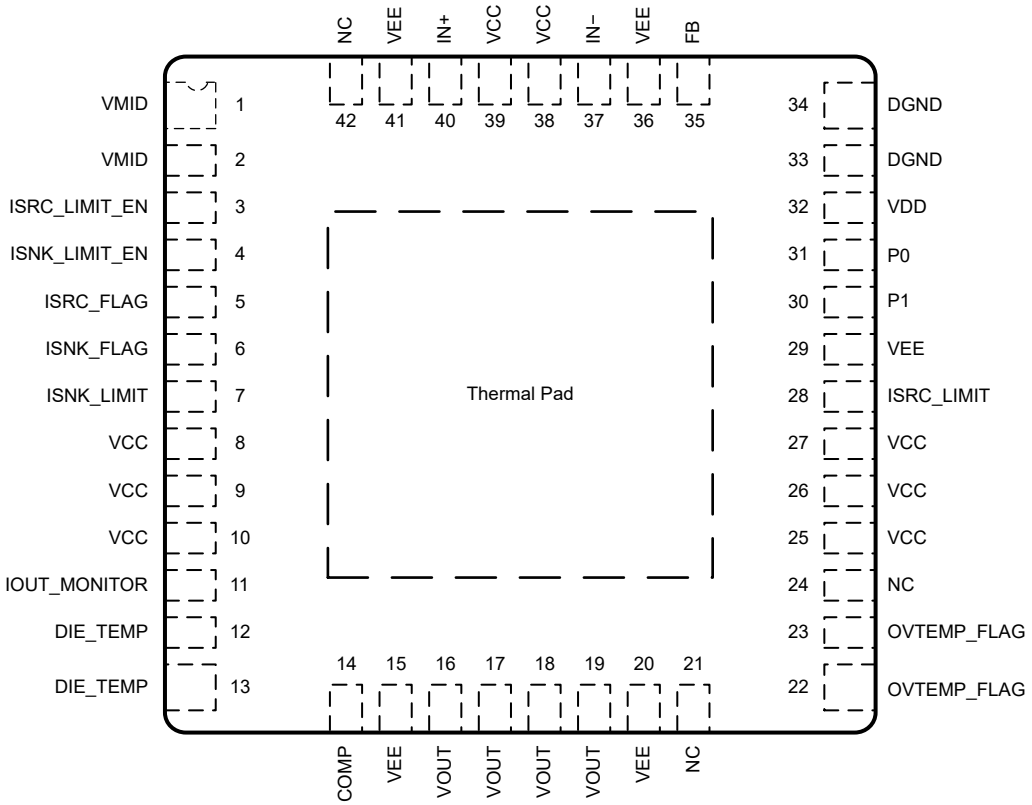


Figure 4-1. REB Package, 42-Pin VQFN (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COMP	14	Input	Internal compensation pin. Leave unconnected, with ground cutout, by default. See Section 6.3.7 for more details about pin operation.
DGND	33, 34	Input	Digital ground
DIE_TEMP	12, 13	Output	Die temperature output. The pin outputs 1.6V at 25°C by default. See Section 6.3.6 for more details about pin operation.
FB	35	Output	Input side feedback pin
IN−	37	Input	Inverting input
IN+	40	Input	Noninverting input
IOUT_MONITOR	11	Output	Output current monitor. Must be connected with 10kΩ pull-up and pull-down resistor by default. See Section 6.3.5 for more details about pin operation.
$\overline{\text{ISNK_FLAG}}$	6	Output	Output current sink flag. Internally pulled-up to VDD when device is under the set sink current limit by default. See Section 6.3.4 for more details about pin operation.
ISNK_LIMIT	7	Input	Output current sink limit. Connect pull-up resistor to VCC by default. See Section 6.3.1 for more details about pin operation.
$\overline{\text{ISNK_LIMIT_EN}}$	4	Input	Output current sink limit control. Internally pulled-up to VDD by default, resulting in no current limit while VOUT is sinking current. See Section 6.3.2 for more details about pin operation.
$\overline{\text{ISRC_FLAG}}$	5	Output	Output current source flag. Internally pulled-up to VDD when device is under the set source current limit by default. See Section 6.3.4 for more details about pin operation.
ISRC_LIMIT	28	Input	Output current source limit. Connect pull-down resistor to VEE by default. See Section 6.3.1 for more details about pin operation.

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{\text{ISRC_LIMIT_EN}}$	3	Input	Output current source limit control. Internally pulled-up to VDD by default, resulting in no current limit while VOUT is sourcing current. See Section 6.3.2 for more details about pin operation.
DNC	21, 24, 42	—	Leave unconnected. Pin disconnected internally.
$\overline{\text{OVTEMP_FLAG}}$	22, 23	Output	Over Temperature Flag. Default logic low when device junction temperature is <165°C. See Section 6.3.3 for more pin details.
P0	31	Input	Power-mode control, bit0. Internally pulled high to enable full bias mode. See Section 6.4.1 and Section 6.3.3 for more details about pin connections and performance.
P1	30	Input	Power-mode control, bit1. Internally pulled high to enable full bias mode. See Section 6.4.1 and Section 6.3.3 for more details about pin connections and performance.
VCC	8, 9, 10, 25, 26, 27, 38, 39	Input	Positive power supply. See Section 7.5.2 for bypass and layout suggestions.
VDD	32	Output	Internally generated 5.0V digital power supply, relative to DGND. See Section 7.5.2 for bypass and layout suggestions.
VEE	15, 20, 29, 36, 41	Input	Negative power supply. See Section 7.5.2 for bypass and layout suggestions.
VMID	1, 2	Output	Midsupply buffered output, $(V_{CC}+V_{EE})/2$. This pin must be buffered externally to use the VMID voltage as a power supply or voltage reference elsewhere in the design. See Section 7.5.2 for bypass and layout suggestions.
VOUT	16, 17, 18, 19	Output	Amplifier output
Thermal Pad		—	Thermal pad. Internally tied to VEE

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V_{CC}) – (V_{EE})$		64 (±32)	V
	Differential input voltage(2)		±0.7	V
	Common mode input voltage	$(V_{EE}) – 0.5$	$(V_{CC}) + 0.5$	V
I_{IN}	Continuous input current(2)		±10	mA
I_{OUT}	Continuous output current(3)		±500	mA
P_D	Power dissipation(4)	See *Thermal Information*		
T_A	Operating ambient temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Continuous input current limit for both the ESD diodes to supply pins and amplifier differential input clamp diode. The differential input clamp diode limits the voltage across the diode to 0.7 V with this continuous input current flowing through the diode.
(3) Long-term continuous current for electromigration limits.
(4) See Safe Operating Area for details about optimizing device performance during heavy power conditions.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Single supply voltage, $(V_{CC}) – (V_{EE})$	12		60	V
$±V_S$	Dual supply voltage, $(V_{S+} = V_{CC})$, $(V_{S-} = V_{EE})$	±6		±30	V
T_J	Junction temperature	–40	25	125(1)	°C

(1) Limited by $R_{\Theta JA}$ and maximum T_J for safe operation.

5.4 Thermal Information

THERMAL METRIC(1)		THS3470 REB (VQFN) 42 PINS	THS3470 REB (VQFN)(2) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.3	4.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.48	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.0	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.8	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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(2) THS3470EVM with 1m/s linear airflow velocity

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5.5 Electrical Characteristics $\pm V_S = \pm 30V$

at $T_A \cong 25°C$, $A_V = 10V/V$, $R_F = 2k\Omega$, and $R_S = 5\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth (–3dB)	$V_O = 2V_{PP}$	$R_L = 100\Omega$		30		MHz
			$R_S = 5\Omega$, $C_L = 1nF$		20		
LSBW	Large-signal bandwidth (–3dB)	$V_O = 50V_{PP}$, < 1dB peaking	$R_L = 100\Omega$		22		MHz
			$C_L = 1nF$ (2)		7		
SR	Slew rate (peak)	$V_O = 50V_{PP}$ step	$R_L = 100\Omega$		6500		V/µs
			$C_L = 1nF$		2600		
	Slew rate (20%–80%)	$V_O = 50V_{PP}$ step	$R_L = 100\Omega$		3500		
			$C_L = 1nF$		2000		
	Rise-and-fall time	$V_O = 50V$ step	$R_L = 100\Omega$		17		ns
			$C_L = 1nF$		22		
	Settling time	To 0.1%, $V_O = 50V$ step	$R_L = 100\Omega$		200		ns
			$C_L = 1nF$		375		
HD2	2nd-harmonic distortion	$V_O = 50V_{PP}$, $R_L = 100\Omega$	f = 10MHz		–47		dBc
			f = 1MHz		–80		
			f = 0.1MHz		–91		
		$V_O = 50V_{PP}$, $C_L = 1nF$	f = 1MHz		–80		
			f = 0.1MHz		–87		
HD3	3rd-harmonic distortion	$V_O = 50V_{PP}$, $R_L = 100\Omega$	f = 10MHz		–43		dBc
			f = 1MHz		–67		
			f = 0.1MHz		–75		
		$V_O = 50V_{PP}$, $C_L = 1nF$	f = 1MHz		–61		
			f = 0.1MHz		–71		
e_n	Voltage noise	f > 100kHz			1.3		nV/√Hz
i_{n+}	Noninverting input-referred current noise	f > 100kHz			31		pA/√Hz
$i_{n–}$	Inverting input-referred current noise	f > 100kHz			20		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	$V_O = \pm 10V$		4.5	5.5		MΩ
Z_{OL}	Open-loop transimpedance gain	$V_O = \pm 10V$, $R_L = 100\Omega$			4.1		MΩ
V_{OS}	Input offset voltage				±0.8	±3.5	mV
	Input offset voltage drift(1)	T_J = –40°C to +125°C			5		µV/°C
$I_{B–}$	Inverting input bias current				±3	±25	µA
	Inverting input bias current drift	T_J = –40°C to +125°C			100		nA/°C
I_{B+}	Noninverting input bias current				±1	±15	µA
	Noninverting input bias current drift	T_J = –40°C to +125°C			70		nA/°C
Z_{IN+}	Noninverting input impedance				900 || 1.5		kΩ || pF

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5.5 Electrical Characteristics $\pm V_S$ = ±30V (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, and R_S = 5Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Z_{IN-}	Inverting input impedance				17		Ω
	Input common-mode voltage			V_{EE} + 4		V_{CC} – 4	V
INPUT							
CMRR	Common-mode rejection ratio	f = dc, V_{ICM} = ±2V			67		dB
		f = dc, V_{ICM} = ±25V			72		
OUTPUT							
HR_{OUT}	Headroom to either supply	R_L = open			±4	±5	V
HR_{OUT}	Headroom to either supply	R_L = 100Ω			±4	±5	V
I_{OUTLIN}	Linear output current	R_L = 5Ω, V_O = ±10V, Z_{OL} > 200kΩ, source and sink		1	1.35		A
I_{OUT}	Maximum current output				1.5		A
Z_{OUT}	DC output impedance	Closed-loop			0.03		Ω
	Open-loop output resistance	Power down			11		kΩ
POWER SUPPLY							
I_Q	Quiescent current	Full bias, no load, ISNK/ISRC_LIMIT = open			31	32	mA
			T_J = –40°C to +125°C		31	33	
		Full bias, no load, ISNK/ISRC_LIMIT = 250mA			29	30	
			T_J = –40°C to +125°C		29	31	
		Full bias, no load, ISNK/ISRC LIMIT = 1A			33	34	
			T_J = –40°C to +125°C		33	34	
		Power down, no load, ISNK/ISRC_LIMIT = open			14	16	
			T_J = –40°C to +125°C		14	16	
PSRR	Power-supply rejection ratio	V_S = ±12V to ±30V		76	81		dB
DIE TEMP MONITORING							
	$\overline{\text{OVTEMP_FLAG}}$ status flag low				165		°C
	$\overline{\text{OVTEMP_FLAG}}$ status flag high				140		°C
T_{J_SENSE}	Die temperature output voltage	T_J = 25°C			1.55		V
	T_{J_SENSE} temperature coefficient	T_J = –40°C to +125°C			4.8		mV/°C
	T_{J_SENSE} output impedance				50		kΩ
OUTPUT CURRENT MONITORING							
	IOUT_MONITOR response time	Referenced to midsupply, 10kΩ Pull-up (VCC) and 10kΩ Pull-down resistor (VEE)			20		µs
	IOUT_MONITOR voltage	Referenced to midsupply		V_{MID} - 2V		V_{MID} + 2V	V
	IOUT_MONITOR accuracy	I_{OUT} = ±200mA			15		%
		I_{OUT} = ±1A			30		
CURRENT LIMIT MANAGEMENT							
	Output current limit	Externally adjustable		200		1500	mA

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5.5 Electrical Characteristics $\pm V_S$ = ±30V (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, and R_S = 5Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Current limit response time				1		us
	Current limit accuracy	I_{LIMIT} = ±200mA			5	15	%
		I_{LIMIT} = ±1A			5	15	
DIGITAL INPUTS (P0, P1, $\overline{ISRC_LIM_EN}$, $\overline{ISNK_LIM_EN}$)							
	DGND voltage			V_{EE}		V_{CC} – 12	V
	Digital input pin voltage	With respect to DGND		0		5.0	V
	Digital input pin logic threshold	Logic high, with respect to DGND			1.3	1.5	V
		Logic low, with respect to DGND		0.5	1.1		
	Digital input pin bias current	V_{IN} = 0V, with respect to DGND	T_J = –40°C to +125°C	-30	-13	30	µA
		V_{IN} = 5V, with respect to DGND	T_J = –40°C to +125°C	-30	-5	30	
DIGITAL OUTPUTS ($\overline{ISRC_FLAG}$, $\overline{ISNK_FLAG}$, $\overline{OVTEMP_FLAG}$)							
	Digital output pin voltage	With respect to DGND		0		5.0	V
	Digital output pin voltage high	With respect to DGND		4.9	4.99		V
	Digital output pin voltage low	With respect to DGND			0.01	0.1	V
	ISRC_FLAG response time				5		µs
	ISNK_FLAG response time				5		µs
	OVTEMP_FLAG response time				5		µs

(1) Current output based on electromigration limit, actual performance depends on system thermals.
(2) High capacitive load values, such as 1nF, limit the bandwidth as a result of large output current transients.

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5.6 Electrical Characteristics $\pm V_S = \pm 20V$

at $T_J \cong 25°C$, $A_V = –5V/V$, $R_F = 1.21k\Omega$, $R_S = 5\Omega$, and $C_L = 300pF$ connected to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth (–3dB)	$V_O = 2V_{PP}$			55		MHz
			$A_V = 2V/V$		70		
LSBW	Large-signal bandwidth (–3dB)	$V_O = 20V_{PP}$ (2)			45		MHz
SR	Slew rate (peak)	V_O = 30V step, A_V = 2V/V			3500		V/µs
	Slew rate (20%–80%)	V_O = 30V step, A_V = 2V/V			3000		
	Rise and fall time	V_O = 30V step, A_V = 2V/V			9		ns
	Settling time	To 0.1%, V_O = 10V step			150		ns
HD2	2nd-harmonic distortion	$V_O = 20V_{PP}$, $A_V = –10V/V$	f = 30MHz		–43		dBc
			f = 1MHz		–90		
			f = 0.1MHz		–105		
		$V_O = 20V_{PP}$, $A_V = –10V/V$, R_L = 25Ω	f = 30MHz		–46		
			f = 1MHz		–95		
			f = 0.1MHz		–91		
HD3	3rd-harmonic distortion	$V_O = 20V_{PP}$, $A_V = –10V/V$	f = 30MHz		–34		dBc
			f = 1MHz		–79		
			f = 0.1MHz		–86		
		$V_O = 20V_{PP}$, $A_V = –10V/V$, R_L = 25Ω	f = 30MHz		–33		
			f = 1MHz		–80		
			f = 0.1MHz		–86		
e_n	Voltage noise	f > 100kHz			1.3		nV/√Hz
i_{n+}	Noninverting input-referred current noise	f > 100kHz			31		pA/√Hz
$i_{n–}$	Inverting input-referred current noise	f > 100kHz			20		pA/√Hz
V_{OS}	Input offset voltage				±0.8	±3.5	mV
	Input offset voltage drift(1)	T_J = –40°C to +125°C			5		µV/°C
DC PERFORMANCE							
$I_{B–}$	Inverting input bias current				±3	±25	µA
	Inverting input bias current drift	T_J = –40°C to +125°C			100		nA/°C
I_{B+}	Noninverting input bias current				±1	±15	µA
	Noninverting input bias current drift	T_J = –40°C to +125°C			70		nA/°C
Z_{OL}	Open-loop transimpedance gain	V_O = ±10V			5.5		MΩ

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5.6 Electrical Characteristics $\pm V_S$ = ±20V (continued)

at T_J ≅ 25°C, A_V = –5V/V, R_F = 1.21kΩ, R_S = 5Ω, and C_L = 300pF connected to midsupply (unless otherwise noted)

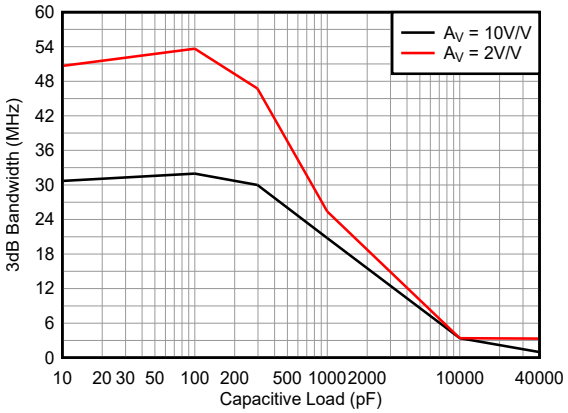
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Z_{IN+}	Noninverting input impedance				180 || 5		kΩ || pF
$Z_{IN–}$	Inverting input impedance				17		Ω
	Input common-mode voltage			V_{EE} + 4		V_{CC} – 4	V
CMRR	Common-mode rejection ratio	f = dc, VICM = ±2V			67		dB
		f = dc, VICM = ±18V			72		
OUTPUT							
HR_{OUT}	Headroom to either supply	R_L = open			±4	±5	V
		R_L = 100Ω			±4	±5	V
I_{OUTLIN}	Linear output current			1	1.2		A
I_{OUT}	Maximum current output				1.5		A
Z_{OUT}	DC output impedance	Closed-loop			0.03		Ω
POWER SUPPLY							
I_Q	Quiescent current	Full bias, no load, ISNK/ISRC_LIMIT = open			31	32	mA
			T_J = –40°C to +125°C		31	33	
		Full bias, no load, ISNK/ISRC_LIMIT = 200mA			29	30	
			T_J = –40°C to +125°C		29	31	
		Full bias, no load, ISNK/ISRC_LIMIT = 1.5A			33	34	
			T_J = –40°C to +125°C		33	34	
		Power down, no load, ISNK/ISRC_LIMIT = open			14	16	
			T_J = –40°C to +125°C		14	16	
OUTPUT CURRENT MONITORING							
	IOUT_MONITOR accuracy	I_{OUT} = ±200mA			5		%
		I_{OUT} = ±1A			15		
CURRENT LIMIT MANAGEMENT							
	Current limit accuracy	I_{LIMIT} = ±200mA			5		%
		I_{LIMIT} = ±1A			5		

(1) Current output based on electromigration limit, actual performance depends on system thermals.
(2) High capacitive load values, like 300pF, limit the bandwidth due to large output current transients.

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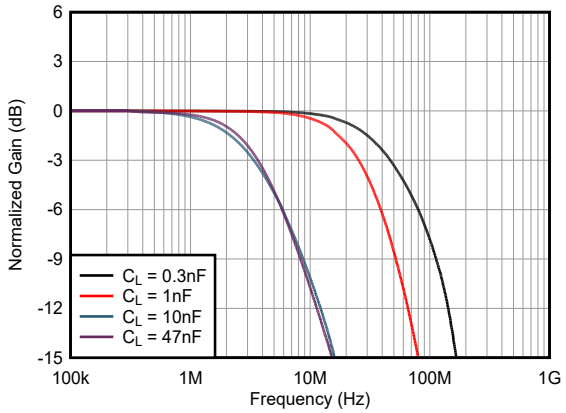
5.7 Typical Characteristics

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, R_S = 5Ω, and V_S = 60V (unless otherwise noted)



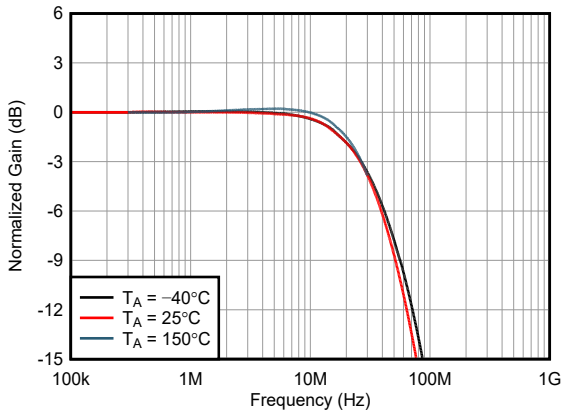
V_{OUT} = 2V_{PP}

Figure 5-1. Small Signal Bandwidth vs Capacitive Load



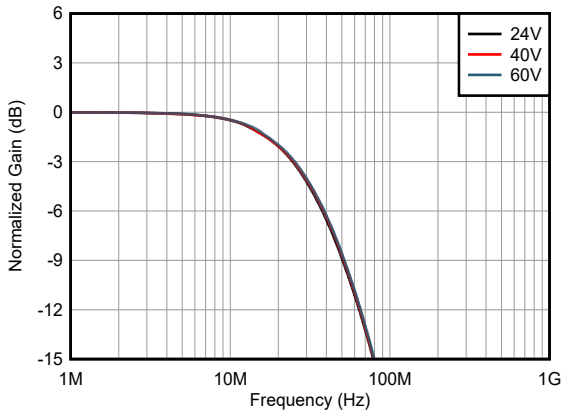
A_V = 2V/V, V_{OUT} = 2V_{PP}

Figure 5-2. Small Signal Bandwidth vs Capacitive Load



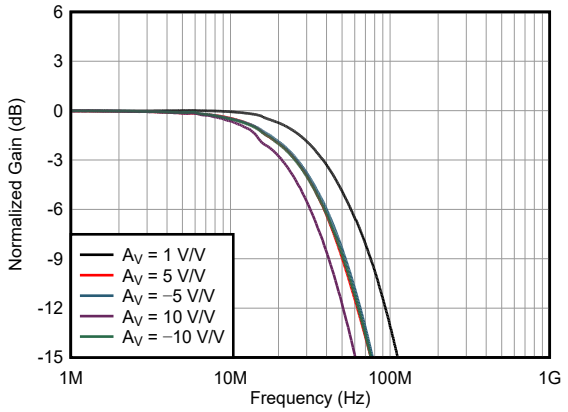
A_V = 2V/V, C_{LOAD} = 1nF, V_{OUT} = 2V_{PP}

Figure 5-3. Small Signal Bandwidth vs Temperature



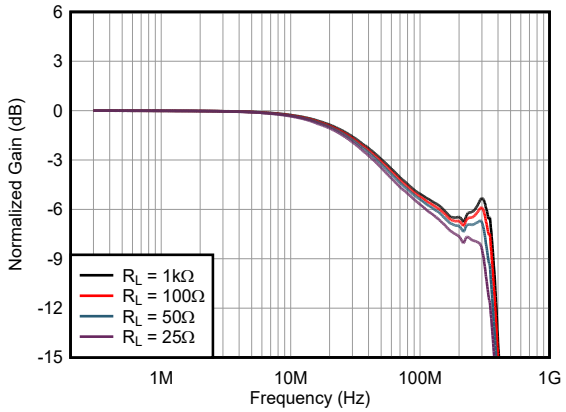
A_V = 2V/V, C_{LOAD} = 1nF, V_{OUT} = 2V_{PP}

Figure 5-4. Small Signal Bandwidth vs Supply Voltage



A_V = 2V/V, C_{LOAD} = 1nF, V_{OUT} = 2V_{PP}

Figure 5-5. Small Signal Bandwidth vs Gain



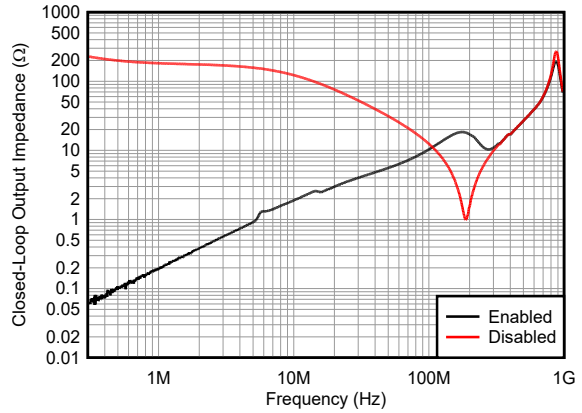
A_V = 2V/V, R_S = 0Ω, C_{LOAD} = Open, V_{OUT} = 2V_{PP}

Figure 5-6. Small Signal Bandwidth vs Resistive Load

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5.7 Typical Characteristics (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, R_S = 5Ω, and V_S = 60V (unless otherwise noted)



R_S = 0Ω, C_{LOAD} = Open

Figure 5-7. Closed Loop Output Impedance vs Frequency

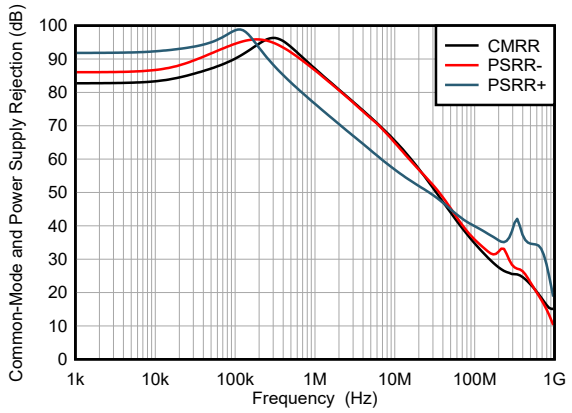
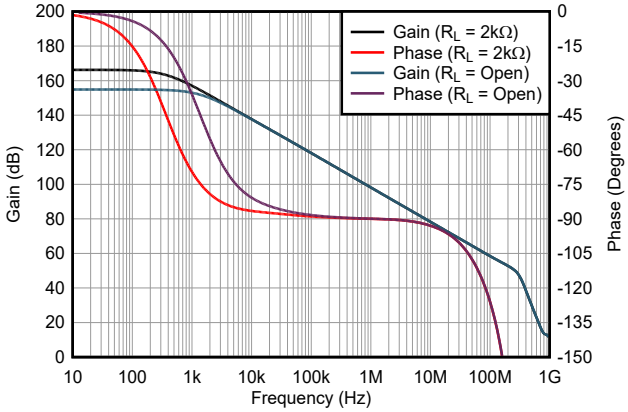
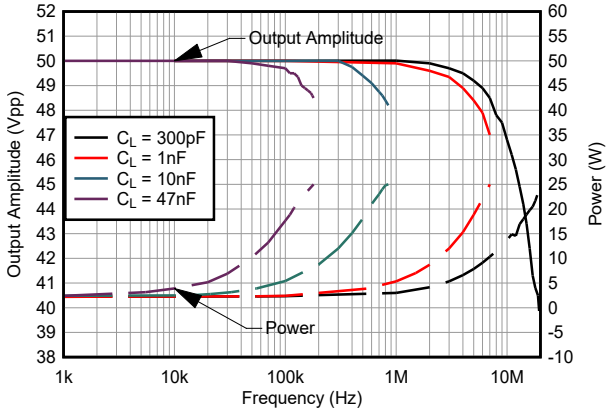


Figure 5-8. Common-Mode and Power Supply Rejection vs Frequency



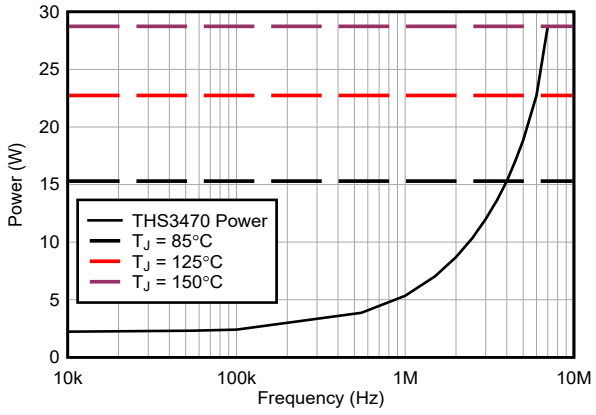
C_{LOAD} = Open

Figure 5-9. Open-Loop Transimpedance vs Frequency



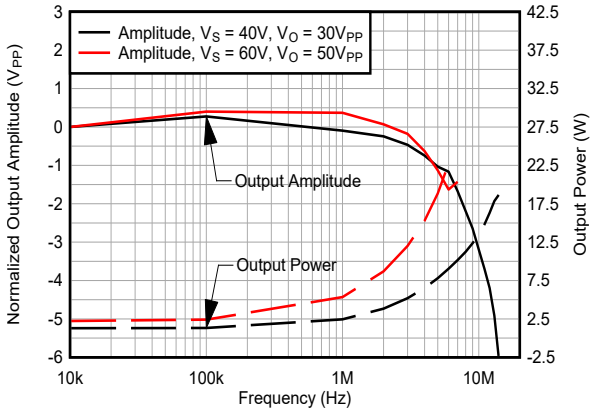
V_{OUT} = 50V_{PP}

Figure 5-10. Large Signal Bandwidth vs Capacitive Load



C_{LOAD} = 1nF, V_{OUT} = 50V_{PP}

Figure 5-11. Large Signal Power vs Frequency



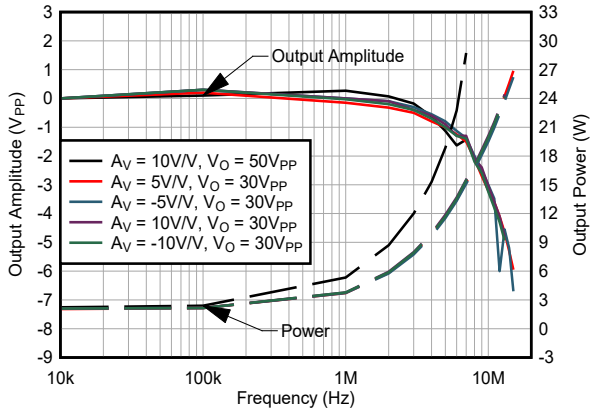
C_{LOAD} = 1nF

Figure 5-12. Large Signal Bandwidth vs Supply Voltage

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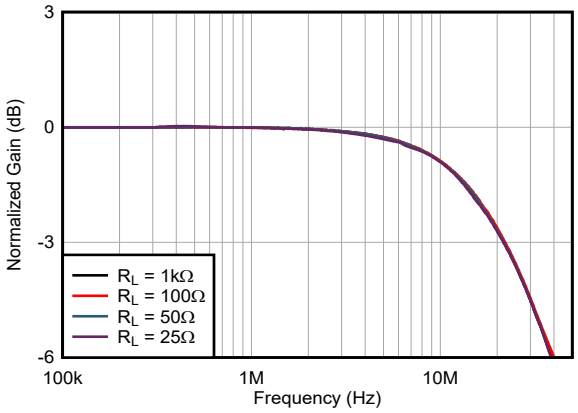
5.7 Typical Characteristics (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, R_S = 5Ω, and V_S = 60V (unless otherwise noted)



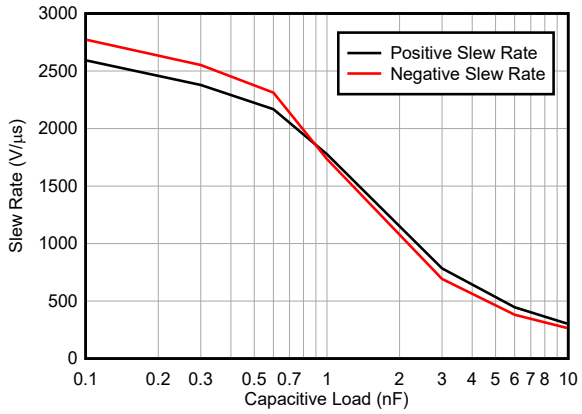
C_{LOAD} = 1nF

Figure 5-13. Large Signal Bandwidth vs Gain



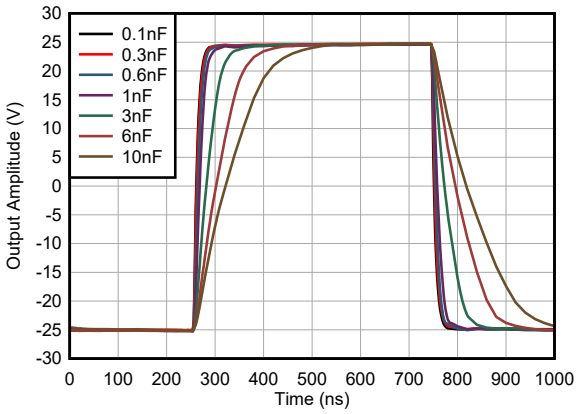
R_S = 0Ω, C_{LOAD} = Open, V_{OUT} = 50V_{PP}

Figure 5-14. Large Signal Bandwidth vs Resistive Load



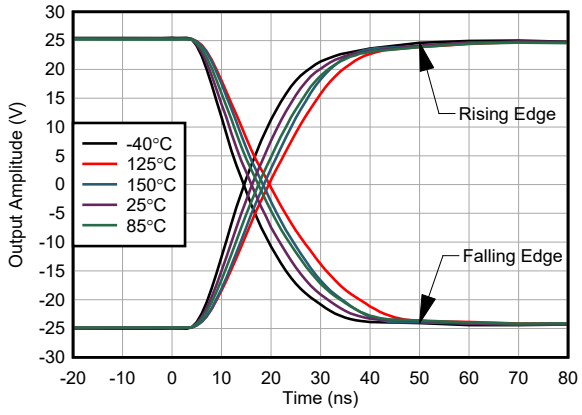
V_{OUT} = 50V_{PP}

Figure 5-15. Slew Rate vs Capacitive Load



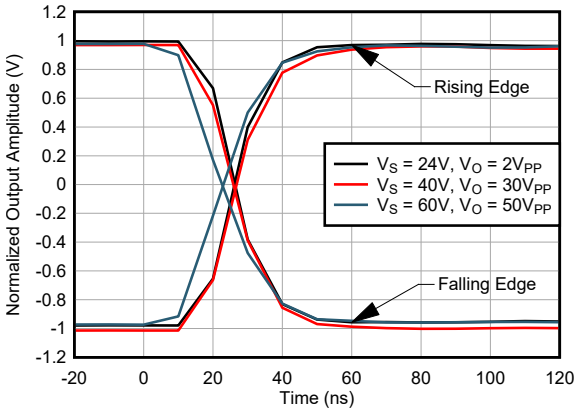
V_{OUT} = 50V_{PP}

Figure 5-16. Large-Signal Step Response vs Capacitive Load



C_{LOAD} = 1nF, V_{OUT} = 50V_{PP}

Figure 5-17. Large-Signal Step Response vs Temperature



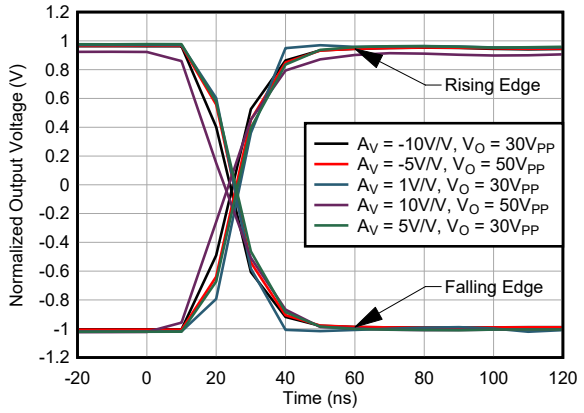
C_{LOAD} = 1nF

Figure 5-18. Large-Signal Step Response vs Supply Voltage

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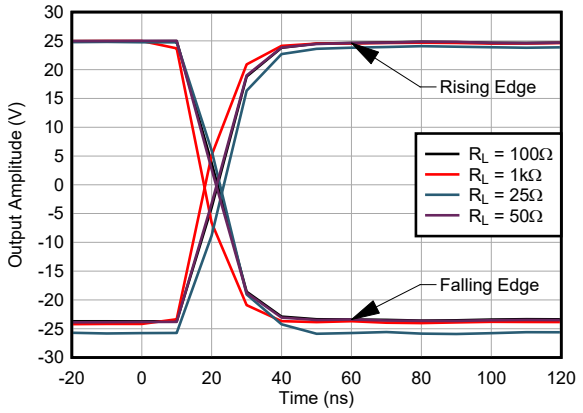
5.7 Typical Characteristics (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, R_S = 5Ω, and V_S = 60V (unless otherwise noted)



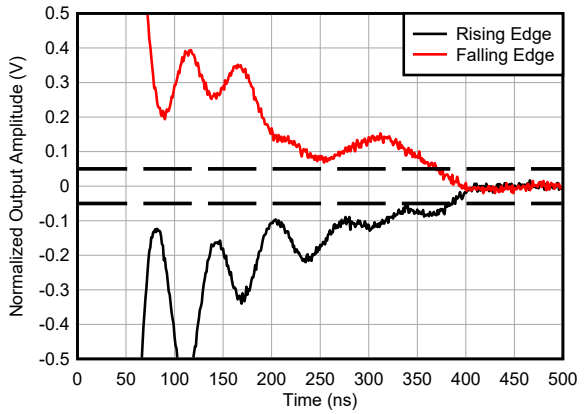
C_{LOAD} = 1nF

Figure 5-19. Large-Signal Step Response vs Gain



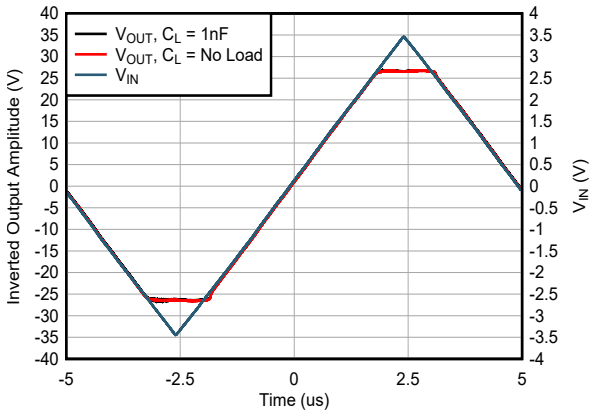
C_{LOAD} = Open, V_{OUT} = 50V_{PP}

Figure 5-20. Large-Signal Step Response vs Resistive Load



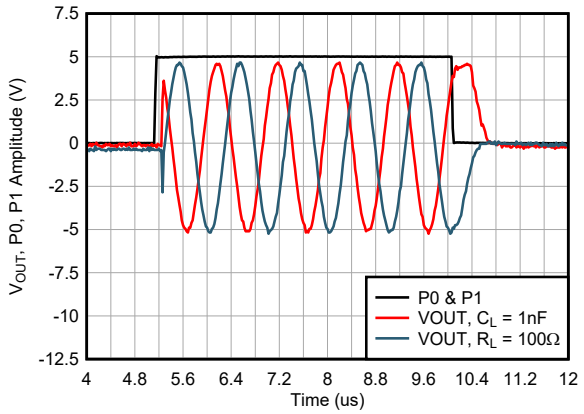
C_{LOAD} = 1nF, V_{OUT} = 50V_{PP}

Figure 5-21. Large-Signal Settling Time



A_V = −10V/V, V_{OUT} = 50V_{PP}

Figure 5-22. Overload Recovery Time



C_{LOAD} = 1nF, V_{OUT} = 50V_{PP} , f_{IN} = 100kHz

Figure 5-23. Output Enable/Disable Time

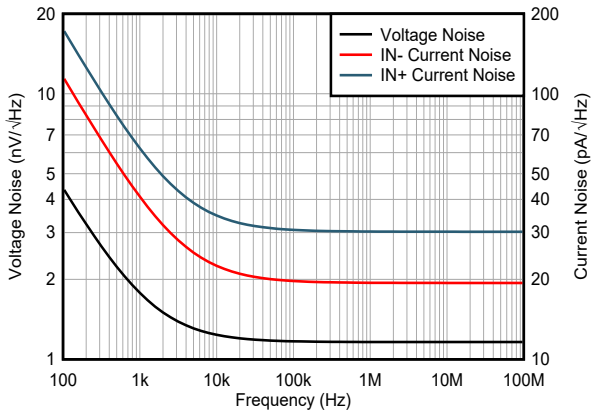
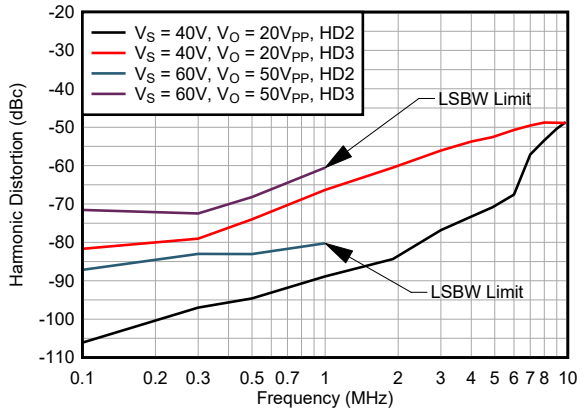


Figure 5-24. Voltage and Current Noise vs Frequency

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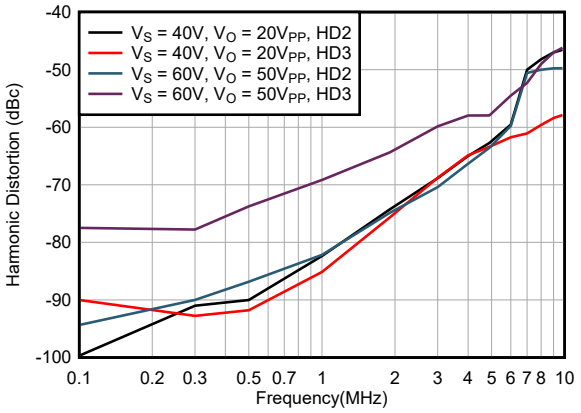
5.7 Typical Characteristics (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, R_S = 5Ω, and V_S = 60V (unless otherwise noted)



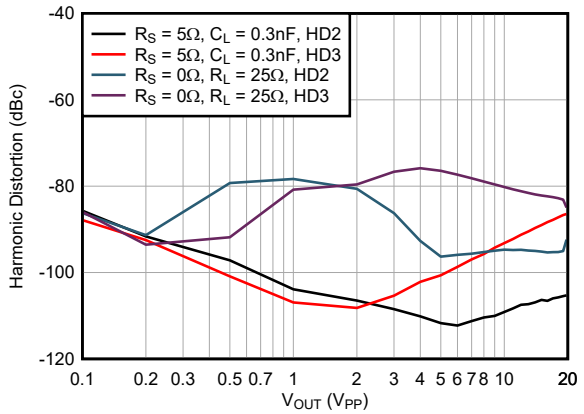
C_{LOAD} = 1nF

Figure 5-25. Harmonic Distortion vs Frequency



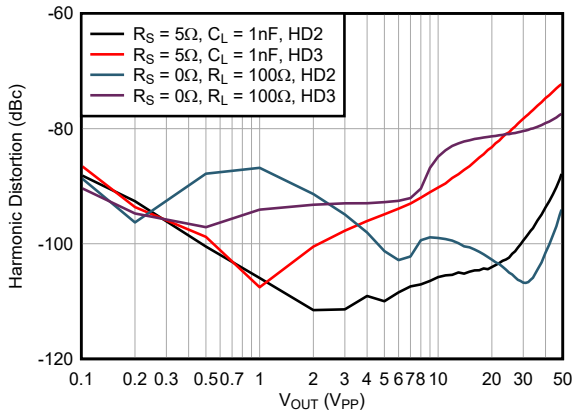
C_{LOAD} = Open, A_V = 10V/V, R_{LOAD} = 100Ω

Figure 5-26. Harmonic Distortion vs Frequency



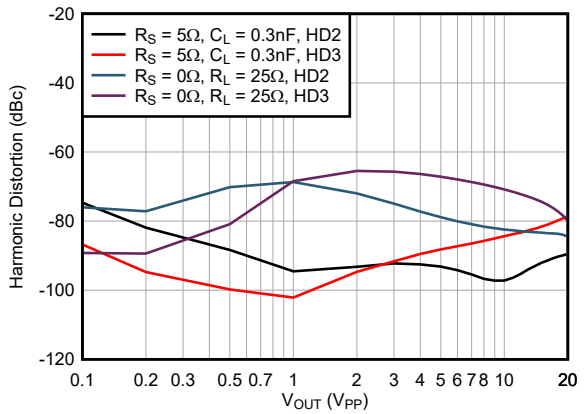
A_V = −10V/V, V_S = 40V, f_{in} = 100kHz

Figure 5-27. Harmonic Distortion vs Output Voltage



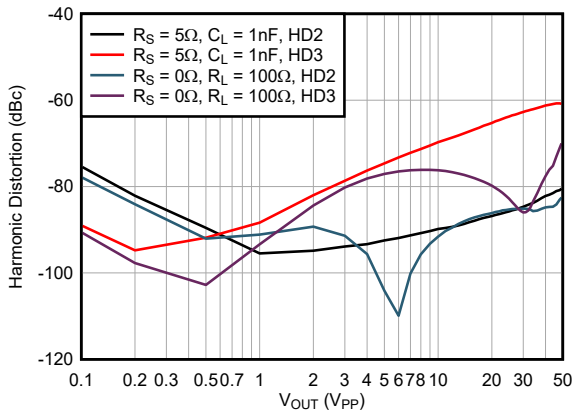
A_V = 10V/V, V_S = 60V, f_{in} = 100kHz

Figure 5-28. Harmonic Distortion vs Output Voltage



A_V = −10V/V, V_S = 40V, f_{in} = 1MHz

Figure 5-29. Harmonic Distortion vs Output Voltage



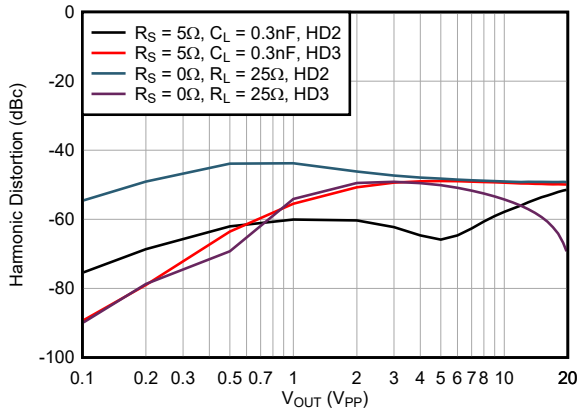
A_V = 10V/V, V_S = 60V, f_{in} = 1MHz

Figure 5-30. Harmonic Distortion vs Output Voltage

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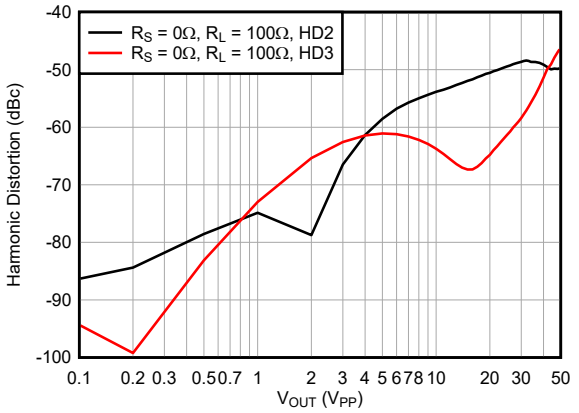
5.7 Typical Characteristics (continued)

at $T_A \cong 25°C$, $A_V = 10V/V$, $R_F = 2k\Omega$, $R_S = 5\Omega$, and $V_S = 60V$ (unless otherwise noted)



$A_V = -10V/V$, $V_S = 40V$, $f_{in} = 10MHz$

Figure 5-31. Harmonic Distortion vs Output Voltage



$A_V = 10V/V$, $V_S = 60V$, $f_{in} = 10MHz$

Figure 5-32. Harmonic Distortion vs Output Voltage

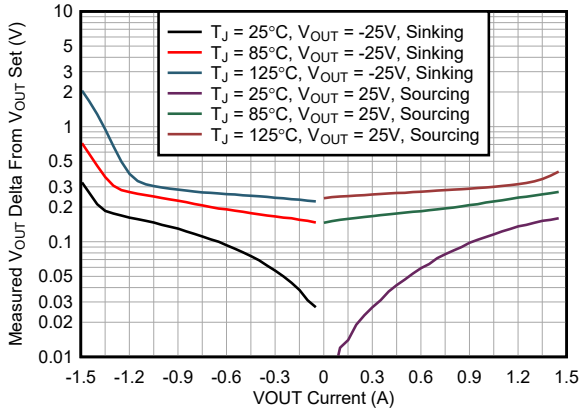
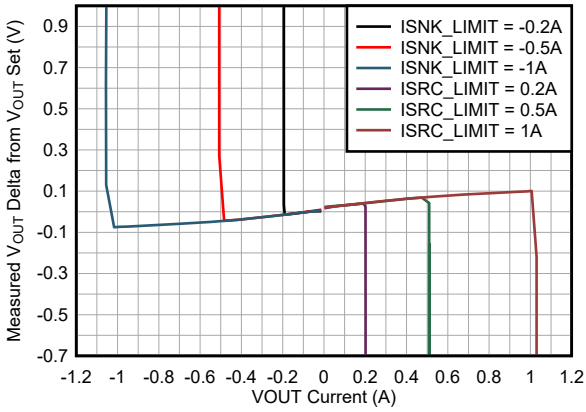


Figure 5-33. Output-Voltage Headroom vs Temperature



V_{OUT} = 25V (Source) and −25V (Sink)

Figure 5-34. Output Headroom vs Current Limit

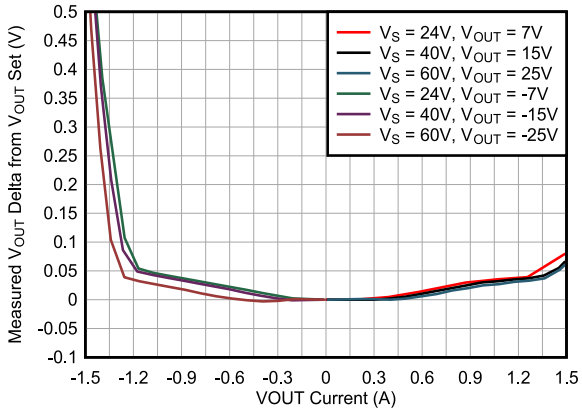
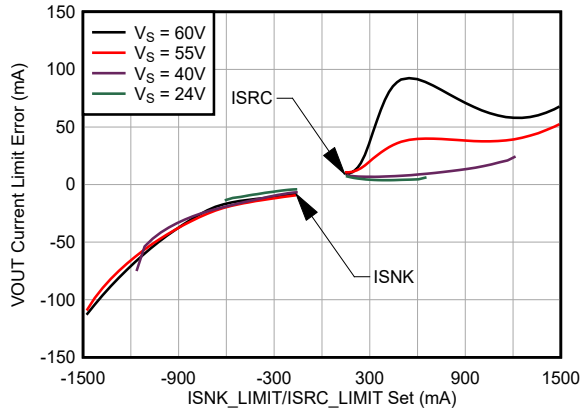


Figure 5-35. Output Headroom vs Supply Voltage



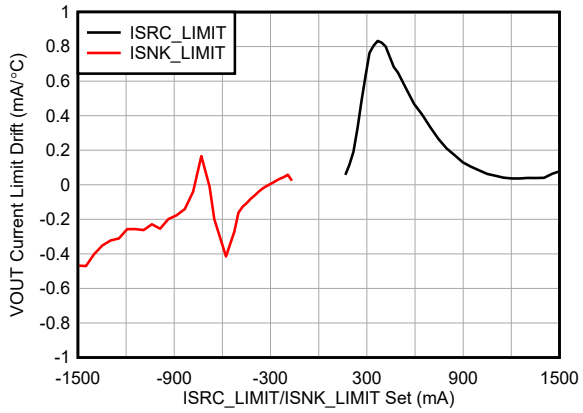
$R_{LOAD} = 12.5\Omega$

Figure 5-36. Output Current Limit vs ILIMIT Set

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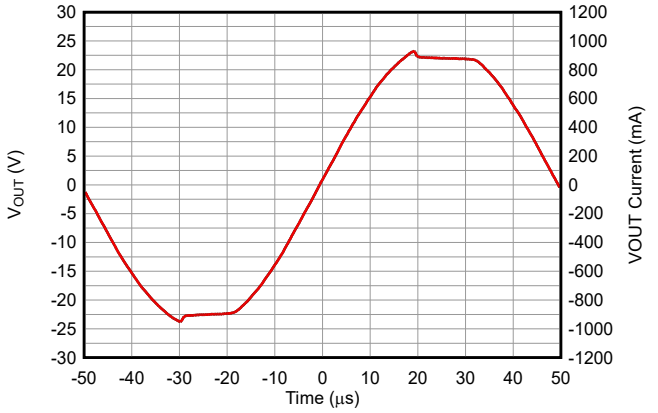
5.7 Typical Characteristics (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, R_S = 5Ω, and V_S = 60V (unless otherwise noted)



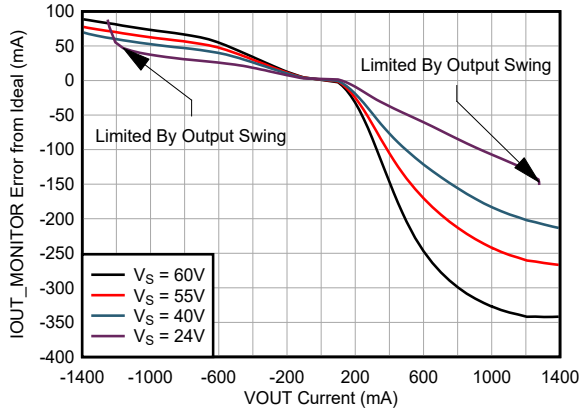
R_{LOAD} = 12.5Ω

Figure 5-37. Output Current Error Drift vs ILIMIT Set



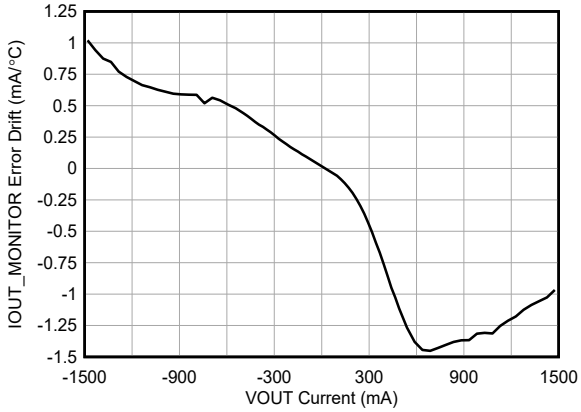
R_{LOAD} = 25Ω, V_{OUT} = 50V_{PP}, ILIMIT = 900mA, f_{in} = 10kHz

Figure 5-38. Output Current Limit vs Time



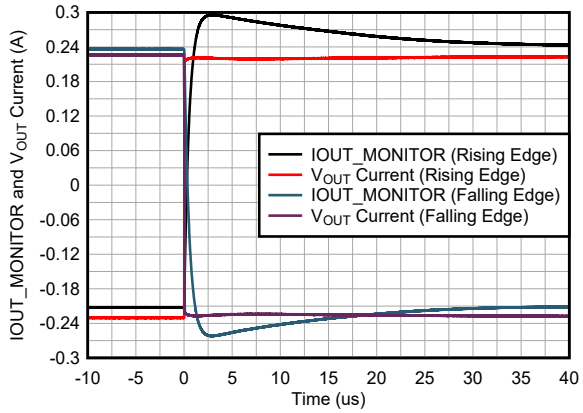
R_{LOAD} = 12.5Ω

Figure 5-39. IOUT_MONITOR Error vs Output Current



R_{LOAD} = 12.5Ω

Figure 5-40. IOUT_MONITOR Temperature Drift vs Output Current



V_{OUT} = 50V_{PP}, RLOAD = 100Ω, R_{IOUT_2048} = 5kΩ

Figure 5-41. IOUT_MONITOR Response Time

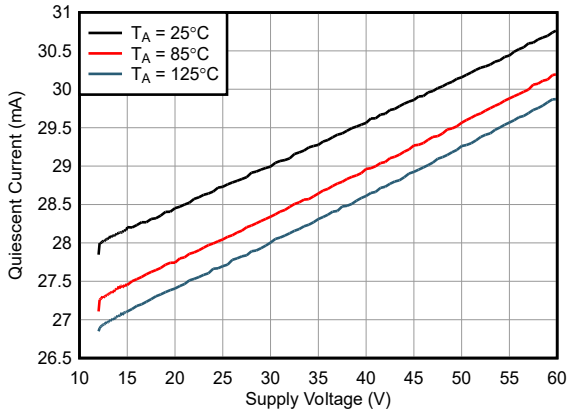


Figure 5-42. Quiescent Current vs Supply Voltage

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5.7 Typical Characteristics (continued)

at T_A ≅ 25°C, A_V = 10V/V, R_F = 2kΩ, R_S = 5Ω, and V_S = 60V (unless otherwise noted)

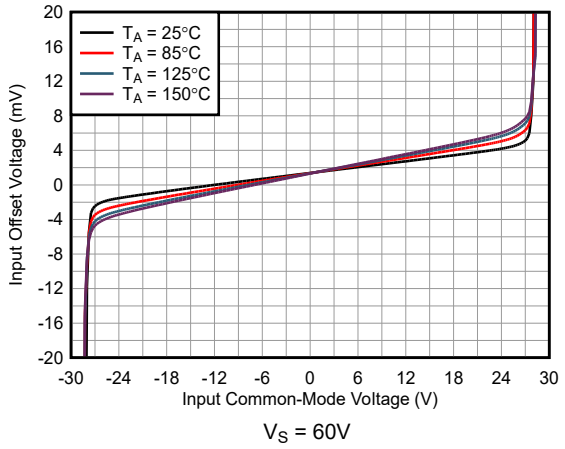


Figure 5-43. Input Offset vs Input Common-Mode

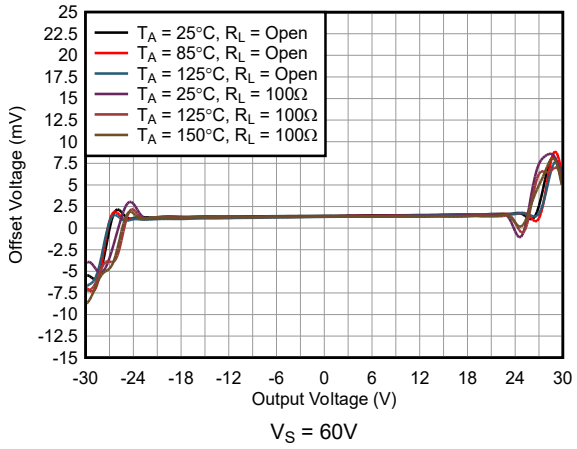


Figure 5-44. Input Offset vs Output Voltage

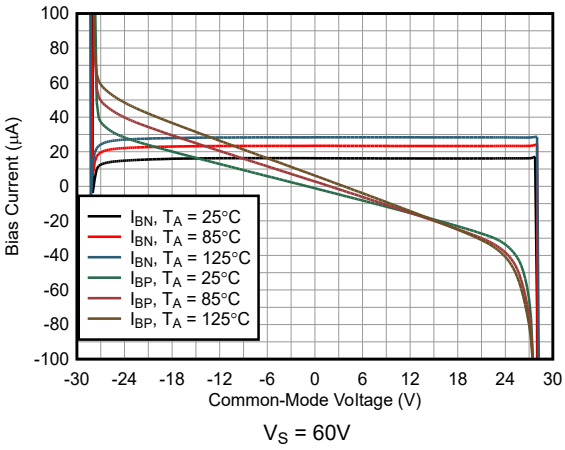


Figure 5-45. Input Bias Current vs Input Common-Mode

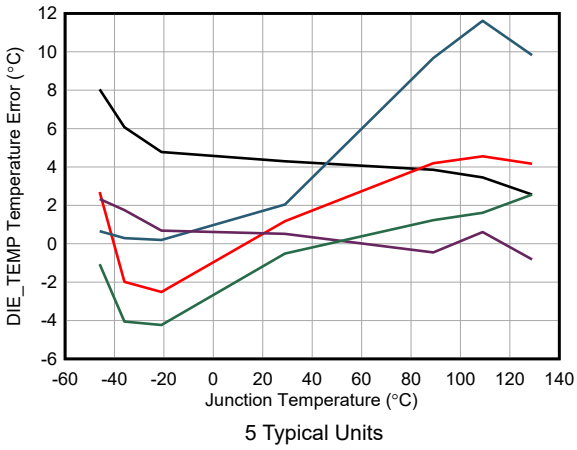


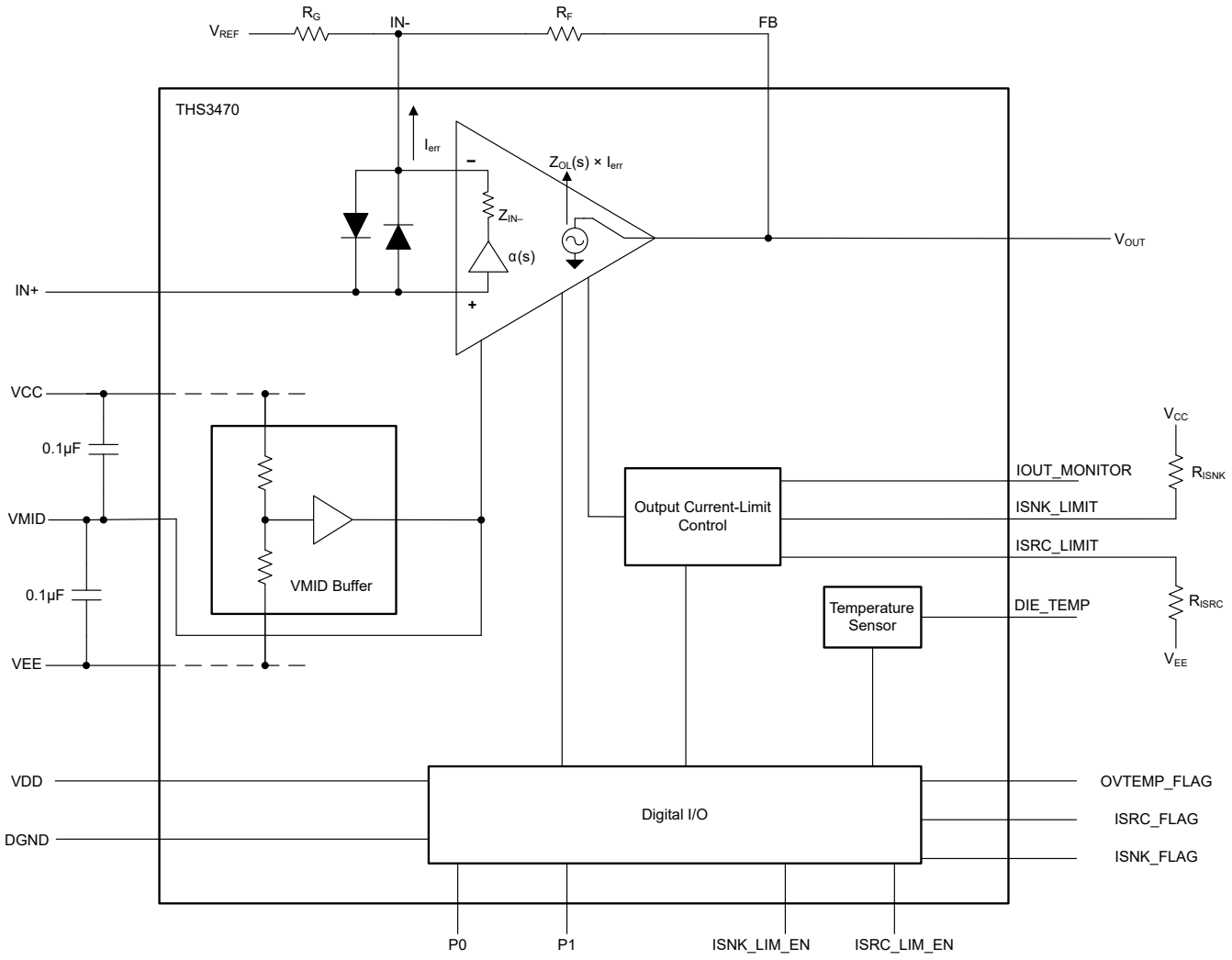
Figure 5-46. DIE_TEMP Accuracy vs Temperature

6 Detailed Description

6.1 Overview

The THS3470 is a 60V current-feedback amplifier that is capable of driving large dynamic and static output currents up to 1.35A. For arbitrary waveform generator applications, the THS3470 creates large-signal sinusoids up to $50V_{PP}$ at 22MHz into 100Ω transmission lines. For LCD test applications, the THS3470 can create $50V_{PP}$ voltage pulses at 2kV/µs into a 1nF of capacitive load. The THS3470 comes equipped with a wide variety of diagnostic pins to help monitor and limit device thermals and output currents. The device also comes in an REB package (42-pin VQFN) with top-side heat dissipation that provides $R_{\theta JA}$ performance of 4°C/W of thermal resistance with forced air and a heat sink. This combination of features makes the THS3470 a unique catalog power amplifier for a host of high-voltage and high-output-current applications.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Output Current Limit

The THS3470 features two pins, ISRC_LIMIT and ISNK_LIMIT, that set output current limits through the VOUT pin. ISRC_LIMIT controls the VOUT sourcing current limit (current exiting the device output, I_{OUT} source) from 200mA to 1.5A. ISNK_LIMIT controls the VOUT sinking current limit (current entering the device output, I_{OUT} sink) from 200mA to 1.5A.

Note

To enable the output sourcing limit, governed by the ISRC_LIMIT pin, the $\overline{\text{ISRC_LIMIT_EN}}$ pin must be low. To enable the output sinking limit, governed by the ISNK_LIMIT pin, the $\overline{\text{ISNK_LIMIT_EN}}$ pin must be low.

CAUTION

If ISRC_LIMIT or ISNK_LIMIT is left unconnected, the device defaults to a 2.1A current limit. If ISRC_LIMIT or ISNK_LIMIT is set for less than 200mA, the device enters a 2.1A current limit. Failure to properly regulate the current can increase the junction temperature beyond the absolute maximum junction temperature and cause damage to the device.

To statically set the output sourcing limit, connect resistor R_{SRC_LIMIT} from ISRC_LIMIT and VEE. To statically set the output sinking limit, connect resistor R_{SNK_LIMIT} from ISNK_LIMIT and VCC. Figure 6-1 shows an example of these connections, the equations that govern the current limit are shown in Equation 1 and Equation 2, and the resistor values for typical applications are shown in Table 6-1.

$$R_{SRC_LIMIT} = \frac{(V_{MID} - V_{EE}) \times 2048}{I_{OUT}\ \text{Source Limit (A)}} - 720 \quad (1)$$

$$R_{SNK_LIMIT} = \frac{(V_{CC} - V_{MID}) \times 2048}{I_{OUT}\ \text{Sink Limit (A)}} - 720 \quad (2)$$

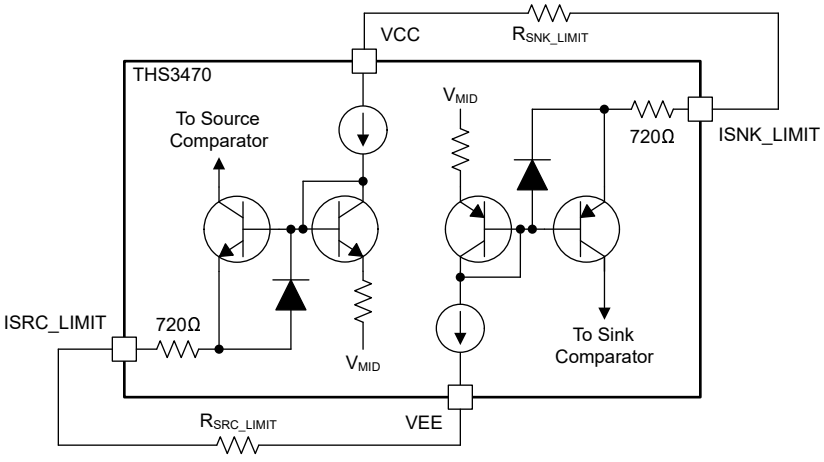


Figure 6-1. Statically Set Output Current Limit

Table 6-1. Typical Resistor Values for Statically Set Output Current Limit

V_S (V)	I_{OUT} Source/Sink Limit (A)	$R_{SNK_LIMIT}/R_{SRC_LIMIT}$ (Ω)
60	0.2	306k
60	0.5	122k
60	1	60k
60	1.5	40k
40	0.2	204k

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Table 6-1. Typical Resistor Values for Statically Set Output Current Limit (continued)

V_S (V)	I_{OUT} Source/Sink Limit (A)	$R_{SNK_LIMIT}/R_{SRC_LIMIT}$ (Ω)
40	0.5	81k
40	1	40k
40	1.5	27k

Alternatively, the current limit pins can be adjusted through a voltage digital-to-analog converter (DAC), or other low impedance voltage source, as shown in Figure 6-2. This method helps provide programmable control of the output current limit if the application requires. The equation that governs the current limit for this method is shown in Equation 3 and Table 6-2 shows examples of dynamically configuring the current limit.

$$V_{DAC}\,(V) = I_{OUT}(A) \times \frac{4.5k\Omega}{2048} \tag{3}$$

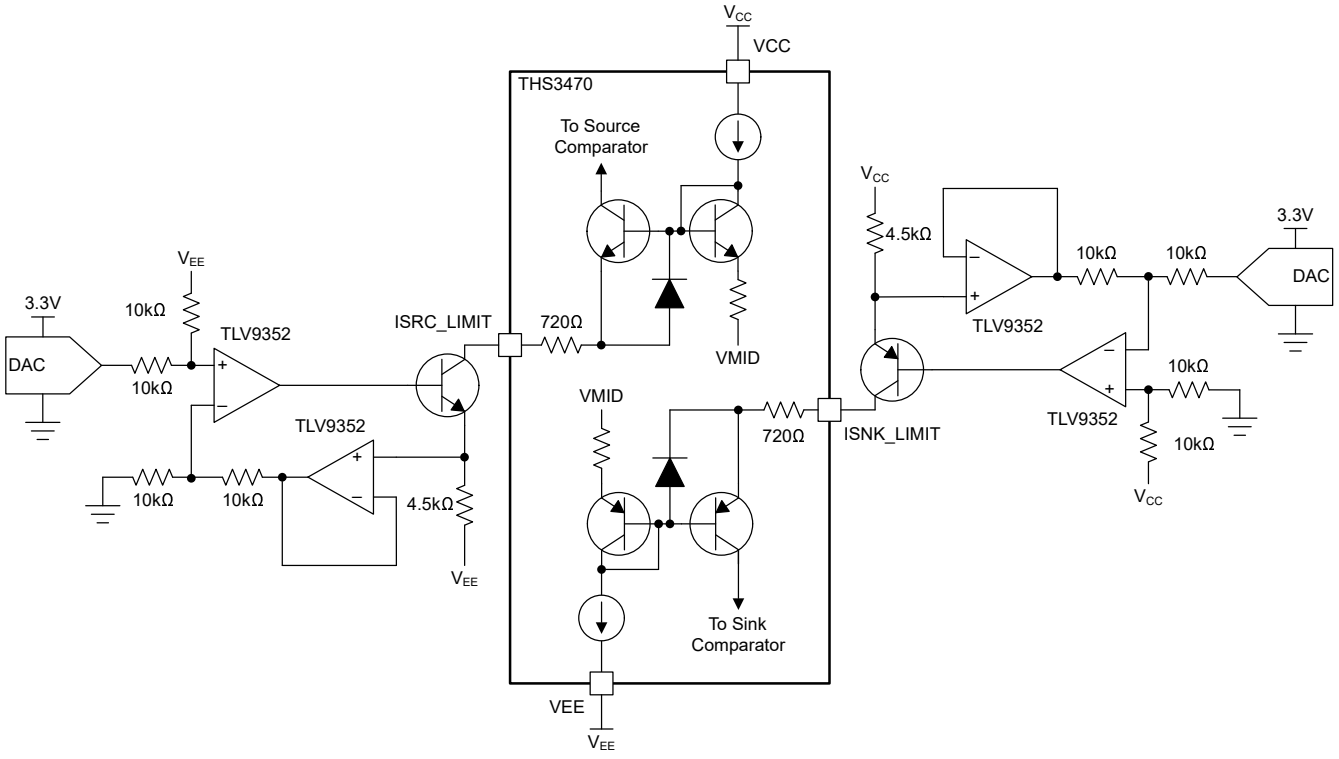


Figure 6-2. Dynamically Set Output Current Limit

Table 6-2. Example DAC Voltages for Dynamically Set Output Current Limit

V_{OUT} CURRENT LIMIT (mA)	$I_{LIMIT_SRC/SNK}$ (µA)	DAC VOLTAGE, V_{DAC} (V)
200	97.65	0.439
500	24.41	1.099
1000	488.28	2.197
1500	732.42	3.296

CAUTION

Make sure that the ISNK_LIMIT voltage is greater than the VMID voltage, and that the ISRC_LIMIT voltage is less than the VMID voltage. Failure to adhere to this caution can result in damage to the device. Additionally, the VMID pin must be externally buffered to be used as a power supply.

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6.3.2 Output Current Enable

The THS3470 features two pins, $\overline{\text{ISNK_LIMIT_EN}}$ and $\overline{\text{ISRC_LIMIT_EN}}$ that allow toggling of the internal current limiting features set by the ISNK_LIMIT and ISRC_LIMIT pins.

If the $\overline{\text{ISNK_LIMIT_EN}}$ pin is connected low, the internal current limit for sinking current is activated, and the current at the VOUT pin is regulated according to the ISNK_LIMIT configuration. If the $\overline{\text{ISNK_LIMIT_EN}}$ is connected high, the internal current limit for sinking current is deactivated and limited by the inherent maximum allowable current (2.1A). Regardless of the $\overline{\text{ISNK_LIMIT_EN}}$ pin configuration, the $\overline{\text{ISNK_FLAG}}$ pin triggers when the VOUT sinking current exceeds the threshold dictated by the ISNK_LIMIT configuration.

For the $\overline{\text{ISNK_LIMIT_EN}}$ disabled case, use this functionality as a warning flag when the device is approaching a limit that must be monitored closely for system health using the I_{OUT} pin or the $\overline{\text{OVTEMP_FLAG}}$ pin. This approach gives designers an option to better control when to disable or shutdown the device on a microcontroller; Figure 6-3 shows this option. If the application does not require fine control of the current limit, designers can hard connect the $\overline{\text{ISNK_FLAG}}$ pin to the $\overline{\text{ISNK_LIMIT_EN}}$ pin; Figure 6-3 also shows this option.

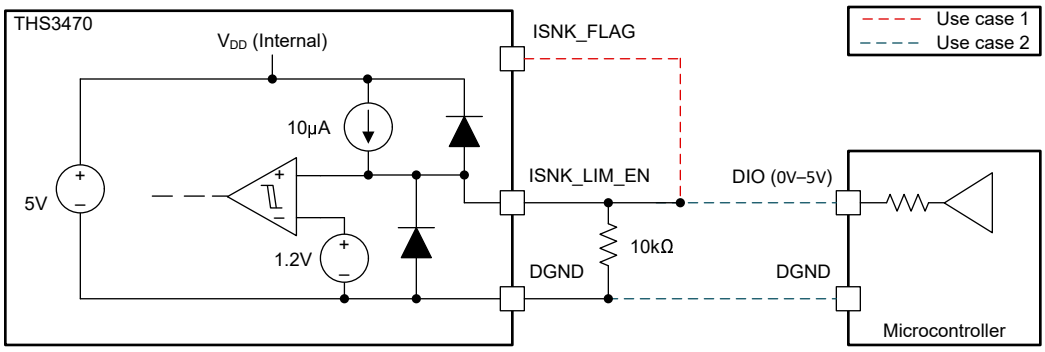


Figure 6-3. Output Current Enable Schematic

The $\overline{\text{ISRC_LIMIT_EN}}$, ISRC_LIMIT, and $\overline{\text{ISRC_FLAG}}$ pins all function identically to the sinking current equivalents, but instead govern the sourcing limits of the VOUT pin.

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6.3.3 Over Temperature Flag

The THS3470 over temperature flag, $\overline{\text{OVTEMP_FLAG}}$, is used to monitor when the internal thermal shutdown of the device is active. The $\overline{\text{OVTEMP_FLAG}}$ typically asserts low when the die temperature exceeds 160 degrees, depending on process variation of the device. After asserting the flag low, the flag typically asserts high when the device temperature cools to 140 degrees, also dependent on process variation, to create a hysteresis window to prevent the device from continuously asserting an de-asserting.

There are two primary use cases for the over temperature flag. The typical use case is to connect the $\overline{\text{OVTEMP_FLAG}}$ directly to the P0 and P1 pins to allow the device to thermally shutdown when the die temperature is too hot. Additionally, if one of the other power modes is desired on the P0 and P1 pins, a logical AND gate can be used with the preferred P0 and P1 bias states. The second use case is to connect $\overline{\text{OVTEMP_FLAG}}$ to a digital input/output pin of a micro controller and monitor the pin as a temperature warning flag. In this case, the micro controller can make decisions, along with the DIE_TEMP pin, to toggle the P0 and P1 pins earlier or later than when the P0 or P1 pins are tied to the $\overline{\text{OVTEMP_FLAG}}$ to more tightly control the thermal regulation of the THS3470.

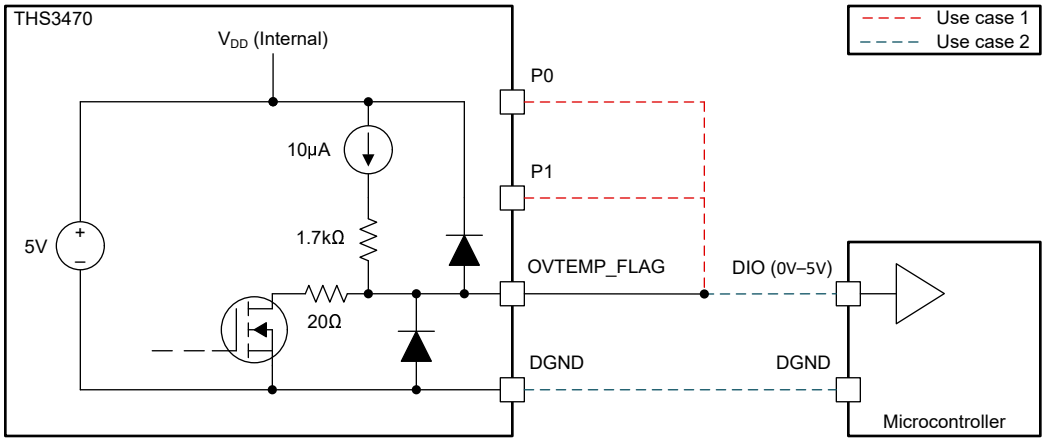


Figure 6-4. $\overline{\text{OVTEMP_FLAG}}$ Schematic

Note

The device temperature is not always symmetric across the die and "hot spots" can develop depending on the application. Pay special attention to rapid heating scenarios, such as driving large capacitive loads, that cannot trigger the $\overline{\text{OVTEMP_FLAG}}$ in time to save the device from a destructive failure. Refer to the Safe Operating Area of the data sheet for more information on preventing device overheating in these applications.

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6.3.4 Output Current Flags

The THS3470 output current flags, $\overline{\text{ISNK_FLAG}}$ and $\overline{\text{ISRC_FLAG}}$, are used to monitor when the current limits set by ISNK_LIMIT and ISRC_LIMIT and are met or exceeded on the VOUT pin of the device. If the ISNK_LIMIT current sinking limit (current entering the device output) is exceeded, the $\overline{\text{ISNK_FLAG}}$ pin is pulled low to DGND. If the ISNK_LIMIT current sinking limit is not exceeded, the $\overline{\text{ISNK_FLAG}}$ pin is pulled high to the internal VDD voltage of 5V. If the ISRC_LIMIT current sourcing limit (current exiting the device output) are exceeded, the $\overline{\text{ISNK_FLAG}}$ pin is pulled low to DGND. If the ISRC_LIMIT current sourcing limit is not exceeded, the $\overline{\text{ISNK_FLAG}}$ pin is pulled high to the internal VDD voltage of 5V.

Note

The output current flags function the same, regardless of the state of the output current enable flags.

There are two primary use cases for the output current flags. The first use case is to connect the $\overline{\text{ISNK_FLAG}}$ to the $\overline{\text{ISNK_LIMIT_EN}}$ pin to allow the device to self-limit the current into VOUT. The second use case is to connect $\overline{\text{ISNK_FLAG}}$ to a digital input/output pin of a microcontroller and monitor the pin as a current-warning flag. For more information regarding each of these use cases, see also Section 6.3.2.

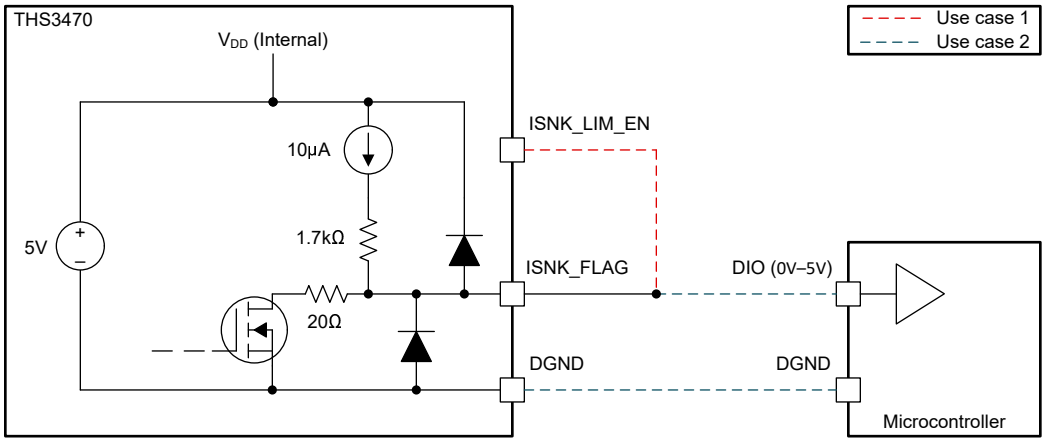


Figure 6-5. ISNK_FLAG Schematic

6.3.5 Output Current Monitoring

The $I_{OUT_MONITOR}$ pin is used to monitor the output current (I_{OUT}) that is entering (sinking) or exiting (sourcing) the VOUT pin. To monitor the output current, the $I_{OUT_MONITOR}$ pin uses an internal current mirror to create a scaled-down current source that mirrors the output current through the VOUT pin. Equation 4 shows the equation that governs the relationship of the $I_{OUT_MONITOR}$ pin and output current.

$$I_{OUT_MONITOR} = \frac{I_{OUT}}{2048} \quad (4)$$

For example, if the VOUT pin is sourcing 204.8mA, the $I_{OUT_MONITOR}$ pin sources 100µA. Alternatively, if the VOUT pin is sinking 204.8mA, the $I_{OUT_MONITOR}$ pin sinks 100µA.

CAUTION

Keep $I_{OUT_MONITOR}$ within 5V of the VMID pin. Failure to adhere to this caution can result in damage to the device.

To read the IOUT_MONITOR current with an ADC, include the external transimpedance circuit shown in Figure 6-6. This circuit is intended to achieve three key objectives. The first objective is to convert the IOUT_MONITOR pin current to a voltage (V_{OUT_TIA}) that scales to match the ADC range (V_{ADC_RANGE}). The second objective is to shift the V_{OUT_TIA} voltage to 1/2 V_{ADC_RANGE} when IOUT_MONITOR is equal to 0A. The last objective is to keep the IOUT_MONITOR pin within ±5V of the VMID voltage.

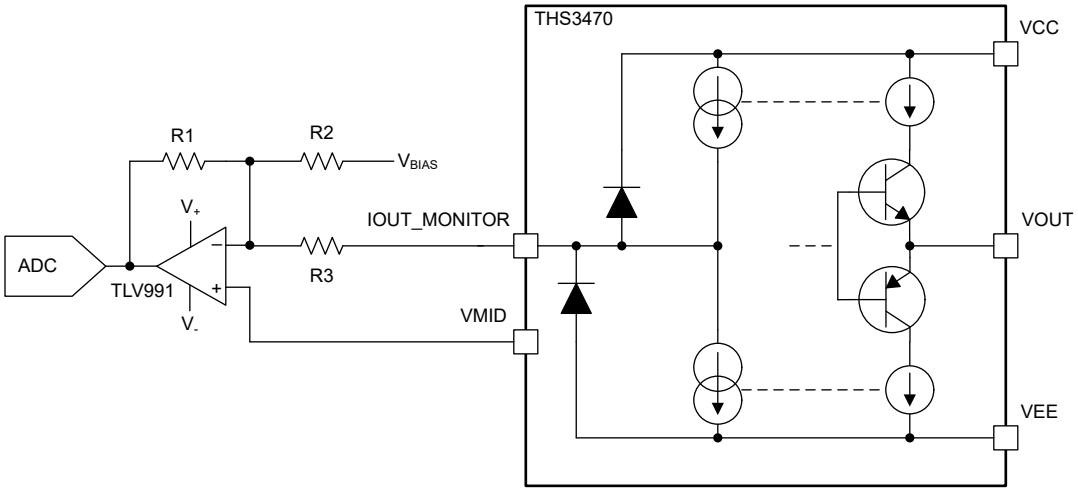


Figure 6-6. IOUT_2048 Transimpedance Schematic

Resistor R_1 in the transimpedance circuit is ultimately responsible for converting the maximum expected current (I_{MAX}) from IOUT_MONITOR into a voltage that is optimized for the V_{ADC_RANGE}. To calculate R_1 for the transimpedance circuit, use Equation 5.

$$R_1 = \frac{V_{ADC_RANGE}}{I_{MAX}} \quad (5)$$

For example, if the maximum expected current (typically governed by the output-current-limit pin configurations) is ±1A, the I_{MAX} current is 1A / 2048 = 488µA. If a 3.3V ADC is used in the application, the V_{ADC_RANGE} for the application is 3.3V. Plugging these values into Equation 5 results in an R_1 value of 3.381kΩ.

Resistor R_2 in the transimpedance circuit is responsible for shifting V_{OUT_TIA} to 1/2 of V_{ADC_RANGE} when $I_{OUT_MONITOR}$ is equal to 0A. To shift, use a proper reference voltage (V_{BIAS}) that depends on the supply configuration of the THS3470. If the device is operating in a positive single-ended supply configuration (that is, V_{CC} = 60V and V_{EE} = 0V), then V_{BIAS} can be connected to the VCC pin. If the device is operating in a negative single-ended supply configuration (that is, V_{CC} = 0V and V_{EE} = –60V), then V_{BIAS} can be connected to the VEE

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pin. If the device is operating in a split-supply configuration (that is, V_{CC} = 30V and V_{EE} = –30V), then V_{BIAS} can be connected to the ADC supply voltage (V_{ADC}). Ultimately, there is a large permutation of V_{BIAS} voltages than can be used, but the suggested options are selected based on the available voltages already existing in the design. Equation 6 shows how to calculate R_2 after the V_{BIAS} voltage has been selected.

$$R_2 = R_1 \times \left(\frac{V_{BIAS} - V_{MID}}{V_{MID} - \frac{V_{ADC_RANGE}}{2}} \right) \quad (6)$$

For example, if the R_1 resistor is sized to convert a ±488µA current from IOUT_MONITOR to ±1.65V at V_{OUT_TIA}, then the R_2 resistor is selected to move the V_{OUT_TIA} voltage to 1.65V (½ V_{ADC_RANGE}) when the IOUT_MONITOR current is 0A. The supply in this example is a split-supply configuration; therefore, V_{BIAS} is tied to the ADC supply voltage V_{ADC}, which is 3.3V. The V_{MID} voltage is always the average of V_{CC} and V_{EE}, resulting in a voltage of 0V for this example. Plugging in these values to Equation 6 results in an R_2 value of 30kΩ.

The last resistor in the transimpedance amplifier circuit is R_3, which is responsible for keeping the IOUT_MONITOR voltage within ±5V of the V_{MID} voltage. R_3 is also responsible for protecting the pin during start-up events for the THS3470, and is scaled to limit the input current to < 10mA. The noninverting input pin of the transimpedance amplifier is connected to V_{MID} as well as the inverting input pin through negative feedback; therefore, R_3 is sized to limit the voltage drop across R3 to ±4.5V. The maximum current that the THS3470 can provide is 2.1A at I_{OUT}, which results in a maximum allowable current of approximately ±1mA from IOUT_MONITOR. Dividing the maximum allowable voltage of ±4.5V by the maximum current of ±1mA results in a resistance value of 4.5kΩ for R_3.

After the components and bias voltages have been selected, Section 6.3.5 is used to convert V_{OUT_TIA}voltage read by the ADC to I_{OUT}. In addition, Table 6-3 lists some common use cases to help select resistors and bias voltages.

$$I_{OUT} = 2048 \times \left(\frac{V_{OUT_TIA} - V_{MID}}{R_1} \right) \quad (7)$$

Table 6-3. IOUT_2048 Transimpedance Amplifier Configuration (V_{ADC} = 3.3V, I_{MAX} = 1A, R_1 = 3.381kΩ)

USE CASE	R_2 (kΩ)	V_{BIAS} (V)	V+ (V)	V– (V)
Split supply (±20V)	40.96	V_{EE}	V_{ADC}	0
Split supply (±30V)	61.44	V_{EE}	V_{ADC}	0
Single ended (40V)	3.683	V_{CC}	V_{MID}	0
Single ended (60V)	3.576	V_{CC}	V_{MID}	0
Single ended (–40V)	3.121	V_{EE}	V	V_{MID}
Single ended (–60V)	3.203	V_{EE}	V_{ADC}	V_{MID}

Note: V_{ADC} is the ADC supply voltage.

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6.3.6 Die Temperature Monitoring

The THS3470 DIE_TEMP pins converts the die junction temperature to an ADC-readable voltage between 0V and 3.3V. To convert the DIE_TEMP voltage to the die junction temperature, use Equation 8. Use DIE_TEMP to monitor the health of the device and shut down the device using the P0 and P1 pins, or to limit the output current using the output current enable pins. For more information about using these diagnostic functions in tandem with the DIE_TEMP, see also Section 6.3.1 and Section 6.3.2.

$$\text{Junction Temperature}\left(T_J\right) = 208 \times \left(V_{DIE_TEMP} - 1.415\right) \quad (8)$$

For application where the DIE_TEMP is not used, or is only used for debug purposes, designers can simply connect a test point to the pin. The output of the DIE_TEMP pin is internally buffered, so passive scope probes or digital multimeter can be connected without impacting the accuracy of the pin.

Certain applications, such as split-supply operation, require additional circuitry to level-shift the DIE_TEMP voltage into an on board ADC. To level shift, use the difference amplifier circuit in Figure 6-7. Depending on the voltage span of the supply pins, use the TLV9351 (40V) or OPA596 (85V) with the positive supply tied to the ADC supply and the negative supply tied to V_{EE}.

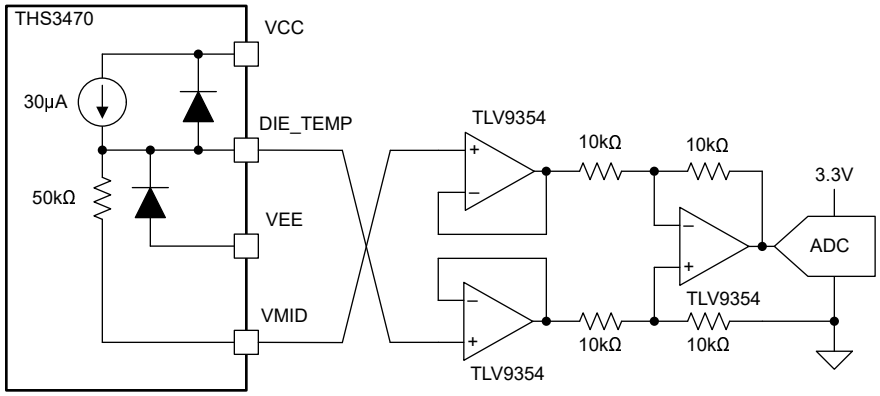


Figure 6-7. DIE_TEMP Level-Shifting Circuit

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6.3.7 External Compensation

The THS3470 COMP pin can be used to limit the bandwidth or slew rate of the amplifier by connecting an external capacitor between the COMP pin and the VOUT pin. Figure 6-8 shows a conceptual block diagram of how the COMP pin acts as an external output compensation network for the device. Using the COMP pin is a context dependent situation, as shown by Figure 6-9 and Figure 6-10, and is typically used in high capacitive load applications needing lower isolation resistances to help properly damp the control loop of the amplifier.

Note

If the compensation pin is not being used, system designers must leave the pin floating and remove the ground plane around and under the pin on the PCB. Parasitic capacitance on the COMP pin can create an undesired reduction in the device's bandwidth and slew rate.

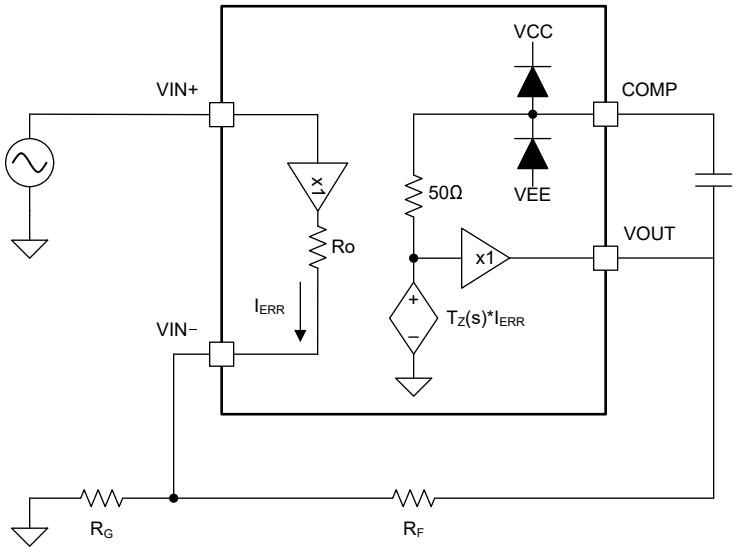


Figure 6-8. THS3470 COMP Pin Conceptual Block Diagram

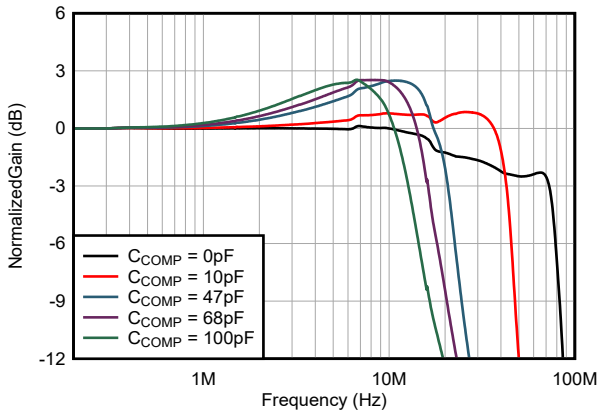


Figure 6-9. THS3470 Small-Signal Bandwidth vs C_{COMP} (R_S = 0Ω, C_{LOAD} = 1nF)

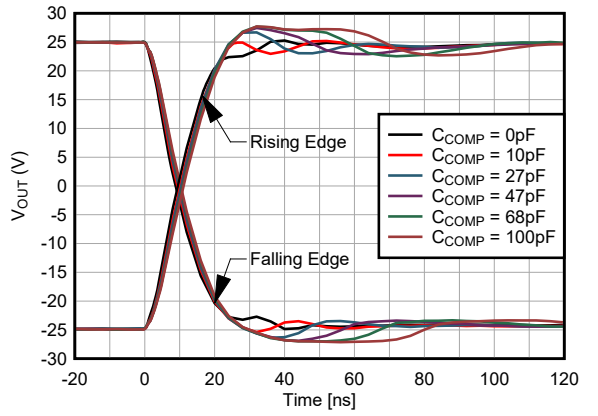


Figure 6-10. THS3470 Large Signal Step vs C_{COMP} (R_S = 0Ω, C_{LOAD} = 1nF)

6.4 Device Functional Modes

6.4.1 Power Modes

The THS3470 features two power-mode control pins P0 (pin 31) and P1 (pin 30) that set the power level of the device. These pins are controlled by connecting the pins to either VDD or DGND of the THS3470. Table 6-4 shows the configurable options for the THS3470.

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Note

The majority of the *Electrical Characteristics* parameters are measured in the full bias mode of the device.

Table 6-4. THS3470 Power Modes

P0	P1	MODE
DGND	DGND	Power Down
VDD	DGND	Low Bias
DGND	VDD	Mid Bias
VDD	VDD	Full Bias

Special care must be taken when the device is in the Power Down state to limit the input current. System designers need to set the input voltage of the device is set so the non-inverting and inverting terminals are at the same voltage potential. Since the THS3470 has anti-parallel diodes to protect the input devices, setting a differential voltage across the inputs during a power down state can conduct current and potentially exceed the absolute maximum allowed current for the input pins. For more information regarding the absolute maximum current on the input pins, refer to Section 5.1

Figures Figure 6-11, Figure 6-12, Figure 6-13, and Figure 6-14 show how the THS3470 performance changes with bias mode for the most prevalent application test conditions. Designers need to evaluate the frequency performance in the specific application of interest to gain proper insight into whether a lower power mode provides acceptable performance. Special consideration must be given when R_{FB} values of less than 2kΩ are chosen to improve the bandwidth or isolation resistors smaller than 5Ω are used in tandem with varying capacitive loads.

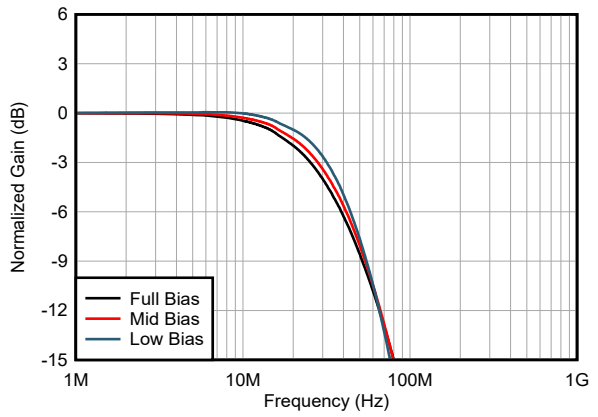


Figure 6-11. Small-signal Bandwidth vs Frequency (R_F = 2kΩ, R_S = 5Ω, C_L = 1nF)

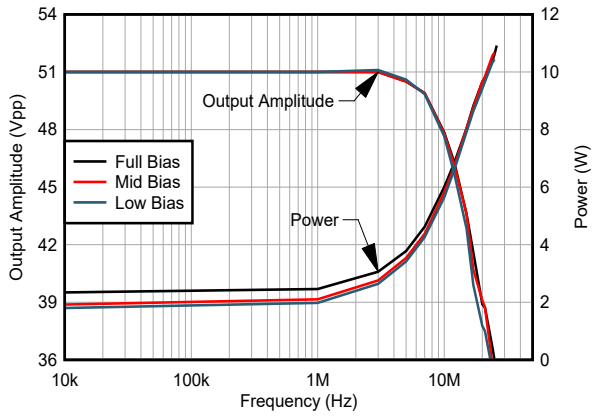


Figure 6-12. Large-signal Bandwidth vs Frequency (R_F = 2kΩ, R_S = 5Ω, C_L = 1nF)

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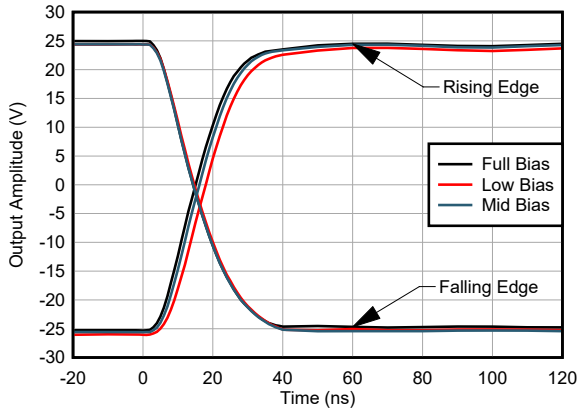


Figure 6-13. Large-signal Step Response vs Frequency (R_F = 2kΩ, R_S = 5Ω, C_L = 1nF)

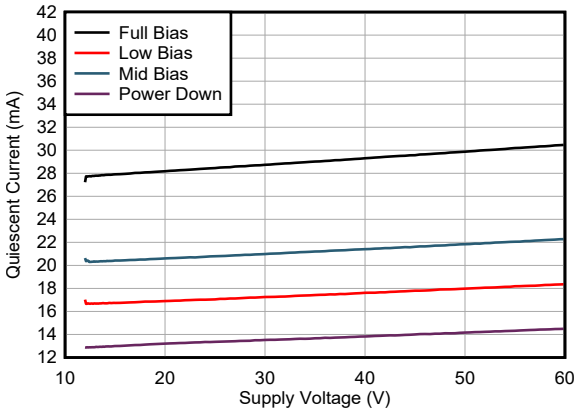


Figure 6-14. Quiescent Current vs Supply Voltage

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6.4.2 Choosing a Feedback Resistor

The THS3470 is a high voltage, high speed, current feedback amplifier that requires special attention when selecting feedback component values. Since the THS3470 can output >50V_{PP} signals, large amounts of transient current can be dissipated in the feedback path of the amplifier. Additionally, since the THS3470 is also a high speed current feedback amplifier, the feedback resistor needs to be kept small to keep the bandwidth high. Since these two design objectives directly impact each other, designers need to choose components values shown in Table 6-5 when beginning designs with the THS3470. Once baseline performance has been established, designers can experiment with lower feedback resistor values, depending on the application, while monitoring the DIE_TEMP pin and working to limit the die temperature within the operating maximum of the device.

Table 6-5. THS3470 Recommended Resistors

Supply Voltage	Desired Gain (A_V)	R_G	R_{FB}
40V	-1	1.2kΩ	1.2kΩ
40V	+1	N/A	1.2kΩ
40V	+10	133	1.2kΩ
40V	+100	12	1.2kΩ
60V	+-1	2kΩ	2kΩ
60V	+1	N/A	2kΩ
60V	+10	220	2kΩ
60V	+100	20	2kΩ

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The THS3470 is a high-speed, high-voltage, high-current operational amplifier. The device is capable of creating voltage pulses of 2000V/µs at $50V_{PP}$ into 1nF capacitive loads. In addition to the THS3470 fast transient performance, the THS3470 can pass large signals at $50V_{PP}$ into 100Ω transmission lines for frequencies up to 22MHz. With regards to high-current operation, the THS3470 has separate current-limit features for output sourcing and sinking, with a configurable range from 200mA to 1.5A. To help system designers with device diagnostics and protection, the THS3470 comes with temperature and current flags to signify over-temperature or over-current conditions of the device. Additionally, designers may use the die temperature pin for more granular readouts of the device junction temperature to proactively take steps for system protection.

7.2 Typical Application

7.2.1 High-Voltage, High-Precision, Composite Amplifier

A common problem for test and measurement applications is creating a high-precision and high-slew-rate signal source. Typical high-voltage amplifiers offer a large supply voltage and high slew rate, but many of the dc specifications such as offset, offset drift, and open-loop gain impact the accuracy of the output signal. In contrast, many precision amplifiers on the market show impressive offset, offset drift, and open-loop gain performance, but are lacking the required supply voltage, output current, and slew rate required for the application.

A unique design that addresses the design requirements of high voltage and high precision is the composite amplifier. A composite amplifier uses two amplifiers in tandem, one that is high voltage and one that is high precision, inside the same feedback loop to optimize performance for each amplifier. The precision amplifier operates closer to the signal source, allowing the device to maximize it's impact on input related parameters such as offset and offset drift. The high voltage amplifier operates closer to the device under test, allowing the device to maximize impact on output related parameters such as slew rate, output current, and high voltage output swing.

An additional feature of this design is the force and sense connections on the output of the composite amplifier. Many test and measurement applications, such as source-measure units and power supplies, have long cables and traces in between the device under test (DUT) and the output of the composite amplifier. When large output currents begin to flow along these traces and cables, there is a voltage drop that causes a large output related error. For instance, if 1A of current flows along a 5Ω cable, there is a 5V voltage drop from the output of the composite amplifier to the DUT. This undesired effect also occurs when using large isolation resistors, typically referred to as R_S, which improve the capacitive load drive of the composite amplifier when driving large DUT decoupling capacitors.

The force and sense connections minimize these errors by bringing the feedback connection of the composite amplifier, known as the sense connection, to the DUT on a different cable or trace the than output trace, known as the force connection. When higher current flows across the force connection resistances, either R_S or the cable (trace) resistance, the sense path measures at the DUT output pin and compensates the output to adjust for the voltage drop along the force line. Cable resistance on the sense path does not experience large voltage drops in most circumstances because the only current returning on the sense line is the feedback current for the amplifier. For example, if a 5V voltage drop occurs along the force connection, as per our previous example, the composite amplifier increases the output voltage by 5V to compensate for the line drop and gives the correct DUT voltage at the pin.

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Note

Keep both feedback resistors on both amplifiers as close as possible to the inverting input pin in the printed circuit board (PCB) layout. Additionally, keep the isolation resistors as close to the output as possible to minimize parasitic capacitance on the output. These best practices help minimize the effects of parasitic capacitance on the input and output, which can cause instability or oscillations.

Note

Even though the force and sense connections compensate for voltage drops across the force connection, pay special attention to the output voltage swing of the output amplifier. Compensating for large force-connection errors limits the usable output range from the perspective of the DUT input.

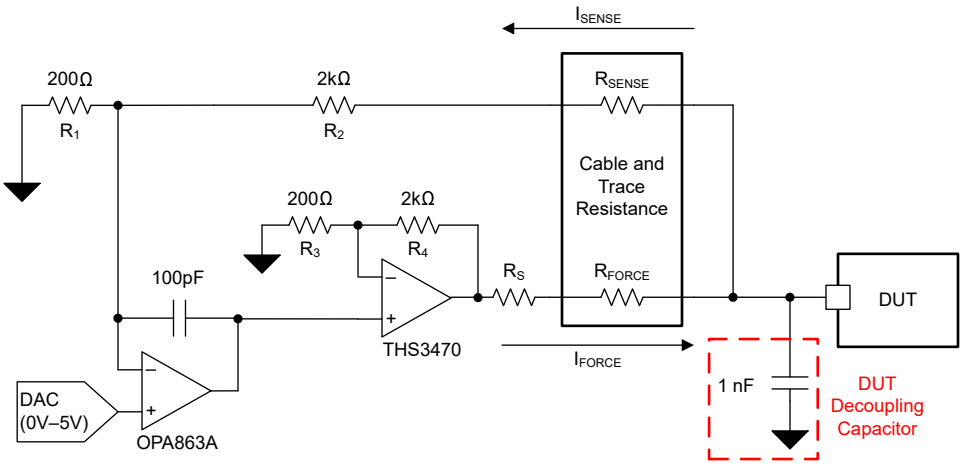


Figure 7-1. High-Voltage and Precision Composite Amplifier

7.2.1.1 Design Requirements

The goal of this design is to optimize the output referred error of the THS3470 while preserving settling behavior using a composite loop. The input step for this design was chosen to be 5V to match a typical DAC to set the output voltage of the design. The output current (1A), output swing ($40V_{PP}$), settling time (250ns), and output referred error (<0.1%) were all chosen based on the theoretical maximum performance of the OPA863A and THS3470. If higher precision is required, an OPA328, OPA387, or OPA365 can be used instead to reduce the output-referred error at the expense of settling time.

Table 7-1. Design Parameters

PARAMETER	VALUE
Supply voltage	60V
Input step size	4V
Output step size	$40V_{PP}$ (1A)
Output current	Up to 1A
Settling time (0.01%)	250ns
Output-referred error	<0.1%

7.2.1.2 Detailed Design Procedure

The THS3470 is designed for use as a high-slew-rate (3000V/µs), high-output-current (±1.35A), and high-output-swing ($50V_{PP}$) device. These performance features make the THS3470 a great candidate for the output amplifier of a high-voltage and precision composite amplifier. In addition to the performance specifications, the THS3470 has a host of diagnostic functions, such as current and temperature flags and current and temperature monitors, that allow system designers to tightly control and monitor the full system design better than discrete transistors.

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The OPA863A is a high-precision, high-bandwidth amplifier that is an excellent choice to perform as an input amplifier in a composite loop. The low offset (95µV) and offset drift (1.2µV/°C) of the OPA863A allows the composite amplifier to settle to the target output-referred error and minimize heating effects from the THS3470 power dissipation into the PCB. Additionally, the high bandwidth of the OP863A (50MHz) allows the small-signal ripple to be minimized for a fast-settling response after the large transient step.

The total composite amplifier loop gain is defined by the external feedback network formed by R_1 and R_2, which is configured in a gain of 10. This value is chosen to optimize for a 5V DAC, but can be easily adjusted to a gain of 20 by changing R_1 to 100Ω to support a 3.3V DAC. The THS3470 amplifier, configured in a local gain of 10 by the feedback network formed by R_3 and R_4, does not have a large impact on the signal source to DUT output gain. Instead, this amplifier divides the output voltage seen by the OPA863A by a factor of 10. This gain works well for the OPA863A with a 5V supply because the maximum output range of the OPA863A is only 5V. The gain of the THS3470 also gains up the slew rate of the OPA863A to 1000V/µs from the inherent 100V/µs slew rate of the device. Faster slew rates are possible by increasing the THS3470 gain, but an increased slew-rate does not always equate to faster settling time in this configuration.

Figure 7-2 shows an example PCB that was built to characterize the performance of the composite loop design. Without the composite loop, Figure 7-3 shows the output referred error that occurs after R_S, on the "DUT side" of the 5Ω isolation resistor, with a normal THS3470EVM. Figure 7-4, by contrast, shows the output referred error on the "DUT side" of the isolation resistor to be less than 10mV for the composite design. For a full $40V_{PP}$ step, Figure 7-5 shows the transient behavior of the THS3470EVM and composite amplifiers side by side. While the precision of the composite amplifier has been drastically improved, the composite design does come at the expense of worse settling and slew rate performance compared to the default THS3470EVM.

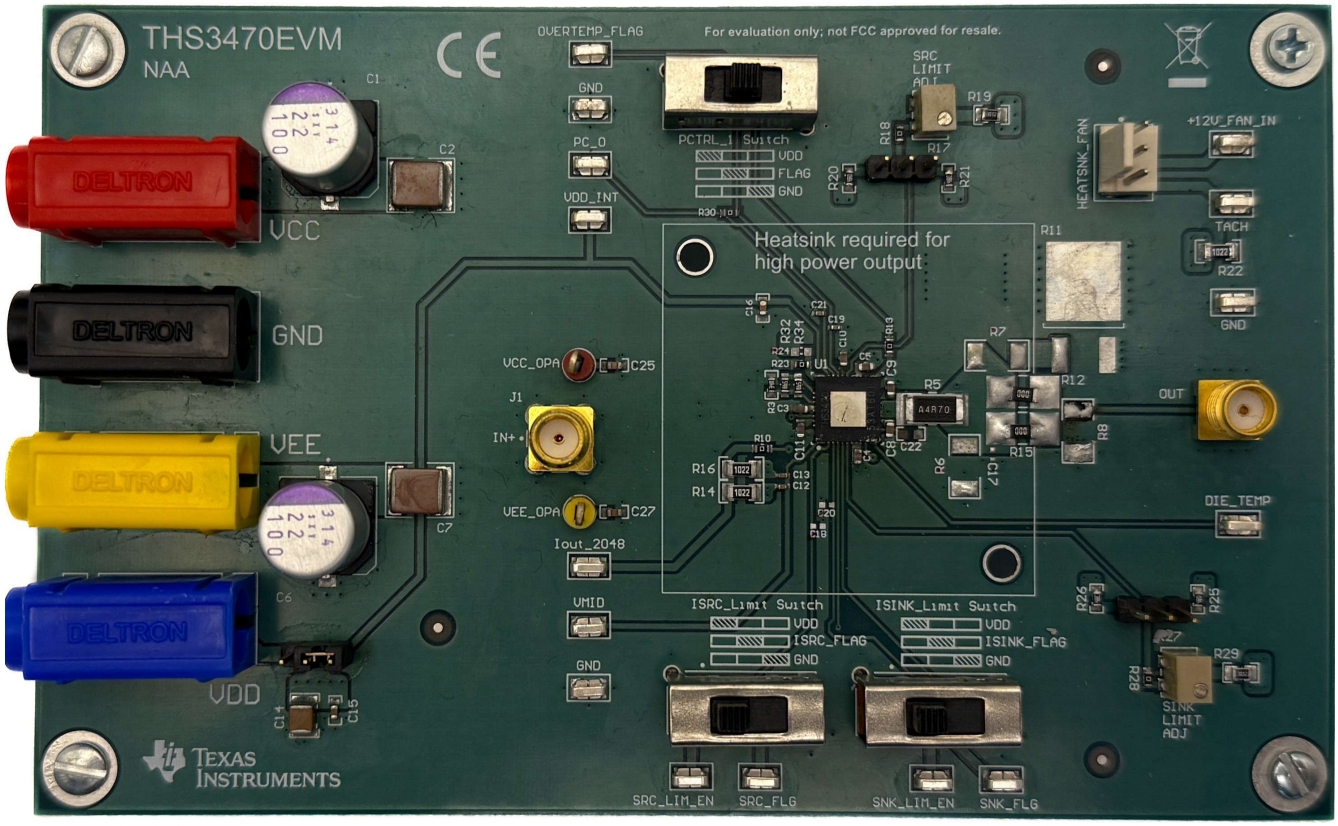


Figure 7-2. THS3470 Composite Amplifier PCB

7.2.1.3 Application Curves

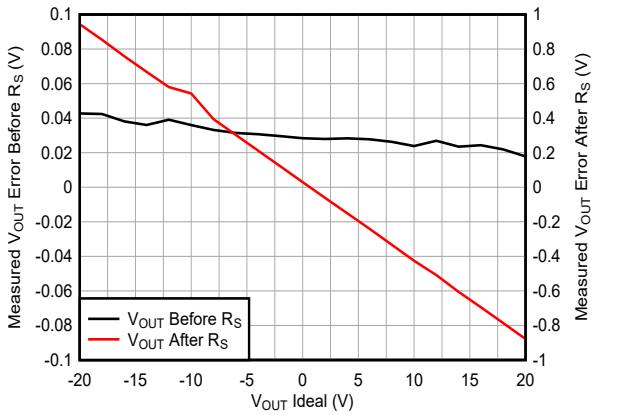


Figure 7-3. THS3470 V_{OUT} error without composite loop (R_L = 100Ω,C_L = 1nF)

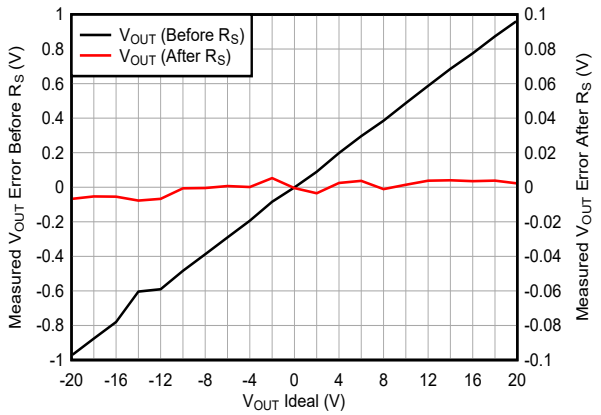


Figure 7-4. THS3470 V_{OUT} error with composite loop (R_L = 100Ω,C_L = 1nF)

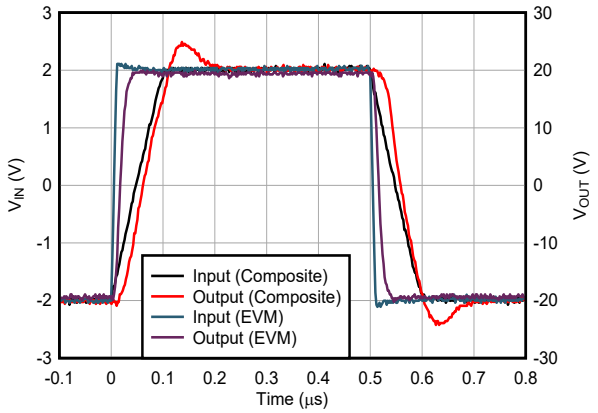


Figure 7-5. THS3470 step response comparison (R_L = 100Ω,C_L = 1nF)

7.2.2 120V Bootstrap Amplifier

The THS3470's unique combination of high supply voltage (60V), high output current (1.35A DC, 2A Peak), and fast slew rate (3kV/us) make the device an attractive option for many applications. Despite the already high voltage of the THS3470 amplifier, many applications demand higher voltage requirements with the unique feature set that the THS3470 already provides. Creating a 3-Amplifier "Bootstrap" design allows designers to increase the voltage headroom while mostly preserving the electrical performance and diagnostic features of the THS3470.

Amplifier bootstrapping uses a resistor divider, a doubled supply range, and two additional amplifiers to move the "signal amplifier" supplies dynamically as the output voltage is moving. The amplifier that is connected to the input signal, as shown in Figure 7-6, is known as the "signal amplifier" and provides the output voltage and current to the application. The "supply amplifiers" are connected such that V_{CC}/V_{EE} = 60V/0V for the top supply amplifier which provides the signal amplifiers V_{CC} connection. Conversely, the bottom supply amplifier has a supply voltage of V_{CC}/V_{EE} = 0V/-60V and provides the signals amplifiers V_{EE} connection. By providing multiple supplies in this way, and using the resistor divider, every amplifier can operate within the operating maximum of the THS3470 (60V) and enable a $100V_{PP}$ output signal.

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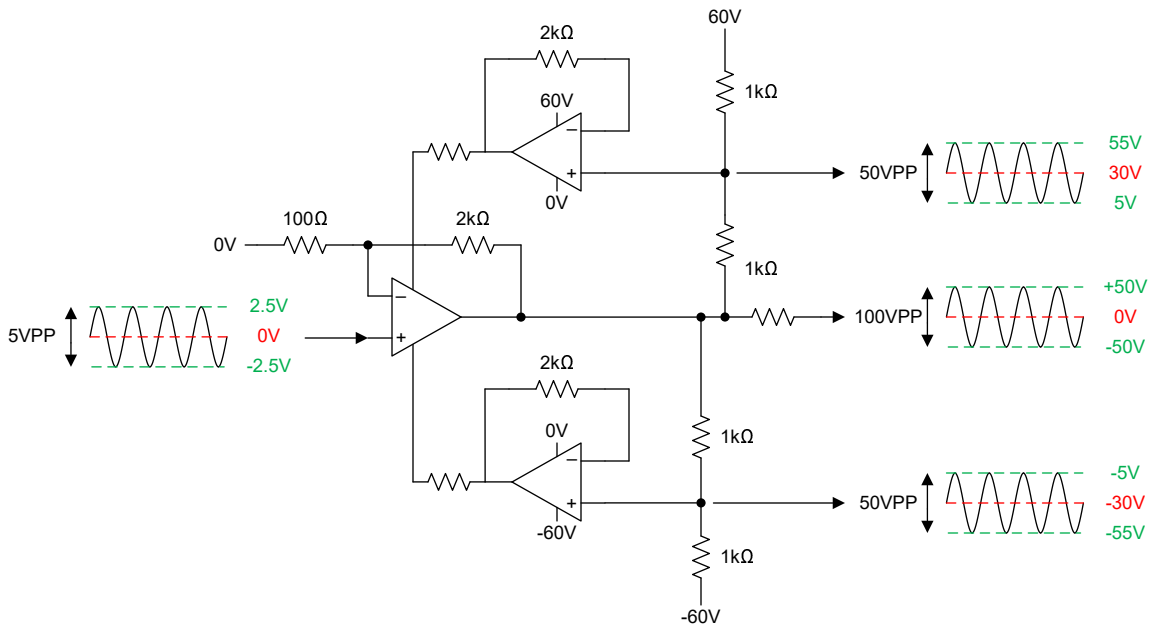


Figure 7-6. 120V Bootstrap Amplifier Example

7.2.2.1 Design Requirements

The goal of this design is to create a 100VPP signal using 3 THS3470 amplifiers in a bootstrap configuration. At a peak voltage of 50V, and with a 100 ohm resistive load, there is a 500mA dc output current delivered out of the signal amplifier. Voltage headroom in this design is limited the DC Output Current (500mA) times the sum of the isolation resistors of the supply and signal amplifiers (4ohms total) plus the output headroom of the signal and supply amplifiers (3V each). Adding these listed elements together, a total voltage headroom loss of 10V to each supply (+-60V) for a total output swing of 100VPP. Using 500mA of the total peak output current limit (2A) for dc allows a total slew rate of 1500V/us into a 1nF capacitive load at 1.5A of ac current. These load specifications were chosen to optimize for the total peak current limit (2A) with a 1nF capacitive and 100ohm resistive load, but can be adjusted accordingly to maximize for differing reactive and passive load combinations.

Table 7-2. Design Parameters

PARAMETER	VALUE
Supply Voltage	+-60V
Output Voltage	100VPP
Slew Rate	1500V/us
Output Load	100Ω + 1nF

7.2.2.2 Detailed Design Procedure

When designing with the THS3470, designers need to keep the total output current from both ac (capacitive) and dc (resistive) loads in mind. The maximum output current allowed for the THS3470 is 1.5A for dc current, but many applications demand an capacitive load drive at the device output (cables, parasitic capacitance, gate capacitance, etc) that can create large ac currents during large dv/dt steps or large signal sinusoid. Since the THS3470 slew rate is so high, 1kV/us in certain bootstrap conditions, special care needs to be given for limiting the ac peak current plus the dc current to 2A as shown in Table 7-3.

Table 7-3. Total Current from AC and DC Loads

Output Voltage (VPP)	Resistive Load (Ω)	DC Current (mA)	Capacitive Load (pF)	Max Slew Rate (V/µs)	AC Peak Current (mA)	AC + DC Peak Current (mA)
±40	Open	0	300	2000	600	600

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Table 7-3. Total Current from AC and DC Loads (continued)

Output Voltage (VPP)	Resistive Load (Ω)	DC Current (mA)	Capacitive Load (pF)	Max Slew Rate (V/µs)	AC Peak Current (mA)	AC + DC Peak Current (mA)
±40	Open	0	1000	2000	2000	2000
±50	Open	0	300	2000	600	600
±50	Open	0	1000	2000	2000	2000
±40	100	±400	300	2000	600	1000
±40	100	±400	1000	1600	1600	2000
±50	100	±500	300	2000	600	1100
±50	100	±500	1000	1500	1500	2000

While the bootstrap design provides some benefits, such as 100V output range with a 60V amplifier, there are some design considerations to understand about the architecture. One of the key drawbacks to this design is that the output headroom limitations are doubled to 6V from each rail due to the supply amplifier and the signal amplifier both being limited to 3V (no load) from the individual supplies. In addition, the output headroom of each amplifier increases as the device is heated up and provides more current from the output. For this reason, the 120V supply loses about 20V of headroom (10V from V_{EE} and 10V from V_{CC}) under heavy load conditions. Designers must pay attention to Figure 5-33 for information about headroom loss, and estimate the worst-case junction temperature of each amplifier for the application.

When driving these heavy loads, designers must pay special attention to the max junction temperature of the device (150C) and keep the device within the safe operating area, as shown in Section 7.5.1.2. A benefit of the bootstrap design, compared to a single 120V amplifier, is that the design splits the power consumed on the die between the signal amplifier and the supply amplifiers as shown in Figure 7-6. A traditional 120V amplifier typically consumes 30W of power in this same scenario, since the 30V of drop must occur on one output stage transistor, whereas the bootstrap design splits the 30W of power between the signal and supply amplifier. Since the THS3470 package can optimistically source 4°C/W, this means the bootstrap can increase the total power consumed from 30W to 60W at an ambient temperate of 25C.

Note

4°C/W for Theta JA performance is a best case high airflow scenario that requires considerable design considerations. For more information about practical thermal performance, see Section 7.5.1.

Note

The thermal pad of the THS3470 is internally connected to VEE on the device. Designers need to create electrical isolation between the different amplifier's thermal pads of the bootstrap design, since the VEE pins are all biased to different voltages. See Section 7.5.1.1 for more information about electrical isolation and thermal performance.

When using the digital features of the THS3470, the DGND of the signal amplifier must be connected to the VEE pin instead of board ground, otherwise the digital blocks of the THS3470 can exceed the supply range of the device while the output signal is moving. Likewise, for the VEE supply amplifier, the DGND range can only operate 7V from the positive supply (0V in this design). Because of this, many of the digital pins (P0, P1, $\overline{\text{OVTEMP_FLAG}}$, $\overline{\text{ISNK_FLAG}}$, $\overline{\text{ISRC_FLAG}}$, $\overline{\text{ISNK_LIMIT_EN}}$, $\overline{\text{ISRC_LIMIT_EN}}$) for the THS3470 must be connected with respect to DGND and VDD to prevent device damage. Reading the status of a flag for the signal amplifier during fast transients requires level shifting circuits (difference amplifier), so designers can use the device flags on the supply amplifiers with current limits disabled to limit the complexity of the circuit.

To set a current limit with the bootstrap circuit, set the signal amplifier current limit to the desired value, using a resistor to connect ISRC_LIMIT to V_{EE} and ISNK_LIMIT to V_{CC}, and leave the supply amplifier current limits at the maximum (1.35A DC). If the supply amplifiers enter into current limit before the signal amplifier, the signal

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amplifier can experience damage. The IOUT_MONITOR pin is not suggested to be used on the signal amplifier, because the VMID voltage is moving with the output voltage. IOUT_MONITOR can be monitored on the supply amplifiers if current monitoring is desired on the bootstrap design.

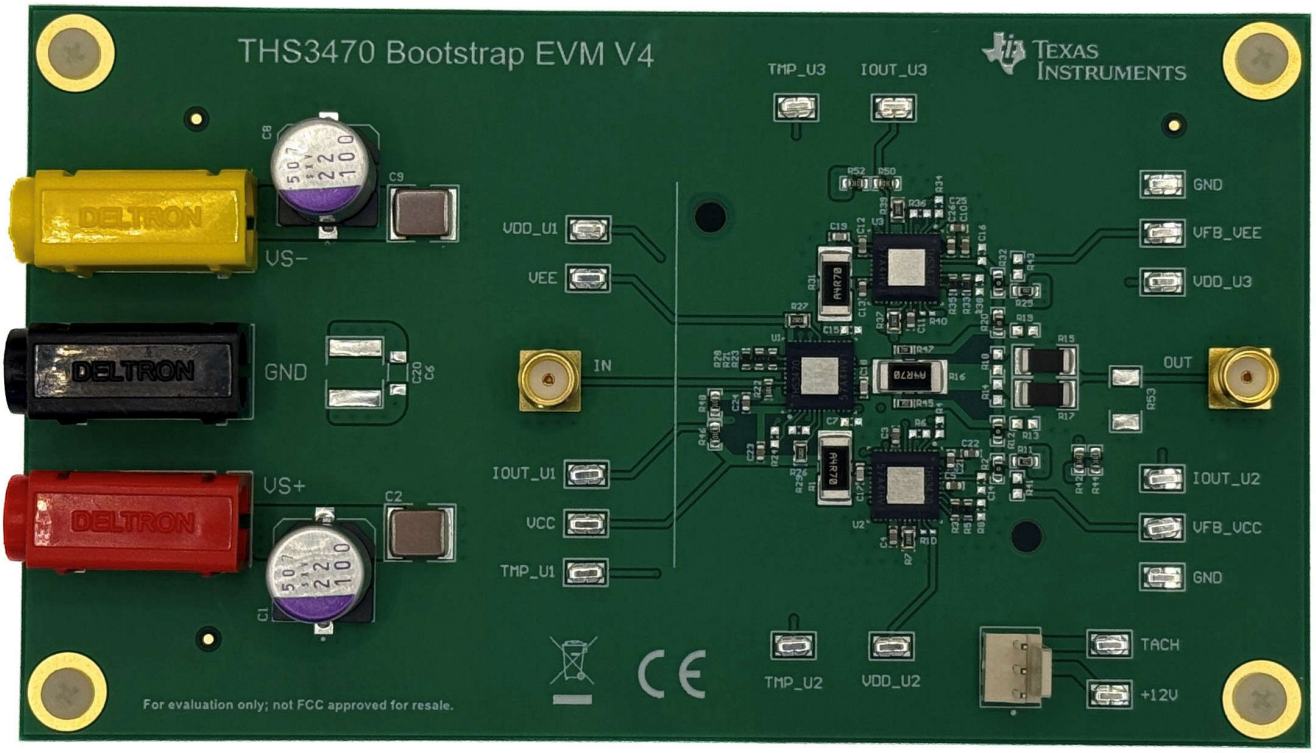


Figure 7-7. THS3470 Bootstrap PCB

7.2.2.3 Application Performance Plots

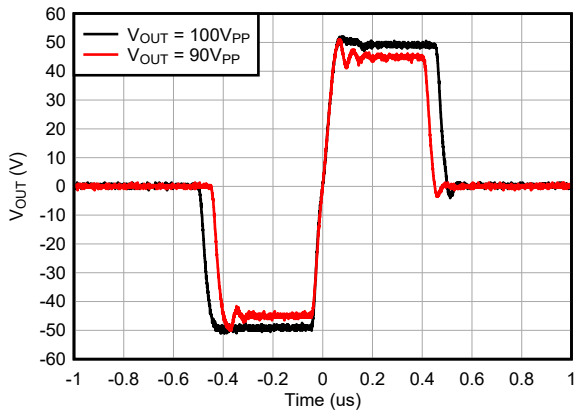


Figure 7-8. THS3470 Bootstrap Step Response (V_{OUT} = 1kV/µs, R_L = 100Ω, C_L = 1nF)

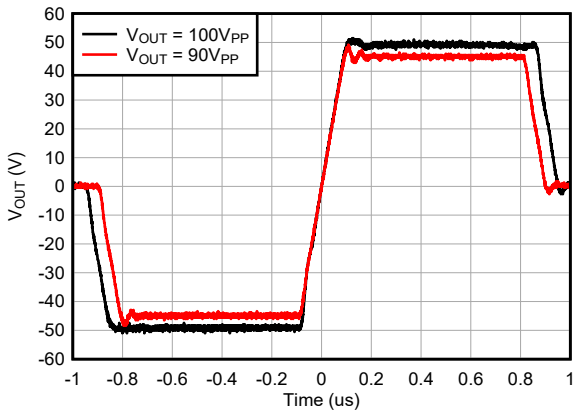


Figure 7-9. THS3470 Bootstrap Step Response (V_{OUT} = 500V/µs, R_L = 100Ω, C_L = 1nF)

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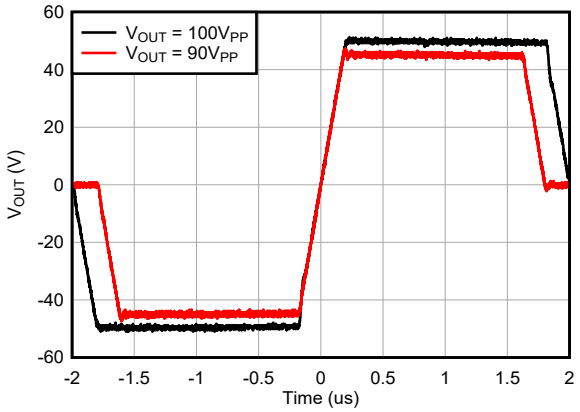


Figure 7-10. THS3470 Bootstrap Step Response (V_{OUT} = 250V/µs, R_L = 100Ω, C_L = 1nF)

7.3 Short Circuit Protection

Many applications that the THS3470 is used with are often concerned with transient short conditions to either ground or the supplies. In systems with multiple THS3470s, "pin to pin" short scenarios can also develop when cables or PCB fixtures fail which inevitably short the output of one THS3470 to another THS3470. For this reason, all of the THS3470 parameters in the data-sheet are measured with a 5Ω isolation resistor. While this 5Ω resistor can limit the performance of the device in certain scenarios, specifically output headroom under load current and total system bandwidth, the protection benefits are highlighted below.

Note

The output isolation resistor on the THS3470 can be reduced from 5 ohms in applications where short to ground is not a concern. Even in applications where short-to-ground scenarios are unlikely, leave at least 1 ohm of isolation resistance as a safe guard against unforeseen output conditions.

CAUTION

The THS3470 can survive short to V_{CC}, V_{EE}, and "pin to pin" short conditions, but only within the boundaries of the safe operating area. Failure to observe the limitations outlined in Section 7.5.1.2 can result in destructive failures for the THS3470.

To test the performance of the THS3470 during short to ground scenarios, the test setup in Figure 7-11 was used. Using this setup, a function generator is set up for 10,000 cycles at 1%, 5%, and 10% duty cycles with 1 to 100ms on pulse-widths. These test are conducted on the bench, with a limited sample size, and designers need to confirm this performance in the actual application to verify device health.

Note

Make sure to monitor the DIE_TEMP pin and keep the junction temperature below 150C. Additionally, pulsing the output at lower pulse widths, or different duty cycles, can change the safe operating area of the device. See Section 7.5.1.2 for more details about transient safe operating area performance.

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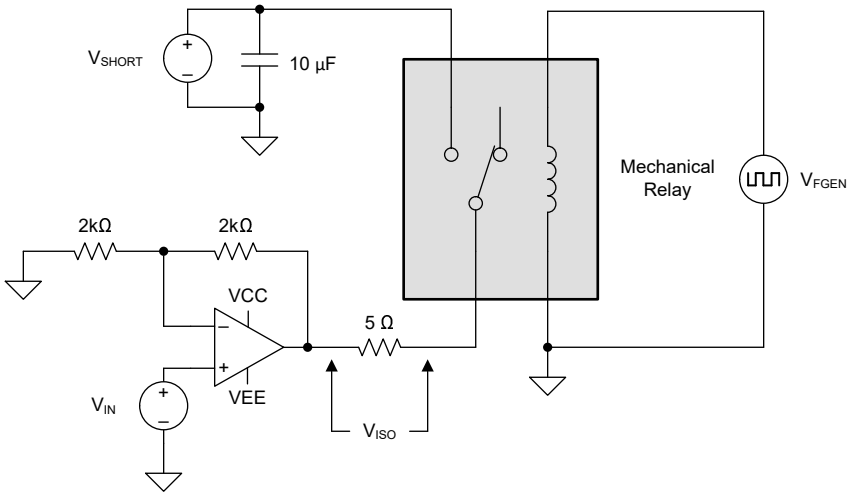


Figure 7-11. THS3470 Short To Ground Test Setup

As shown in Figure 7-11, a high current mechanical relay is selected to simulate quick transient fault conditions. Mechanical relays are well suited for simulating rapid fault conditions since the relay contact is a mechanical latch that can cause a near instantaneous inrush current to the device. Solid state relays, in contrast, provide a slow increase in the resistance as the channel closes, thus providing a gradual increase in current that does not emulate a real world fault scenario. In addition, Figure 7-12 shows that the THS3470 is shorted for much more than just 10,000 cycles, since mechanical relays exhibit "bouncing" when "hot switched". These bounces can vary from 2 to 6 cycles when closing the relay, resulting in somewhere between 20,000 to 60,000 cycles for the conducted test.

Figure 7-13 shows the output current and voltage during one of the transient short conditions. If designers are looking to replicate these results, make sure the oscilloscope time scale is minimized to properly quantize the current and voltage spikes of the waveform. Designers need to choose high frequency (>5GHz) oscilloscope probes and oscilloscopes to make sure the output spikes are not filtered by the signal chain.

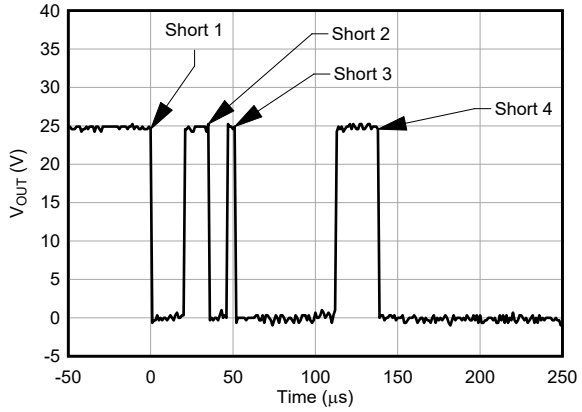


Figure 7-12. THS3470 practical shorting (with mechanical relay bounce)

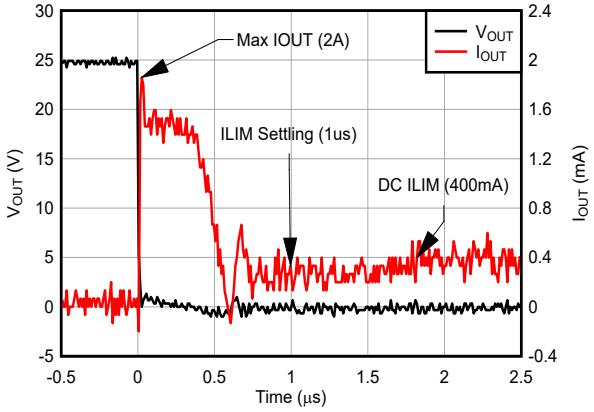


Figure 7-13. THS3470 Output Current and Voltage during mechanical shorting

7.4 Power Supply Recommendations

The THS3470 is designed to operate on power supplies ranging from ±6V to ±30V (single-ended supplies of 12V to 60V). Use a power-supply accuracy of 5% or better. Power supplies must be designed for the expected maximum output current from VOUT for both resistive and capacitive loads. The THS3470 current limit circuitry does not limit the current for rapid transient currents, so adequate bypass capacitance on the VCC and VEE pins is mandatory. Place a 22µF tantalum or electrolytic capacitor and a 10µF X7R capacitor near the supply sources for V_{CC} and V_{EE} to provide bulk decoupling. VCC (pins 8–10, 25–27, 38–39), VEE (pins 15, 20, 29, 36, 41), VMID (pins 1–2), and VDD (pin 32) pins all require 100nF C0G or NP0 capacitors per pin grouping as shown in Section 7.5.3. Place the 100nF C0G or NP0 capacitors as close as possible to the THS3470 pins. In addition, shorten the current return path of the bypass capacitor ground connections as much as possible to minimize loop inductance. Ensure that all capacitors are rated for the correct voltages.

7.5 Layout

7.5.1 Thermal Considerations

7.5.1.1 Top-Side Cooling Benefits

The THS3470 comes in a top-side cooled REB package which gives thermal performance benefits over traditional bottom-side cooled QFN devices. Traditional packages, as shown in Figure 7-14, must interface with the PCB material before entering the heat sink. Without a heat sink, bottom-side cooled devices rely on convection across a smaller surface area of the PCB to remove heat. A helpful conceptualization in these circumstances is to think about the different interfaces as “thermal resistances” that prevent the heat generated by the silicon die from moving to the ambient air. The result of these bottom-side cooled packages often results in a best-case θ_{JA} of above 10°C/W for the total system level performance, even with a forced air system.

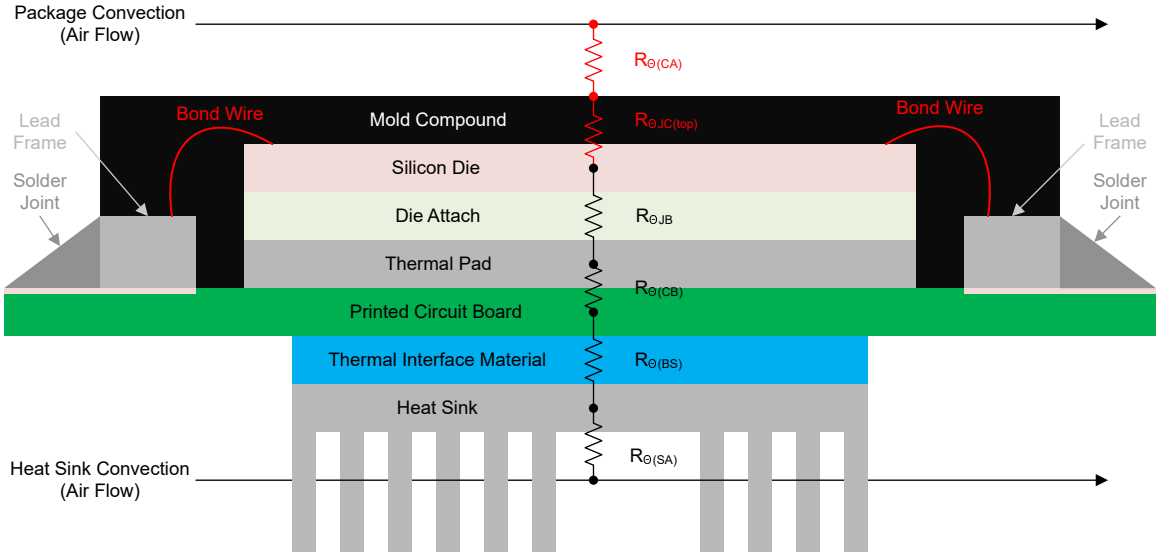


Figure 7-14. Typical Bottom-Side Cooling Example

The THS3470 top-side cooled package, however, does not rely on heat to travel through the PCB before interfacing with the air or heat sink. This more direct contact method essentially removes the PCB “thermal resistance”, as shown in Figure 7-15, and can enable a full system level θ_{JA} performance of approximately 4°C/W. This configuration also enables the potential use of a cold plate or other direct contact methods of cooling that have better mechanisms for removing heat from the system.

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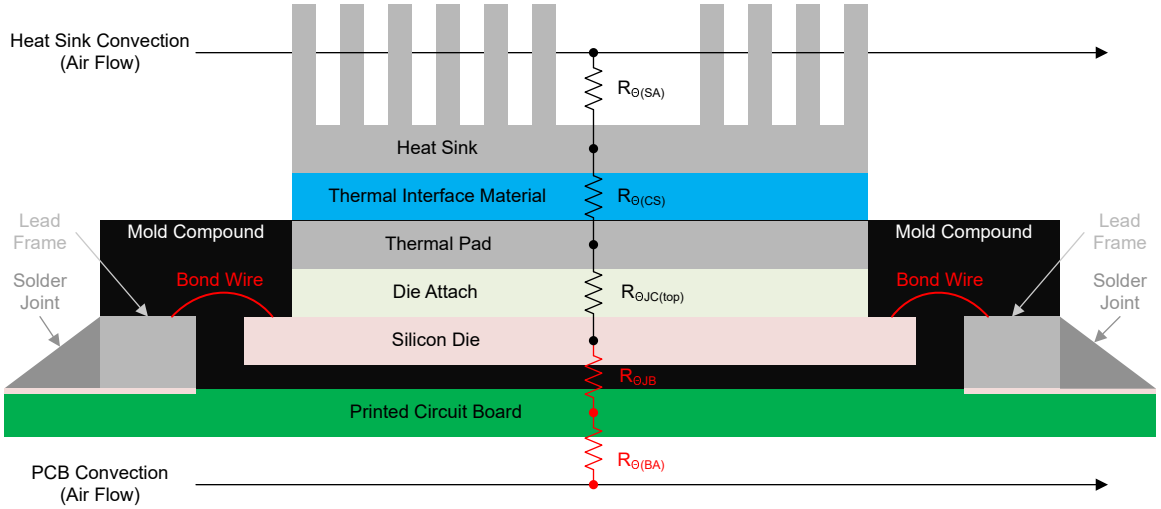


Figure 7-15. THS3470 Top-Side Cooling Example

Note

For air cooled systems, achieving 4°C/W is typically dependent on the "Linear Airflow Velocity" along the fins of the heat sink, typically measured in meters per second (m/s) or linear feet per minute (LFM). Air flow velocities of 1m/s or greater is typically required to achieve 4°C/W θ_{JA} performance.

Due to the high voltage nature of the THS3470, mechanically mounting the heat-sink can require special considerations depending on the application. To provide the best thermal performance possible, the THS3470 uses a conductive die attach that internally connects the thermal pad to VEE. In single ended applications where VEE is connected to −60V and VCC is connected to 0V, the high voltage potential on the thermal pad creates the possibility of a high voltage hazard for the system. To circumvent potential high voltage hazards, a non-conductive thermal interface material can be placed in between a copper or graphite heat spreader and the heat sink as shown in Figure 7-16. The copper heat spreader helps to distribute the heat to a wider surface area before the thermal interface, resulting in a lower overall thermal resistance. Additionally, using an anodized heat sink can help to provide electrical isolation while not degrading the thermal performance significantly. Designers need to keep in mind that anodization on heat sinks can become scratched or damaged, so using a thermal interface material is preferable for situations where the heat-sink has to be regularly removed from the device. Lastly, use alumina or ceramic screws to mechanically secure the fixture while maintaining electrical isolation between the heat spreader and heat sink.

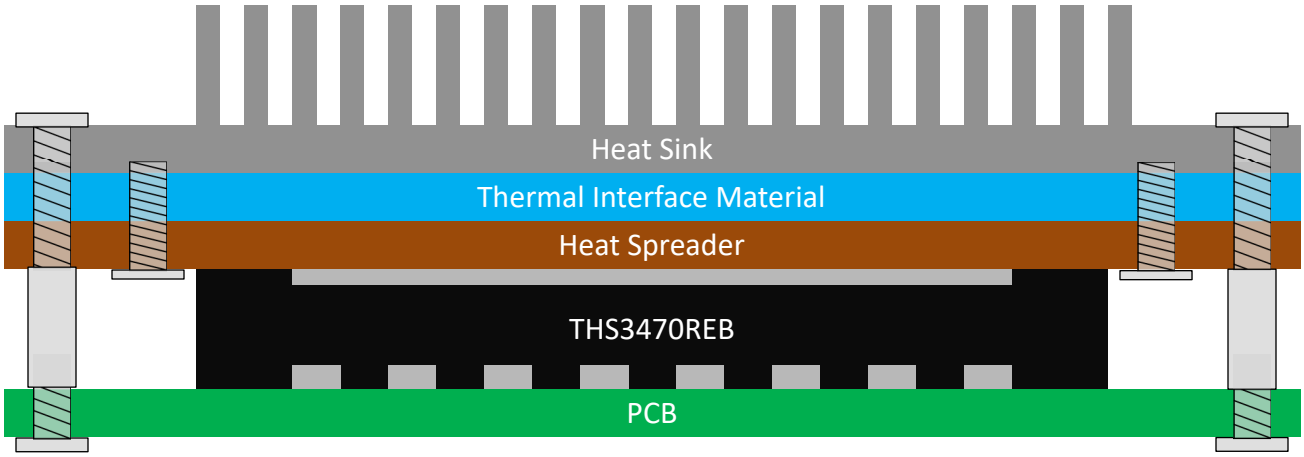


Figure 7-16. Electrical Isolation in Top-Side Cooling Example

7.5.1.2 THS3470 Safe Operating Area

The Safe Operating Area of a device helps designers to identify best practices for managing inherent power limitations of semiconductor devices. For operational amplifiers, these limitations typically manifest through large output currents paired with large voltage drop across the output transistors. The high voltage and high current nature of the THS3470 inherently dissipates more power inside the package, thus special design considerations must be taken to optimize device health over lifetime. For more information regarding sources of stress for power amplifiers with regards to the Safe Operating Area, see SBOA022.

The THS3470 is equipped with a top-side cooled REB package, which helps to optimize thermal performance when burning large amounts of power inside the package. For DC, or near DC performance (i.e. high duty cycle and/or >100ms pulses), power burned in the output stage causes the device to heat up at a near worst-case scenario. While the THS3470 does include diagnostic and protection features such as the DIE_TEMP and OVERTEMP_FLAG to help with thermal management, best practice for enabling device integrity includes planning for the safe operating area of the device.

Figure 7-17 shows how the THS3470 functions at different output voltages and output currents under different cooling conditions. These results showcase the necessity of a heat sink in most applications, with a nearly 2x improvement in power delivered by adding the heat sink. Additionally, the convection across the heat sink fins is the primary mechanism for removing the heat from the die. Figure 7-17 shows 3 scenarios that highlight air flow and heat sink impact: no heat sink, heat sink without air flow (THS3470EVM without fan), and heat sink with air flow (THS3470EVM with fan).

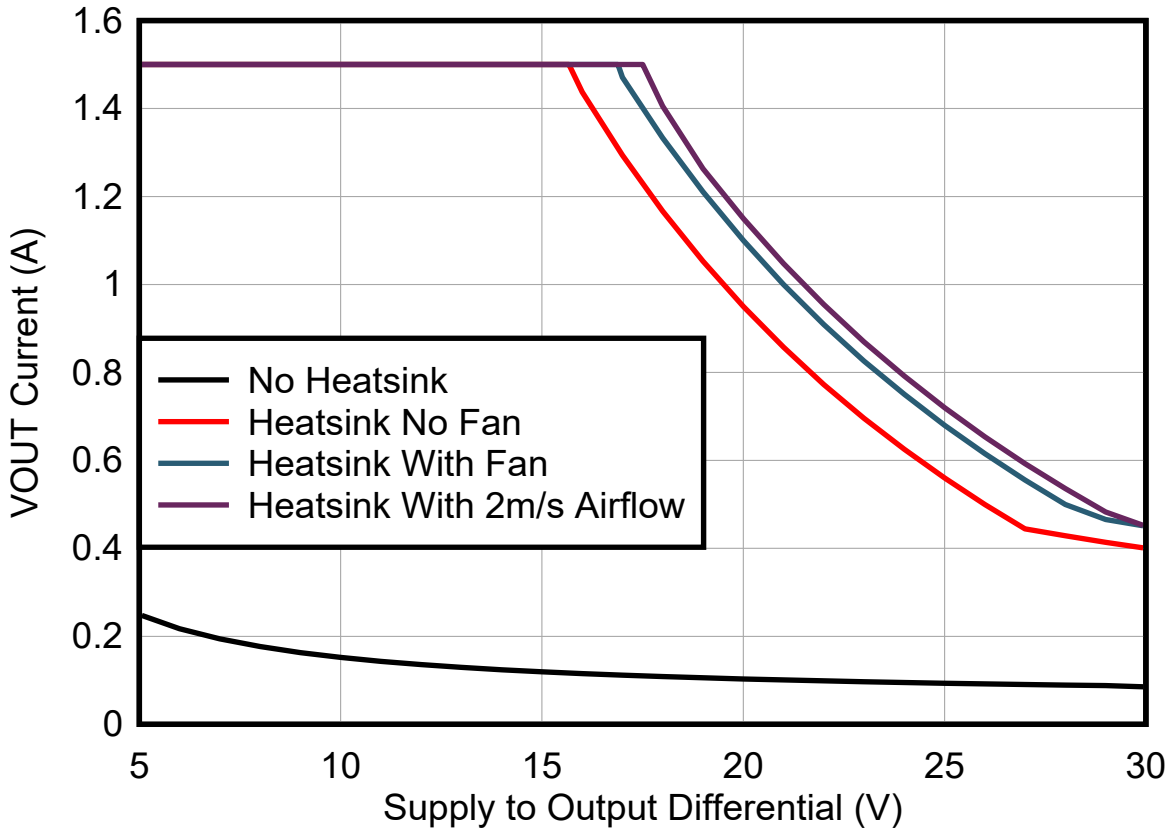


Figure 7-17. THS3470 DC Safe Operating Area (THS3470EVM, V_S = 60V)

Note

Thermal performance of the THS3470 is only shown at the worst case (60V) for the device. Using the device at lower supply voltage reduces the power consumed in the package and results in better thermal performance.

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In addition to dc operation, the THS3470's high slew rate and bandwidth make the device well suited for large voltage pulses. Many applications for the THS3470 use low duty cycle pulses to minimize power dissipated in the system, instead of using a continuous dc voltage, which is often characterized by an "IV Chart". Figure 7-18 shows how the thermal performance of the THS3470 changes under various pulse durations and duty cycles with a purely resistive load while using the THS3470EVM, heat sink, and fan.

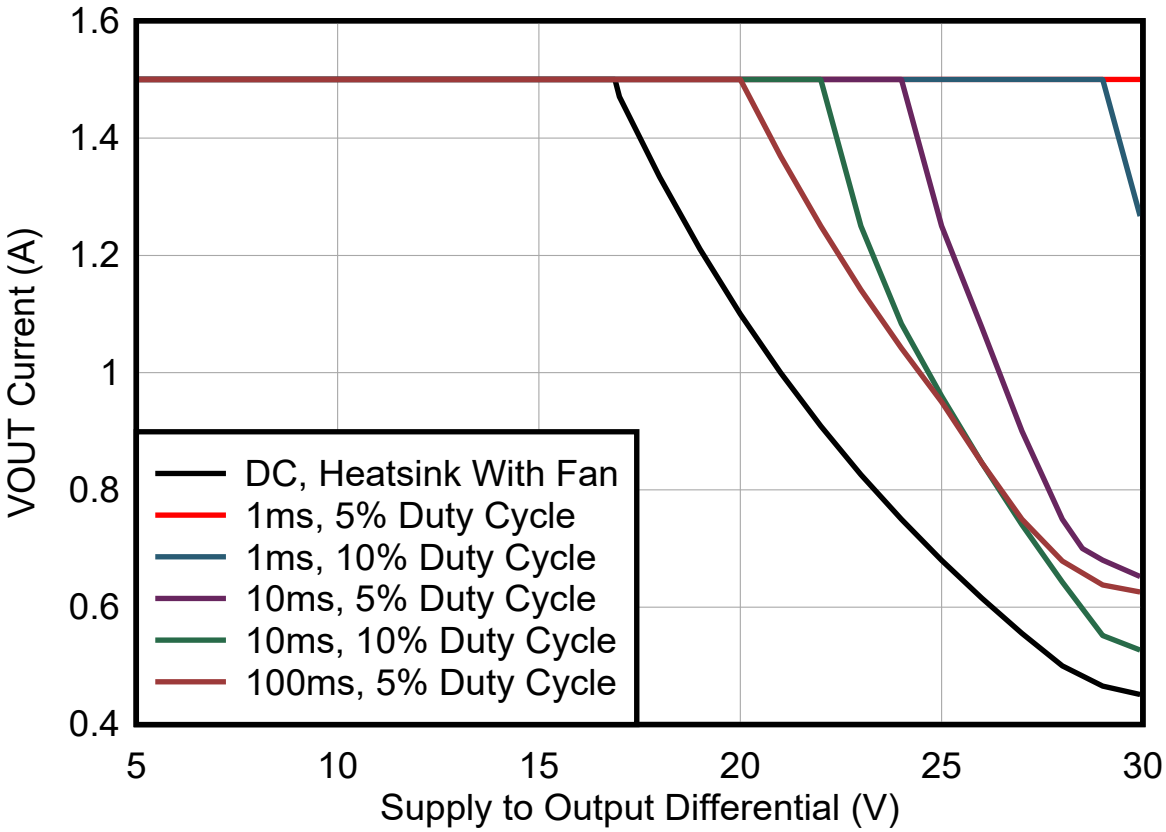


Figure 7-18. THS3470 Safe Operating Area (Square Wave, V_S = 60V)

When driving capacitive loads, Figure 7-19 shows how the THS3470 power consumption changes versus frequency for a square wave with a fixed capacitive load. Since the current into a capacitor is directly correlated to the dv/dt of the output step multiplied by the capacitance, all of the power consumption occurs during the slew event of the square wave. Higher frequencies contain more edges within the same time span, so the THS3470 consumes more power and generates more heat as the frequency increases while driving capacitive loads. The effect of different capacitive loads for a fixed voltage can also be seen in Figure 7-20.

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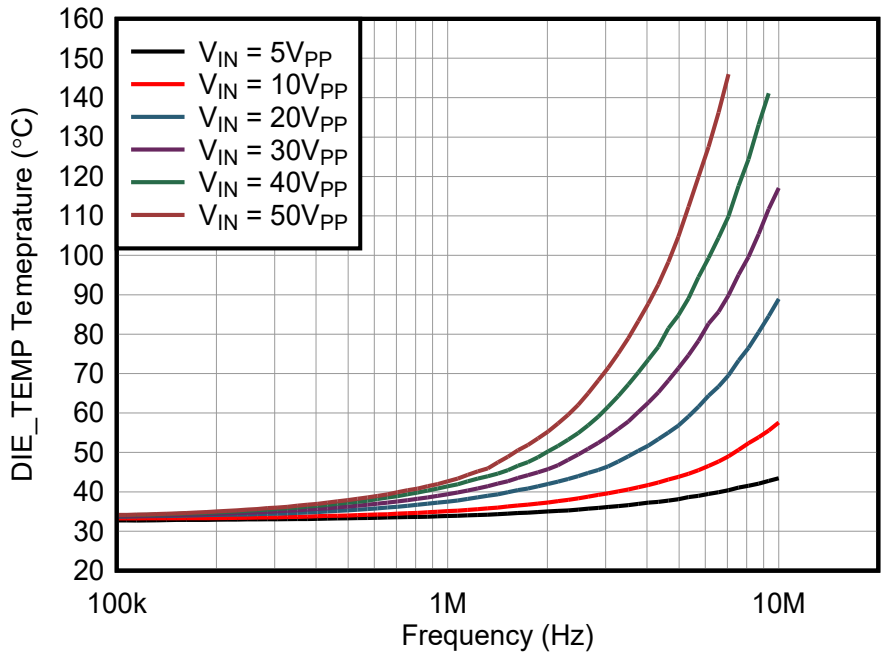


Figure 7-19. THS3470 Safe Operating Area (Square Wave, C_L = 1nF, V_S = 60V)

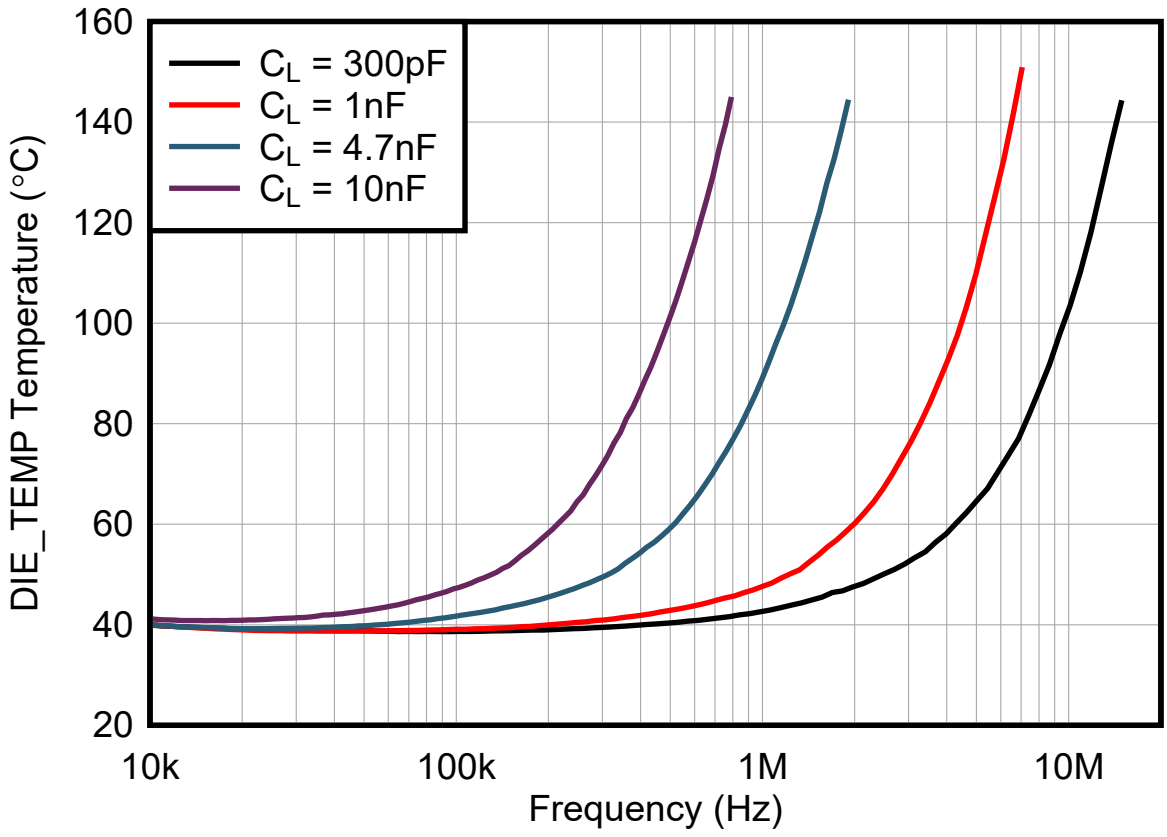


Figure 7-20. THS3470 Safe Operating Area (Square Wave, V_{OUT} = 50V_{PP}, V_S = 60V)

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Note

The input slew rate is configured to limit the peak current to 2A for various capacitive loads in Figure 7-20.

7.5.2 Layout Guidelines

- Use individual power planes for VCC, VEE, and ground nets on the PCB. While not required, creating individual layers with minimal cutouts or traces for the power supplies and ground, as shown in Section 7.5.3, minimizes inductance and provides a large PCB area for current to flow.
- Size traces and vias for VCC, VEE, and VOUT appropriately for the amount of continuous current required for the application. Limit board temperature rise based on IPC-2221 guidelines and PCB manufacturer recommendations. Increase copper weight on layers and use external layers where possible to optimize board space.
- Place a 22µF tantalum or electrolytic capacitor along with a 10µF X7R capacitor close to the VCC and VEE supply sources. In addition, place 100nF capacitors as close to the THS3470 supply pins as possible. Minimize loop inductance for current return paths on the bypass capacitors by placing multiple vias close to the pads of the capacitor.
- VMID requires 100nF C0G or NP0 bypass capacitors from VMID to VCC and VMID to VEE. Place these capacitors as close to pin 1 as possible, with vias to the VCC, VEE, and ground planes as close as possible to the capacitor pad.
- Place 2.2nF capacitors on the VDD, ISRC_LIMIT_EN, ISNK_LIMIT_EN, P0, and P1 between the pin and DGND. Place these capacitors close to the THS3470, but not at the expense of proximity for other components.
- Place plane cutouts underneath any traces or connections on the COMP or IN− pins to reduce parasitic capacitance.
- Place the isolation resistor for VOUT as close to the pin as possible to isolate parasitic capacitance.
- Place components connected to the IN− and FB pins as close to the pin as possible. These nodes are sensitive to parasitic capacitance and can cause oscillations if special care is not taken.
- Place the termination resistor as close to the input of interest as possible. Add multiple vias on the ground connection of the termination resistor to provide a clean current return path and minimize inductance.

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7.5.3 Layout Example

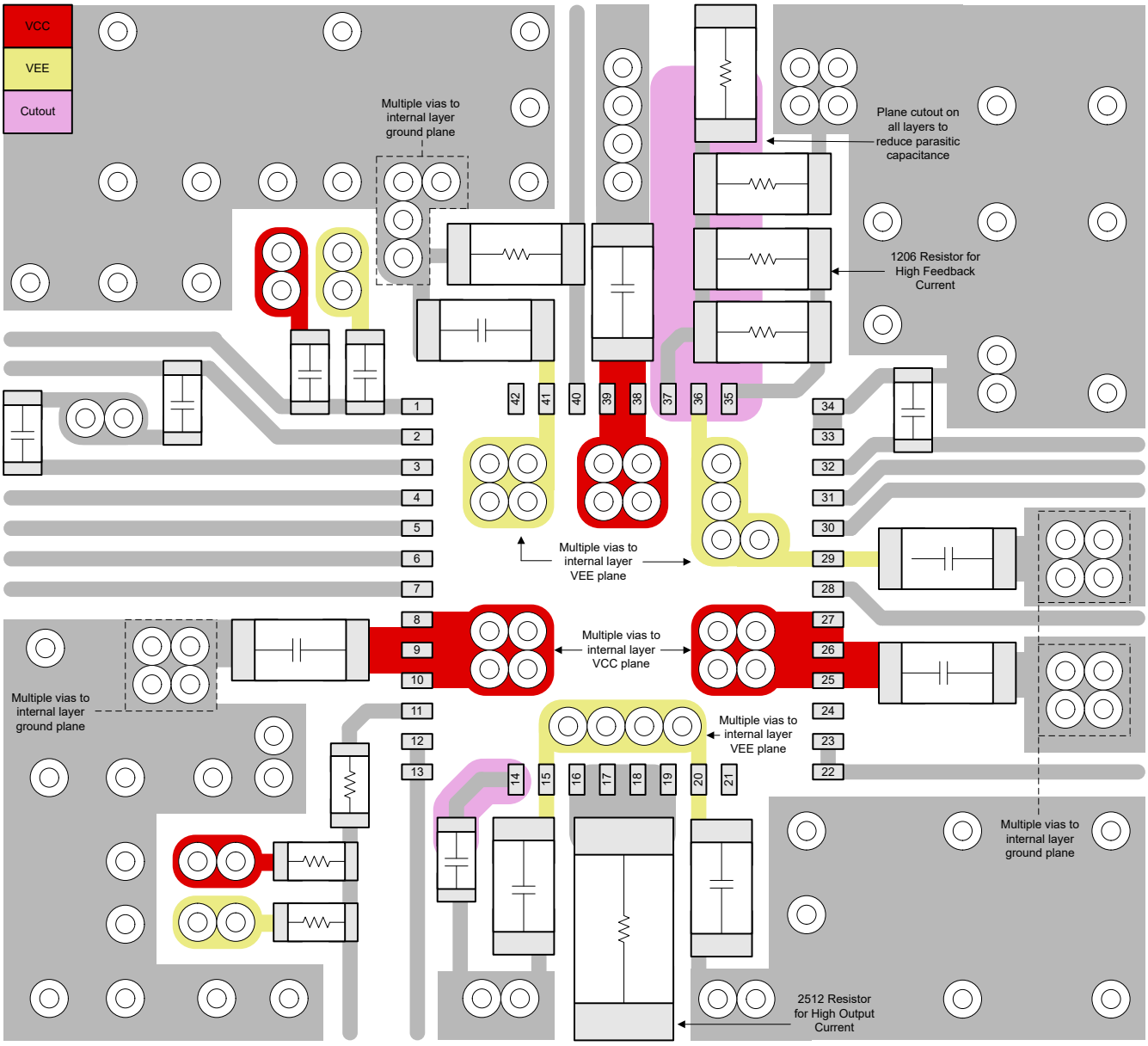


Figure 7-21. THS3470 Layout Example

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2025) to Revision A (October 2025)	Page
• Updated device status to Production Data	1

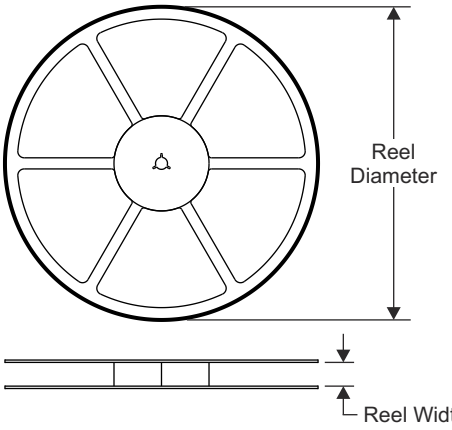
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

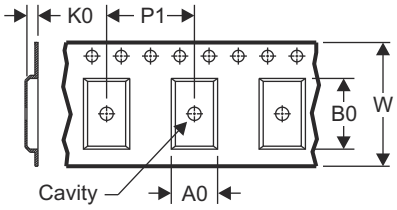
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10.1 TAPE AND REEL INFORMATION

REEL DIMENSIONS

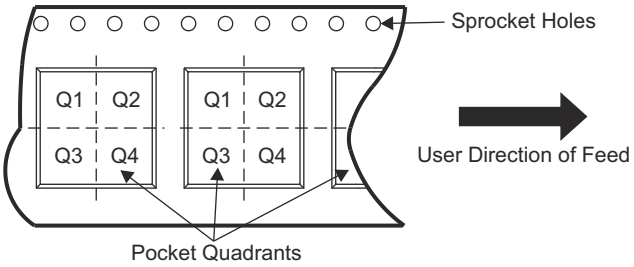


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

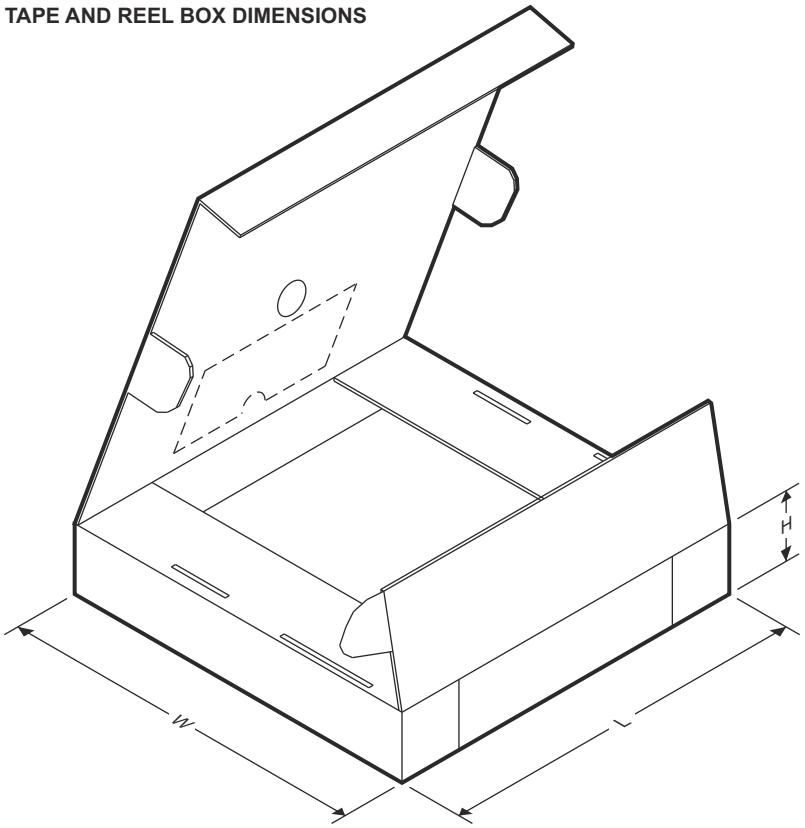
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3470	VQFN	REB	42	3000	330	16.4	7.3	7.3	1.1	12.0	16.0	Q2

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3470	VQFN	REB	42	3000	367.0	367.0	38.0

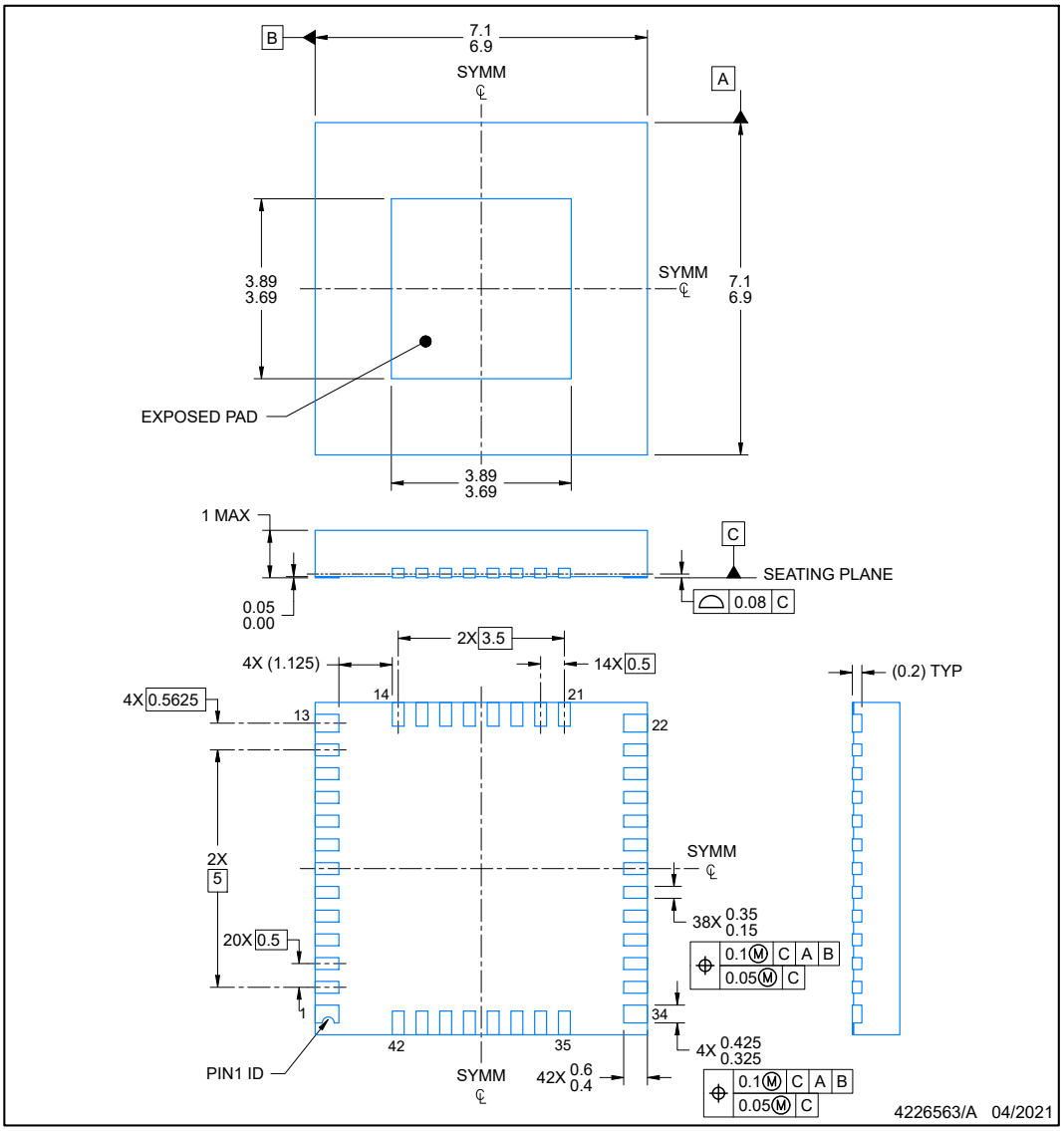
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PACKAGE OUTLINE

REB0042A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package incorporates an exposed thermal pad that is designed to be attached directly to an external heat sink. This optimizes the heat transfer from the integrated circuit (IC).

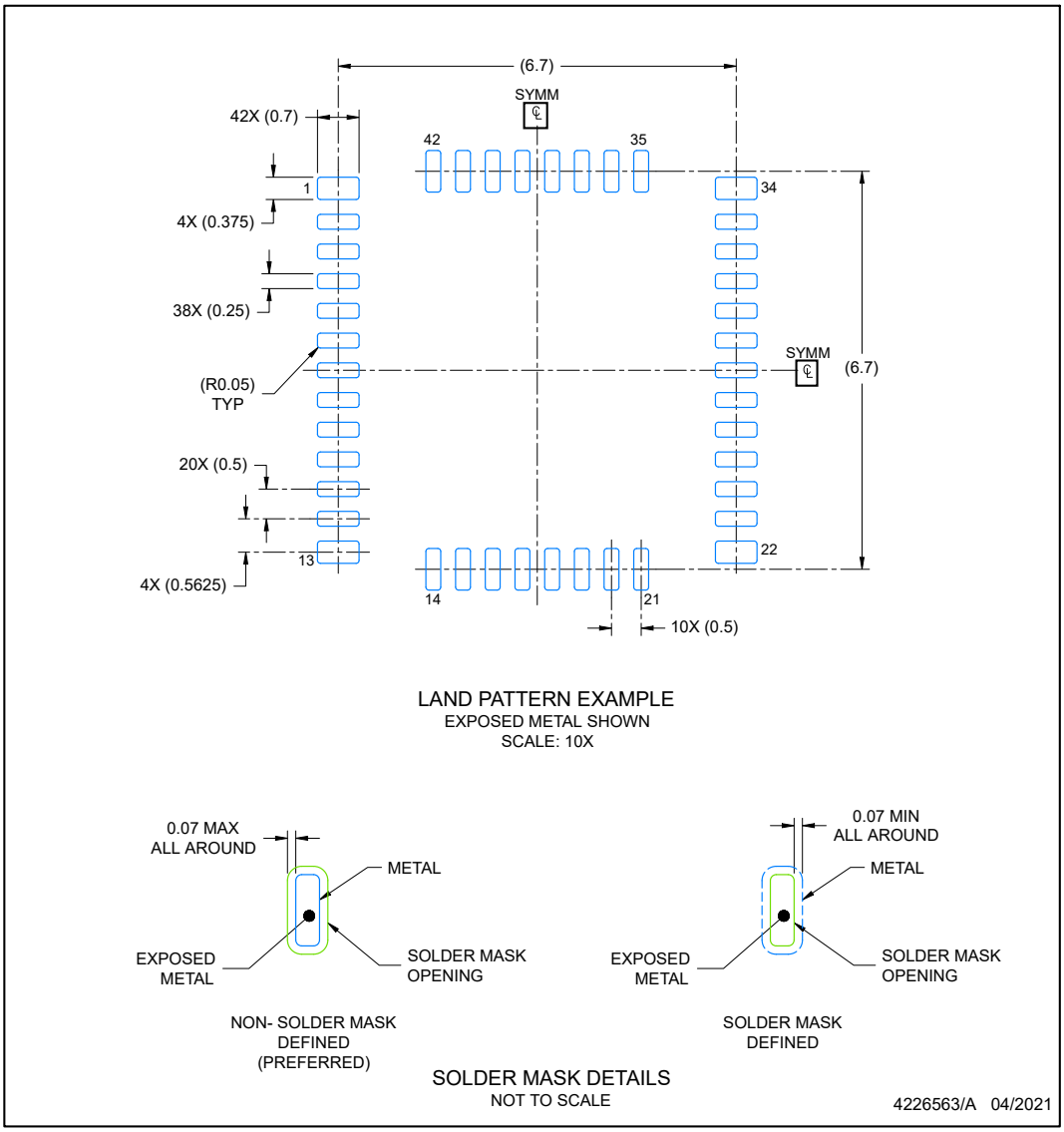
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EXAMPLE BOARD LAYOUT

REB0042A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

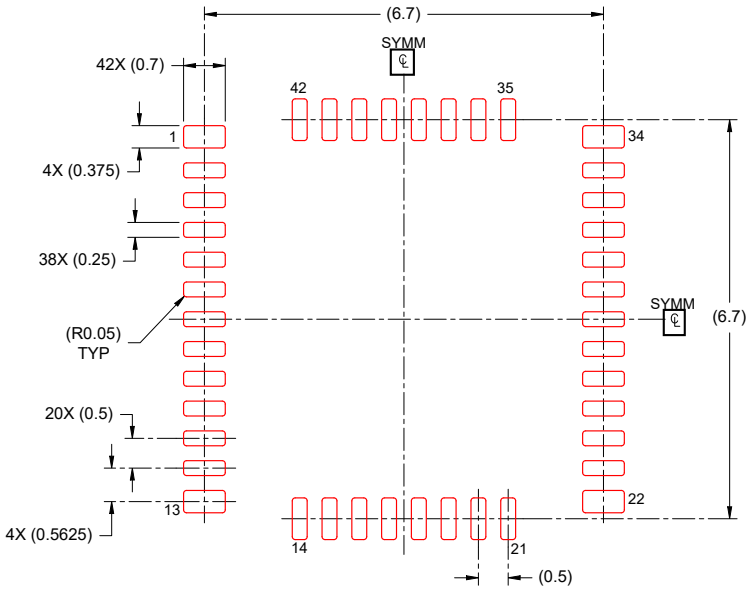
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. For best BLR performance please use non solder mask defined pads.

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EXAMPLE STENCIL DESIGN

REB0042A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS3470REBR	Active	Production	VQFN (REB) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	THS3470
THS3470REBT	Active	Production	VQFN (REB) | 42	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	THS3470

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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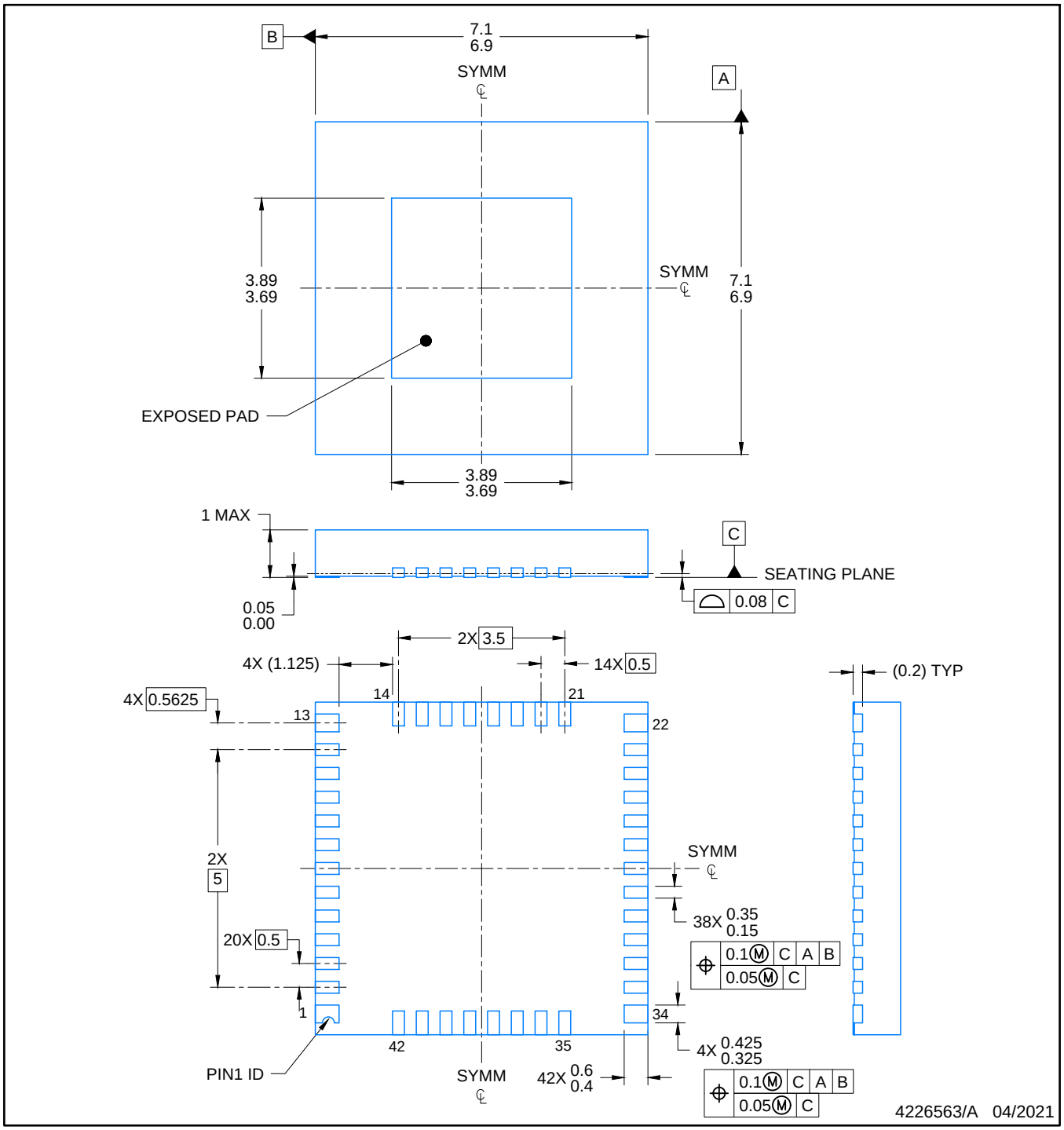
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

REB0042A

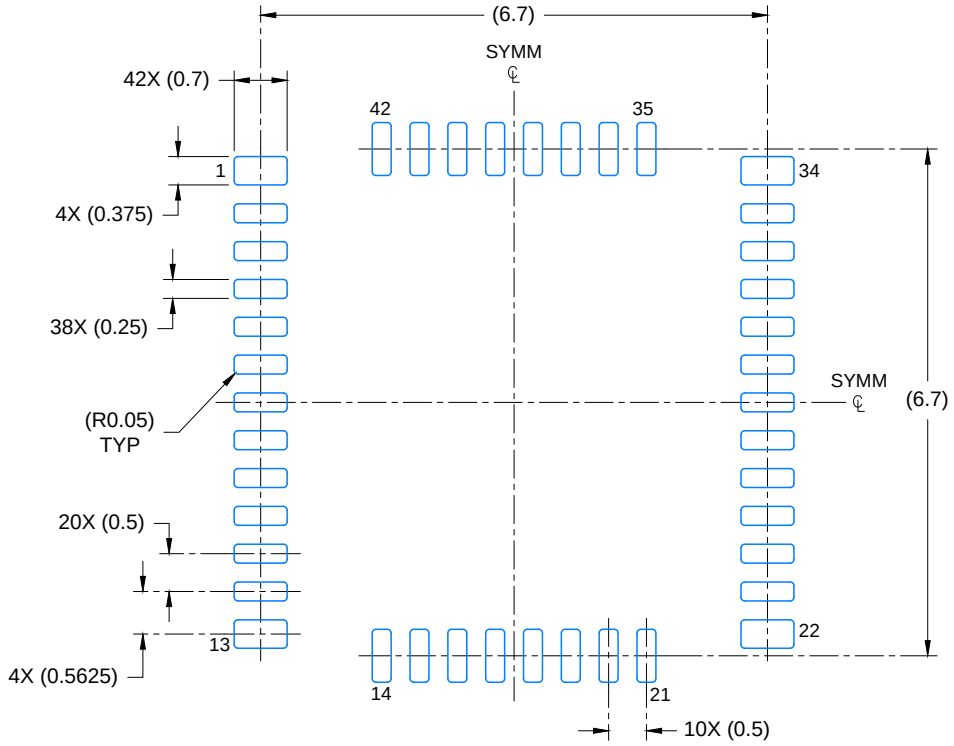
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

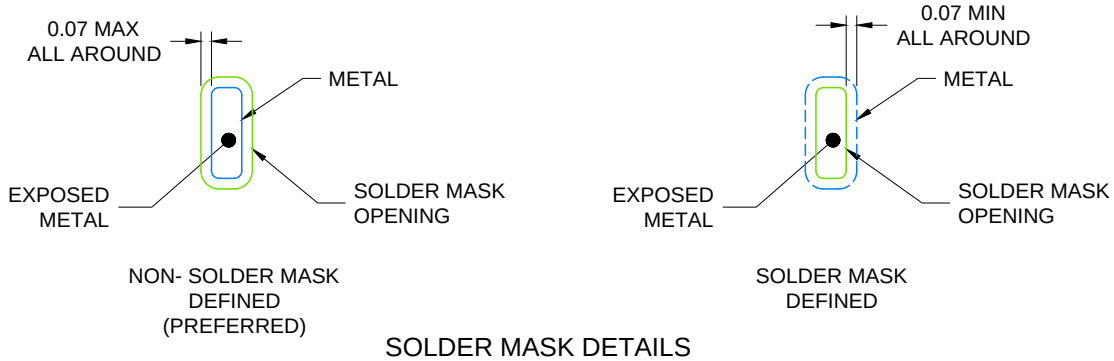


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package incorporates an exposed thermal pad that is designed to be attached directly to an external heat sink. This optimizes the heat transfer from the integrated circuit (IC).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

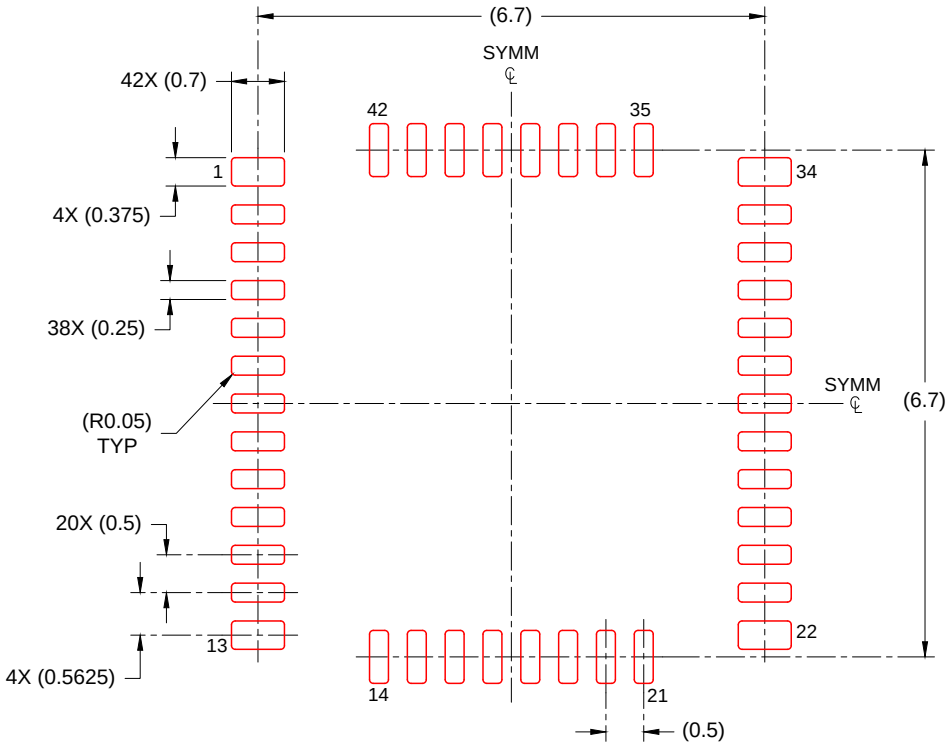


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. For best BLR performance please use non solder mask defined pads.



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025