

# TCAN943-Q1 Automotive CAN FD Transceiver With Sleep Mode

## 1 Features

- AEC Q100 Qualified for automotive applications
- [Functional Safety-Capable](#)
  - [Documentation available to aid in functional safety system design](#)
- Meets the requirements of ISO 11898-2:2024
- Wide input operational voltage range
- Supports classic CAN and CAN FD up to 5Mbps
- $V_{IO}$  level shifting supports: 3.3V to 5.5V
- Operating modes:
  - Normal mode
  - Silent mode
  - Standby mode
  - Low-power sleep mode
- High-voltage INH output for system power control
- Local wake-up support using the WAKE pin
- Defined behavior when unpowered
  - Bus and IO terminals are high impedance (no load to operating bus or application)
- Protection features:
  - $\pm 40V$  CAN bus fault tolerant
  - Load dump support on  $V_{SUP}$
  - IEC ESD protection
  - Under-voltage protection
  - Thermal shutdown protection
  - TXD dominant state timeout (TXD DTO)
- Available in 14-pin leaded (SOT and SOIC) packages and leadless (VSON) package with wettable flanks for improved automated optical inspection (AOI) capability

## 2 Applications

- [Body electronics and lighting](#)
- [Automotive gateway](#)
- [Advanced driver assistance systems \(ADAS\)](#)
- [Infotainment and cluster](#)
- [Hybrid, electric & powertrain systems](#)
- [Personal transport vehicles - electric bike](#)
- [Industrial transportation](#)

## 3 Description

The TCAN943-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 high-speed CAN specification. The device supports both classical CAN and CAN FD data rates up to 5 megabits per second (Mbps).

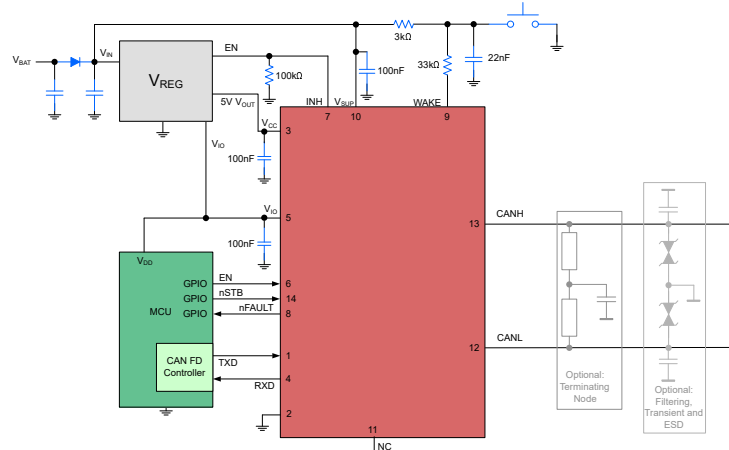
The TCAN943-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that can be present on a system via the INH output pin. This allows a low-current sleep state in which power is gated to all system components except for the TCAN943-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN943-Q1 initiates system start-up by driving INH high.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| TCAN943-Q1  | DYY (SOT, 14)          | 4.2mm × 2mm                 |
|             | D (SOIC, 14)           | 8.65mm × 6mm                |
|             | DMT (VSON, 14)         | 4.5mm × 3mm                 |

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Simplified Schematic**

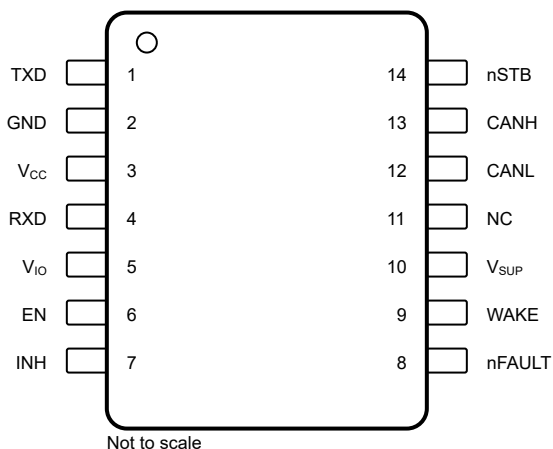


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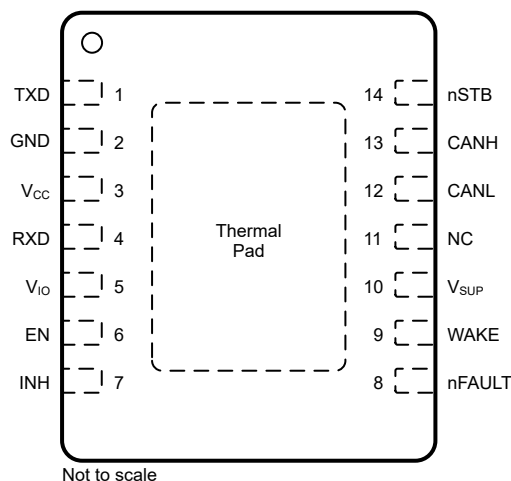
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## 4 Pin Configuration and Functions



**Figure 4-1. D and DYY Packages, 14 Pin (SOIC) and (SOT) (Top View)**



**Figure 4-2. DMT Package, 14 Pin (VSON) (Top View)**

| PINS             |     | TYPE (1) | DESCRIPTION                                                                                |
|------------------|-----|----------|--------------------------------------------------------------------------------------------|
| NAME             | NO. |          |                                                                                            |
| TXD              | 1   | I        | CAN transmit data input, integrated pull-up                                                |
| GND              | 2   | GND      | Ground connection                                                                          |
| V <sub>CC</sub>  | 3   | P        | 5V transceiver supply                                                                      |
| RXD              | 4   | O        | CAN receive data output, tri-state when V <sub>IO</sub> < UV <sub>IO</sub>                 |
| V <sub>IO</sub>  | 5   | P        | I/O supply voltage                                                                         |
| EN               | 6   | I        | Enable input for mode control, integrated pull-down                                        |
| INH              | 7   | O        | Inhibit pin to control system voltage regulators and supplies, high-voltage                |
| nFAULT           | 8   | O        | Fault output, inverted logic                                                               |
| WAKE             | 9   | I        | Local WAKE input terminal, high voltage                                                    |
| V <sub>SUP</sub> | 10  | P        | High-voltage supply from battery                                                           |
| NC               | 11  | NC       | No connect, internally not connected                                                       |
| CANL             | 12  | I/O      | Low-level CAN bus input/output line                                                        |
| CANH             | 13  | I/O      | High-level CAN bus input/output line                                                       |
| nSTB             | 14  | I        | Standby mode control input, integrated pull-down                                           |
| Thermal Pad      | —   |          | Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief |

(1) I = input, O = output, P = power, GND = ground, NC = not connected

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                       |                                                                                           | MIN  | MAX                                           | UNIT |
|-----------------------|-------------------------------------------------------------------------------------------|------|-----------------------------------------------|------|
| V <sub>SUP</sub>      | Supply voltage                                                                            | −0.3 | 40                                            | V    |
| V <sub>CC</sub>       | Supply voltage                                                                            | −0.3 | 6                                             | V    |
| V <sub>IO</sub>       | Supply voltage I/O level shifter                                                          | −0.3 | 6                                             | V    |
| V <sub>BUS</sub>      | CAN bus I/O voltage (CANH, CANL)                                                          | −40  | 40                                            | V    |
| V <sub>DIFF</sub>     | CAN bus differential voltage (V <sub>DIFF</sub> = V <sub>CANH</sub> - V <sub>CANL</sub> ) | −40  | 40                                            | V    |
| V <sub>WAKE</sub>     | WAKE input voltage                                                                        | −40  | 40 and V <sub>I</sub> ≤ V <sub>SUP</sub> +0.3 | V    |
| V <sub>INH</sub>      | INH pin voltage                                                                           | −0.3 | 40 and V <sub>O</sub> ≤ V <sub>SUP</sub> +0.3 | V    |
| V <sub>LOGIC</sub>    | Logic pin voltage                                                                         | −0.3 | 6                                             | V    |
| I <sub>O(LOGIC)</sub> | Logic pin output current                                                                  |      | 8                                             | mA   |
| I <sub>O(INH)</sub>   | Inhibit pin output current                                                                |      | 6                                             | mA   |
| I <sub>O(WAKE)</sub>  | WAKE pin output current                                                                   |      | 3                                             | mA   |
| T <sub>J</sub>        | Junction temperature                                                                      | −40  | 165                                           | °C   |
| T <sub>STG</sub>      | Storage temperature                                                                       | −65  | 150                                           | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

|                  |                         |                                                         |                                                   | VALUE | UNIT |
|------------------|-------------------------|---------------------------------------------------------|---------------------------------------------------|-------|------|
| V <sub>ESD</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> | CANH and CANL with respect to GND                 | ±8000 | V    |
|                  |                         |                                                         | All pins except CANH and CANL with respect to GND | ±2000 | V    |
|                  |                         | Charged device model (CDM), per AEC Q100-011            | All pins                                          | ±500  | V    |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 ESD Ratings - IEC Specifications

|                   |                                                 |                                              |                                                                                           | VALUE  | UNIT |
|-------------------|-------------------------------------------------|----------------------------------------------|-------------------------------------------------------------------------------------------|--------|------|
| V <sub>ESD</sub>  | System level electro-static discharge (ESD)     | CANH, CANL, and V <sub>SUP</sub> to GND      | IEC 62228-3: Unpowered contact discharge <sup>(1)</sup>                                   | ±8000  | V    |
|                   |                                                 | WAKE pin to GND                              |                                                                                           | ±6000  | V    |
| V <sub>ESD</sub>  | Electrostatic discharge                         | CANH and CANL terminal to GND                | SAE J2962-2 per ISO 10605 Powered Contact Discharge <sup>(2)</sup>                        | ±8000  | V    |
|                   |                                                 |                                              | SAE J2962-2 per ISO 10605 Powered Air discharge <sup>(2)</sup>                            | ±15000 | V    |
| V <sub>TRAN</sub> | Transient voltage per ISO-7637-2 <sup>(1)</sup> | CAN, V <sub>SUP</sub> , WAKE terminal to GND | Pulse 1                                                                                   | −100   | V    |
|                   |                                                 |                                              | Pulse 2                                                                                   | +75    | V    |
|                   |                                                 |                                              | Pulse 3a                                                                                  | −150   | V    |
|                   |                                                 |                                              | Pulse 3b                                                                                  | +100   | V    |
|                   | Transient voltage per ISO-7637-3 <sup>(2)</sup> | CAN terminal to GND                          | Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered | ±30    | V    |

- (1) According to IEC 62228-3 Integrated circuits – EMC evaluation of transceivers – Part 3: CAN transceivers.  
(2) According to SAE J2962-2 Communication Transceivers Qualification Requirements – CAN.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|               |                                   | MIN | NOM | MAX | UNIT |
|---------------|-----------------------------------|-----|-----|-----|------|
| $V_{SUP}$     | Supply voltage                    | 4.5 |     | 28  | V    |
| $V_{IO}$      | I/O supply voltage                | 2.9 |     | 5.5 | V    |
| $V_{CC}$      | CAN transceiver supply voltage    | 4.5 |     | 5.5 | V    |
| $I_{OH(DO)}$  | Digital output high-level current | –2  |     |     | mA   |
| $I_{OL(DO)}$  | Digital output low-level current  |     |     | 2   | mA   |
| $I_{O(INH)}$  | Inhibit output current            |     |     | 2   | mA   |
| $T_J$         | Operating junction temperature    | –40 |     | 150 | °C   |
| $T_{SDR}$     | Thermal shutdown                  | 165 |     |     | °C   |
| $T_{SDF}$     | Thermal shutdown release          | 155 |     |     | °C   |
| $T_{SD(HYS)}$ | Thermal shutdown hysteresis       |     | 10  |     | °C   |

## 5.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TCAN943-Q1 |            |           | UNIT |
|-------------------------------|----------------------------------------------|------------|------------|-----------|------|
|                               |                                              | D (SOIC)   | DMT (VSON) | DYY (SOT) |      |
|                               |                                              | 14 PINS    | 14 PINS    | 14 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 87.1       | 39.7       | 91.0      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 41.8       | 41.1       | 41.7      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 43.7       | 15.9       | 25.6      | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 8.5        | 0.9        | 25.4      | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 43.3       | 15.9       | 1.1       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A        | 6.6        | N/A       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.6 Power Dissipation Ratings

| PARAMETER | TEST CONDITIONS                                                                                                                                                                                                                                                                                                                                        | POWER DISSIPATION | UNIT |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------|
| $P_D$     | Average power dissipation<br>$V_{SUP} = 14\text{ V}$ , $V_{CC} = 5\text{ V}$ , $V_{IO} = 5\text{ V}$ , $T_J = 27^\circ\text{C}$ , $R_L = 60\ \Omega$ , $nSTB = 5\text{ V}$ , $EN = 5\text{ V}$ , $C_{L\_RXD} = 15\text{ pF}$ . Typical CAN operating conditions at 500 kbps with 25% transmission (dominant) rate.                                     | 57                | mW   |
|           | Average power dissipation<br>$V_{SUP} = 14\text{ V}$ , $V_{CC} = 5.5\text{ V}$ , $V_{IO} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ , $R_L = 50\ \Omega$ , $nSTB = 5.5\text{ V}$ , $EN = 5.5\text{ V}$ , $C_{L\_RXD} = 15\text{ pF}$ . Typical high load CAN operating conditions at 1 Mbps with 50% transmission (dominant) rate and loaded network. | 151               | mW   |

## 5.7 Power Supply Characteristics

Over recommended operating conditions with  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , unless otherwise noted. All typical values are taken at  $25^{\circ}\text{C}$ ,  $V_{\text{SUP}} = 12\text{V}$ ,  $V_{\text{IO}} = 3.3\text{V}$ ,  $V_{\text{CC}} = 5\text{V}$  and  $R_L = 60\Omega$

| PARAMETER                                         |                                                                       | TEST CONDITIONS                                                                                                                          | MIN | TYP | MAX | UNIT          |
|---------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| <b>Supply Voltage and Current Characteristics</b> |                                                                       |                                                                                                                                          |     |     |     |               |
| $I_{\text{SUP\_NORMAL}}$                          | Supply current<br>CAN active                                          | Normal mode, silent mode, go-to-sleep mode <sup>(1)</sup>                                                                                |     |     | 140 | $\mu\text{A}$ |
| $I_{\text{SUP\_STBY}}$                            | Supply current                                                        | Standby mode, $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$                                                                        |     |     | 60  | $\mu\text{A}$ |
| $I_{\text{SUP\_SLEEP}}$                           | Supply current                                                        | Sleep mode, $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$                                                                          |     | 18  | 30  | $\mu\text{A}$ |
| $UV_{\text{SUP(R)}}$                              | Undervoltage $V_{\text{SUP}}$ threshold rising                        |                                                                                                                                          | 3.9 |     | 4.3 | V             |
| $UV_{\text{SUP(F)}}$                              | Undervoltage $V_{\text{SUP}}$ threshold falling                       |                                                                                                                                          | 3.6 |     | 4.1 | V             |
| $I_{\text{CC\_NORMAL}}$                           | Supply current<br>CAN active: dominant                                | Normal mode<br>$\text{TXD} = 0\text{V}$ , $R_L = 60\Omega$ , $C_L = \text{open}$                                                         |     |     | 70  | mA            |
|                                                   | $V_{\text{CC}}$ supply current normal mode<br>Dominant with bus fault | Normal mode<br>$\text{TXD} = 0\text{V}$ , $R_L = \text{open}$ , $C_L = \text{open}$ , $\text{CANH} = \text{CANL} = \pm 25\text{V}$       |     |     | 130 | mA            |
|                                                   | Supply current<br>CAN active: recessive                               | Normal mode<br>$\text{TXD} = V_{\text{IO}}$ , $R_L = 60\Omega$ , $C_L = \text{open}$                                                     |     |     | 7.5 | mA            |
| $I_{\text{CC\_STBY}}$                             | Supply current, Standby mode                                          | Standby mode $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$<br>$\text{EN} = \text{nSTB} = 0\text{V}$                                |     |     | 3.5 | $\mu\text{A}$ |
| $I_{\text{CC\_SILENT}}$                           | Supply current, Silent mode                                           | Silent and go-to-sleep mode <sup>(1)</sup><br>$\text{TXD} = \text{nSTB} = V_{\text{IO}}$ , $R_L = 60\Omega$ , $C_L = \text{open}$        |     |     | 4   | mA            |
| $I_{\text{CC\_SLEEP}}$                            | Supply current, Sleep mode                                            | Sleep mode $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$<br>$\text{EN} = 0\text{V}$ or $V_{\text{IO}}$ , $\text{nSTB} = 0\text{V}$ |     |     | 3.2 | $\mu\text{A}$ |
| $UV_{\text{CC(R)}}$                               | Undervoltage $V_{\text{CC}}$ threshold rising                         |                                                                                                                                          | 3.9 | 4   | 4.3 | V             |
| $UV_{\text{CC(F)}}$                               | Undervoltage $V_{\text{CC}}$ threshold falling                        |                                                                                                                                          | 3.7 | 3.9 | 4.2 | V             |
| $V_{\text{HYS(UVCC)}}$                            | Hysteresis voltage on $UV_{\text{CC}}$                                |                                                                                                                                          | 50  |     | 300 | mV            |
| $I_{\text{IO\_NORMAL}}$                           | I/O supply current                                                    | Normal mode<br>$\text{RXD}$ floating, $\text{TXD} = 0\text{V}$                                                                           |     |     | 200 | $\mu\text{A}$ |
| $I_{\text{IO\_NORMAL}}$                           | I/O supply current                                                    | Normal mode, silent mode, or go-to-sleep mode <sup>(1)</sup><br>$\text{RXD}$ floating, $\text{TXD} = V_{\text{IO}}$                      |     |     | 3   | $\mu\text{A}$ |
| $I_{\text{IO\_STBY}}$                             | I/O supply current                                                    | Standby mode $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$<br>$\text{RXD}$ floating, $\text{TXD} = V_{\text{IO}}$                  |     |     | 3   | $\mu\text{A}$ |
| $I_{\text{IO\_SLEEP}}$                            | I/O supply current                                                    | Sleep mode $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$<br>$\text{nSTB} = 0\text{V}$                                              |     |     | 2.5 | $\mu\text{A}$ |
| $UV_{\text{IO(R)}}$                               | Under voltage $V_{\text{IO}}$ threshold rising                        | Ramp up                                                                                                                                  | 2.2 | 2.5 | 2.8 | V             |
| $UV_{\text{IO(F)}}$                               | Under voltage $V_{\text{IO}}$ threshold falling                       | Ramp down                                                                                                                                | 2.1 | 2.4 | 2.7 | V             |
| $V_{\text{HYS(UVIO)}}$                            | Hysteresis voltage on $UV_{\text{IO}}$                                |                                                                                                                                          | 40  | 100 | 160 | mV            |

(1) Current consumption in go-to-sleep mode is specified by design

## 5.8 Electrical Characteristics

Over recommended operating conditions with  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , unless otherwise noted. All typical values are taken at  $25^{\circ}\text{C}$ ,  $V_{\text{SUP}} = 12\text{V}$ ,  $V_{\text{IO}} = 3.3\text{V}$ ,  $V_{\text{CC}} = 5\text{V}$  and  $R_L = 60\Omega$

| PARAMETER                                      |                                                                                                              |             | TEST CONDITIONS                                                                                                                                                                                                             | MIN  | TYP | MAX  | UNIT          |
|------------------------------------------------|--------------------------------------------------------------------------------------------------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|------|---------------|
| <b>CAN Driver Characteristics</b>              |                                                                                                              |             |                                                                                                                                                                                                                             |      |     |      |               |
| $V_{\text{CANH(D)}}$                           | Dominant output voltage                                                                                      | CANH        | TXD = 0V, $50\Omega \leq R_L \leq 65\Omega$ , $C_L = \text{open}$ , $R_{\text{CM}} = \text{open}$                                                                                                                           | 2.75 |     | 4.5  | V             |
| $V_{\text{CANL(D)}}$                           | Normal mode                                                                                                  | CANL        |                                                                                                                                                                                                                             | 0.5  |     | 2.25 | V             |
| $V_{\text{CANH(R)}}$<br>$V_{\text{CANL(R)}}$   | Recessive output voltage<br>Normal mode, Silent mode                                                         |             | TXD = $V_{\text{IO}}$ , $R_L = \text{open}$ (no load), $R_{\text{CM}} = \text{open}$                                                                                                                                        | 2    | 2.5 | 3    | V             |
| $V_{\text{SYM}}$                               | Driver symmetry<br>Normal mode<br>$(V_{\text{O(CANH)}} + V_{\text{O(CANL)}}) / V_{\text{CC}}$ <sup>(1)</sup> |             | EN = nSTB = $V_{\text{IO}}$ , $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , $R_L = 60\Omega$ , $C_{\text{SPLIT}} = 4.7\text{nF}$ , $C_L = \text{Open}$ , $R_{\text{CM}} = \text{Open}$ , TXD = 250kHz, 1MHz, 2.5MHz | 0.9  |     | 1.1  | V/V           |
| $V_{\text{SYM\_DC}}$                           | DC Driver symmetry<br>Normal mode<br>$V_{\text{CC}} - V_{\text{O(CANH)}} - V_{\text{O(CANL)}}$               |             | EN = nSTB = $V_{\text{IO}}$ , $R_L = 60\Omega$ , $C_L = \text{open}$                                                                                                                                                        | -300 |     | 300  | mV            |
| $V_{\text{DIFF(D)}}$                           | Differential output voltage<br>Normal mode<br>Dominant                                                       | CANH - CANL | EN = nSTB = $V_{\text{IO}}$ , $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , TXD = 0V, $50\Omega \leq R_L \leq 65\Omega$ , $C_L = \text{open}$                                                                       | 1.5  |     | 3    | V             |
|                                                |                                                                                                              | CANH - CANL | EN = nSTB = $V_{\text{IO}}$ , $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , TXD = 0V, $45\Omega \leq R_L \leq 70\Omega$ , $C_L = \text{open}$                                                                       | 1.4  |     | 3.3  | V             |
|                                                |                                                                                                              | CANH - CANL | EN = nSTB = $V_{\text{IO}}$ , $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , TXD = 0V, $R_L = 2240\Omega$ , $C_L = \text{open}$                                                                                      | 1.5  |     | 5    | V             |
| $V_{\text{DIFF(R)}}$                           | Differential output voltage<br>Normal mode, Silent mode<br>Recessive                                         | CANH - CANL | EN = nSTB = $V_{\text{IO}}$ , $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , TXD = $V_{\text{IO}}$ , $R_L = \text{open}$ , $C_L = \text{open}$                                                                       | -50  |     | 50   | mV            |
| $V_{\text{CAN(INACT)}}$                        | Bus output voltage<br>Sleep mode, Standby mode                                                               | CANH        | nSTB = 0V, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , TXD = $V_{\text{IO}}$ , $R_L = \text{open}$ (no load), $C_L = \text{open}$                                                                                 | -0.1 |     | 0.1  | V             |
|                                                |                                                                                                              | CANL        | nSTB = 0V, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , TXD = $V_{\text{IO}}$ , $R_L = \text{open}$ (no load), $C_L = \text{open}$                                                                                 | -0.1 |     | 0.1  | V             |
|                                                |                                                                                                              | CANH - CANL | nSTB = 0V, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ , TXD = $V_{\text{IO}}$ , $R_L = \text{open}$ (no load), $C_L = \text{open}$                                                                                 | -0.2 |     | 0.2  | V             |
| $I_{\text{OS(DOM)}}$                           | Short-circuit steady-state output current<br>Normal mode<br>Dominant                                         |             | nSTB = $V_{\text{IO}}$ , TXD = 0V<br>$-3\text{V} \leq V_{\text{CANH}} \leq 18\text{V}$                                                                                                                                      | -100 |     |      | mA            |
|                                                |                                                                                                              |             | nSTB = $V_{\text{IO}}$ , TXD = 0V<br>$-3\text{V} \leq V_{\text{CANL}} \leq 18\text{V}$                                                                                                                                      |      |     | 100  | mA            |
| $I_{\text{OS\_REC}}$                           | Short-circuit steady-state output current<br>Normal mode, Silent mode<br>Recessive                           |             | nSTB = $V_{\text{IO}}$ , $V_{\text{BUS}} = \text{CANH} = \text{CANL}$<br>$-27\text{V} \leq V_{\text{BUS}} \leq 40\text{V}$                                                                                                  | -3   |     | 3    | mA            |
| <b>CAN Receiver Characteristics</b>            |                                                                                                              |             |                                                                                                                                                                                                                             |      |     |      |               |
| $V_{\text{DIFF\_RX(D)}}$                       | Receiver dominant state input voltage range<br>Normal mode, Silent mode                                      |             | nSTB = $V_{\text{IO}}$ , $-12\text{V} \leq V_{\text{CM}} \leq 12\text{V}$                                                                                                                                                   | 0.9  |     | 8    | V             |
| $V_{\text{DIFF\_RX(R)}}$                       | Receiver recessive state input voltage range<br>Normal mode, Silent mode                                     |             |                                                                                                                                                                                                                             | -3   |     | 0.5  | V             |
| $V_{\text{HYS}}$                               | Hysteresis voltage for input threshold<br>Normal mode, Silent mode                                           |             | nSTB = $V_{\text{IO}}$                                                                                                                                                                                                      |      | 80  |      | mV            |
| $V_{\text{DIFF\_RX(D\_INACT)}}$                | Receiver dominant state input voltage range<br>Sleep mode, Standby mode                                      |             | nSTB = 0V, $-12\text{V} \leq V_{\text{CM}} \leq 12\text{V}$                                                                                                                                                                 | 1.1  |     | 9    | V             |
| $V_{\text{DIFF\_RX(R\_INACT)}}$                | Receiver recessive state input voltage range<br>Sleep mode, Standby mode                                     |             |                                                                                                                                                                                                                             | -4   |     | 0.4  | V             |
| $V_{\text{CM}}$                                | Common mode range                                                                                            |             | nSTB = $V_{\text{IO}}$                                                                                                                                                                                                      | -12  |     | 12   | V             |
| $I_{\text{LKG(IOFF)}}$                         | Power-off (unpowered) input leakage current<br>CANH, CANL pins                                               |             | $V_{\text{SUP}} = 0\text{V}$ , CANH = CANL = 5V                                                                                                                                                                             |      |     | 5    | $\mu\text{A}$ |
| $C_i$                                          | Input capacitance to ground (CANH or CANL) <sup>(1)</sup>                                                    |             |                                                                                                                                                                                                                             |      |     | 20   | pF            |
| $C_{\text{ID}}$                                | Differential input capacitance <sup>(1)</sup>                                                                |             |                                                                                                                                                                                                                             |      |     | 10   | pF            |
| $R_{\text{DIFF}}$                              | Differential input resistance                                                                                |             | TXD = $V_{\text{CC}} = V_{\text{IO}} = 5\text{V}$ , nSTB = 5V<br>$-2\text{V} \leq V_{\text{CM}} \leq 7\text{V}$                                                                                                             | 50   |     | 100  | k $\Omega$    |
| $R_{\text{SE\_CANH}}$<br>$R_{\text{SE\_CANL}}$ | Input resistance (CANH or CANL)                                                                              |             |                                                                                                                                                                                                                             | 25   |     | 50   | k $\Omega$    |
| $m_R$                                          | Input resistance matching:<br>$[1 - R_{\text{IN(CANH)}} / R_{\text{IN(CANL)}}] \times 100\%$                 |             | $V_{\text{CANH}} = V_{\text{CANL}} = 5\text{V}$                                                                                                                                                                             | -2   |     | 2    | %             |
| <b>TXD Characteristics</b>                     |                                                                                                              |             |                                                                                                                                                                                                                             |      |     |      |               |

## 5.8 Electrical Characteristics (continued)

Over recommended operating conditions with  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , unless otherwise noted. All typical values are taken at  $25^{\circ}\text{C}$ ,  $V_{\text{SUP}} = 12\text{V}$ ,  $V_{\text{IO}} = 3.3\text{V}$ ,  $V_{\text{CC}} = 5\text{V}$  and  $R_L = 60\Omega$

| PARAMETER                     |                                                                                            | TEST CONDITIONS                                                                             | MIN  | TYP | MAX  | UNIT            |
|-------------------------------|--------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|------|-----|------|-----------------|
| $V_{\text{IH}}$               | High-level input voltage                                                                   |                                                                                             | 0.7  |     |      | $V_{\text{IO}}$ |
| $V_{\text{IL}}$               | Low-level input voltage                                                                    |                                                                                             |      |     | 0.3  | $V_{\text{IO}}$ |
| $I_{\text{IH}}$               | High-level input leakage current                                                           | $\text{TXD} = V_{\text{IO}} = 5.5\text{V}$                                                  | -1   | 0   | 1    | $\mu\text{A}$   |
| $I_{\text{IL}}$               | Low-level input leakage current                                                            | $\text{TXD} = 0\text{V}$ , $V_{\text{IO}} = 5.5\text{V}$                                    | -115 |     | -2.5 | $\mu\text{A}$   |
| $I_{\text{LKG(OFF)}}$         | Unpowered leakage current                                                                  | $\text{TXD} = 5.5\text{V}$ , $V_{\text{SUP}} = V_{\text{IO}} = 0\text{V}$                   | -1   | 0   | 1    | $\mu\text{A}$   |
| $C_i$                         | Input Capacitance                                                                          | $V_{\text{IN}} = 0.4 \times \sin(2 \times \pi \times 2 \times 10^6 \times t) + 2.5\text{V}$ |      | 5   | 10   | pF              |
| <b>RXD Characteristics</b>    |                                                                                            |                                                                                             |      |     |      |                 |
| $V_{\text{OH}}$               | High-level output voltage                                                                  | $I_O = -2\text{mA}$                                                                         | 0.8  |     |      | $V_{\text{IO}}$ |
| $V_{\text{OL}}$               | Low-level output voltage                                                                   | $I_O = 2\text{mA}$                                                                          |      |     | 0.2  | $V_{\text{IO}}$ |
| $I_{\text{LKG(OFF)}}$         | Unpowered leakage current                                                                  | $\text{RXD} = 5.5\text{V}$ , $V_{\text{SUP}} = V_{\text{IO}} = 0\text{V}$                   | -1   |     | 1    | $\mu\text{A}$   |
| <b>nSTB Characteristics</b>   |                                                                                            |                                                                                             |      |     |      |                 |
| $V_{\text{IH}}$               | High-level input voltage                                                                   |                                                                                             | 0.7  |     |      | $V_{\text{IO}}$ |
| $V_{\text{IL}}$               | Low-level input voltage                                                                    |                                                                                             |      |     | 0.3  | $V_{\text{IO}}$ |
| $I_{\text{IH}}$               | High-level input leakage current                                                           | $\text{nSTB} = V_{\text{IO}} = 5.5\text{V}$                                                 | 0.5  |     | 115  | $\mu\text{A}$   |
| $I_{\text{IL}}$               | Low-level input leakage current                                                            | $\text{nSTB} = 0\text{V}$ , $V_{\text{IO}} = 5.5\text{V}$                                   | -1   |     | 1    | $\mu\text{A}$   |
| $I_{\text{LKG(OFF)}}$         | Unpowered leakage current                                                                  | $\text{nSTB} = 5.5\text{V}$ , $V_{\text{IO}} = 0\text{V}$                                   | -1   | 0   | 1    | $\mu\text{A}$   |
| <b>nFAULT Characteristics</b> |                                                                                            |                                                                                             |      |     |      |                 |
| $V_{\text{OH}}$               | High-level output voltage                                                                  | $I_O = -2\text{mA}$                                                                         | 0.8  |     |      | $V_{\text{IO}}$ |
| $V_{\text{OL}}$               | Low-level output voltage                                                                   | $I_O = 2\text{mA}$                                                                          |      |     | 0.2  | $V_{\text{IO}}$ |
| $I_{\text{LKG(OFF)}}$         | Unpowered leakage current                                                                  | $\text{nFAULT} = 5.5\text{V}$ , $V_{\text{IO}} = 0\text{V}$                                 | -1   | 0   | 1    | $\mu\text{A}$   |
| <b>EN Characteristics</b>     |                                                                                            |                                                                                             |      |     |      |                 |
| $V_{\text{IH}}$               | High-level input voltage                                                                   |                                                                                             | 0.7  |     |      | $V_{\text{IO}}$ |
| $V_{\text{IL}}$               | Low-level input voltage                                                                    |                                                                                             |      |     | 0.3  | $V_{\text{IO}}$ |
| $I_{\text{IH}}$               | High-level input leakage current                                                           | $\text{EN} = V_{\text{CC}} = V_{\text{IO}} = 5.5\text{V}$                                   | 0.5  |     | 115  | $\mu\text{A}$   |
| $I_{\text{IL}}$               | Low-level input leakage current                                                            | $\text{EN} = 0\text{V}$ , $V_{\text{CC}} = V_{\text{IO}} = 5.5\text{V}$                     | -1   |     | 1    | $\mu\text{A}$   |
| $I_{\text{LKG(OFF)}}$         | Unpowered leakage current                                                                  | $\text{EN} = 5.5\text{V}$ , $V_{\text{CC}} = V_{\text{IO}} = 0\text{V}$                     | -1   |     | 1    | $\mu\text{A}$   |
| $R_{\text{PD}}$               | Pull-down resistance                                                                       |                                                                                             | 50   |     | 2000 | k $\Omega$      |
| <b>WAKE Characteristics</b>   |                                                                                            |                                                                                             |      |     |      |                 |
| $V_{\text{IH}}$               | High-level input voltage                                                                   | Sleep mode                                                                                  | 2.6  |     |      | V               |
| $V_{\text{IL}}$               | Low-level input voltage                                                                    |                                                                                             |      |     | 1.8  | V               |
| $I_{\text{IH}}$               | High-level input leakage current <sup>(2)</sup>                                            | $\text{WAKE} = V_{\text{SUP}}$                                                              |      |     | 2    | $\mu\text{A}$   |
|                               |                                                                                            | $\text{WAKE} = 4\text{V}$                                                                   | -3   |     |      | $\mu\text{A}$   |
| $I_{\text{IL}}$               | Low-level input leakage current <sup>(2)</sup>                                             | $\text{WAKE} = 1\text{V}$                                                                   |      |     | 3    | $\mu\text{A}$   |
| $R_{\text{WAKE}}$             | Pull-up/pull-down resistance <sup>(2)</sup>                                                |                                                                                             |      | 600 |      | k $\Omega$      |
| <b>INH Characteristics</b>    |                                                                                            |                                                                                             |      |     |      |                 |
| $\Delta V_{\text{H}}$         | High-level voltage drop from $V_{\text{SUP}}$ to INH ( $V_{\text{SUP}} - V_{\text{INH}}$ ) | $I_{\text{INH}} = -2\text{mA}$                                                              |      | 1   | 2    | V               |
| $I_{\text{LKG(INH)}}$         | Sleep mode leakage current                                                                 | $\text{INH} = 0\text{V}$                                                                    | -0.5 |     | 0.5  | $\mu\text{A}$   |

(1) Specified by design and verified via bench characterization

(2) The WAKE pin automatically configures itself based on the applied voltage to either an internal pull-up to 5V or pull-down to GND. A high-level input results in an internal pull-up to 5V and a low-level input results in an internal pull-down to GND. Current consumption is minimized overall when WAKE is connected to  $V_{\text{CC}}$  or GND.



## 5.9 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                          |                                                                                                                   | TEST CONDITIONS                                                                                | MIN | TYP | MAX  | UNIT    |
|------------------------------------|-------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|-----|-----|------|---------|
| <b>Supply Characteristics</b>      |                                                                                                                   |                                                                                                |     |     |      |         |
| $t_{PWRUP}$                        | Time required for INH active after $V_{SUP} \geq UV_{SUP(R)}$                                                     |                                                                                                |     | 310 | 1000 | $\mu s$ |
| $t_{UV}$                           | Undervoltage filter time $V_{CC}$ and $V_{IO}$ <sup>(1)</sup>                                                     | $V_{CC} \leq UV_{CC}$ or $V_{IO} \leq UV_{IO}$                                                 | 100 |     | 350  | ms      |
| $t_{UV\_det}$                      | Undervoltage detection time for $V_{CC}$ and $V_{IO}$                                                             | $V_{CC} \leq UV_{CC}$ or $V_{IO} \leq UV_{IO}$                                                 |     |     | 30   | $\mu s$ |
| $t_{UV(RE-ENABLE)}$                | Re-enable time after undervoltage event <sup>(1)</sup>                                                            | Time for device to return to normal operation from a $UV_{CC}$ or $UV_{IO}$ undervoltage event |     |     | 50   | $\mu s$ |
| <b>Device Characteristics</b>      |                                                                                                                   |                                                                                                |     |     |      |         |
| $t_{PROP(LOOP1)}$                  | Total loop delay, driver input (TXD) to receiver output (RXD) Recessive to dominant                               | $R_L = 60\Omega$ , $C_L = 100pF$ , $C_{L\_RXD} = 15pF$ $V_{IO}=3V - 5.5V$                      |     |     | 250  | ns      |
| $t_{PROP(LOOP2)}$                  | Total loop delay, driver input (TXD) to receiver output (RXD) Dominant to recessive                               | $R_L = 60\Omega$ , $C_L = 100pF$ , $C_{L\_RXD} = 15pF$ $V_{IO}=3V - 5.5V$                      |     |     | 250  | ns      |
| $t_{WK(TIMEOUT)}$                  | Bus wake-up timeout value <sup>(1)</sup>                                                                          |                                                                                                | 0.8 |     | 2    | ms      |
| $t_{WK(FILTER)}$                   | Bus time to meet filtered bus requirements for wake-up request <sup>(1)</sup>                                     |                                                                                                | 0.5 |     | 1.8  | $\mu s$ |
| $t_{FILTER\_IO}$                   | Filter time for EN/nSTB <sup>(1)</sup>                                                                            |                                                                                                | 1   |     | 5    | $\mu s$ |
| $t_{WAKE\_HT}$                     | Hold time for which WAKE pin voltage must be stable after the rising or falling edge on WAKE pin to recognize LWU |                                                                                                | 5   |     | 50   | $\mu s$ |
| <b>Mode Change Characteristics</b> |                                                                                                                   |                                                                                                |     |     |      |         |
| $t_{INH\_SLP\_STB}$                | Time after WUP or LWU event until INH asserted <sup>(1)</sup>                                                     |                                                                                                |     |     | 50   | $\mu s$ |
| $t_{MODE1}$                        | Mode change time from leaving the Sleep mode to entering Normal or Silent mode <sup>(1)</sup>                     | Time measured from VCC and VIO crossing UV thresholds to entering normal or silent mode.       |     |     | 50   | $\mu s$ |
| $t_{MODE2}$                        | Mode change time between normal, silent and standby mode and from sleep to standby mode <sup>(1)</sup>            | Mode change time between normal, silent and standby mode and from sleep to standby mode        |     |     | 50   | $\mu s$ |
| $t_{nFAULT\_MODE\_CHANGE}$         | nFAULT stabilization time after mode change                                                                       |                                                                                                |     |     | 20   | $\mu s$ |
| $t_{GOTOSLEEP}$                    | Minimum hold time for transition to sleep mode <sup>(1)</sup>                                                     | EN = H and nSTB = L                                                                            | 20  |     | 50   | $\mu s$ |

(1) Specified by design and verified using bench characterization

## 5.10 Switching Characteristics

Over recommended operating conditions with  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , unless otherwise noted. All typical values are taken at  $25^{\circ}\text{C}$ ,  $V_{\text{SUP}} = 12\text{V}$ ,  $V_{\text{IO}} = 3.3\text{V}$ ,  $V_{\text{CC}} = 5\text{V}$  and  $R_L = 60\Omega$

| PARAMETER                         |                                                                                                            | TEST CONDITIONS                                                                                                                                        | MIN  | TYP | MAX | UNIT |
|-----------------------------------|------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|-----|------|
| <b>Driver Characteristics</b>     |                                                                                                            |                                                                                                                                                        |      |     |     |      |
| $t_{\text{pHR}}$                  | Propagation delay time, high TXD to driver recessive                                                       | $R_L = 60\Omega$ , $C_L = 100\text{pF}$ , $R_{\text{CM}} = \text{open}$                                                                                |      | 90  |     | ns   |
| $t_{\text{pLD}}$                  | Propagation delay time, low TXD to driver dominant                                                         |                                                                                                                                                        |      | 75  |     | ns   |
| $t_{\text{sk(p)}}$                | Pulse skew ( $ t_{\text{pHR}} - t_{\text{pLD}} $ )                                                         |                                                                                                                                                        |      | 25  |     | ns   |
| $t_{\text{R}}$                    | Differential output signal rise time                                                                       |                                                                                                                                                        |      | 45  |     | ns   |
| $t_{\text{F}}$                    | Differential output signal fall time                                                                       |                                                                                                                                                        |      | 45  |     | ns   |
| $t_{\text{TXDDTO}}$               | Dominant timeout                                                                                           | $\text{TXD} = 0\text{V}$ , $R_L = 60\Omega$ , $C_L = \text{open}$                                                                                      | 1.2  |     | 3.8 | ms   |
| <b>Receiver Characteristics</b>   |                                                                                                            |                                                                                                                                                        |      |     |     |      |
| $t_{\text{pRH}}$                  | Propagation delay time, bus recessive input to high RXD                                                    | $C_{\text{L(RXD)}} = 15\text{pF}$                                                                                                                      |      | 65  |     | ns   |
| $t_{\text{pDL}}$                  | Propagation delay time, bus dominant input to RXD low output                                               |                                                                                                                                                        |      | 60  |     | ns   |
| $t_{\text{R}}$                    | Output signal rise time (RXD)                                                                              |                                                                                                                                                        |      | 10  |     | ns   |
| $t_{\text{F}}$                    | Output signal fall time (RXD)                                                                              |                                                                                                                                                        |      | 10  |     | ns   |
| $t_{\text{BUSDOM}}$               | Dominant time out                                                                                          | $R_L = 60\Omega$ , $C_L = \text{open}$                                                                                                                 | 1.2  |     | 3.8 | ms   |
| <b>CAN FD Characteristics</b>     |                                                                                                            |                                                                                                                                                        |      |     |     |      |
| $t_{\Delta\text{BIT(BUS)}}^{(1)}$ | Transmitted recessive bit width variation on CAN bus output pins with $t_{\text{BIT(TXD)}} = 500\text{ns}$ | $R_L = 60\Omega$ , $C_L = 100\text{pF}$ , $C_{\text{L\_RXD}} = 15\text{pF}$<br>$t_{\Delta\text{BIT(BUS)}} = t_{\text{BIT(BUS)}} - t_{\text{BIT(TXD)}}$ | -65  |     | 30  | ns   |
| $t_{\Delta\text{BIT(BUS)}}^{(1)}$ | Transmitted recessive bit width variation on CAN bus output pins with $t_{\text{BIT(TXD)}} = 200\text{ns}$ | $R_L = 60\Omega$ , $C_L = 100\text{pF}$ , $C_{\text{L\_RXD}} = 15\text{pF}$<br>$t_{\Delta\text{BIT(BUS)}} = t_{\text{BIT(BUS)}} - t_{\text{BIT(TXD)}}$ | -45  |     | 10  | ns   |
| $t_{\Delta\text{BIT(RXD)}}^{(1)}$ | Received recessive bit width variation on RXD output pins with $t_{\text{BIT(TXD)}} = 500\text{ns}$        | $R_L = 60\Omega$ , $C_2 = 100\text{pF}$ , $C_{\text{L\_RXD}} = 15\text{pF}$<br>$t_{\Delta\text{BIT(RXD)}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(TXD)}}$ | -100 |     | 50  | ns   |
| $t_{\Delta\text{BIT(RXD)}}^{(1)}$ | Received recessive bit width variation on RXD output pins with $t_{\text{BIT(TXD)}} = 200\text{ns}$        | $R_L = 60\Omega$ , $C_2 = 100\text{pF}$ , $C_{\text{L\_RXD}} = 15\text{pF}$<br>$t_{\Delta\text{BIT(RXD)}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(TXD)}}$ | -80  |     | 20  | ns   |
| $t_{\Delta\text{REC}}^{(1)}$      | Receiver timing symmetry with $t_{\text{BIT(TXD)}} = 500\text{ns}$                                         | $R_L = 60\Omega$ , $C_2 = 100\text{pF}$ , $C_{\text{L\_RXD}} = 15\text{pF}$<br>$\Delta t_{\text{REC}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(BUS)}}$     | -65  |     | 40  | ns   |
|                                   | Receiver timing symmetry with $t_{\text{BIT(TXD)}} = 200\text{ns}$                                         | $R_L = 60\Omega$ , $C_2 = 100\text{pF}$ , $C_{\text{L\_RXD}} = 15\text{pF}$<br>$\Delta t_{\text{REC}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(BUS)}}$     | -45  |     | 15  | ns   |

(1) The input signal on TXD shall have rise times and fall times (10% to 90%) of less than 10ns

## 5.11 Typical Characteristics

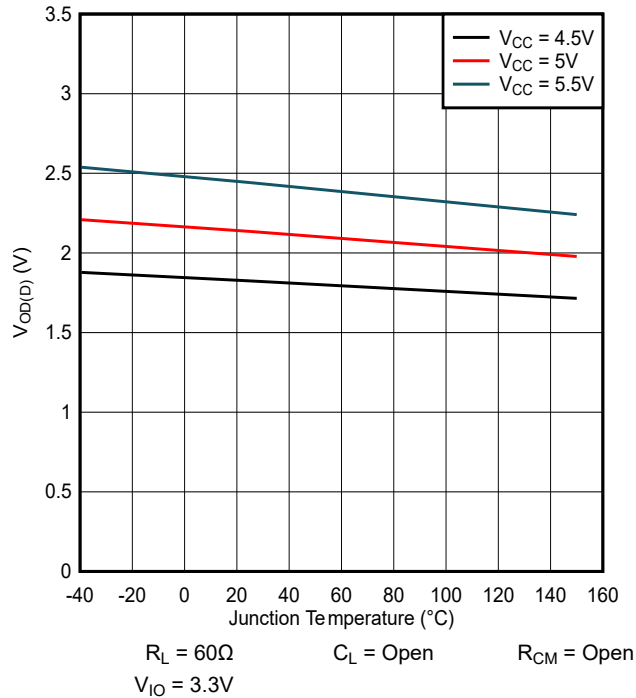


Figure 5-1.  $V_{OD(DOM)}$  vs Temperature and  $V_{CC}$

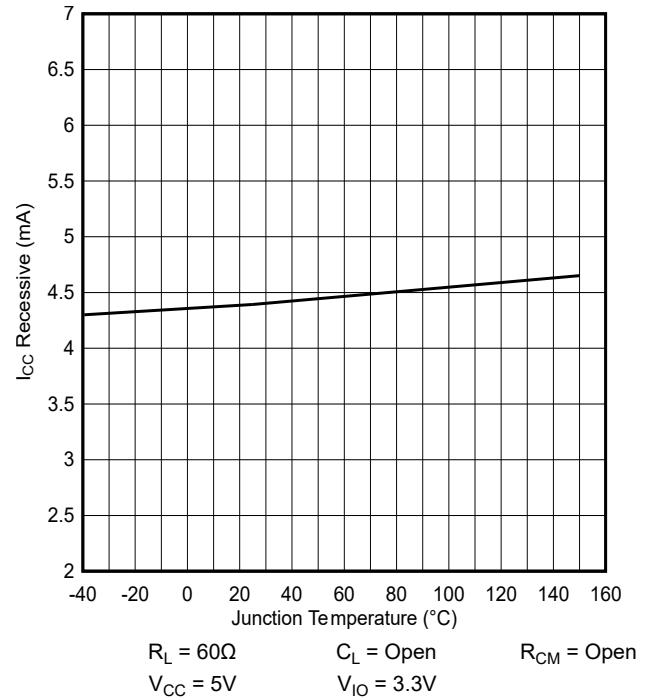


Figure 5-2.  $I_{CC \text{ Recessive}}$  vs Temperature

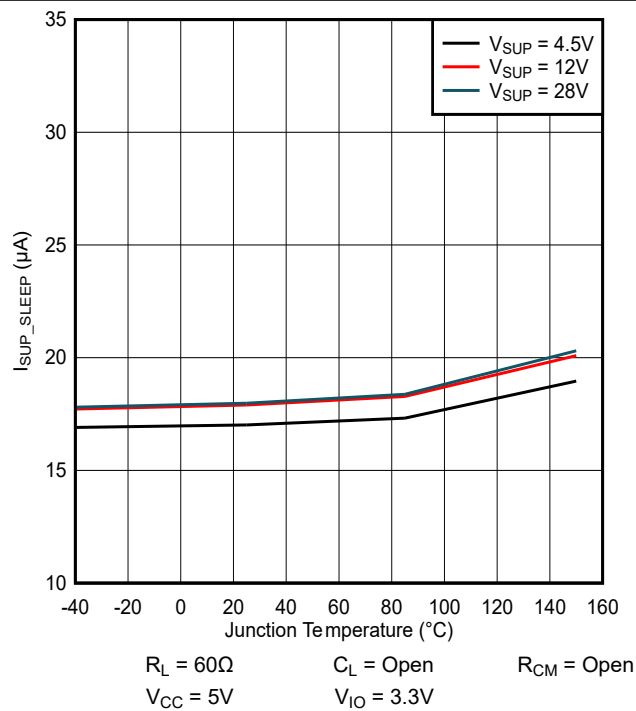


Figure 5-3.  $I_{SUP}$  in Sleep Mode vs  $V_{SUP}$  and Temperature

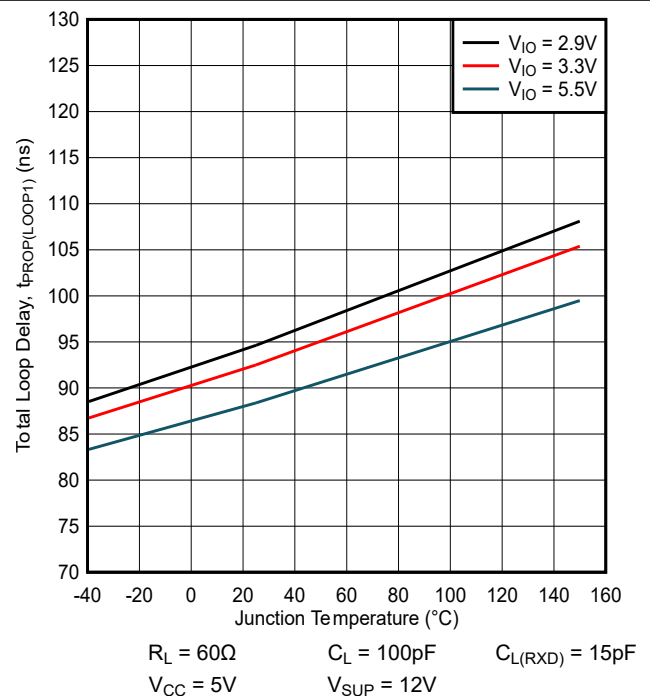
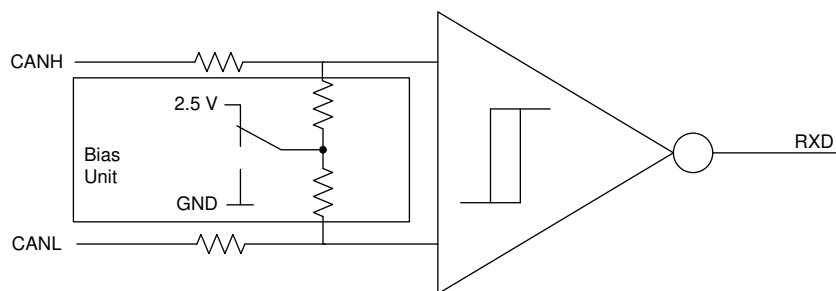
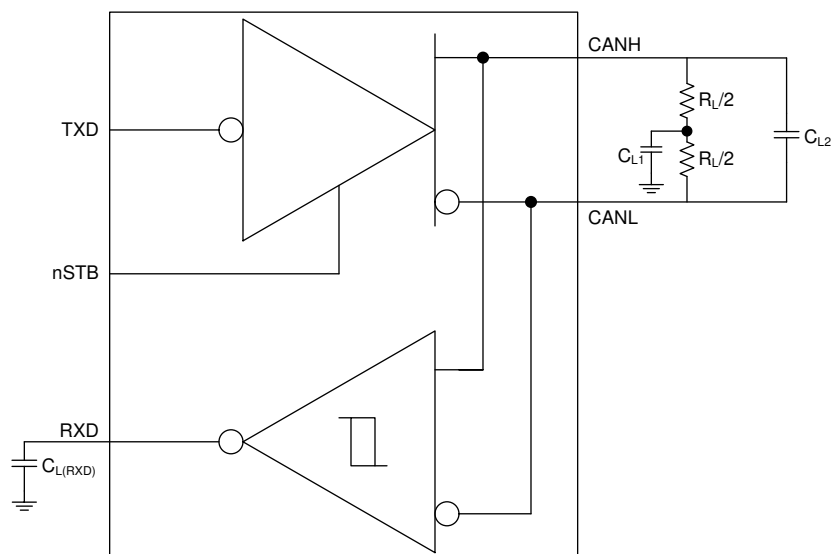


Figure 5-4. Loop Propagation Delay vs  $V_{IO}$  and Temperature

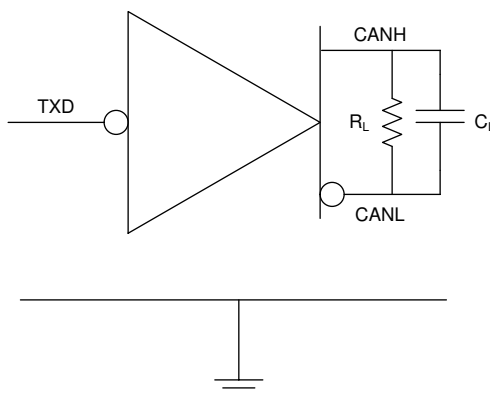
## 6 Parameter Measurement Information



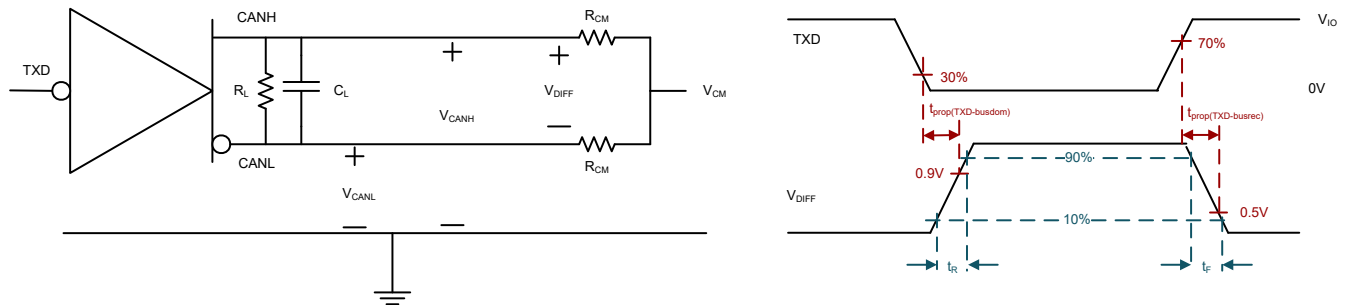
**Figure 6-1. Common-Mode Bias Unit and Receiver**



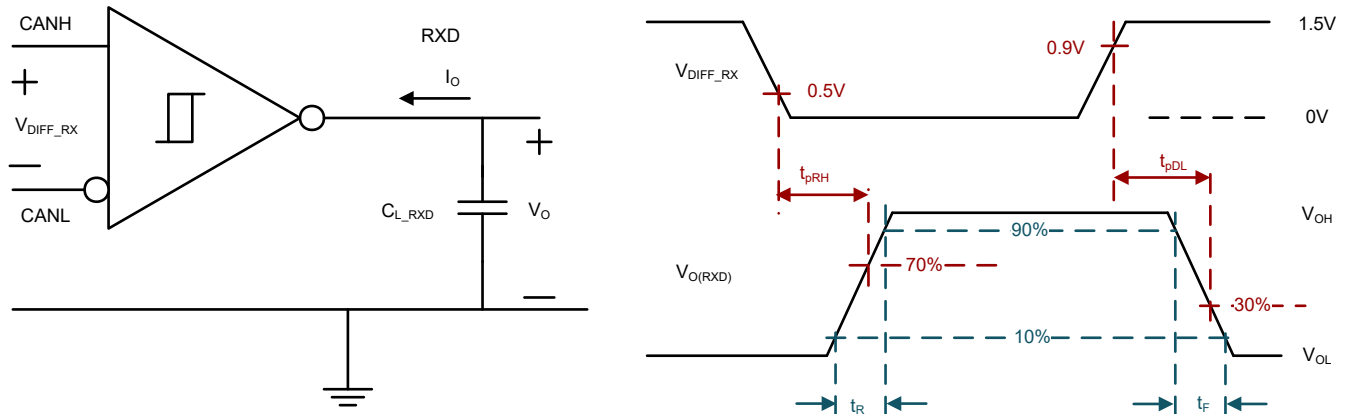
**Figure 6-2. Test Circuit**



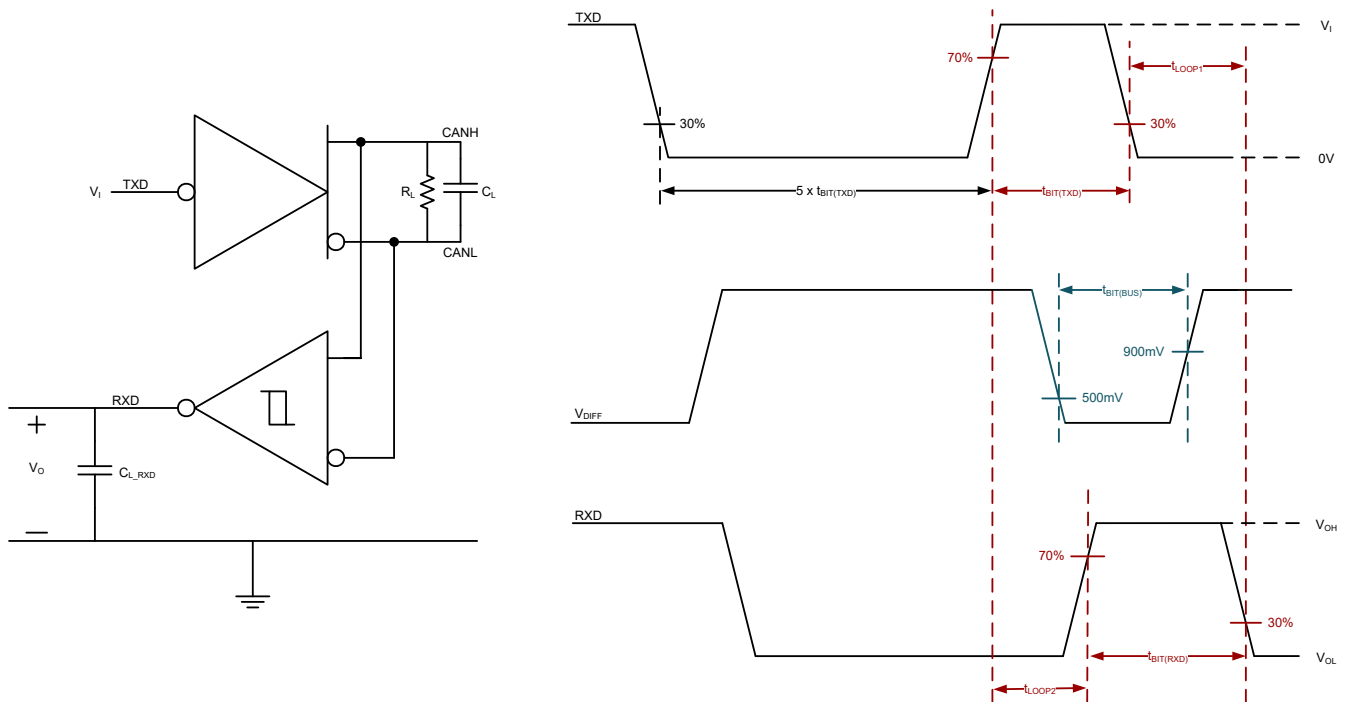
**Figure 6-3. Supply Test Circuit**



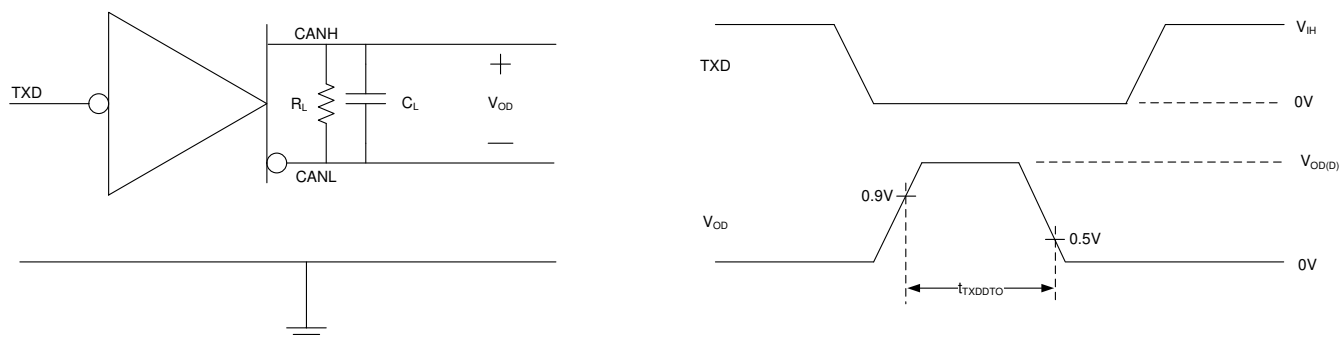
**Figure 6-4. Driver Test Circuit and Measurement**



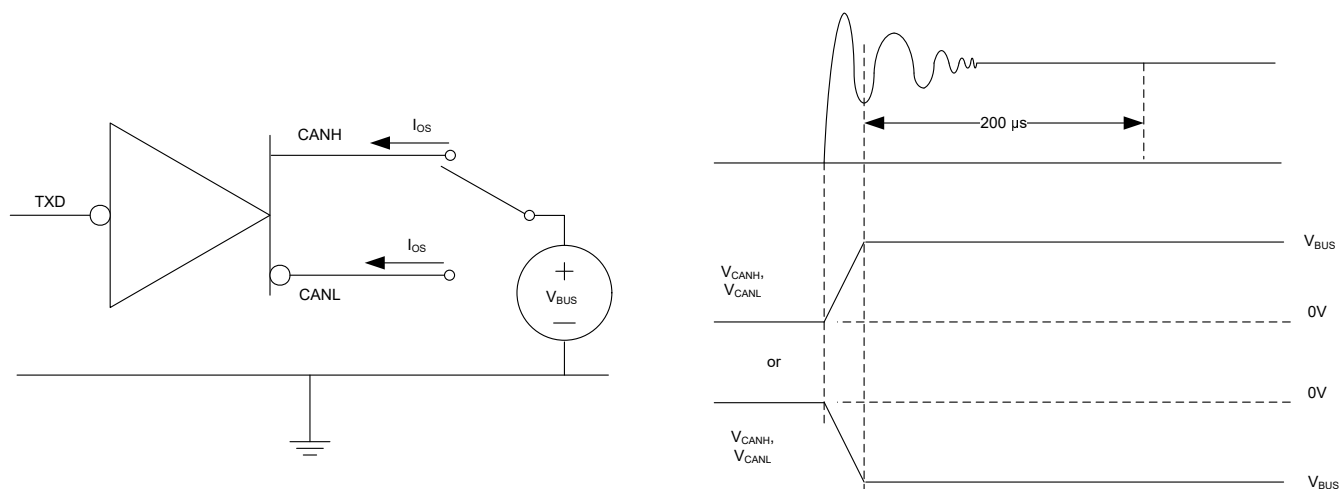
**Figure 6-5. Receiver Test Circuit and Measurement**



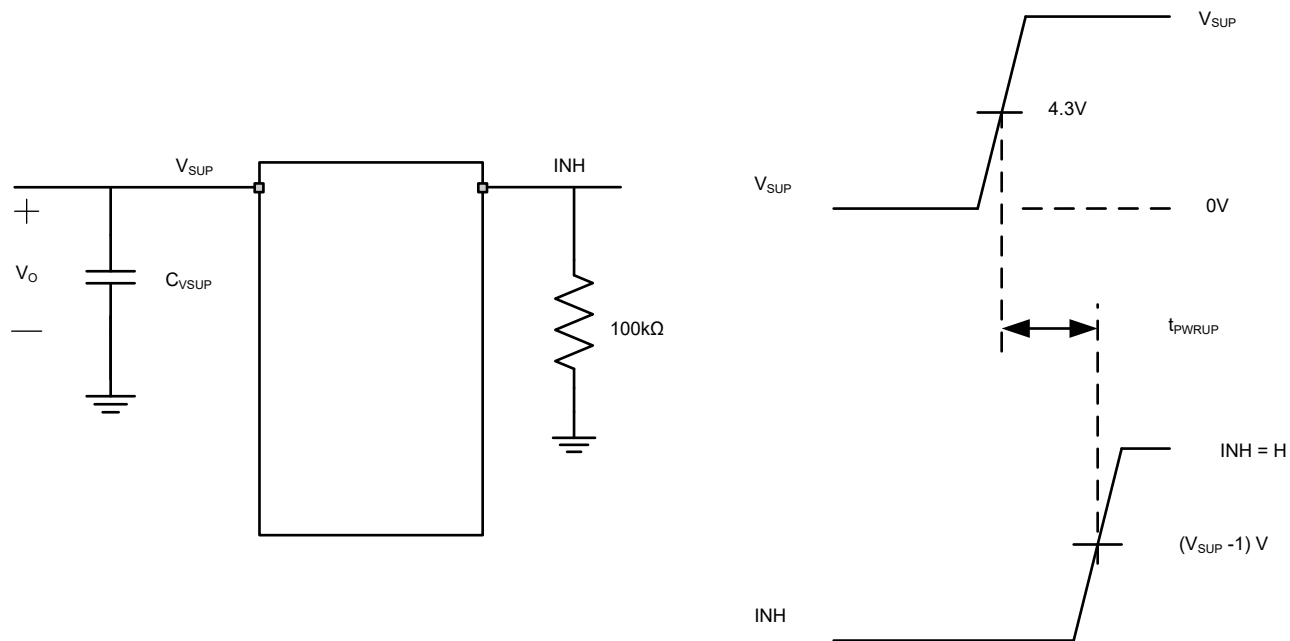
**Figure 6-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement**



**Figure 6-7. TXD Dominant Time Out Test Circuit and Measurement**



**Figure 6-8. Driver Short-Circuit Current Test and Measurement**



**Figure 6-9. Power-Up Timing**

## 7 Detailed Description

### 7.1 Overview

The TCAN943-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 high-speed CAN specification. The TCAN943-Q1 supports both classical CAN and CAN FD networks up to 5 megabits per second (Mbps).

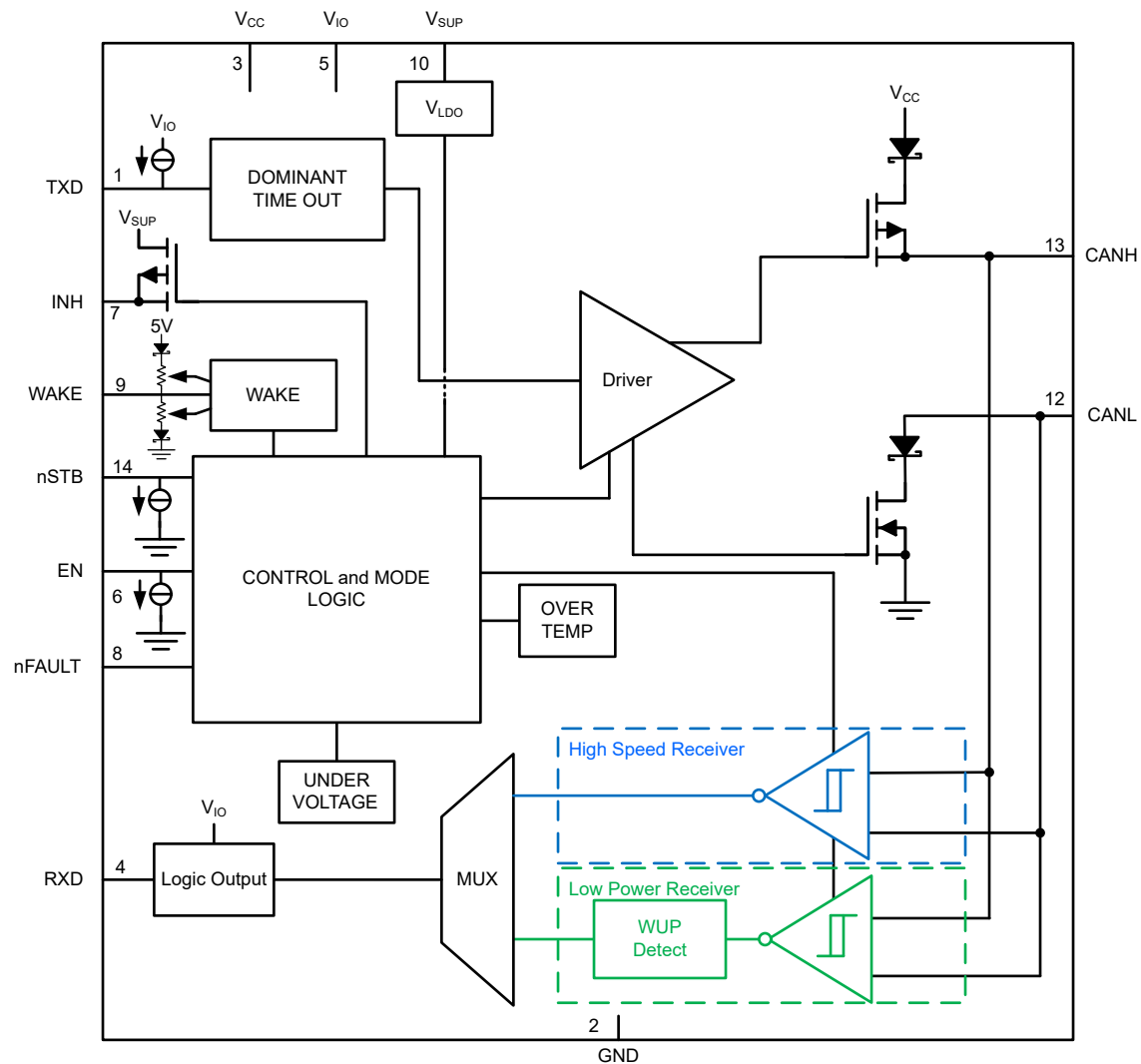
The TCAN943-Q1 supports at least the following CAN and CAN FD standards:

- Physical layer:
  - ISO 11898-2:2024 – High-speed physical medium attachment (PMA) sublayer
  - SAE J2284-1 – High Speed CAN (HSC) for Vehicle Applications at 125kbps
  - SAE J2284-2 – High Speed CAN (HSC) for Vehicle Applications at 250kbps
  - SAE J2284-3 – High Speed CAN (HSC) for Vehicle Applications at 500kbps
  - SAE J2284-4 – High Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
  - SAE J2284-5 – High Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps
- Conformance test requirements
  - ISO 16845-2:2018 – High-speed medium access unit – Conformance test plan
  - IOPT.CAN – Interoperability test specification for high-speed CAN transceiver or equivalent devices

The transceiver has three separate supply inputs,  $V_{SUP}$ ,  $V_{CC}$ , and  $V_{IO}$ . By using  $V_{IO}$ , the TCAN943-Q1 can interface directly to a 3.3V, or 5V controller without the need for a level shifter. The TCAN943-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that can be present in the system via the INH output pin. This enables a low-current sleep state in which power is gated to all system components except for the TCAN943-Q1, which remains in a low-power state while monitoring the CAN bus. When a wake-up pattern is detected on the bus or when a local wake up is requested via the WAKE input, the device initiates node start-up by driving INH high.

The TCAN943-Q1 includes many protection and diagnostic features including undervoltage detection, CAN bus fault detection, battery connection detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and bus fault protection up to  $\pm 40V$ .

## 7.2 Functional Block Diagram



**Figure 7-1. TCAN943-Q1 Functional Block Diagram**



## 7.3 Feature Description

### 7.3.1 Supply Pins

The TCAN943-Q1 implements three independent supply inputs for regulating different portions of the device.

#### 7.3.1.1 $V_{SUP}$ Pin

This pin is connected to the battery supply. The pin provides the supply to the internal regulators that support the digital core and the low power CAN receiver.

#### 7.3.1.2 $V_{CC}$ Pin

This pin provides the 5V supply voltage for the CAN transceiver.

#### 7.3.1.3 $V_{IO}$ Pin

This pin provides the digital I/O voltage to match the CAN FD controller's I/O voltage. The pin supports I/O voltages from 2.9V to 5.5V providing a wide range of controller support.

### 7.3.2 Digital Inputs and Outputs

#### 7.3.2.1 TXD Pin

TXD is a logic-level input signal, referenced to  $V_{IO}$ , from a CAN FD controller to the TCAN943-Q1. TXD is biased to the  $V_{IO}$  level to force a recessive input in case the pin floats.

#### 7.3.2.2 RXD Pin

RXD is a logic-level signal output, referenced to  $V_{IO}$ , from the TCAN943-Q1 to a CAN FD controller. The RXD pin is driven to the  $V_{IO}$  level as logic-high outputs once a valid  $V_{IO}$  is present.

When a power-on or wake-up event takes place, the RXD pin is pulled low.

#### 7.3.2.3 nFAULT Pin

nFAULT is a logic-level output signal, referenced to  $V_{IO}$ , from the TCAN943-Q1 to a CAN FD controller. The nFAULT output is driven to the  $V_{IO}$  level as logic-high output.

The nFAULT output is used to transmit the TCAN943-Q1 status indicator flags to the CAN FD controller. Please see [Table 7-1](#) for the specific fault scenarios that are indicated externally via the nFAULT pin. The TCAN943-Q1 drives the nFAULT pin high when  $V_{IO}$  is present and in the Sleep mode to conserve power because there are no fault scenarios that are indicated externally in Sleep mode.

#### 7.3.2.4 EN Pin

EN is a logic-level input signal, referenced to  $V_{IO}$ , from a CAN FD controller to the TCAN943-Q1. The EN input pin is for mode selection in conjunction with the nSTB pin. EN is internally pulled low to prevent excessive system power and false wake-up events.

#### 7.3.2.5 nSTB Pin

nSTB is a logic-level input signal, referenced to  $V_{IO}$ , from a CAN FD controller to the TCAN943-Q1. The nSTB input pin is for mode selection in conjunction with the EN pin. nSTB is internally pulled low to prevent excessive system power and false wake-up events.

#### 7.3.2.6 NC Pin

NC pin is not connected internally, leave this pin floating or connect the pin to GND

### 7.3.3 GND

GND is the ground pin of the transceiver, the pin must be connected to the PCB ground.

### 7.3.4 INH Pin

The INH pin is a high-voltage output. The pin can be used to control external regulators. These regulators are typically used to support the microprocessor and  $V_{IO}$  pin. The INH function is on in all modes except for sleep mod. In sleep mode, the INH pin is turned off, going into a high-impedance state. This allows the node to be

placed into the lowest power state while in sleep mode. A 100k $\Omega$  load can be added to the INH output for a fast transition time from the driven high state to the low state and to force the pin low when left floating.

This terminal must be considered a high-voltage logic terminal, not a power output. The INH pin must be used to drive the EN terminal of the system power management device, and must not be used as a switch for the power management supply. This terminal is not reverse-battery protected; thus, must not be connected outside the system module.

### 7.3.5 WAKE Pin

The WAKE pin is a high-voltage reverse-blocked input used for the local wake-up (LWU) function. The WAKE pin is bi-directional edge-triggered and recognizes a local wake-up (LWU) on either a rising or falling edge of WAKE pin transition. The LWU function is explained further in the [Local Wake-Up \(LWU\) via WAKE Input Terminal](#) section.

### 7.3.6 CAN Bus Pins

These are the CAN high and CAN low, CANH and CANL, differential bus pins. These pins are internally connected to the CAN transceiver and the low-voltage wake receiver.

### 7.3.7 Faults

#### 7.3.7.1 Internal and External Fault Indicators

The following device status indicator flags are implemented to allow for the MCU to determine the status of the device and the system. In addition to faults, the nFAULT terminal also signals wake-up requests and a “cold” power-up sequence on the V<sub>SUP</sub> battery terminal so the system can do any diagnostics or cold booting sequence necessary. The RXD terminal indicates wake-up request and the faults are multiplexed (ORed) to the nFAULT output.

**Table 7-1. TCAN943-Q1 Transceiver Status Indicator**

| EVENT                                     | FLAG NAME                    | CAUSE                                                                                                | INDICATORS <sup>(1)</sup>                                                                                                                                                               | FLAG IS CLEARED                                                                                                                                                         | COMMENT                                                                                                                                                                      |
|-------------------------------------------|------------------------------|------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power-up                                  | <i>PWRON</i>                 | Power up on $V_{SUP}$ and any return of $V_{SUP}$ after the battery supply has been below $UV_{SUP}$ | nFAULT = low upon entering silent mode from standby or sleep mode                                                                                                                       | After a transition to normal mode                                                                                                                                       | A cold start condition generates a local wake-up WAKERQ, WAKESR and a PWRON flag.                                                                                            |
| Wake-up Request                           | <i>WAKERQ</i> <sup>(2)</sup> |                                                                                                      | nFAULT = RXD = low after wake-up upon entering standby mode                                                                                                                             | After a transition to normal mode or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \geq t_{UV}$                                                                 | Wake-up request can only be set from standby, go-to-sleep, or sleep mode. Resets expired timers for $UV_{VCC}$ or $UV_{VIO}$ in sleep mode.                                  |
| Wake-up Source Recognition <sup>(3)</sup> | <i>WAKESR</i>                | Wake-up event on CAN bus, state transition on WAKE pin, or initial power up                          | Available upon entering normal mode <sup>(4)</sup><br>nFAULT = low indicates a local wake-up event from the WAKE pin<br>nFAULT = high indicates a remote wake-up event from the CAN bus | After four recessive-to-dominant edges on TXD in normal mode, <sup>(5)</sup> leaving normal mode, or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \geq t_{UV}$ | A cold start condition generates a local wake-up WAKERQ, WAKESR and a PWRON flag.                                                                                            |
| Undervoltage                              | $UV_{CC}$                    | $V_{CC} < UV_{CC(F)}$                                                                                | Not externally indicated                                                                                                                                                                | $V_{CC} > UV_{CC(R)}$ , or a wake-up request occurs                                                                                                                     |                                                                                                                                                                              |
|                                           | $UV_{IO}$                    | $V_{IO} < UV_{IO(F)}$                                                                                | Not externally indicated                                                                                                                                                                | $V_{IO} > UV_{IO(R)}$ , or a wake-up request occurs                                                                                                                     |                                                                                                                                                                              |
|                                           | $UV_{SUP}$                   | $V_{SUP} < UV_{SUP(F)}$                                                                              | Not externally indicated                                                                                                                                                                | $V_{SUP} > UV_{SUP(R)}$                                                                                                                                                 | A $V_{SUP}$ undervoltage event generates a cold start condition once $V_{SUP} > UV_{SUP(R)}$ .                                                                               |
| Local Faults                              | <i>TXDDTO</i>                | TXD dominant time out, dominant (low) signal for $t \geq t_{TXDDTO}$                                 | nFAULT = low upon entering silent mode from normal mode                                                                                                                                 | RXD = low and TXD = high for 4 $\mu$ s, or a mode transition into normal, standby, go-to-sleep, or sleep modes                                                          | CAN driver remains disabled until the <i>TXDDTO</i> is cleared. CAN receiver remains active during the <i>TXDDTO</i> fault.                                                  |
|                                           | <i>TXDRXD</i>                | TXD and RXD pins are shorted together for $t \geq t_{TXDDTO}$                                        |                                                                                                                                                                                         |                                                                                                                                                                         | CAN driver remains disabled until the <i>TXDRXD</i> is cleared. CAN receiver remains active during the <i>TXDRXD</i> fault. <i>TXDRXD</i> is detected while TXD = RXD = low. |
|                                           | <i>CANDOM</i>                | CAN bus dominant fault, when dominant bus signal received for $t \geq t_{BUSDOM}$                    |                                                                                                                                                                                         | RXD = high, or a transition into normal, standby, go-to-sleep, or sleep modes                                                                                           | CAN driver remains enabled during <i>CANDOM</i> fault.                                                                                                                       |
|                                           | <i>TSD</i>                   | Thermal shutdown, $T_J \geq T_{SDR}$                                                                 |                                                                                                                                                                                         | $T_J < T_{SDF}$ and RXD = low and TXD = high for 4 $\mu$ s, or transition into normal, standby, go-to-sleep, or sleep modes                                             | CAN driver remains disabled until the <i>TSD</i> event is cleared. CAN receiver remains active during the <i>TSD</i> fault.                                                  |

(1)  $V_{IO}$  and  $V_{SUP}$  are present

(2) Transitions to go-to-sleep mode is blocked until WAKERQ flag is cleared

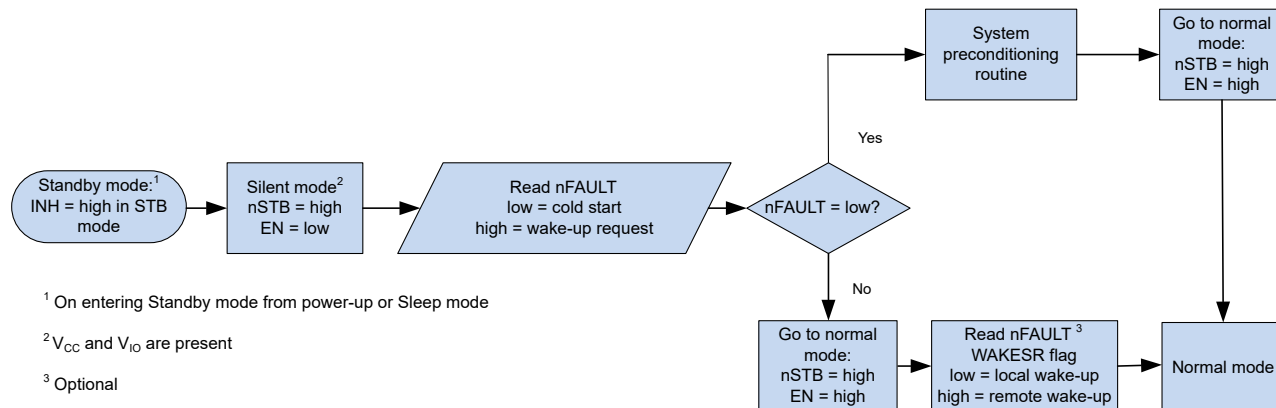
(3) Wake-up source recognition reflects the first wake up source. If additional wake-up events occur the source still indicates the original wake-up source

(4) Indicator is only available in normal mode until the flag is cleared

(5) A minimum of 4 $\mu$ s between recessive-to-dominant edges is required to clear the WAKESR flag

#### 7.3.7.1.1 Power-Up (*PWRON* Flag)

This is an internal and external flag that can be used to control the power-up sequence of the system. When a new battery connection to the transceiver is made the *PWRON* flag is set signifying a cold start condition. The TCAN943-Q1 treats any undervoltage conditions on the  $V_{SUP}$ ,  $V_{SUP} < UV_{SUP(F)}$ , as a cold start. Therefore, when the  $V_{SUP} > UV_{SUP(R)}$  condition is met the TCAN943-Q1 sets the *PWRON* flag which can be used by the system to enter a routine that is only called upon in cold start situations. The *PWRON* flag is indicated by nFAULT driven low after entering silent mode from either standby mode or sleep mode. This flag is cleared after a transition to normal mode.



**Figure 7-2. Distinguishing between *PWRON* and Wake Request by Entering Silent Mode**

#### 7.3.7.1.2 Wake-Up Request (WAKERQ Flag)

This is an internal and external flag that can be set in standby, go-to-sleep, or sleep mode. This flag is set when either a valid local wake-up (LWU) request occurs, or a valid remote wake request occurs, or on power up on  $V_{SUP}$ . The setting of this flag clears the  $t_{UV}$  timer for the  $UV_{CC}$  or  $UV_{IO}$  fault detection. This flag is cleared upon entering normal mode or during an undervoltage event on  $V_{CC}$  or  $V_{IO}$ .

#### 7.3.7.1.3 Undervoltage Faults

The TCAN943-Q1 device implements undervoltage detection circuits on all supply terminals:  $V_{SUP}$ ,  $V_{CC}$ , and  $V_{IO}$ . The undervoltage flags are internal indicator flags and are not indicated on the nFAULT output pin.

##### 7.3.7.1.3.1 Undervoltage on $V_{SUP}$

$UV_{SUP}$  is set when the voltage on  $V_{SUP}$  drops below the undervoltage detection voltage threshold,  $UV_{SUP}$ . The *PWRON*, *WAKERQ*, and *WAKESR* flags are set once  $V_{SUP} > UV_{SUP(R)}$ .

##### 7.3.7.1.3.2 Undervoltage on $V_{CC}$

$UV_{CC}$  is set when the voltage on  $V_{CC}$  drops below the undervoltage detection voltage threshold,  $UV_{CC}$ , for longer than the  $t_{UV}$  undervoltage filter time.

##### 7.3.7.1.3.3 Undervoltage on $V_{IO}$

$UV_{IO}$  is set when the voltage on  $V_{IO}$  drops below the undervoltage detection voltage threshold,  $UV_{IO}$ , for longer than the  $t_{UV}$  undervoltage filter time.

#### 7.3.7.1.4 TXD Dominant State Timeout (TXDDTO Flag)

TXDDTO is an external flag that is set if the TXD pin is held dominant for  $t > t_{TXDDTO}$ . If a TXD DTO condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode. The TXDDTO flag is cleared when TXD = H and RXD = L in normal mode or upon a transition into normal, standby, go-to-sleep, or sleep modes.

#### 7.3.7.1.5 TXD Shorted to RXD Fault (TXDRXD Flag)

TXDRXD is an external flag that is set if the transceiver detects that the TXD and RXD lines have been shorted together. The device requires a dominant signal for  $t \geq t_{TXDDTO}$  for this fault to be detected. If a TXDRXD condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode and the CAN bus driver is disabled until the TXDRXD fault is cleared. The TXDRXD flag is cleared on the next dominant-to-recessive transition with TXD high and RXD low or upon a transition into normal, standby, go-to-sleep, or sleep modes.

#### 7.3.7.1.6 CAN Bus Dominant Fault (CANDOM Flag)

CANDOM is an external flag that is set if the CAN bus is stuck dominant state for  $t > t_{BUSDOM}$ . If a CANDOM condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode. The CANDOM

flag is cleared on the next dominant-to-recessive transition on RXD or upon a transition into normal, standby, go-to-sleep, or sleep modes.

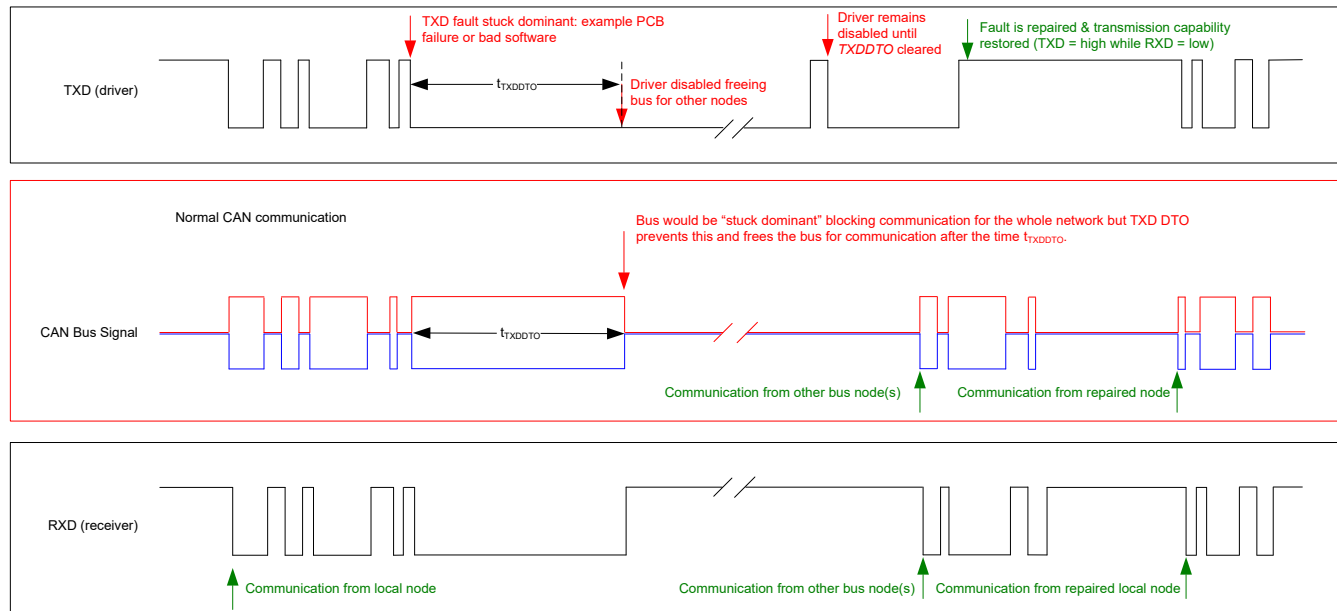
### 7.3.8 Local Faults

Local faults are detected in both normal mode and silent mode, but are only indicated via the nFAULT pin when the TCAN943-Q1 transitions from normal mode to silent mode. All other mode transitions clear the local fault flag indicators.

#### 7.3.8.1 TXD Dominant Timeout (TXD DTO)

While the CAN driver is in active mode a TXD dominant state timeout circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the timeout period,  $t > t_{TXDDTO}$ . The TXD dominant state timeout circuit is triggered by a falling edge on the TXD pin. If no rising edge is seen before on TXD before  $t > t_{TXDDTO}$  then the CAN driver is disabled releasing the bus lines to the recessive level. This keeps the bus free for communication between other nodes on the network.

The CAN driver is activated again once there is a mode transition, or once TXD is high while RXD is low. During a *TXDDTO* fault the high-speed receiver remains active and the RXD output pin mirrors the CAN bus.



**Figure 7-3. Timing Diagram for TXD DTO**

The minimum dominant TXD time allowed by the dominant state timeout circuit limits the minimum possible transmitted data rate of the transceiver. The CAN protocol allows a maximum of eleven successive dominant bits to be transmitted in the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate is calculated using the minimum  $t_{TXDDTO}$  time in [Equation 1](#).

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXDDTO} = 11 \text{ bits} / 1.2\text{ms} = 9.2\text{kbps} \quad (1)$$

#### 7.3.8.2 Thermal Shutdown (TSD)

If the junction temperature of the TCAN943-Q1 exceeds the thermal shutdown threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The CAN bus terminals are biased to recessive level during a *TSD* fault and the receiver to RXD path remains operational. The *TSD* fault condition is cleared when the junction temperature,  $T_J$ , of the device drops below the thermal shutdown release temperature,  $T_{SDF}$ , of the device and either a mode change into Normal, Standby, or Sleep mode occurs or  $TXD = H$  while  $RXD = L$ . If the fault condition that caused the *TSD* fault is still present, the temperature can rise again, and the device enters thermal shutdown again. Prolonged operation with *TSD* fault conditions can affect device reliability.

The TSD circuit includes hysteresis to avoid any oscillation of the driver output. During the fault the TSD fault condition is indicated to the CAN FD controller via the nFAULT terminal in Silent mode.

### 7.3.8.3 Undervoltage Lockout (UVLO)

The supply terminals,  $V_{SUP}$ ,  $V_{IO}$  and  $V_{CC}$ , are monitored for undervoltage events. If an undervoltage event occurs the TCAN943-Q1 enters a protected state where the bus pins present no load to the CAN bus. This protects the CAN bus and system from unwanted glitches and excessive current draw that can impact communication between other CAN nodes on the CAN bus.

If an undervoltage event occurs on  $V_{SUP}$  in any mode, the TCAN943-Q1 CAN transceiver enters the CAN off state.

If an undervoltage event occurs on  $V_{CC}$ , the TCAN943-Q1 remains in normal or silent mode but the CAN transceiver changes to the CAN passive state. During a  $UV_{CC}$  event, RXD remains high as long as  $V_{IO}$  is present and there is no wake-up event being signaled on RXD. The CAN bus is weakly biased to GND. If the undervoltage event persists longer than  $t_{UV}$ , the TCAN943-Q1 transitions to sleep mode.

If an undervoltage event occurs on the  $V_{IO}$ , the TCAN943-Q1 transitions to standby mode. If the undervoltage event persists longer than  $t_{UV}$ , the TCAN943-Q1 transitions to sleep mode.

Once an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically needs  $t_{MODE1}$  to transition to normal operation.

### 7.3.8.4 Unpowered Devices

The device is designed to be high-impedance to the CAN bus if the device is unpowered. The CANH and CANL pins have low leakage currents when the device is unpowered, so no load is present on the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The logic terminals also have low leakage currents when the device is unpowered, so there is not a load down other circuits which can remain powered.

### 7.3.8.5 Floating Terminals

The TCAN943-Q1 has internal pull-ups and pull-downs on critical pins to make sure a known operating behavior if the pins are left floating. See [Table 7-2](#) for the pin fail-safe biasing protection description.

**Table 7-2. Pin Fail-safe Biasing**

| PIN  | FAIL-SAFE PROTECTION | VALUE        | COMMENT                  |
|------|----------------------|--------------|--------------------------|
| TXD  | Recessive level      | 60k $\Omega$ | Weak pull-up to $V_{IO}$ |
| EN   | Low-power mode       |              | Weak pull-down to GND    |
| nSTB | Low-power mode       |              | Weak pull-down to GND    |

This internal bias must not be relied upon by design but rather a fail-safe option. Special care needs to be taken when the transceiver is used with a CAN FD controller that has open-drain outputs. The TCAN943-Q1 implements a weak internal pull-up resistor on the TXD pin. The bit timing requirements for CAN FD data rates require special consideration and the pull-up strength must be considered carefully when using open-drain outputs. An adequate external pull-up resistor must be used to make sure the TXD output of the CAN FD controller maintains proper bit timing input to the CAN device.

### 7.3.8.6 CAN Bus Short-Circuit Current Limiting

The TCAN943-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault.

During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current can be viewed either as the current during each bus state or as an average current. The average short-circuit current must be used when considering system power for the termination resistors and common-mode

choke. The percentage of time that the driver can be dominant is limited by the TXD dominant state timeout and the CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe spacing. These makes sure there is a minimum recessive time on the bus even if the data field contains a high percentage of dominant bits.

The short-circuit current of the bus depends on the ratio of recessive to dominant bits and the respective short-circuit currents. The average short-circuit current can be calculated using [Equation 2](#).

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (2)$$

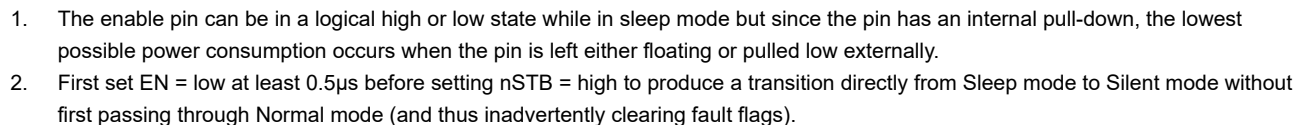
Where:

- $I_{OS(AVG)}$  is the average short-circuit current
- $\%Transmit$  is the percentage the node is transmitting CAN messages
- $\%Receive$  is the percentage the node is receiving CAN messages
- $\%REC\_Bits$  is the percentage of recessive bits in the transmitted CAN messages
- $\%DOM\_Bits$  is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$  is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$  is the dominant steady state short-circuit current

The short-circuit current and possible fault cases of the network must be taken into consideration when sizing the power ratings of the termination resistance and other network components.

## 7.4 Device Functional Modes

The TCAN943-Q1 has six operating modes: normal, standby, silent, go-to-sleep, sleep, and off mode. Operating mode selection is controlled using the nSTB pin and EN pin in conjunction with supply conditions, temperature conditions, and wake events.



### Table 7-3. TCAN943-Q1 Mode Overview

| MODE   | V <sub>CC</sub> and V <sub>IO</sub>       | V <sub>SUP</sub>    | EN   | nSTB | WAKERQ FLAG | DRIVER   | RECEIVER | RXD               | INH |
|--------|-------------------------------------------|---------------------|------|------|-------------|----------|----------|-------------------|-----|
| Normal | > UV <sub>CC</sub> and > UV <sub>IO</sub> | > UV <sub>SUP</sub> | High | High | X           | Enabled  | Enabled  | Mirrors bus state | On  |
| Silent | > UV <sub>CC</sub> and > UV <sub>IO</sub> | > UV <sub>SUP</sub> | Low  | High | X           | Disabled | Enabled  | Mirrors bus state | On  |



**Table 7-3. TCAN943-Q1 Mode Overview (continued)**

| MODE                       | V <sub>CC</sub> and V <sub>IO</sub>       | V <sub>SUP</sub>    | EN   | nSTB | WAKERQ FLAG | DRIVER   | RECEIVER                      | RXD                                          | INH               |
|----------------------------|-------------------------------------------|---------------------|------|------|-------------|----------|-------------------------------|----------------------------------------------|-------------------|
| Standby                    | > UV <sub>CC</sub> and > UV <sub>IO</sub> | > UV <sub>SUP</sub> | High | Low  | Set         | Disabled | Low power bus monitor enabled | Low signals wake-up                          | On                |
|                            | > UV <sub>CC</sub> and > UV <sub>IO</sub> | > UV <sub>SUP</sub> | Low  | Low  | X           | Disabled | Low power bus monitor enabled | Low signals wake-up                          | On                |
|                            | > UV <sub>CC</sub> and < UV <sub>IO</sub> | > UV <sub>SUP</sub> | Low  | Low  | X           | Disabled | Low power bus monitor enabled | High impedance                               | On                |
| Go-to-sleep <sup>(1)</sup> | > UV <sub>CC</sub> and > UV <sub>IO</sub> | > UV <sub>SUP</sub> | High | Low  | Cleared     | Disabled | Low power bus monitor enabled | High or high impedance (no V <sub>IO</sub> ) | On <sup>(2)</sup> |
| Sleep <sup>(3)</sup>       | > UV <sub>CC</sub> and > UV <sub>IO</sub> | > UV <sub>SUP</sub> | High | Low  | Cleared     | Disabled | Low power bus monitor enabled | High or high impedance (no V <sub>IO</sub> ) | High Impedance    |
|                            | < UV <sub>CC</sub> or < UV <sub>IO</sub>  | > UV <sub>SUP</sub> | X    | X    | X           | Disabled | Low power bus monitor enabled | High or high impedance (no V <sub>IO</sub> ) | High impedance    |
| Passive <sup>(4)</sup>     | < UV <sub>CC</sub> and > UV <sub>IO</sub> | > UV <sub>SUP</sub> | X    | High | X           | Disabled | Disabled                      | High                                         | On                |
| Protected                  | X                                         | < UV <sub>SUP</sub> | X    | X    | X           | Disabled | Disabled                      | High impedance                               | High impedance    |

- (1) Go-to-sleep: Transitional mode for EN = H, nSTB = L until t<sub>GOTOSLEEP</sub> timer has expired. The low-power bus monitor becomes/remains enabled in this state.
- (2) The INH pin transitions to high impedance once the t<sub>GOTOSLEEP</sub> timer has expired and the device transitions to Sleep mode.
- (3) Mode change from Go-to-Sleep mode to Sleep mode once t<sub>GOTOSLEEP</sub> timer has expired.
- (4) Passive mode is entered from Normal mode or Silent mode when a UV<sub>CC</sub> event occurs for t > t<sub>UV\_det</sub>. The device transitions from Passive mode to Sleep mode once the t<sub>UV</sub> timer has expired.

## 7.4.1 Operating Mode Description

### 7.4.1.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

Entering normal mode clears both the WAKERQ and the PWRON flags. If Normal mode is entered while TXD is low, the driver is not enabled until TXD becomes high, preventing glitches during state transitions or bus interruptions due to TXD faults.

### 7.4.1.2 Silent Mode

Silent mode is commonly referred to as listen only and receive only mode. In this mode, the CAN driver is disabled but the receiver is fully operational and CAN communication is unidirectional into the device. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD terminal.

In silent mode, PWRON and Local Failure flags are indicated on the nFAULT pin.

### 7.4.1.3 Standby Mode

Standby mode is a low-power mode where the driver and receiver are disabled, reducing current consumption. However, this is not the lowest power mode of the device since the INH terminal is on, allowing the rest of the system to resume normal operation.

During standby mode, a wake-up request (WAKERQ) is indicated by the RXD terminal being low. The wake-up source is identified via the nFAULT pin after the device is returned to normal mode.

### 7.4.1.4 Go-To-Sleep Mode

Go-to-sleep mode is the transitional mode of the device from any state to sleep. In this state, the driver and receiver are disabled, reducing the current consumption. The INH pin is active to supply an enable to the V<sub>IO</sub> controller which allows the rest of the system to operate normally. In this mode, the low-power bus monitor activates or remains active to monitor for bus wake-up events. If the device is held in this state for t ≥ t<sub>GOTOSLEEP</sub>, the device transitions to sleep mode and the INH turns off transitioning to the high impedance state.

If any wake-up events persist, the TCAN943-Q1 remains in standby mode until the device is switched into normal mode to clear the pending wake-up events.

#### 7.4.1.5 Sleep Mode

Sleep mode is the lowest power mode of the TCAN943-Q1. In sleep mode, the CAN transmitter and the main receiver are switched off, and the transceiver cannot send or receive data. The low power receiver is able to monitor the bus for any activity that validates the wake-up pattern (WUP) requirements, and the WAKE monitoring circuit monitors for state changes on the WAKE terminal for a local wake-up (LWU) event. The INH pin is switched off in sleep mode causing any system power supplies controlled by INH to be switched off thus reducing system power consumption.

Sleep mode is exited if:

- a valid wake-up pattern (WUP) is received via the CAN bus pins
- a local WAKE (LWU) event occurs
- nSTB becomes high while  $V_{IO} > UV_{IO}$  (the device enters Normal or Silent mode depending upon the logic level on the EN pin)

##### 7.4.1.5.1 Remote Wake Request via Wake-Up Pattern (WUP)

The TCAN943-Q1 implements a low-power wake receiver in the standby and sleep mode that uses the multiple filtered dominant wake-up pattern (WUP) defined in the ISO11898-2:2016 standard.

The wake-up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered dominant bus time. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive. Other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant. Other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant, the bus monitor recognizes the WUP and drives the RXD terminal low, if a valid  $V_{IO}$  is present signaling to the controller the wake-up request. If a valid,  $V_{IO}$  is not present when the wake-up pattern is received, the transceiver drives the RXD output pin low once  $V_{IO} > UV_{IO(R)}$  after  $t_{UV(RE-ENABLE)}$ .

The WUP consists of:

- A filtered dominant bus of at least  $t_{WK(FILTER)}$  followed by
- A filtered recessive bus time of at least  $t_{WK(FILTER)}$  followed by
- A second filtered dominant bus time of at least  $t_{WK(FILTER)}$

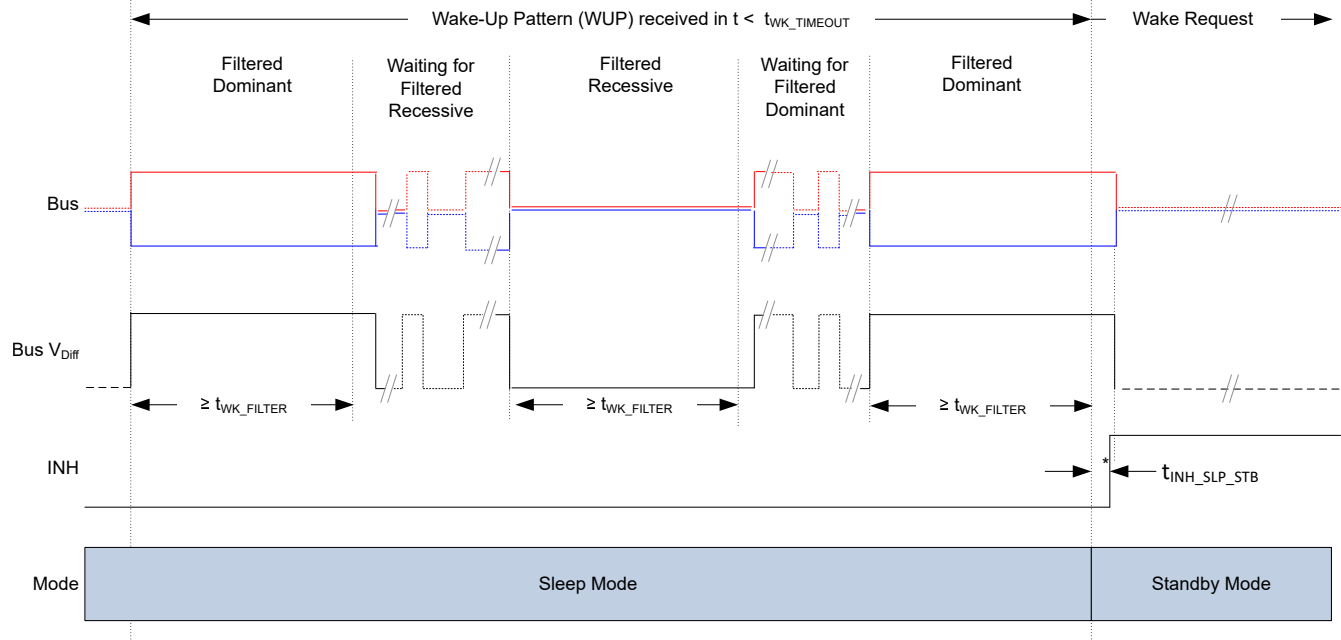
For a dominant or recessive to be considered “filtered,” the bus must be in that state for more than  $t_{WK(FILTER)}$  time. Due to variability in the  $t_{WK(FILTER)}$  the following scenarios are applicable. Bus state times less than the  $t_{WK(FILTER)}$  minimum are never detected as part of a WUP, and thus, no wake request is generated. Bus state times between  $t_{WK(FILTER)}$  minimum and  $t_{WK(FILTER)}$  maximum can be detected as part of a WUP and a wake request can be generated. Bus state times more than  $t_{WK(FILTER)}$  maximum is always detected as part of a WUP, and thus, a wake request is always generated. See [Figure 7-5](#) for the timing diagram of the WUP.

The pattern and  $t_{WK(FILTER)}$  time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

ISO11898-2:2024 has two sets of times for a short and long wake-up filter times. The  $t_{WK(FILTER)}$  timing for the TCAN943-Q1 has been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back to back bit times at 1Mbps trigger the filter in either bus state.

For an additional layer of robustness and to prevent false wake-ups, the transceiver implements the  $t_{WK(TIMEOUT)}$  timer. For a remote wake-up event to successfully occur, the entire wake-up pattern must be received within the timeout value. If the full wake-up pattern is not received before the  $t_{WK(TIMEOUT)}$  expires then the internal logic is reset and the transceiver remains in sleep mode without waking up. The full pattern must then be transmitted again within the  $t_{WK(TIMEOUT)}$  window. See [Figure 7-5](#).

A recessive bus of at least  $t_{WK(FILTER)}$  must separate the next WUP pattern if the CAN bus is dominant when the  $t_{WK(TIMEOUT)}$  expires.

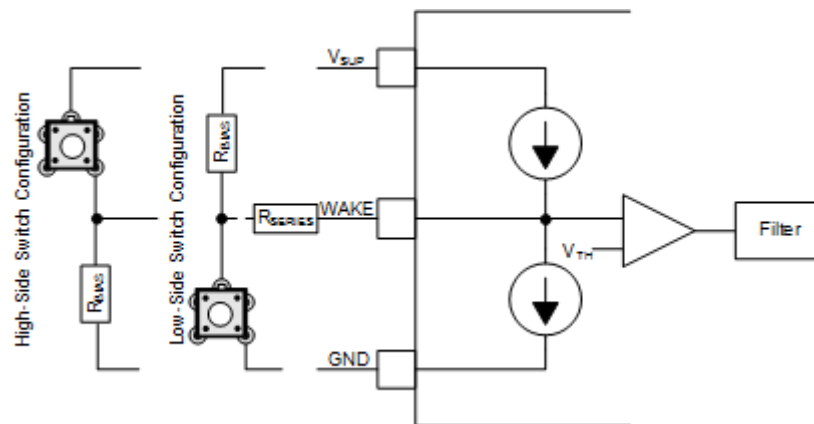


\*The RXD pin is only driven once  $V_{IO}$  is present.

**Figure 7-5. Wake-Up Pattern (WUP)**

#### 7.4.1.5.2 Local Wake-Up (LWU) by WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage reverse-battery protected input which can be used for local wake-up (LWU) requests through a voltage transition. A LWU event is triggered on either a low-to-high or high-to-low transition due to the bi-directional input thresholds. The WAKE pin can be used with a switch to  $V_{SUP}$ , to  $V_{CC}$ , to  $V_{IO}$ , or to ground. If the terminal is unused, the terminal must be pulled to supply or to ground to avoid unwanted parasitic wake-up events. Current consumption is minimized when WAKE is connected to 5V or to ground.



**Figure 7-6. WAKE Circuit Example**

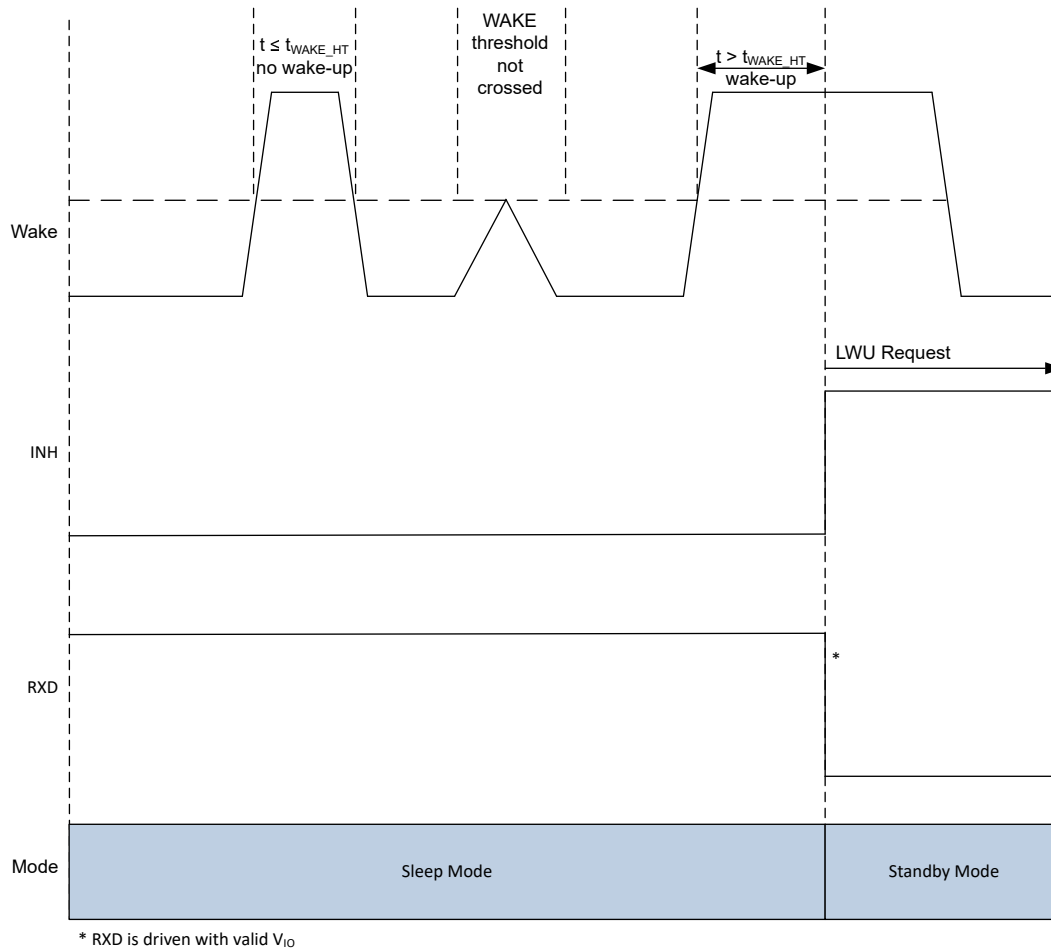
Figure 7-6 shows two possible configurations for the WAKE pin, a low-side and high-side switch configuration. The objective of the series resistor,  $R_{SERIES}$ , is to protect the WAKE input of the device from over current conditions that can occur in the event of a ground shift or ground loss. The minimum value of  $R_{SERIES}$  can be calculated using the maximum supply voltage,  $V_{SUPMAX}$ , and the maximum allowable current of the WAKE pin,  $I_{IO(WAKE)}$ .  $R_{SERIES}$  is calculated using:

$$R_{\text{SERIES}} = V_{\text{SUPMAX}} / I_{\text{IO(WAKE)}} \quad (3)$$

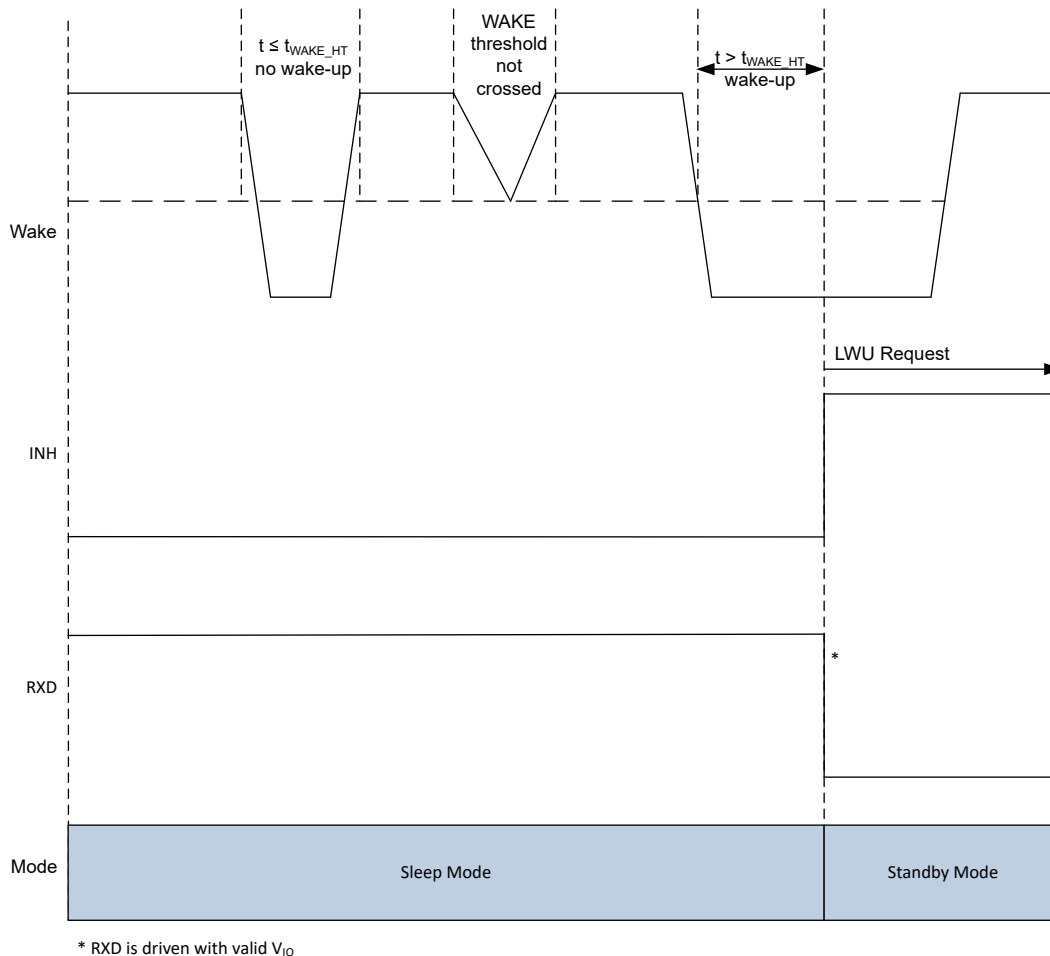
With absolute maximum voltage,  $V_{\text{SUPMAX}}$ , of 40V and maximum allowable  $I_{\text{IO(WAKE)}}$  of 3mA, the minimum required  $R_{\text{SERIES}}$  value is 13.3k $\Omega$ .

The LWU circuitry is active in Sleep mode and Standby mode.

The WAKE circuitry is switched off in Normal mode and Silent mode.



**Figure 7-7. LWU Request Rising Edge**



**Figure 7-8. LWU Request Falling Edge**

## 7.4.2 CAN Transceiver

### 7.4.2.1 CAN Transceiver Operation

The TCAN943-Q1 supports the ISO 11898-2:2024 CAN physical layer standard normal bus biasing scheme. Normal bus biasing means that the CAN bus is biased when the transceiver is in Normal mode or Silent mode. In other modes, the CAN pins are either high-impedance or weakly biased to GND.

#### 7.4.2.1.1 Driver and Receiver Function Tables

**Table 7-4. Driver Function Table**

| DEVICE MODE | TXD INPUTS <sup>(1)</sup> | BUS OUTPUTS    |                | DRIVEN BUS STATE <sup>(2)</sup> |
|-------------|---------------------------|----------------|----------------|---------------------------------|
|             |                           | CANH           | CANL           |                                 |
| Normal      | Low                       | High           | Low            | Dominant                        |
|             | High or Open              | High impedance | High impedance | $V_{CC}/2$                      |
| Silent      | x                         | High impedance | High impedance | $V_{CC}/2$                      |
| Standby     | x                         | High impedance | High impedance | Weak bias to GND                |
| Sleep       | x                         | High impedance | High impedance | Weak bias to GND                |

(1) x = irrelevant

(2) For bus states and typical bus voltages see [Figure 7-9](#)

**Table 7-5. Receiver Function Table**

| DEVICE MODE                        | CAN DIFFERENTIAL INPUTS<br>$V_{ID} = V_{CANH} - V_{CANL}$ | BUS STATE     | RXD TERMINAL                                               |
|------------------------------------|-----------------------------------------------------------|---------------|------------------------------------------------------------|
| Normal / Silent                    | $V_{ID} \geq 0.9V$                                        | Dominant      | Low                                                        |
|                                    | $0.5V < V_{ID} < 0.9V$                                    | Indeterminate | Indeterminate                                              |
|                                    | $V_{ID} \leq 0.5V$                                        | Recessive     | High                                                       |
|                                    | Open ( $V_{ID} \approx 0V$ )                              | Open          | High                                                       |
| Standby                            | $V_{ID} \geq 1.15V$                                       | Dominant      | High<br>Low if wake-up event persists                      |
|                                    | $0.4V < V_{ID} < 1.15V$                                   | Indeterminate |                                                            |
|                                    | $V_{ID} \leq 0.4$                                         | Recessive     |                                                            |
|                                    | Open ( $V_{ID} \approx 0V$ )                              | Open          |                                                            |
| Sleep / Go-to-sleep <sup>(1)</sup> | $V_{ID} \geq 1.15V$                                       | Dominant      | High<br>Tri-state if $V_{IO}$ or $V_{SUP}$ are not present |
|                                    | $0.4V < V_{ID} < 1.15V$                                   | Indeterminate |                                                            |
|                                    | $V_{ID} \leq 0.4V$                                        | Recessive     |                                                            |
|                                    | Open ( $V_{ID} \approx 0V$ )                              | Open          |                                                            |

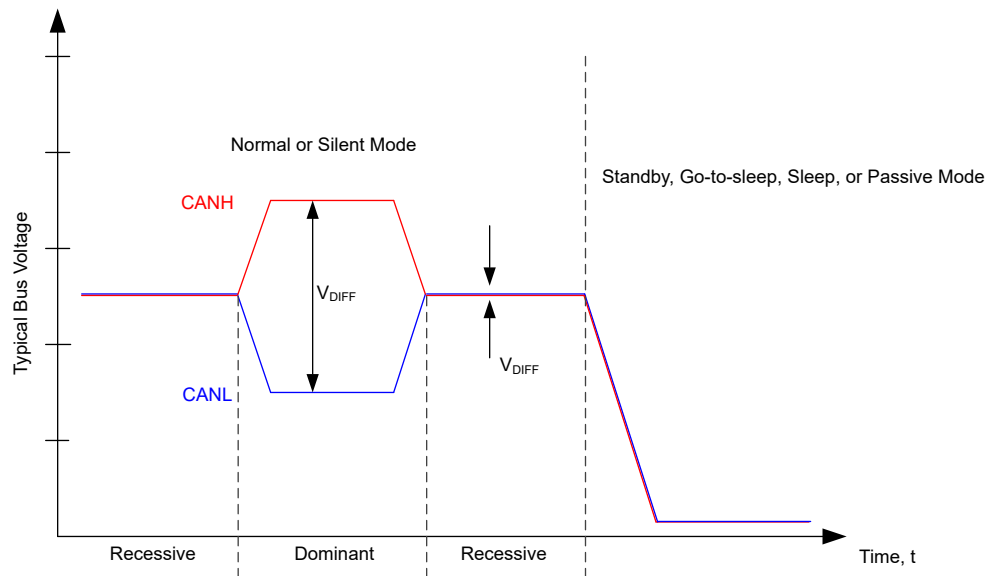
(1) Low power wake-up receiver is active

#### 7.4.2.1.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See [Figure 7-9](#).

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to one half of the CAN transceiver supply voltage via the high resistance internal input resistors ( $R_{IN}$ ) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes can be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the CAN bus is greater than the differential voltage of a single CAN driver. The TCAN943-Q1 CAN transceiver implements low-power standby and sleep modes which enable a third bus state where the bus pins are biased to ground via the high-resistance internal resistors of the receiver.



**Figure 7-9. Bus States**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.



Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2:2024 standard. These organization and standards made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

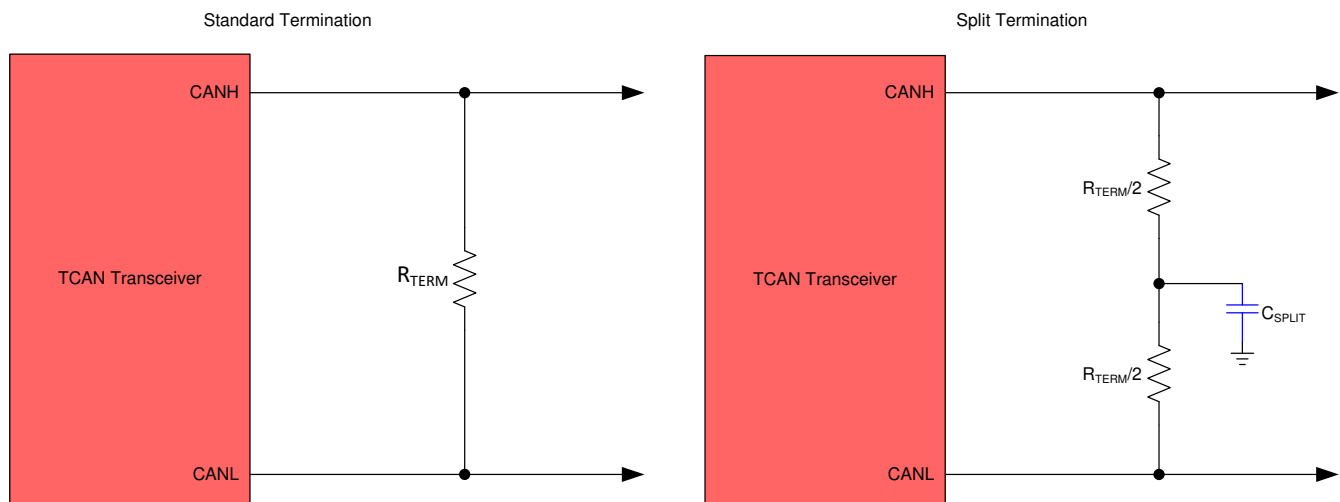
A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification the differential output driver is specified with a bus load that can range from  $50\Omega$  to  $65\Omega$  where the differential output must be greater than 1.5V. The TCAN943-Q1 is specified to meet the 1.5V requirement down to  $50\Omega$  and is specified to meet 1.4V differential output at  $45\Omega$  bus load. The differential input resistance,  $R_{ID}$ , of the TCAN943-Q1 is a minimum of  $50k\Omega$ . If 100 TCAN943-Q1 transceivers are in parallel on a bus, this is equivalent to a  $500\Omega$  differential load in parallel with the nominal  $60\Omega$  bus termination which gives a total bus load of approximately  $54\Omega$ . Therefore, the TCAN943-Q1 theoretically supports over 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length can also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths allowing for these system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for a robust network operation.

### 8.1.3 Detailed Design Procedure

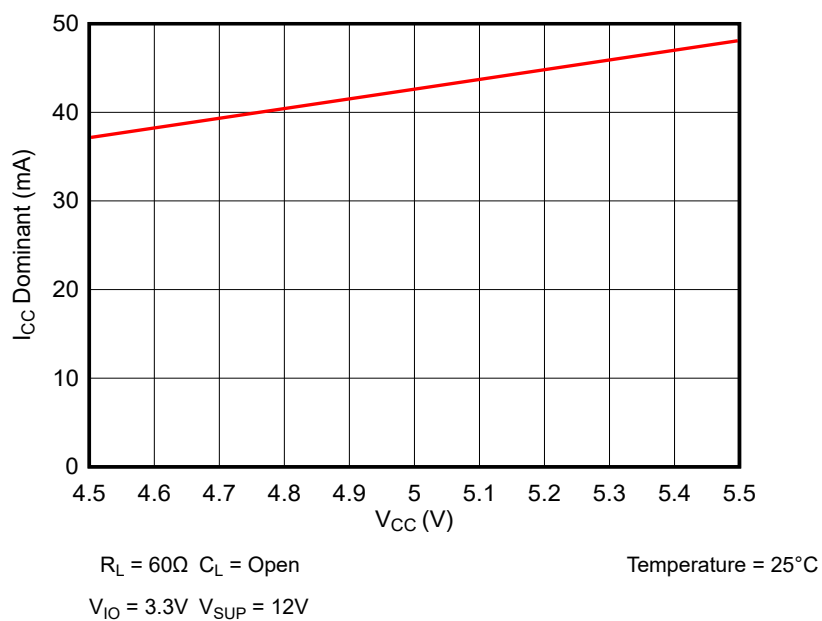
#### 8.1.3.1 CAN Termination

Termination can be a single  $120\Omega$  resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination can be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that can be present on the differential signal lines.



**Figure 8-2. CAN Bus Termination Concepts**

### 8.1.4 Application Curves



**Figure 8-3.  $I_{CC}$  Dominant over  $I_{CC}$  Supply Voltage**

## 8.2 Power Supply Recommendations

The TCAN943-Q1 is designed to operate off of three supply rails;  $V_{SUP}$ ,  $V_{CC}$ , and  $V_{IO}$ .  $V_{SUP}$  is a high-voltage supply pin designed to connect to the  $V_{BAT}$  rail,  $V_{CC}$  is a low-voltage supply pin with an input voltage range from 4.5V to 5.5V that supports the CAN transceiver and  $V_{IO}$  is a low-voltage supply pin with an input voltage range from 2.95V to 5.5V that provides the I/O voltage to match the system controller. For a reliable operation, a 100nF decoupling capacitor must be placed as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the output of switched-mode power supplies, and also helps to compensate for the resistance and inductance of the PCB power planes.

## 8.3 Layout

Robust and reliable CAN node design can require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques must be applied during PCB design.

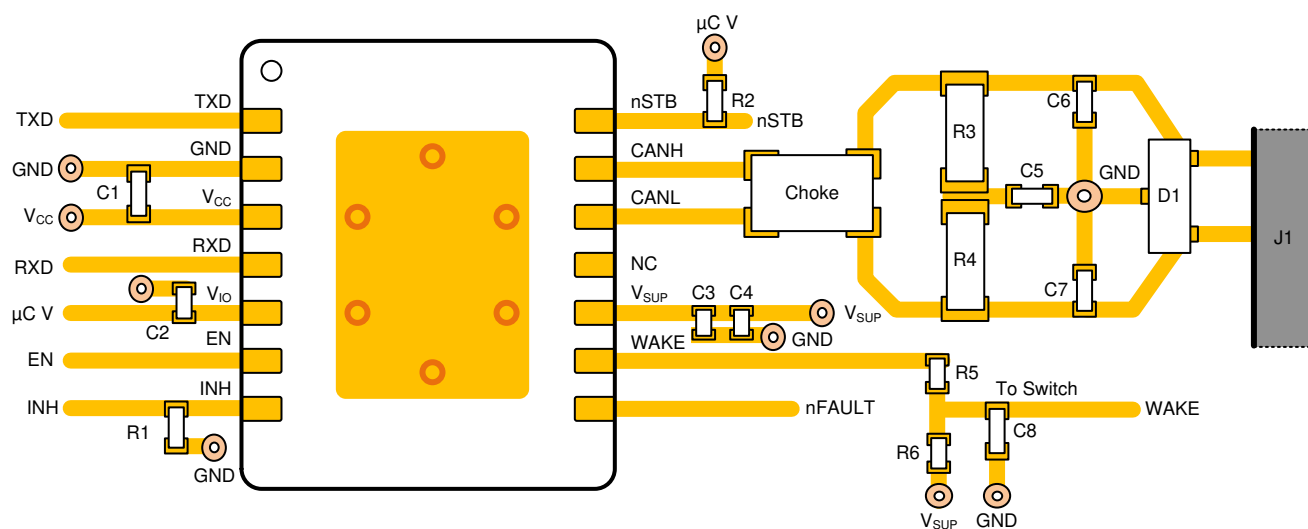
### 8.3.1 Layout Guidelines

The layout example provides information on components around the device. Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. Transient voltage suppression (TVS) device can be added for extra protection, shown as D1. The production solution can be either a bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C6 and C7. A series common-mode choke (CMC) is placed on the CANH and CANL lines between the device and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance. Note that high-frequency currents follow the path of least impedance and not the path of least resistance. Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors must be placed as close as possible to the supply terminals of transceiver, examples are C1 on  $V_{CC}$ , C2 on  $V_{IO}$ , and C3 and C4 on the  $V_{SUP}$  supply.
- $V_{IO}$  pin of the transceiver is connected to the microcontroller IO supply voltage ( $\mu C V$ ).
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R3 and R4, with the center or split tap of the termination connected to ground via capacitor C5. Split termination provides common-mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus; thus, also removing the termination.
- INH, pin 7, can have a 100k $\Omega$  resistor (R1) to ground.
- WAKE, pin 9, can recognize either a rising or a falling edge of a wake signal and is typically connected to an external switch. The pin must be configured as shown with C8 which is a 22nF capacitor to GND where R5 is 33k $\Omega$  and R6 is 3k $\Omega$ .

### 8.3.2 Layout Example



**Figure 8-4. Example Layout**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2024: Controller area network (CAN) - High-speed physical medium attachment sublayer
- SAE J2284-1: High-Speed CAN for Vehicle Applications at 125kbps
- SAE J2284-2: High-Speed CAN for Vehicle Applications at 250kbps
- SAE J2284-3: High-Speed CAN for Vehicle Applications at 500kbps
- SAE J2284-4: High-Speed CAN for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
- SAE J2284-5: High-Speed CAN for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE      | REVISION | NOTES           |
|-----------|----------|-----------------|
| July 2026 | *        | Initial Release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins            | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|---------------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">PTCAN943DMTRQ1</a> | Active        | Preproduction        | VSON (DMT)   14           | 3000   LARGE T&R      | -           | Call TI                              | Call TI                           | -40 to 150   |                     |
| <a href="#">PTCAN943DRQ1</a>   | Active        | Preproduction        | SOIC (D)   14             | 3000   LARGE T&R      | -           | Call TI                              | Call TI                           | -40 to 150   |                     |
| <a href="#">PTCAN943DYRQ1</a>  | Active        | Preproduction        | SOT-23-THIN<br>(DYY)   14 | 3000   LARGE T&R      | -           | Call TI                              | Call TI                           | -40 to 150   |                     |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

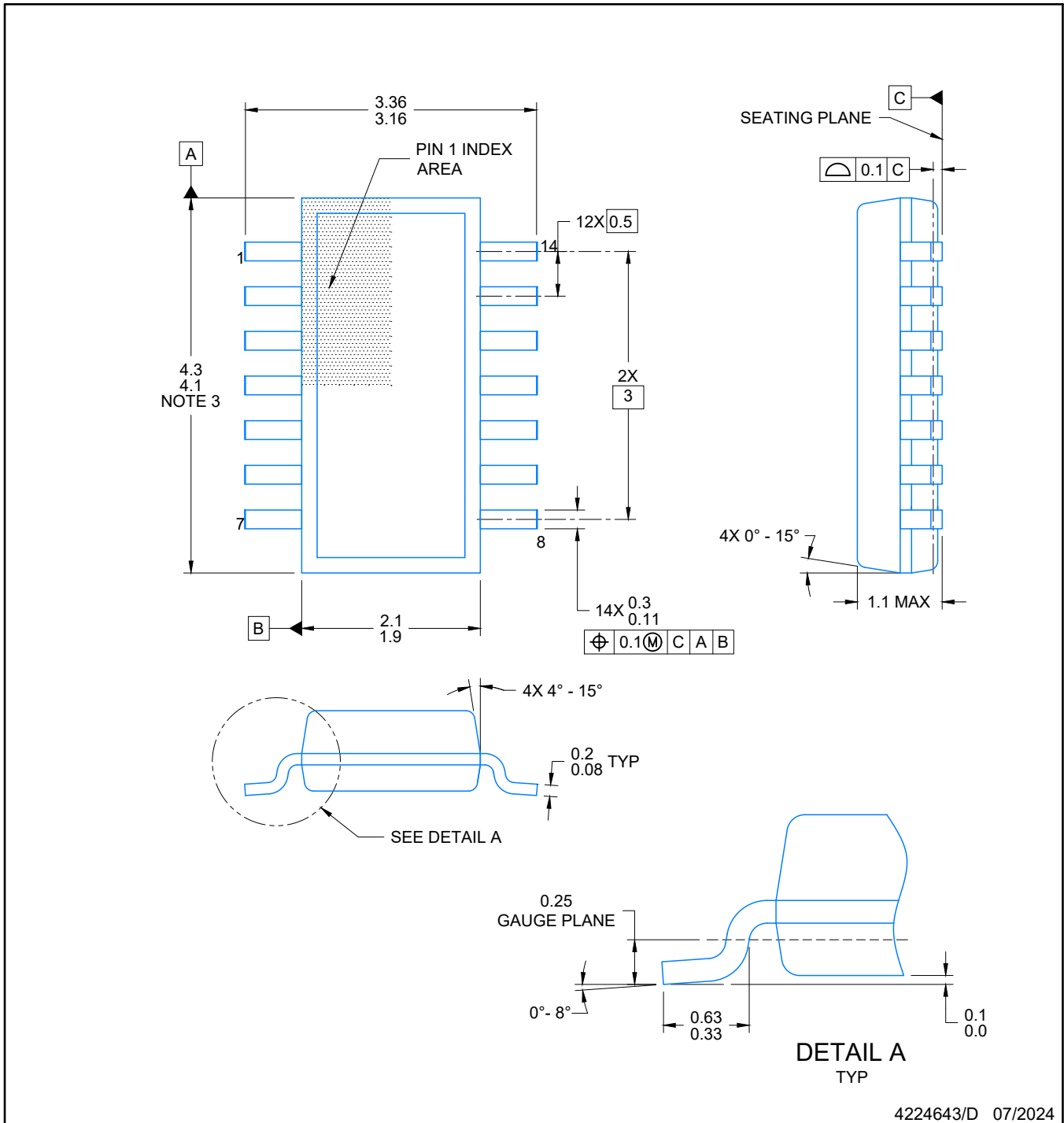
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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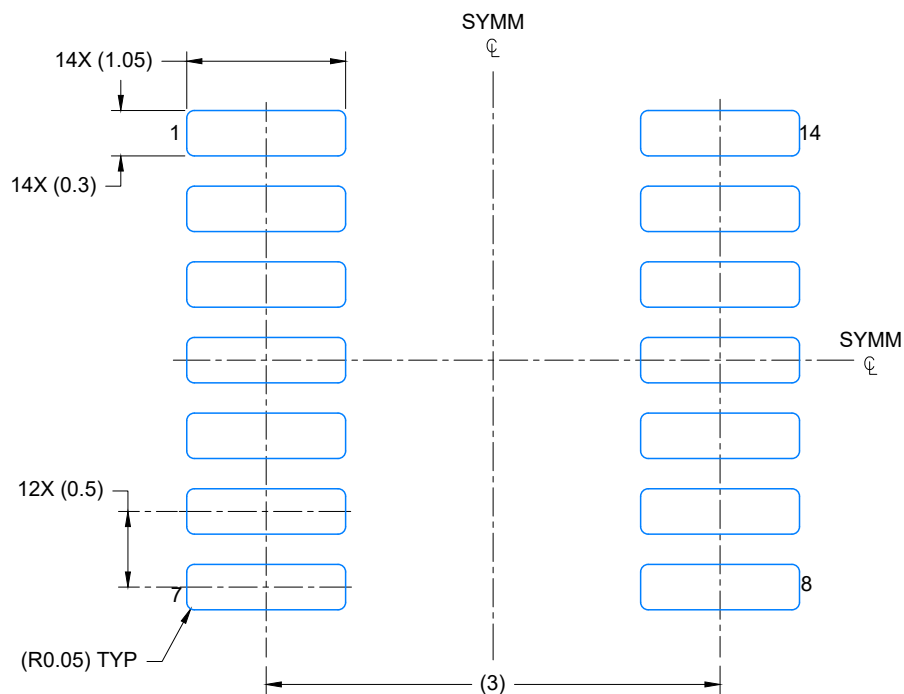
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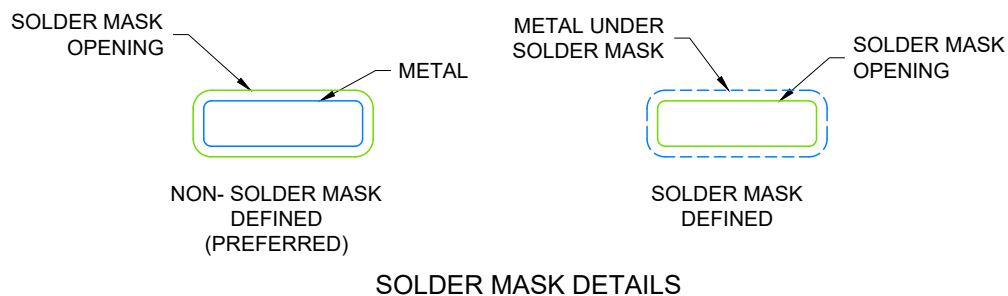
4224643/D 07/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

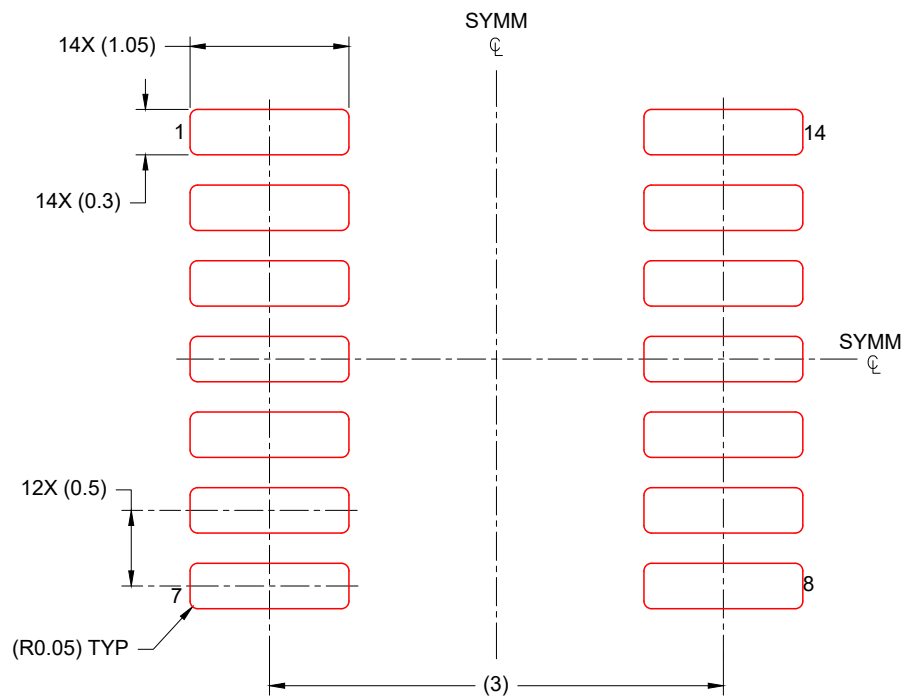


4224643/D 07/2024

## NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



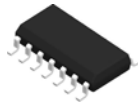


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 20X

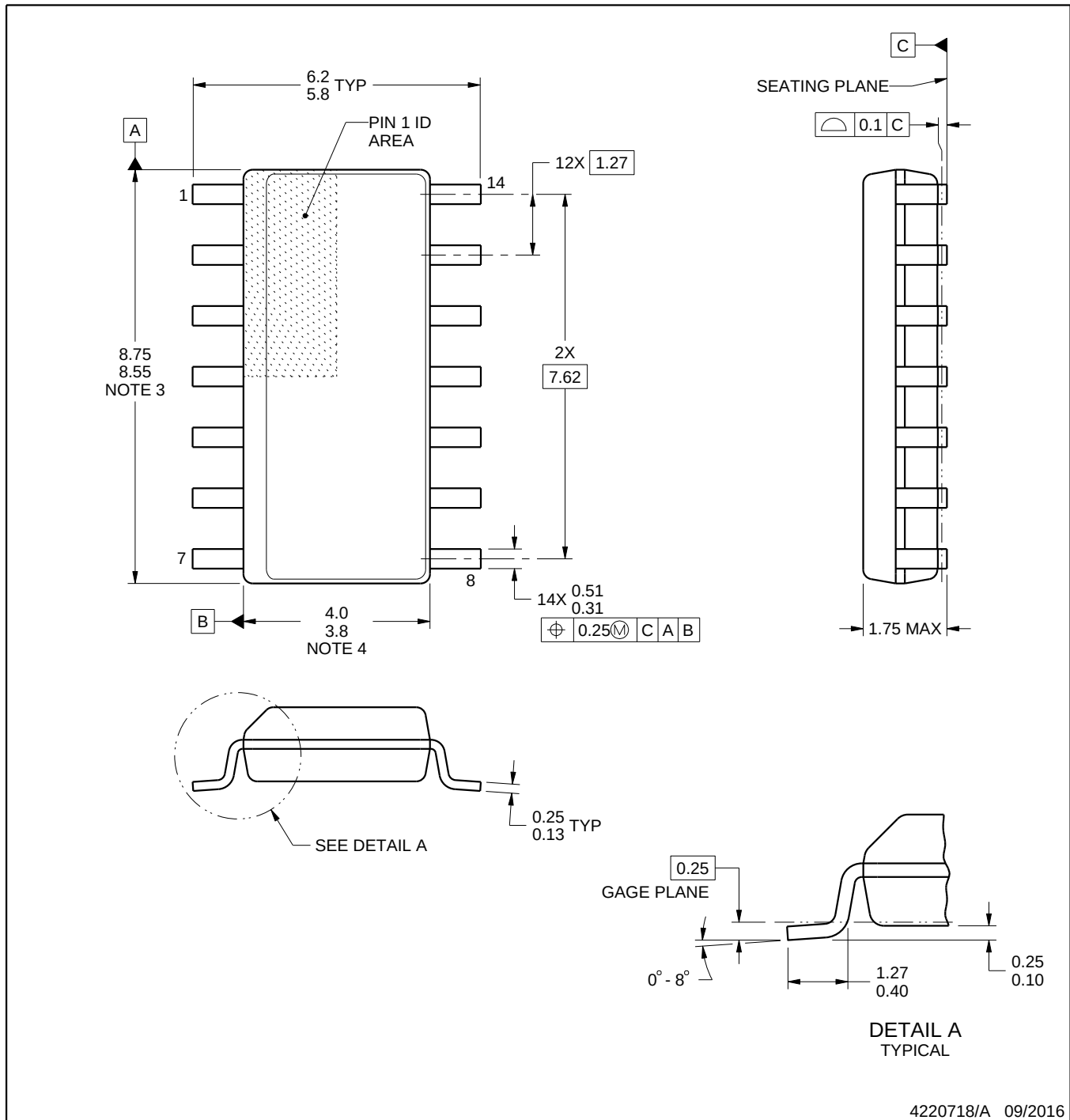
4224643/D 07/2024

## NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

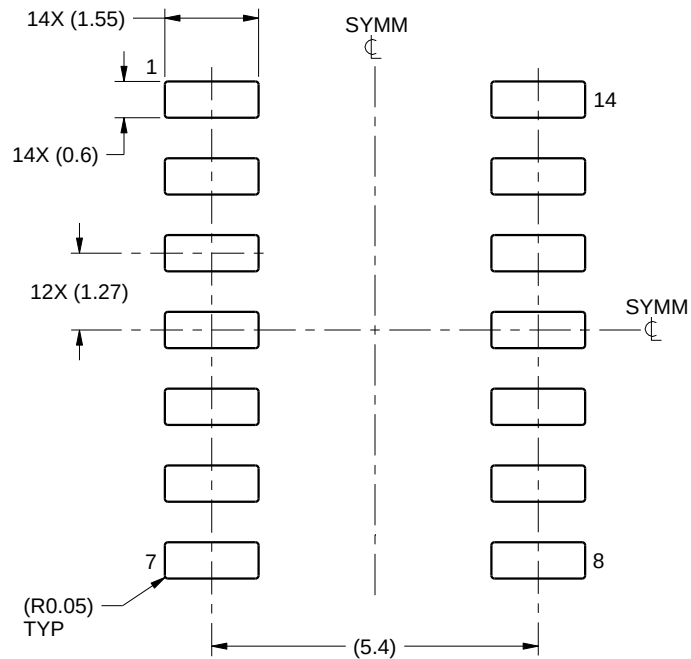
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

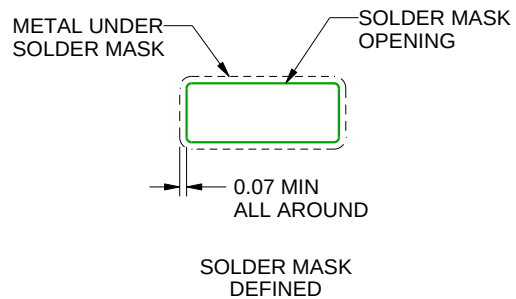
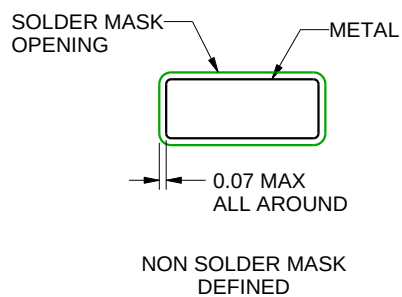
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

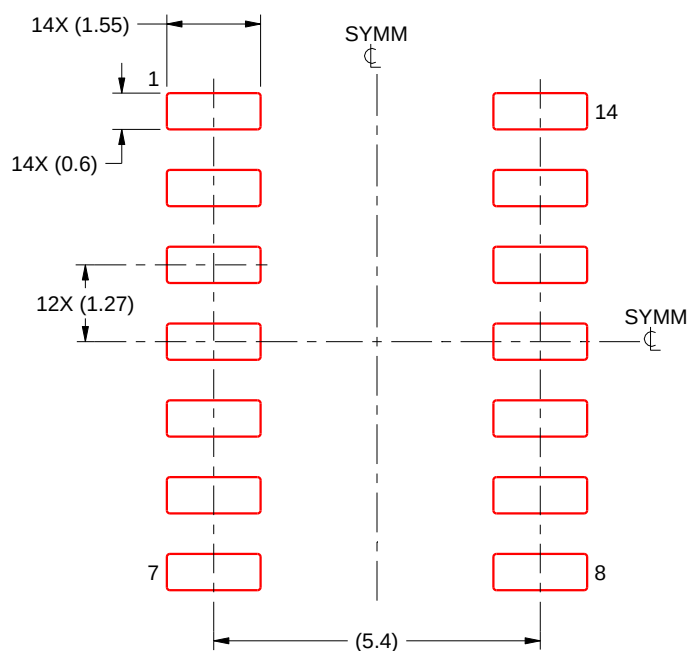
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

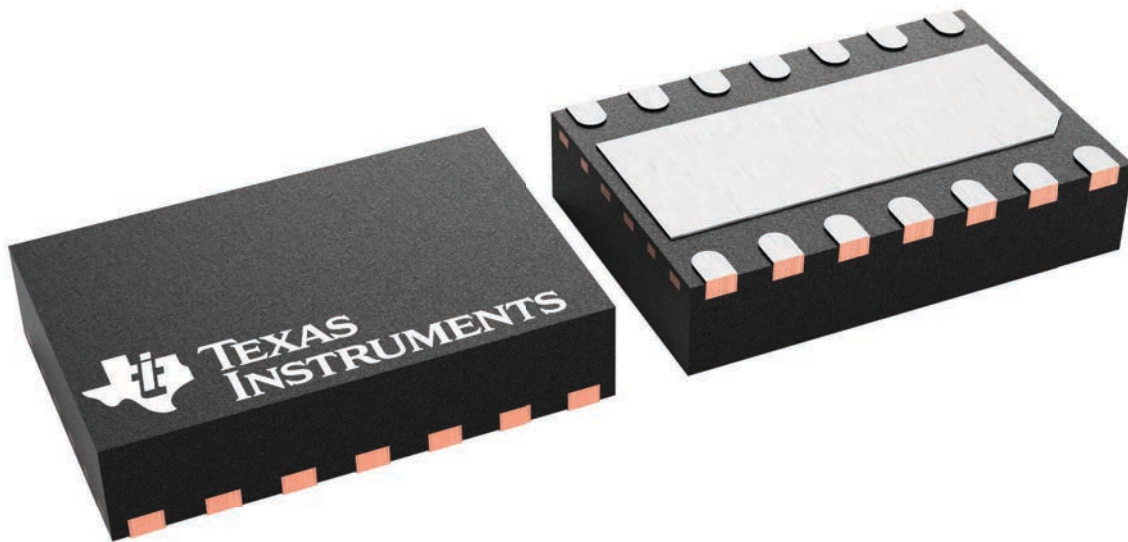
**DMT 14**

**VSON - 0.9 mm max height**

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

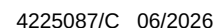


4225088/A



**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

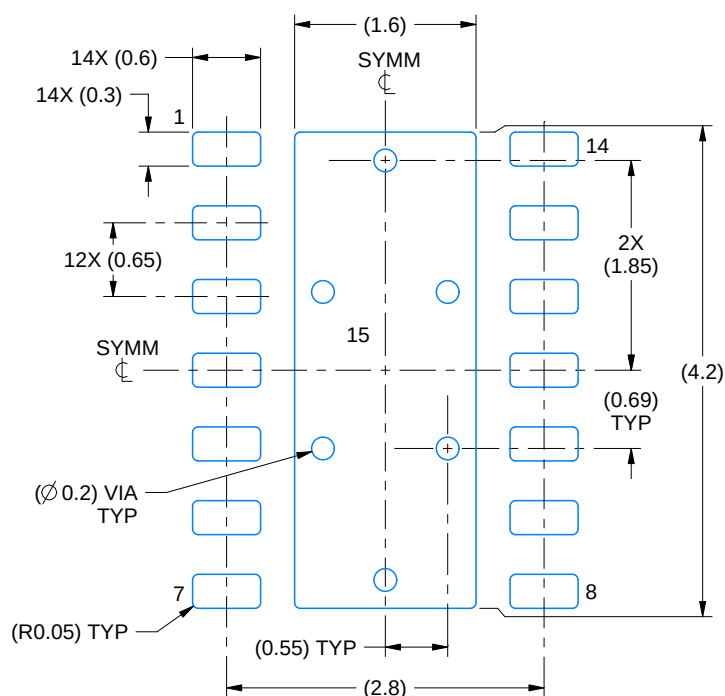


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed side wall metal may vary in shape, size and quantity.

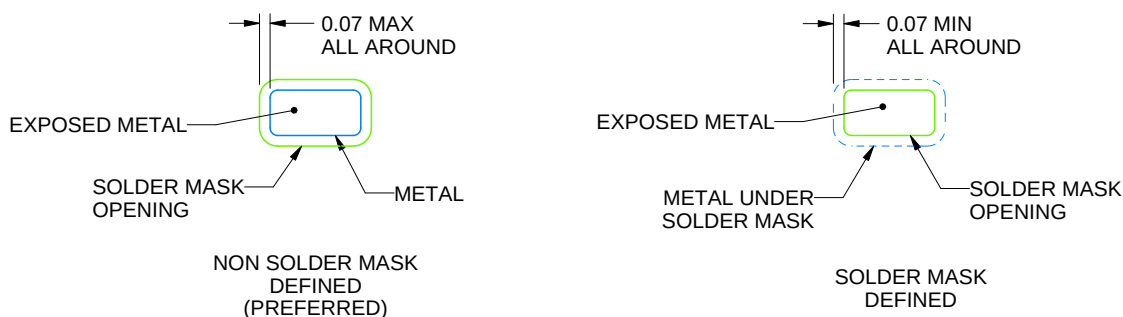
**DMT0014B**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



## SOLDER MASK DETAILS

4225087/C 06/2026

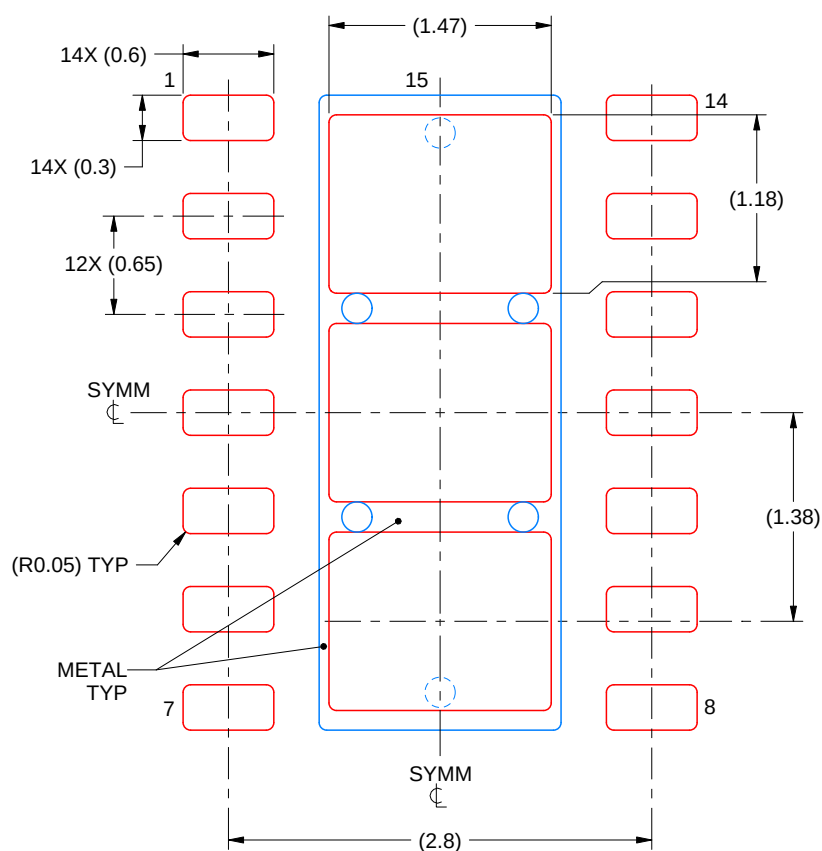
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DMT0014B**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15  
77.4% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4225087/C 06/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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