

## 160 W STEREO/300W MONO PurePath™ HD Analog-Input Power Stage

Check for Samples: [TAS5615](#)

### FEATURES

- **Active Enabled Integrated Feedback Provides: (PurePath™ HD Technology)**
  - Signal Bandwidth up to 80 kHz for High-Frequency Content From High-Definition Sources
  - Ultralow 0.03% THD at 1 W into 8  $\Omega$
  - 0.03% THD Across All Frequencies for Natural Sound at 1 W
  - 80-dB PSRR (BTL, No Input Signal)
  - >100-dB (A weighted) SNR
  - Click- and Pop-Free Start-Up
  - Minimal External Components Compared to Discrete Solutions
- **Multiple Configurations Possible on the Same PCB:**
  - Mono Parallel Bridge-Tied Load (PBTTL)
  - 2.1 Single-Ended (SE) Stereo Pair and Bridge-Tied Load (BTL) Subwoofer
  - Quad Single-Ended (SE) Outputs
- **Total Output Power at 10% THD+N**
  - 300 W in Mono PBTTL Configuration
  - 160 W per Channel in Stereo BTL
  - 80 W per Channel in Quad Single-Ended
- **High Efficiency Power Stage (> 90%) With 120 m $\Omega$  Output MOSFETs**
- **Two Thermally Enhanced Package Options:**
  - PHD (64-Pin QFP)
  - DKD (44-Pin PSOP3)
- **Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short-Circuit Protection) With Error Reporting**
- **EMI Compliant When Used With Recommended System Design**

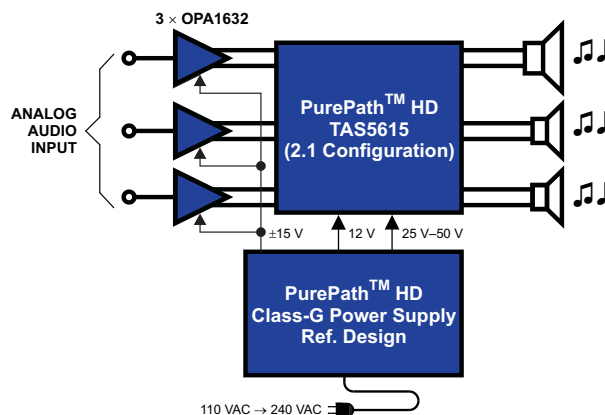
### DESCRIPTION

The TAS5615 is a high-performance analog input class-D amplifier with integrated closed-loop feedback technology (known as PurePath™ HD technology). It has the ability to drive up to 160 W<sup>(1)</sup> stereo into 8- $\Omega$  speakers from a single 50-V supply.

PurePath HD technology enables traditional AB-amplifier performance (<0.03% THD) levels while providing the power efficiency of traditional class-D amplifiers.

Ultralow 0.03% THD+N is flat across all frequencies, ensuring that the amplifier does not add uneven distortion characteristics, and helps maintain a natural sound.

The efficiency of this class-D amplifier is greater than 90%. Undervoltage protection, overtemperature, clipping, short-circuit and overcurrent protection are all integrated, safeguarding the device and speakers against fault conditions that could damage the system.



### APPLICATIONS

- Mini Combo System
- AV Receivers
- DVD Receivers
- Active Speakers

- (1) Achievable output power levels are dependent on the thermal configuration of the target application. A high performance thermal interface material between the package exposed heatslug and the heat sink should be used to achieve high output power levels



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

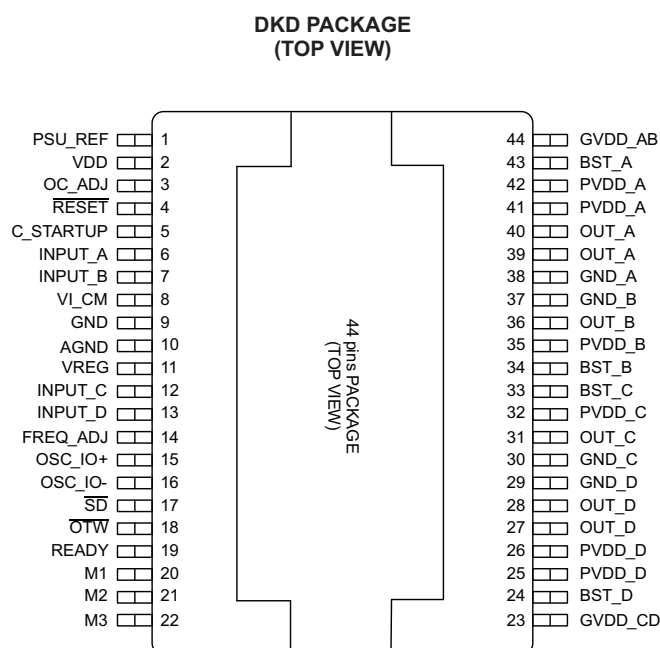
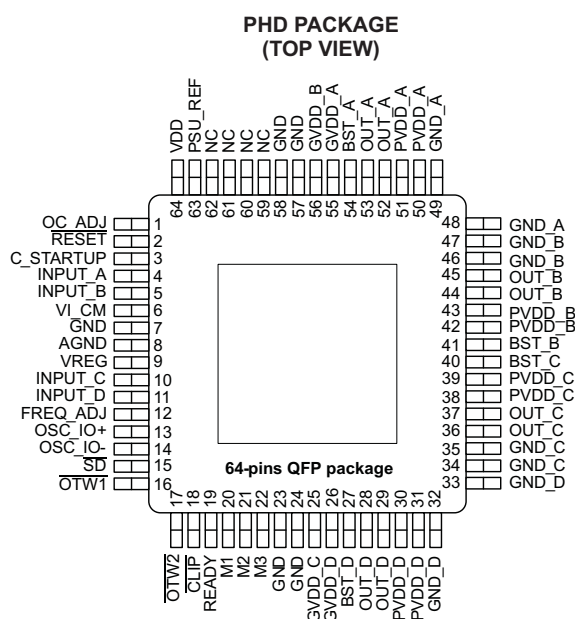
## DEVICE INFORMATION

### Terminal Assignment

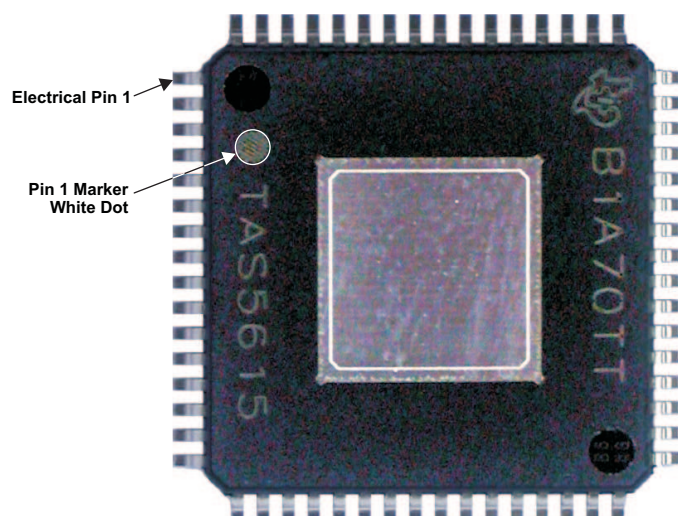
The TAS5615 is available in two thermally enhanced packages:

- 64-Pin QFP (PHD) Power Package
- 44-Pin PSOP3 package (DKD)

The package type contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.



### PIN ONE LOCATION PHD PACKAGE



## MODE SELECTION PINS

| MODE PINS |    |    | ANALOG INPUT              | OUTPUT CONFIGURATION | DESCRIPTION               |                        |         |
|-----------|----|----|---------------------------|----------------------|---------------------------|------------------------|---------|
| M3        | M2 | M1 |                           |                      |                           |                        |         |
| 0         | 0  | 0  | Differential              | 2 × BTL              | AD mode                   |                        |         |
| 0         | 0  | 1  | —                         | —                    | Reserved                  |                        |         |
| 0         | 1  | 0  | Differential              | 2 × BTL              | BD mode                   |                        |         |
| 0         | 1  | 1  | Differential Single-ended | 1 × BTL +2 × SE      | AD mode, BTL differential |                        |         |
| 1         | 0  | 0  | Single-ended              | 4 × SE               | AD mode                   |                        |         |
| 1         | 0  | 1  | Differential              | 1 × PBTL             | INPUT_C <sup>(1)</sup>    | INPUT_D <sup>(1)</sup> |         |
|           |    |    |                           |                      | 0                         | 0                      | AD mode |
|           |    |    |                           |                      | 1                         | 0                      | BD mode |
| 1         | 1  | 0  | Reserved                  |                      |                           |                        |         |
| 1         | 1  | 1  |                           |                      |                           |                        |         |

(1) INPUT\_C and \_D are used to select between a subset of AD and BD mode operations in PBTL mode (1 = VREG and 0 = AGND).

## PACKAGE HEAT DISSIPATION RATINGS<sup>(1)</sup>

| PARAMETER                                          | TAS5615PHD         | TAS5615DKD         |
|----------------------------------------------------|--------------------|--------------------|
| R <sub>θJC</sub> (°C/W) – 2 BTL or 4 SE channels   | 3.63               | 2.52               |
| R <sub>θJC</sub> (°C/W) – 1 BTL or 2 SE channel(s) | 5.95               | 3.22               |
| R <sub>θJC</sub> (°C/W) – 1 SE channel             | 9.9                | 6.9                |
| Pad area <sup>(2)</sup>                            | 49 mm <sup>2</sup> | 80 mm <sup>2</sup> |

(1) J<sub>C</sub> is junction-to-case, CH is case-to-heat sink

(2) R<sub>θH</sub> is an important consideration. Assume a 2-mil thickness of typical thermal grease between the pad area and the heat sink and both channels active. The R<sub>θCH</sub> with this condition is 1.22°C/W for the PHD package and 1.02°C/W for the DKD package.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

| T <sub>A</sub> | PACKAGE    | DESCRIPTION  |
|----------------|------------|--------------|
| 0°C–70°C       | TAS5615PHD | 64-pin HTQFP |
| 0°C–70°C       | TAS5615DKD | 44-pin PSOP3 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

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## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted <sup>(1)</sup>

| TAS5615                                                                           |                                                | UNIT |
|-----------------------------------------------------------------------------------|------------------------------------------------|------|
| VDD to AGND                                                                       | –0.3 to 13.2                                   | V    |
| GVDD to AGND                                                                      | –0.3 to 13.2                                   | V    |
| PVDD_X to GND_X <sup>(2)</sup>                                                    | –0.3 to 69.0                                   | V    |
| OUT_X to GND_X <sup>(2)</sup>                                                     | –0.3 to 69.0                                   | V    |
| BST_X to GND_X <sup>(2)</sup>                                                     | –0.3 to 82.2                                   | V    |
| BST_X to GVDD_X <sup>(2)</sup>                                                    | –0.3 to 69.0                                   | V    |
| VREG to AGND                                                                      | –0.3 to 4.2                                    | V    |
| GND_X to GND                                                                      | –0.3 to 0.3                                    | V    |
| GND_X to AGND                                                                     | –0.3 to 0.3                                    | V    |
| OC_ADJ, M1, M2, M3, OSC_IO+, OSC_IO–, FREQ_ADJ, VI_CM, C_STARTUP, PSU_REF to AGND | –0.3 to 4.2                                    | V    |
| INPUT_X                                                                           | –0.3 to 5                                      | V    |
| RESET, SD, OTW1, OTW2, CLIP, READY to AGND                                        | –0.3 to 7.0                                    | V    |
| Continuous sink current (SD, OTW1, OTW2, CLIP, READY)                             | 9                                              | mA   |
| Operating junction temperature range, T <sub>J</sub>                              | 0 to 150                                       | °C   |
| Storage temperature, T <sub>stg</sub>                                             | –40 to 150                                     | °C   |
| Electrostatic discharge                                                           | Human-body model <sup>(3)</sup> (all pins)     | ±2   |
|                                                                                   | Charged-device model <sup>(3)</sup> (all pins) | ±500 |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.
- (3) Failure to follow good anti-static ESD handling during manufacture and rework contributes to device malfunction. Make sure the operators handling the device are adequately grounded through the use of ground straps or alternative ESD protection.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                            |                                                                                |                                                                               | MIN  | NOM | MAX  | UNIT |
|----------------------------|--------------------------------------------------------------------------------|-------------------------------------------------------------------------------|------|-----|------|------|
| PVDD_x                     | Half-bridge supply                                                             | DC supply voltage                                                             | 25   | 50  | 52.5 | V    |
| GVDD_x                     | Supply for logic regulators and gate-drive circuitry                           | DC supply voltage                                                             | 10.8 | 12  | 13.2 | V    |
| VDD                        | Digital regulator supply voltage                                               | DC supply voltage                                                             | 10.8 | 12  | 13.2 | V    |
| R <sub>L</sub> (BTL)       | Load impedance                                                                 | Output filter according to schematics in the application information section. | 7    | 8.0 |      | Ω    |
| R <sub>L</sub> (SE)        |                                                                                |                                                                               | 3.5  | 4.0 |      |      |
| R <sub>L</sub> (PBTL)      |                                                                                |                                                                               | 3.5  | 4.0 |      |      |
| L <sub>OUTPUT</sub> (BTL)  | Output filter inductance                                                       | Minimum output inductance at I <sub>OC</sub>                                  | 14   | 15  |      | μH   |
| L <sub>OUTPUT</sub> (SE)   |                                                                                |                                                                               | 14   | 15  |      |      |
| L <sub>OUTPUT</sub> (PBTL) |                                                                                |                                                                               | 14   | 15  |      |      |
| f <sub>PWM</sub>           | PWM frame rate selectable for AM interference avoidance; 1% resistor tolerance | Nominal                                                                       | 385  | 400 | 415  | kHz  |
|                            |                                                                                | AM1                                                                           | 315  | 333 | 350  |      |
|                            |                                                                                | AM2                                                                           | 260  | 300 | 335  |      |
| R <sub>FREQ_ADJ</sub>      | PWM frame-rate programming resistor                                            | Nominal; master mode                                                          | 9.9  | 10  | 10.1 | kΩ   |
|                            |                                                                                | AM1; master mode                                                              | 19.8 | 20  | 20.2 |      |
|                            |                                                                                | AM2; master mode                                                              | 29.7 | 30  | 30.3 |      |
| V <sub>FREQ_ADJ</sub>      | Voltage on FREQ_ADJ pin for slave mode operation                               | Slave mode                                                                    | 3.3  |     |      |      |
| T <sub>J</sub>             | Junction temperature                                                           |                                                                               | 0    |     | 150  | °C   |

### PIN FUNCTIONS

| PIN       |                   |         | FUNCTION <sup>(1)</sup> | DESCRIPTION                                                                                                                               |
|-----------|-------------------|---------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| NAME      | PHD NO.           | DKD NO. |                         |                                                                                                                                           |
| AGND      | 8                 | 10      | P                       | Analog ground                                                                                                                             |
| BST_A     | 54                | 43      | P                       | HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_A required                                                                  |
| BST_B     | 41                | 34      | P                       | HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_B required                                                                  |
| BST_C     | 40                | 33      | P                       | HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_C required                                                                  |
| BST_D     | 27                | 24      | P                       | HS bootstrap supply (BST), external 0.033-μF capacitor to OUT_D required                                                                  |
| /CLIP     | 18                | –       | O                       | Clipping warning; open drain; active-low                                                                                                  |
| C_STARTUP | 3                 | 5       | O                       | Startup ramp requires a charging capacitor of 4.7 nF to AGND.                                                                             |
| FREQ_ADJ  | 12                | 14      | I                       | PWM frame-rate programming pin requires resistor to AGND.                                                                                 |
| GND       | 7, 23, 24, 57, 58 | 9       | P                       | Ground                                                                                                                                    |
| GND_A     | 48, 49            | 38      | P                       | Power ground for half-bridge A                                                                                                            |
| GND_B     | 46, 47            | 37      | P                       | Power ground for half-bridge B                                                                                                            |
| GND_C     | 34, 35            | 30      | P                       | Power ground for half-bridge C                                                                                                            |
| GND_D     | 32, 33            | 29      | P                       | Power ground for half-bridge D                                                                                                            |
| GVDD_A    | 55                | –       | P                       | Gate-drive voltage supply requires 0.1-μF capacitor to GND_A.                                                                             |
| GVDD_B    | 56                | –       | P                       | Gate-drive voltage supply requires 0.1-μF capacitor to GND_B.                                                                             |
| GVDD_C    | 25                | –       | P                       | Gate-drive voltage supply requires 0.1-μF capacitor to GND_C.                                                                             |
| GVDD_D    | 26                | –       | P                       | Gate-drive voltage supply requires 0.1-μF capacitor to GND_D.                                                                             |
| GVDD_AB   | –                 | 44      | P                       | Gate-drive voltage supply requires 0.22-μF capacitor to GND_A/GND_B.                                                                      |
| GVDD_CD   | –                 | 23      | P                       | Gate-drive voltage supply requires 0.22-μF capacitor to GND_C/GND_D.                                                                      |
| INPUT_A   | 4                 | 6       | I                       | Input signal for half bridge A                                                                                                            |
| INPUT_B   | 5                 | 7       | I                       | Input signal for half bridge B                                                                                                            |
| INPUT_C   | 10                | 12      | I                       | Input signal for half bridge C                                                                                                            |
| INPUT_D   | 11                | 13      | I                       | Input signal for half bridge D                                                                                                            |
| M1        | 20                | 20      | I                       | Mode selection                                                                                                                            |
| M2        | 21                | 21      | I                       | Mode selection                                                                                                                            |
| M3        | 22                | 22      | I                       | Mode selection                                                                                                                            |
| NC        | 59–62             | –       | –                       | No connect; pins may be grounded.                                                                                                         |
| OC_ADJ    | 1                 | 3       | O                       | Analog overcurrent-programming pin requires resistor to ground:<br>64 pin QFP package (PHD) = 22 kΩ<br>44 pin PSOP3 Package (DKD) = 24 kΩ |
| OSC_IO+   | 13                | 15      | I/O                     | Oscillator master/slave output/input                                                                                                      |
| OSC_IO–   | 14                | 16      | I/O                     | Oscillator master/slave output/input                                                                                                      |
| /OTW      | –                 | 18      | O                       | Overtemperature warning signal, open-drain, active-low                                                                                    |
| /OTW1     | 16                | –       | O                       | Overtemperature warning signal, open-drain, active-low                                                                                    |
| /OTW2     | 17                | –       | O                       | Overtemperature warning signal, open-drain, active-low                                                                                    |
| OUT_A     | 52, 53            | 39, 40  | O                       | Output, half bridge A                                                                                                                     |
| OUT_B     | 44, 45            | 36      | O                       | Output, half bridge B                                                                                                                     |
| OUT_C     | 36, 37            | 31      | O                       | Output, half bridge C                                                                                                                     |
| OUT_D     | 28, 29            | 27, 28  | O                       | Output, half bridge D                                                                                                                     |
| PSU_REF   | 63                | 1       | P                       | PSU reference requires close decoupling of 330 pF to AGND.                                                                                |
| PVDD_A    | 50, 51            | 41, 42  | P                       | Power supply input for half-bridge A requires close decoupling of 2.2-μF capacitor to GND_A.                                              |
| PVDD_B    | 42, 43            | 35      | P                       | Power supply input for half-bridge B requires close decoupling of 2.2-μF capacitor to GND_B.                                              |
| PVDD_C    | 38, 39            | 32      | P                       | Power supply input for half-bridge C requires close decoupling of 2.2-μF capacitor to GND_C.                                              |

(1) I = Input, O = Output, P = Power

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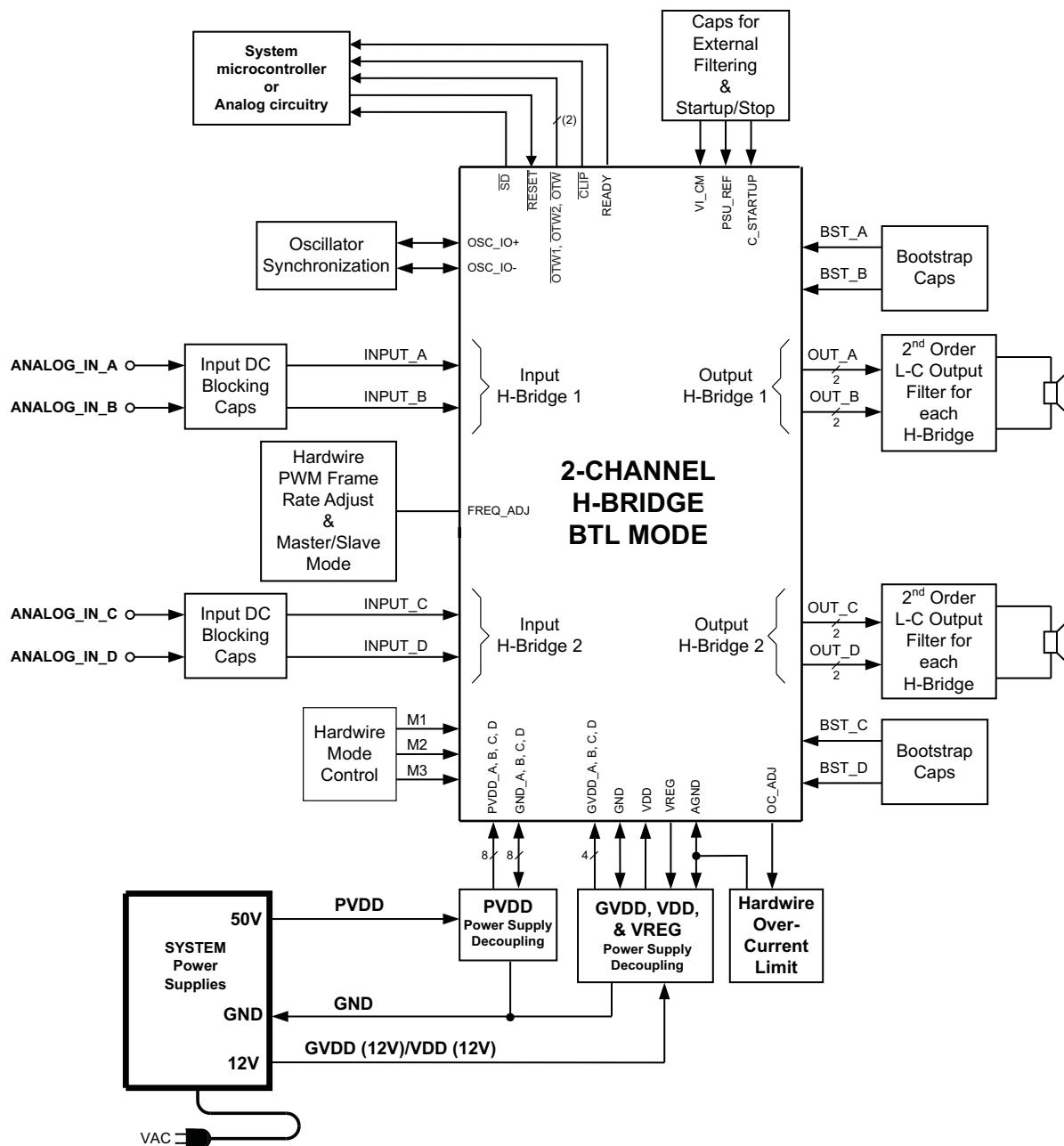
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## PIN FUNCTIONS (continued)

| PIN                       |         |         | FUNCTION <sup>(1)</sup> | DESCRIPTION                                                                                                           |
|---------------------------|---------|---------|-------------------------|-----------------------------------------------------------------------------------------------------------------------|
| NAME                      | PHD NO. | DKD NO. |                         |                                                                                                                       |
| PVDD_D                    | 30, 31  | 25, 26  | P                       | Power supply input for half-bridge D requires close decoupling of 2.2-μF capacitor to GND_D.                          |
| READY                     | 19      | 19      | O                       | Normal operation; open drain; active-high                                                                             |
| $\overline{\text{RESET}}$ | 2       | 4       | I                       | Device reset input, active-low; requires 47-kΩ pullup resistor to VREG                                                |
| $\overline{\text{SD}}$    | 15      | 17      | O                       | Shutdown signal, open-drain, active-low                                                                               |
| VDD                       | 64      | 2       | P                       | Power supply for internal voltage regulator requires a 10-μF capacitor with a 0.1-μF capacitor to GND for decoupling. |
| VI_CM                     | 6       | 8       | O                       | Analog comparator reference node requires close decoupling of 1 nF to GND.                                            |
| VREG                      | 9       | 11      | P                       | Internal regulator supply filter pin requires 0.1-μF capacitor to GND.                                                |

## TYPICAL SYSTEM BLOCK DIAGRAM

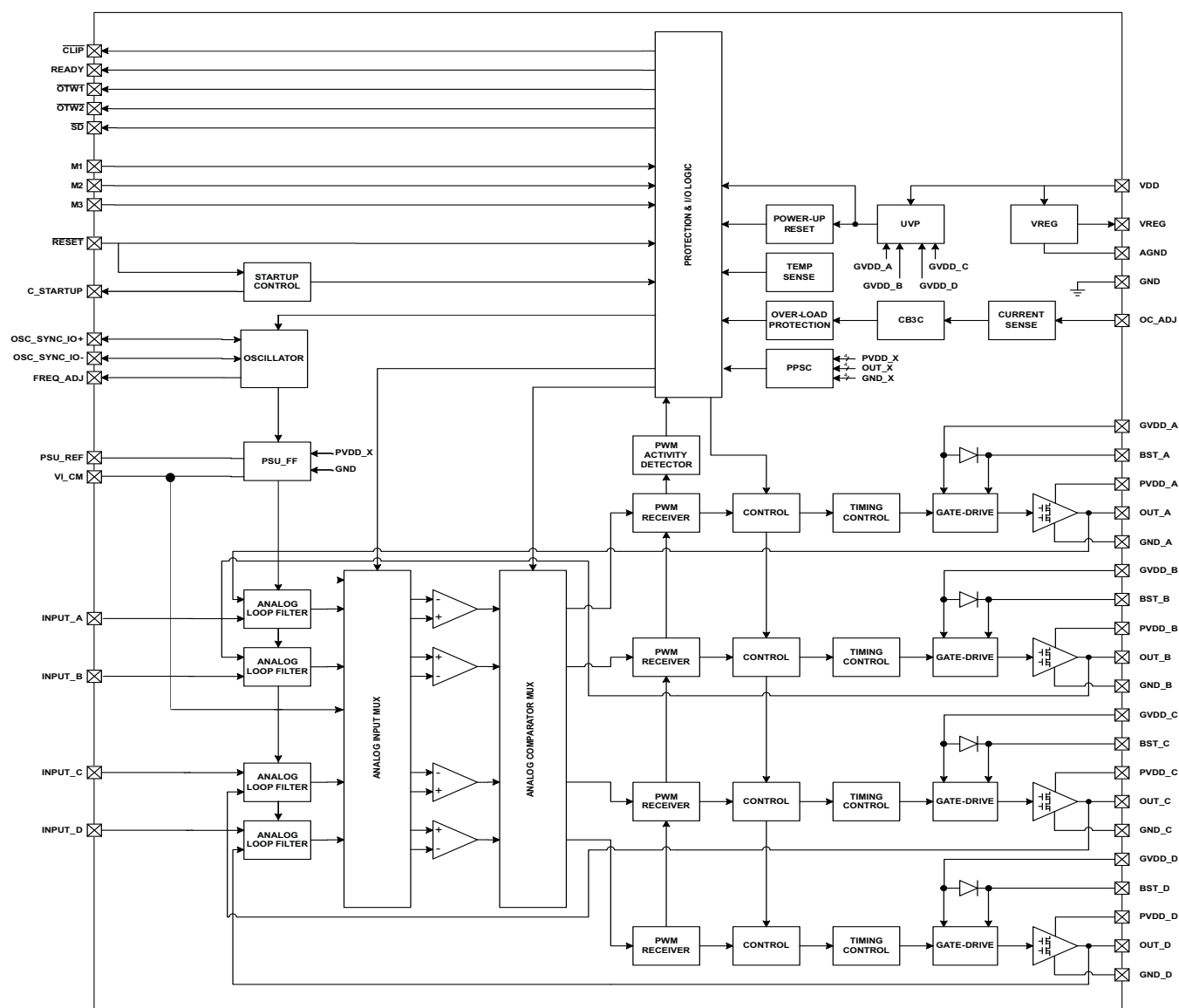


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## FUNCTIONAL BLOCK DIAGRAM



## AUDIO CHARACTERISTICS (BTL)

PCB and system configuraton are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD\_X = 50 V, GVDD\_X = 12 V,  $R_L = 8\ \Omega$ ,  $f_s = 400\ \text{kHz}$ ,  $R_{OC} = 22\ \text{k}\Omega$ ,  $T_C = 75^\circ\text{C}$ , output filter:  $L_{DEM} = 15\ \mu\text{H}$ ,  $C_{DEM} = 680\ \text{nF}$ , mode = 010, unless otherwise noted.

| PARAMETER         |                                                             | TEST CONDITIONS                                         | MIN | TYP  | MAX | UNIT          |
|-------------------|-------------------------------------------------------------|---------------------------------------------------------|-----|------|-----|---------------|
| P <sub>O</sub>    | Power output per channel                                    | $R_L = 8\ \Omega$ , 10% THD+N, clipped output signal    |     | 160  |     | W             |
|                   |                                                             | $R_L = 8\ \Omega$ , 1% THD+N, unclipped output signal   |     | 125  |     |               |
| THD+N             | Total harmonic distortion + noise                           | 1 W                                                     |     | 0.05 |     | %             |
| V <sub>n</sub>    | Output integrated noise                                     | A-weighted, AES17 filter, input capacitor grounded      |     | 260  |     | $\mu\text{V}$ |
| V <sub>OS</sub>   | Output offset voltage                                       | Inputs ac-coupled to AGND                               |     | 40   | 150 | mV            |
| SNR               | Signal-to-noise ratio <sup>(1)</sup>                        |                                                         |     | 100  |     | dB            |
| DNR               | Dynamic range                                               |                                                         |     | 100  |     | dB            |
| P <sub>idle</sub> | Power dissipation due to idle losses (I <sub>PVDD_X</sub> ) | P <sub>O</sub> = 0, 4 channels switching <sup>(2)</sup> |     | 2.3  |     | W             |

(1) SNR is calculated relative to 1% THD+N output level.

(2) Actual system idle losses also are affected by core losses of output inductors.

## AUDIO SPECIFICATION (Single-Ended Output)

PCB and system configuraton are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD\_X = 50 V, GVDD\_X = 12 V,  $R_L = 4\ \Omega$ ,  $f_s = 400\ \text{kHz}$ ,  $R_{OC} = 22\ \text{k}\Omega$ ,  $T_C = 75^\circ\text{C}$ , output filter:  $L_{DEM} = 15\ \mu\text{H}$ ,  $C_{DEM} = 330\ \text{nF}$ , MODE = 100, unless otherwise noted.

| PARAMETER         |                                                             | TEST CONDITIONS                                         | MIN | TYP  | MAX | UNIT          |
|-------------------|-------------------------------------------------------------|---------------------------------------------------------|-----|------|-----|---------------|
| P <sub>O</sub>    | Power output per channel                                    | $R_L = 4\ \Omega$ , 10% THD+N, clipped output signal    |     | 75   |     | W             |
|                   |                                                             | $R_L = 4\ \Omega$ , 1% THD+N, unclipped output signal   |     | 60   |     |               |
| THD+N             | Total harmonic distortion + noise                           | 1 W                                                     |     | 0.05 |     | %             |
| V <sub>n</sub>    | Output integrated noise                                     | A-weighted                                              |     | 350  |     | $\mu\text{V}$ |
| SNR               | Signal-to-noise ratio <sup>(1)</sup>                        | A-weighted                                              |     | 93   |     | dB            |
| DNR               | Dynamic range                                               | A-weighted                                              |     | 93   |     | dB            |
| P <sub>idle</sub> | Power dissipation due to idle losses (I <sub>PVDD_X</sub> ) | P <sub>O</sub> = 0, 4 channels switching <sup>(2)</sup> |     | 1.15 |     | W             |

(1) SNR is calculated relative to 1% THD+N output level.

(2) Actual system idle losses are affected by core losses of output inductors.

## AUDIO SPECIFICATION (PBTL)

PCB and system configuraton are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD\_X = 50 V, GVDD\_X = 12 V,  $R_L = 4\ \Omega$ ,  $f_s = 400\text{ kHz}$ ,  $R_{OC} = 22\text{ k}\Omega$ ,  $T_C = 75^\circ\text{C}$ , output filter:  $L_{DEM} = 15\ \mu\text{H}$ ,  $C_{DEM} = 680\text{ nF}$ , MODE = 101-BD, unless otherwise noted.

| PARAMETER         |                                                | TEST CONDITIONS                                         | MIN | TYP  | MAX | UNIT          |
|-------------------|------------------------------------------------|---------------------------------------------------------|-----|------|-----|---------------|
| P <sub>O</sub>    | Power output per channel                       | $R_L = 4\ \Omega$ , 10% THD+N, clipped output signal    |     | 300  |     | W             |
|                   |                                                | $R_L = 6\ \Omega$ , 10% THD+N, clipped output signal    |     | 210  |     |               |
|                   |                                                | $R_L = 8\ \Omega$ , 10% THD+N, clipped output signal    |     | 160  |     |               |
|                   |                                                | $R_L = 4\ \Omega$ , 1% THD+N, unclipped output signal   |     | 240  |     |               |
|                   |                                                | $R_L = 6\ \Omega$ , 1% THD+N, unclipped output signal   |     | 160  |     |               |
|                   |                                                | $R_L = 8\ \Omega$ , 1% THD+N, unclipped output signal   |     | 125  |     |               |
| THD+N             | Total harmonic distortion + noise              | 1 W                                                     |     | 0.05 |     | %             |
| V <sub>n</sub>    | Output integrated noise                        | A-weighted                                              |     | 260  |     | $\mu\text{V}$ |
| SNR               | Signal-to-noise ratio <sup>(1)</sup>           | A-weighted                                              |     | 100  |     | dB            |
| DNR               | Dynamic range                                  | A-weighted                                              |     | 100  |     | dB            |
| P <sub>idle</sub> | Power dissipation due to idle losses (IPVDD_X) | P <sub>O</sub> = 0, 4 channels switching <sup>(2)</sup> |     | 2.3  |     | W             |

(1) SNR is calculated relative to 1% THD+N output level.

(2) Actual system idle losses are affected by core losses of output inductors.

## ELECTRICAL CHARACTERISTICS

PVDD\_X = 50 V, GVDD\_X = 12 V, VDD = 12 V,  $T_C$  (case temperature) =  $75^\circ\text{C}$ ,  $f_s = 400\text{ kHz}$ , unless otherwise specified.

| PARAMETER                                          |                                                | TEST CONDITIONS                                           | MIN  | TYP  | MAX  | UNIT |
|----------------------------------------------------|------------------------------------------------|-----------------------------------------------------------|------|------|------|------|
| INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION |                                                |                                                           |      |      |      |      |
| VREG                                               | Voltage regulator, only used as reference node | VDD = 12 V                                                | 3    | 3.3  | 3.6  | V    |
| VI_CM                                              | Analog comparator reference node               |                                                           | 1.5  | 1.75 | 1.9  | V    |
| IVDD                                               | VDD supply current                             | Operating, 50% duty cycle                                 | 22.5 |      |      | mA   |
|                                                    |                                                | Idle, reset mode                                          | 22.5 |      |      |      |
| IGVDD_x                                            | Gate-supply current per half-bridge            | 50% duty cycle                                            | 8    |      |      | mA   |
|                                                    |                                                | Reset mode                                                | 1.5  |      |      |      |
| IPVDD_x                                            | Half-bridge idle current                       | 50% duty cycle without output filter or load              | 7    |      |      | mA   |
|                                                    |                                                | Reset mode, no switching                                  | 610  |      |      | μA   |
| ANALOG INPUTS                                      |                                                |                                                           |      |      |      |      |
| RIN                                                | Input resistance                               | READY = HIGH                                              | 33   |      |      | kΩ   |
| VIN                                                | Maximum input voltage swing                    |                                                           | 5    |      |      | V    |
| IIN                                                | Maximum input current                          |                                                           | 342  |      |      | mA   |
| G                                                  | Voltage gain (VOUT/VIN)                        |                                                           | 23   |      |      | dB   |
| OSCILLATOR                                         |                                                |                                                           |      |      |      |      |
| fOSC_IO+                                           | Nominal, master mode                           | FPWM × 10                                                 | 3.85 | 4    | 4.15 | MHz  |
|                                                    | AM1, master mode                               |                                                           | 3.15 | 3.33 | 3.5  |      |
|                                                    | AM2, master mode                               |                                                           | 2.6  | 3    | 3.35 |      |
| VIH                                                | High-level input voltage                       |                                                           | 1.86 |      |      | V    |
| VIL                                                | Low-level input voltage                        |                                                           | 1.45 |      |      | V    |
| OUTPUT-STAGE MOSFETS                               |                                                |                                                           |      |      |      |      |
| RDS(on)                                            | Drain-to-source resistance, low side (LS)      | TJ = 25°C, includes metallization resistance, GVDD = 12 V | 120  | 200  | mΩ   |      |
|                                                    | Drain-to-source resistance, high side (HS)     |                                                           | 120  | 200  | mΩ   |      |

## ELECTRICAL CHARACTERISTICS (continued)

PVDD\_X = 50 V, GVDD\_X = 12 V, VDD = 12 V, T<sub>C</sub> (case temperature) = 75°C, f<sub>s</sub> = 400 kHz, unless otherwise specified.

| PARAMETER                                        |                                                                                                           | TEST CONDITIONS                                                                                                       | MIN | TYP  | MAX | UNIT    |
|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-----|------|-----|---------|
| <b>I/O PROTECTION</b>                            |                                                                                                           |                                                                                                                       |     |      |     |         |
| V <sub>uvp,G</sub>                               | Undervoltage protection limit, GVDD_X and VDD                                                             |                                                                                                                       |     | 9.5  |     | V       |
| V <sub>uvp,hyst</sub> <sup>(1)</sup>             |                                                                                                           |                                                                                                                       |     | 0.6  |     | V       |
| OTW1 <sup>(1)</sup>                              | Overtemperature warning 1                                                                                 |                                                                                                                       | 95  | 100  | 105 | °C      |
| OTW2 <sup>(1)</sup>                              | Overtemperature warning 2                                                                                 |                                                                                                                       | 115 | 125  | 135 | °C      |
| OTW <sub>HYST</sub> <sup>(1)</sup>               | Temperature drop needed below OTW temperture for OTW to be inactive after OTW event.                      |                                                                                                                       |     | 25   |     | °C      |
| OTE <sup>(1)</sup>                               | Overtemperature error                                                                                     |                                                                                                                       | 145 | 155  | 165 | °C      |
| OTE-OTW <sub>differential</sub> <sup>(1)</sup>   | OTE-OTW differential                                                                                      |                                                                                                                       |     | 30   |     | °C      |
| OTE <sub>HYST</sub> <sup>(1)</sup>               | A reset must occur for $\overline{SD}$ to be released following an OTE event                              |                                                                                                                       |     | 25   |     | °C      |
| OLPC                                             | Overload protection counter                                                                               | f <sub>PWM</sub> = 400 kHz                                                                                            |     | 2.6  |     | ms      |
| I <sub>OC</sub>                                  | Overcurrent limit protection                                                                              | Resistor – programmable, nominal continious current in 1-Ω load, 64 pin QFP package (PHD), R <sub>OCP</sub> = 22 kΩ   |     | 10   |     | A       |
|                                                  |                                                                                                           | Resistor – programmable, nominal continious current in 1-Ω load, 44 pin PSOP3 package (DKD), R <sub>OCP</sub> = 24 kΩ |     | 10   |     | A       |
| I <sub>OC_LATCHED</sub>                          | Overcurrent limit protection                                                                              | Resistor – programmable, continious current in 1-Ω load, R <sub>OCP</sub> = 47 kΩ                                     |     | 10   |     | A       |
| I <sub>OCT</sub>                                 | Overcurrent response time                                                                                 | Time from switching transition to flip-state induced by overcurrent                                                   |     | 150  |     | ns      |
| I <sub>PD</sub>                                  | Output pulldown current of each half                                                                      | Connected when $\overline{RESET}$ is active to provide bootstrap charge. Not used in SE mode.                         |     | 3    |     | mA      |
| <b>STATIC DIGITAL SPECIFICATIONS</b>             |                                                                                                           |                                                                                                                       |     |      |     |         |
| V <sub>IH</sub>                                  | High-level input voltage                                                                                  | INPUT_X, M1, M2, M3, $\overline{RESET}$                                                                               | 1.9 |      |     | V       |
| V <sub>IL</sub>                                  | Low-level input voltage                                                                                   |                                                                                                                       |     | 1.45 |     | V       |
| Leakage                                          | Input leakage current                                                                                     |                                                                                                                       |     | 100  |     | μA      |
| <b>OTW/SHUTDOWN (<math>\overline{SD}</math>)</b> |                                                                                                           |                                                                                                                       |     |      |     |         |
| R <sub>INT_PU</sub>                              | Internal pullup resistance, $\overline{OTW1}$ to VREG, $\overline{OTW2}$ to VREG, $\overline{SD}$ to VREG |                                                                                                                       | 20  | 26   | 32  | kΩ      |
| V <sub>OH</sub>                                  | High-level output voltage                                                                                 | Internal pullup resistor                                                                                              | 3   | 3.3  | 3.6 | V       |
|                                                  |                                                                                                           | External pullup of 4.7 kΩ to 5 V                                                                                      | 4.5 |      | 5   |         |
| V <sub>OL</sub>                                  | Low-level output voltage                                                                                  | I <sub>O</sub> = 4 mA                                                                                                 |     | 200  | 500 | mV      |
| FANOUT                                           | Device fanout $\overline{OTW1}$ , $\overline{OTW2}$ , $\overline{SD}$ , CLIP, READY                       | No external pullup                                                                                                    |     | 30   |     | devices |

(1) Specified by design.

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC+NOISE  
vs  
OUTPUT POWER

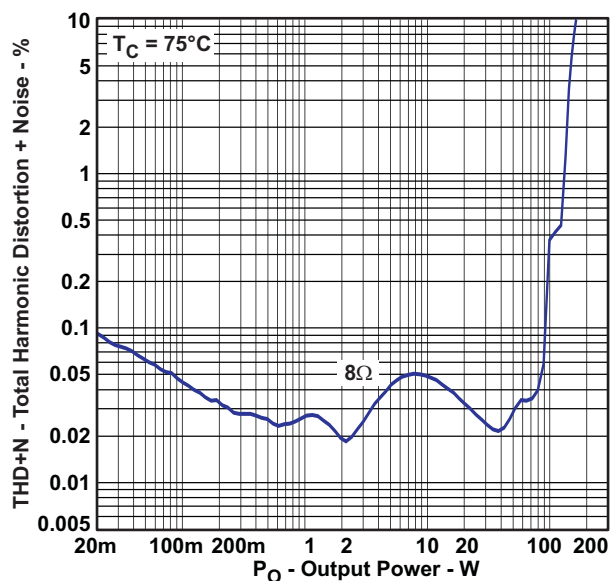


Figure 1.

OUTPUT POWER  
vs  
SUPPLY VOLTAGE

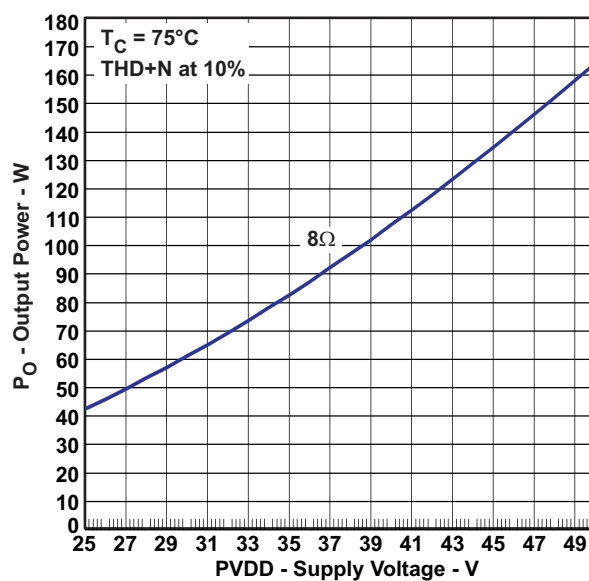


Figure 2.

UNCLIPPED OUTPUT POWER  
vs  
SUPPLY VOLTAGE

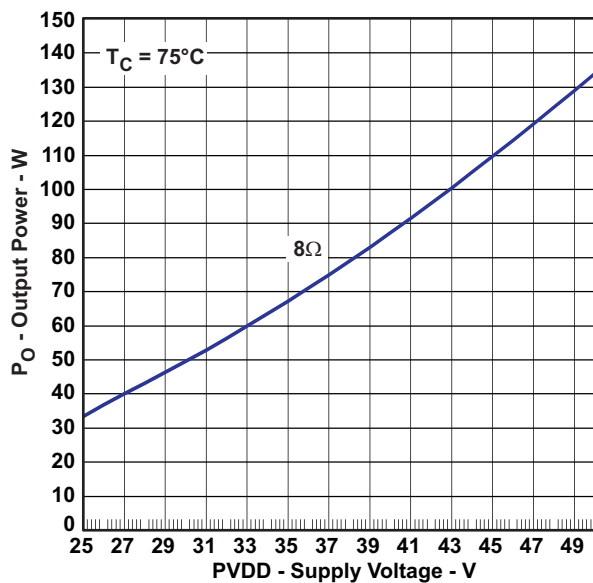


Figure 3.

SYSTEM EFFICIENCY  
vs  
OUTPUT POWER

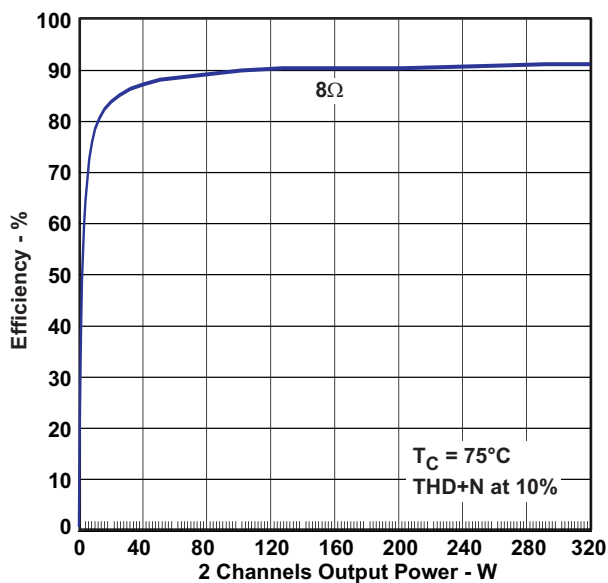


Figure 4.

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

SYSTEM POWER LOSS  
vs  
OUTPUT POWER

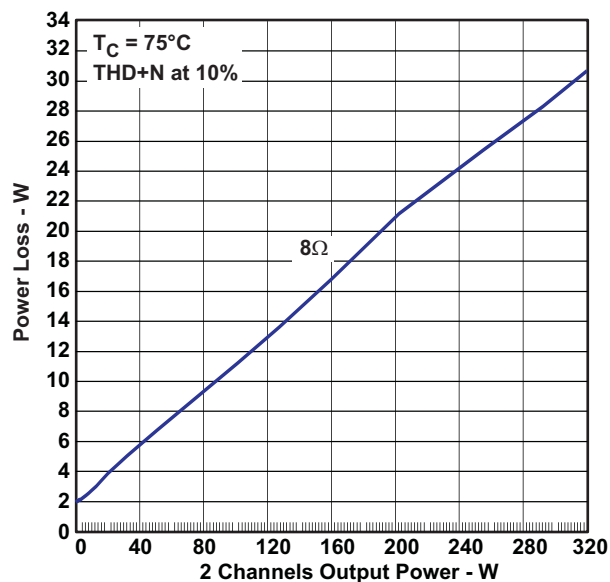


Figure 5.

OUTPUT POWER  
vs  
CASE TEMPERATURE

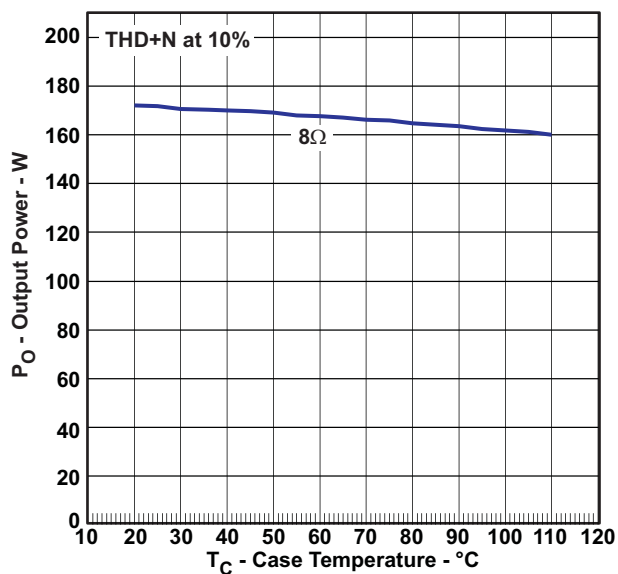


Figure 6.

NOISE AMPLITUDE  
vs  
FREQUENCY

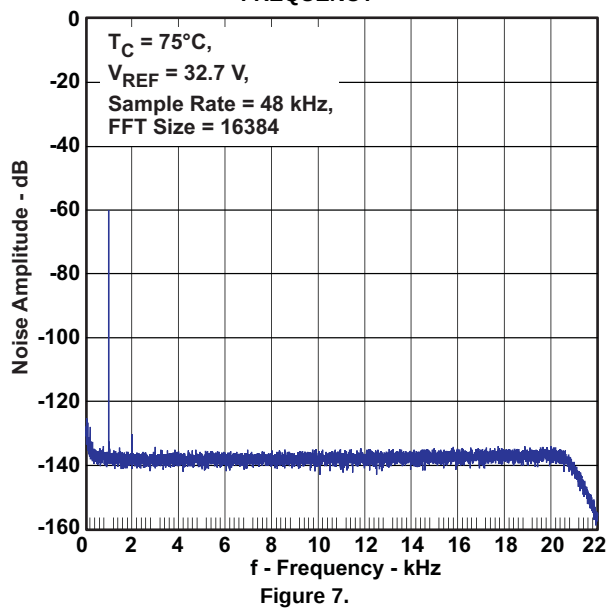


Figure 7.

## TYPICAL CHARACTERISTICS, SE CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE  
vs  
OUTPUT POWER

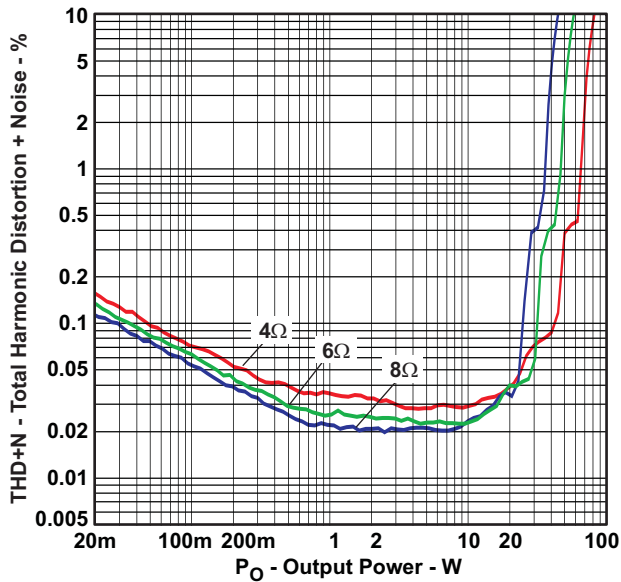


Figure 8.

OUTPUT POWER  
vs  
SUPPLY VOLTAGE

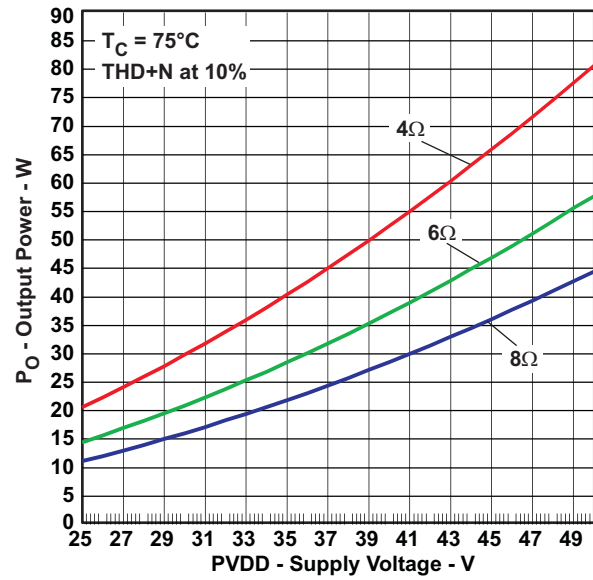


Figure 9.

OUTPUT POWER  
vs  
CASE TEMPERATURE

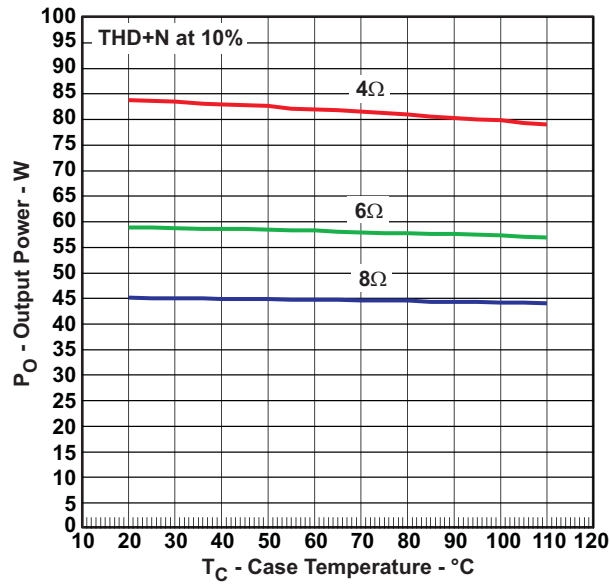


Figure 10.

## TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE  
vs  
OUTPUT POWER

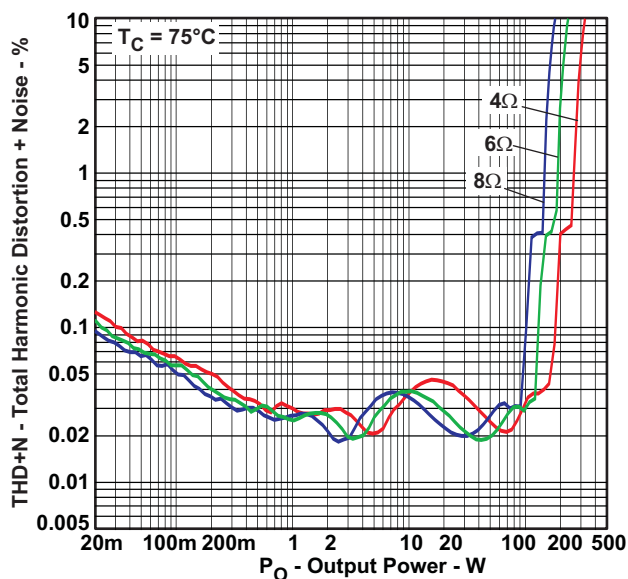


Figure 11.

OUTPUT POWER  
vs  
SUPPLY VOLTAGE

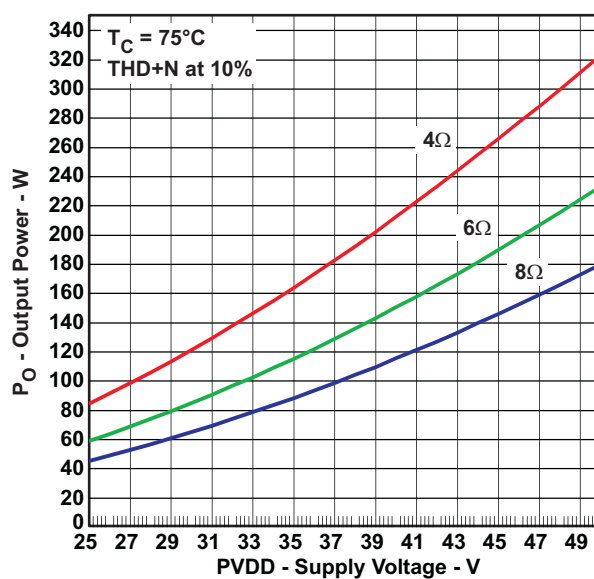


Figure 12.

OUTPUT POWER  
vs  
CASE TEMPERATURE

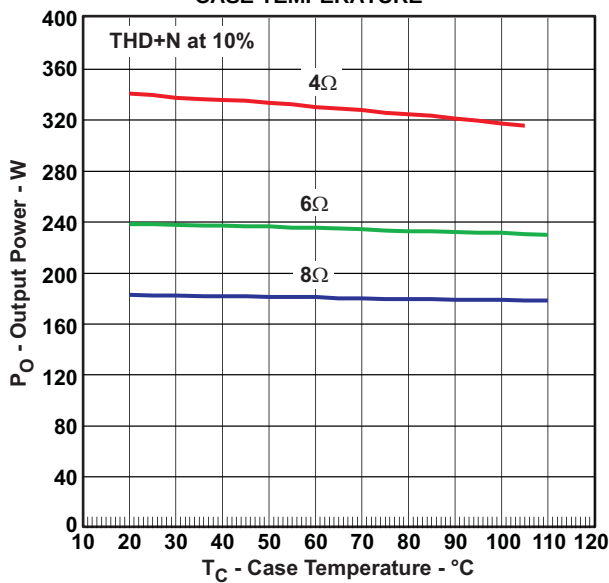


Figure 13.

## APPLICATION INFORMATION

### PCB MATERIAL RECOMMENDATION

FR-4 glass epoxy material with 2 oz. (70  $\mu\text{m}$ ) is recommended for use with the TAS5615. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin, due to lower PCB trace inductance.

### PVDD CAPACITOR RECOMMENDATION

The large capacitors used in conjunction with each full bridge are referred to as the PVDD capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed system power supply, 1000  $\mu\text{F}$ , 63 V will support more applications. The PVDD capacitors should be low-ESR type because they are used in a circuit associated with high-speed switching.

### DECOUPLING CAPACITOR RECOMMENDATIONS

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good-quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 2.2  $\mu\text{F}$  that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 63 V is required for use with a 50-V power supply.

### SYSTEM DESIGN RECOMMENDATIONS

The following schematics and PCB layouts illustrate best practices in the use of the TAS5615.

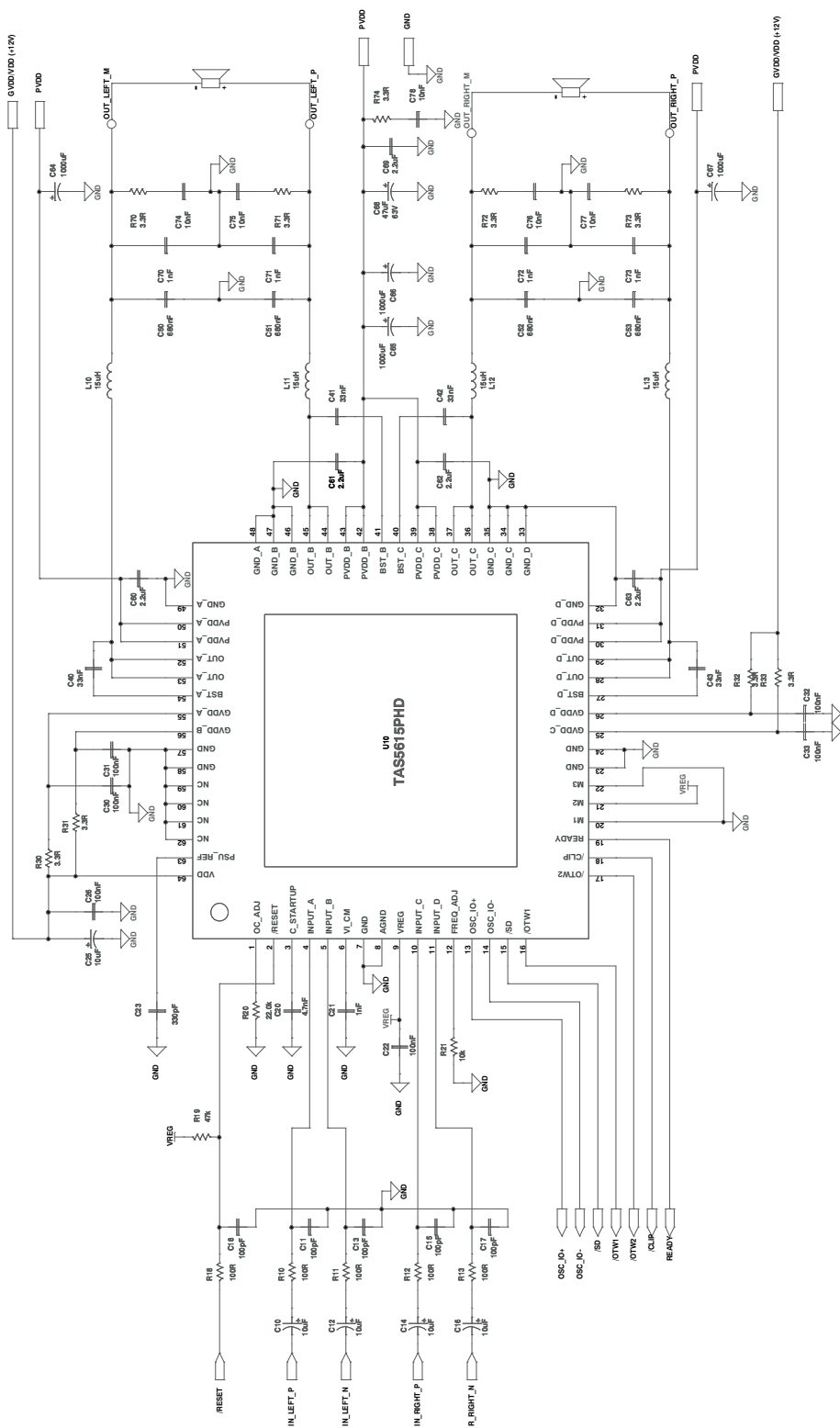


Figure 14. Typical Differential Input BTL Application With BD Modulation Filters



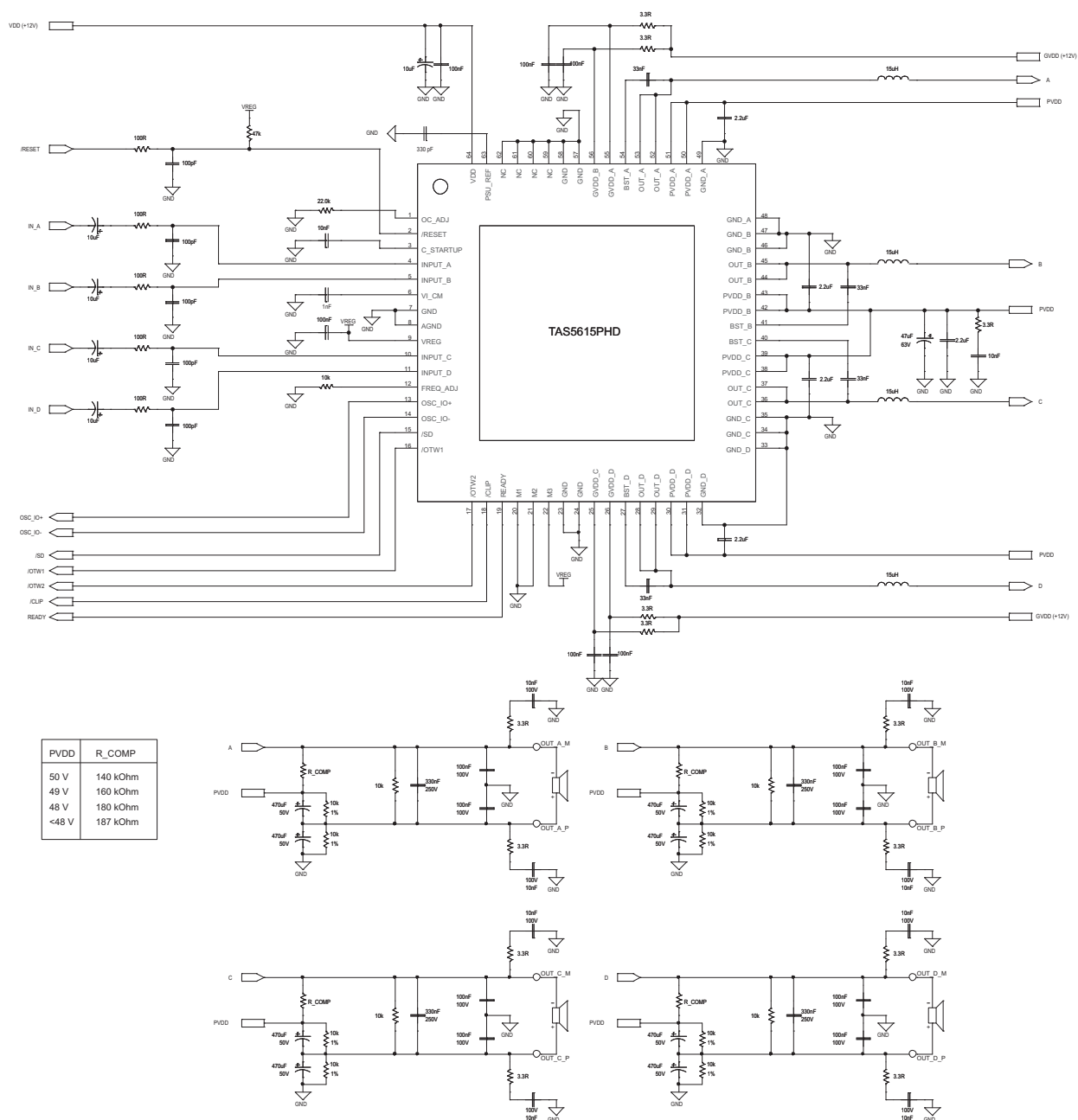


Figure 16. Typical SE Application

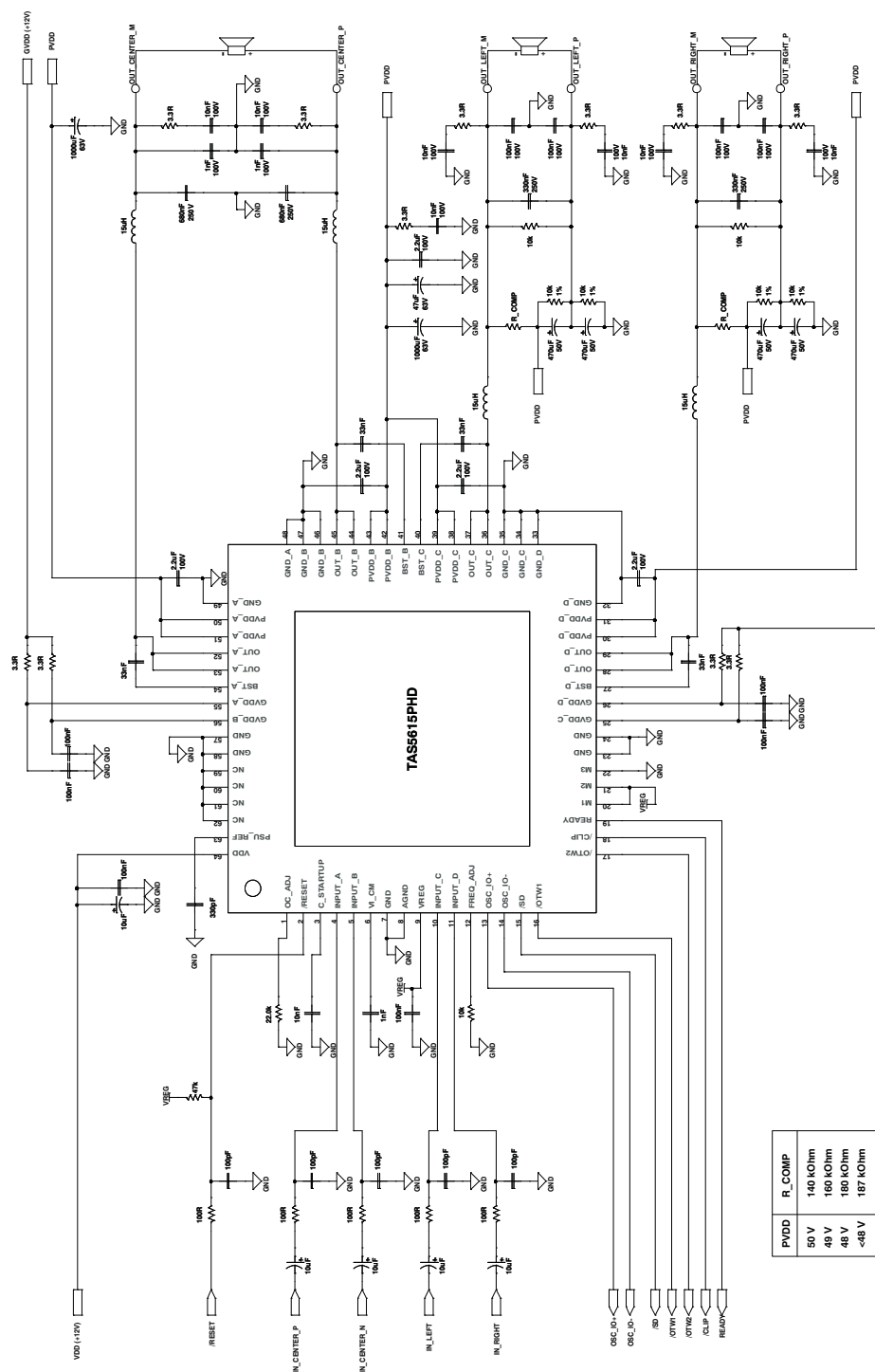


Figure 17. Typical 2.1 System Differential-Input BTL and Unbalanced-Input SE Application

## THEORY OF OPERATION

### POWER SUPPLIES

To facilitate system design, the TAS5615 needs only a 12-V supply in addition to the (typical) 50-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate-drive supply (GVDD\_X), bootstrap pins (BST\_X), and power-stage supply pins (PVDD\_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD\_A, GVDD\_B, GVDD\_C, GVDD\_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST\_X) to the power-stage output pin (OUT\_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD\_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300 kHz to 400 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned-on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD\_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD\_X pin is decoupled with a 2.2-μF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5615 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5615 is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the [Recommended Operating Conditions](#) table of this data sheet).

### SYSTEM POWER-UP/POWER-DOWN SEQUENCE

#### Powering Up

The TAS5615 does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD\_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the [Electrical Characteristics](#) table of this data sheet). Although not specifically required, it is recommended to hold  $\overline{\text{RESET}}$  in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

#### Powering Down

The TAS5615 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD\_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the [Electrical Characteristics](#) table of this data sheet). Although not specifically required, it is a good practice to hold  $\overline{\text{RESET}}$  low during power down, thus preventing audible artifacts including pops or clicks.

## ERROR REPORTING

The  $\overline{\text{SD}}$ ,  $\overline{\text{OTW}}$ ,  $\overline{\text{OTW1}}$  and  $\overline{\text{OTW2}}$  pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the  $\overline{\text{SD}}$  pin going low. Likewise,  $\overline{\text{OTW}}$  and  $\overline{\text{OTW2}}$  go low when the device junction temperature exceeds 125°C and  $\overline{\text{OTW1}}$  goes low when the junction temperature exceeds 100°C (see the following table).

| $\overline{\text{SD}}$ | $\overline{\text{OTW1}}$ | $\overline{\text{OTW2}}, \overline{\text{OTW}}$ | DESCRIPTION                                                                                                                     |
|------------------------|--------------------------|-------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| 0                      | 0                        | 0                                               | Overtemperature (OTE) or overload (OLP) or undervoltage (UVP). Junction temperature higher than 125°C (overtemperature warning) |
| 0                      | 0                        | 1                                               | Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)                          |
| 0                      | 1                        | 1                                               | Overload (OLP) or undervoltage (UVP). Junction temperature lower than 100°C                                                     |
| 1                      | 0                        | 0                                               | Junction temperature higher than 125°C (overtemperature warning)                                                                |
| 1                      | 0                        | 1                                               | Junction temperature higher than 100°C (overtemperature warning)                                                                |
| 1                      | 1                        | 1                                               | Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)                                               |

Note that asserting either  $\overline{\text{RESET}}$  low forces the  $\overline{\text{SD}}$  signal high, independent of faults being present. TI recommends monitoring the  $\overline{\text{OTW}}$  signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both  $\overline{\text{SD}}$  and  $\overline{\text{OTW}}$  outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the Electrical Characteristics section of this data sheet for further specifications).

## DEVICE PROTECTION SYSTEM

The TAS5615 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5615 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the  $\overline{\text{SD}}$  pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

The device functions on errors, as shown in the following table

| BTL            | MODE      | PBTL           | MODE      | SE             | MODE      |
|----------------|-----------|----------------|-----------|----------------|-----------|
| LOCAL ERROR IN | TURNS OFF | LOCAL ERROR IN | TURNS OFF | LOCAL ERROR IN | TURNS OFF |
| A              | A+B       | A              | A+B+C+D   | A              | A+B       |
| B              |           | B              |           | B              | C+D       |
| C              | C+D       | C              |           | C              |           |
| D              |           | D              |           | D              |           |

Bootstrap UVP does not shut down according to the table, it shuts down the respective half-bridge.

## PIN-TO-PIN SHORT CIRCUIT PROTECTION (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT\_X) is shorted to GND\_X or PVDD\_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at start-up, i.e., when VDD is supplied; consequently, a short to either GND\_X or PVDD\_X after system start-up does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed; the device then continues the start-up sequence and starts switching. The detection is controlled globally by a two-step sequence. The first step ensures that there are no shorts from OUT\_X to GND\_X; the second step tests that there are no shorts from OUT\_X to PVDD\_X. The total duration of this process is roughly proportional to the capacitance of the

output LC filter. The typical duration is  $< 15 \text{ ms}/\mu\text{F}$ . While the PPSC detection is in progress,  $\overline{\text{SD}}$  is kept low, and the device does not react to changes applied to the  $\overline{\text{RESET}}$  pin. If no shorts are present, the PPSC detection passes, and  $\overline{\text{SD}}$  is released. A device reset does not start a new PPSC detection. PPSC detection is enabled in BTL and PBTl output configurations; the detection is not performed in SE mode. To make sure not to trip the PPSC detection system, it is recommended not to insert resistive load to  $\text{GND\_X}$  or  $\text{PVDD\_X}$ .

## OVERTEMPERATURE PROTECTION

The two different package options have individual overtemperature protection schemes.

### PHD Package

The TAS5615 PHD package option has a three-level temperature-protection system that asserts an active-low warning signal (OTW1) when the device junction temperature exceeds  $100^\circ\text{C}$  (typical), (OTW2) when the device junction temperature exceeds  $125^\circ\text{C}$  (typical) and, if the device junction temperature exceeds  $155^\circ\text{C}$  (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and  $\overline{\text{SD}}$  being asserted low. OTE is latched in this case. To clear the OTE latch,  $\overline{\text{RESET}}$  must be asserted. Thereafter, the device resumes normal operation.

### DKD Package

The TAS5615 DKD package option has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds  $125^\circ\text{C}$  (typical) and, if the device junction temperature exceeds  $155^\circ\text{C}$  (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and  $\overline{\text{SD}}$  being asserted low. OTE is latched in this case. To clear the OTE latch,  $\overline{\text{RESET}}$  must be asserted. Thereafter, the device resumes normal operation.

## UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5615 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the  $\text{GVDD\_X}$  and  $\text{VDD}$  supply voltages reach levels stated in the [Electrical Characteristics](#) table. Although  $\text{GVDD\_X}$  and  $\text{VDD}$  are independently monitored, a supply-voltage drop below the UVP threshold on any  $\text{VDD}$  or  $\text{GVDD\_X}$  pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and  $\overline{\text{SD}}$  being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

## DEVICE RESET

When  $\overline{\text{RESET}}$  is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high-impedance state when asserting the reset input low.

Asserting the reset input low removes any fault information to be signalled on the  $\overline{\text{SD}}$  output, i.e.,  $\overline{\text{SD}}$  is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of  $\overline{\text{SD}}$ .

## SYSTEM DESIGN CONSIDERATION

A rising-edge transition on the reset input allows the device to execute the start-up sequence and starts switching.

Apply only audio when the state of  $\text{READY}$  is high; that starts and stops the amplifier without having audible artifacts in the output transducers. If an overcurrent protection event is introduced, the  $\text{READY}$  signal goes low; hence, filtering is needed if the signal is intended for audio muting in non-microcontroller systems.

The CLIP signal indicates that the output is approaching clipping. The signal can be used to decrease either an audio volume or an intelligent power supply controlling a low and a high rail.

The device inverts the audio signal from input to output.

The VREG pin is not recommended to be used as a voltage source for external circuitry.

## OSCILLATOR

The oscillator frequency can be trimmed by external control of the FREQ\_ADJ pin.

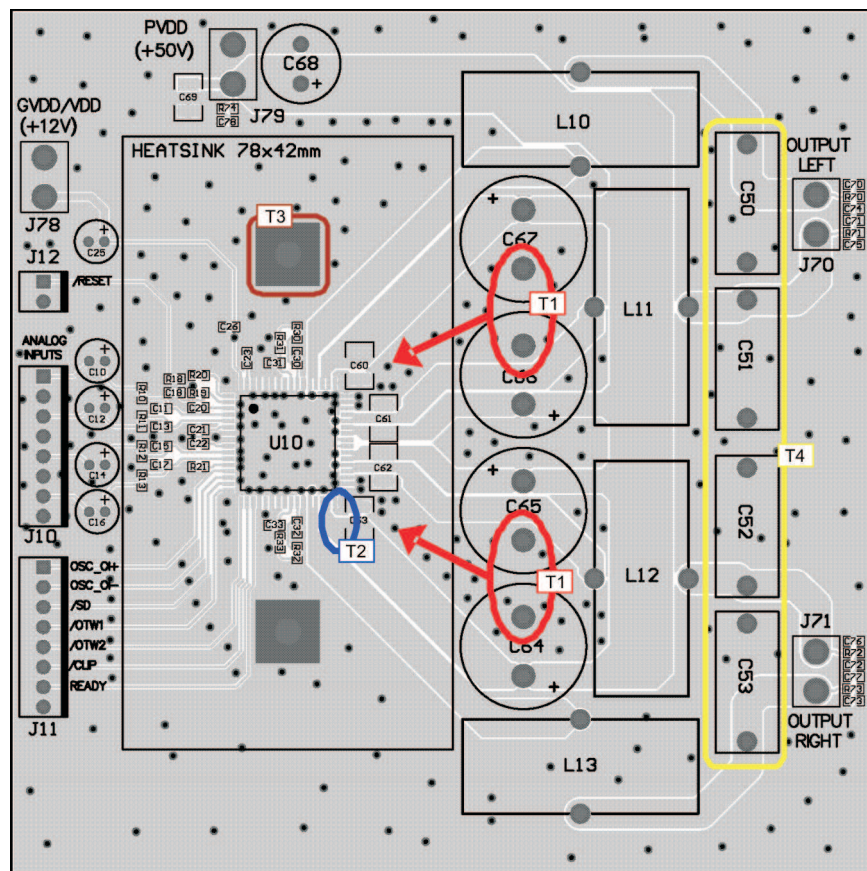
To reduce interference problems while using a radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower values. These values should be chosen such that the nominal and the lower-value switching frequencies together result in the fewest cases of interference throughout the AM band. Switching frequencies can be selected by the value of the FREQ\_ADJ resistor connected to AGND in master mode.

For slave-mode operation, turn off the oscillator by pulling the FREQ\_ADJ pin to VREG. This configures the OSC\_I/O pins as inputs and must be slaved from an external clock.

## PRINTED CIRCUIT BOARD RECOMMENDATION

Use an unbroken ground plane to have a good low-impedance and -inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high, fast-switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing of the audio input should be kept short and together with the accompanied audio source ground. It is important to keep a solid local ground area underneath the device to minimize ground bounce.

Netlist for this printed circuit board is generated from the schematic in [Figure 14](#).



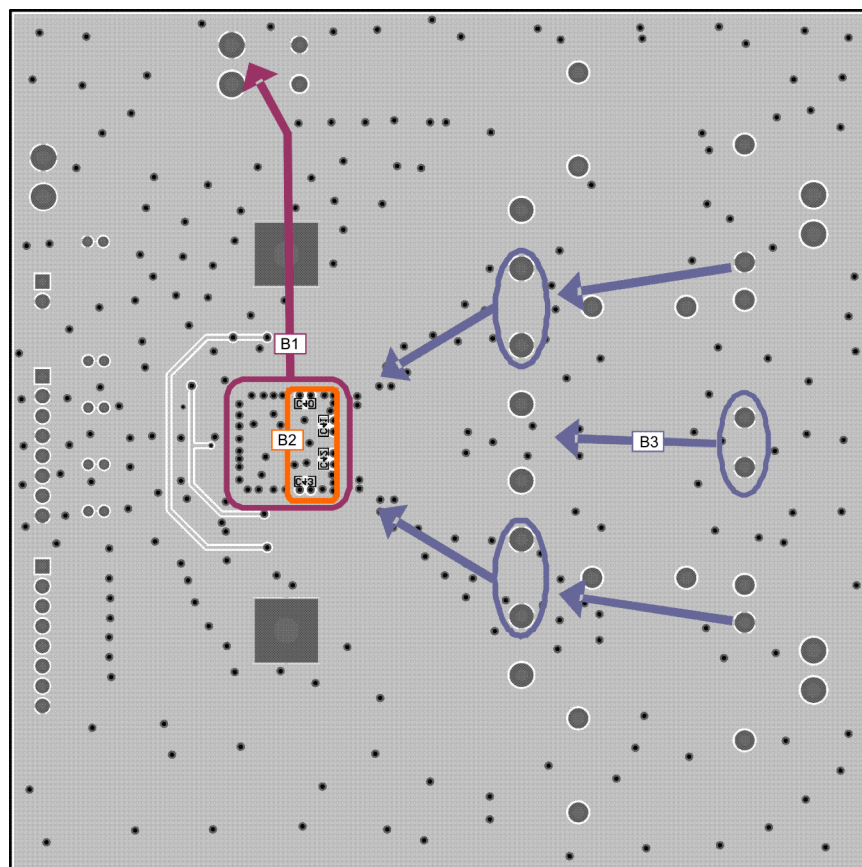
**Note T1:** PVDD decoupling bulk capacitors C60–C64 should be as close as possible to the PVDD and GND\_X pins; the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

**Note T2:** Close decoupling of PVDD with low-impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

**Note T3:** Heat sink must have a good connection to PCB ground.

**Note T4:** Output filter capacitors, preferably metal film types, must be linear in the applied voltage range.

**Figure 18. Printed Circuit Board – Top Layer**



**Note B1:** It is important to have a direct low-impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

**Note B2:** Bootstrap low-impedance X7R ceramic capacitors placed on bottom side providing a short low-inductance current loop.

**Note B3:** Return currents from bulk capacitors and output filter capacitors.

**Figure 19. Printed Circuit Board – Bottom Layer**

## REVISION HISTORY

| Changes from Original (June 2009) to Revision A                                                  | Page |
|--------------------------------------------------------------------------------------------------|------|
| Deleted Product Preview from the PHD package .....                                               | 3    |
| Changes from Revision A (September 2009) to Revision B                                           | Page |
| Changed pin location diagram .....                                                               | 2    |
| Replaced chip graphic in pinout diagram .....                                                    | 2    |
| Changed several frame-rate specifications in the <i>Recommended Operating Conditions</i> .....   | 4    |
| Changed specifications for oscillator frequencies in the <i>Electrical Characteristics</i> ..... | 10   |
| Changed response time for overload protection counter in <i>Electrical Characteristics</i> ..... | 11   |
| Revised component values on pins 6 and 63 in Typical SE Application illustration .....           | 19   |

## PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TAS5615DKD            | Active        | Production           | HSSOP (DKD)   44 | 29   TUBE             | Yes         | NIPDAU                               | Level-4-260C-72 HR                | 0 to 70      | TAS5615             |
| TAS5615DKD.A          | Active        | Production           | HSSOP (DKD)   44 | 29   TUBE             | Yes         | NIPDAU                               | Level-4-260C-72 HR                | 0 to 70      | TAS5615             |
| TAS5615DKD.B          | Active        | Production           | HSSOP (DKD)   44 | 29   TUBE             | Yes         | NIPDAU                               | Level-4-260C-72 HR                | 0 to 70      | TAS5615             |
| TAS5615DKDR           | Active        | Production           | HSSOP (DKD)   44 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-4-260C-72 HR                | 0 to 70      | TAS5615             |
| TAS5615DKDR.A         | Active        | Production           | HSSOP (DKD)   44 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-4-260C-72 HR                | 0 to 70      | TAS5615             |
| TAS5615DKDR.B         | Active        | Production           | HSSOP (DKD)   44 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-4-260C-72 HR                | 0 to 70      | TAS5615             |
| TAS5615PHD            | Active        | Production           | HTQFP (PHD)   64 | 90   JEDEC TRAY (5+1) | Yes         | NIPDAU                               | Level-5A-260C-24 HR               | 0 to 70      | TAS5615             |
| TAS5615PHD.A          | Active        | Production           | HTQFP (PHD)   64 | 90   JEDEC TRAY (5+1) | Yes         | NIPDAU                               | Level-5A-260C-24 HR               | 0 to 70      | TAS5615             |
| TAS5615PHDR           | Active        | Production           | HTQFP (PHD)   64 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-5A-260C-24 HR               | 0 to 70      | TAS5615             |
| TAS5615PHDR.A         | Active        | Production           | HTQFP (PHD)   64 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-5A-260C-24 HR               | 0 to 70      | TAS5615             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

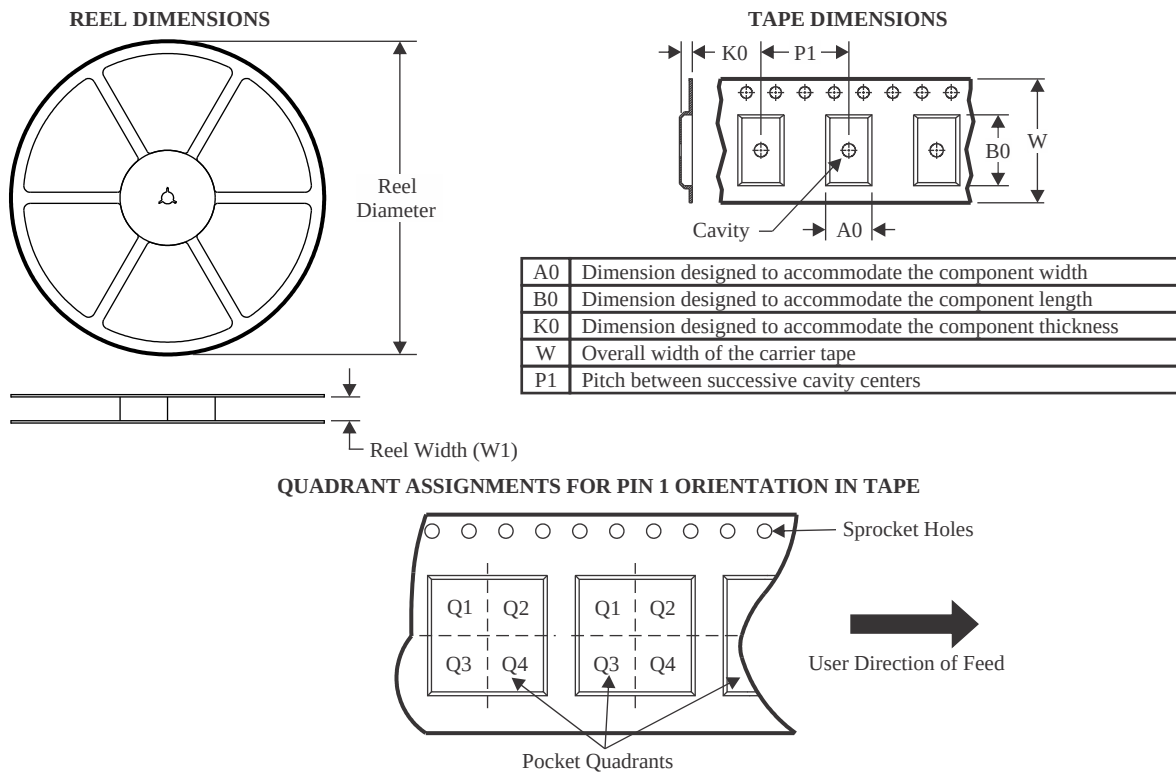
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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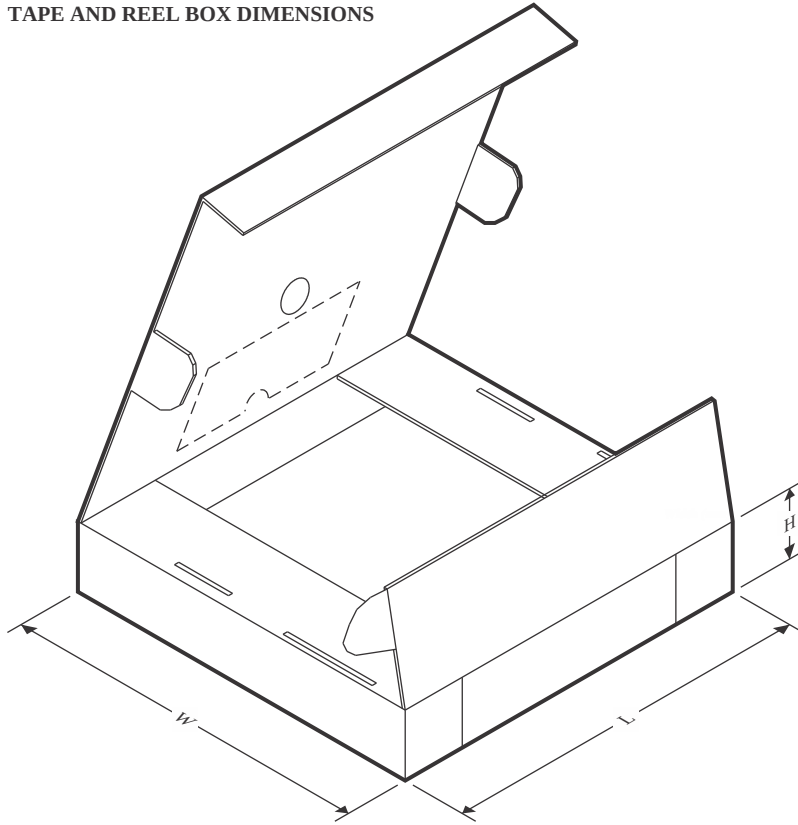
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS5615PHDR | HTQFP        | PHD             | 64   | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 1.5     | 20.0    | 24.0   | Q2            |

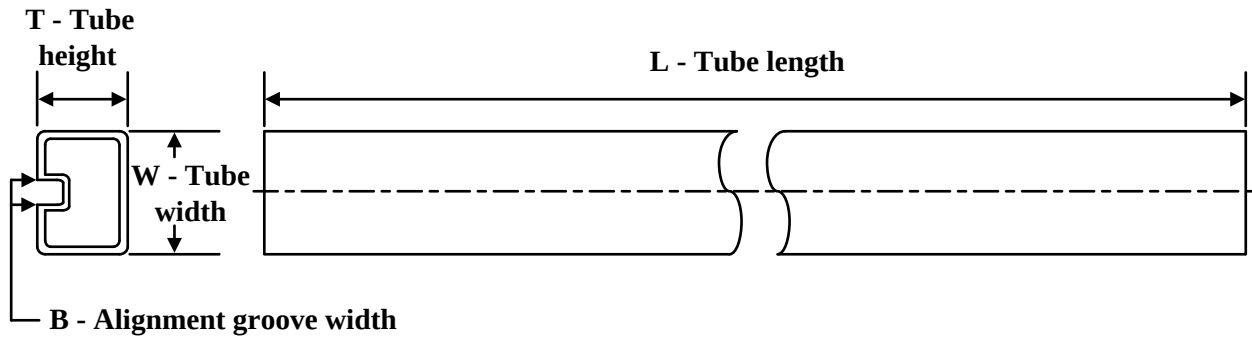
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS5615PHDR | HTQFP        | PHD             | 64   | 1000 | 350.0       | 350.0      | 43.0        |

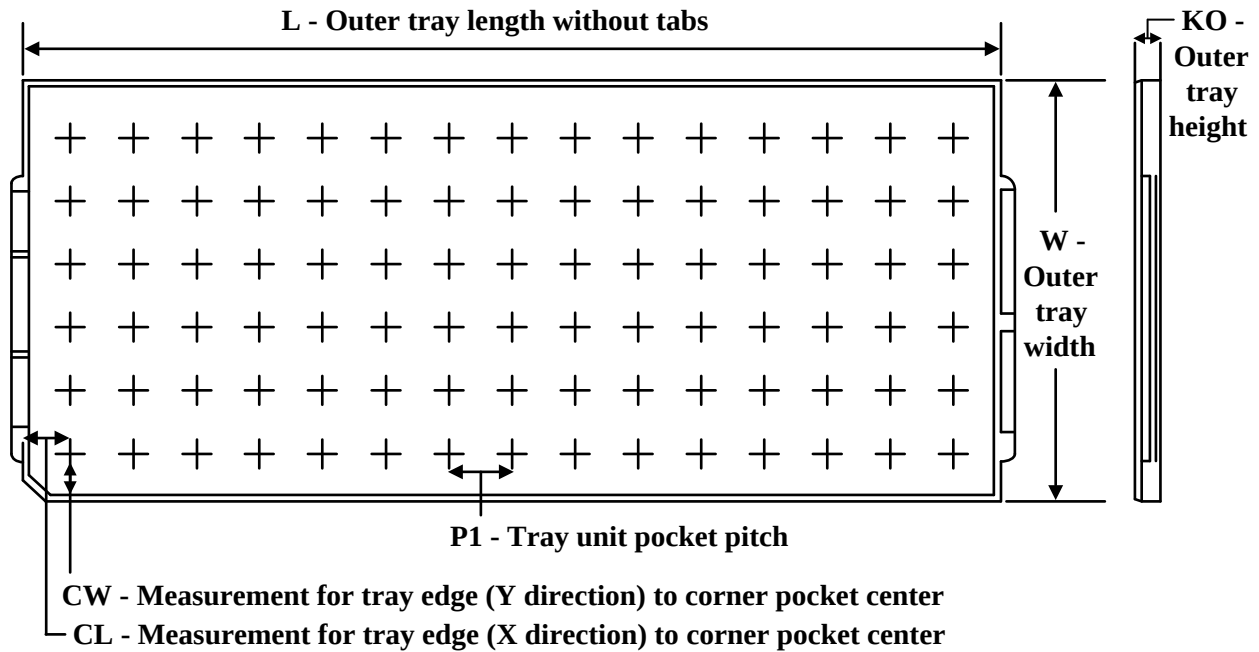
## TUBE



\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TAS5615DKD   | DKD          | HSSOP        | 44   | 29  | 508    | 18.54  | 6350   | 8.13   |
| TAS5615DKD.A | DKD          | HSSOP        | 44   | 29  | 508    | 18.54  | 6350   | 8.13   |
| TAS5615DKD.B | DKD          | HSSOP        | 44   | 29  | 508    | 18.54  | 6350   | 8.13   |

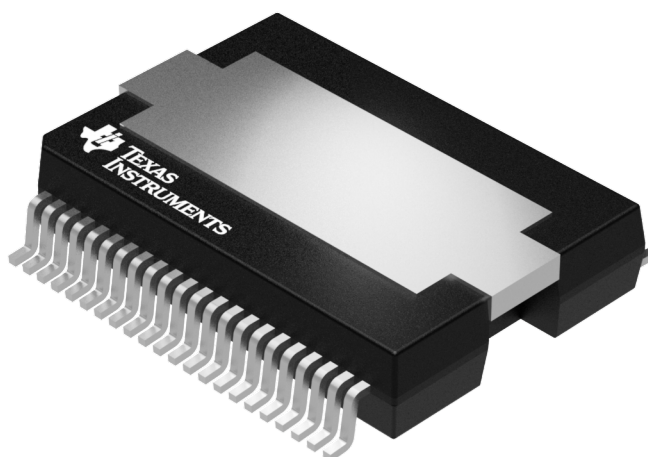
## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| TAS5615PHD   | PHD          | HTQFP        | 64   | 90  | 6 X 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |
| TAS5615PHD.A | PHD          | HTQFP        | 64   | 90  | 6 X 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

## GENERIC PACKAGE VIEW

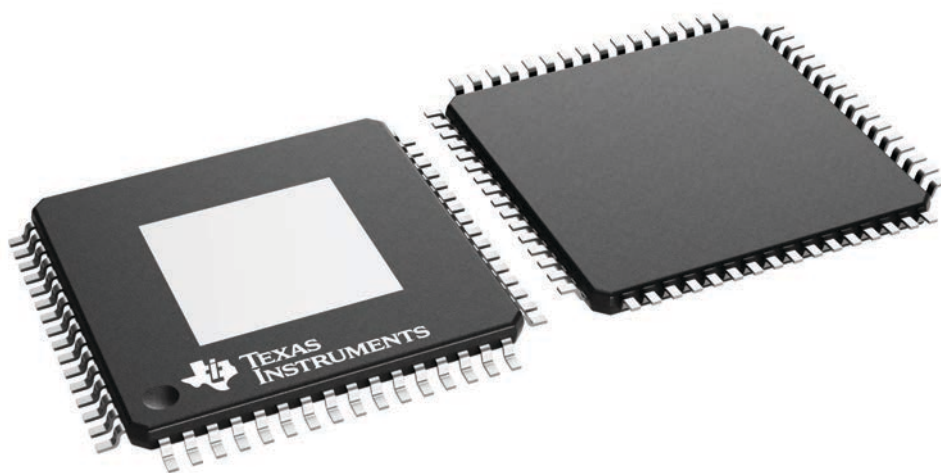
**PHD 64**

**HTQFP - 1.2 mm max height**

14 x 14, 0.8 mm pitch

PLASTIC QUAD FLATPACK

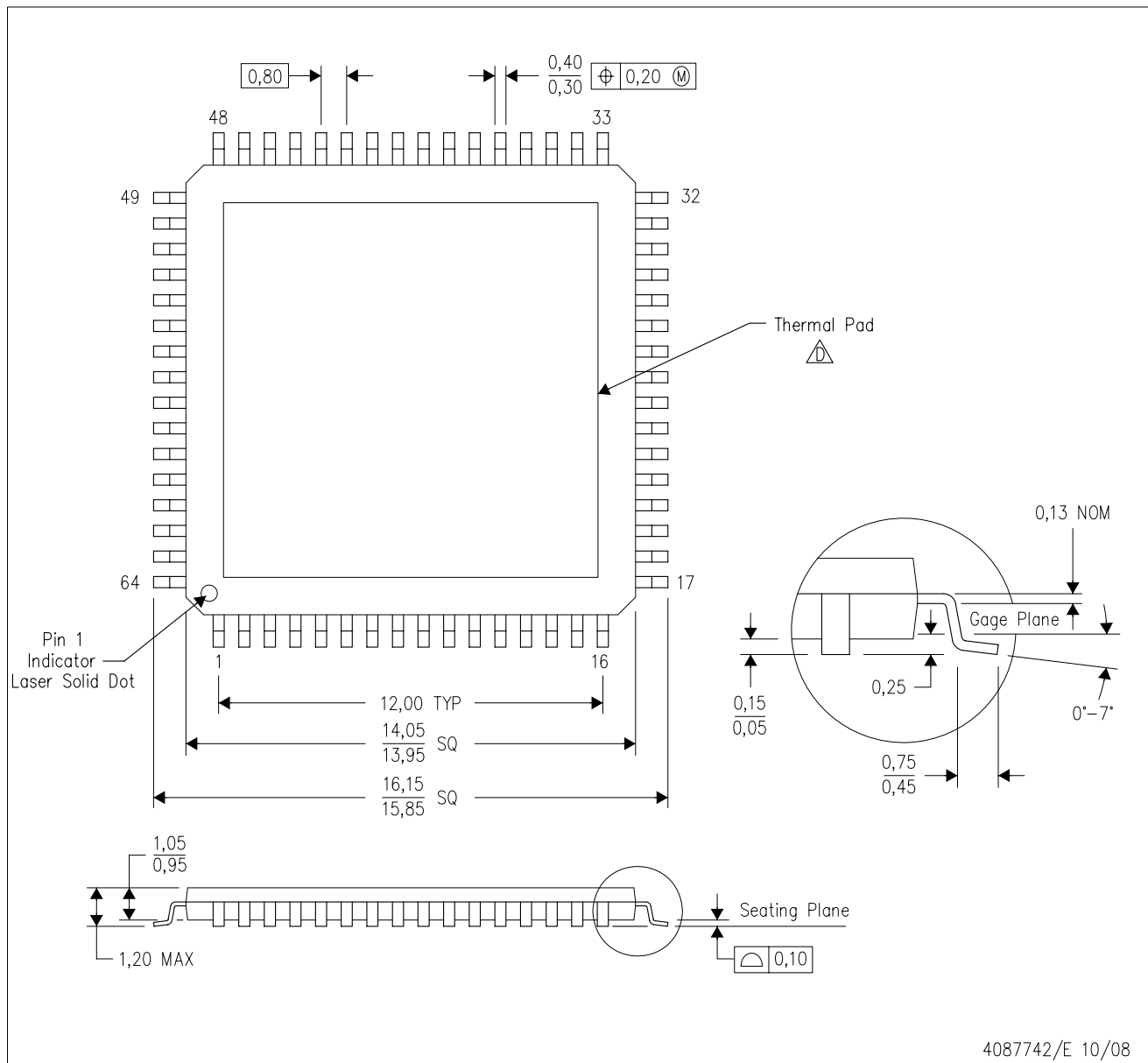
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224851/B

## MECHANICAL DATA

## PHD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  -  This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. See the product data sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MS-026

**PowerPAD is a trademark of Texas Instruments.**

## THERMAL PAD MECHANICAL DATA

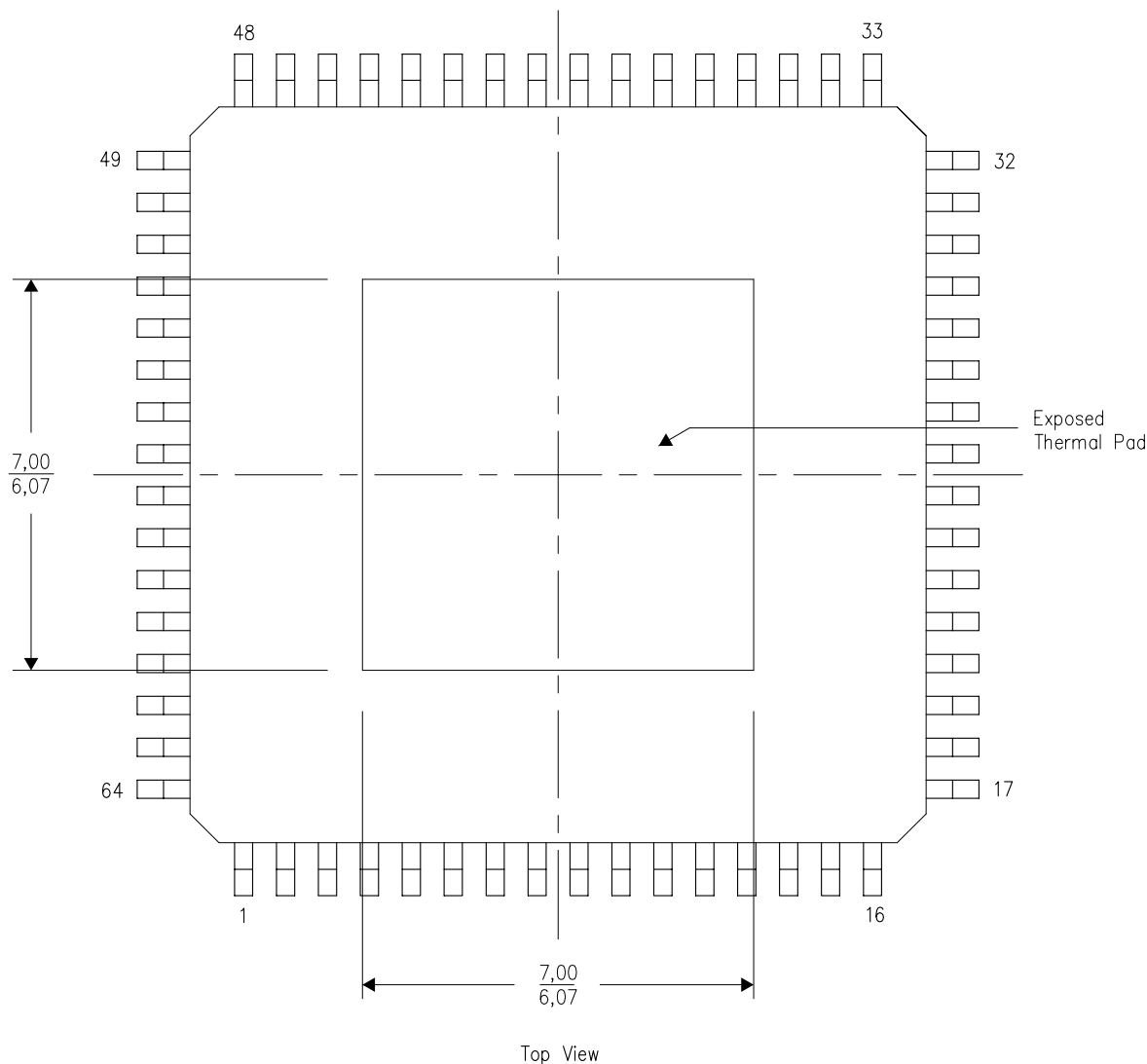
### PHD (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)

#### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206328-4/H 04/11

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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