SN65HVD0x, SN75HVD0x High Output RS-485 Transceivers

1 Features

- Minimum differential output voltage of 2.5 V Into a 54-Ω load
- Open-circuit, short-circuit, and idle-bus failsafe receiver
- 1/8th Unit-load option available (Up to 256 nodes on the bus)
- Bus-pin ESD protection exceeds 16 kV HBM
- Driver output slew rate control options
- Electrically compatible with ANSI TIA/EIA-485-A standard
- Low-current standby mode: 1 µA typical
- Glitch-free power-up and power-down protection for hot-plugging applications
- Pin compatible with industry standard SN75176

2 Applications

- Data transmission over long or lossy lines or electrically noisy environments
- Profibus line interface
- Industrial process control networks
- Point-of-sale (POS) networks
- Electric utility metering
- Building automation
- Digital motor control

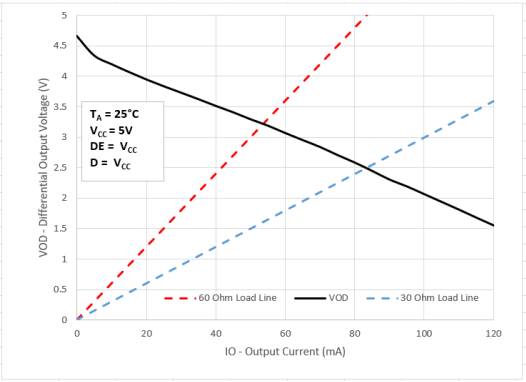


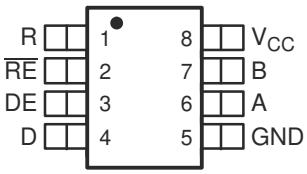
Figure 3-1. Differential Output Voltage vs Differential Output Current

3 Description

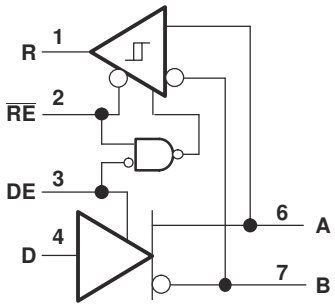
The SN65HVD05, SN75HVD05, SN65HVD06, SN75HVD06, SN65HVD07, and SN75HVD07 combine a 3-state differential line driver and differential line receiver. They are designed for balanced data transmission and interoperate with ANSI TIA/EIA-485-A and ISO 8482E standard-compliant devices. The driver is designed to provide a differential output voltage greater than that required by these standards for increased noise margin. The drivers and receivers have active-high and active-low enables respectively, which can be externally connected together to function as direction control.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or not powered. These devices feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

D OR P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM
(POSITIVE LOGIC)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2009) to Revision F (March 2023)	Page
• Deleted the *Ordering Information* table	1
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics*	9

Changes from Revision D (July 2006) to Revision E (August 2009)	Page
• Added IDLE Bus to the Receivers Function Table	16
• Added the Receiver Failsafe paragraph	16

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

			SN65HVD05, SN65HVD06, SN65HVD07 SN75HVD05, SN75HVD06, SN75HVD07
Supply voltage range, V_{CC}			–0.3 V to 6 V
Voltage range at A or B			–9 V to 14 V
Input voltage range at D, DE, R or $\overline{RE}$			–0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 6-11)			–50 V to 50 V
Receiver output current, I_O			–11 mA to 11mA
Electrostatic discharge	Human body model(3)	A, B, and GND	16 kV
		All pins	4 kV
	Charged-device model(4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under" recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		–7(1)		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Figure 6-7)		–12		12	V
High-level output current, I_{OH}	Driver	–100			mA
	Receiver	–8			
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65HVD05	–40		85	°C
	SN65HVD06				
	SN65HVD07				
	SN75HVD05	0		70	°C
	SN75HVD06				
	SN75HVD07				

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.3 Thermal Information

THERMAL METRIC[1]		D (SOIC) SN65 Variation	D (SOIC) SN75 Variation	P (PDIP)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	175.4	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	53.6	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	45.1	23.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	10.1	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	44.4	23.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.4 Package Dissipation Ratings

(See Figure 5-1 and Figure 5-2)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR[1] ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D[2]	710 mW	5.7 mW/°C	455 mW	369 mW
D[3]	1282 mW	10.3 mW/°C	821 mW	667 mW
P	1000 mW	8.0 m W/°C	640 mW	520 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

5.5 Driver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA		–1.5			V
$\|V_{OD}\|$	Differential output voltage		No Load				V_{CC}	V
			R_L = 54 Ω, See Figure 6-4		2.5			
			V_{test} = –7 V to 12 V, See Figure 6-2		2.2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		See Figure 6-4 and Figure 6-2		–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 6-3		2.2		3.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD05	See Figure 6-3			600		mV
		HVD06				500		
		HVD07				900		
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			–100		0	μA
		DE			0		100	
I_{OS}	Short-circuit output current		–7 V ≤ V_O ≤ 12 V		–250		250	mA
$C_{(diff)}$	Differential output capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC} DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

5.6 Driver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD05	R_L = 54 Ω, C_L = 50 pF, See Figure 6-4		6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD05			6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_r	Differential output signal rise time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
t_f	Differential output signal fall time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD05				2	ns
		HVD06				2.5	
		HVD07				10	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD05				3.5	ns
		HVD06				14	
		HVD07				100	
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See Figure 6-5			25	ns
		HVD06				45	
		HVD07				250	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD05				25	ns
		HVD06				60	
		HVD07				250	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See Figure 6-6			15	ns
		HVD06				45	
		HVD07				200	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD05				14	ns
		HVD06				90	
		HVD07				550	
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110Ω , $\overline{RE}$ at 3 V, See Figure 6-5			6	µs
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 6-6			6	µs

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.7 Receiver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = –8 mA					–0.01	V
V_{IT-}	Negative-going input threshold voltage		I_O = 8 mA			–0.2			
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})						35		mV
V_{IK}	Enable-input clamp voltage		I_I = –18 mA			–1.5			V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = –8 mA,	See Figure 6-7	4			V
V_{OL}	Low-level output voltage		V_{ID} = -200 mV,	I_{OL} = 8 mA,	See Figure 6-7			0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC}	$\overline{RE}$ at V_{CC}		–1		1	µA
I_I	Bus input current	HVD05	Other inputat 0 V	V_A or V_B = 12 V			0.23	0.5	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.3	0.5	
				V_A or V_B = –7 V		–0.4	0.13		
				V_A or V_B = –7 V,	V_{CC} = 0 V	–0.4	0.15		
		HVD06 HVD07	Other inputat 0 V	V_A or V_B = 12 V			0.06	0.1	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.08	0.13	
				V_A or V_B = –7 V		–0.1	0.05		
				V_A or V_B = –7 V,	V_{CC} = 0 V	–0.05	0.03		
I_{IH}	High-level input current, $\overline{RE}$		V_{IH} = 2 V			–60	26.4		µA
I_{IL}	Low-level input current, $\overline{RE}$		V_{IL} = 0.8 V			–60	27.4		µA
$C_{(diff)}$	Differential input capacitance		V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V				16		pF
I_{CC}	Supply current		$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled and driver disabled			5	10	mA
			$\overline{RE}$ at V_{CC}, DE at 0 V, D at V_{CC}, No load	Receiver disabled and driver disabled (standby)			1	5	µA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled			9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

5.8 Receiver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output 1/2 UL	HVD05	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 6-8		14.6	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output 1/2 UL	HVD05			14.6	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
t_{PHL}	Propagation delay time, high-to-low-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD05				2	ns
		HVD06				4.5	
		HVD07				4.5	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD05				6.5	ns
		HVD06				14	
		HVD07				14	
t_r	Output signal rise time		C_L = 15 pF, See Figure 6-8		2	3	ns
t_f	Output signal fall time				2	3	
t_{PZH1}	Output enable time to high level		C_L = 15 pF, DE at 3 V, See Figure 6-9			10	ns
t_{PZL1}	Output enable time to low level					10	
t_{PHZ}	Output disable time from high level					15	
t_{PLZ}	Output disable time from low level					15	
t_{PZH2}	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0, See Figure 6-10			6	µs
t_{PZL2}	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.9 Typical Characteristics

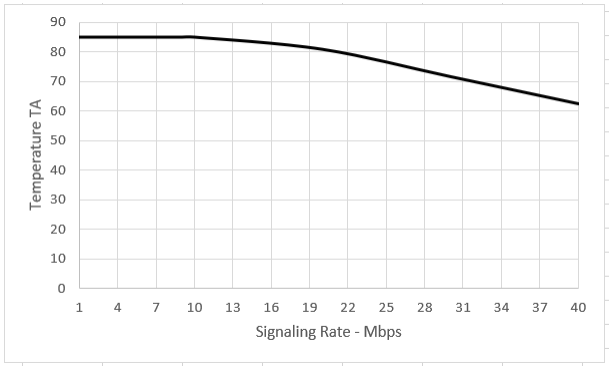


Figure 5-1. HVD05 Maximum Recommended Still-Air Operating Temperature vs Signaling Rate (D-Package)

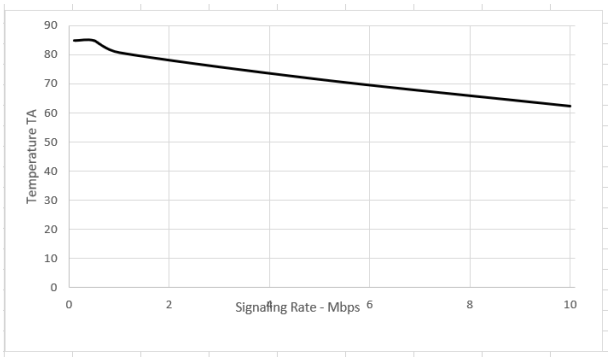


Figure 5-2. HVD06 Maximum Recommended Still-Air Operating Temperature vs Signaling Rate (D-Package)

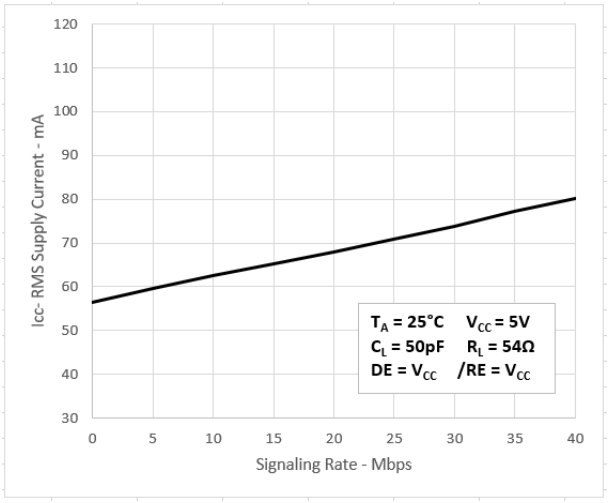


Figure 5-3. HVD05 RMS Supply Current vs Signaling Rate

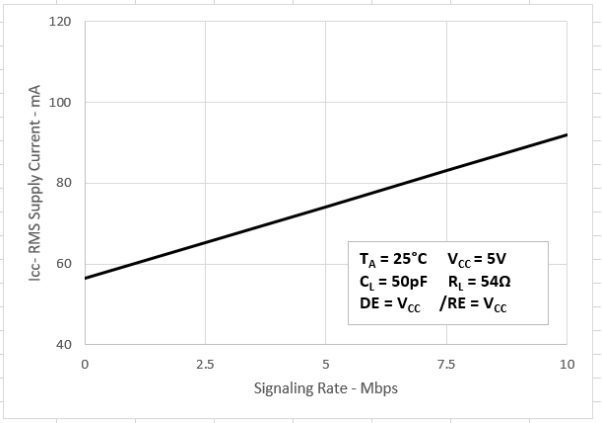


Figure 5-4. HVD06 RMS Supply Current vs Signaling Rate

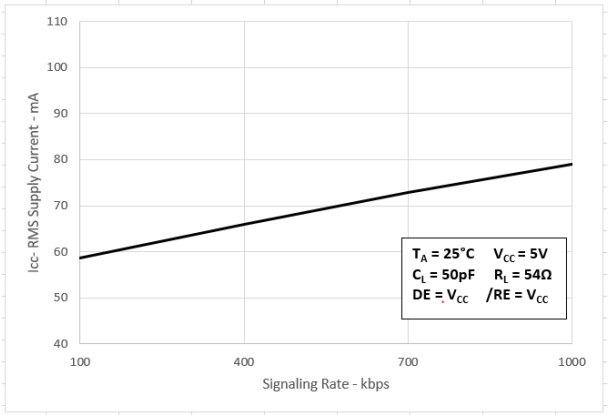


Figure 5-5. HVD07 RMS Supply Current vs Signaling Rate

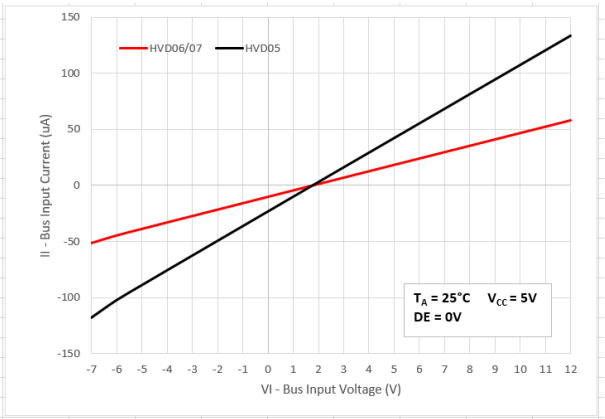


Figure 5-6. BUS Input Current vs BUS Input Voltage

5.9 Typical Characteristics (continued)

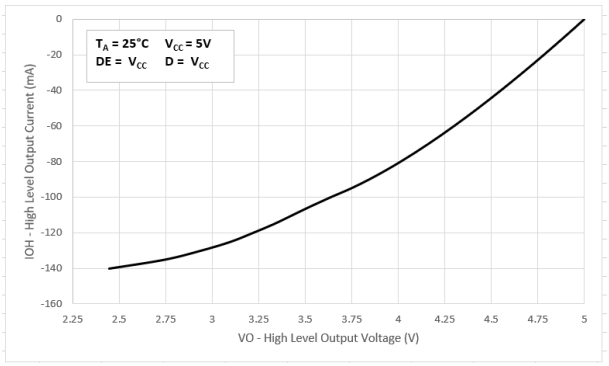


Figure 5-7. Driver High-Level Output Current vs High-Level Output Voltage

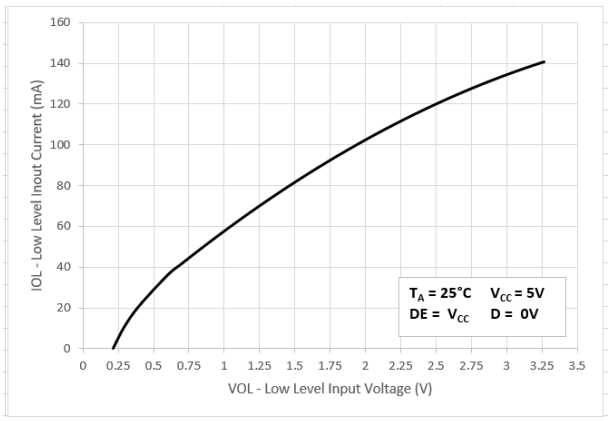


Figure 5-8. Driver Low-Level Output Current vs Low-Level Output Voltage

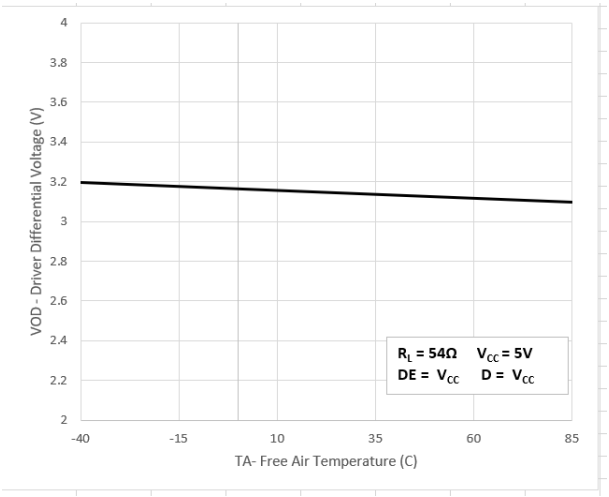


Figure 5-9. Differential Output Voltage vs Free-Air Temperature

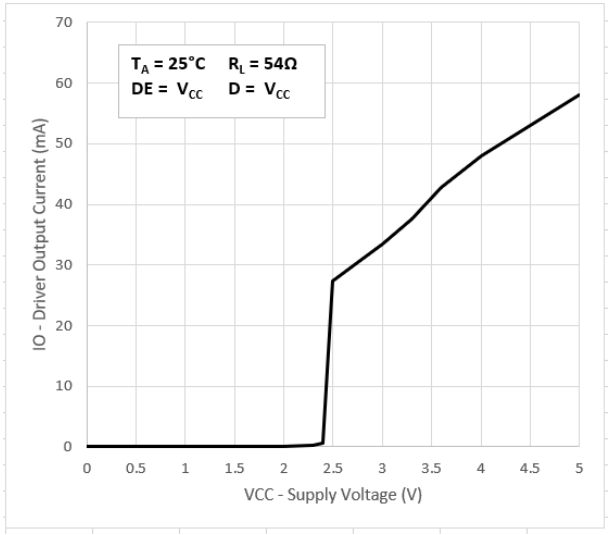


Figure 5-10. Driver Output Current vs Supply Voltage

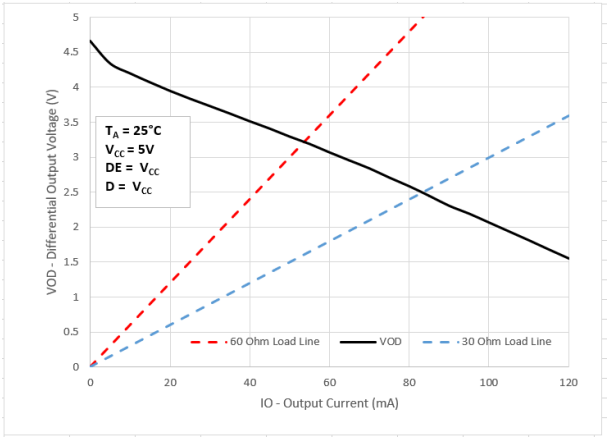


Figure 5-11. Differential Output Voltage vs Differential Output Current

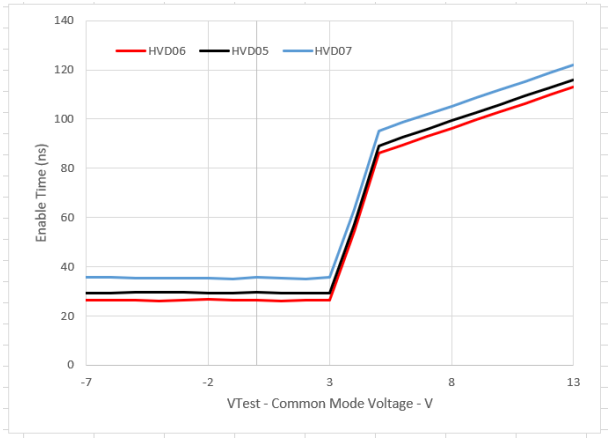


Figure 5-12. Enable Time vs Common-Mode Voltage (See Figure 5-13)

5.9 Typical Characteristics (continued)

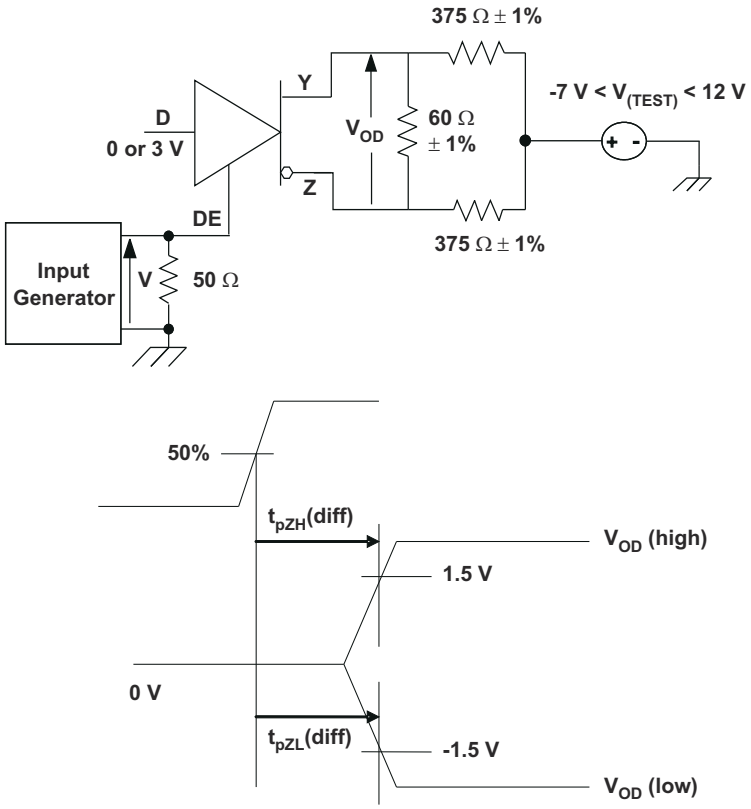


Figure 5-13. Driver Enable Time From DE to V_{OD}

Parameter Measurement Information

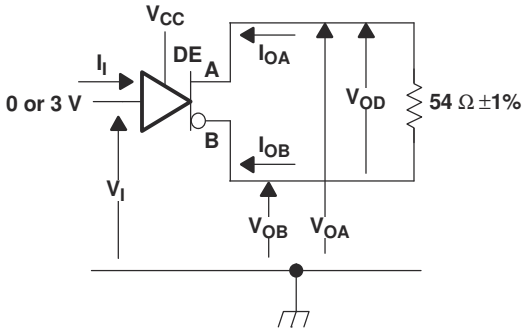


Figure 6-1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

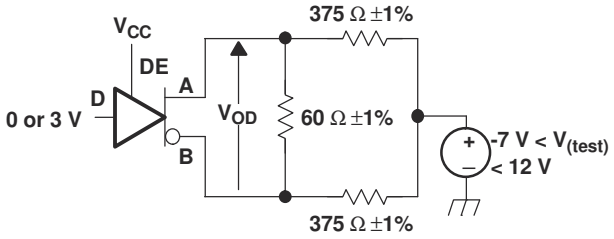
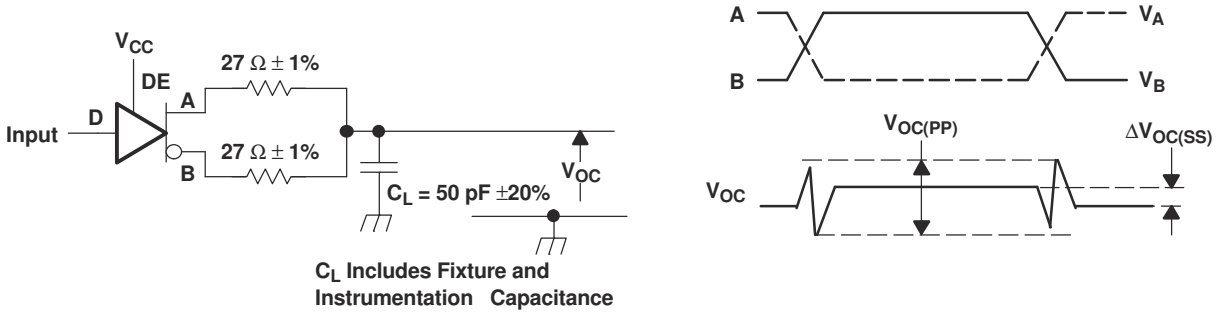
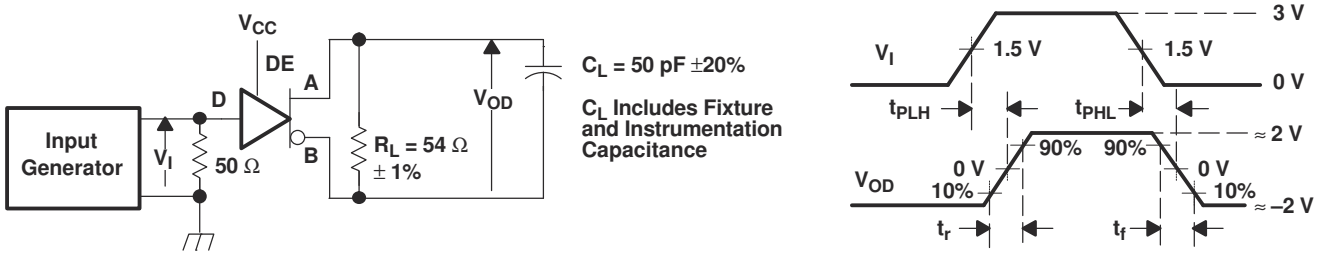


Figure 6-2. Driver V_{OD} With Common-Mode Loading Test Circuit



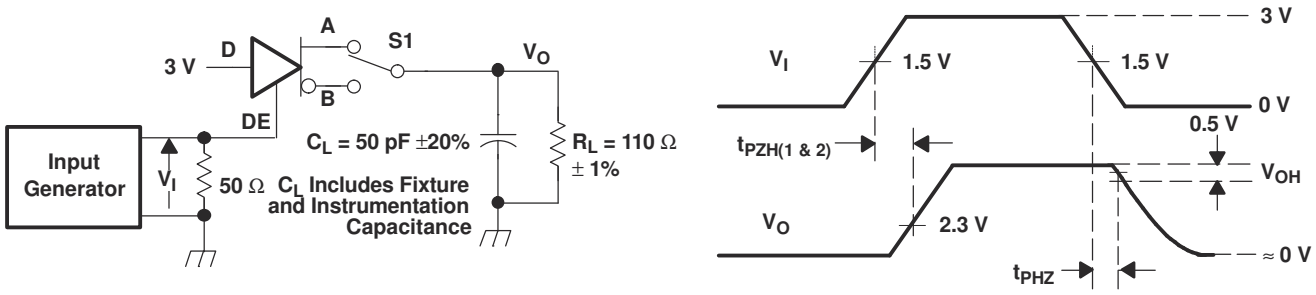
Input: PRR = 500 kHz, 50% Duty Cycle, t_r<6ns, t_f<6ns, Z_O = 50 Ω

Figure 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



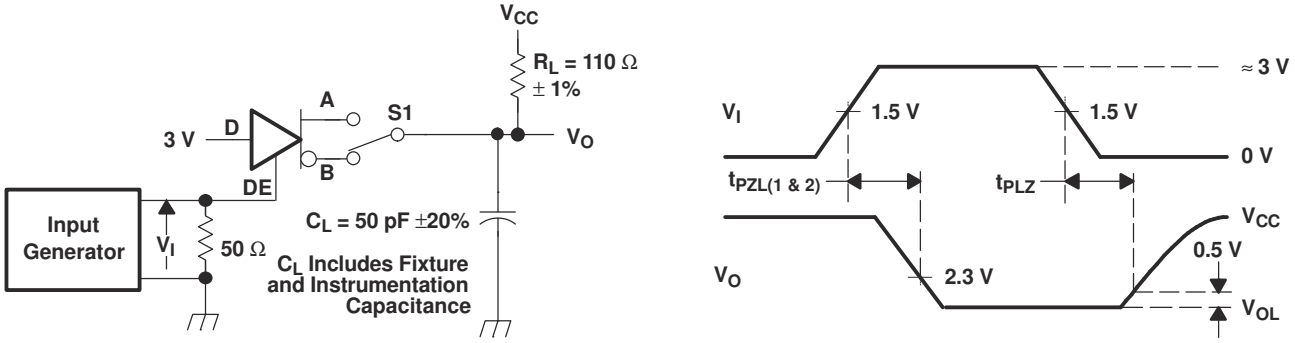
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 6-4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 6-5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 6-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

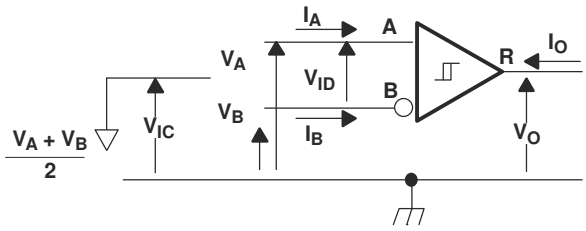
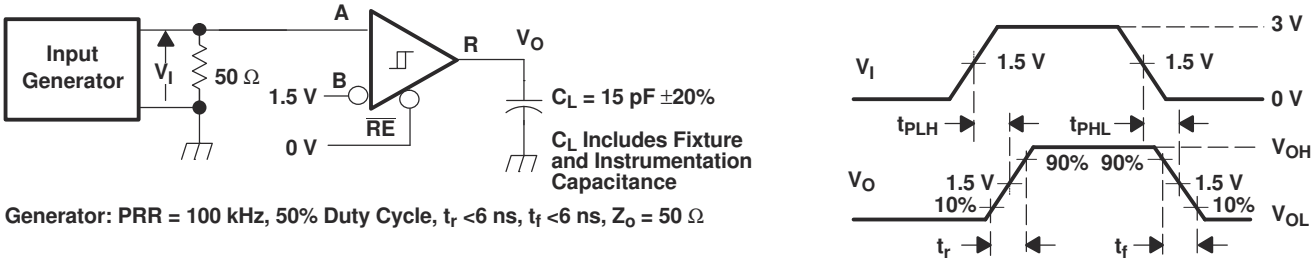


Figure 6-7. Receiver Voltage and Current Definitions



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 6-8. Receiver Switching Test Circuit and Voltage Waveforms

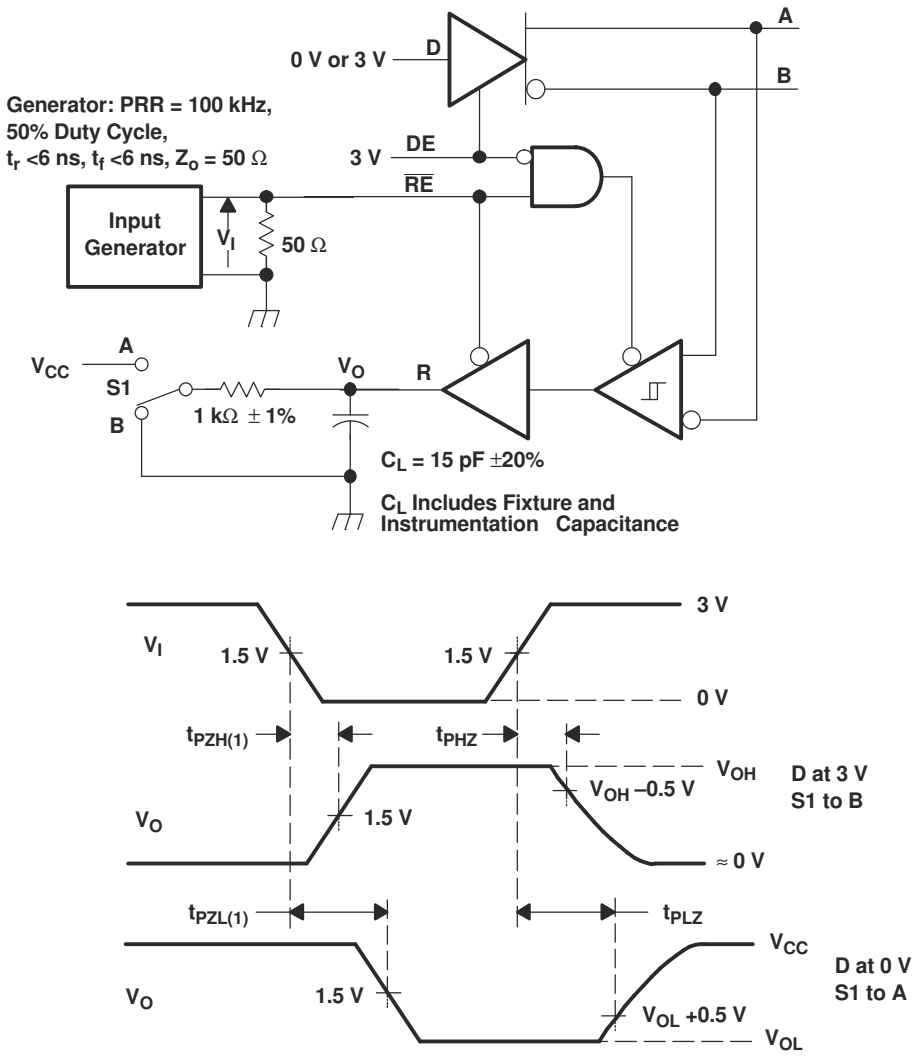


Figure 6-9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

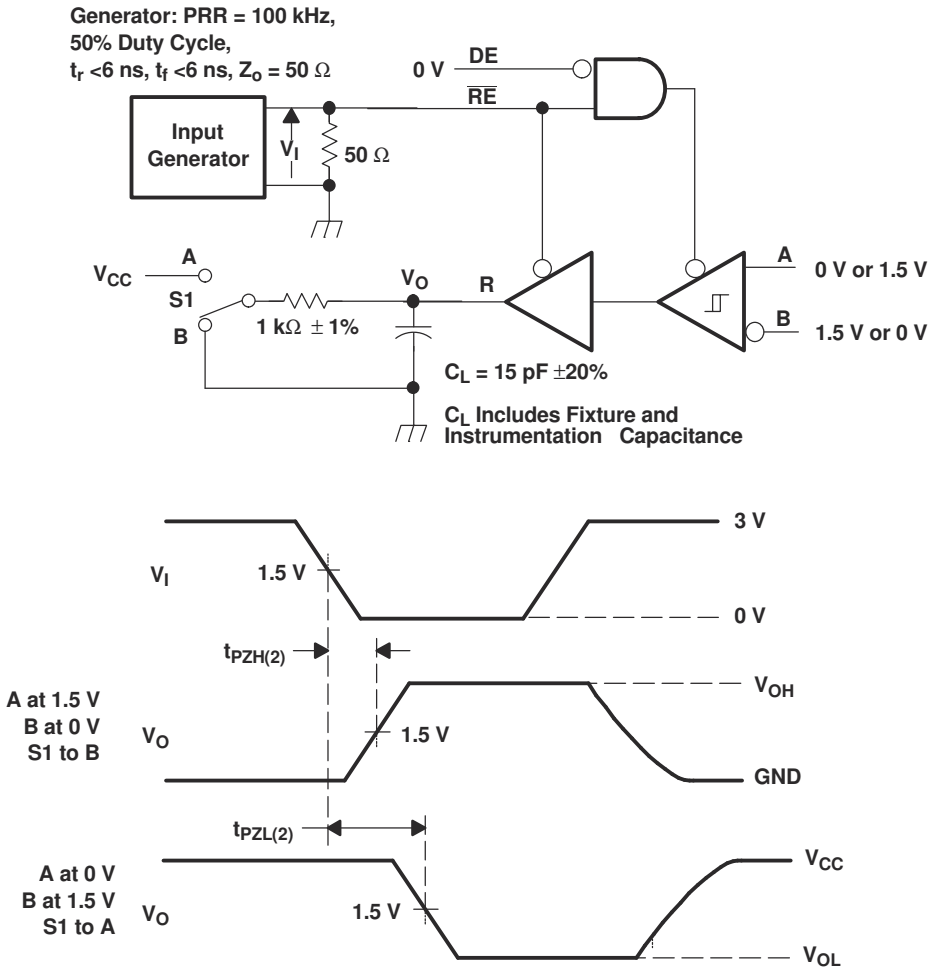
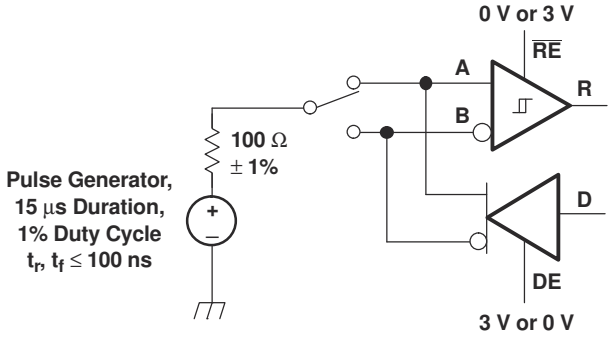


Figure 6-10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 6-11. Test Circuit, Transient Over Voltage Test

6 Function Tables

Table 6-1. DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L
X	Open	Z	Z

Table 6-2. RECEIVER

DIFFERENTIAL INPUTS(1)	ENABLE	OUTPUT
$V_{ID} = V_A – V_B$	$\overline{RE}$	R
$V_{ID} \leq –0.2$ V	L	L
$–0.2 V < V_{ID} < –0.01$ V	L	?
$–0.01 V \leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H
IDLE Bus	L	H
X	Open	Z

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

6.1 Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

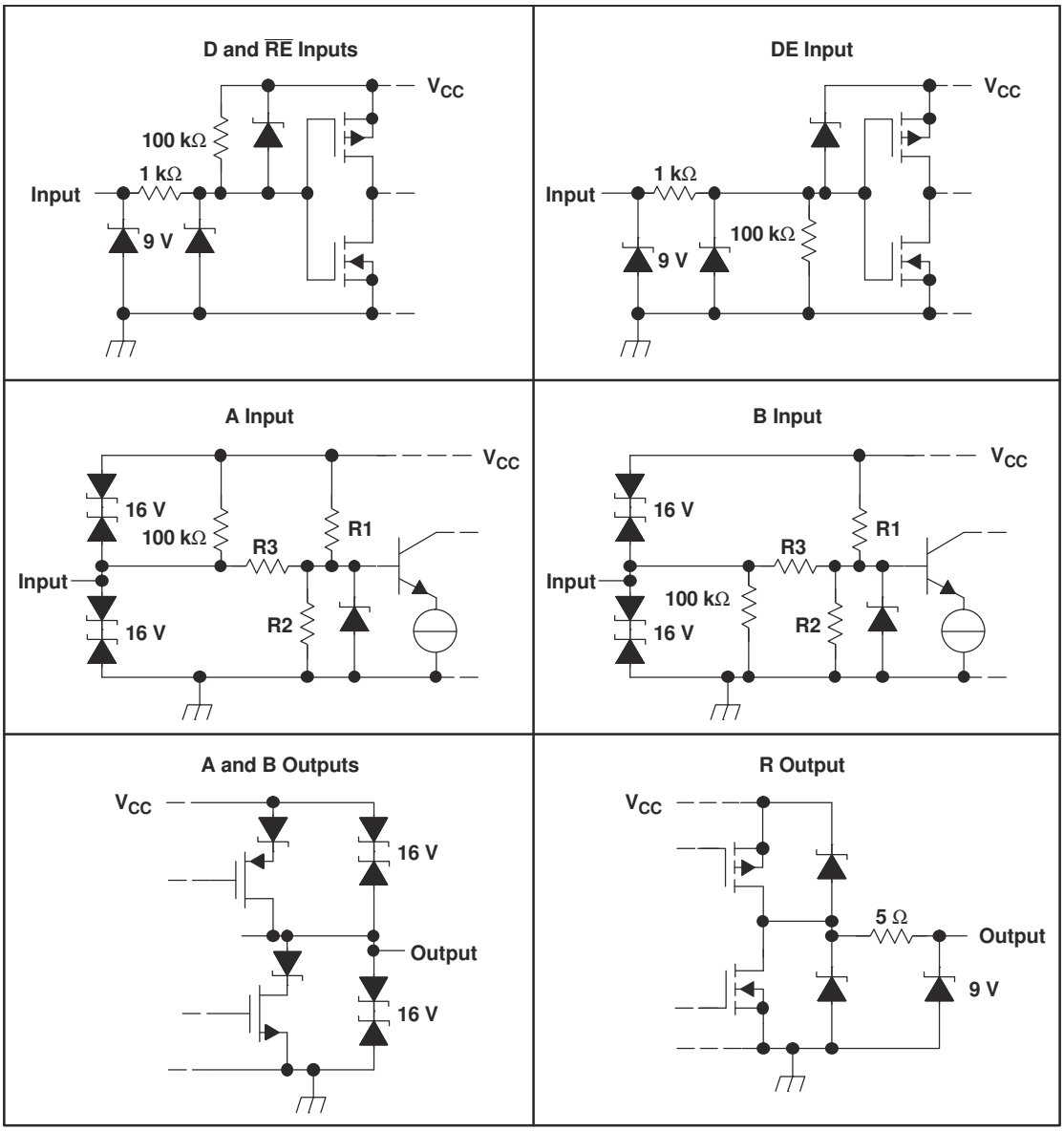
- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output *must* output a High when the differential input V_{ID} is more positive than +200 mV, and *must* output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. As seen in the Receiver Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will *always* cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

7 Equivalent Input and Output Schematic Diagrams



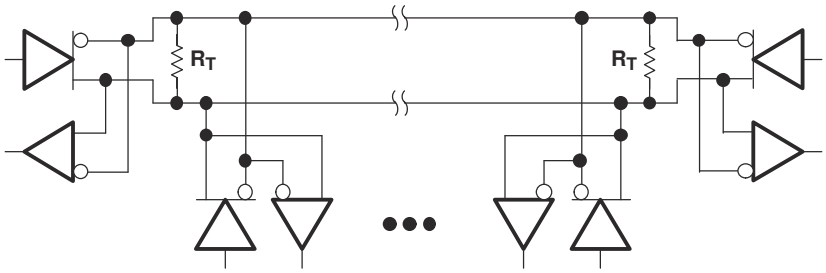
	R1/R2	R3
SN65HVD05	9 kΩ	45 kΩ
SN65HVD06	36 kΩ	180 kΩ
SN65HVD07	36 kΩ	180 kΩ

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

Typical Application



Device	Number of Devices on Bus
HVD05	64
HVD06	256
HVD07	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 8-1. Typical Application Circuit

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD05D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP05
SN65HVD05DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD05
SN65HVD05P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD05
SN65HVD06DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP06
SN65HVD06DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP06
SN65HVD06P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD06
SN65HVD06P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD06
SN65HVD07D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP07
SN65HVD07DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD07
SN65HVD07P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD07
SN75HVD05D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN05
SN75HVD05P	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	0 to 70	75HVD05
SN75HVD06D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD06D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD06DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD06DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD07D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD07

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75HVD07P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD07

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

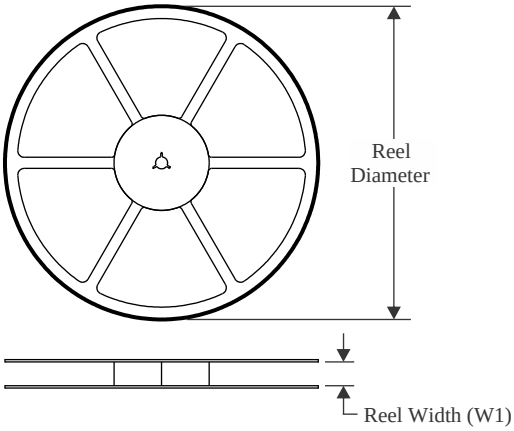
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

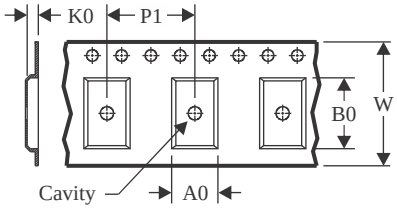
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

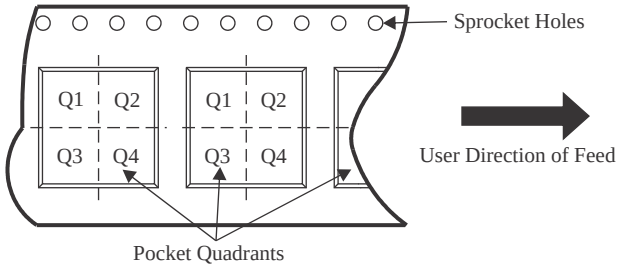


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

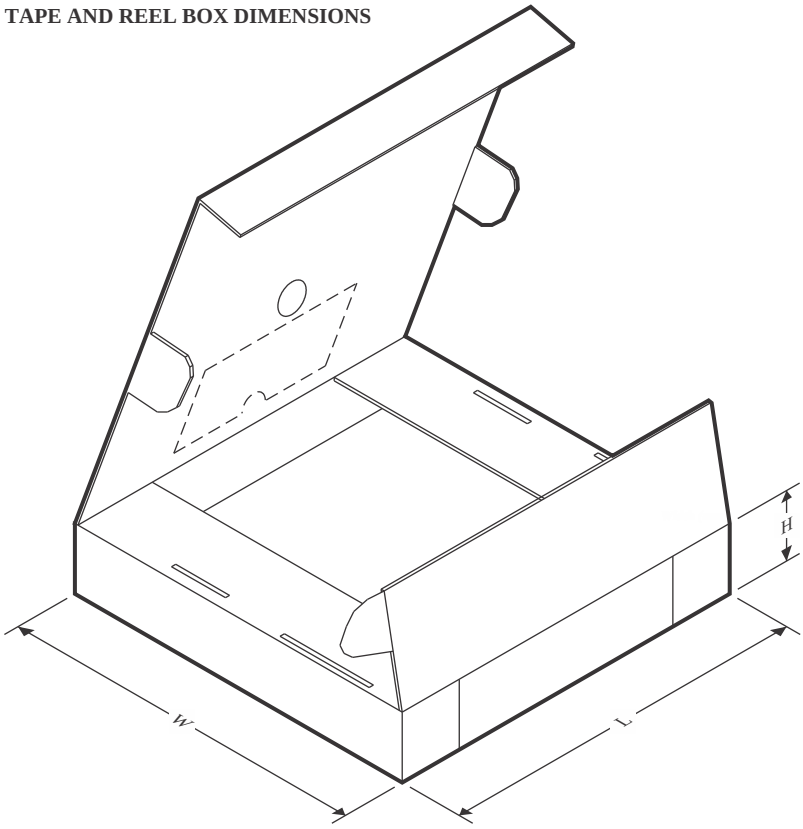
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD05DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD05DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD06DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD07DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD07DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD06DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD07DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

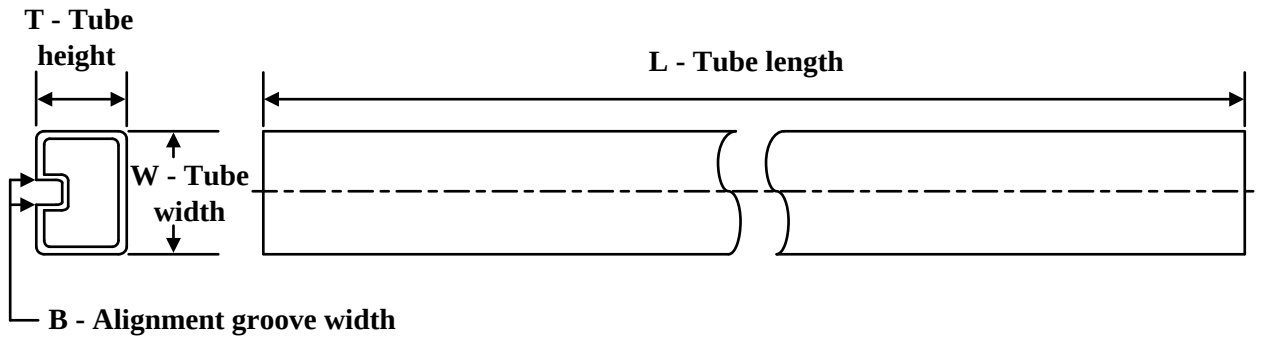
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

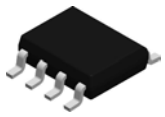
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD05DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD05DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD06DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD07DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD07DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN75HVD06DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75HVD07DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD05P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD05P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD06P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD06P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD07P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD07P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD06D	D	SOIC	8	75	507	8	3940	4.32
SN75HVD06D.A	D	SOIC	8	75	507	8	3940	4.32
SN75HVD07D	D	SOIC	8	75	507	8	3940	4.32
SN75HVD07D.A	D	SOIC	8	75	507	8	3940	4.32
SN75HVD07P	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD07P.A	P	PDIP	8	50	506	13.97	11230	4.32

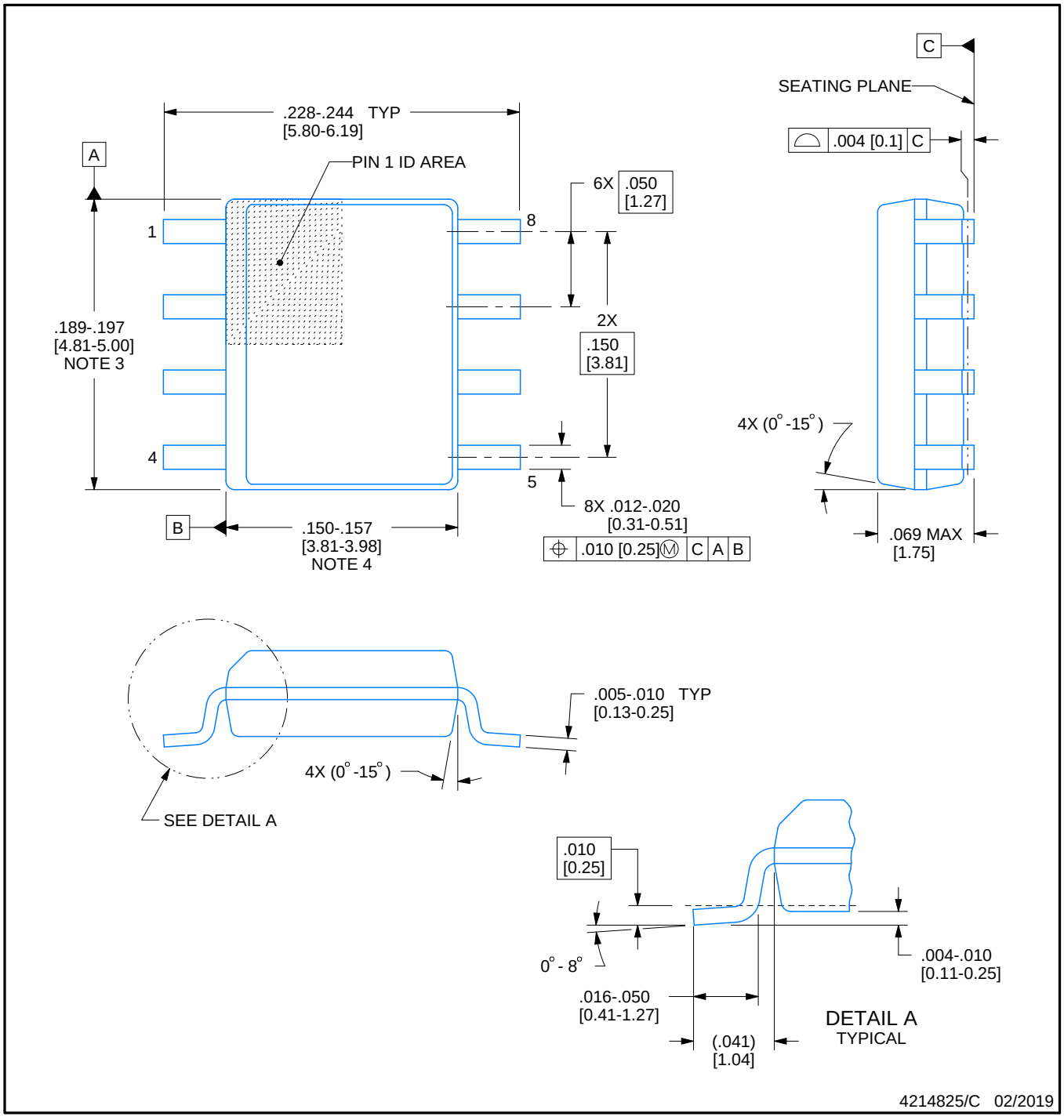


PACKAGE OUTLINE

D0008A

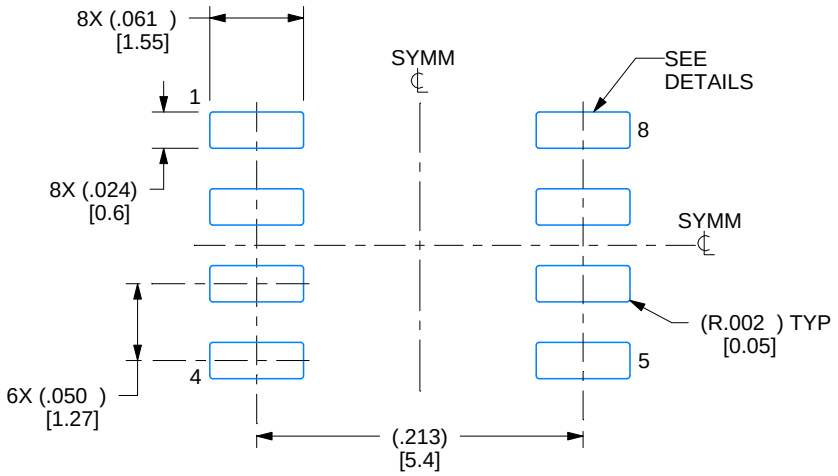
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

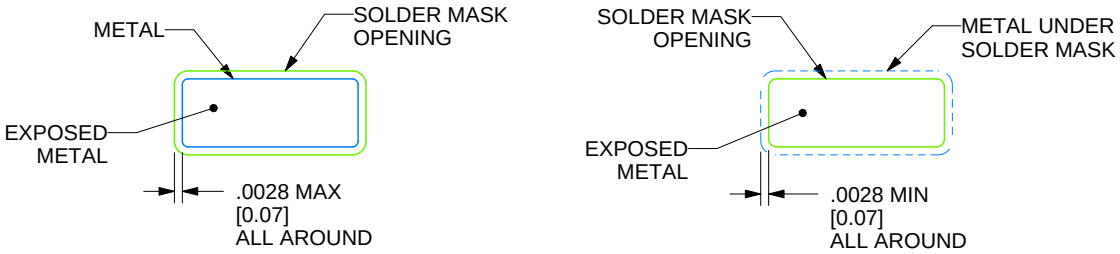


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

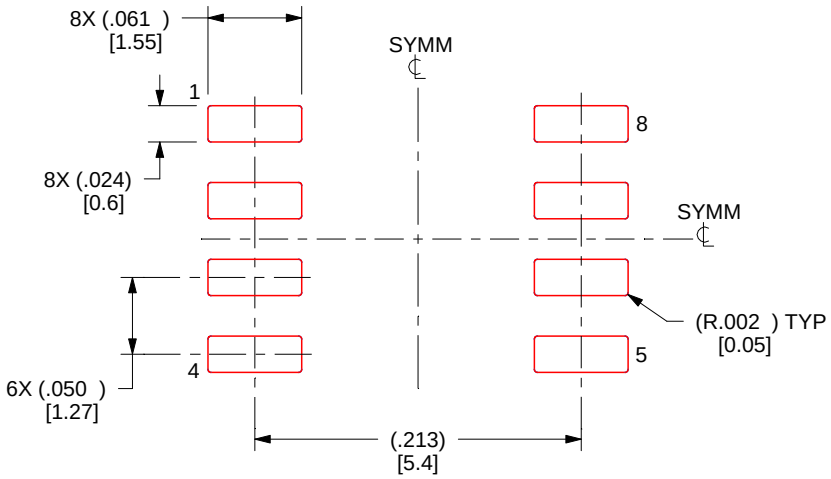
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



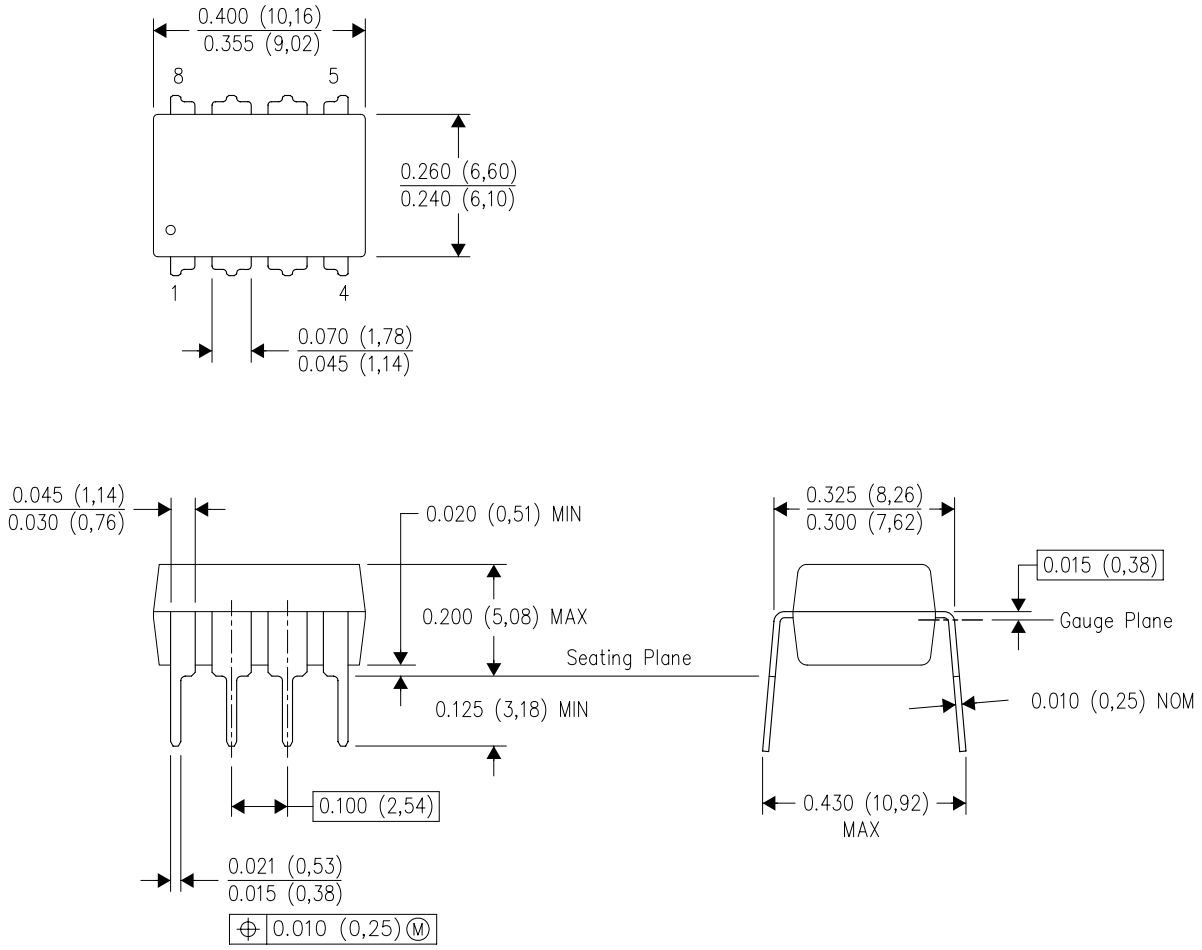
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Last updated 10/2025