SN5545xB, SN7545xB Dual-Peripheral Drivers for High-Current, High-Speed Switching

1 Features

- Characterized for use to 300mA
- High-voltage outputs up to 30V
- No output latch-up at 20V (after conducting 300mA)
- High-speed switching
- Open-collector outputs
- Circuit flexibility for varied applications
- TTL compatible diode-clamped inputs
- Standard supply voltages

2 Applications

- High-speed logic buffers
- Power drivers
- Lamp drivers
- LED drivers
- Line drivers
- Memory drivers

3 Description

The SN5545xB and SN7545xB devices are dual-peripheral drivers designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the devices is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design.

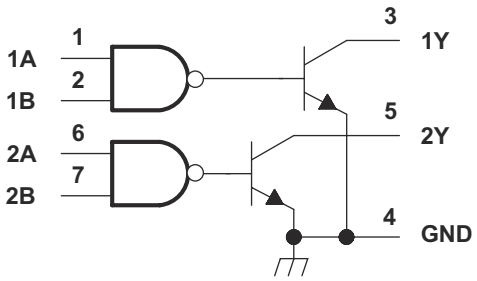
The SNx5451B, SNx5452B, SNx5453B, and SNx5454B devices are dual peripheral AND, NAND, OR, and NOR drivers, respectively (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

The SN5545xB drivers are characterized for operation over the full military range of –55°C to 125°C. The SN7545xB drivers are characterized for operation from 0°C to 70°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN7545xBP	PDIP (8)	9.81mm × 6.35mm
SN7545xBD	SOIC (8)	4.90mm × 3.90mm
SN7545xBPS	SO (8)	6.20mm x 5.30mm
SN5545xBJG	CDIP (8)	9.60mm × 6.67mm
SN5545xBFK	LCCC (20)	8.89mm × 8.89mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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SN75451B Logic Diagram

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4 Device Comparison Table

DEVICE	LOGIC OF COMPLETE CIRCUIT	OPERATING FREE AIR TEMPERATURE RANGE
SN55451B	AND	–55°C to 125°C
SN55452B	NAND	–55°C to 125°C
SN55453B	OR	–55°C to 125°C
SN55454B	NOR	–55°C to 125°C
SN75451B	AND	0°C to 70°C
SN75452B	NAND	0°C to 70°C
SN75453B	OR	0°C to 70°C
SN75454B	NOR	0°C to 70°C

5 Pin Configuration and Functions

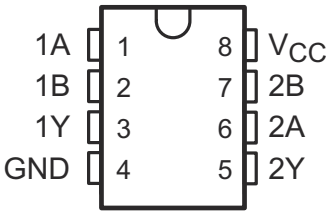
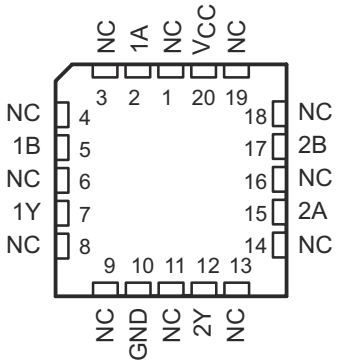


Figure 5-1. JG, D, P, or PS Package 8-Pin CDIP, SOIC, PDIP, or SO Top View



NC – No internal connection

Figure 5-2. FK Package 20-Pin LCCC Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, SOIC, PDIP, SO	LCCC		
1A	1	2	I	Channel 1 Logic Input A
1B	2	5	I	Channel 1 Logic Input B
1Y	3	7	O	Channel 1 Driver
2A	6	15	I	Channel 2 Logic Input A
2B	7	17	I	Channel 2 Logic Input B
2Y	5	12	O	Channel 2 Driver
GND	4	10	—	Ground
NC	—	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	No Internal Connection
VCC	8	20	—	Supply Voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage, (see (2))			7	V
V_I	Input voltage			5.5	V
	Inter-emitter voltage (see Note (3))			5.5	V
V_O	Off-state output voltage			30	V
I_{OK}	Continuous collector or output current, (see Note (4))			400	mA
	Peak collector or output current, II (tw ≤ 10 ms, duty cycle ≤ 50%, see Note (5))			500	mA
	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature	SN5545xB	–55	125	°C
		SN7545xB	0	70	
	Case temperature for 60 seconds	SN5545xB FK package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	SN5545xB JG package		100	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	SN7545xB D or P package		260	°C
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network GND, unless otherwise specified.
(3) This is the voltage between two emitters of a multiple-emitter transistor.
(4) This value applies when the base-emitter resistance (RBE) is equal to or less than 500 Ω.
(5) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN5545xB	4.5	5	5.5	V
		SN7545xB	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
T_A	Operating free-air temperature	SN5545xB	–50		125	°C
		SN7545xB	0		70	

6.3 Thermal Information

THERMAL METRIC(1)		SN7545xB			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.2	63.7	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.4	53.6	71.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.4	40.8	68.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.2	31.1	31.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.0	40.8	67.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = – 12 mA			–1.2	–1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, IOL = 100 mA	SN5545xB		0.25	0.5	V
			SN7545xB		0.25	0.4	
		V_{CC} = MIN, V_{IL} = 0.8 V, IOL = 300 mA	SN5545xB		0.5	0.8	
			SN7545xB		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, VOH = 30 V	SN5545xB			300	µA
			SN7545xB			100	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			–1	–1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V	SNx5451B		7	11	mA
			SNx5453B		8	11	
		V_{CC} = MAX, V_I = 0 V	SNx5452B		11	14	
			SNx5454B		13	17	
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0 V	SNx5451B		52	65	mA
			SNx5453B		54	68	
		V_{CC} = MAX, V_I = 5 V	SNx5452B		56	71	
			SNx5454B		61	79	

6.5 Switching Characteristics, V_{CC} = 5 V, T_A = 25°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 7-1	SNx5451B, SNx5453B		18	25	ns
			SNx5452B		26	35	
			SNx5454B		27	35	
t_{PHL}	Propagation delay time, high-to-low-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 7-1	SNx5451B, SNx5453B		18	25	
			SNx5452B, SNx5454B		24	35	
tTLH	Transition time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 7-1			5	8	
t_{THL}	Transition time, high-to-low-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 7-1			7	12	
V_{OH}	High level output voltage after switching	VS = 20 V, IO 9 300 mA, See Figure 7-1	SN5545xB		V_S – 6.5		mV
			SN7545xB	V_S – 6.5			

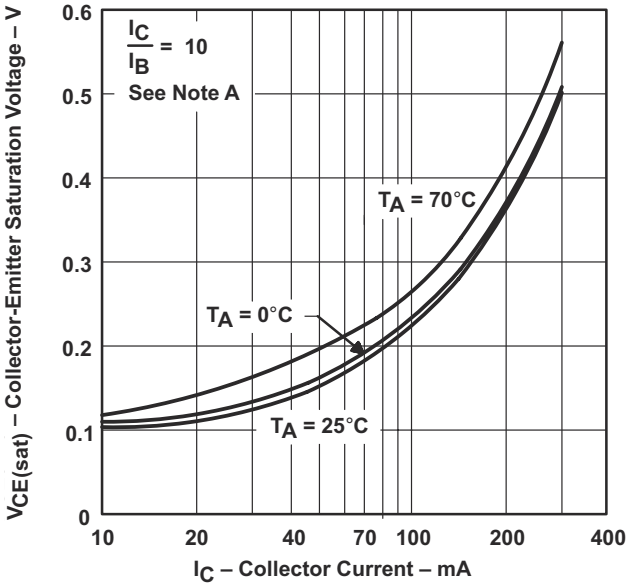
(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.

6.6 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464	—
FK	1375 mW	11.0 mW/°C	880	275 mW
JG	1050 mW	8.4 mW/°C	672	210 mW
P	1000 mW	8.0 mW/°C	640	—

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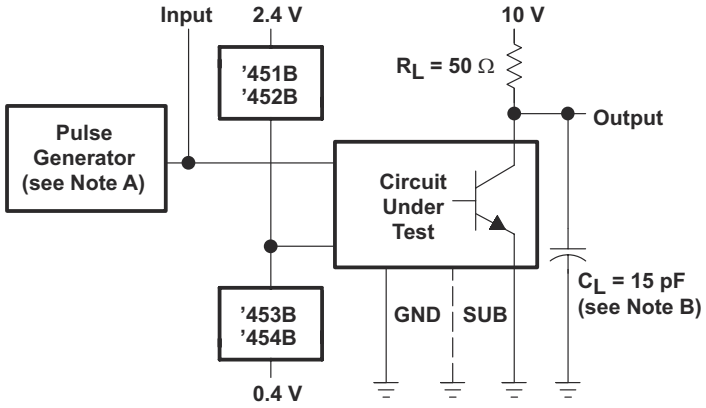
6.7 Typical Characteristics



NOTE A: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

Figure 6-1. Transistor Collector-Emitter Saturation Voltage vs Collector Current

7 Parameter Measurement Information

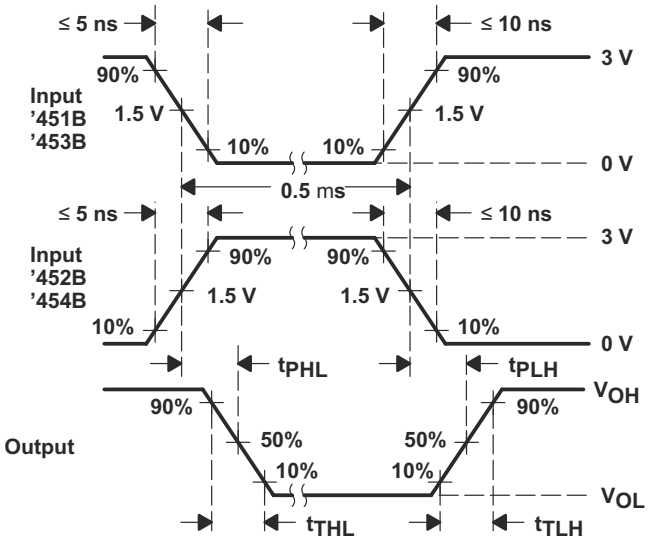


A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω.

B. CL includes probe and jig capacitance.

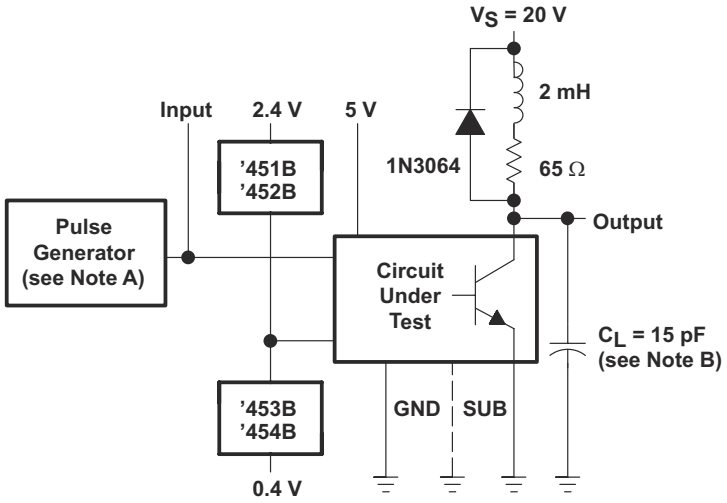
Figure 7-1. Test Circuit, Complete Drivers

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A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω.
B. CL includes probe and jig capacitance.

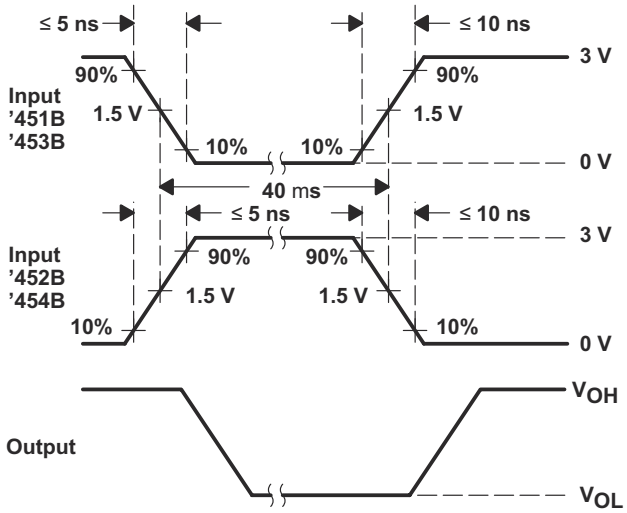
Figure 7-2. Waveforms, Complete Drivers



A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, ZO = 50 Ω.
B. CL includes probe and jig capacitance.

Figure 7-3. Test Circuit for Latch-Up Test of Complete Drivers

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A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, ZO = 50 Ω.
B. CL includes probe and jig capacitance.

Figure 7-4. Voltage Waveforms for Latch-Up Test of Complete Drivers

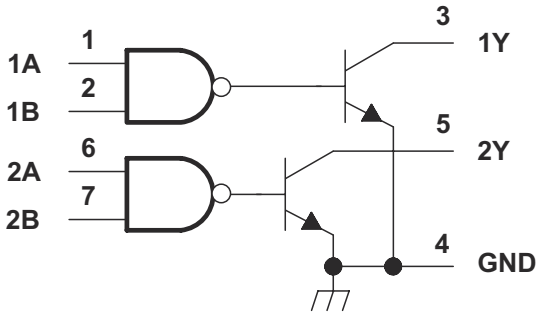
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8 Detailed Description

8.1 Overview

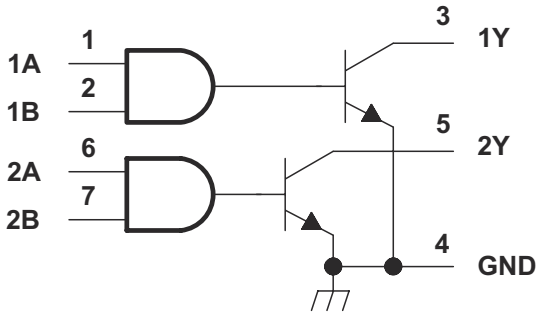
The SN7545xB and SN5545xB devices provide dual-output drivers with AND, NAND, NOR, or OR logic inputs. If each logic input is set to the appropriate voltage level, then the output driver will turn on, pulling the driver to ground and allowing current to flow.

8.2 Functional Block Diagrams



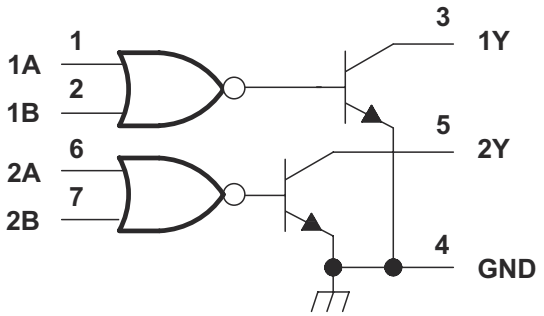
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Figure 8-1. SNx5451B Logic Diagram (Positive Logic)



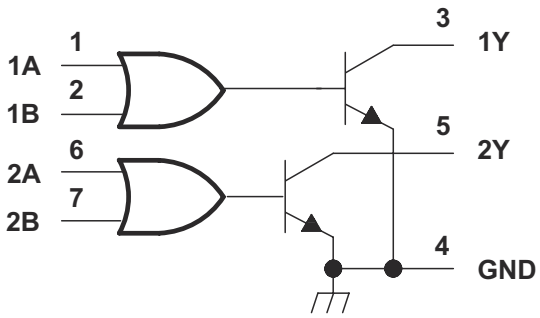
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Figure 8-2. SNx5452B Logic Diagram (Positive Logic)



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Figure 8-3. SNx5453B Logic Diagram (Positive Logic)



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Figure 8-4. SNx5454B Logic Diagram (Positive Logic)

8.3 Feature Description

The SNx5451B devices allow for high current driving up to 300 mA. This family of devices have AND, NAND, OR, or NOR input logic gates to allow for a wide variety of applications. The SN7545xB devices are rated for a commercial temperature range of 0°C to 70°C, and the SN5545xB devices are rated for a military temperature range of –65°C to 125°C.

8.4 Device Functional Modes

Table 8-1, Table 8-2, Table 8-3, and Table 8-4 list the functional modes of the SNx545xB.



Figure 8-5. SNx5451B Logic Symbol

Table 8-1. SNx5451B Function Table

A	B	Y (1)
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

(1) Positive logic: Y = AB or NOT($\overline{A}$ + $\overline{B}$)

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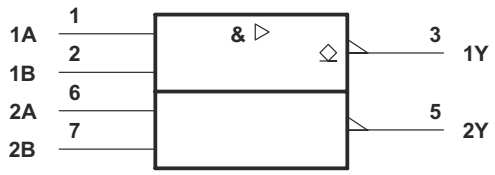


Figure 8-6. SNx5452B Logic Symbol

Table 8-2. SNx5452B Function Table

A	B	Y (1)
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

(1) Positive logic: Y = $\overline{AB}$ or $\overline{A}$ + $\overline{B}$

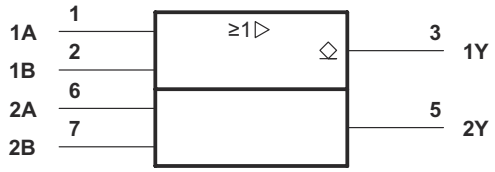


Figure 8-7. SNx5453B Logic Symbol

Table 8-3. SNx5453B Function Table

A	B	Y(1)
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

(1) Positive logic: Y = A+B or NOT($\overline{A}$ $\overline{B}$)

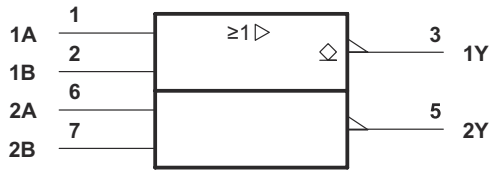
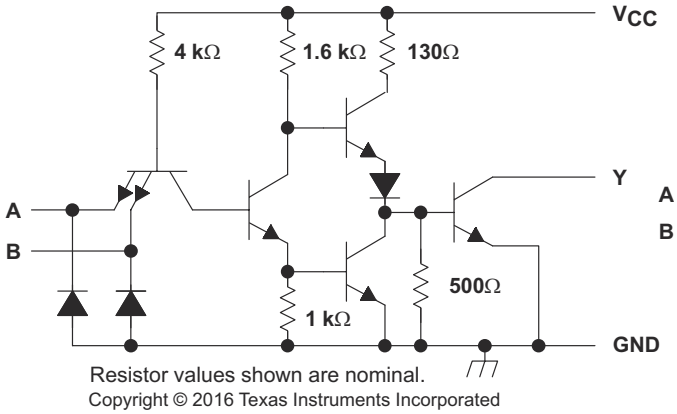


Figure 8-8. SNx5454B Logic Symbol

Table 8-4. SNx5454B Function Table

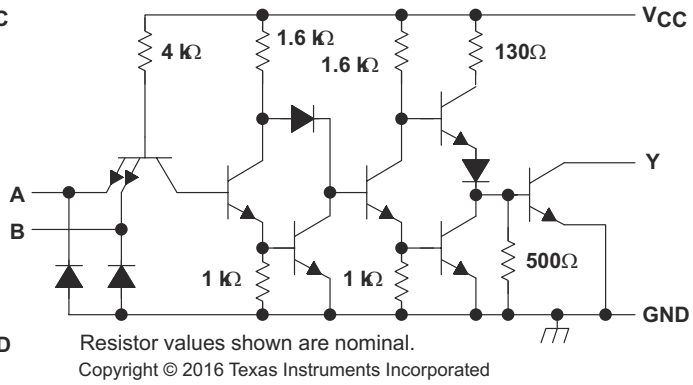
A	B	Y (1)
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

(1) Positive logic: Y = $\overline{A+B}$ or $\overline{A}$ $\overline{B}$



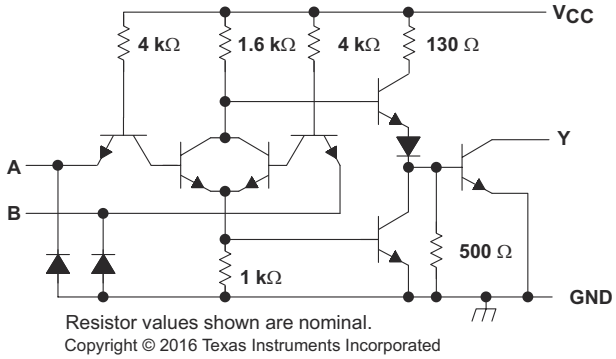
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Figure 8-9. SNx5451B Schematic (Each Driver)



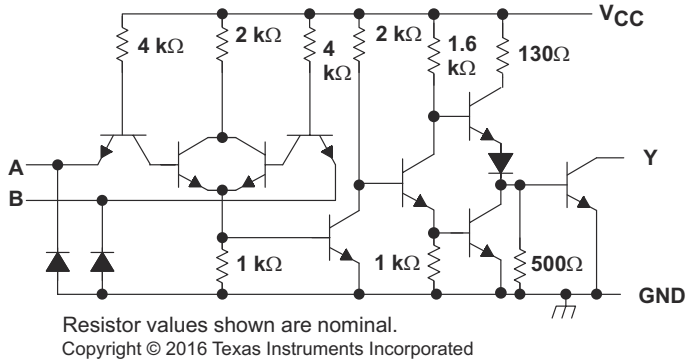
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Figure 8-10. SNx5452B Schematic (Each Driver)



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Figure 8-11. SNx5453B Schematic (Each Driver)



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Figure 8-12. SNx5454B Schematic (Each Driver)

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9 Application and Implementation

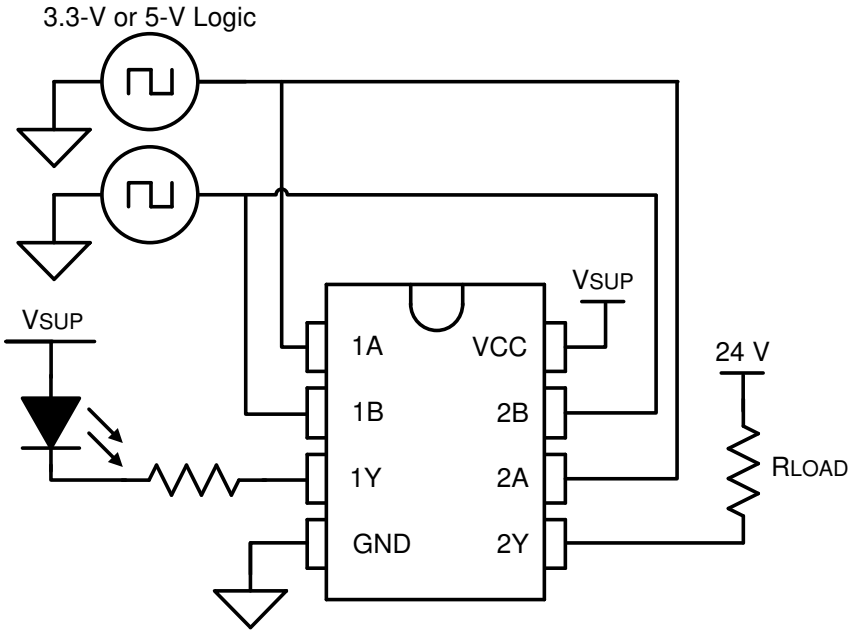
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Typically the SN75451B device drives a high-voltage or high-current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of the SN75451B device, driving an LED using one channel and a high voltage peripheral using the other. In this configuration, the LED will turn on whenever the high voltage peripheral is on.

9.2 Typical Application



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Figure 9-1. SN75451B Driving an LED and a High Voltage Peripheral

9.2.1 Design Requirements

Each of the inputs to the logic gate should never float. If one of the inputs is floating, then the logic gate could be in an unknown state. Be sure to connect ground or V_{CC} to any unused input channels.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - The input voltage must not exceed the V_I specified in *Absolute Maximum Ratings*.
2. Recommended Output Conditions:
   - It is recommended that the load current not exceed 300 mA.
   - The load current must never exceed the I_{OK} noted in *Absolute Maximum Ratings*.

9.2.3 Application Curves

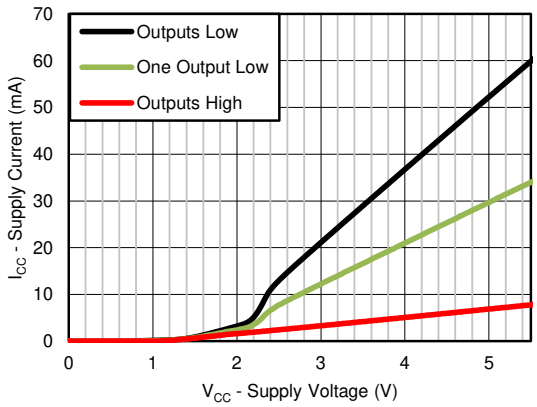


Figure 9-2. SN75451B Typical Supply Current vs Supply Voltage

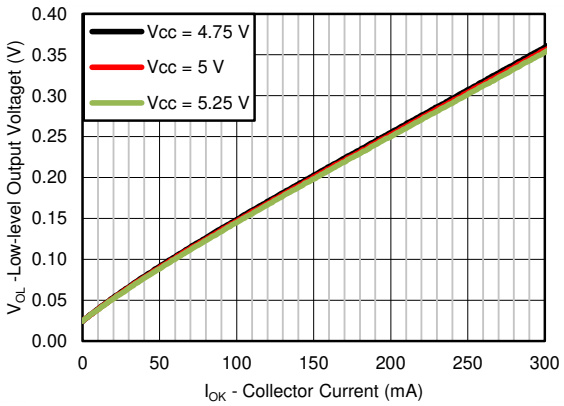


Figure 9-3. SN75451B Typical Low-Level Output Voltage vs Collector Current

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*. The V_{CC} pin should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is suitable for this device.

11 Layout

11.1 Layout Guidelines

Thin traces can be used on the input due to the low-current logic that is used to drive the SNx545xB devices. Take care to separate the input channels to eliminate crosstalk. These traces are recommended for the output to be able to drive high currents. Be sure to connect ground or V_{CC} to any unused input channels, and use a bypass capacitor on the V_{CC} pin to prevent any power glitches.

11.2 Layout Example

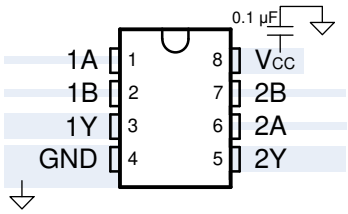


Figure 11-1. SN75451BD Layout

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2017) to Revision E (May 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision C (May 2016) to Revision D (January 2017)	Page
• Replaced image *SN75451B Logic Diagram*	1

Changes from Revision B (January 1999) to Revision C (May 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9563301Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9563301Q2A SNJ55453BFK
5962-9563301QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9563301QPA SNJ55453B
77049012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77049012A SNJ55452BFK
7704901PA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704901PA SNJ55452B
77049022A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77049022A SNJ55451BFK
7704902PA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704902PA SNJ55451B
JM38510/12902BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12902BPA
JM38510/12902BPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12902BPA
JM38510/12903BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12903BPA
JM38510/12903BPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12903BPA
JM38510/12905BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12905BPA
JM38510/12905BPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12905BPA
M38510/12902BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12902BPA
M38510/12903BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12903BPA
M38510/12905BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/12905BPA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN55451BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55451BJG
SN55451BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55451BJG
SN55452BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55452BJG
SN55452BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55452BJG
SN55453BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55453BJG
SN55453BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55453BJG
SN55454BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55454BJG
SN55454BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55454BJG
SN75451BD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B
SN75451BD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B
SN75451BDE4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B
SN75451BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B
SN75451BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B
SN75451BDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B
SN75451BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B
SN75451BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75451BP
SN75451BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75451BP
SN75451BPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75451BP
SN75451BPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	A451B
SN75451BPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A451B
SN75451BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A451B
SN75451BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A451B
SN75452BD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B
SN75452BD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B
SN75452BDE4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B
SN75452BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B
SN75452BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B
SN75452BDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B
SN75452BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B
SN75452BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75452BP
SN75452BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75452BP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75452BPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75452BP
SN75452BPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	A452B
SN75452BPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B
SN75452BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B
SN75452BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B
SN75452BPSRG4	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B
SN75453BD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B
SN75453BD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B
SN75453BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B
SN75453BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B
SN75453BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B
SN75453BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75453BP
SN75453BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75453BP
SN75453BPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75453BP
SN75453BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A453B
SN75453BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A453B
SN75454BD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B
SN75454BD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B
SN75454BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B
SN75454BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B
SN75454BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75454BP
SN75454BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75454BP
SN75454BPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75454BP
SN75454BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A454B
SN75454BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A454B
SNJ55451BFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77049022A SNJ55 451BFK
SNJ55451BFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77049022A SNJ55 451BFK

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ55451BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704902PA SNJ55451B
SNJ55451BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704902PA SNJ55451B
SNJ55452BFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77049012A SNJ55 452BFK
SNJ55452BFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77049012A SNJ55 452BFK
SNJ55452BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704901PA SNJ55452B
SNJ55452BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7704901PA SNJ55452B
SNJ55453BFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9563301Q2A SNJ55 453BFK
SNJ55453BFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9563301Q2A SNJ55 453BFK
SNJ55453BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9563301QPA SNJ55453B
SNJ55453BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9563301QPA SNJ55453B
SNJ55454BJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ55 454BJG
SNJ55454BJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ55 454BJG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55451B, SN55452B, SN55453B, SN55454B, SN75451B, SN75452B, SN75453B, SN75454B :

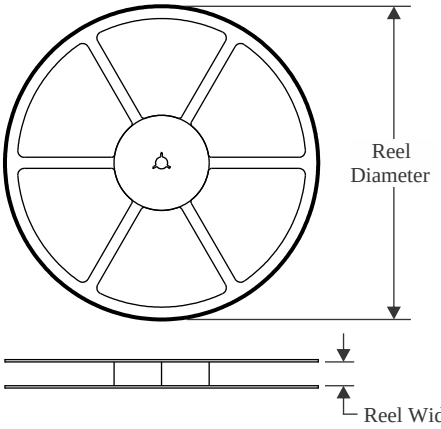
- Catalog : SN75451B, SN75452B, SN75453B, SN75454B
- Military : SN55451B, SN55452B, SN55453B, SN55454B

NOTE: Qualified Version Definitions:

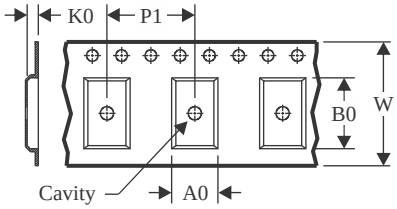
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

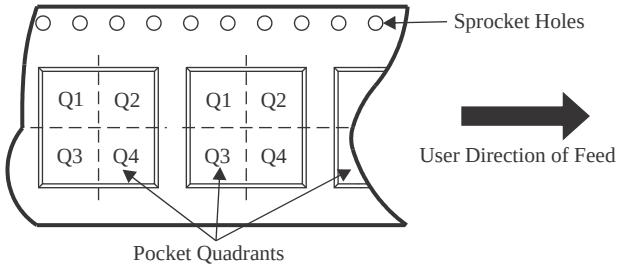


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

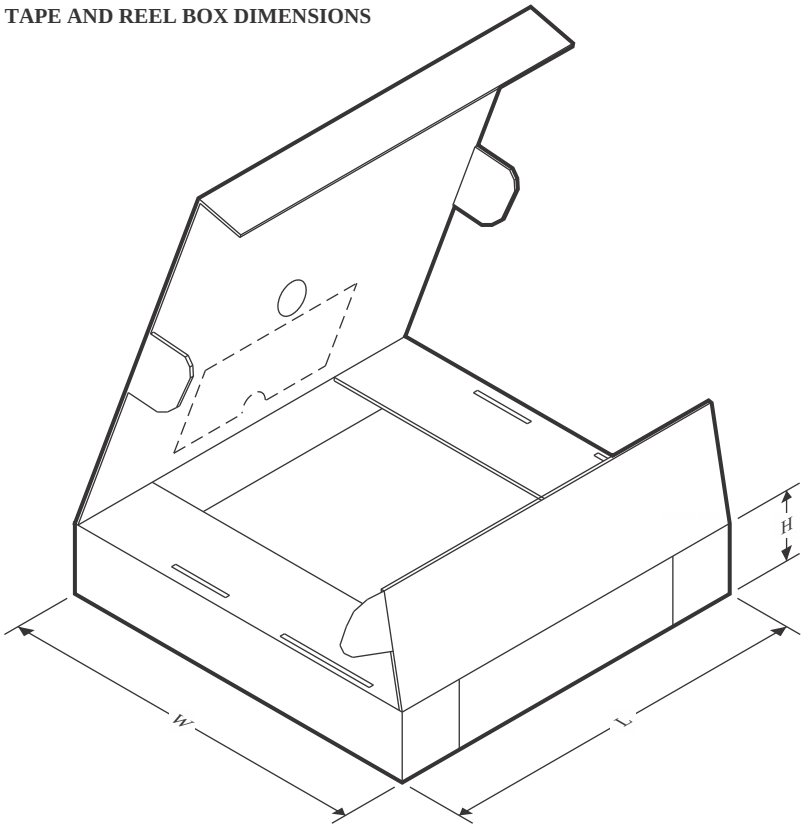
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75451BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75451BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75452BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75452BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75453BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75453BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75454BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75454BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

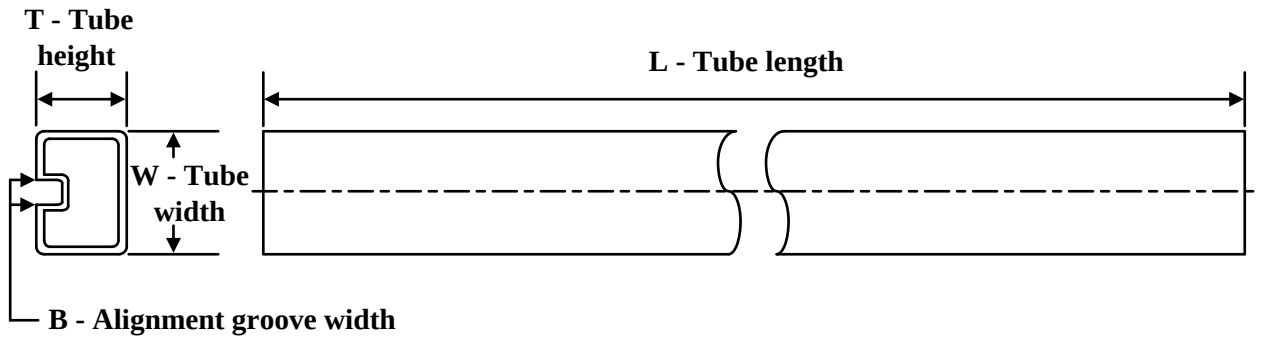
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75451BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN75451BPSR	SO	PS	8	2000	353.0	353.0	32.0
SN75452BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN75452BPSR	SO	PS	8	2000	353.0	353.0	32.0
SN75453BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN75453BPSR	SO	PS	8	2000	353.0	353.0	32.0
SN75454BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN75454BPSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9563301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
77049012A	FK	LCCC	20	55	506.98	12.06	2030	NA
77049022A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN75451BD	D	SOIC	8	75	507	8	3940	4.32
SN75451BD.A	D	SOIC	8	75	507	8	3940	4.32
SN75451BDE4	D	SOIC	8	75	507	8	3940	4.32
SN75451BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75451BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75451BPE4	P	PDIP	8	50	506	13.97	11230	4.32
SN75451BPS	PS	SOP	8	80	530	10.5	4000	4.1
SN75451BPS.A	PS	SOP	8	80	530	10.5	4000	4.1
SN75452BD	D	SOIC	8	75	507	8	3940	4.32
SN75452BD.A	D	SOIC	8	75	507	8	3940	4.32
SN75452BDE4	D	SOIC	8	75	507	8	3940	4.32
SN75452BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75452BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75452BPE4	P	PDIP	8	50	506	13.97	11230	4.32
SN75452BPS	PS	SOP	8	80	530	10.5	4000	4.1
SN75452BPS.A	PS	SOP	8	80	530	10.5	4000	4.1
SN75453BD	D	SOIC	8	75	507	8	3940	4.32
SN75453BD.A	D	SOIC	8	75	507	8	3940	4.32
SN75453BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75453BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75453BPE4	P	PDIP	8	50	506	13.97	11230	4.32
SN75454BD	D	SOIC	8	75	507	8	3940	4.32
SN75454BD.A	D	SOIC	8	75	507	8	3940	4.32
SN75454BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75454BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75454BPE4	P	PDIP	8	50	506	13.97	11230	4.32

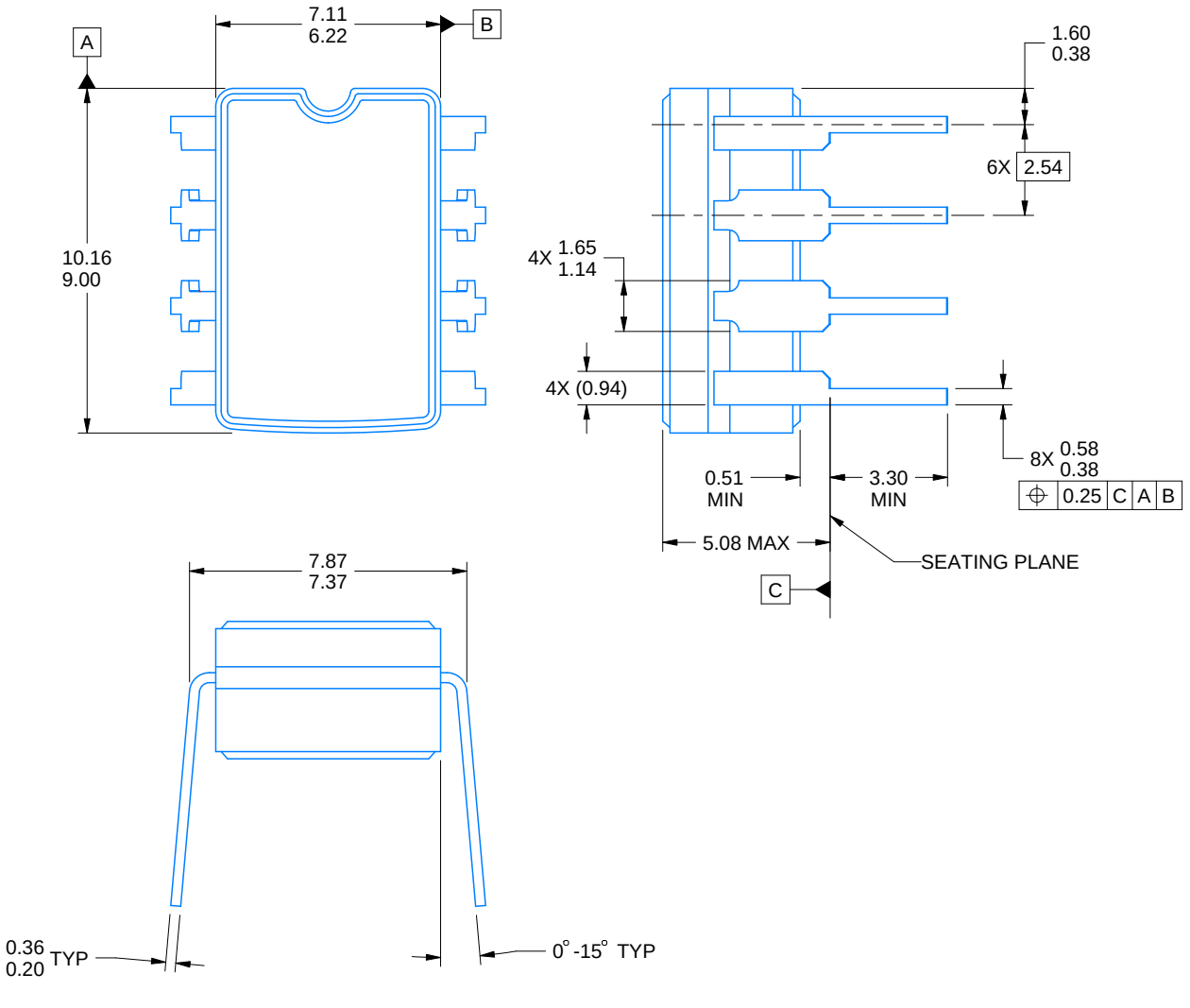
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SNJ55451BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55451BFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55452BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55452BFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55453BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55453BFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

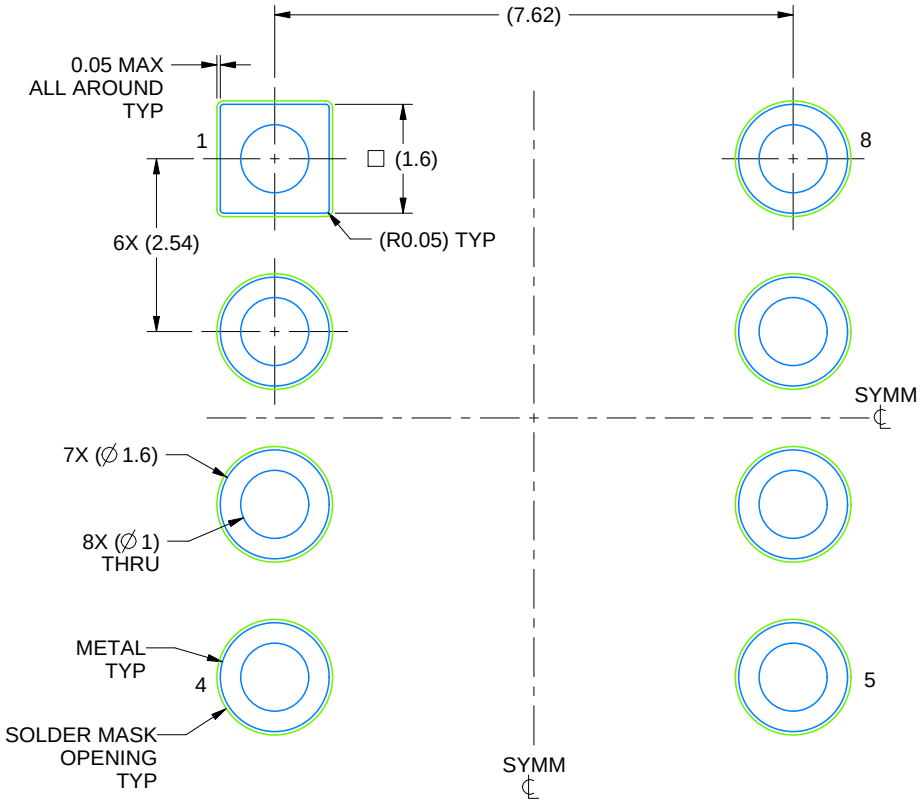
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

GENERIC PACKAGE VIEW

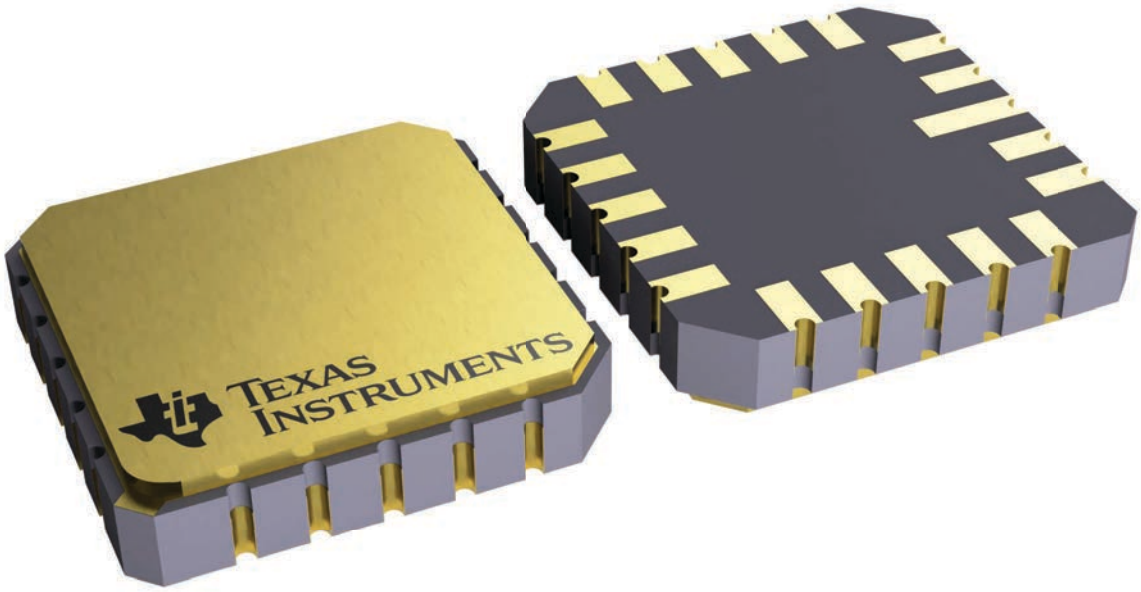
FK 20

LCCC - 2.03 mm max height

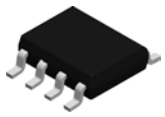
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

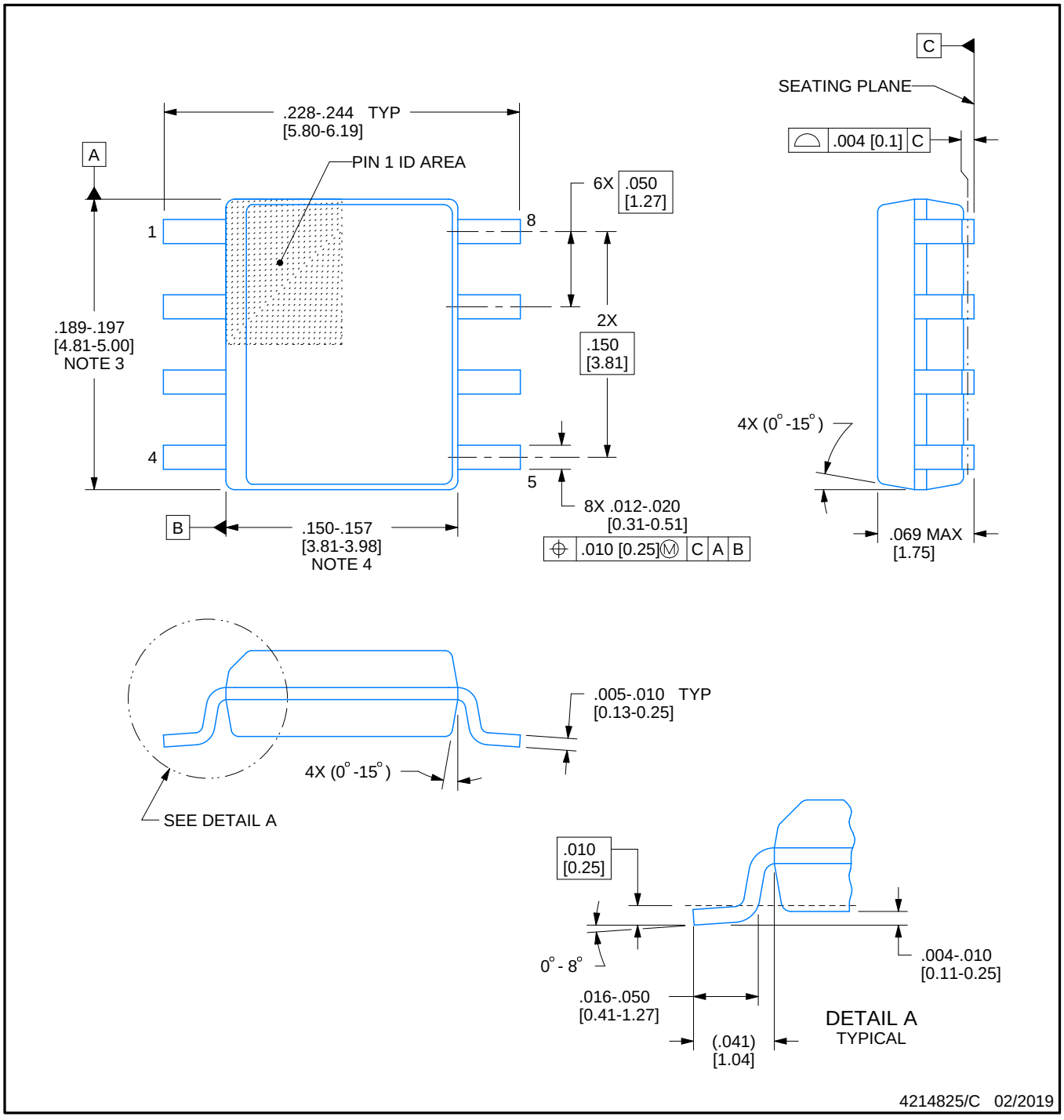


PACKAGE OUTLINE

D0008A

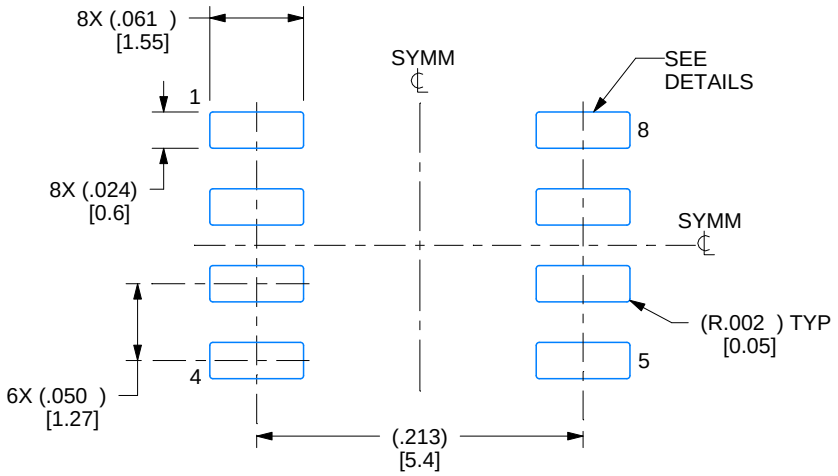
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

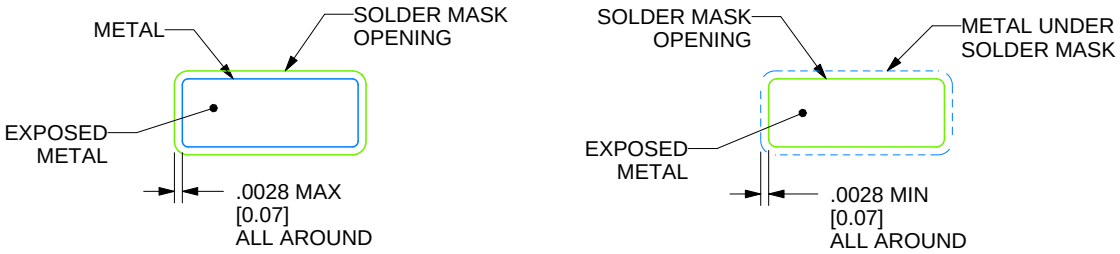


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

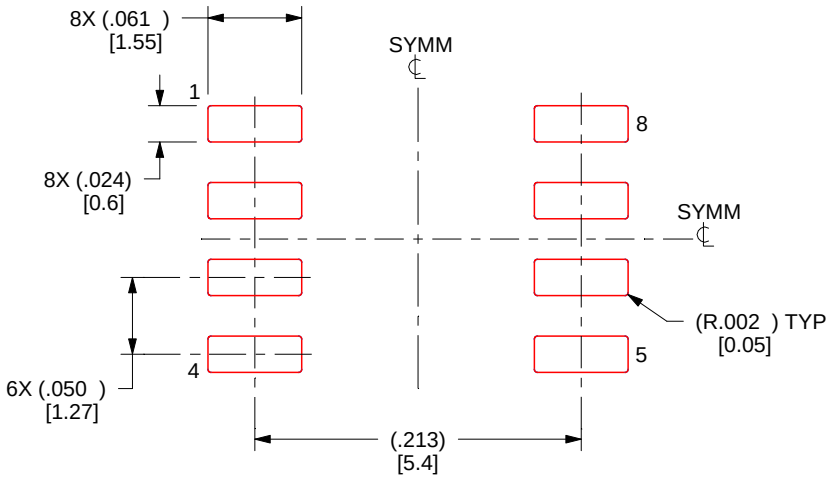
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

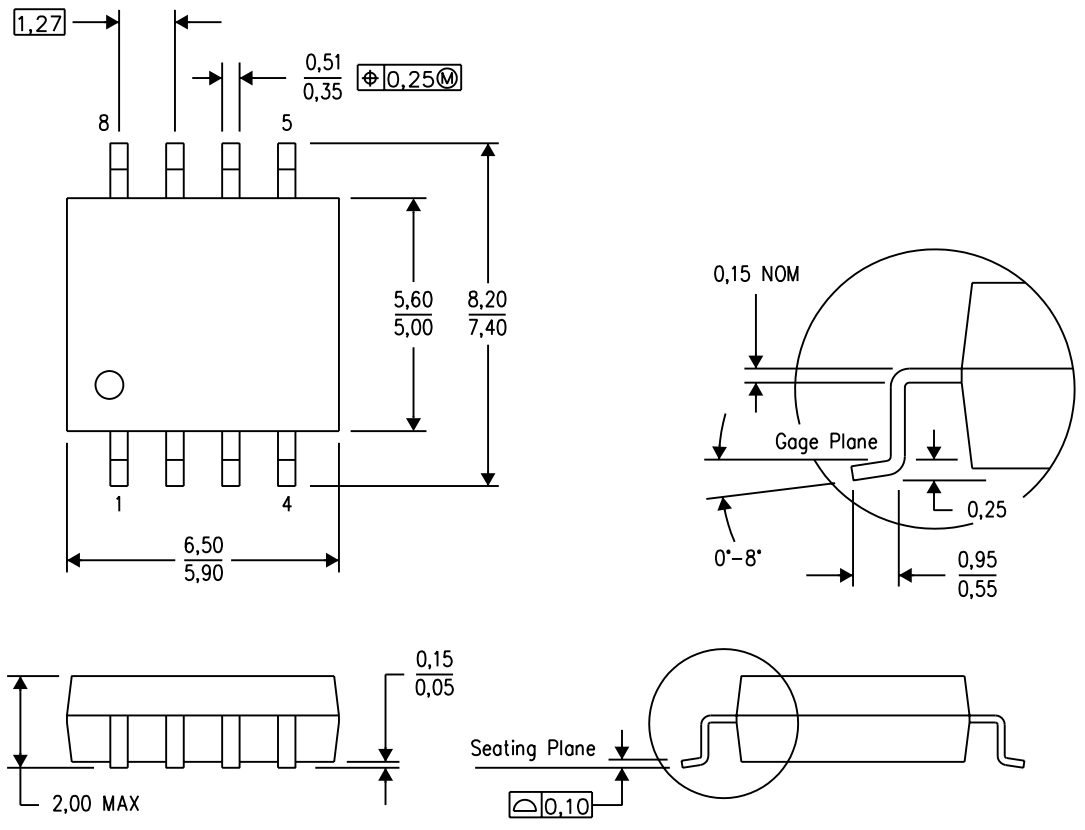
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

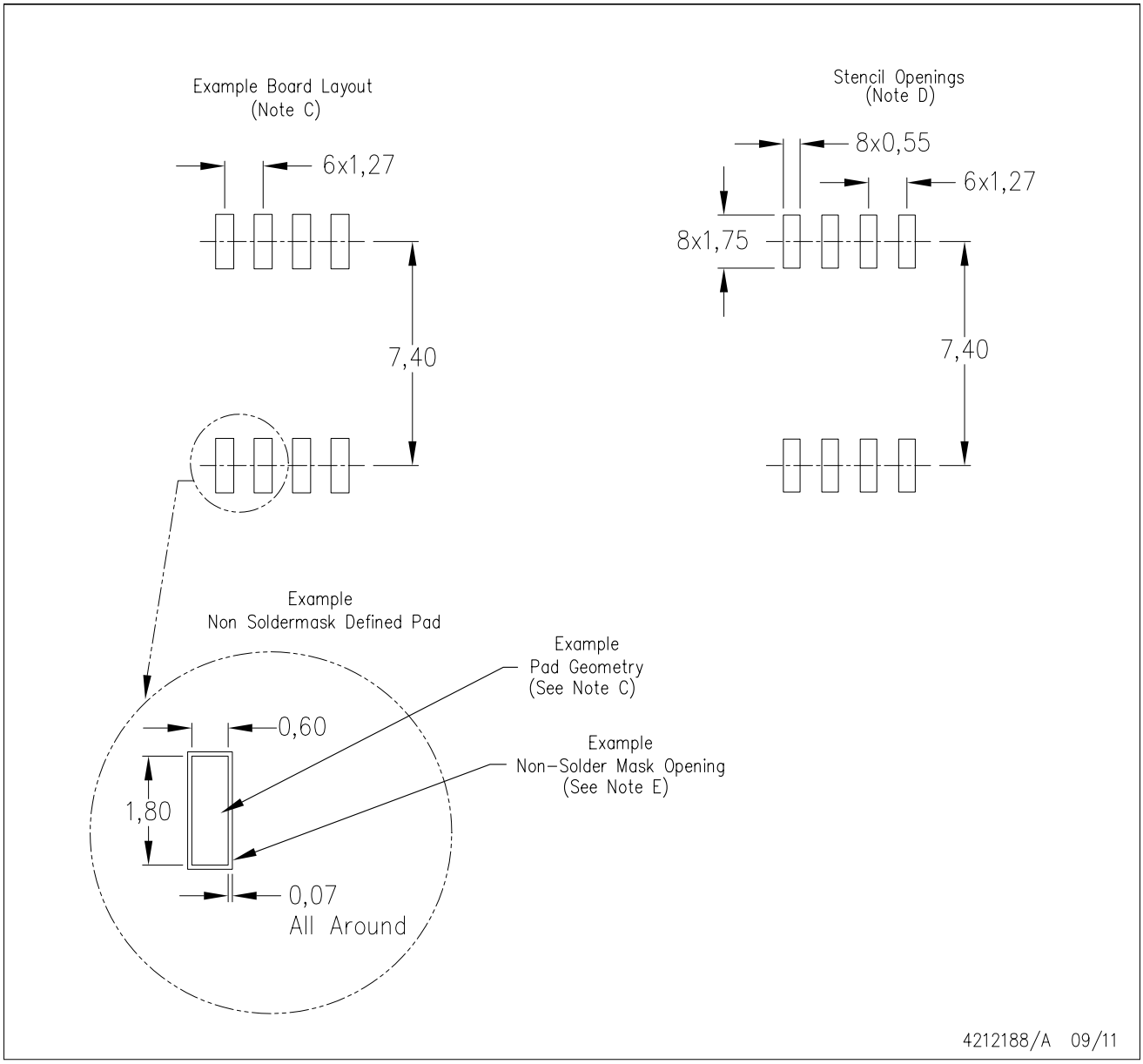
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

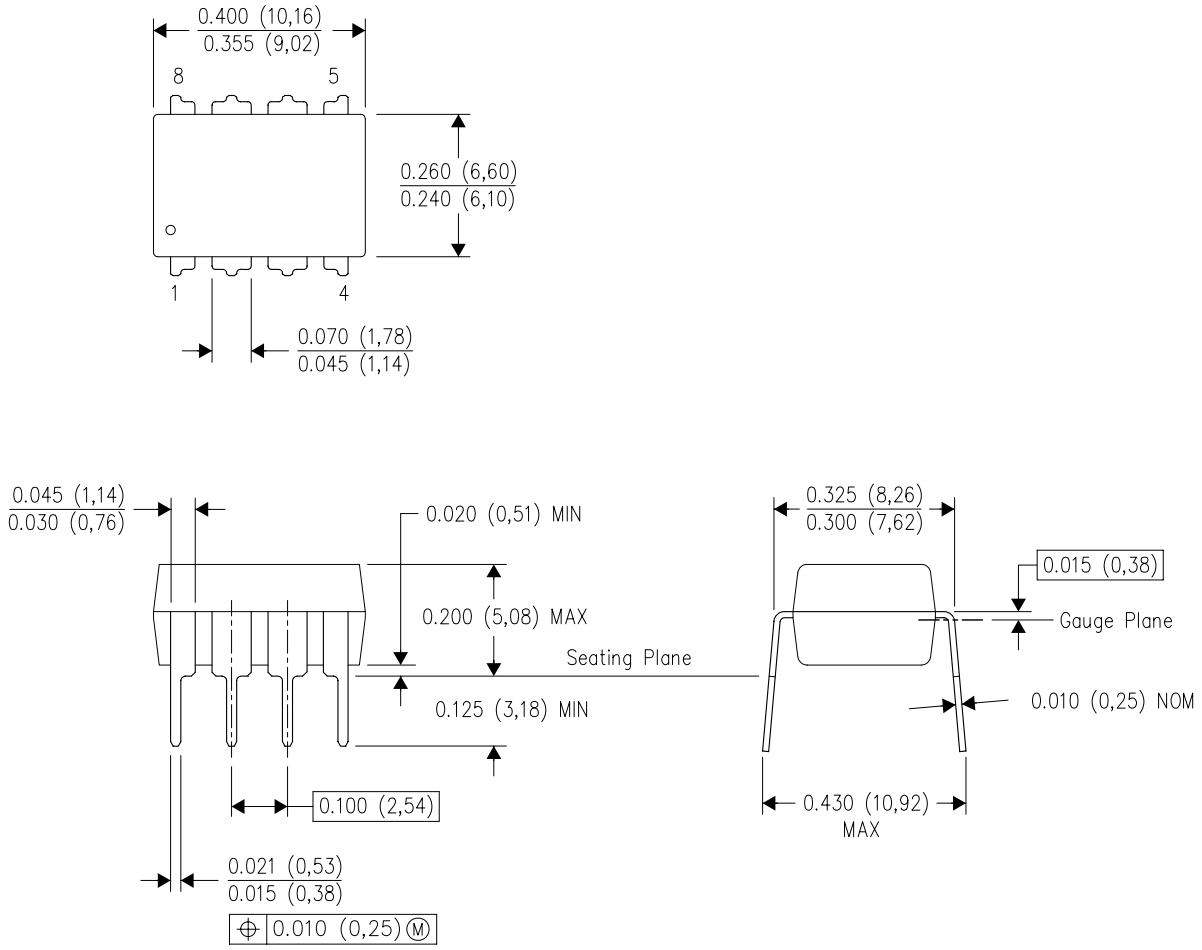
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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