

SN74UVP1G04 Low-Power Single Inverter Gate

1 Features

- Extended low-voltage operation with 0.63V to 3.6V supply range
- Extended operating temperature range: -40°C to 125°C
- Low power consumption
 - Typical $I_{\text{CC}} = 10\text{nA}$
 - Typical input leakage $I_{\text{I}} = 3\text{nA}$
 - Typical output off-state leakage current $I_{\text{OZ}} = 100\text{nA}$
 - Typical partial-power-down $I_{\text{OFF}} = 0.2\mu\text{A}$
- 3.6V tolerant input to support down translation
- Maximum t_{pd} of 9.5ns at 3.3V
- Drop-in compatible with AUP1G family and V_{CC} extended from 0.8V to 0.63V

2 Applications

- PC and notebooks
- Data center
- Building automation
- Mobile phones
- Wearables
- Wired networking

3 Description

The SN74UVP1G04 device is a low-power single inverter that performs the Boolean function $Y = \bar{A}$.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74UVP1G04	DBV (SOT-23, 5)	2.90mm × 1.60mm
	DCK (SC-70, 5)	2.00mm × 1.25mm
	DRY (USON, 6)	1.45mm × 1.00mm
	DSF (X2SON, 6)	1.00mm × 1.00mm
	DPW (X2SON, 5)	0.80mm × 0.80mm

(1) For more information, see [Section 11](#).

(2) The body size (length × width) is a nominal value and does not include pins.



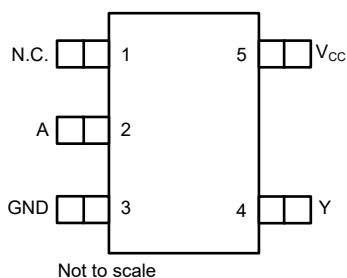
Simplified Schematic



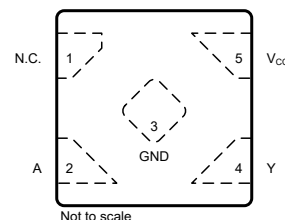
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4 Pin Configuration and Functions



**Figure 4-1. DBV or DCK Package,
5-Pin SOT-23 or SC-70
(Top View)**

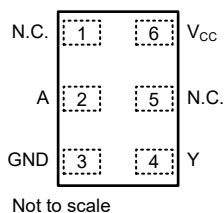


**Figure 4-2. DPW Package,
5-Pin X2SON
(Top View)**

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	DPW, DBV, DCK		
N.C.	1	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y (push pull)
VCC	5	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power



**Figure 4-3. DRY or DSF Package,
5-Pin USON or X2SON
(Top View)**

Table 4-2. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	DSF, DRY		
N.C.	1, 5	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y (push pull)
VCC	6	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6	V
V _I	Input voltage range ⁽²⁾		-0.5	6	V
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0V		-50	mA
I _{OK}	Output clamp current	V _O < 0V		-50	mA
I _O	Continuous output current			±50	mA
I _O	Continuous output current through V _{CC} or GND			±100	mA
T _J	Junction temperature		-65	150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		0.63	3.6	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 0.63V to 0.77V	0.65 × V _{CC}		V
		V _{CC} = 0.72V to 0.88V	0.65 × V _{CC}		
		V _{CC} = 0.9V to 1.1V	0.65 × V _{CC}		
		V _{CC} = 1.08V to 1.32V	0.65 × V _{CC}		
		V _{CC} = 1.35V to 1.65V	0.65 × V _{CC}		
		V _{CC} = 1.62V to 1.98V	0.65 × V _{CC}		
		V _{CC} = 2.3V to 2.7V	1.7		
		V _{CC} = 3.0V to 3.6V	2		

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V _{IL}	Low-Level input voltage	V _{CC} = 0.63V to 0.77V		0.35 × V _{CC}	V
		V _{CC} = 0.72V to 0.88V		0.35 × V _{CC}	
		V _{CC} = 0.9V to 1.1V		0.35 × V _{CC}	
		V _{CC} = 1.08V to 1.32V		0.35 × V _{CC}	
		V _{CC} = 1.35V to 1.65V		0.35 × V _{CC}	
		V _{CC} = 1.62V to 1.98V		0.35 × V _{CC}	
		V _{CC} = 2.3V to 2.7V		0.7	
		V _{CC} = 3.0V to 3.6V		0.8	
I _{OH}	High-level output current	V _{CC} = 0.63V		-0.2	mA
		V _{CC} = 0.72V		-0.5	
		V _{CC} = 0.9V		-0.7	
		V _{CC} = 1.08V		-1.1	
		V _{CC} = 1.35V		-1.7	
		V _{CC} = 1.62V		-1.9	
		V _{CC} = 2.3V		-3.1	
		V _{CC} = 3.0V		-4	
I _{OL}	Low-level output current	V _{CC} = 0.63V		0.2	mA
		V _{CC} = 0.72V		0.5	
		V _{CC} = 0.9V		0.7	
		V _{CC} = 1.08V		1.1	
		V _{CC} = 1.35V		1.7	
		V _{CC} = 1.62V		1.9	
		V _{CC} = 2.3V		3.1	
		V _{CC} = 3.0V		4	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.65V to 3.6V		200	ns/V
T _A	Operating free-air temperature		-40	125	°C

ADVANCE INFORMATION

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
DBV (SOT-23, 5)	5	298.6	240.2	134.6	114.5	133.9	n/a	°C/W
DCK (SC-70, 5)	5	314.4	128.7	100.6	7.1	99.8	n/a	°C/W
DRY (USON, 6)	6	554.9	385.4	388.2	159.0	384.1	n/a	°C/W
DSF (X2SON, 6)	6	407.1	232.0	306.9	40.3	306.0	n/a	°C/W
DPW (X2SON, 5)	5	291.8	224.2	245.8	31.4	245.6	195.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = –20μA	0.63V to 3.6V	V _{CC} – 0.1			V
	I _{OH} = –0.7mA	1.0V	0.65			
	I _{OH} = –1.1mA	1.2V	0.97			
	I _{OH} = –1.7mA	1.5V	1.24			
	I _{OH} = –1.9mA	1.65V	1.4			
	I _{OH} = –3.1mA	2.3V	1.99			
	I _{OH} = –3.5mA	2.7V	2.35			
	I _{OH} = –4mA	3V	2.67			
V _{OL}	I _{OL} = 20μA	0.63V to 3.6V			0.15	V
	I _{OL} = 0.7mA	1.0V			0.35	
	I _{OL} = 1.1mA	1.2V			0.25	
	I _{OL} = 1.7mA	1.5V			0.23	
	I _{OL} = 1.9mA	1.65V			0.23	
	I _{OL} = 3.1mA	2.3V			0.26	
	I _{OL} = 3.5mA	2.7V			0.27	
	I _{OL} = 4mA	3V			0.29	
I _I	V _I = V _{CC} or GND	V _{CC} = 0V to 3.6V	±0.003		±0.5	μA
I _{OFF}	V _I or V _O = V _{CC}	V _{CC} = 0V	±0.2		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	V _{CC} = 0.63V to 3.6V	0.01		1.4	μA
ΔI _{CC}	One input at V _{CC} – 0.6V, other inputs at V _{CC} or GND	3.3V			60	μA
C _I	V _I = V _{CC} or GND	3.3V		4.4		pF
C _O	V _O = V _{CC} or GND	3.3V		2.59		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CONDITION	V _{CC}	MIN	TYP	MAX	UNIT
t _{pd}	A	Y	C _L = 5pF	0.7V ± 0.07V			130	ns
				0.8V ± 0.08V			81.5	ns
			C _L = 10pF	1.0V ± 0.1V			27.8	ns
				1.2V ± 0.12V			10.1	ns
			C _L = 15pF	1.5V ± 0.15V			7.3	ns
				1.8V ± 0.18V			5.3	ns
			C _L = 30pF	2.5V ± 0.2V			5.1	ns
				3.3V ± 0.3V			4	ns

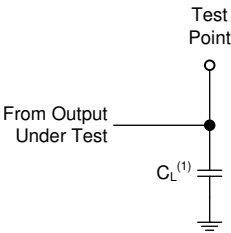
over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CONDITION	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}			$f = 10\text{MHz}$	0.7V		5.26		pF
				0.8V		5.61		pF
				1.0V		5.61		pF
				1.2V		5		pF
				1.5V		4.9		pF
				1.8V		4.9		pF
				2.5V		4.7		pF
				3.3V		4.4		pF

6 Parameter Measurement Information

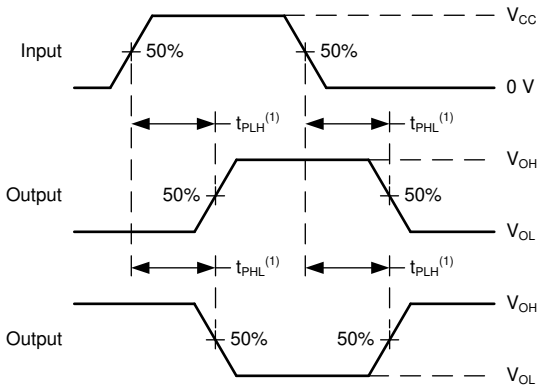
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_t < 3\text{ ns}$.

The outputs are measured individually with one input transition per measurement.



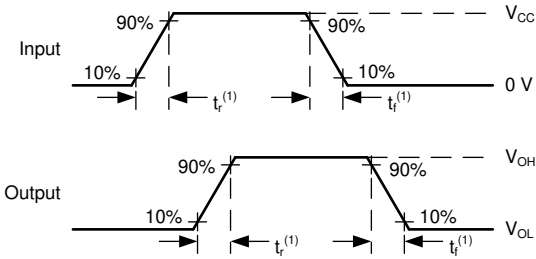
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PLH} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as the transition time.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Feature Description

7.1.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.1.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10k Ω resistor, however, is recommended and typically meets all requirements.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UVP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

8.2 Typical Application

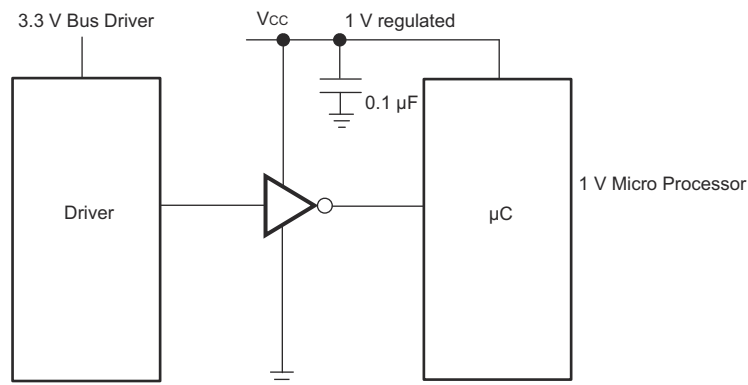


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention. Bus contention can drive currents that exceed maximum limits.

8.2.2 Detailed Design Procedure

- Recommended input conditions
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in [Section 5.3](#)
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in [Section 5.3](#)
 - Inputs are overvoltage tolerant allowing them to go as high as 3.6V at any valid V_{CC}
- Recommend output conditions
 - Load currents must not exceed 20mA on the output and 50mA total for the part
 - Do not pull outputs above V_{CC}

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each V_{CC} terminal has a good bypass capacitor to prevent power disturbance. For the SN74UVP1G04, a 0.1μF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1μF and 1μF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

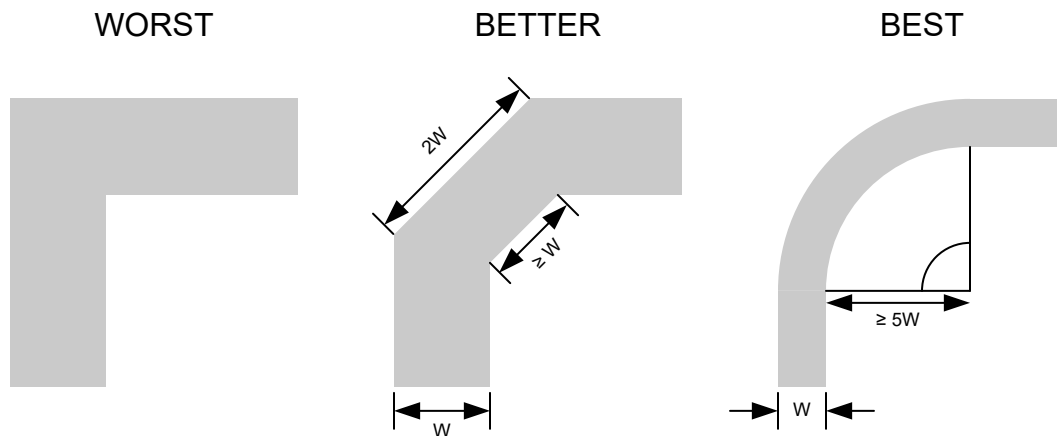


Figure 8-2. Example Trace Corners for Improved Signal Integrity

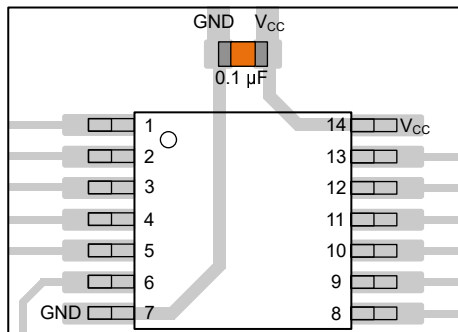


Figure 8-3. Example Bypass Capacitor Placement for TSSOP and Similar Packages

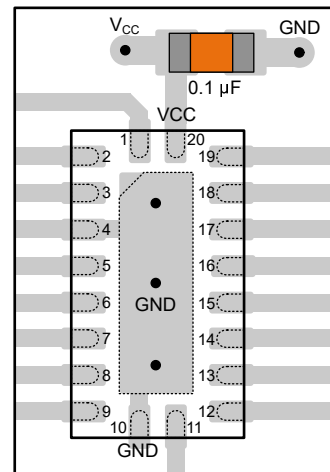


Figure 8-4. Example Bypass Capacitor Placement for WQFN and Similar Packages

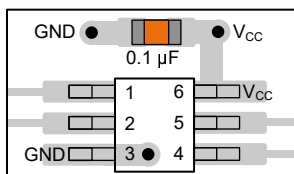


Figure 8-5. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

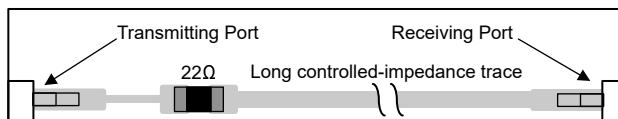


Figure 8-6. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

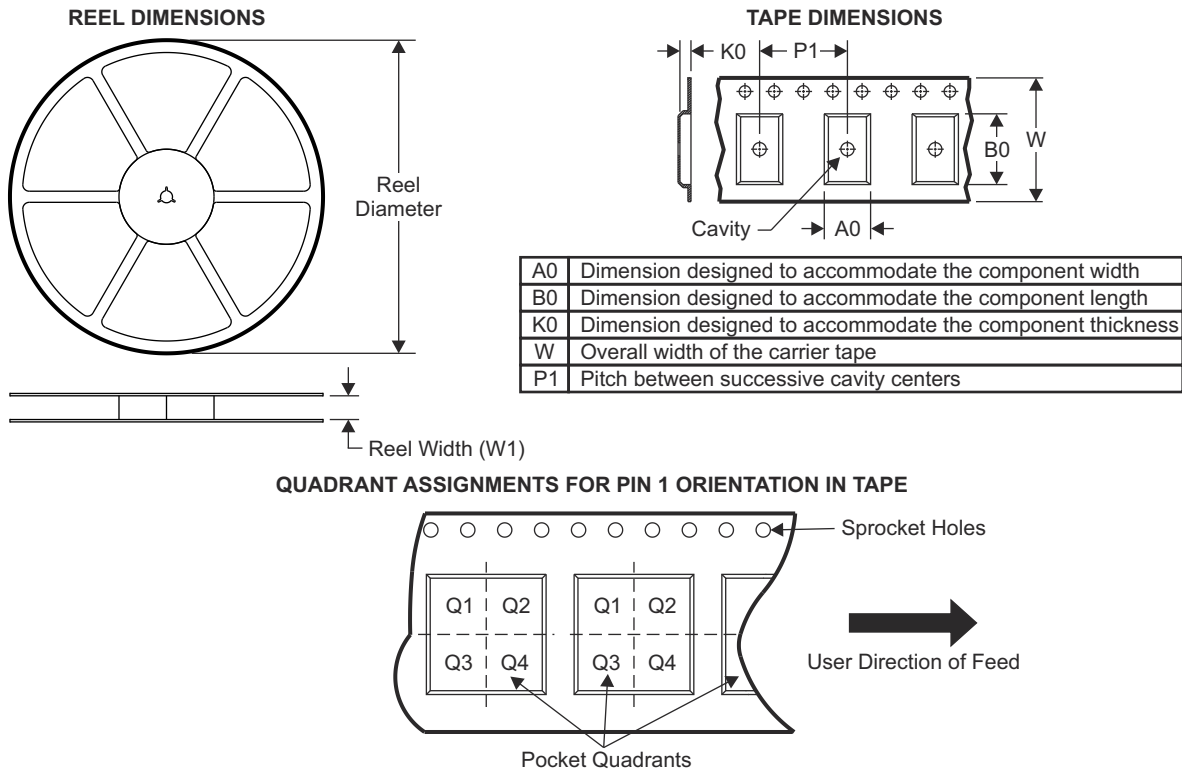
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

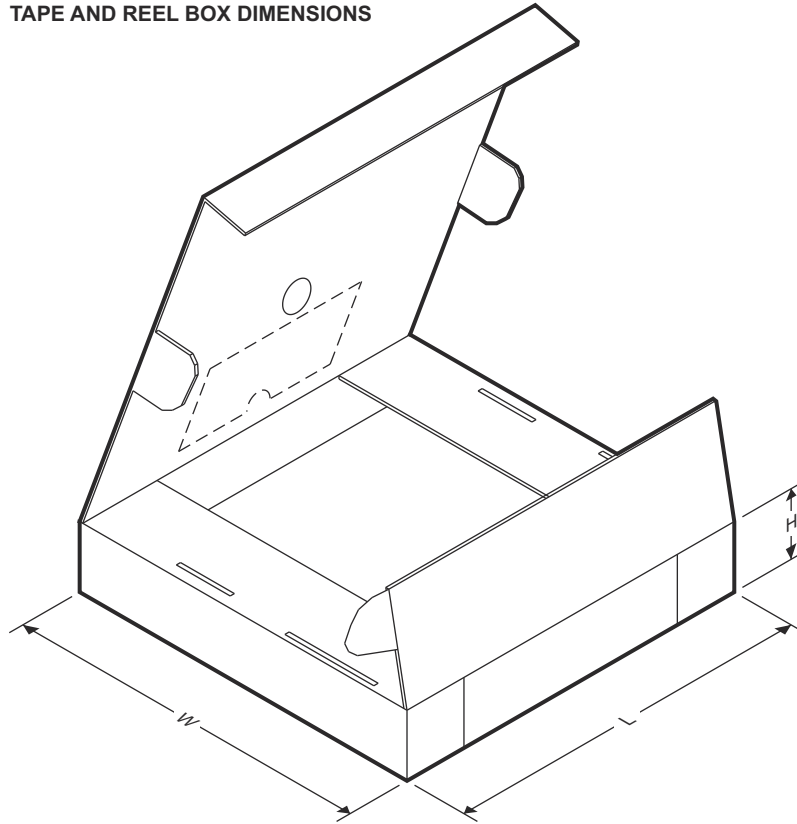
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PSN74UVP1G04DBV R	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PSN74UVP1G04DC KR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
PSN74UVP1G04DP WR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
PSN74UVP1G04DR YR	USON	DRY	5	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
PSN74UVP1G04DSF R	USON	DSF	5	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

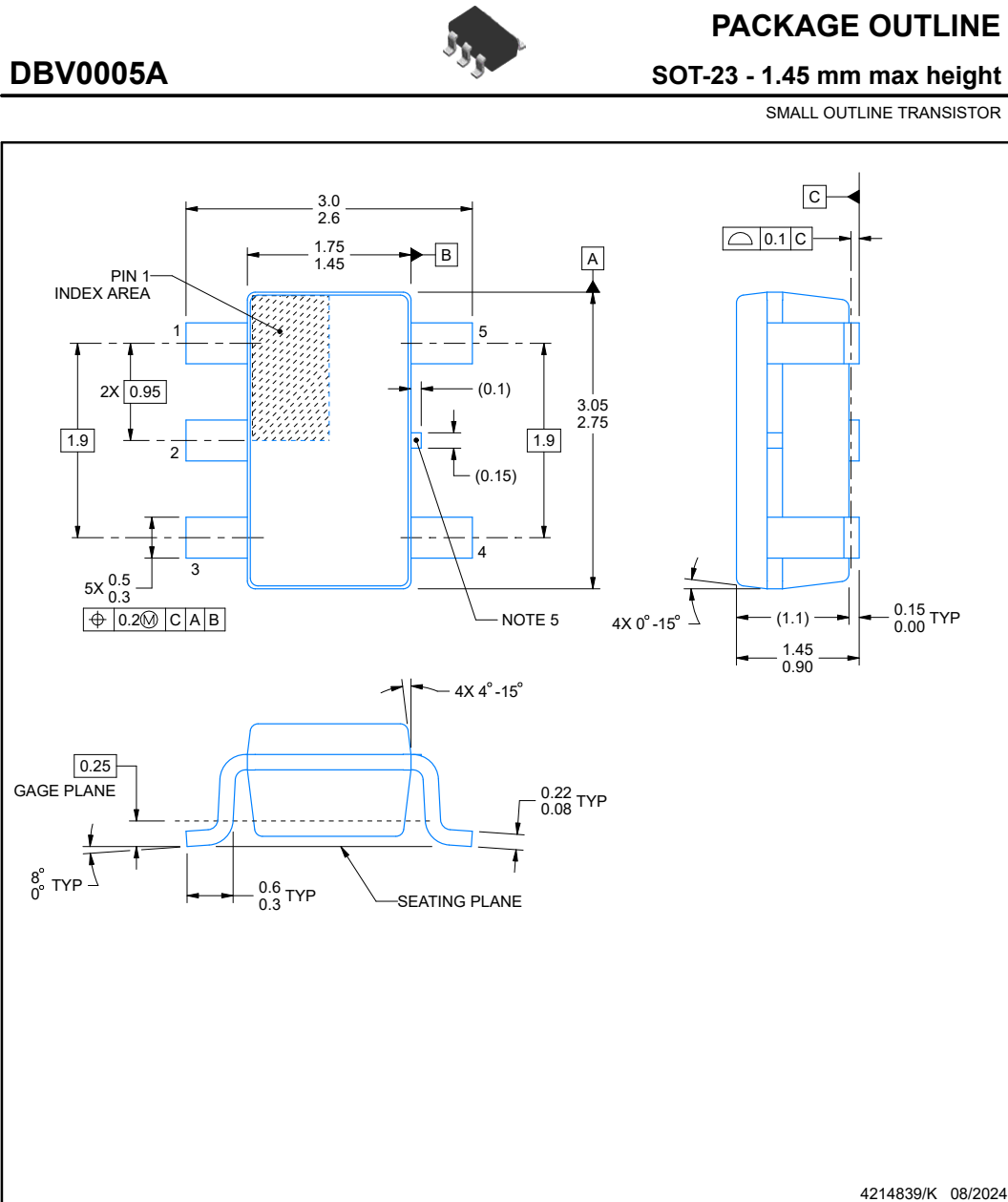


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PSN74UVP1G04DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
PSN74UVP1G04DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
PSN74UVP1G04DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
PSN74UVP1G04DRYR	USON	DRY	5	5000	184.0	184.0	19.0
PSN74UVP1G04DSFR	USON	DSF	5	5000	210.0	185.0	35.0

ADVANCE INFORMATION

11.2 Mechanical Data

ADVANCE INFORMATION



NOTES:

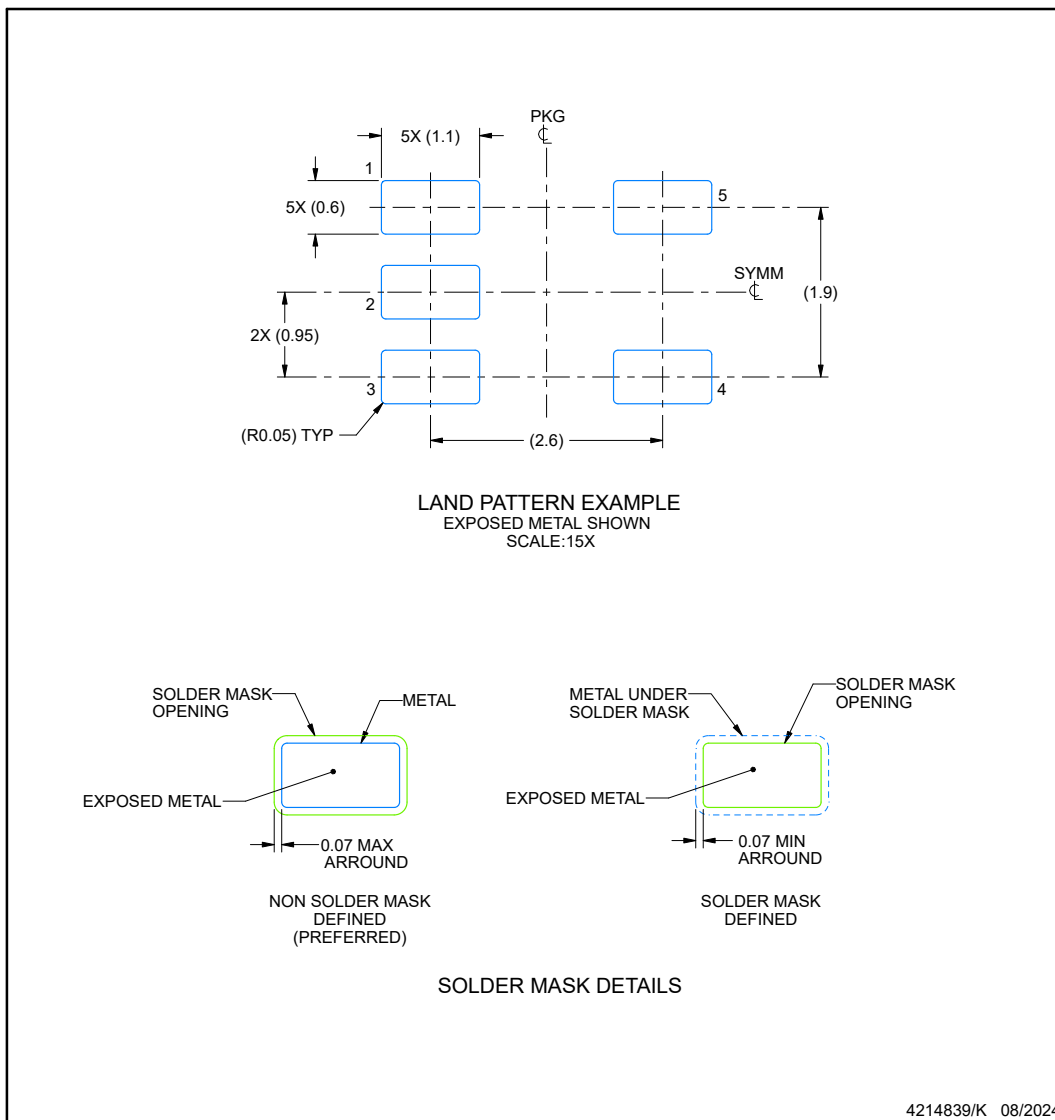
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

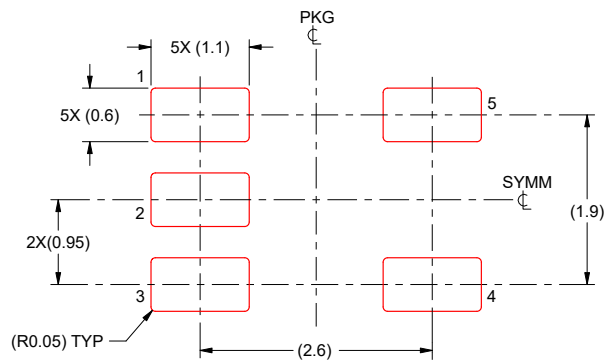
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

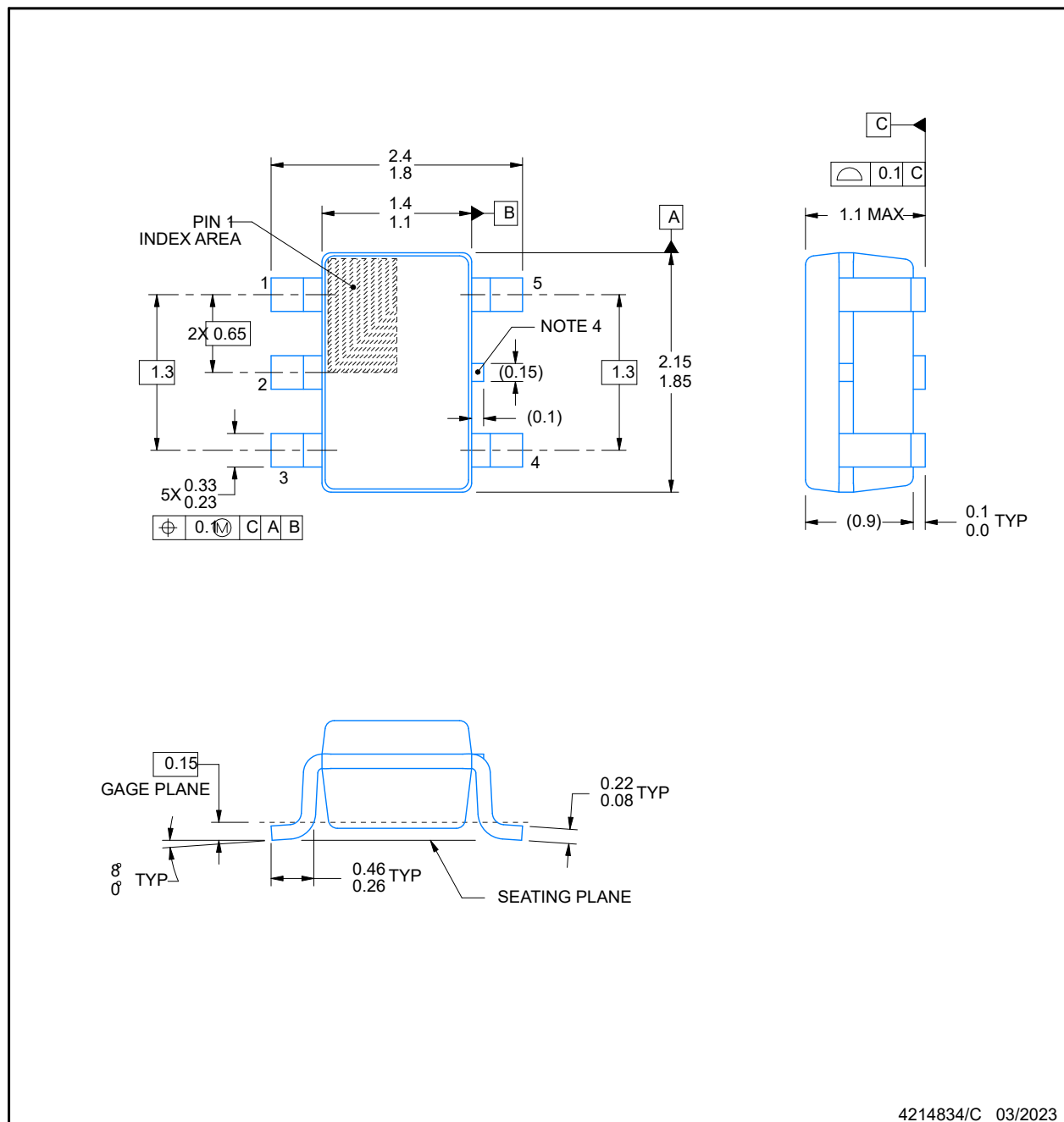


DCK0005A

PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

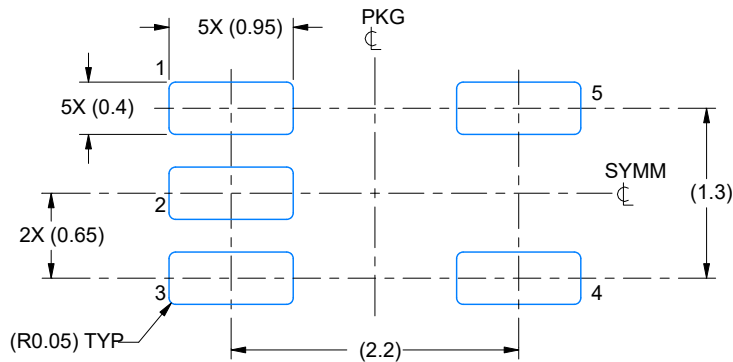
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

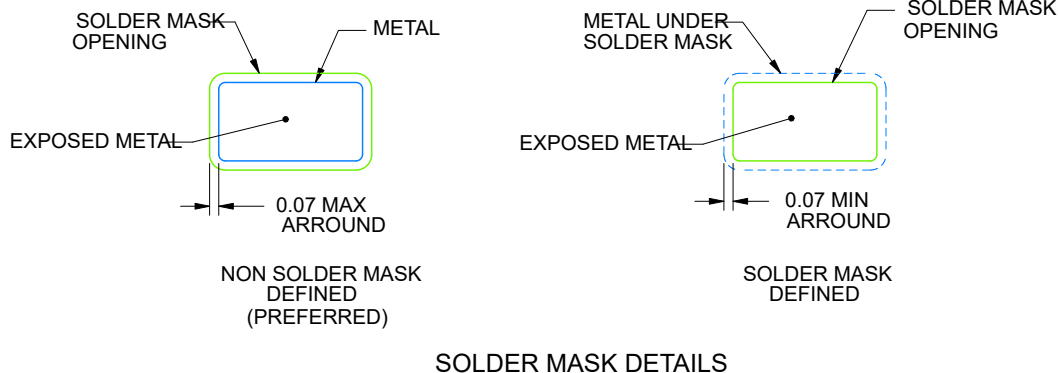
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



4214834/C 03/2023

NOTES: (continued)

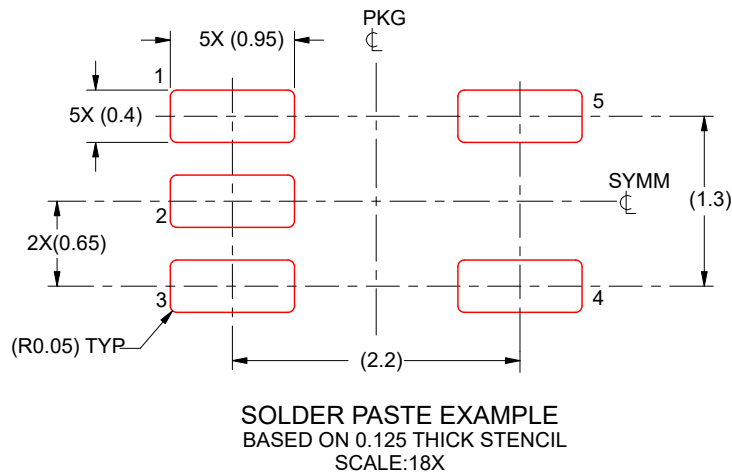
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/C 03/2023

ADVANCE INFORMATION

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

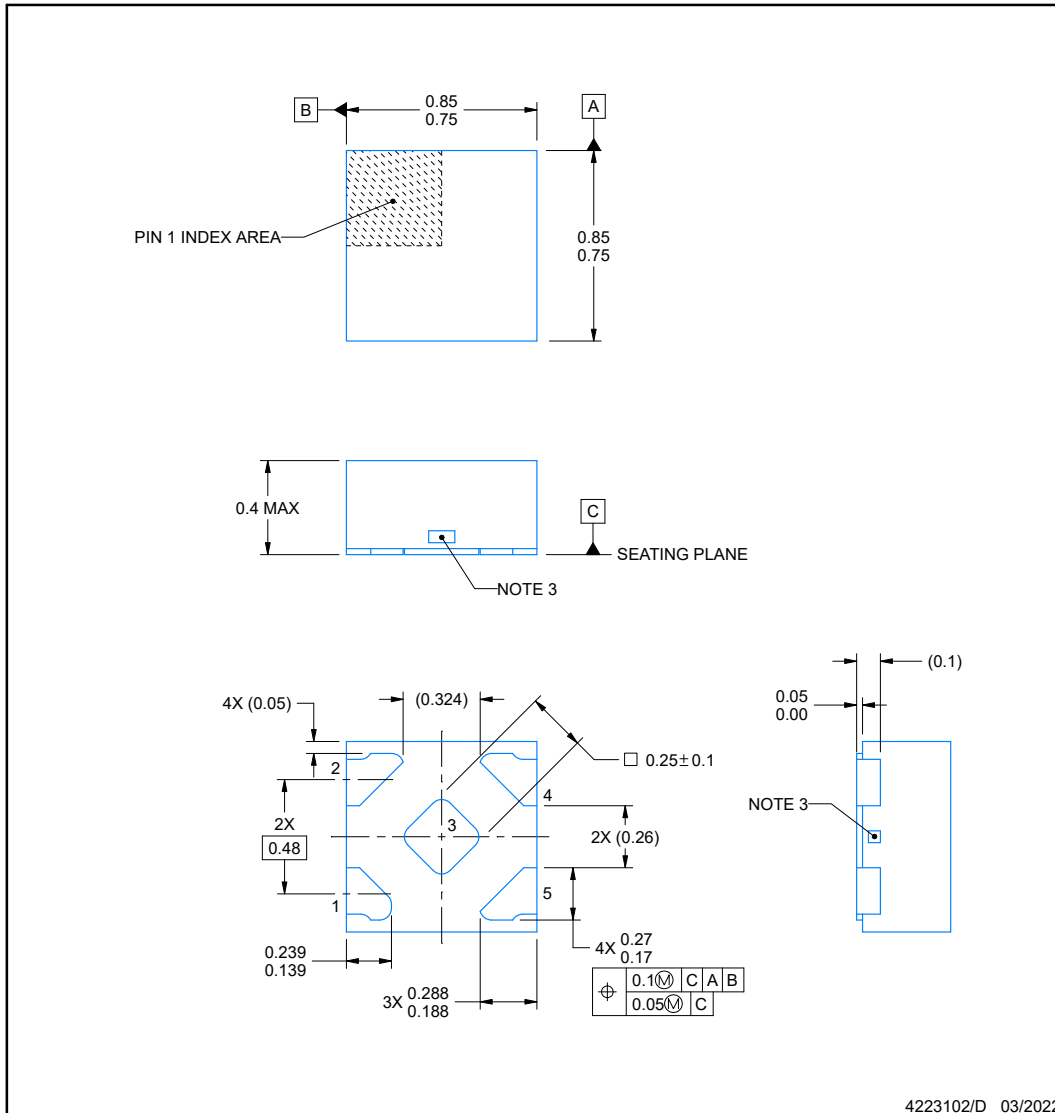


DPW0005A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

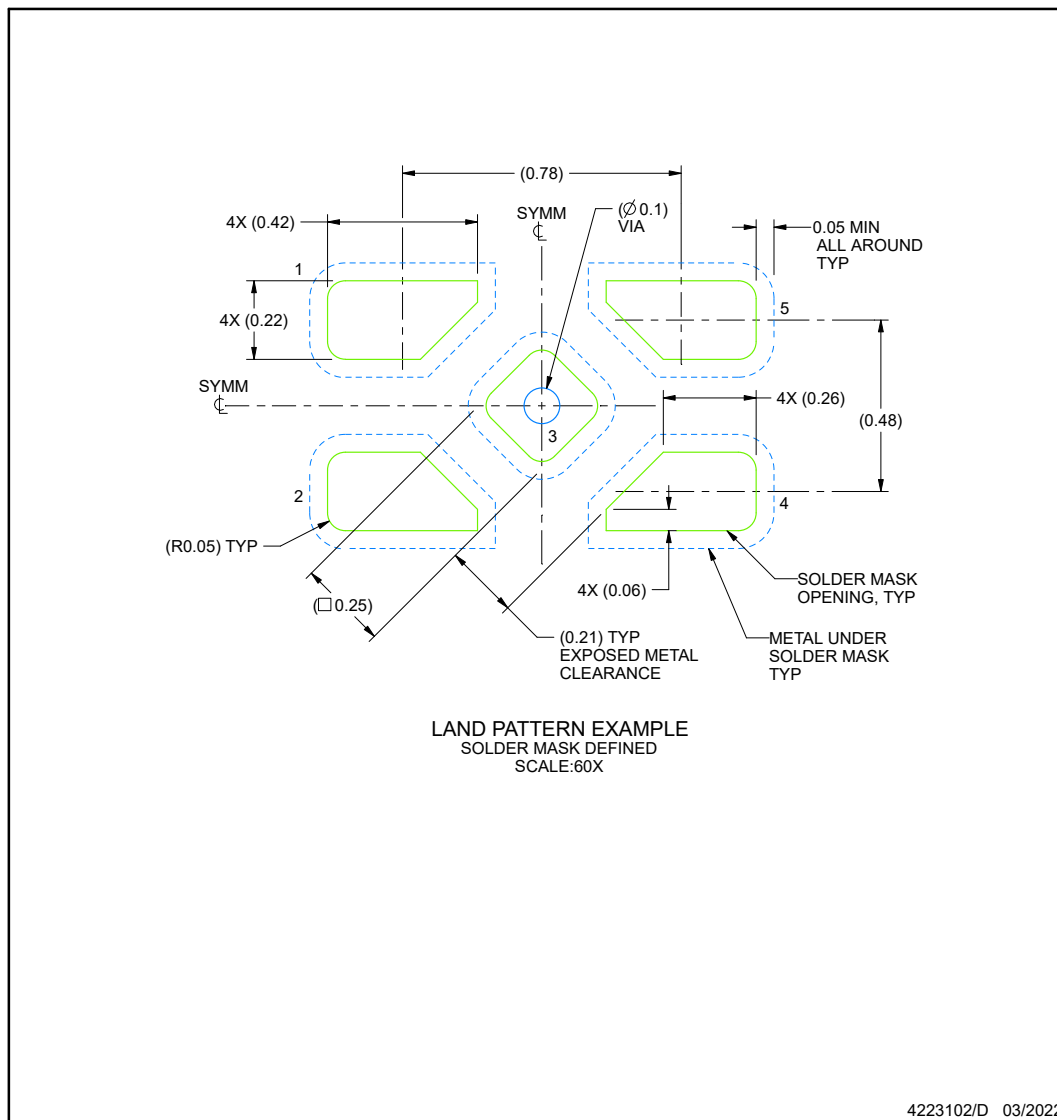
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

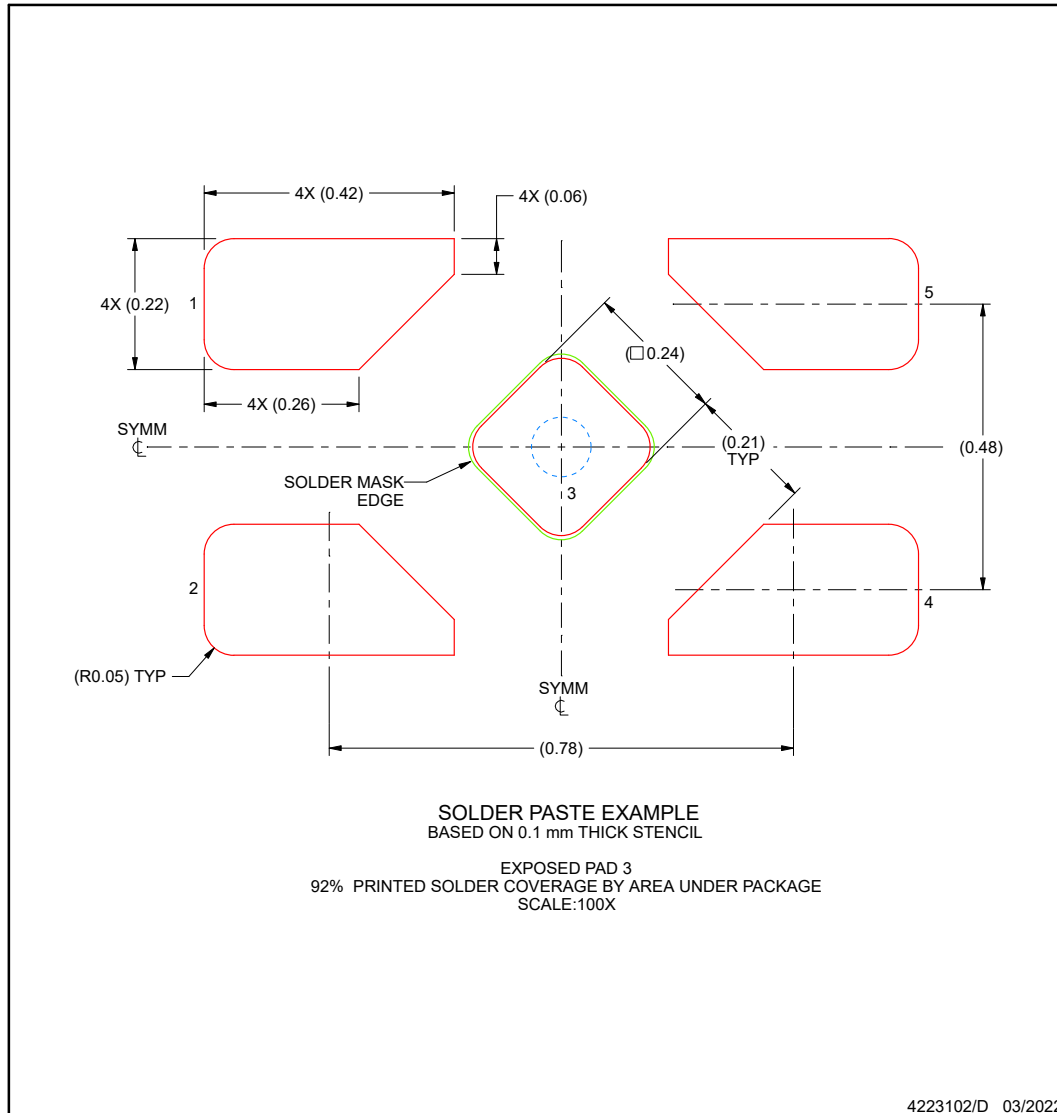
- This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DPW0005A

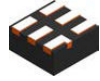
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

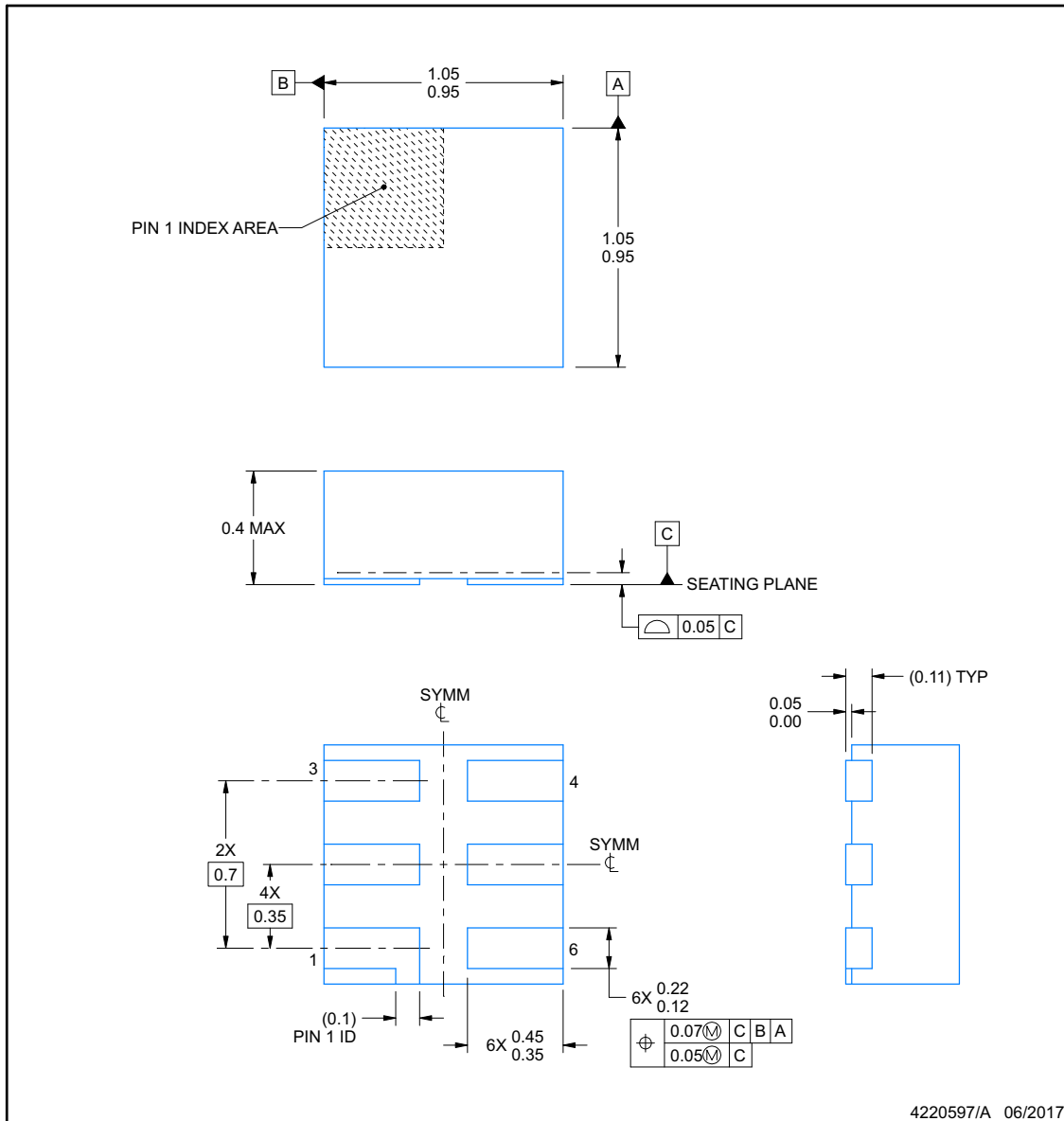
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



DSF0006A

PACKAGE OUTLINE
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

www.ti.com

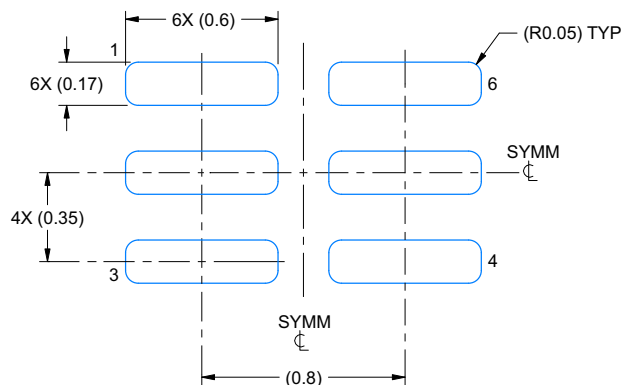
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

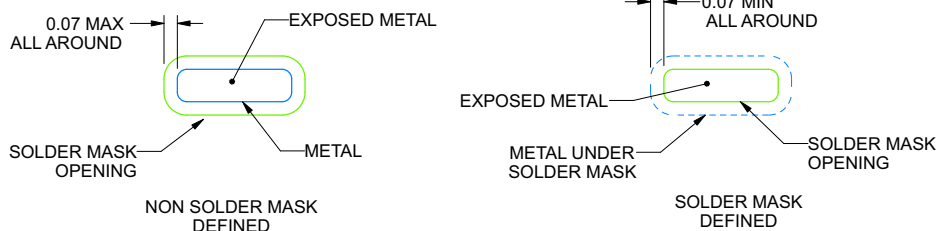
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

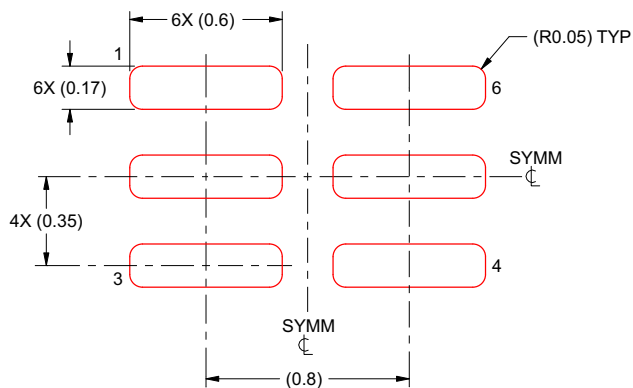
www.ti.com

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

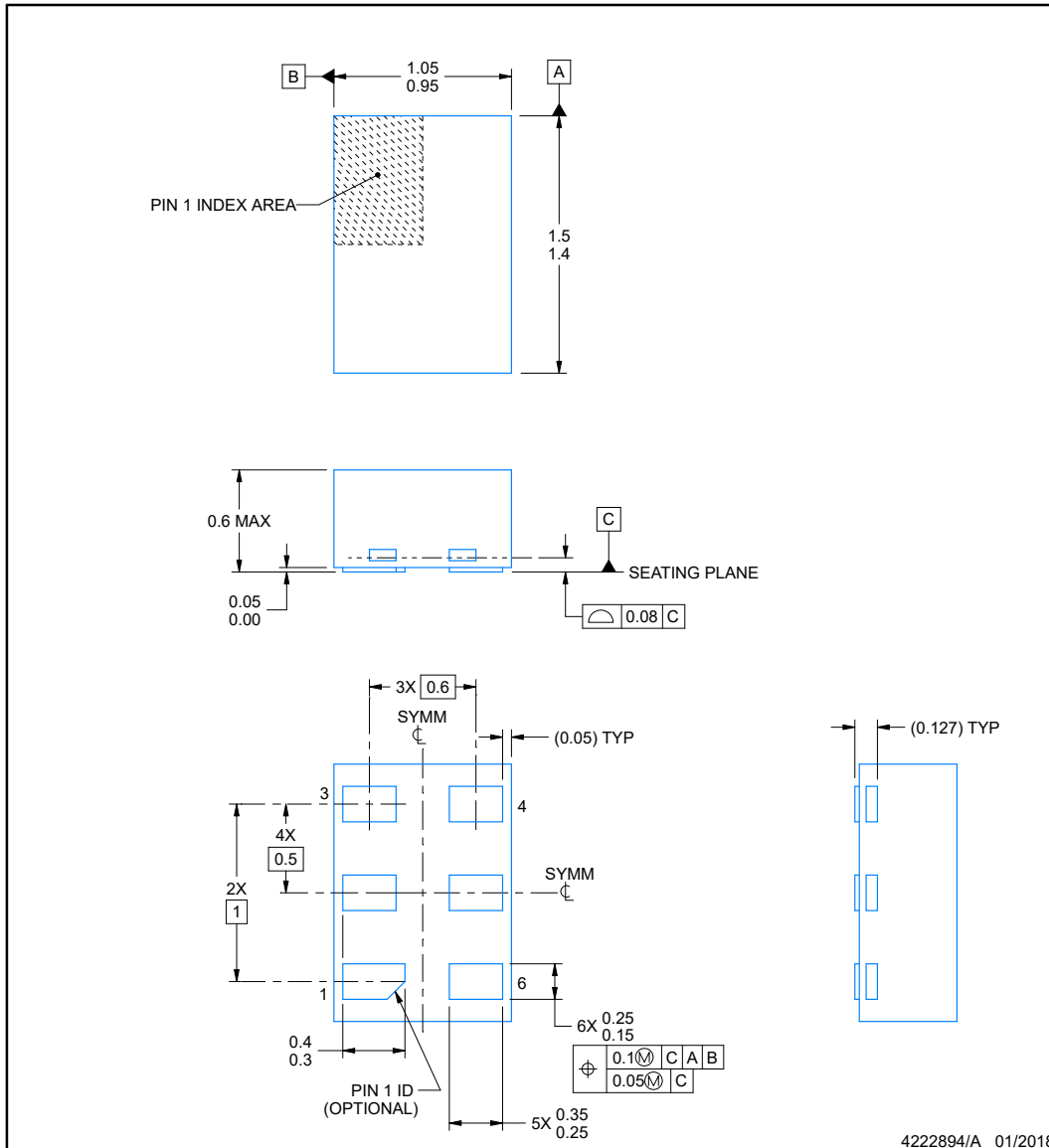
www.ti.com

DRY0006A



PACKAGE OUTLINE
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

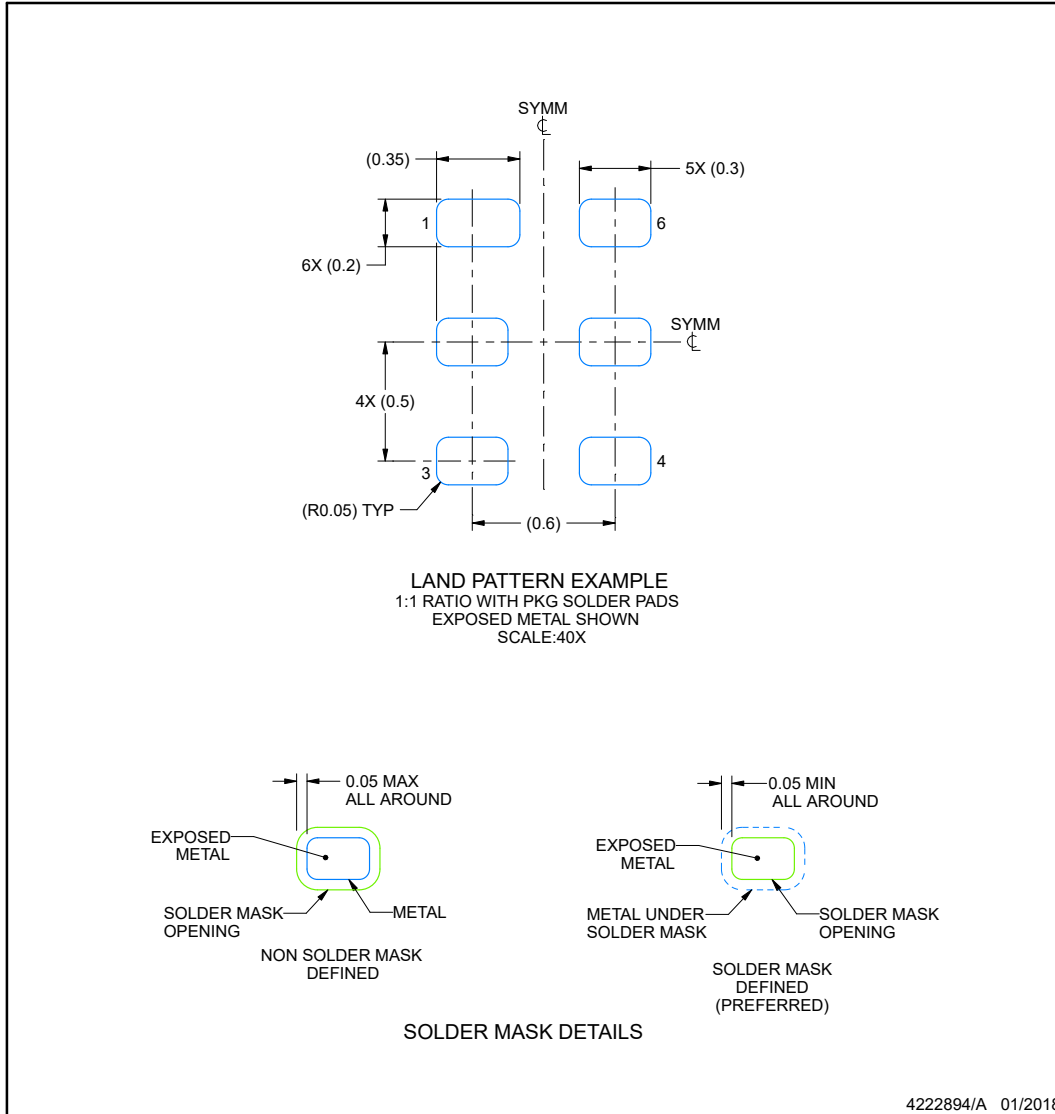
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

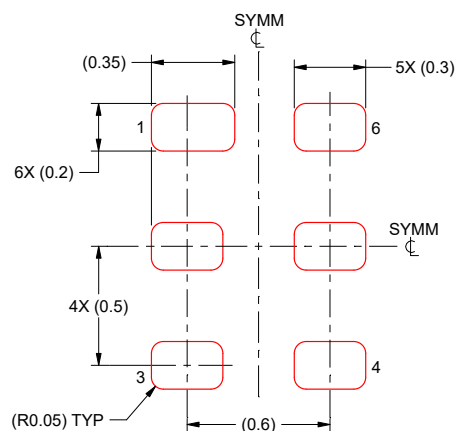
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN74UVP1G04DPWR	Active	Preproduction	X2SON (DPW) 5	3000 LARGE T&R	-	Call TI	Call TI	-	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



SOT - 1.1 max height

Technical drawing of a mechanical part showing three views: front, side, and top.

Front View:

- Overall dimensions: 2.4 (width) x 2.15 (height).
- Feature locations: 1.4, 1.1, 1.3, 1.3.
- Feature sizes: 0.15, 0.1.
- Feature labels: PIN 1 INDEX AREA, NOTE 4.
- Feature control frames: ϕ 0.1 M C A B, 0.1 C.

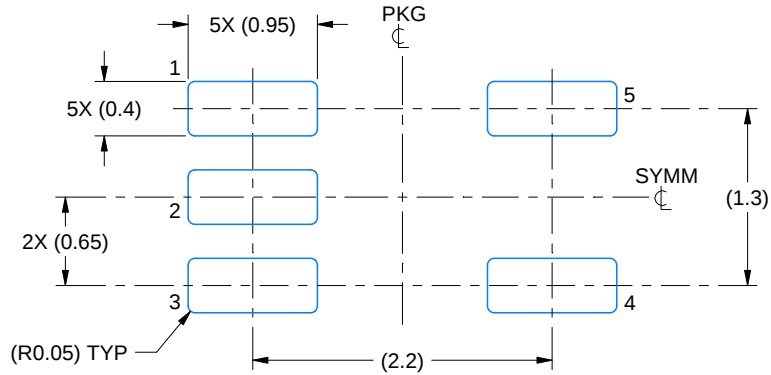
Side View:

- Overall dimensions: 1.1 MAX (width) x 0.1 (thickness).
- Feature label: 4X 0° -12°.

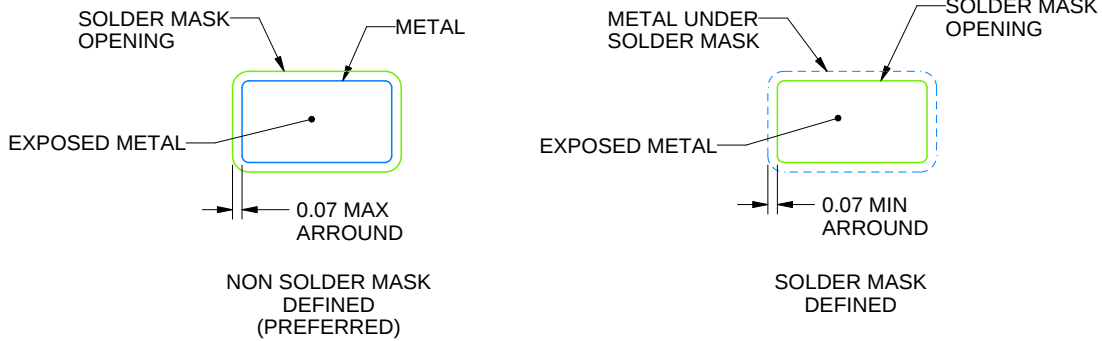
Top View:

- Overall dimensions: 0.46 TYP (width) x 0.22 TYP (height).
- Feature label: 4X 4° -15°.
- Feature label: SEATING PLANE.
- Feature label: GAGE PLANE.
- Feature label: 8° 0° TYP.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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