SN74LVC245B Octal Bus Transceiver With 3-State Outputs

1 Features

- Operating range from 1.1V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Maximum propagation delay of 5ns at 3.3V
- Supports partial-power-down with back drive protection (I_{off})
- High output drive strength:
  - ±24mA at 3.3V
  - ±8mA at 2.3V
  - ±4mA at 1.65V

2 Applications

- Drive an indicator LED
- Redrive a digital signal
- Drive a transmission line
- Hold a signal during controller reset

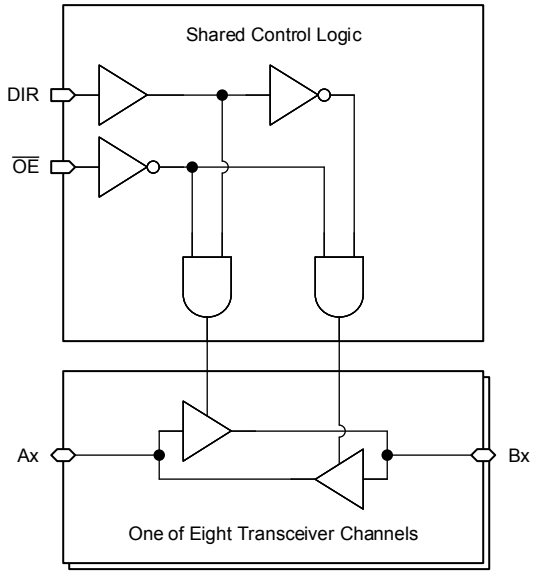
3 Description

The SN74LVC245B is an octal bus transceiver with 3-state outputs. The direction (DIR) pin and output enable ($\overline{OE}$) pin control all eight channels.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC245B	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

Table of Contents

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
I_{IK}	Input clamp diode current, V_I < 0.5V	continuous		–50	mA
	Input clamp diode current, V_I < 0.5V	pulsed 1µs		–200	
I_{OK}	Output clamp diode current, V_O < 0.5V	continuous		–50	mA
	Output clamp diode current, V_O < 0.5V	pulsed 1µs		–200	
I_O	Continuous output current, 0V ≤ V_O ≤ V_{CC}	continuous		±50	mA
		pulsed 1µs		±200	
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	3.6	V
V_I	Input voltage			5.5	V
V_O	Output voltage	Low or high state	0	V_{CC}	V
		High impedance state	0	5.5	
V_{IH}	High-level input voltage	V_{CC} = 1.1V to 1.95V	0.65 x V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3V to 3.6V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.1V to 1.95V		0.35 x V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3V to 3.6V		0.8	

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I_{OH} (1)	High-level output current	V_{CC} = 1.2V		–1	mA
		V_{CC} = 1.5V		–4	
		V_{CC} = 1.8V		–6	
		V_{CC} = 2.5V		–16	
		V_{CC} = 3.3V		–32	
I_{OL} (1)	Low-level output current	V_{CC} = 1.2V		1	mA
		V_{CC} = 1.5V		4	
		V_{CC} = 1.8V		6	
		V_{CC} = 2.5V		16	
		V_{CC} = 3.3V		32	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	125	°C

(1) Recommended maximum output current for continuous operation; see *Electrical Characteristics* for test current values to maintain V_{OH} and V_{OL} specifications. Operating with average output current greater than 32mA may impact device reliability and shorten the device lifetime.

4.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
RKS (VQFN)	20	75.3	77.5	46	19.2	46	30.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –100µA	1.1V to 3.6V	V_{CC} – 0.2			V
	I_{OH}= –4mA	1.65V	1.2			V
	I_{OH}= –8mA	2.3V	1.75			V
	I_{OH}= –12mA	2.7V	2.2			V
		3V	2.4			V
	I_{OH}= –24mA	3V	2.1			V
V_{OL}	I_{OL}= 100µA	1.1V to 3.6V			0.15	V
	I_{OL}= 4mA	1.65V			0.6	V
	I_{OL}= 8mA	2.3V			0.75	V
	I_{OL}= 12mA	2.7V			0.4	V
		3V			0.6	V
	I_{OL}= 24mA	3V			0.8	V
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_{off}	V_I or V_O = V_{CC}	0V to 0.3V			±10	µA
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±15	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V			40	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	2.7V to 3.6V			100	µA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
C_I	V_I = V_{CC} or GND	3.3V		2.9		pF
C_O	V_O = V_{CC} or GND	3.3V		5.1		pF

4.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A or B	B or A	C_L = 30pF	1.2V ± 0.12V			27.6	ns
				1.8V ± 0.15V			9.9	
				2.5V ± 0.2V			5.9	
			C_L = 50pF	2.7V			5.6	
				3.3V ± 0.3V			5	
$t_{e\ n}$	$\overline{OE}$	A or B	C_L = 30pF	1.2V ± 0.12V			54	ns
				1.8V ± 0.15V			14.5	
				2.5V ± 0.2V			8.4	
			C_L = 50pF	2.7V			8.1	
				3.3V ± 0.3V			6.7	
t_{dis}	$\overline{OE}$	A or B	C_L = 30pF	1.2V ± 0.12V			33.8	ns
				1.8V ± 0.15V			12.3	
				2.5V ± 0.2V			7	
			C_L = 50pF	2.7V			7.1	
				3.3V ± 0.3V			6.4	
C_{PD}	A or B	Outputs enabled	f = 10MHz	1.8V		15		pF
				2.5V		16		
				3.3V		18		
		Outputs disabled	f = 10MHz	1.8V		4		
				2.5V		4		
				3.3V		5		

5 Parameter Measurement Information

Phase relationships between waveforms are selected arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

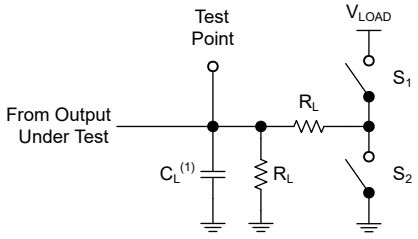
The outputs are measured individually with one input transition per measurement.

Table 5-1. 3-State Outputs

TEST	S1	S2
t_{PLH}, t_{PHL}	OPEN	OPEN
t_{PLZ}, t_{PZL}	CLOSED	OPEN
t_{PHZ}, t_{PZH}	OPEN	CLOSED

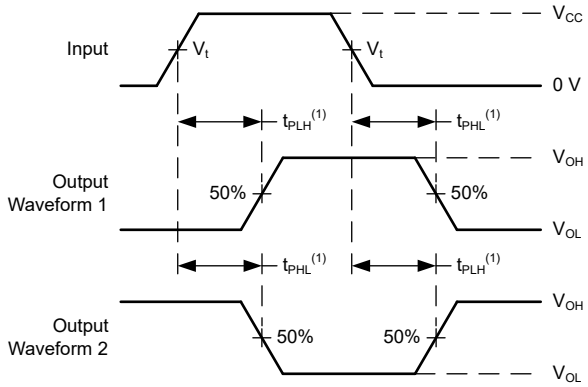
Table 5-2. 3-State or Open-Drain Outputs

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
1.2V ± 0.1V	V_{CC}/2	2kΩ	30pF	0.1V	2×V_{CC}
1.5V ± 0.12V	V_{CC}/2	2kΩ	30pF	0.1V	2×V_{CC}
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V	2×V_{CC}
2.7V	1.5V	500Ω	50pF	0.3V	6V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V	6V



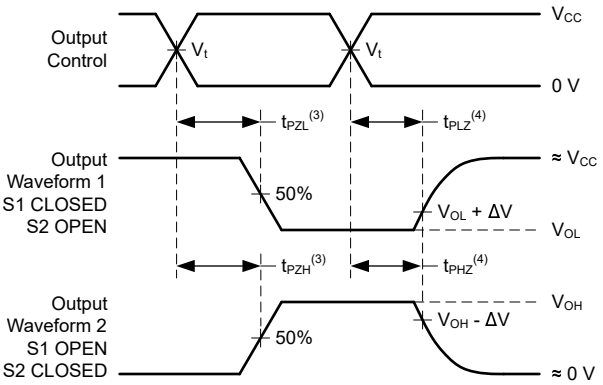
(1) C_L includes probe and test-fixture capacitance.

Figure 5-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

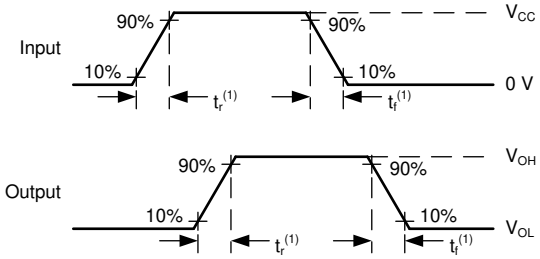
Figure 5-2. Voltage Waveforms Propagation Delays



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 5-3. Voltage Waveforms Enable and Disable Times



(1) The greater between t_r and t_f is the same as t_t.

Figure 5-4. Voltage Waveforms, Input and Output Transition Times

6 Detailed Description

6.1 Overview

The SN74LVC245B contains 8 individual high-speed CMOS transceivers with 3-state outputs.

Each transceiver includes one buffer oriented from Ax to Bx and one from Bx to Ax, with at least one output disabled at all times. The direction (DIR) pin controls which buffer is active. The buffer that is not active has the output placed into the high-impedance state.

The output enable ($\overline{OE}$) controls all outputs in the device. When the $\overline{OE}$ pin is in the low state, the appropriate outputs as the direction (DIR) pin determines are enabled. When the $\overline{OE}$ pin is in the high state, all outputs of the device are disabled. All disabled outputs are placed into the high-impedance state.

To establish the high-impedance state during power up or power down, tie the $\overline{OE}$ pin to V_{CC} through a pull-up resistor; the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table determine the minimum value of the resistor. Typically, a 10kΩ resistor is sufficient.

6.2 Functional Block Diagram

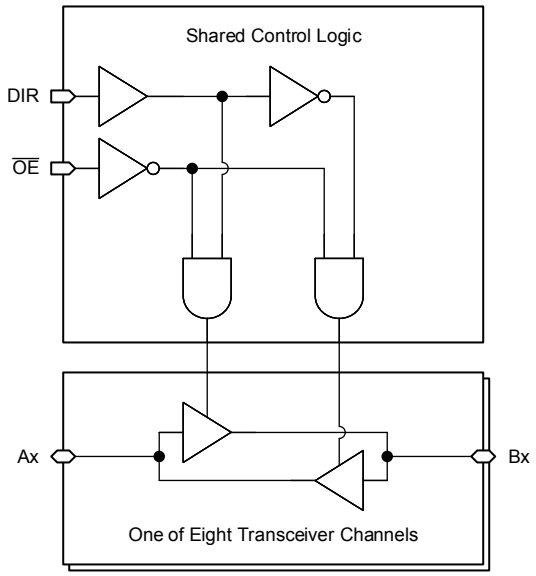


Figure 6-1. Logic Diagram (Positive Logic) for SN74LVC245B

6.3 Feature Description

6.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

6.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

6.3.3 CMOS IOs

This device includes input/output (IO) pins. These pins can be configured as either an input or an output. Resistors are required when terminating unused IO pins due to the possibility of the pin acting as an output.

Terminate unused transceiver channels as shown in Figure 6-2.

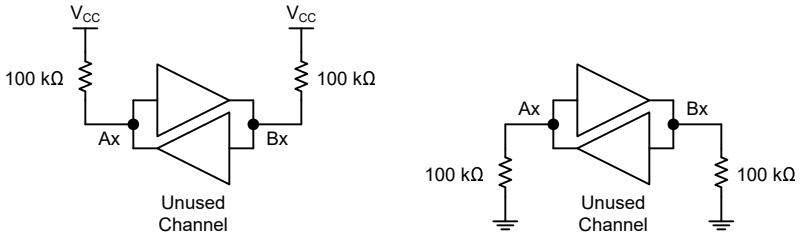


Figure 6-2. Proper Termination of Unused Transceiver Channels

6.3.4 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

6.3.5 Clamp Diode Structure

Figure 6-3 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

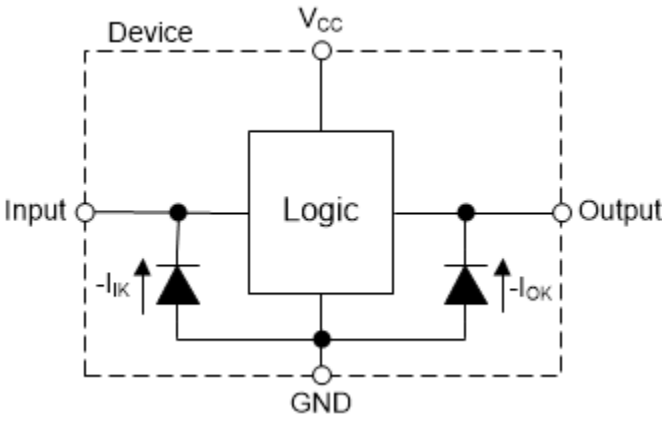


Figure 6-3. Electrical Placement of Clamping Diodes for Each Input and Output

6.3.6 Over-Voltage Tolerant Inputs

The SN74LVC245B includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

CAUTION

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

6.4 Device Functional Modes

Table 6-1 lists the functional modes of the SN74LVC245B.

Table 6-1. Function Table

INPUTS(1)		OUTPUTS(2)	
$\overline{OE}$	DIR	A	B
L	L	B	Z
L	H	Z	A
H	X	Z	Z

(1) H = High voltage level, L = Low voltage level, X = Don't care
(2) A = Logic value at 'A' input, B = Logic value at 'B' input, Z = High impedance

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

SN74LVC245B is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

7.2 Typical Application

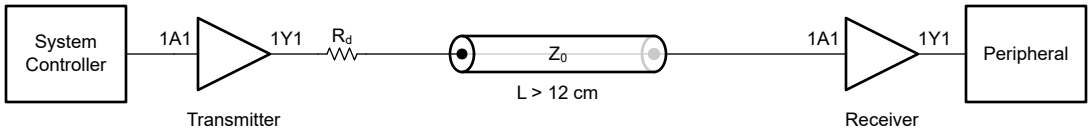


Figure 7-1. Application Schematic

7.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

7.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specification, see ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended maximum Output Conditions:
   - Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs must not be pulled above V_{CC}.

7.2.3 Application Curves

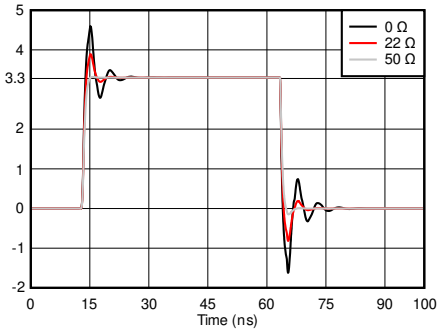


Figure 7-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

7.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

7.4 Layout

7.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

7.4.2 Layout Example

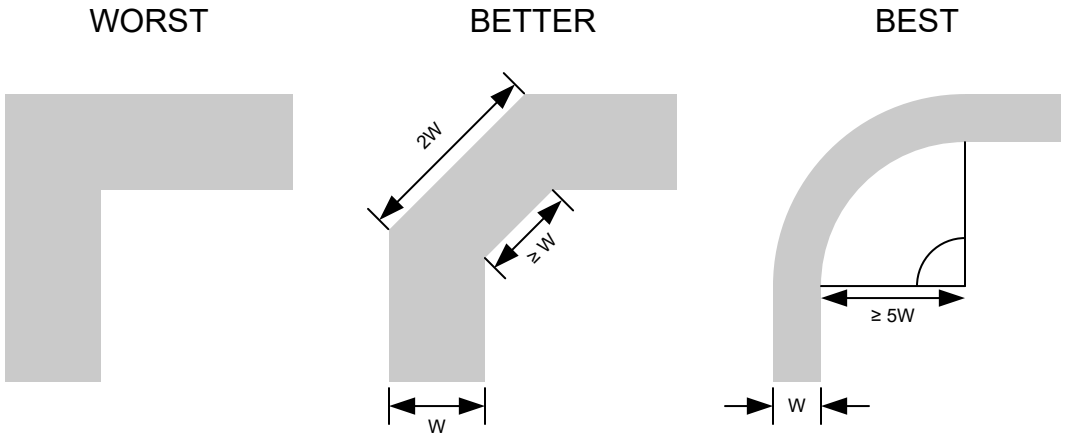


Figure 7-3. Example Trace Corners for Improved Signal Integrity

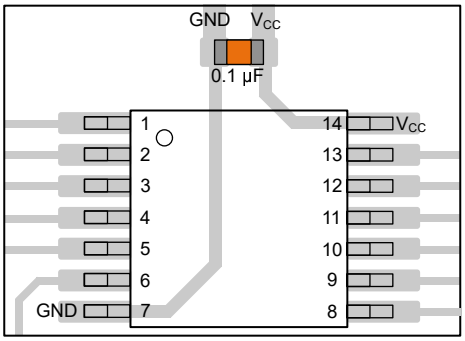


Figure 7-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

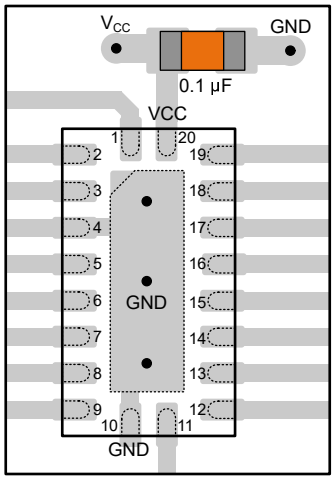


Figure 7-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

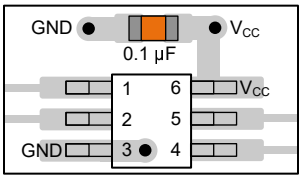


Figure 7-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

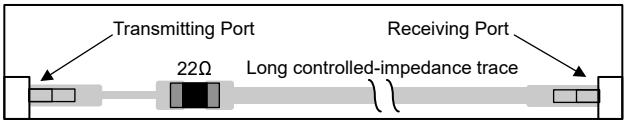


Figure 7-7. Example Damping Resistor Placement for Improved Signal Integrity

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

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