# SN74LVC1G97 Configurable Multiple-Function Gate

## 1 Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to $V_{CC}$
- Max $t_{pd}$ of 6.3 ns at 3.3 V
- Low Power Consumption, 10-µA Max $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Choose From Nine Specific Logic Functions

## 2 Applications

- Barcode Scanners
- Cable Solutions
- E-Books
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboards and PSUs
- Software Defined Radios (SDR)
- TVs: High Definition (HDTV), LCD, and Digital
- Video Communications Systems
- Wireless Data Access Cards, Headsets, Keyboard, Mouse, and LAN Cards

## 3 Description

The SN74LVC1G97 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to $V_{CC}$ or GND.

This configurable multiple-function gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going ($V_T$+) and negative-going ($V_T$–) signals.

NanoFree package technology is a major break-through in IC packaging concepts, using the die as the package.

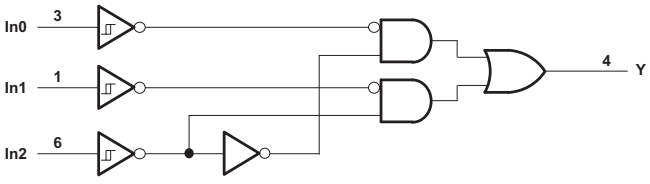
This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC1G97DBV | SOT-23 (6) | 2.90 mm × 1.60 mm |
| SN74LVC1G97DCK | SC70 (6) | 2.00 mm × 1.25 mm |
| SN74LVC1G97DRL | SOT (6) | 1.60 mm × 1.20 mm |
| SN74LVC1G97DRY | | 1.45 mm × 1.00 mm |
| SN74LVC1G97DSF | | 1.00 mm × 1.00 mm |
| SN74LVC1G97YZP | DSBGA (6) | 1.41 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision M (June 2015) to Revision N** — **Page**

- Changed body size for SN74LVC1G97DRY to 1.45 mm × 1.00 mm ... 1
- Changed body size for SN74LVC1G97DSF to 1.00 mm × 1.00 mm ... 1
- Added Junction temperature, $T_J$ in *Absolute Maximum Ratings* ... 4
- Added Operating free-air temperature, $T_A$ for BGA package in *Recommended Operating Conditions* ... 4
- Added *Receiving Notification of Documentation Updates* section ... 14

**Changes from Revision L (December 2013) to Revision M** — **Page**

- Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

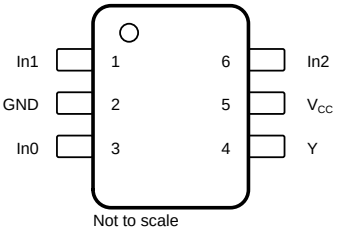
**Changes from Revision K (October 2011) to Revision L** — **Page**

- Updated document to new TI data sheet format. ... 1
- Removed *Ordering Information* table. ... 1
- Updated $I_{off}$ in *Features* ... 1
- Updated operating temperature range. ... 4


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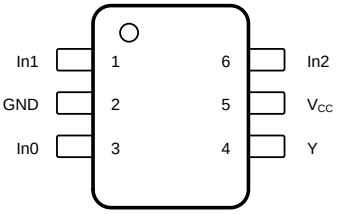
# 5 Pin Configuration and Functions

**DBV Package**
**6-Pin SOT-23**
**(Top View)**



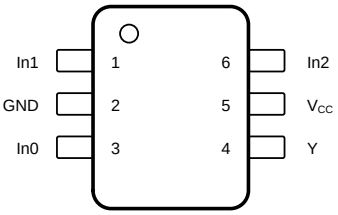

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**DCK Package**
**6-Pin SC70**
**(Top View)**



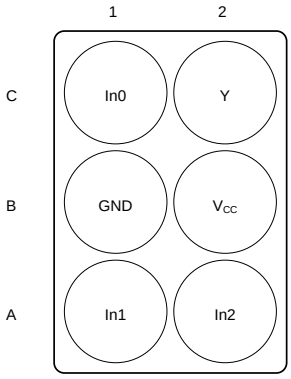

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**DRL Package**
**6-Pin SOT**
**(Top View)**



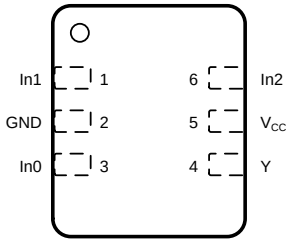

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**YZP Package**
**6-Pin DSBGA**
**(Bottom View)**



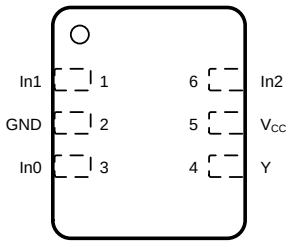

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**DRY Package**
**6-Pin SON**
**(Top View)**




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**DSF Package**
**6-Pin SON**
**(Top View)**




Not to scale

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DCT, DCU, DRY | YZP | | |
| In0 | 3 | C1 | I | Input 0 |
| In1 | 1 | A1 | I | Input 1 |
| In2 | 6 | A2 | I | Input 2 |
| GND | 2 | B1 | — | Ground |
| $V_{CC}$ | 5 | B2 | — | Power |
| Y | 4 | C2 | O | Output |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 V | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 V | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101\(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

See (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $T_A$ | Operating free-air temperature | BGA package | –40 | 85 | °C |
| | | All other packages | –40 | 125 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LVC1G97 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DRL (SOT) | YZP (DSBGA) | |
| | | 6 PINS | 6 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 165 | 259 | 142 | 123 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | –40°C TO +85°C | | | –40°C TO +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | |
| $V_{T+}$ Positive-going input threshold voltage | | 1.65 V | 0.79 | | 1.16 | 0.79 | | 1.16 | V |
| | | 2.3 V | 1.11 | | 1.56 | 1.11 | | 1.56 | |
| | | 3 V | 1.5 | | 1.87 | 1.5 | | 1.87 | |
| | | 4.5 V | 2.16 | | 2.74 | 2.16 | | 2.74 | |
| | | 5.5 V | 2.61 | | 3.33 | 2.61 | | 3.33 | |
| $V_{T-}$ Negative-going input threshold voltage | | 1.65 V | 0.35 | | 0.62 | 0.35 | | 0.62 | V |
| | | 2.3 V | 0.58 | | 0.87 | 0.58 | | 0.87 | |
| | | 3 V | 0.84 | | 1.19 | 0.84 | | 1.19 | |
| | | 4.5 V | 1.41 | | 1.9 | 1.41 | | 1.9 | |
| | | 5.5 V | 1.87 | | 2.29 | 1.87 | | 2.29 | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 1.65 V | 0.3 | | 0.62 | 0.3 | | 0.62 | V |
| | | 2.3 V | 0.4 | | 0.8 | 0.4 | | 0.8 | |
| | | 3 V | 0.53 | | 0.87 | 0.53 | | 0.87 | |
| | | 4.5 V | 0.71 | | 1.04 | 0.71 | | 1.04 | |
| | | 5.5 V | 0.71 | | 1.11 | 0.71 | | 1.11 | |
| $V_{OH}$ | $I_{OH}$ = –100 µA | 1.65 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | V |
| | $I_{OH}$ = –4 mA | 1.65 V | 1.2 | | | 1.2 | | | |
| | $I_{OH}$ = –8 mA | 2.3 V | 1.9 | | | 1.9 | | | |
| | $I_{OH}$ = –16 mA | 3 V | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | 2.3 | | | 2.3 | | | |
| | $I_{OH}$ = –32 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 4 mA | 1.65 V | | | 0.45 | | | 0.45 | |
| | $I_{OL}$ = 8 mA | 2.3 V | | | 0.3 | | | 0.3 | |
| | $I_{OL}$ = 16 mA | 3 V | | | 0.4 | | | 0.45 | |
| | $I_{OL}$ = 24 mA | | | | 0.55 | | | 0.55 | |
| | $I_{OL}$ = 32 mA | 4.5 V | | | 0.55 | | | 0.58 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±5 | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | 0 | | | ±10 | | | ±10 | µA |
| $I_{CC}$ | $V_I$ = 5.5 V or GND, $I_O$ = 0 | 1.65 V to 5.5 V | | | 10 | | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V | | | 500 | | | 500 | µA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 3.5 | | | 3.5 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

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## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C TO 85°C | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Any In | Y | 3.2 | 14.4 | 2 | 8.3 | 1.5 | 6.3 | 1.1 | 5.1 | ns |

## 6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C TO 125°C | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Any In | Y | 3.2 | 16.4 | 2 | 9.3 | 1.5 | 7.3 | 1.1 | 6.1 | ns |

## 6.8 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 22 | 23 | 23 | 26 | pF |

## 6.9 Typical Characteristics

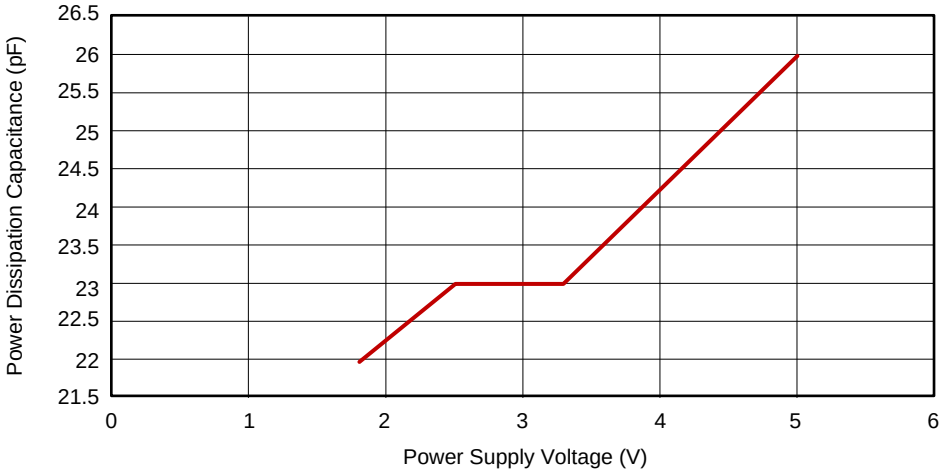
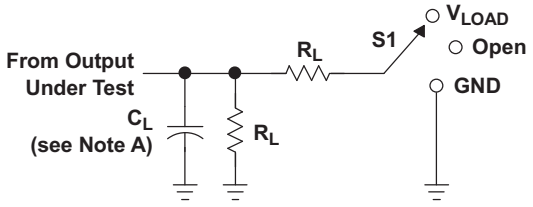



**Figure 1. Power Dissipation Capacitance vs Power Supply Voltage**


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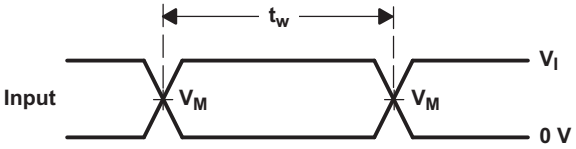
# 7 Parameter Measurement Information



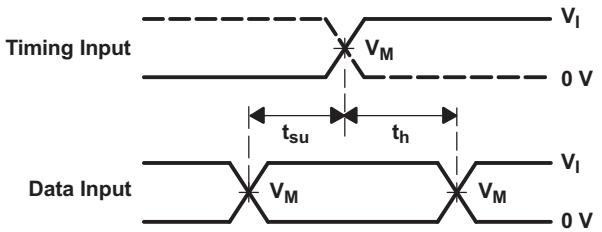

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

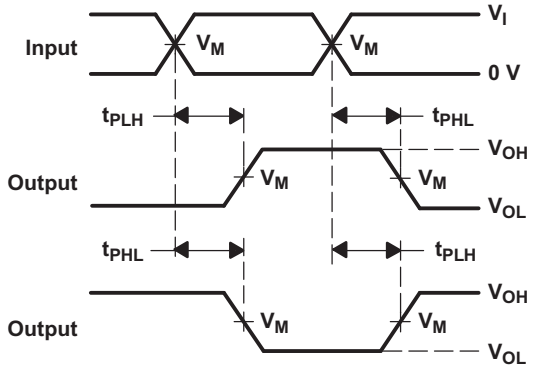
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



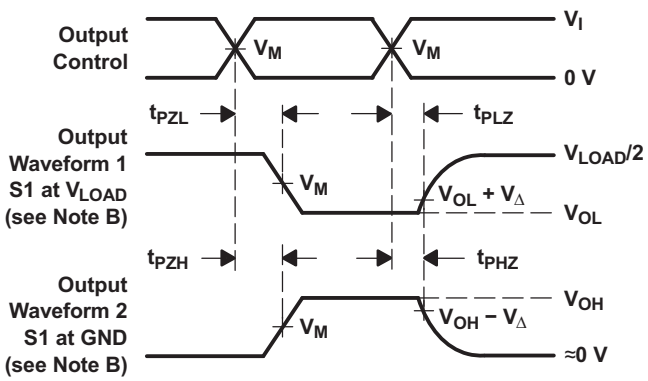

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, $Z_O$ = 50 W.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

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# 8 Detailed Description

## 8.1 Overview

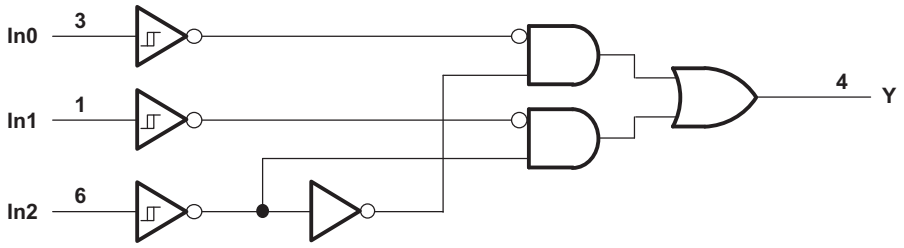
This configurable multiple-function gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1G97 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose variations of common logic functions, like AND, OR, and NOT. All inputs can be connected to $V_{CC}$ or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going ($V_{T+}$) and negative-going ($V_{T-}$) signals.

This device is fully-specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

The SN74LVC1G97 device has a wide operating $V_{CC}$ range of 1.65 V to 5.5 V, which allows use in a broad range of systems. The 5.5-V I/Os allow down translation and also allow voltages at the inputs when $V_{CC}$ = 0 V.

## 8.4 Device Functional Modes

Table 1 shows the functional modes of SN74LVC1G97.

**Table 1. Function Table**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| In2 | In1 | In0 | Y |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |


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**Table 2. Function Selection Table**

| LOGIC FUNCTION | FIGURE NUMBER |
|---|---|
| 2-to-1 data selector | Figure 3 |
| 2-input AND gate | Figure 4 |
| 2-input OR gate with one inverted input | Figure 5 |
| 2-input NAND gate with one inverted input | Figure 5 |
| 2-input AND gate with one inverted input | Figure 6 |
| 2-input NOR gate with one inverted input | Figure 6 |
| 2-input OR gate | Figure 7 |
| Inverter | Figure 8 |
| Noninverted buffer | Figure 9 |

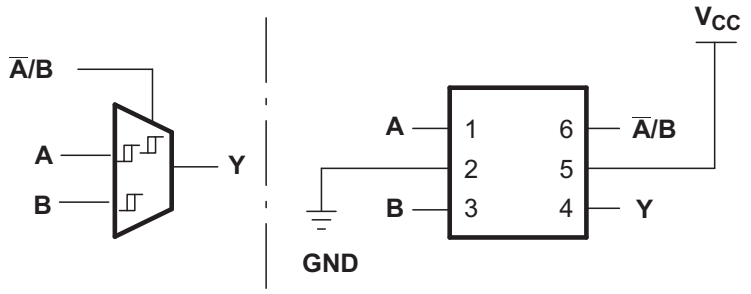



**Figure 3. 2-to-1 Data Selector**

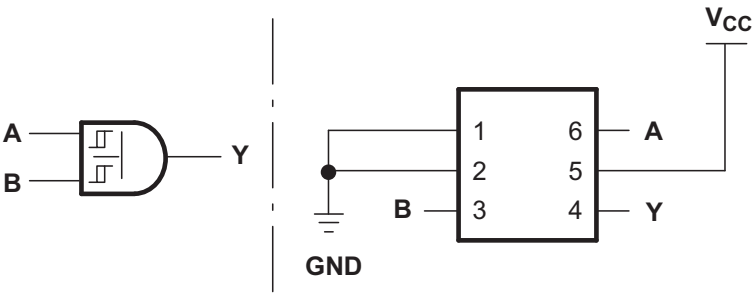



**Figure 4. 2-Input AND Gate**

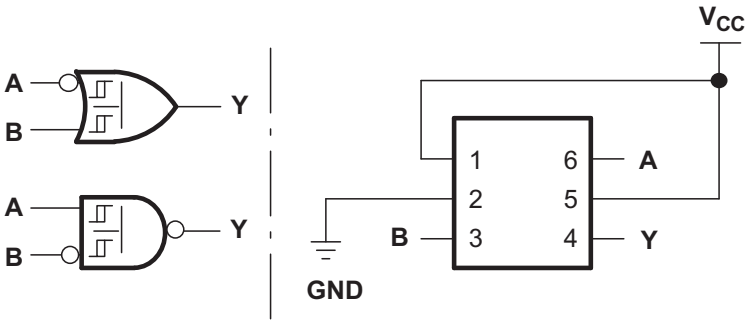



**Figure 5. 2-Input OR Gate With One Inverted Input**
**2-Input NAND Gate With One Inverted Input**

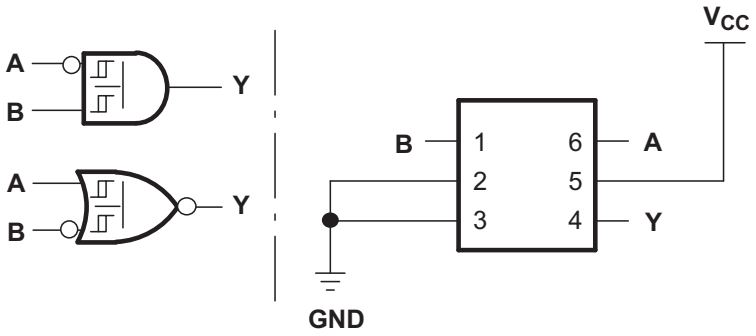



**Figure 6. 2-Input AND Gate With One Inverted Input**
**2-Input NOR Gate With One Inverted Input**

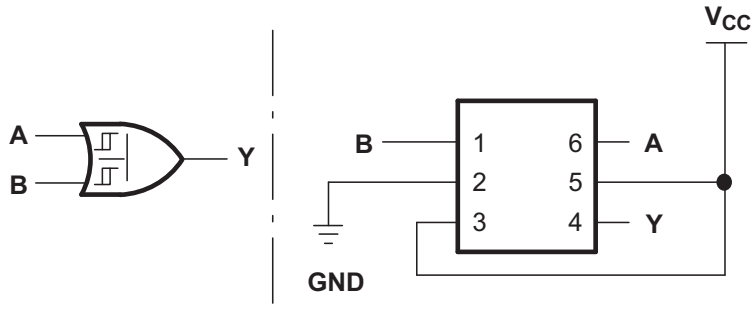



**Figure 7. 2-Input OR Gate**

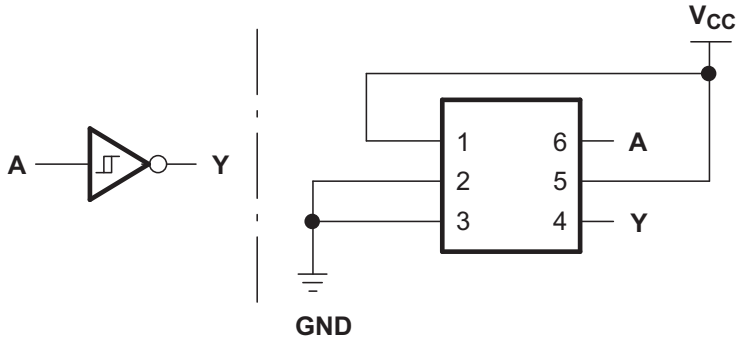



**Figure 8. Inverter**

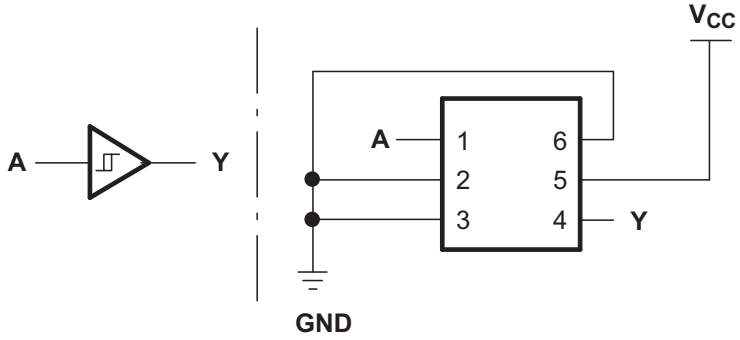



**Figure 9. Noninverted Buffer**


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC1G97 device offers flexible configuration for many design applications. This example describes basic power sequencing using the AND gate configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning.

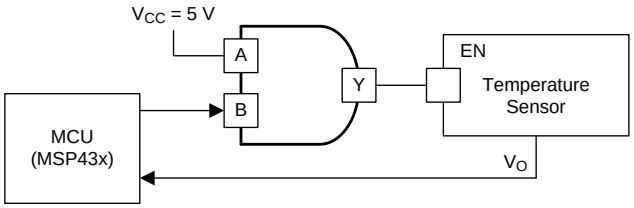



**Figure 10. Simplified Application**

## 9.2 Typical Application

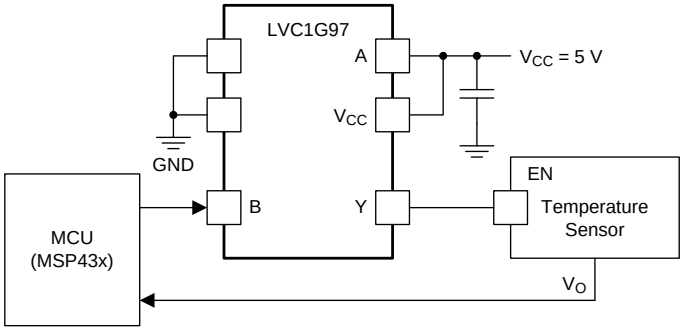



**Figure 11. Typical Application**

### 9.2.1 Design Requirements

- Recommended input conditions:
  - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the *Recommended Operating Conditions* table.
  - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in the *Recommended Operating Conditions* table.
  - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid $V_{CC}$.
- Recommended output conditions:
  - Load currents must not exceed ±50 mA.
- Frequency selection criterion:
  - Figure 12 illustrates the effects of frequency on output current.
  - Added trace resistance and capacitance can reduce maximum frequency capability. Follow the layout practices listed in the *Layout* section.

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## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

The SN74LVC1G97 device uses CMOS technology and has balanced output drive. Avoid bus contentions that can drive currents that can exceed maximum limits.

The SN74LVC1G97 allows for performing logical Boolean functions with digital signals. Maintain input signals as close as possible to either 0 V or $V_{CC}$ for optimal operation.

### 9.2.3 Application Curve

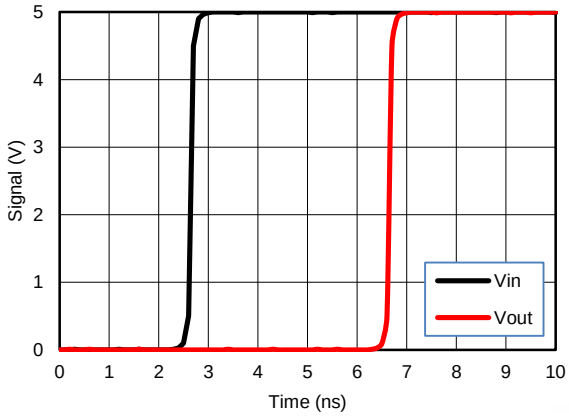



**Figure 12. Simulated Input-to-Output Voltage Response Showing Propagation Delay at $V_{CC}$ = 5 V**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table.

To prevent power disturbance, ensure good bypass capacitance for each $V_{CC}$ terminal. For devices with a single-supply, a 0.1-μF bypass capacitor is recommended. If multiple pins are labeled $V_{CC}$, then a 0.01-μF or 0.022-μF capacitor is recommended for each $V_{CC}$ because the $V_{CC}$ pins are tied together internally. For devices with dual supply pins operating at different voltages, for example $V_{CC}$ and $V_{DD}$, a 0.1-μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. Place the bypass capacitor as close to the power terminal as possible for best results.


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# 11 Layout

## 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. Figure 13 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

## 11.2 Layout Example

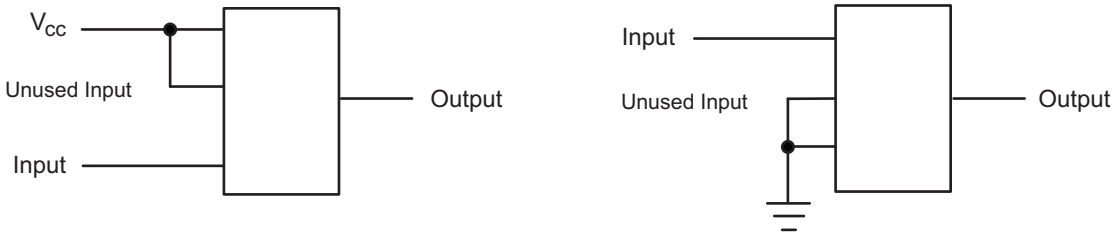



**Figure 13. Layout Diagrams**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *Selecting the Right Texas Instruments Signal Switch*, SZZA030

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G97DBVR | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (C975, C97K, C97R) |
| SN74LVC1G97DBVR.B | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (C975, C97K, C97R) |
| SN74LVC1G97DBVRE4 | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (C975, C97K, C97R) |
| SN74LVC1G97DBVRG4 | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C975, C97K, C97R) |
| SN74LVC1G97DBVT | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C975, C97K, C97R) |
| SN74LVC1G97DBVT.B | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C975, C97K, C97R) |
| SN74LVC1G97DBVTG4 | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C975, C97K, C97R) |
| SN74LVC1G97DCKR | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (CS5, CSF, CSJ, CSK, CSR) |
| SN74LVC1G97DCKR.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (CS5, CSF, CSJ, CSK, CSR) |
| SN74LVC1G97DCKRE4 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS5 |
| SN74LVC1G97DCKRG4 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS5 |
| SN74LVC1G97DCKRG4.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS5 |
| SN74LVC1G97DCKT | Active | Production | SC70 (DCK) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (CS5, CSF, CSJ, CSK, CSR) |
| SN74LVC1G97DCKT.B | Active | Production | SC70 (DCK) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CS5, CSF, CSJ, CSK, CSR) |
| SN74LVC1G97DCKTG4 | Active | Production | SC70 (DCK) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS5 |
| SN74LVC1G97DCKTG4.B | Active | Production | SC70 (DCK) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS5 |
| SN74LVC1G97DRLR | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (1K4, CS7, CSR) |
| SN74LVC1G97DRLR.B | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (1K4, CS7, CSR) |
| SN74LVC1G97DRYR | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |
| SN74LVC1G97DRYR.B | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |
| SN74LVC1G97DRYRG4 | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G97DRYRG4.B | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |
| SN74LVC1G97DSFR | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |
| SN74LVC1G97DSFR.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |
| SN74LVC1G97DSFRG4 | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |
| SN74LVC1G97DSFRG4.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CS |
| SN74LVC1G97YZPR | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CSN |
| SN74LVC1G97YZPR.B | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CSN |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G97 :**

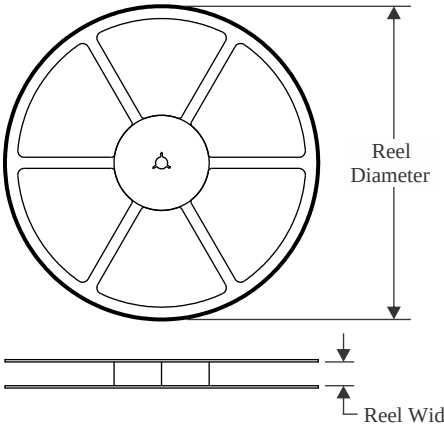
- Automotive : SN74LVC1G97-Q1
- Enhanced Product : SN74LVC1G97-EP

NOTE: Qualified Version Definitions:

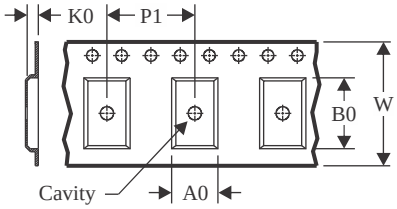
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

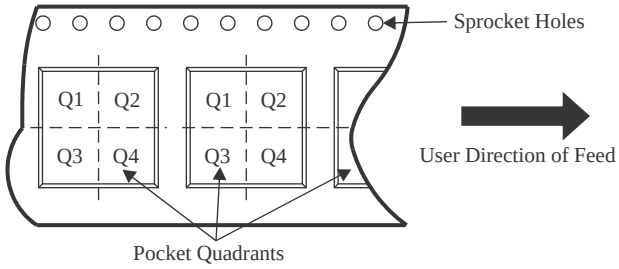



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

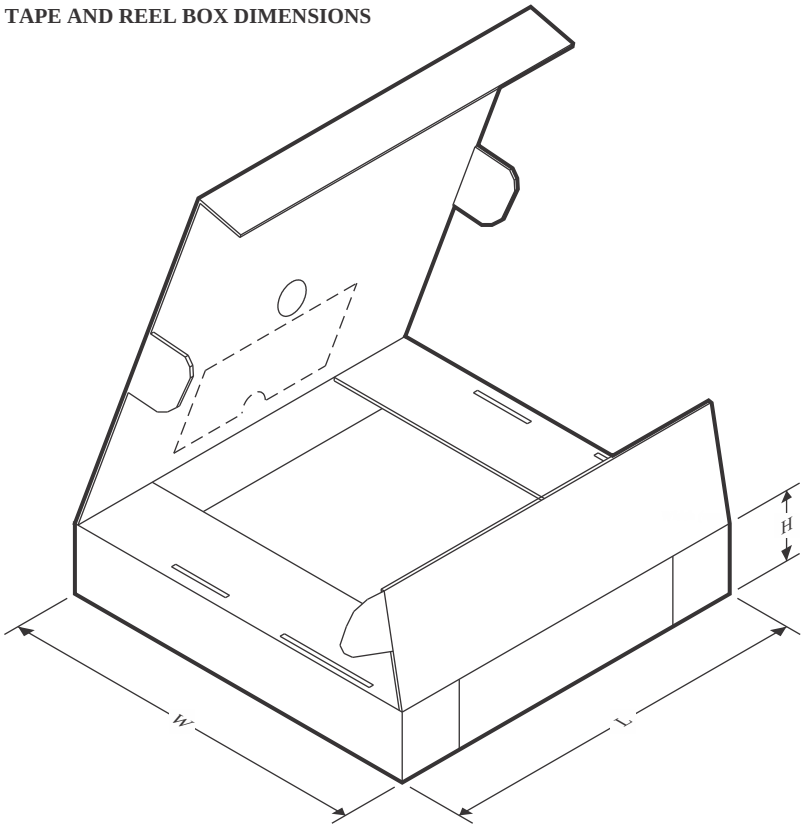



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G97DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DBVRG4 | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKRG4 | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DCKTG4 | SC70 | DCK | 6 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74LVC1G97DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G97DRYRG4 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G97DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G97DSFRG4 | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G97YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G97DBVR | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G97DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G97DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DBVRG4 | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DBVT | SOT-23 | DBV | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G97DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DCKRG4 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G97DCKTG4 | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G97DRLR | SOT-5X3 | DRL | 6 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G97DRLR | SOT-5X3 | DRL | 6 | 4000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G97DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G97DRYRG4 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G97DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G97DSFRG4 | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G97YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

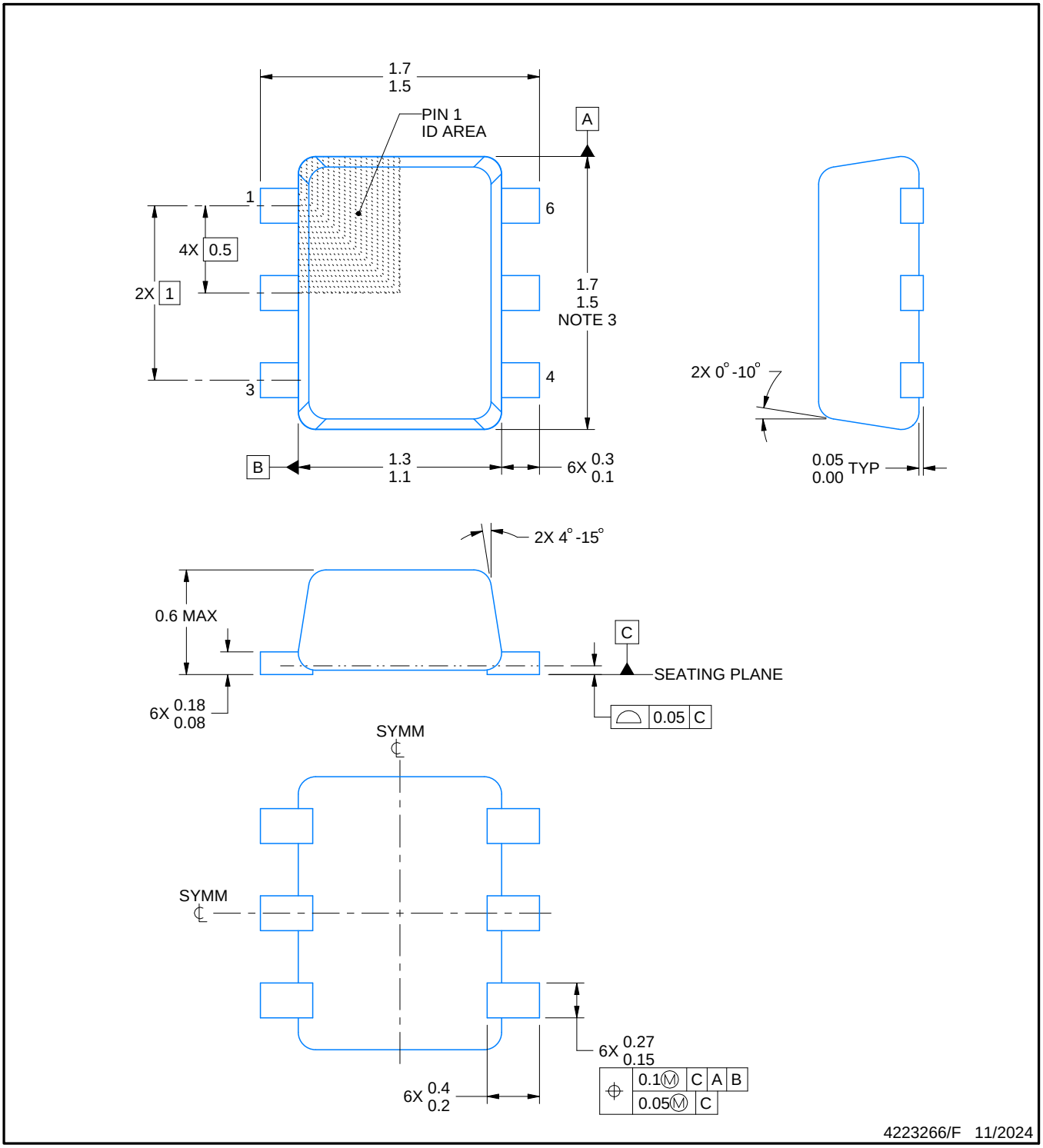


# PACKAGE OUTLINE

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




NOTES:

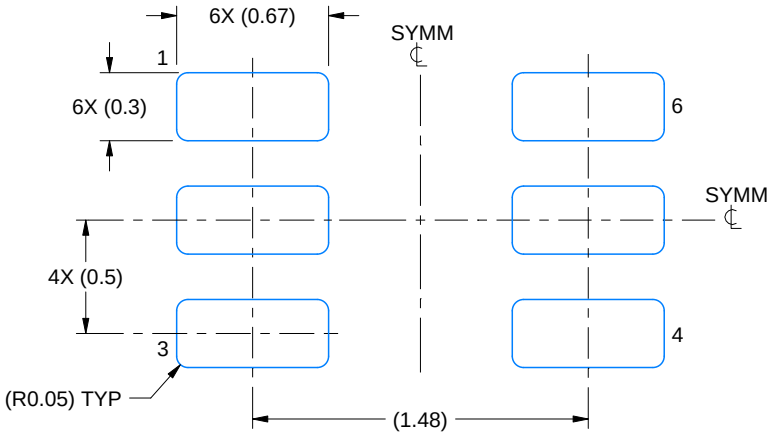
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

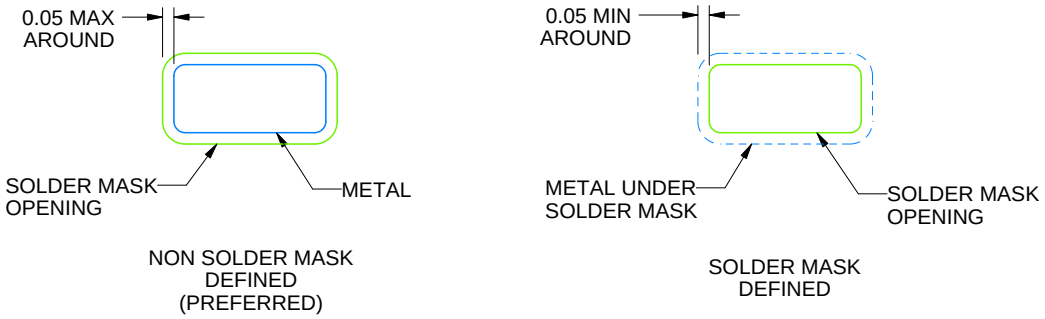
## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
SCALE:30X




SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

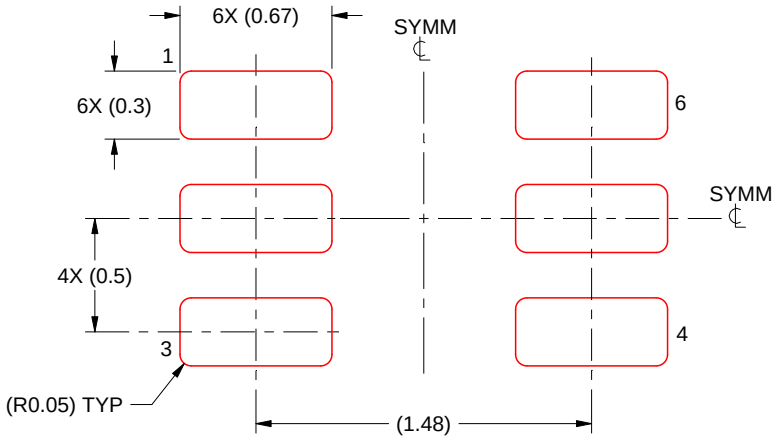
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

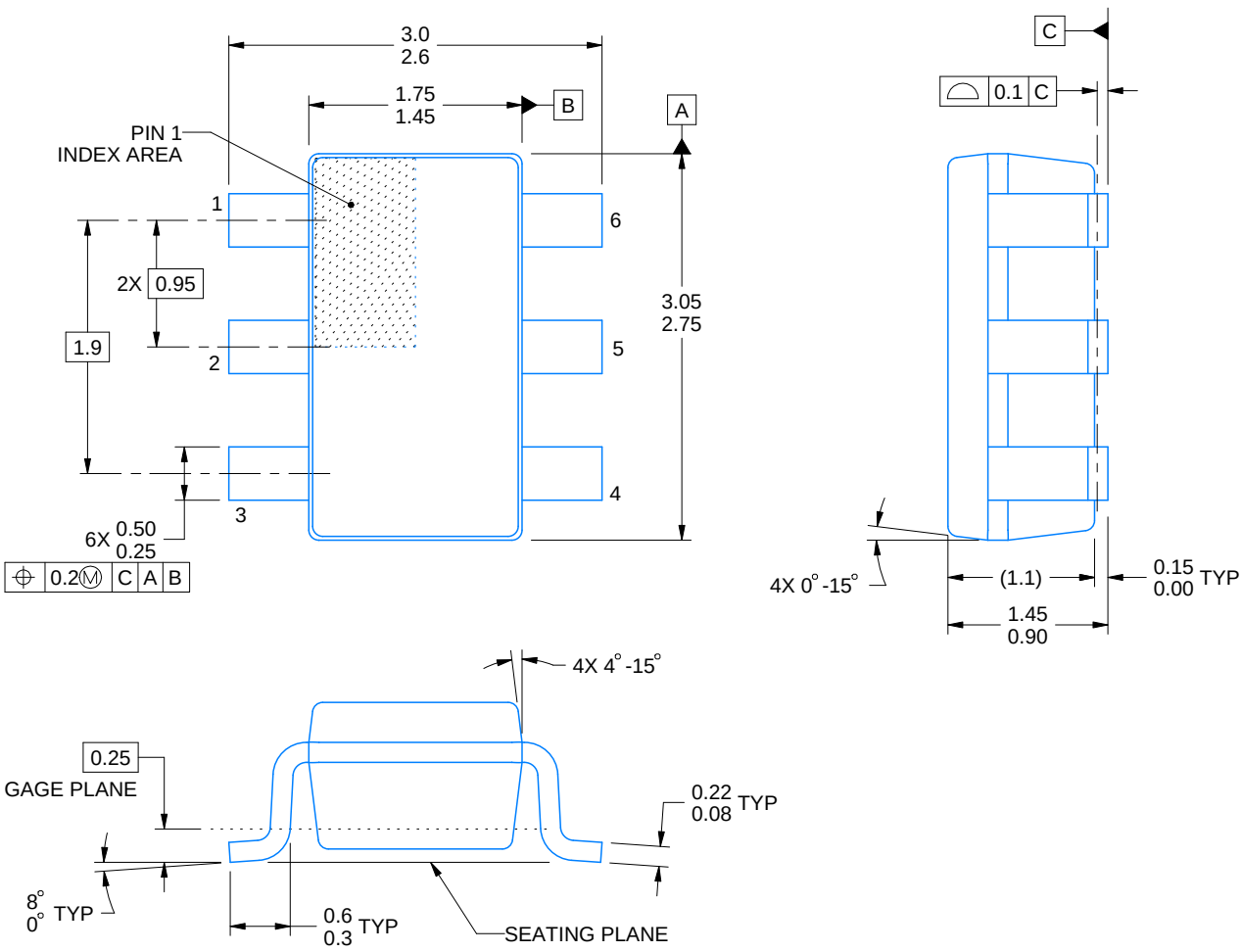
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

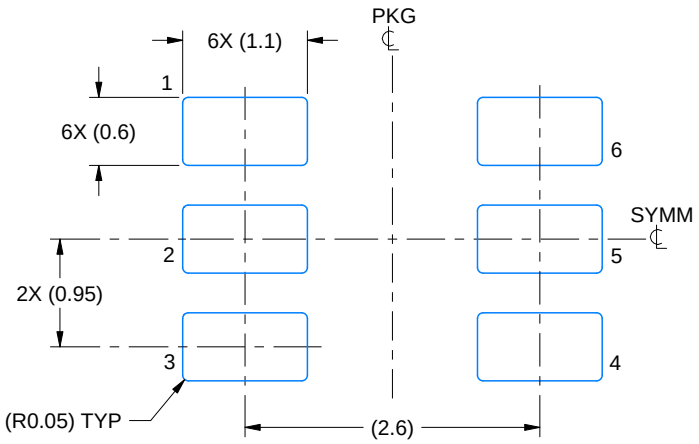
SMALL OUTLINE TRANSISTOR



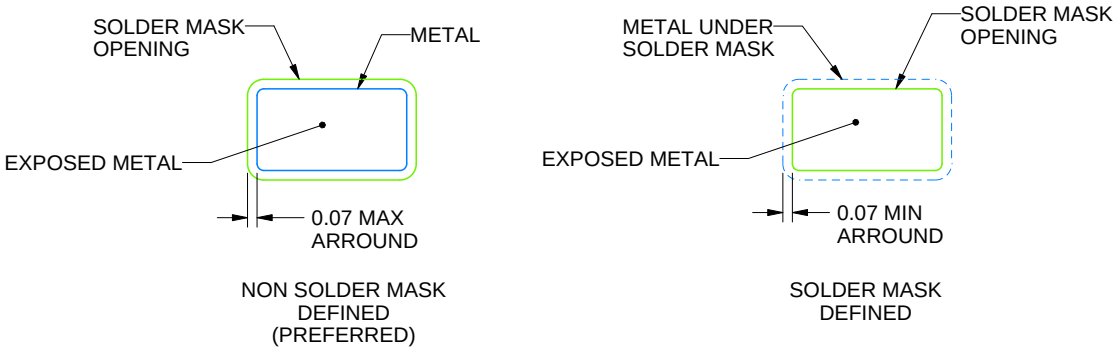

4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

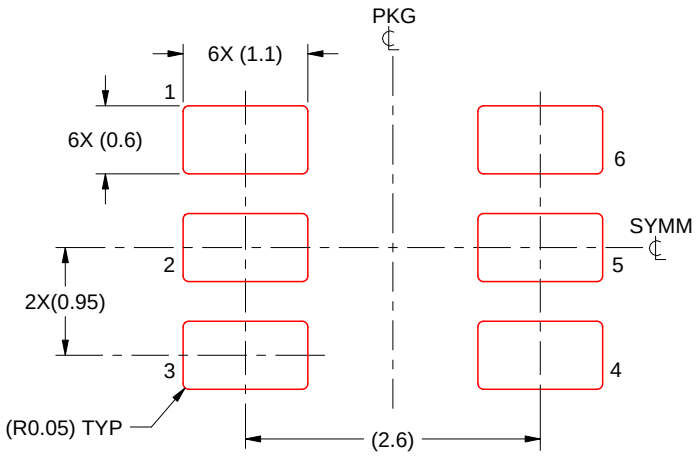



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

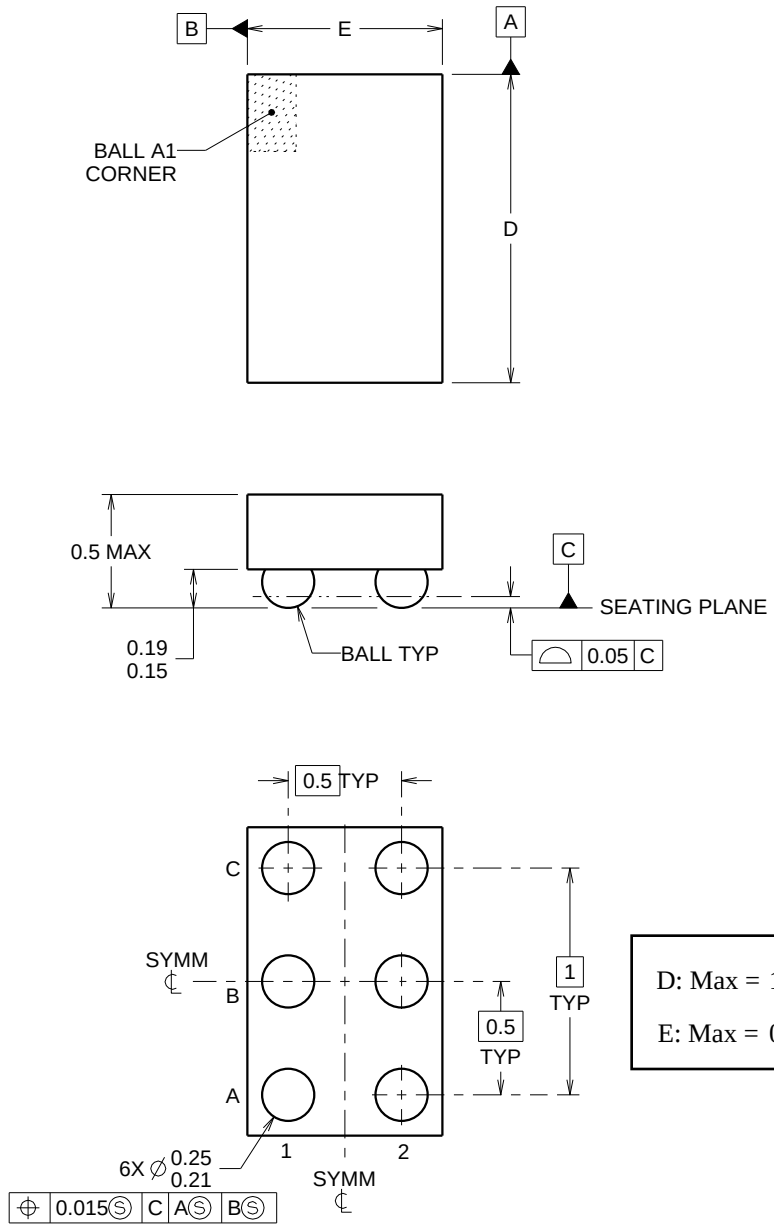
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## YZP0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




D: Max = 1.418 mm, Min =1.357 mm

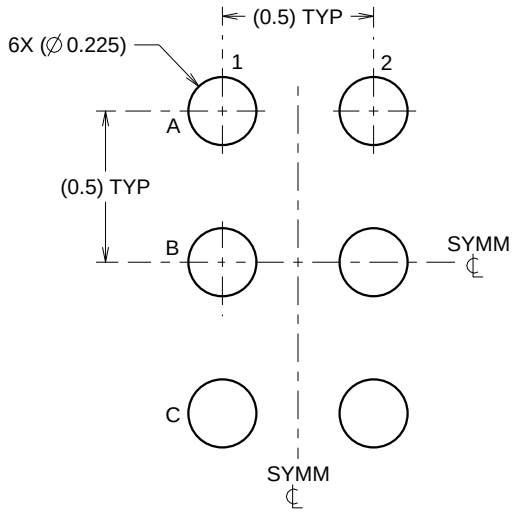
E: Max = 0.918 mm, Min =0.857 mm

4219524/A 06/2014

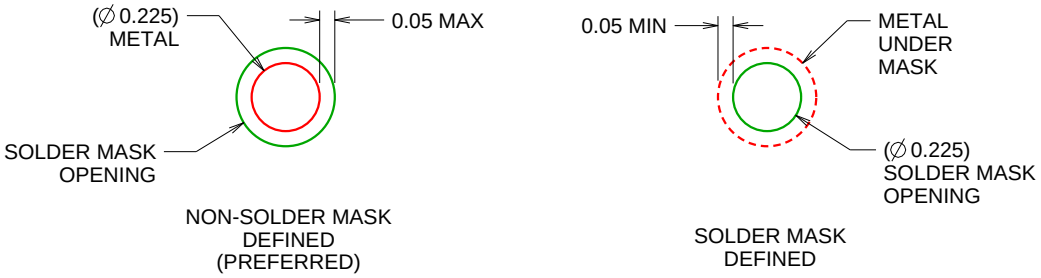
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
SCALE:40X

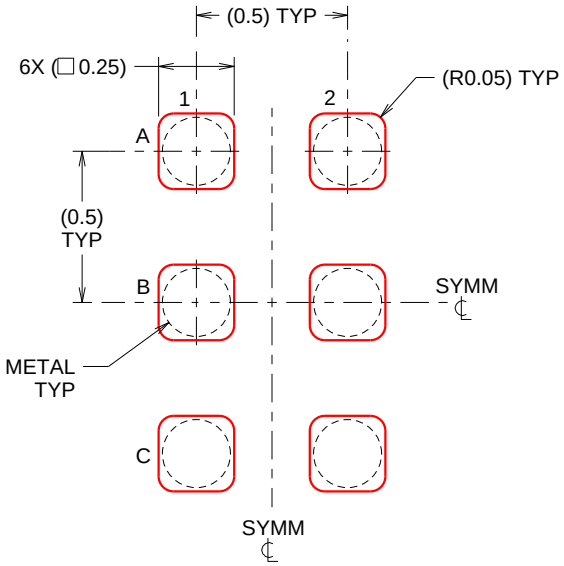



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

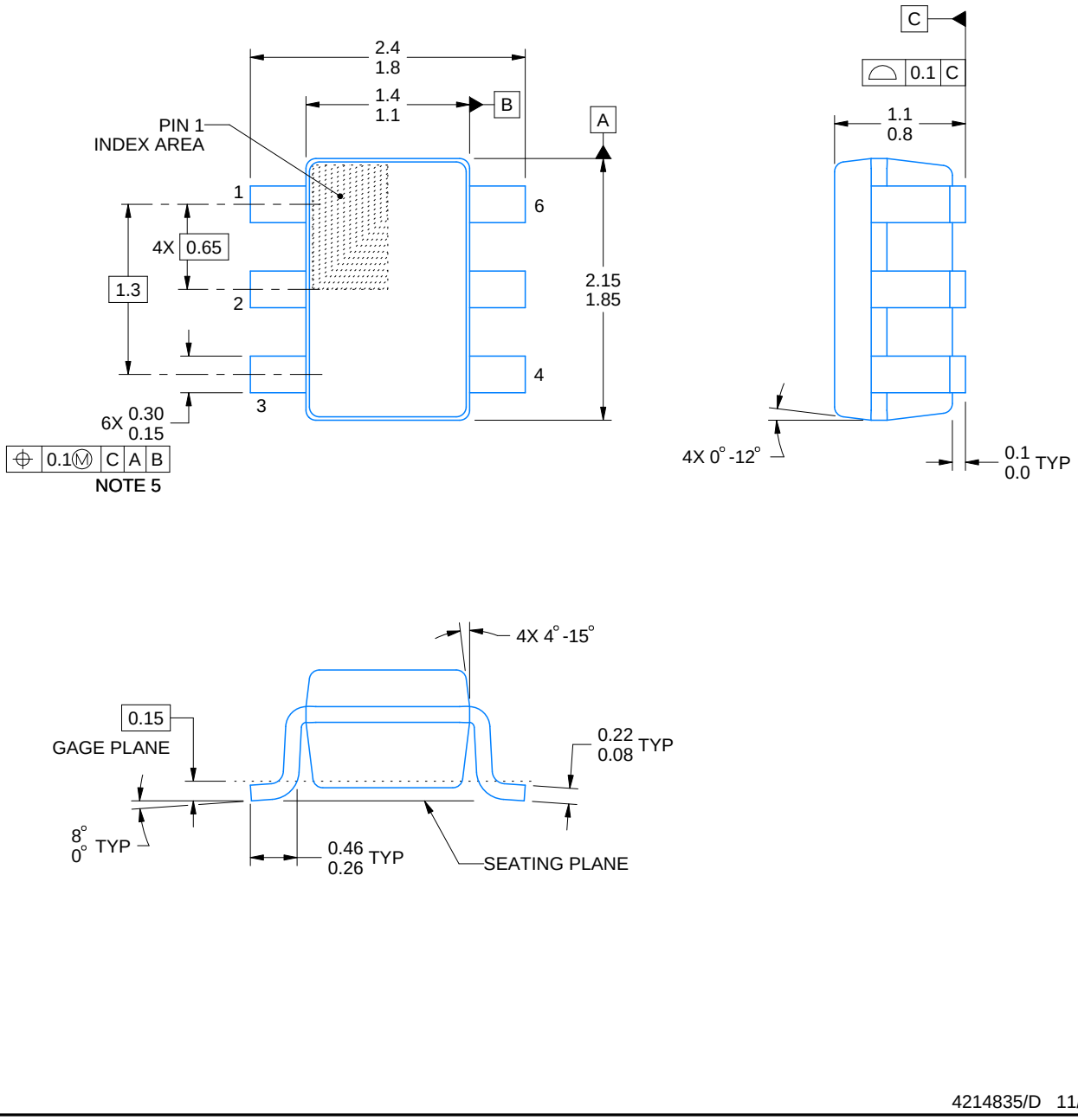
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DCK0006A

## SOT - 1.1 max height

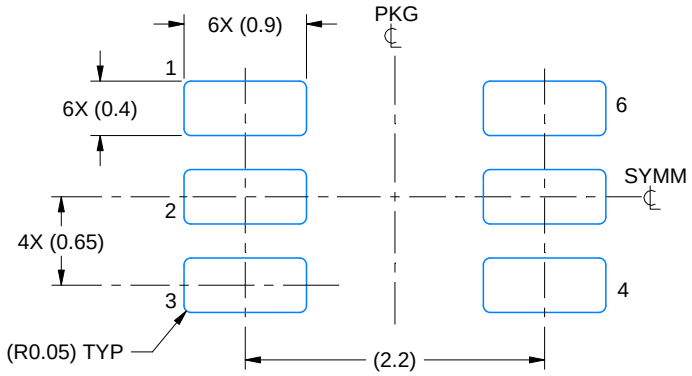
SMALL OUTLINE TRANSISTOR



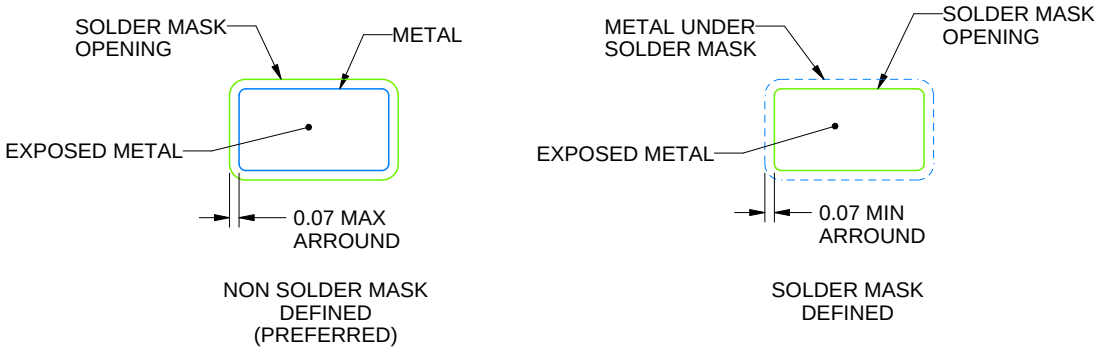

4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

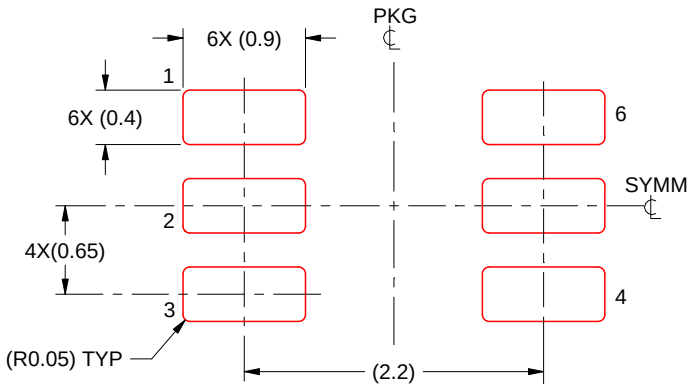



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

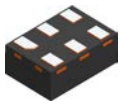
# DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

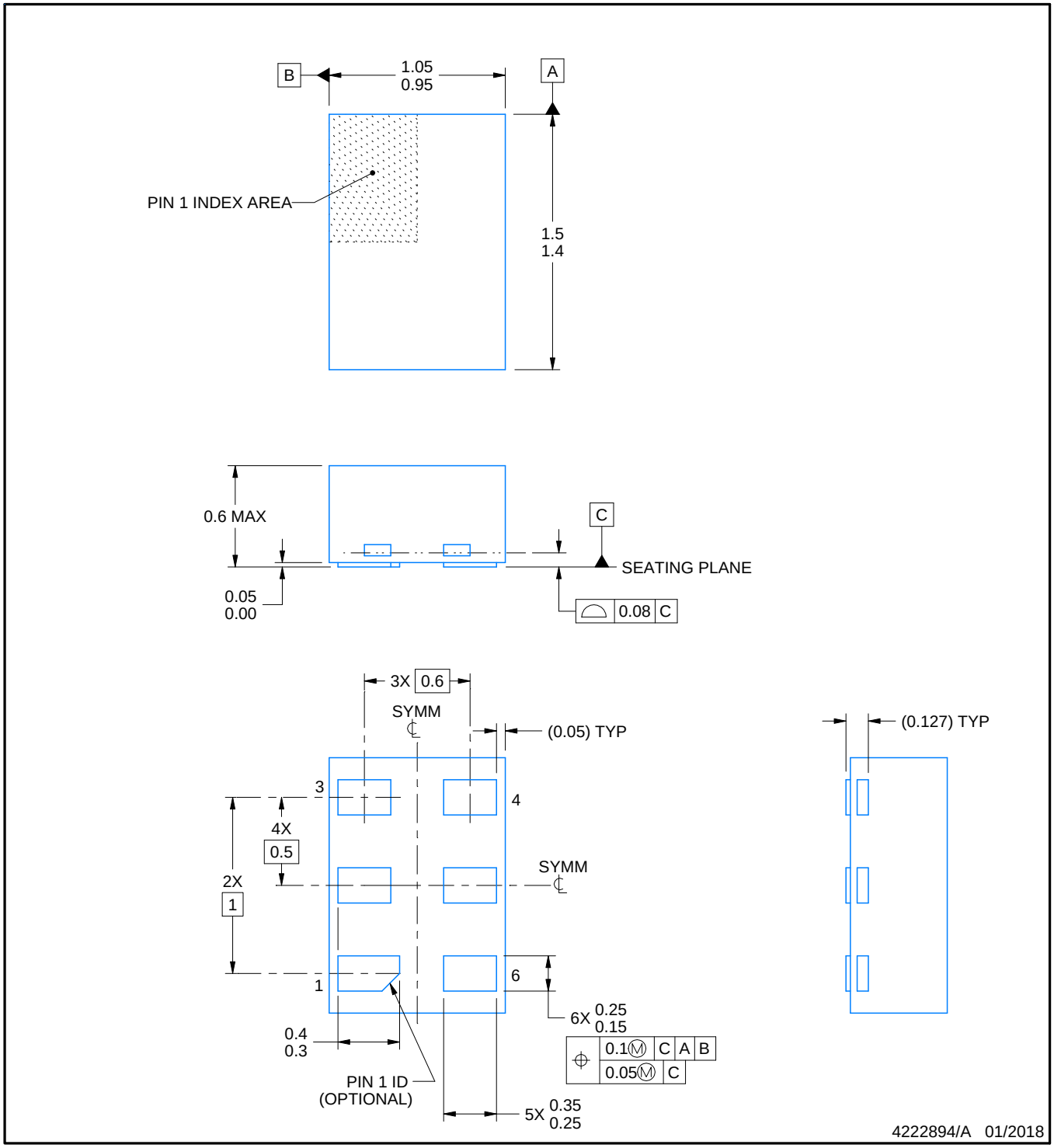
# DRY0006A



# PACKAGE OUTLINE

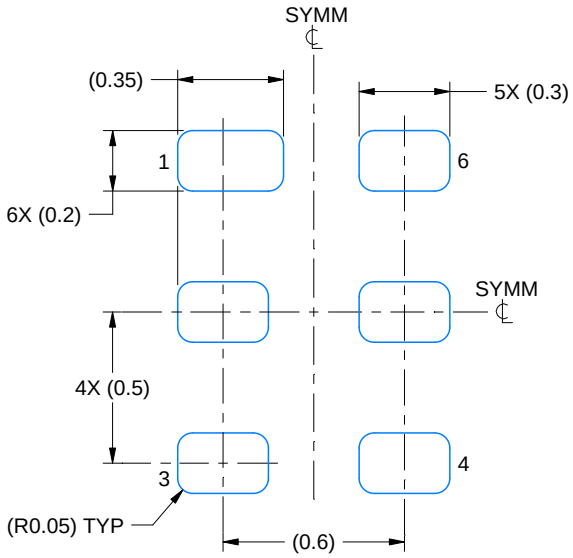
## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

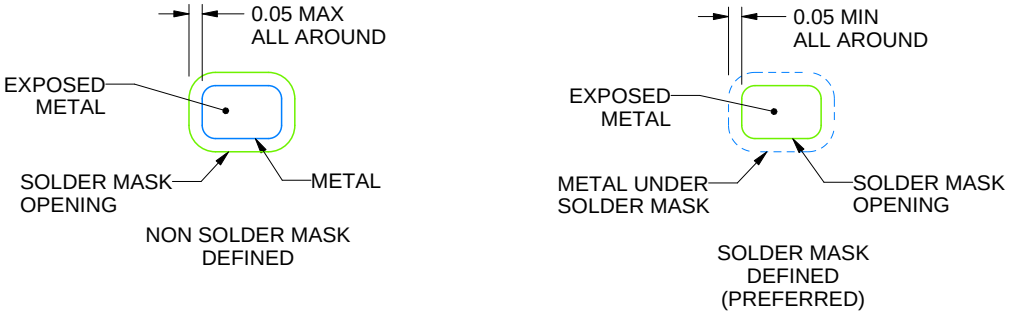



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

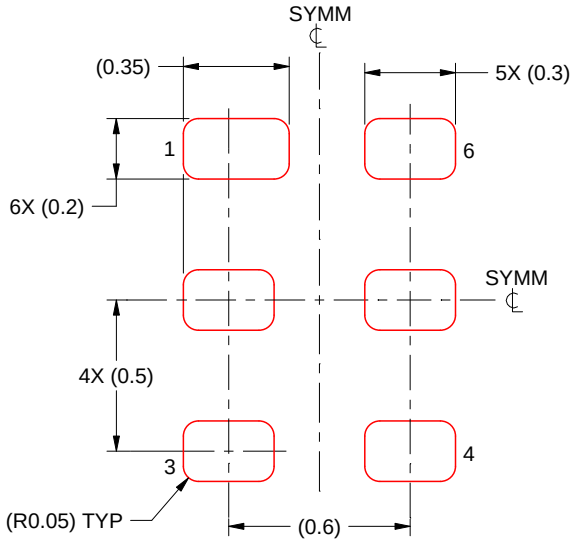
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

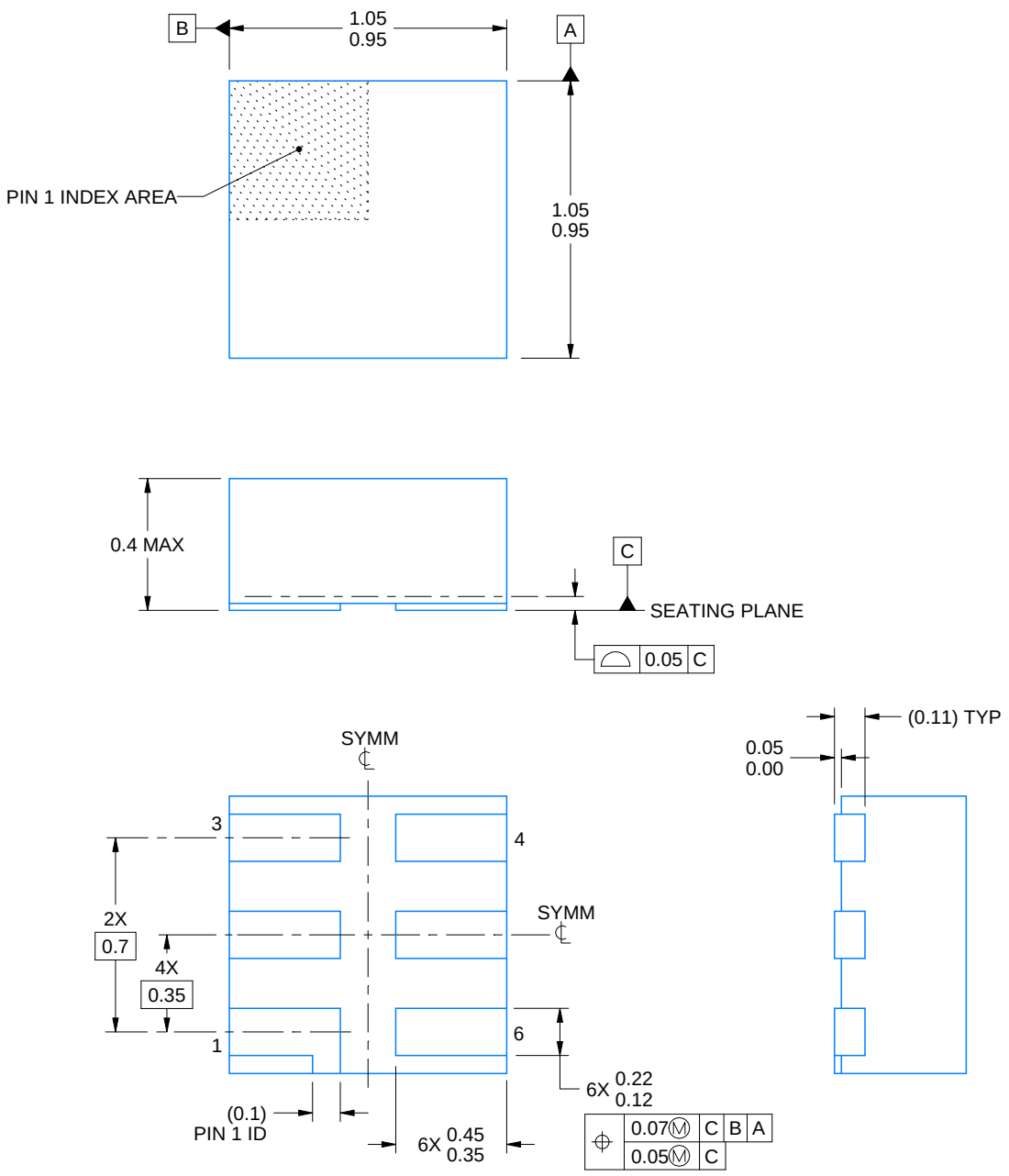
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DSF0006A

## X2SON - 0.4 mm max height

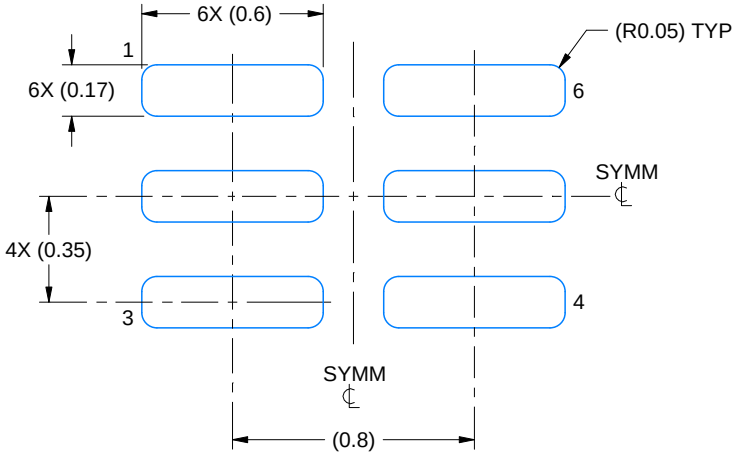
PLASTIC SMALL OUTLINE - NO LEAD



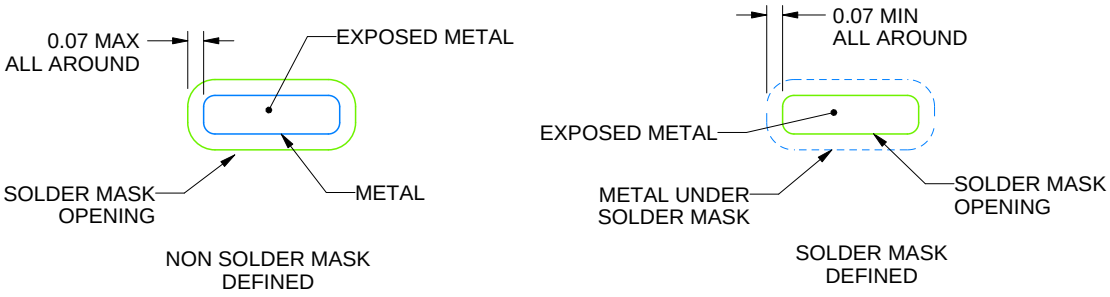

4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

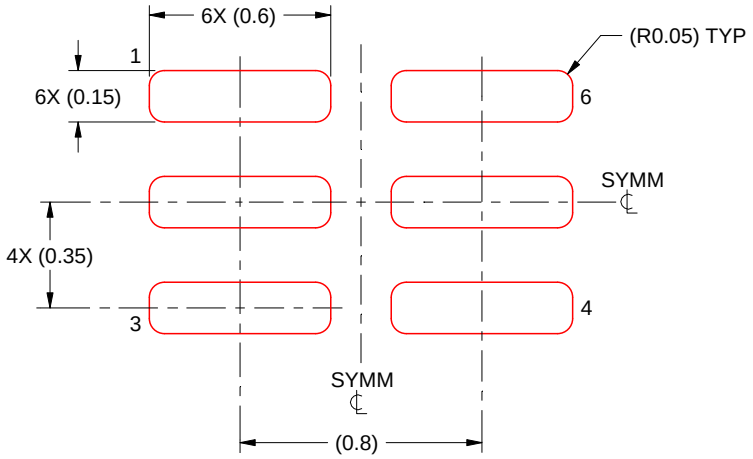
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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